EG800K-LA

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2024-05-23	Reuben WANG/ Kevin SU/ Yule DENG	Creation of the document
1.0.0	2024-05-23	Reuben WANG/ Kevin SU/ Yule DENG	Preliminary

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1 Introduction

This document defines the EG800K-LA module and describes its air interface and hardware interfaces which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

The module is an SMD type module with compact packaging, which is engineered to meet the demands in M2M applications.

Table 2: Basic Information

EG800K-LA	
Packaging type	LGA
Pin counts	109
Dimensions	(17.7 ±0.15) mm × (15.8 ±0.15) mm × (2.4 ±0.2) mm
Weight	Approx. 1.36 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Technology	EG800K-LA
LTE-FDD	B2/B3/B4/B5/B7/B8/B28/B66

2.2. Key Features

Table 4: Key Features

Feature	Capability
Supply Voltage	● Supply voltage range: 3.4–4.3 V ● Typical supply voltage: 3.8 V
SMS (optional)*	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: stored in USIM card and ME, ME by default ● SGS SMS (default)
USB Interface	● Compliant with USB 2.0 (slave mode only), with data transmission rates up to 480 Mbps ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● Supports USB serial drivers for Windows 8.1/10/11, Linux 2.6–6.7 and Android 4.x–13.x
USB_BOOT Interface	Supports one forced download interface
USIM Interface	Supports 1.8 V and 3.0 V USIM card
UART	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for log output ● Baud rate: 115200 bps **Auxiliary UART*:** ● Used for communication with peripherals ● Baud rate: 115200 bps
I2C Interface*	● Supports one I2C interface ● Complies with I2C-bus specification
ADC Interfaces*	Supports two ADC interfaces
Network Indication	NET_STATUS: indicates network registration status
AT Commands	Compliant with *3GPP TS 27.007, 3GPP TS 27.005* and Quectel enhanced AT commands
Antenna Interface	● Main antenna/Wi-Fi Scan antenna interface (ANT_MAIN) ● 50 Ω characteristic impedance
Transmitting Power	LTE-FDD: Class 3 (23 dBm ±2 dB)

LTE Features	● Supports 3GPP Rel-13 Cat 1 bis FDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports UL QPSK, 16QAM ● Supports DL QPSK, 16QAM, 64QAM ● LTE-FDD maximum data rates: – DL: 10 Mbps – UL: 5 Mbps
Position Fixing*	Supports Wi-Fi Scan (shares the main antenna)
Internet Protocol Features [1]	● Compliant with TCP/UDP/PPP*/NTP/NITZ/FTP*/HTTP*/PING/CMUX*/ HTTPS*/FTPS*/SSL/FILE*/MQTT/MMS*/SMTP*/SMTPS* protocols ● Support PAP and CHAP for PPP connections
Temperature Ranges	● Normal operating temperature [2]: -35 °C to +75 °C ● Extended temperature [3]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	Use USB 2.0 interface or DFOTA to upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive

NOTE

The 6.0 and above version QFlash tool must be used for firmware upgrade.

[1] PPP, FTP, HTTP, PING, CMUX*, HTTPS, FTPS, FILE, MQTT, MMS*, SMTP* and SMTPS* protocols are optional. PAP and CHAP for PPP connections are optional. For more details, please contact Quectel Technical Support.
[2] Within this range, the module's indicators comply with 3GPP specification requirements.
[3] Within this range, the module retains the ability to establish and maintain functions such as SMS*, data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

2.3. Pin Assignment

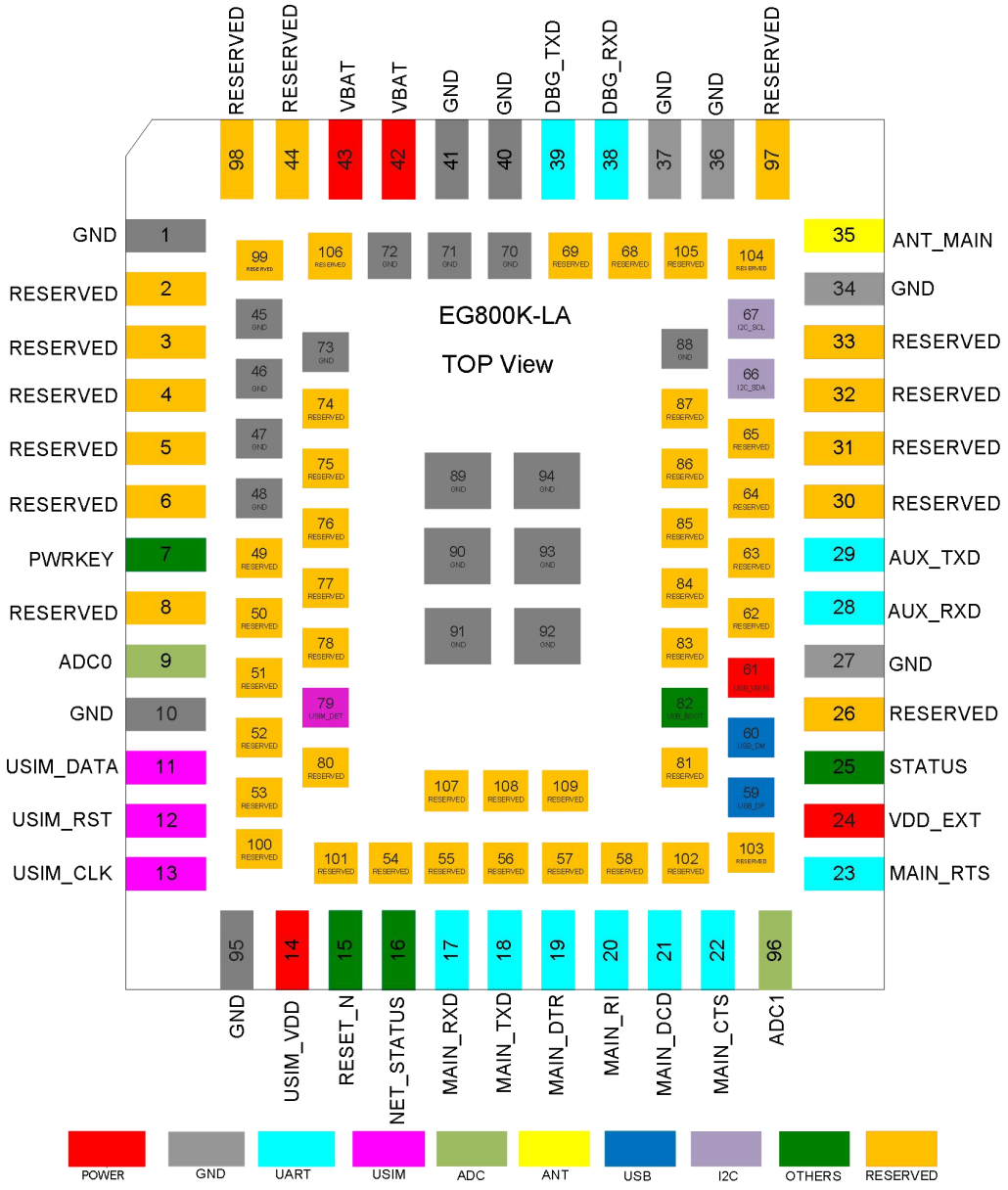


Figure 1: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins and unused pins open. Connect all GND pins to the ground.
2. Do not pull USB_BOOT to low level before the module starts up successfully.
3. Ensure that there is a complete reference ground plane under the module, and the plane shall be placed as close to the module layer as possible. Ensure that there are no other traces on the first layer under the module. And at least four-layer board design is recommended.

4. The 6.0 and above version QFlash tool must be used for firmware upgrading.

2.4. Pin Description

Table 5: Parameter Definition

Parameters	Descriptions
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 6: Pin Description

Power Supply Input					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Power supply for the module	Vmax = 4.3 V Vmin = 3.4 V Vnom = 3.8 V	External power supply must be provided with sufficient current of at least 2.0 A. It is recommended to add a TVS externally. Test points are recommended to be reserved.

GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95				
Power Supply Output					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_EXT	24	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. A test point is recommended to be reserved.
Turn On/Off/Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	V_{IL}max = 0.5 V Vnom = VBAT	Pull down PWRKEY for at least 700 ms to turn on/off the module. A test point is recommended to be reserved.
RESET_N	15	DI	Reset the module	V_{IL}max = 0.5 V Vnom = 1.8 V	Active Low. A test point is recommended to be reserved if unused.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_STATUS	16	DO	Indicate the module's network activity status	1.8 V	If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_DP	59	AIO	USB 2.0 differential data (+)		Complies with USB 2.0. A 90 Ω differential impedance is needed. Test points must be reserved.
USB_DM	60	AIO	USB 2.0 differential data (-)		

USB_VBUS	61	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DATA	11	DIO	USIM card data	1.8/3.0 V	
USIM_RST	12	DO	USIM card reset		
USIM_CLK	13	DO	USIM card clock		
USIM_VDD	14	PO	USIM card power supply		Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM_DET	79	DI	USIM card hot-plug detect	1.8 V	If unused, keep it open.
Auxiliary UART*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_RXD	28	DI	Auxiliary UART receive	1.8 V	If unused, keep them open.
AUX_TXD	29	DO	Auxiliary UART transmit		
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RXD	17	DI	Main UART receive	1.8 V	If unused, keep them open.
MAIN_TXD	18	DO	Main UART transmit		
MAIN_DTR	19	DI	Main UART data terminal ready		
MAIN_RI	20	DO	Main UART ring indication		
MAIN_DCD	21	DO	Main UART data carrier detect		
MAIN_CTS	22	DO	Clear to send signal from the module		Connect to the MCU's CTS. If unused, keep it open.

MAIN_RTS	23	DI	Request to send signal to the module		Connect to the MCU's RTS. If unused, keep it open.
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	38	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	39	DO	Debug UART transmit		
I2C Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SDA	66	OD	I2C serial data		An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SCL	67	OD	I2C serial clock		
Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	35	AIO	Main antenna/ Wi-Fi Scan antenna interface		50 Ω characteristic impedance.
ADC Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	9	AI	General-purpose ADC interface	0–1.2 V	If unused, keep them open.
ADC1	96	AI			
Other Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	82	DI	Force the module into download mode	1.8 V	Active low. It cannot be pulled down to low level before the module starts up successfully. A test point is recommended to be reserved.

RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	2–6, 8, 26, 30–33, 44, 49–58, 62–65, 68, 69, 74–78, 80, 81, 83–87, 97–109	Keep them open.

NOTE

1. Keep all RESERVED pins and unused pins open. Connect all GND pins to the ground.
2. Do not pull USB_BOOT to low level before the module starts up successfully.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Modes	Functions	
Full Functionality Mode	Idle	Software is active. The module is registered on the network but has no data interaction with the network.
	Data	Network connection is ongoing. Power consumption is decided by the network setting and data transmission rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to the minimum functionality mode when the power is on. In this case, both RF function and USIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	Power consumption of the module will be reduced to a minimal level. The module can still receive paging, SMS*, voice call and TCP/UDP data from network.	
Power Down Mode	PMU shuts down the power supply. Software is not active. However, operating voltage connected to VBAT remains applied.	

NOTE

For more details about **AT+CFUN**, see ***document [2]***.

3.2. Sleep Mode

In sleep mode, power consumption of the module can be reduced to an ultra-low level. The following sub-chapters describe how to let the module enter sleep mode.

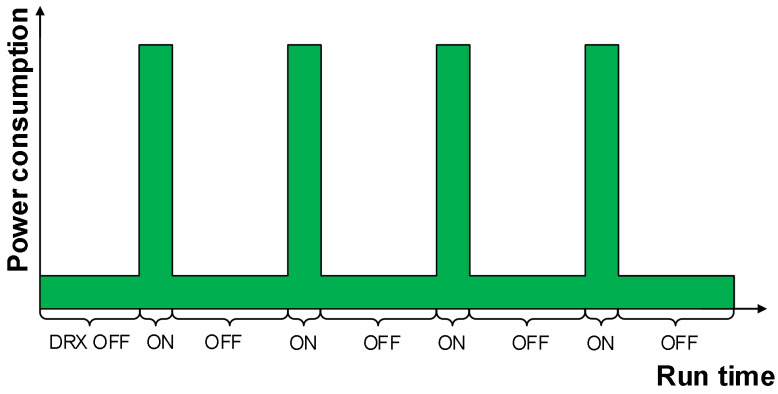


Figure 2: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. UART Application Scenario

If the module communicates with the MCU via MAIN_UART, both the following two preconditions should be met to set the module to enter sleep mode:

- Execute **AT+QSCLK=1**.
- Drive MAIN_DTR to high level or keep it open.

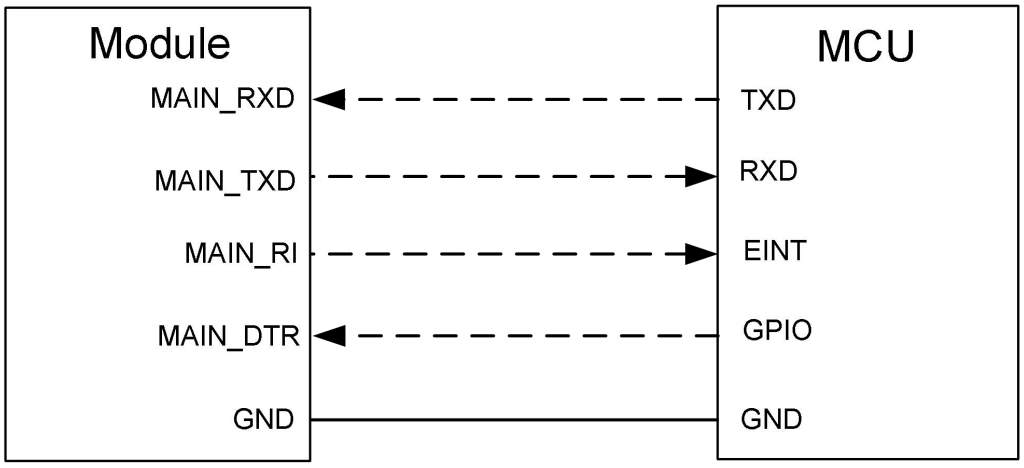


Figure 3: Block Diagram of UART Application in Sleep Mode

- You can wake up the module by driving MAIN_DTR low by the MCU.
- When the module has a URC to report, MAIN_RI signal will wake up the MCU. See ***Chapter 4.7.3*** for details about MAIN_RI.

3.2.2. USB Application Scenario

For the two situations ("USB application with USB remote wakeup function" and "USB application with USB Suspend/Resume and RI function") below, three preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held at a high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters into Suspend state.

3.2.2.1. USB Application with USB Remote Wakeup Function*

The host supports USB Suspend/Resume and remote wakeup functions.

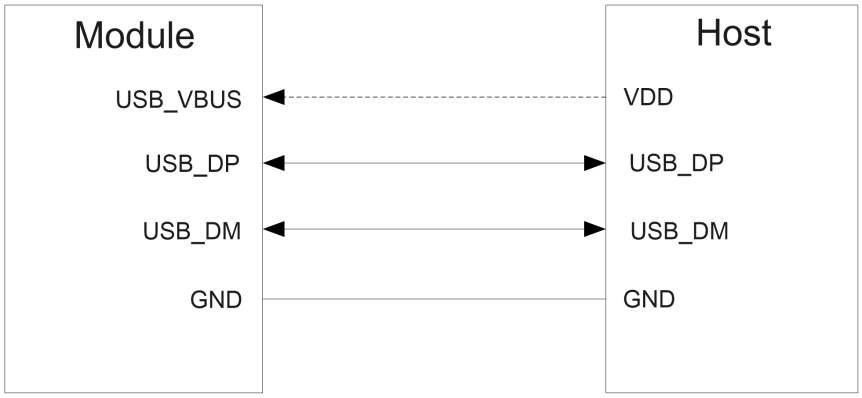


Figure 4: Block Diagram of Application with USB Remote Wakeup Function in Sleep Mode

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.2.2.2. USB Application with USB Suspend/Resume and RI Function*

If the host supports USB Suspend/Resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

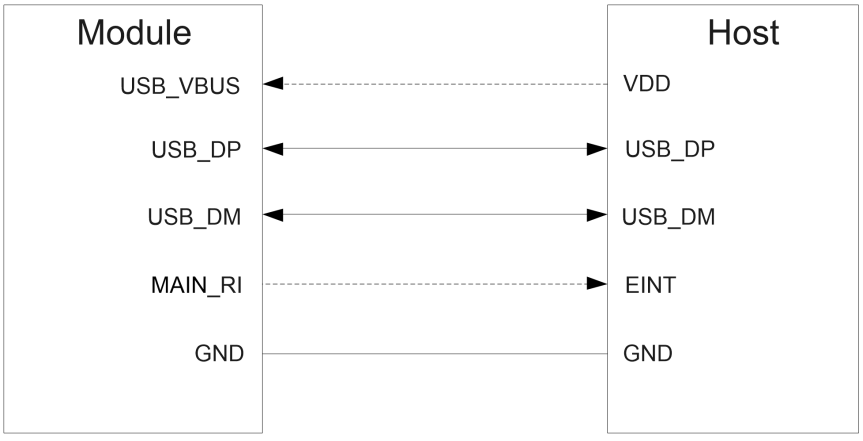


Figure 5: Block Diagram of Application with MAIN_RI Function in Sleep Mode

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN_RI signal. See ***Chapter 4.7.3*** for details about MAIN_RI.

3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB Suspend function, the following three preconditions must be met to let the module enter sleep mode:

- Execute **AT+QSCLK=1**.
- Drive MAIN_DTR to high level or keep it open.
- Disconnect USB_VBUS via the Power Switch.

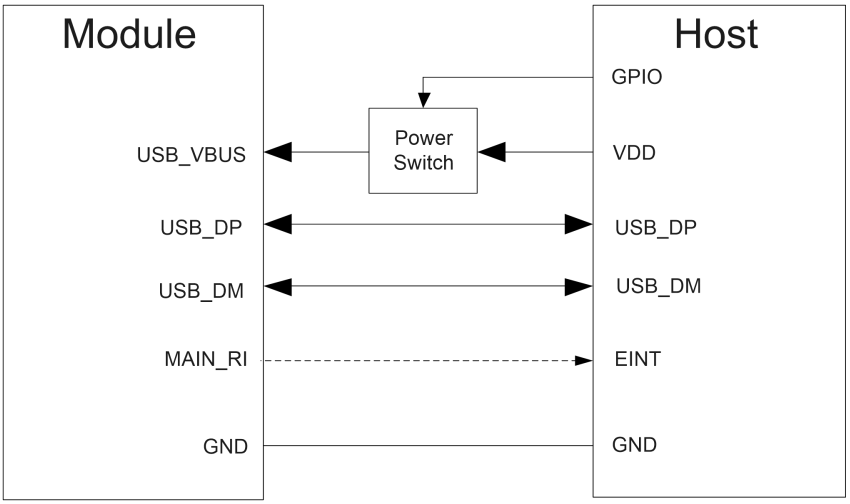


Figure 6: Block Diagram of Application without USB Suspend Function in Sleep Mode

Restore the power supply of USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level matching represented by the dotted line between the module and the host/MCU.
2. For more details about AT commands, see ***document [2]***.

3.3. Airplane Mode

When the module enters into airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via following ways:

Software:

AT+CFUN=<fun> provides choices of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality (disable RF function and USIM function).
- **AT+CFUN=1:** Full functionality (default).
- **AT+CFUN=4:** Airplane mode (disable RF function).

NOTE

For more details about AT commands, see ***document [2]***.

3.4. Power Supply

3.4.1. Power Supply Interface

The module provides two VBAT pins dedicated for connection with the external power supply:

Table 8: Pin Description of Power Supply Interface

Pin Name	Pin No.	I/O	Description	Comment
VBAT	42, 43	PI	Power supply for the module	External power supply must be provided with sufficient current of at least 2.0 A. It is recommended to add a TVS externally. Test points are recommended to be reserved.
GND	1, 10, 27, 34, 36, 37, 40, 41, 45–48, 70–73, 88–95			

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 2 A. If the voltage difference between input voltage and the desired output VBAT is small, it is suggested to use an LDO; if the voltage difference is large, then a buck converter is suggested to use.

The following figure illustrates a reference design for 5 V input power supply.

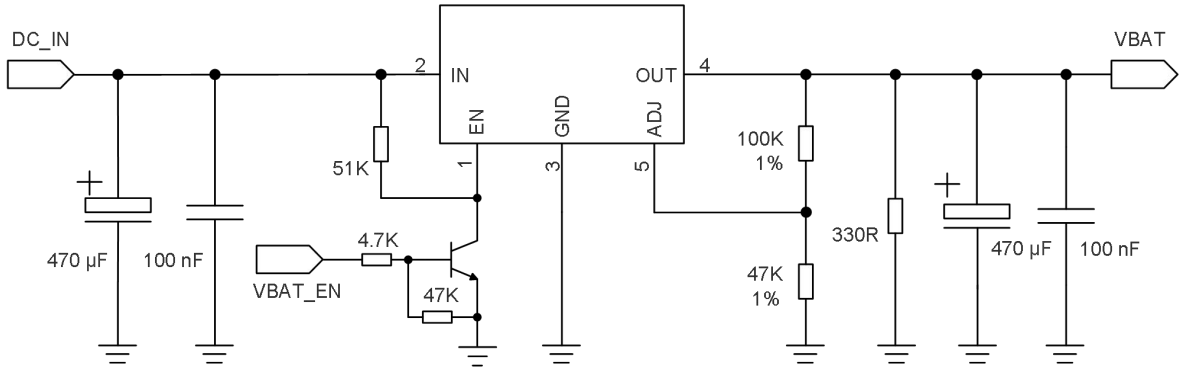


Figure 7: Reference Design of Power Input

NOTE

To avoid corrupting internal flash, do not cut off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.

3.4.3. Power Supply Voltage Detection

Use **AT+CBC*** to monitor or read VBAT voltage. For more details, see ***document [2]***.

3.4.4. Requirements for Voltage Stability

The power supply range of the module is from 3.4 V to 4.3 V. Ensure the input voltage never drops below 3.4 V.

To decrease the voltage drop, a bypass capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω) should be used, and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR. Use five ceramic capacitors (1.8 pF, 3.9 pF ,10 pF, 33 pF and 100 nF) for composing the MLCC array and a 0 Ω resistor for future debugging (resistance package is not less than 0603), and place these capacitors close to VBAT pins. The main power supply from an external application should be a single voltage source. The width of VBAT trace should be not less than 2 mm respectively. As per design rules, the longer the VBAT trace is, the wider it should be.

In order to avoid the ripple and surge and ensure the stability of the power supply to the module, add a TVS with V_{RWM} = 4.7 V, low-clamp voltage and peak pulse current Ipp at the front end of the power supply.

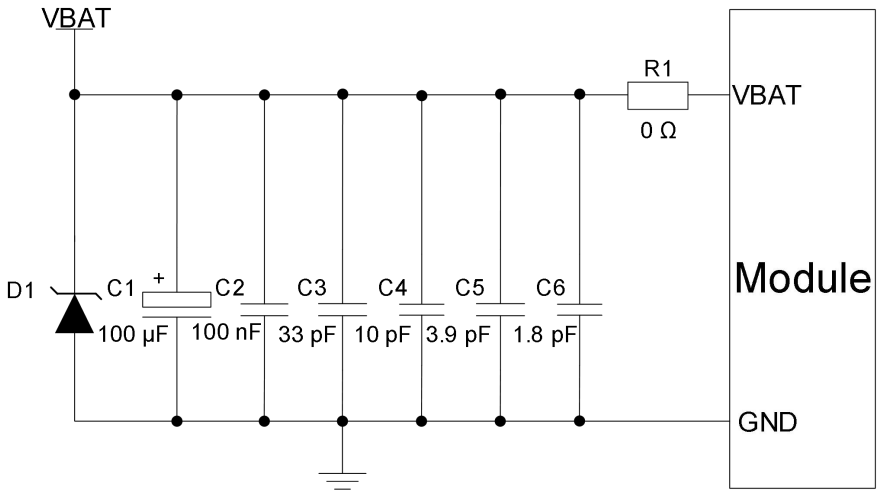


Figure 8: Reference Design of Power Supply

3.5. Turn-on

3.5.1. Turn-on with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	Pull down PWRKEY for at least 700 ms to turn on/off the module. A test point is recommended to be reserved.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 700 ms. It is recommended to use an open drain/collector driver to control PWRKEY.

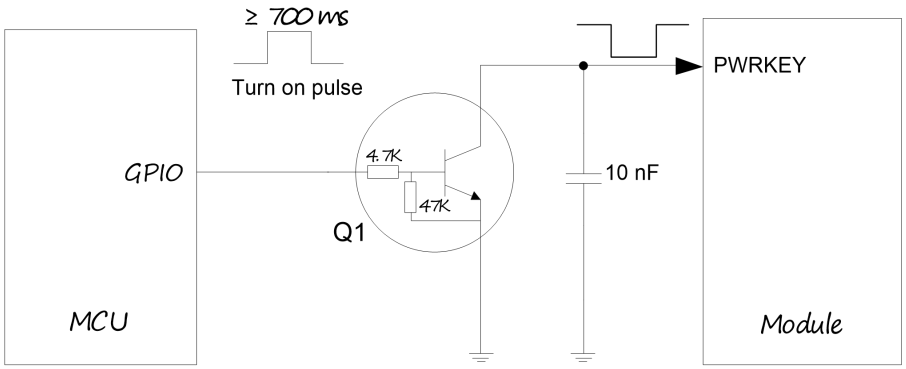


Figure 9: Reference Design of Turn-on with Driving Circuit

Another way to control PWRKEY is by using a push button directly. When pressing the button, an electrostatic

strike may be generated from finger. Therefore, a TVS should be placed near the push button for ESD protection.

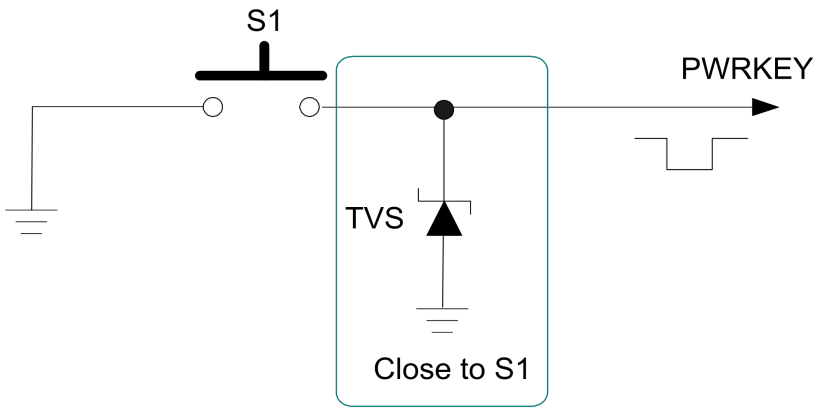


Figure 10: Reference Design of Turn-on with a Button

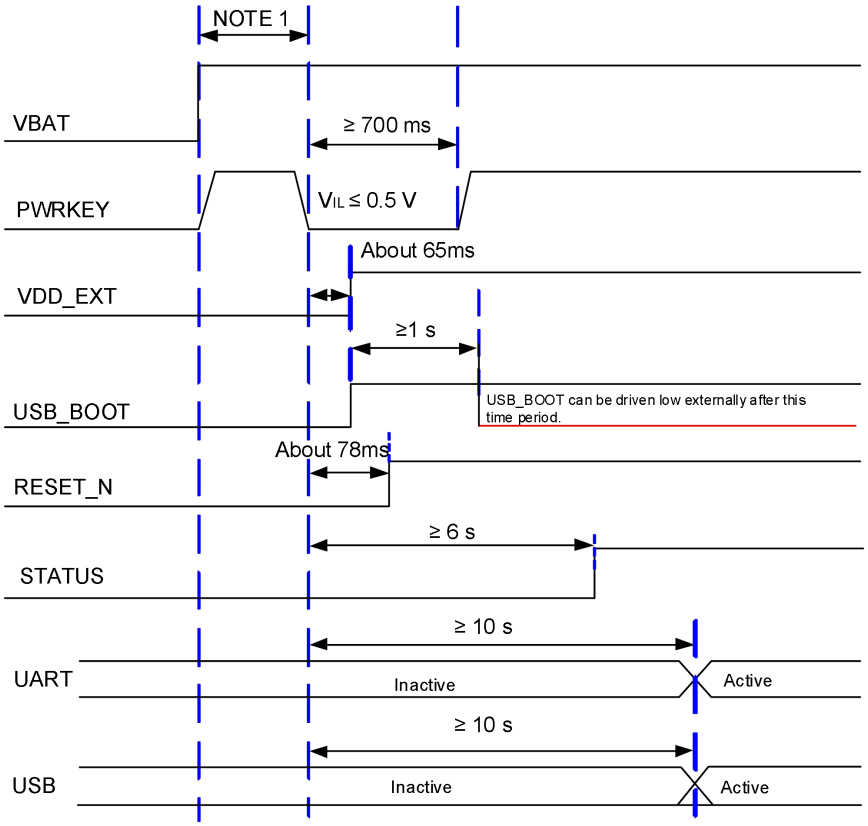


Figure 11: Timing of Turn-on with PWRKEY

NOTE

1. Ensure that VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need power-off function, PWRKEY can be driven low directly to ground with a recommended 1 kΩ resistor.

3.6. Turn-off

3.6.1. Turn-off with PWRKEY

Drive PWRKEY low for at least 650 ms and then release it, the module will execute power-down procedure.

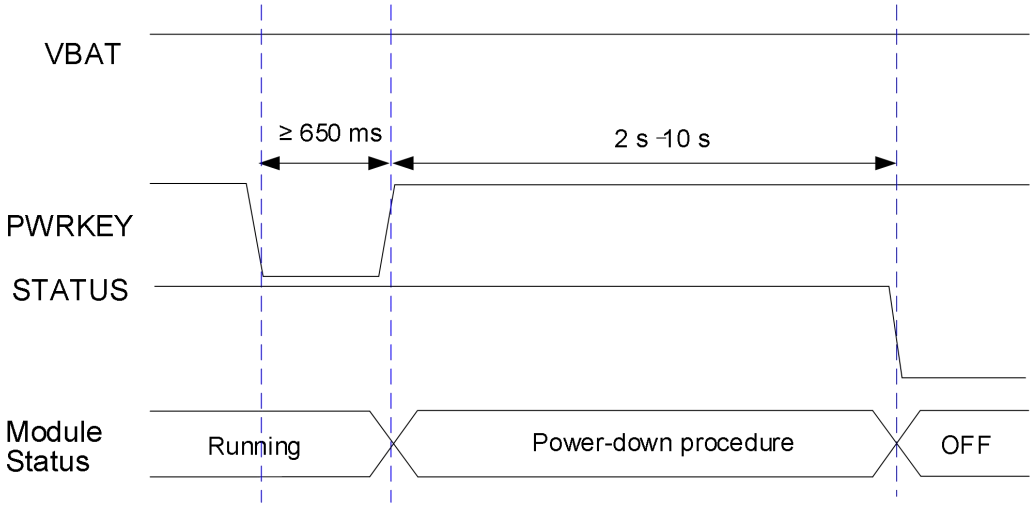


Figure 12: Timing of Turn-off with PWRKEY

3.6.2. Turn-off with AT Command

For proper shutdown procedure, execute **AT+QPOWD** which has similar timing and effect as turning off the module through driving PWRKEY low. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not cut off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command, can you cut off the power supply.
2. After executing the power off commands, keep the PWRKEY at high level, otherwise the module will be turned on again automatically after successful power-off.

3.7. Reset

Drive RESET_N low for at least 300 ms and then release it can reset the module. RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	15	DI	Reset the module	Active Low. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to PWRKEY control circuit, you can use open drain/collector driver or button to control RESET_N.

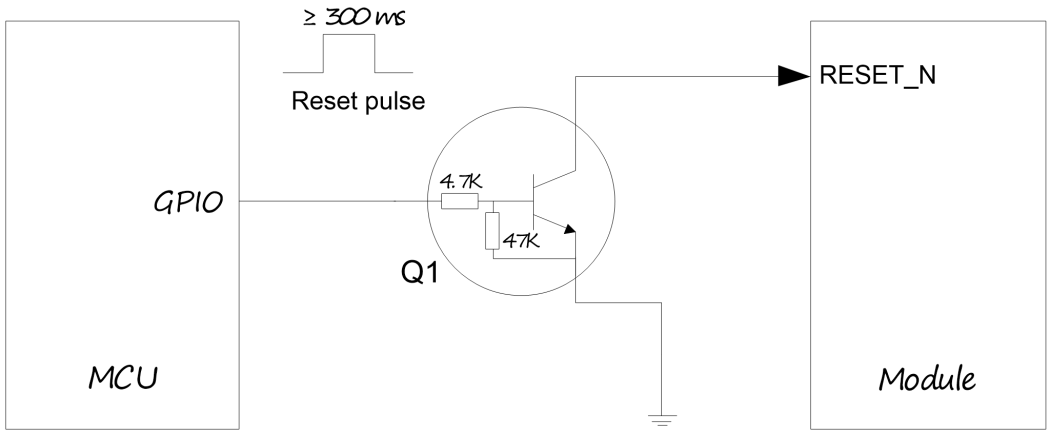


Figure 13: Reference Design of Reset with Driving Circuit

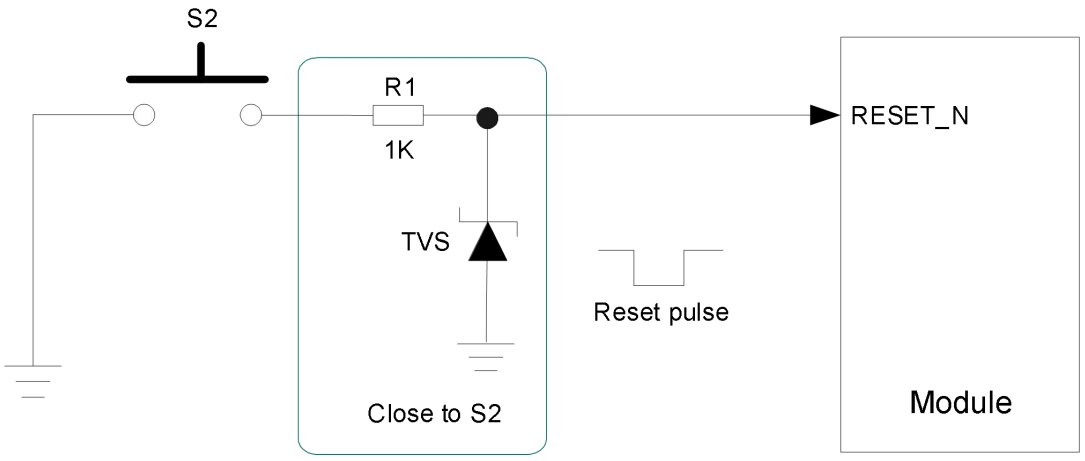


Figure 14: Reference Design of Reset with a Button

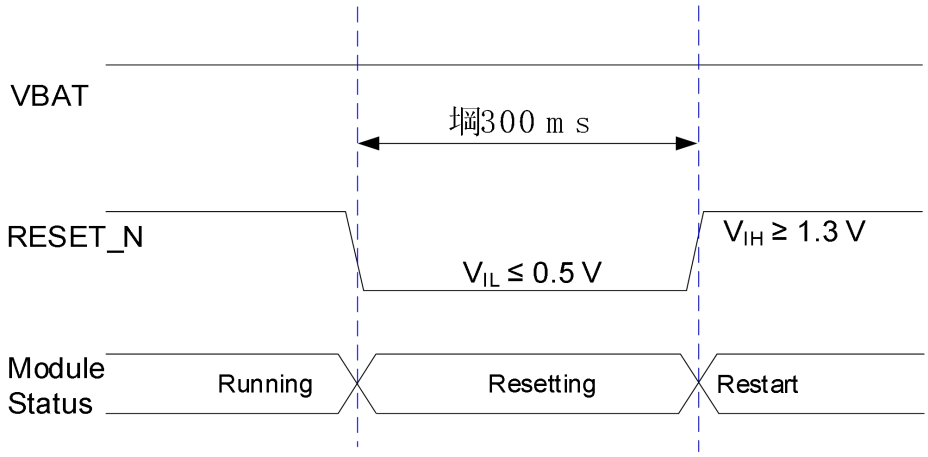


Figure 15: Timing of Reset

NOTE

1. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
2. Ensure the capacitance on PWRKEY and RESET_N does not exceed 10 nF.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specifications and supports High-Speed (480 Mbps) and Full-Speed (12 Mbps) on USB 2.0. The USB interface can be used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 11: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_DP	59	AIO	USB 2.0 differential data (+)	Complies with USB 2.0. A 90 Ω differential impedance is needed. Test points must be reserved.
USB_DM	60	AIO	USB 2.0 differential data (-)	
USB_VBUS	61	AI	USB connection detect	Typical value is 5.0 V. A test point must be reserved.

It is recommended to use USB 2.0 interface for firmware upgrading and reserve test points for debugging.

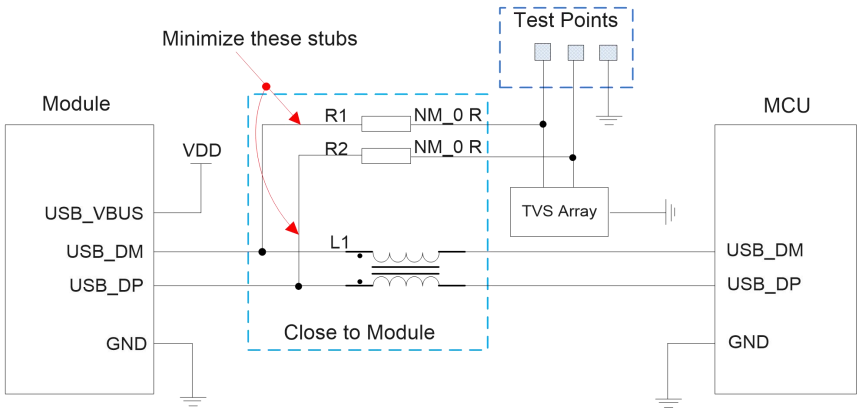


Figure 16: Reference Design of USB 2.0 Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI. Meanwhile, it is also suggested to add R1 and R2 in series between the module and test points for debugging.

These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, L1, R1 and R2 should be placed close to the module, and resistors should be placed close to each other. Extra stubs of trace should be kept as short as possible.

To ensure performance, the following principles should be complied with when designing USB interface:

- The impedance of USB differential trace is 90 Ω.
- Route USB differential traces in the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Do not route signal traces under VBAT traces, crystal-oscillators, magnetic devices, sensitive circuits and provide clearance from RF signals, analog signals, and noise signals generated by clock and DC-DC.
- Pay attention to the impact caused by junction capacitance of the ESD protection component on USB data traces. Typically, junction capacitance should be less than 2 pF.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. USB_BOOT Interface

The module provides a USB_BOOT for forced download. You can make the module enter forced download mode by driving USB_BOOT low to GND before turning on the module. In this mode, the module supports firmware upgrade over USB 2.0 interface with shorter time period.

Table 12: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	82	DI	Force the module into download mode	Active low. It cannot be pulled down to low level before the module starts up successfully. A test point is recommended to be reserved.

The following figure shows a reference design of USB_BOOT interface.

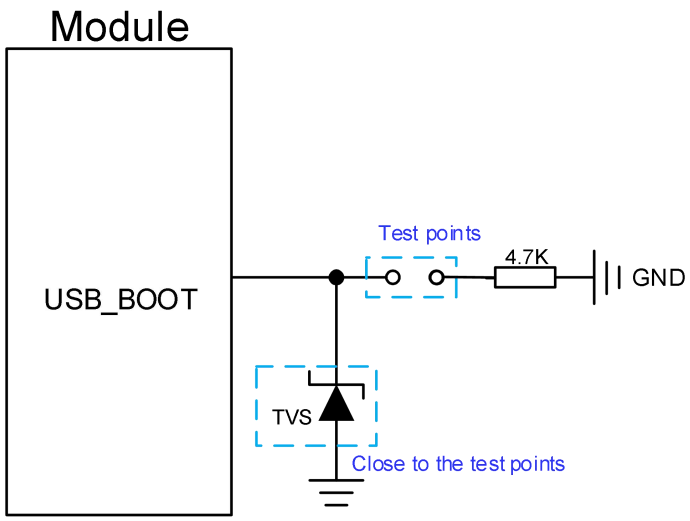


Figure 17: Reference Design of USB_BOOT

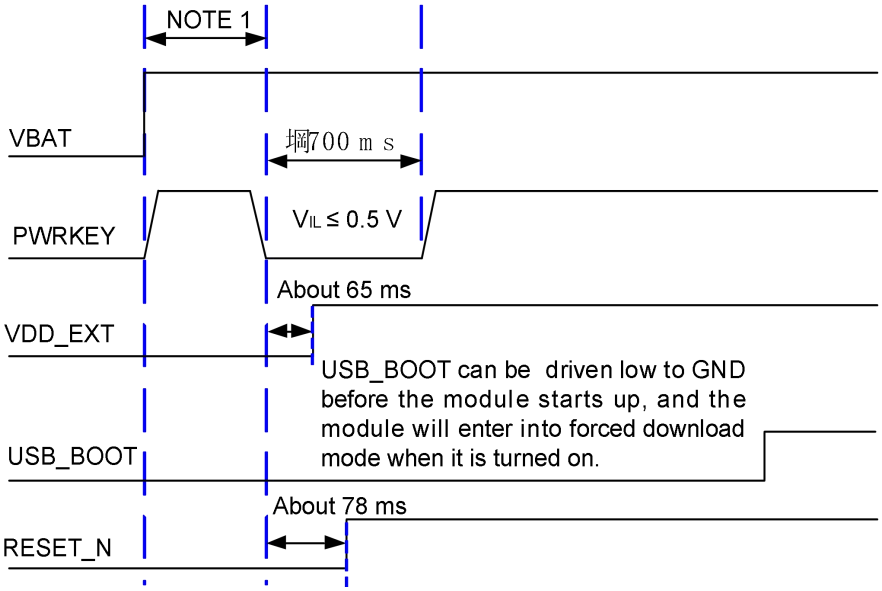


Figure 18: Timing of Entering Forced Download Mode

NOTE

1. Ensure that VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low should be not less than 30 ms.
2. Follow the above timing when using MCU to control module to enter the forced download mode. Directly connect the test points as shown in ***Figure 17*** can manually force the module to enter download mode.
3. Drive USB_BOOT low to GND and the pull-down resistor is recommended to be 4.7 kΩ.

4. The 6.0 and above version QFlash tool must be used for firmware upgrading.

4.3. USIM Interface

The USIM interface meet ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V USIM card is supported.

Table 13: Pin Description of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DATA	11	DIO	USIM card data	
USIM_RST	12	DO	USIM card reset	
USIM_CLK	13	DO	USIM card clock	
USIM_VDD	14	PO	USIM card power supply	Either 1.8 V or 3.0 V USIM card is supported and can be identified automatically by the module.
USIM_DET	79	DI	USIM card hot-plug detect	If unused, keep it open.

The module supports USIM card hot-plug via USIM_DET (level trigger pin), and both high-level and low-level detections are supported. Hot-plug function is disabled by default, you can use **AT+QSIMDET** to configure this function. For more details, see ***document [2]***.

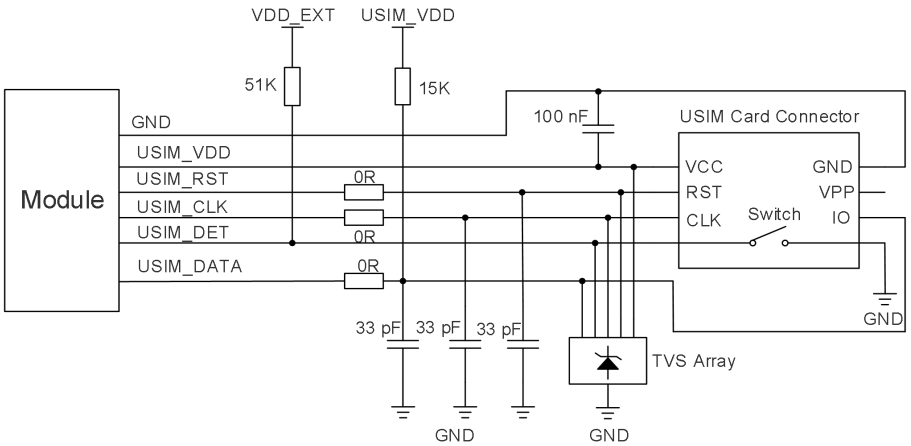


Figure 19: Reference Design of USIM Interface with an 8-pin USIM Card Connector

If the function of USIM card hot-plug is not needed, then keep USIM_DET open. A reference circuit for USIM interface with a 6-pin USIM card connector is illustrated in the following figure.

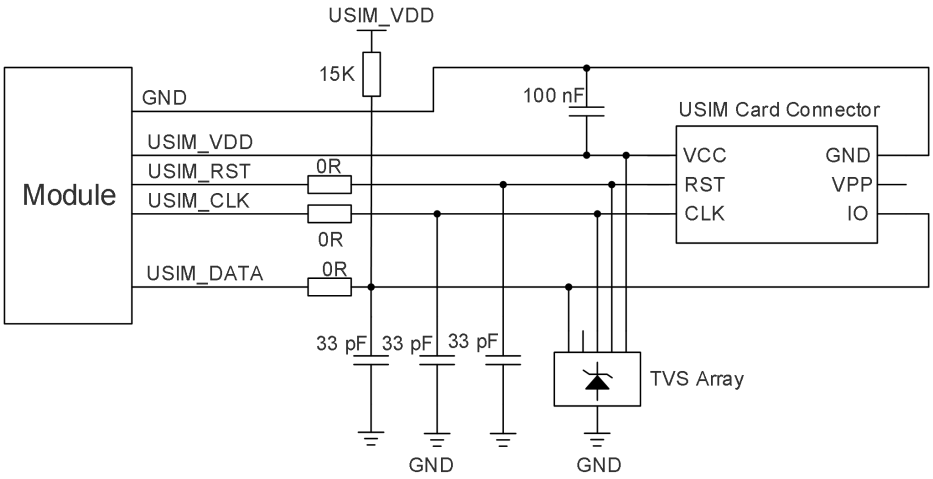


Figure 20: Reference Design of USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, you should follow the principles below in the USIM circuit design:

- Place USIM card connector close to the module. Keep the trace length less than 200 mm if possible.
- Keep USIM card signals away from RF and VBAT traces.
- Ensure the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be placed close to the USIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer better ESD protection, add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the USIM card to facilitate debugging. The 33 pF capacitors in parallel on USIM_DATA, USIM_CLK and USIM_RST traces are used for filtering RF interference. Additionally, keep the USIM peripheral circuit close to the USIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the USIM card. If the USIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the USIM card connector.

4.4. UART

The module provides three UARTs.

Table 14: Information of UARTs

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
Main UART	4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600	115200	Data transmission and AT command communication
Debug UART	115200	115200	Log output
Auxiliary UART*	115200	115200	Communication with peripherals

Table 15: Pin Description of UARTs

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RXD	17	DI	Main UART receive	If unused, keep them open.
MAIN_TXD	18	DO	Main UART transmit	
MAIN_DTR	19	DI	Main UART data terminal ready	
MAIN_RI	20	DO	Main UART ring indication	
MAIN_DCD	21	DO	Main UART data carrier detect	
MAIN_CTS	22	DO	Clear to send signal from the module	Connect to the MCU's CTS. If unused, keep it open.
MAIN_RTS	23	DI	Request to send signal to the module	Connect to the MCU's RTS. If unused, keep it open.
AUX_RXD*	28	DI	Auxiliary UART receive	If unused, keep them open.
AUX_TXD*	29	DO	Auxiliary UART transmit	
DBG_RXD	38	DI	Debug UART receive	Test points must be reserved.
DBG_TXD	39	DO	Debug UART transmit	

The module provides 1.8 V UART. You can use a voltage-level translator between the module and MCU's UART if the application is equipped with a 3.3 V UART. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design:

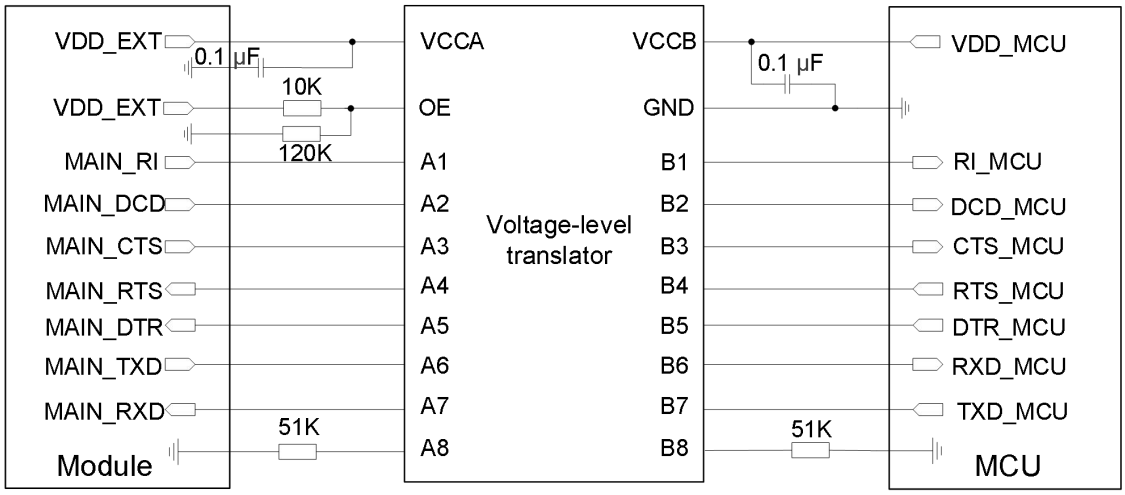


Figure 21: Reference Design of UART with a Voltage-level Translator

Another example of level-shifting circuit is shown as below. Refer to the solid line for input/output circuit design in the dotted line below, but remember to follow the input/output sequence from or towards the module.

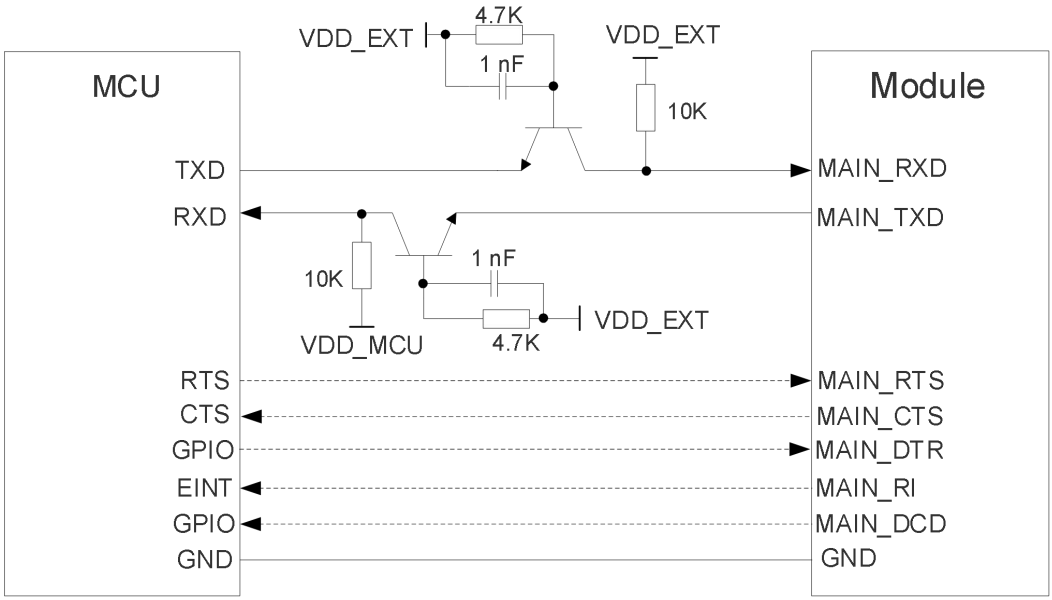


Figure 22: Reference Design of UART Interface with Transistor Circuit

NOTE

1. Transistor circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.

3. To increase the stability of UART communication, it is recommended to add UART hardware flow control design.

4.5. I2C Interface*

The module provides one I2C interface:

Table 16: Pin Description of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SDA	66	OD	I2C serial data	An external 1.8 V pull-up resistor is required. If unused, keep them open.
I2C_SCL	67	OD	I2C serial clock	

4.6. ADC Interfaces*

The module provides two ADC interfaces. To improve the accuracy of ADC, the trace of ADC interfaces should be surrounded by ground.

Table 17: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	9	AI	General-purpose ADC interface	If unused, keep them open.
ADC1	96	AI		

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

For more details about the AT command, see ***document [2]***.

Table 18: Characteristics of ADC Interfaces

Parameters	Min.	Typ.	Max.	Units

ADC0 voltage range	0	-	1.2	V
ADC1 voltage range	0	-	1.2	V
ADC resolution	-	-	12	bits

NOTE

1. A voltage divider with resistance of more than 100 kΩ must be used for ADC interface application.
2. The accuracy of the two resistors in each voltage divider affects the sampling error of the ADC. It is recommended to use resistors with an accuracy of 1 %; if the accuracy of the ADC needs to be higher, resistors with an accuracy of 0.5 % are recommended. See ***document [3]*** for details.

4.7. Indication Signal

Table 19: Pin Description of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	16	DO	Indicate the module's network activity status	If unused, keep them open.
STATUS	25	DO	Indicate the module's operation status	
MAIN_RI	20	DO	Main UART ring indication	

4.7.1. Network Status Indication

The module provides one network status indication pin: NET_STATUS for module's network registration status indication. This pin can be used to drive corresponding LED.

Table 20: Level Status and Module Network Status of Network Status Indication Pin

Pin Name	Level Status	Module Network Status
NET_STATUS	Blink slowly (200 ms high level/1800 ms low level)	Network searching
	Blink slowly (1800 ms high level/200 ms low level)	Idle
	Blink quickly (125 ms high level/125 ms low level)	Data transmission is ongoing

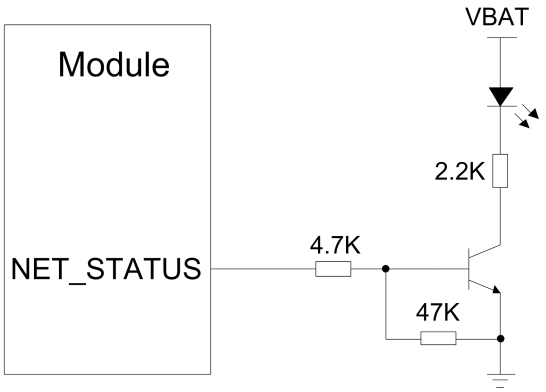


Figure 23: Reference Design of Network Status Indication

4.7.2. STATUS

STATUS indicates the module's operation status. It will output high level when module is turned on successfully.

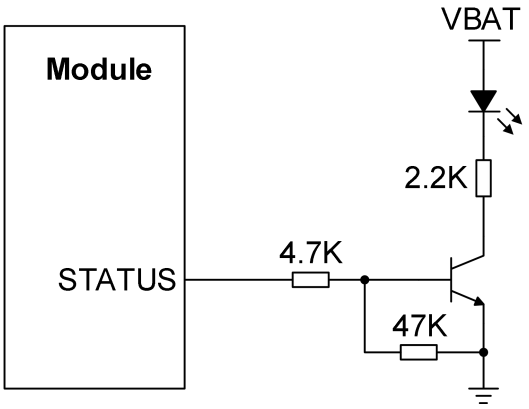


Figure 24: Reference Design of STATUS

4.7.3. MAIN_RI

AT+QCFG="risignaltype", "physical" can be used to configure the indication behavior for MAIN_RI. No matter on which port (main UART, USB AT port or USB modem port) a URC is presented, the URC will trigger the behavior of MAIN_RI.

NOTE

The **AT+QURCCFG** allows you to set main UART, USB AT port or USB modem port as the URC output port. The USB AT port is used to send AT commands by default.

MAIN_RI behaviors can be configured flexibly, and default behaviors are shown as below:

Table 21: MAIN_RI Level Status and Module Status

Module Status	MAIN_RI Level Status
Idle	High level
When a new URC return	MAIN_RI outputs at least 120 ms low level. After the module outputs the data, the level status will then become high.

Indication behavior of MAIN_RI can be configured via several commands, e.g. **AT+QCFG="urc/ri/ring"** can be used to specify the MAIN_RI behavior when the URC indicating an incoming call is reported. See ***document [2]*** for details.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. LTE/Wi-Fi Scan Antenna Interface

5.1.1. Antenna Interface & Frequency Bands

Table 22: Pin Description of LTE/Wi-Fi Scan Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	35	AIO	Main antenna/ Wi-Fi Scan antenna interface	50 Ω characteristic impedance.

NOTE

The module supports Wi-Fi Scan* function. Wi-Fi Scan* that only supports receiving, shares the same antenna interface with main antenna. The two functions cannot be used at the same time.

Table 23: Operating Frequency (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B2	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1754.9	2110–2154.9
LTE-FDD B5	824–849	869–894
LTE-FDD B8	880–915	925–960
LTE-FDD B7	2500–2570	2620–2690

LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710-1779.9	2110-2179.9

5.1.2. Tx Power

Table 24: RF Transmitting Power

Frequency	Max.	Min.
LTE-FDD B2/B3/B4/B5/B7/B8/B28/B66	23 dBm ±2 dB	< -39 dBm

5.1.3. Rx Sensitivity

Table 25: Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO	
LTE-FDD B2 (10 MHz)	TBD	-	-	-94.3
LTE-FDD B3 (10 MHz)	TBD	-	-	-93.3
LTE-FDD B4 (10 MHz)	TBD	-	-	-96.3
LTE-FDD B5 (10 MHz)	TBD	-	-	-94.3
LTE-FDD B7 (10 MHz)	TBD	-	-	-94.3
LTE-FDD B8 (10 MHz)	TBD	-	-	-93.3
LTE-FDD B28 (10 MHz)	TBD	-	-	-94.8
LTE-FDD B66 (10 MHz)	TBD	-	-	-96.5

5.1.4. Reference Design

Use a π-type matching circuit for all the antenna interfaces for better cellular performance. Capacitors are not mounted by default.

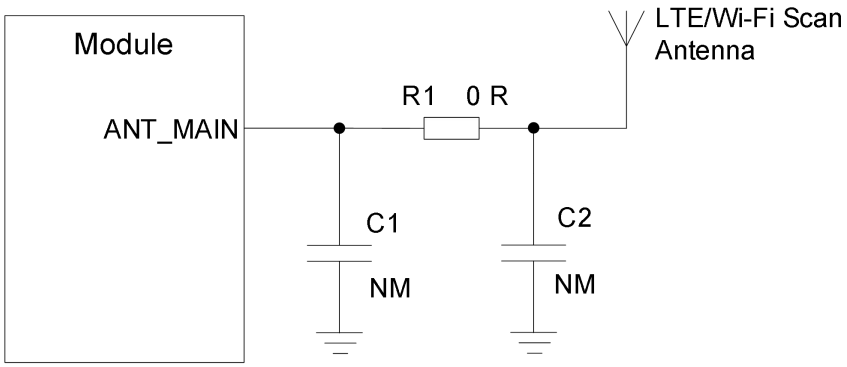


Figure 25: Reference Design of LTE/Wi-Fi Scan Antenna

NOTE

1. To reduce the coexistence problems and avoid the interference of receiving sensitivity, make sure that the isolation between antennas is not less than 20 dB.
2. Place the π-type matching components (R1, C1, C2) as close to antennas as possible.

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

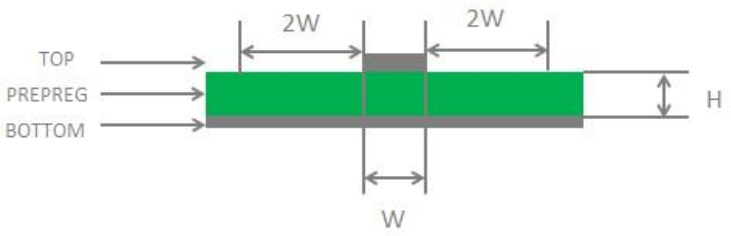


Figure 26: Microstrip Design on a 2-layer PCB

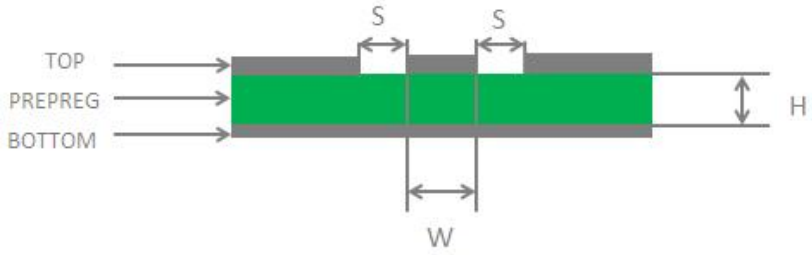


Figure 27: Coplanar Waveguide Design on a 2-layer PCB

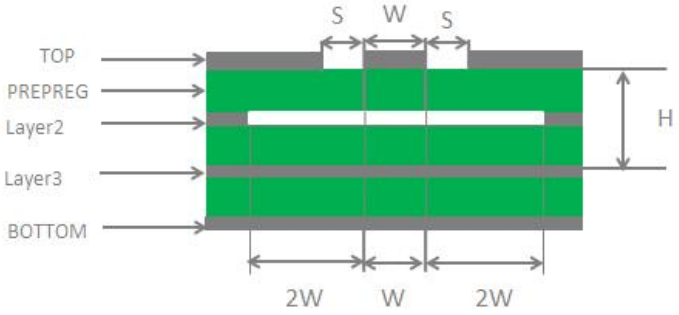


Figure 28: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

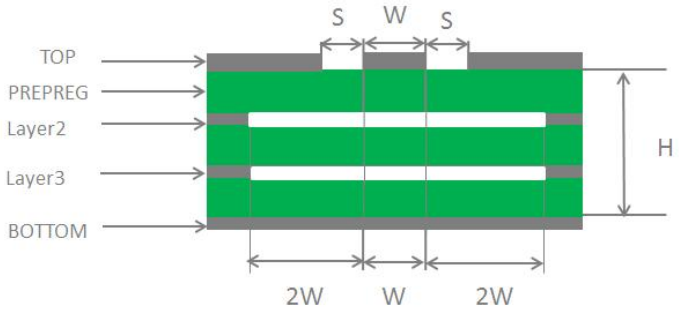


Figure 29: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.

- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

5.3. Requirements for Antenna Design

Table 26: Requirements for Antenna Design

Antenna Types	Requirements
Cellular	● VSWR：≤ 2 ● Efficiency: > 30 % ● Max. input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

5.4. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by Hirose.

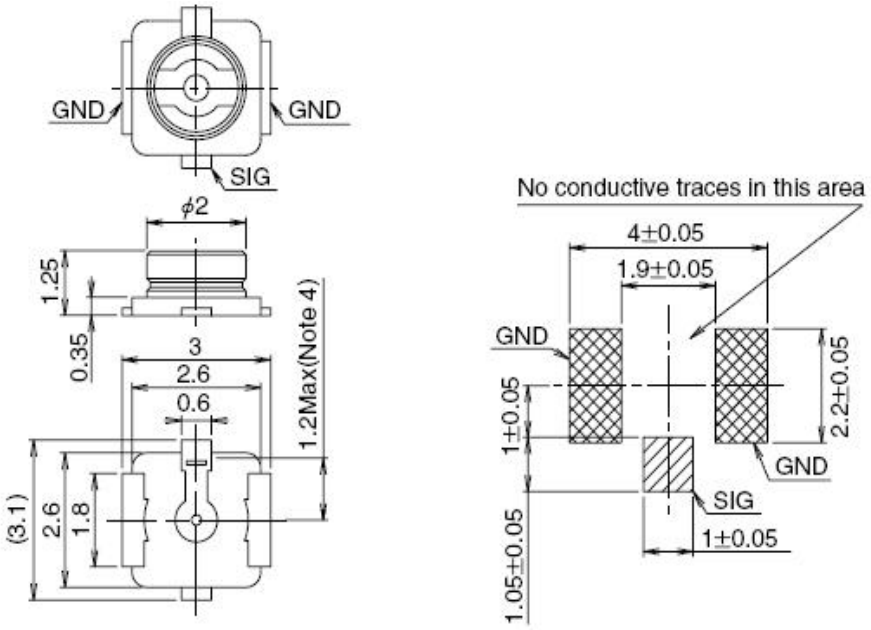


Figure 30: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

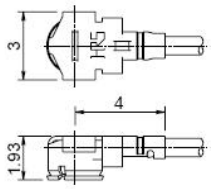
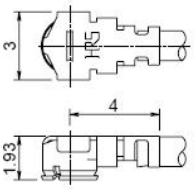
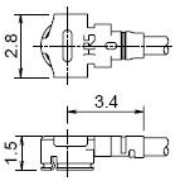
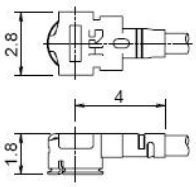
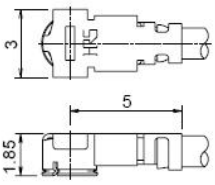
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 31: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connectors.

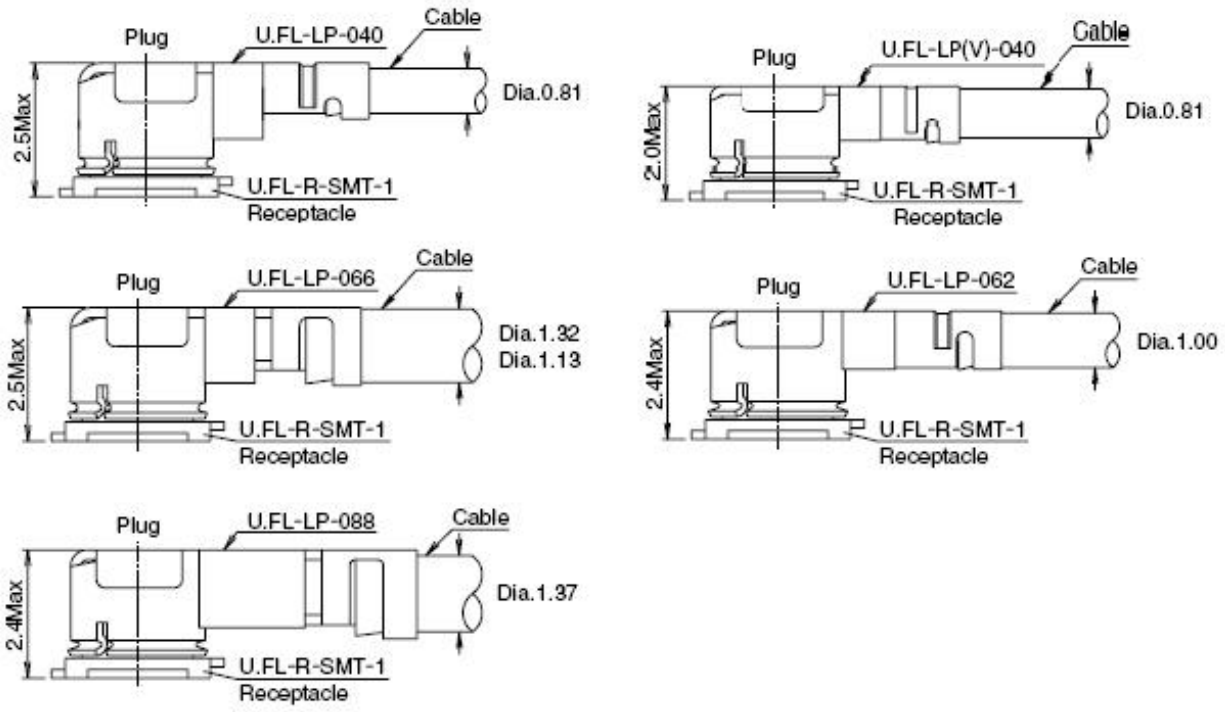


Figure 32: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Table 27: Absolute Maximum Ratings

Parameters	Min.	Max.	Unit
Voltage at VBAT	-0.3	6	V
Voltage at USB_VBUS	-0.3	5.5	V
Voltage at digital pins	-0.3	2.2	V
Voltage at ADC0	0	1.2	V
Voltage at ADC1	0	1.2	V
Current at VBAT	-	2	A

6.2. Power Supply Ratings

Table 28: Module Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltage must be within this range	3.4	3.8	4.3	V
I_{VBAT}	Peak supply current	at Maximum power control level	-	1.5	2	A
USB_VBUS	USB connection detect	-	3.0	5.0	5.25	V

6.3. Power Consumption

Table 29: Power Consumption

Modes	Conditions	Typ.	Units
OFF state	Power down	6.61	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	0.52	mA
	AT+CFUN=4 (USB disconnected)	0.59	mA
	LTE-FDD @ PF = 32 (USB disconnected)	1.06	mA
	LTE-FDD @ PF = 64 (USB disconnected)	0.76	mA
	LTE-FDD @ PF = 64 (USB Suspend)	0.95	mA
	LTE-FDD @ PF = 128 (USB disconnected)	0.60	mA
	LTE-FDD @ PF = 256 (USB disconnected)	0.58	mA
Idle state	LTE-FDD @ PF = 64 (USB disconnected)	7.34	mA
	LTE-FDD @ PF = 64 (USB connected)	19.34	mA
LTE data transmission	LTE-FDD B2	TBD	mA
	LTE-FDD B3	TBD	mA
	LTE-FDD B4	TBD	mA
	LTE-FDD B5	TBD	mA
	LTE-FDD B7	TBD	mA
	LTE-FDD B8	TBD	mA
	LTE-FDD B28	TBD	mA
	LTE-FDD B66	TBD	mA

6.4. Digital I/O Characteristics

Table 30: 1.8 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	0.7 × VDDIO	VDDIO + 0.2
V_{IL}	Low-level input voltage	-0.3	0.3 × VDDIO
V_{OH}	High-level output voltage	VDDIO - 0.2	-
V_{OL}	Low-level output voltage	-	0.2

Table 31: USIM Low-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
USIM_VDD	Power supply	1.62	1.98
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Low-level input voltage	0	0.2 × USIM_VDD
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD

Table 32: USIM High-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
USIM_VDD	Power supply	2.7	3.3
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD
V_{IL}	Low-level input voltage	0	0.15 × USIM_VDD
V_{OH}	High-level output voltage	0.7 × USIM_VDD	USIM_VDD
V_{OL}	Low-level output voltage	0	0.15 × USIM_VDD

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 33: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Test Points	Contact Discharge	Air Discharge	Unit
VBAT & GND	±5	±10	kV
All antenna interfaces	±4	±8	kV
Other interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 34: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature [4]	-35	+25	+75
Extended Operating Temperature [5]	-40	-	+85
Storage Temperature	-40	-	+90

[4] Within this range, the module's indicators comply with 3GPP specification requirements.
[5] Within this range, the module retains the ability to establish and maintain functions such as SMS*, data transmission, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

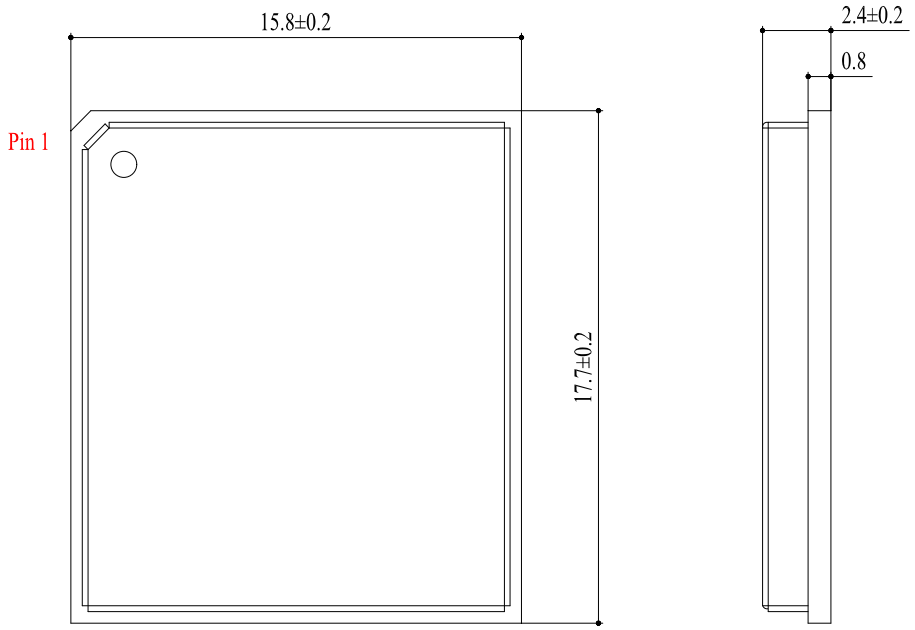


Figure 33: Module Top and Side Dimensions

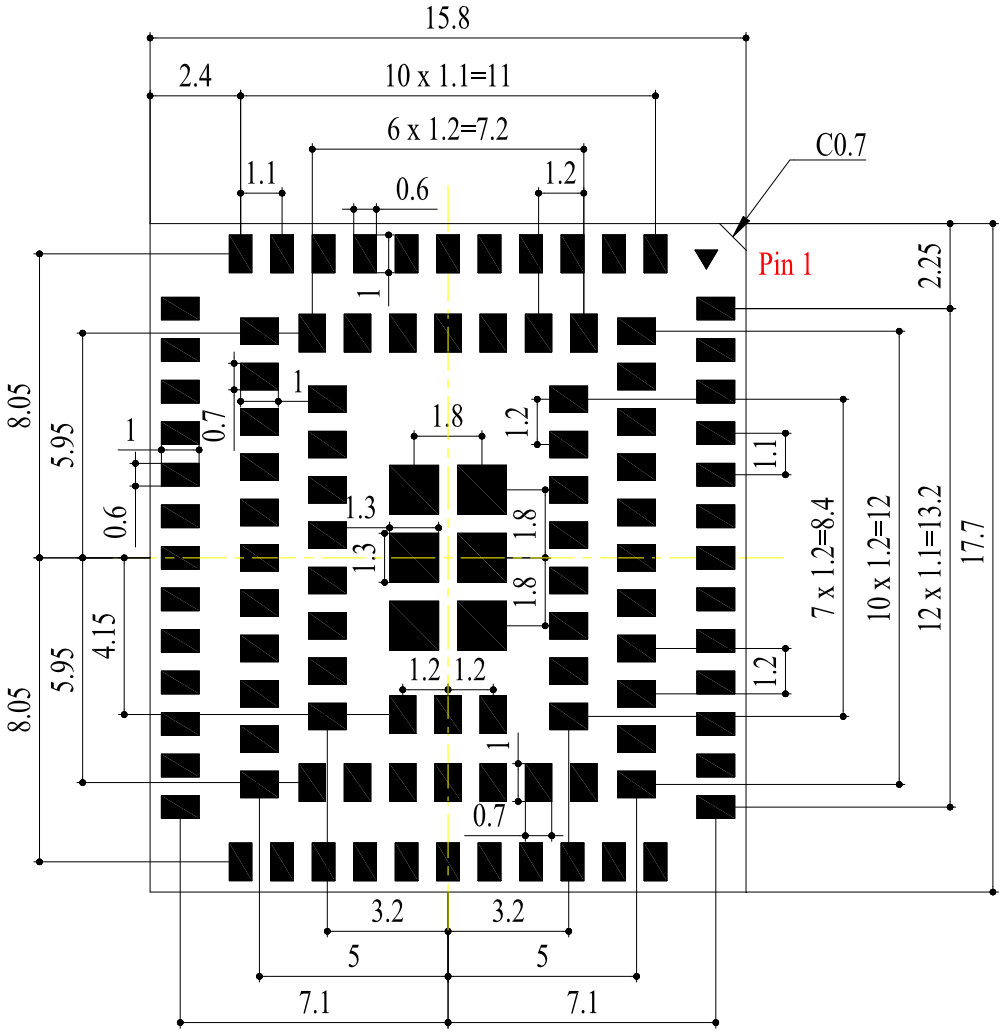


Figure 34: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module refers to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

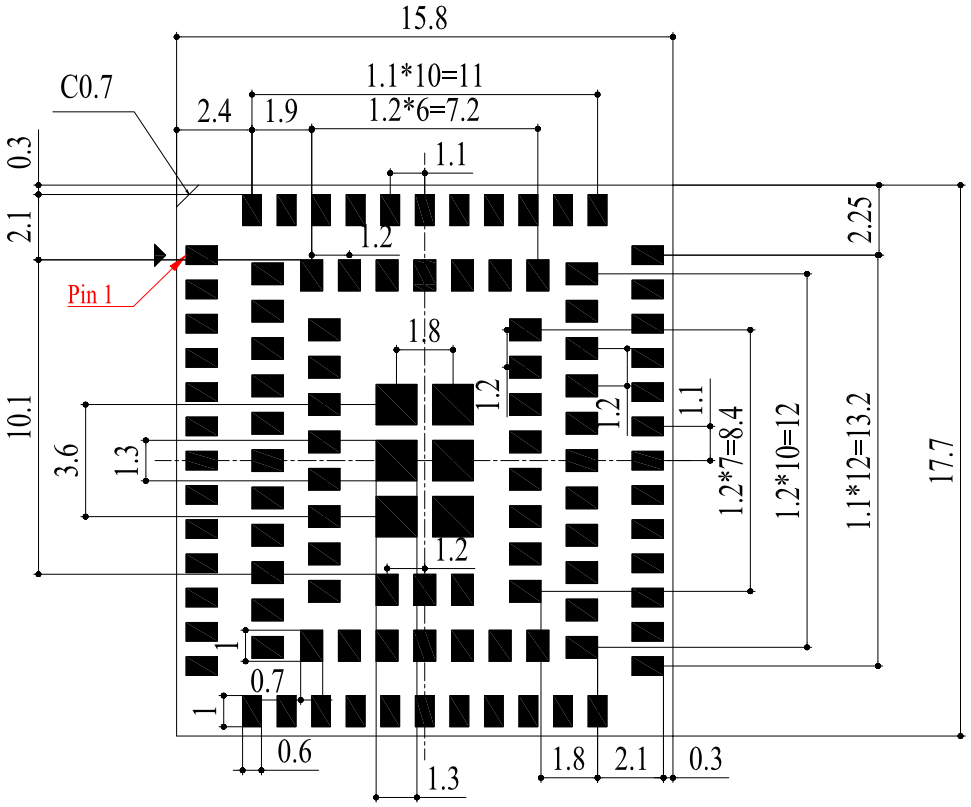


Figure 35: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

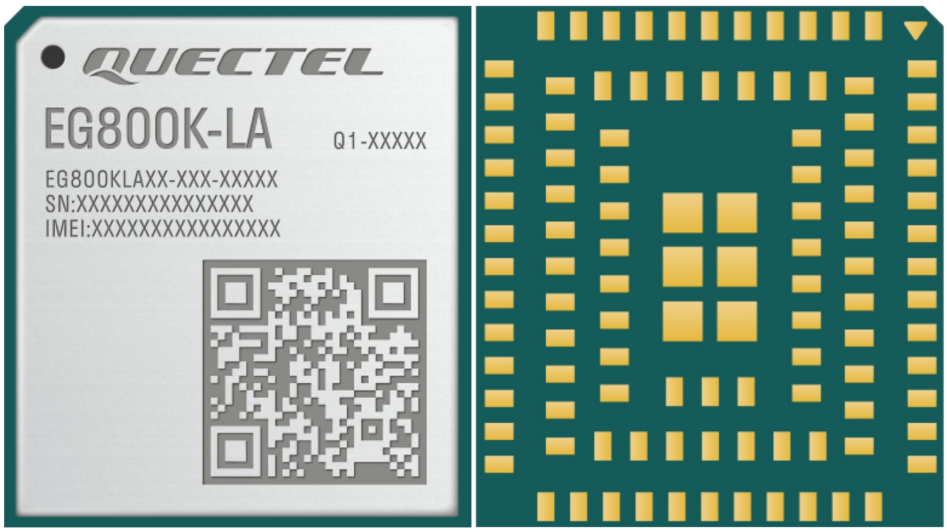


Figure 36: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [6] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [5]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

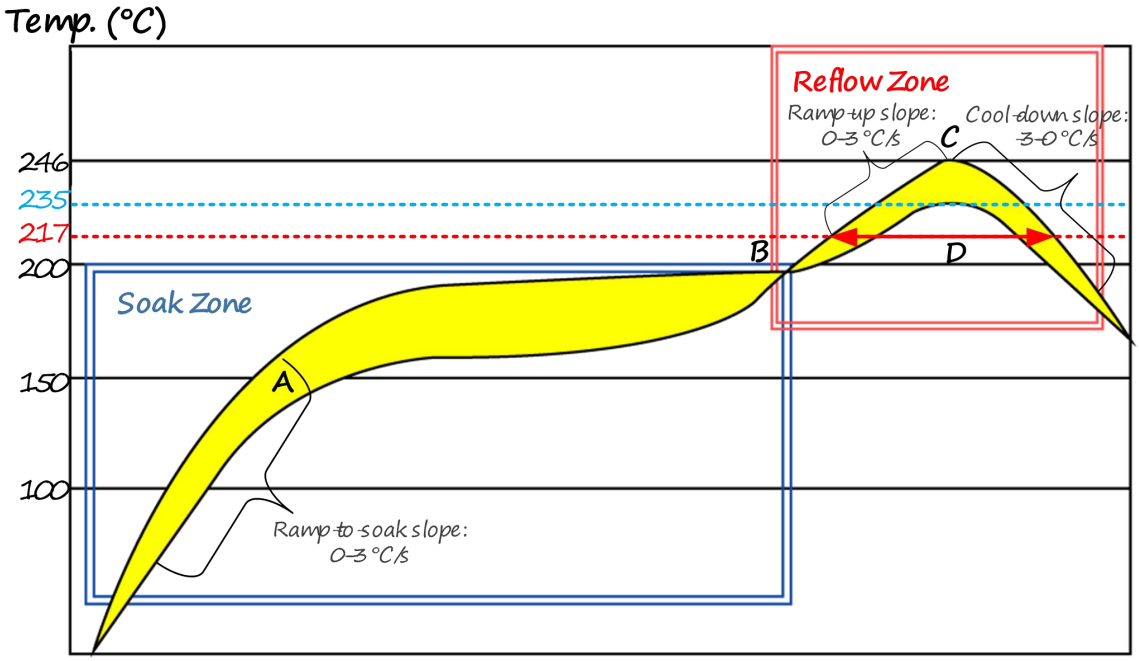


Figure 37: Recommended Reflow Soldering Thermal Profile

Table 35: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

8.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

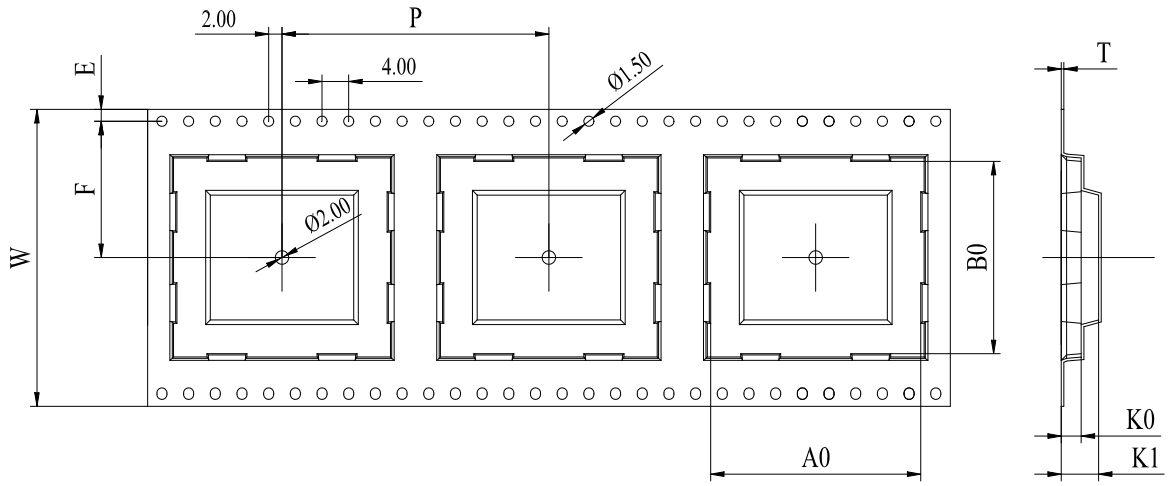


Figure 38: Carrier Tape Dimension Drawing (Unit: mm)

Table 36: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.2	18.1	2.8	4.6	14.2	1.75

8.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

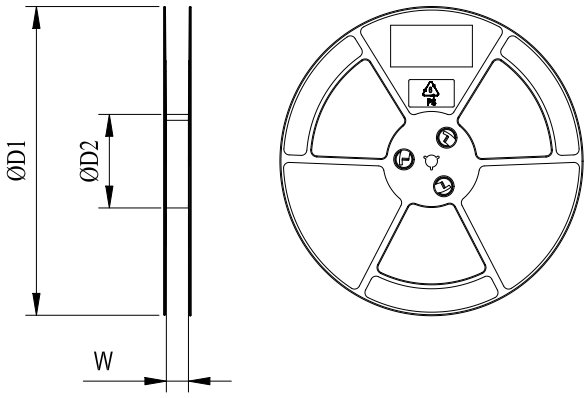


Figure 39: Plastic Reel Dimension Drawing

Table 37: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

8.3.3. Mounting Direction

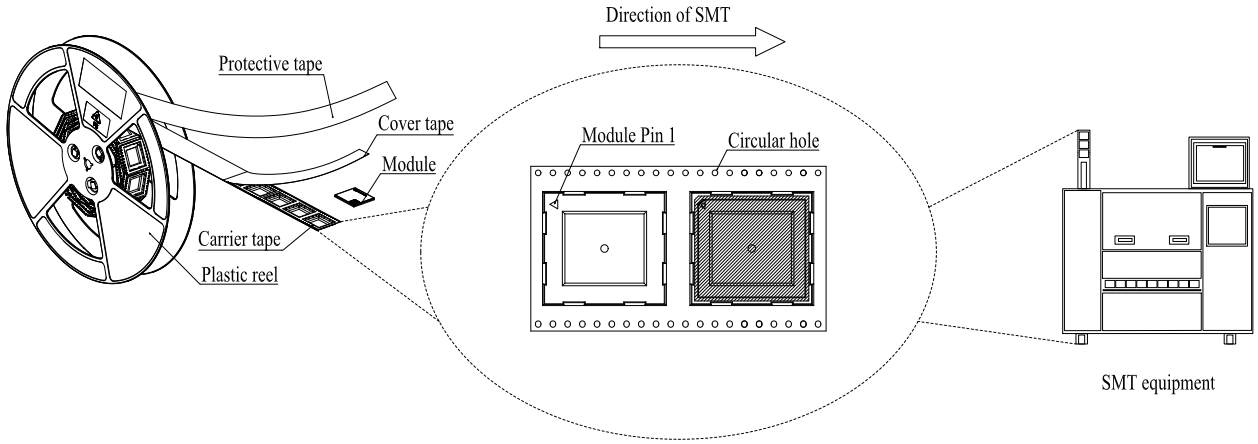
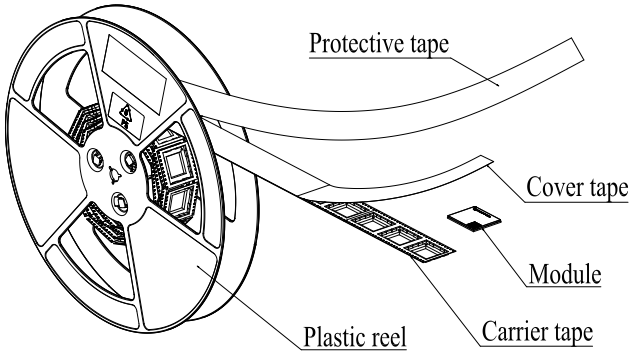


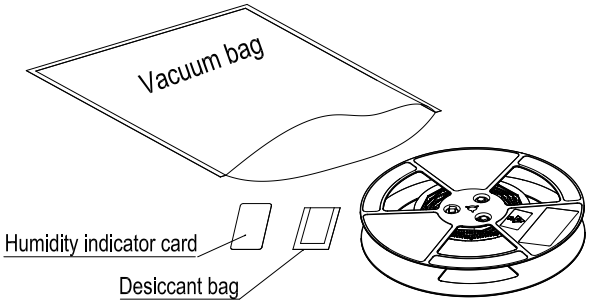
Figure 40: Mounting Direction

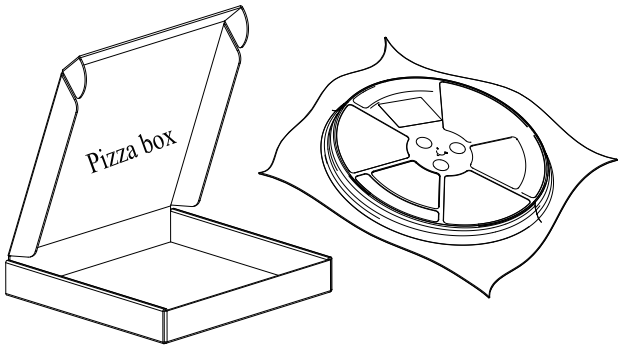
8.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can pack 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Place the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 2000 modules.

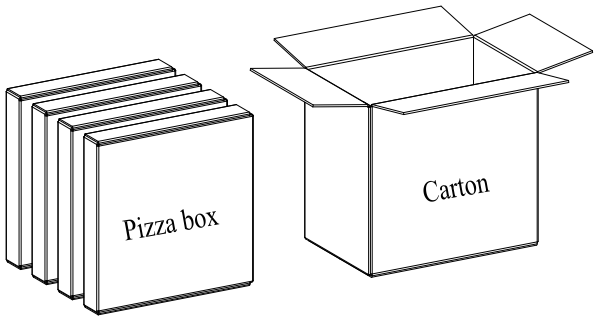


Figure 41: Packaging Process

9 Appendix References

Table 38: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_LTE_Standard(A)_Series_AT_Commands_Manual
[3] Quectel_EC800K&EG800K_Series_Reference_Design
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_Stencil_Design_Requirements
[6] Quectel_Module_SMT_Application_Note

Table 39: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
AMR	Adaptive Multi-Rate
bps	Bits per second
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection MUX
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute

EVB	Evaluation Board
FDD	Frequency Division Duplexing
FILE	File Protocol
FTP	File Transfer Protocol
FTPS	FTP over SSL
GND	Ground
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IMS	IP Multimedia Subsystem
IMU	Inertial Measurement Unit
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCU	Microcontroller Unit
ME	Mobile Equipment
MLCC	Multi-layer Ceramic Capacitor
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
OTT	Over The Top
PA	Power Amplifier
PAP	Password Authentication Protocol

PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PF	Paging Frame
PING	Packet Internet Groper
PMU	Power Management Unit
PPP	Point-to-Point Protocol
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SMD	Surface Mount Device
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
USIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage

Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

Notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID XMR2024EG800KLA procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2024EG800KLA”
The FCC ID ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna Gain

LTE Band 2: 1.59dBi
LTE Band 4: 2.00dBi
LTE Band 5: 2.13dBi
LTE Band 7: 3.00dBi
LTE Band 66: 2.00dBi

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or
remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

The device must not be co-located or operating in conjunction with any other antenna or transmitter. This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions : (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

List of applicable FCC rules

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM

This module has been tested and found to comply with part 22, part 24, part 27 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

Integration instructions for host product manufacturers according to KDB 996369 D03 OEM Manual v01

2.2 List of applicable FCC rules

FCC part 22, part 24, part 27

2.3 Specific operational use conditions

The module can be used for mobile applications with a maximum 3.0dBi antenna. The host manufacturer installing this module into their product must ensure that the final compos it product complies with the FCC requirements by a technical assessment or evaluation to the FCC rules, including the transmitter operation. The host manufacturer has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module The end user manual shall include all required regulatory information/warning as show in this manual.

2.4 Limited module procedures

Not applicable The module is a Single module and complies with the requirement of FCC Part 15 212.

2.5 Trace antenna designs

Not applicable The module has its own antenna, and doesn’t need a hosts printed board micro strip trace antenna etc.

2.6 RF exposure considerations

The module must be installed in the host equipment such that at least 20cm is maintained between the antenna and users" body; and if RF exposure statement or module layout is changed, then the host product manufacturer required to take responsibility of the module through a change in FCC ID or new application The FCC ID of the module cannot be used on the final product In these circumstances, the host manufacturer will be responsible for reevaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

2.7 Antennas

Antenna Specification are as follows:

Type: External Antenna

Gain: 3.0 dBi Max

This device is intended only for host manufacturers under the following conditions: The transmitter module may not be co-located with any other transmitter or antenna; The module shall be only used with the internal antenna(s) that has been originally tested and certified with this module. The antenna must be either permanently attached or employ a “unique" antenna coupler.

As long as the conditions above are met, further transmitter test will not be required However, the host manufacturer is still responsible for testing their end-product for any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc).

2.8 Label and compliance information

Host product manufacturers need to provide a physical or e-label stating "Contains FCC ID: XMR2024EG800KLA " with their finished product.

2.9 Information on test modes and additional testing requirements

Host manufacturer must perform test of radiated & conducted emission and spurious emission, e.t.c according to the actual test modes for a stand-alone modular transmitter in a host, as well as for

multiple simultaneously transmitting modules or other transmitters in a host product. Only when all the test results of test modes comply with FCC requirements, then the end product can be sold legally.

2.10 Additional testing, Part 15 Subpart B disclaimer

The modular transmitter is only FCC authorized for FCC Part 22, Part24, Part27 and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.