PRODUCT SPECIFICATION
納　入　仕　様　書

MODEL NAME

型　　名 :　NS73B0WC33-01-EF-E1

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新潟精密(株) NIIGATA SEIMITSU Co., Ltd.	発行年月日 DATE	2005.Dec.26
承認 APPROVED	調査 CHECKED	作成 DRAWN

CONTENTS; 目次

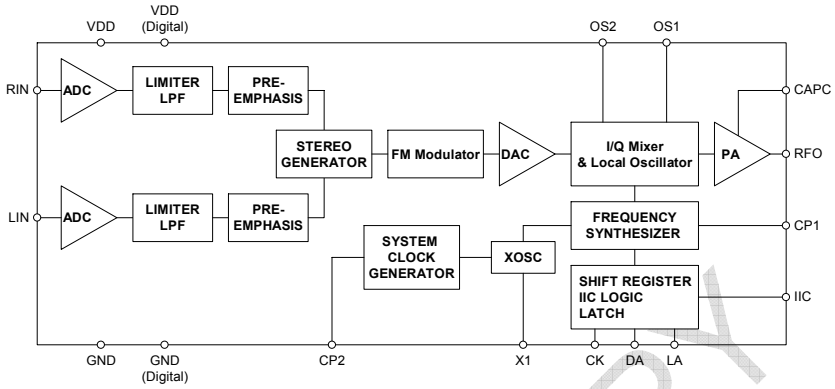
1. Scope ; 適用

This specification applies to the FM STEREO TRANSMITTER IC: NS73B0WC33-01-EF-E1.

2. Model Name ; 型名

NS73B0WC33-01-EF-E1

3. Block Diagram ; ブロック図



4. Absolute Maximum Specification ; 絶対最大定格

No.	ITEM 項目	MIN. 最小値	MAX. 最大値	UNIT 単位
1	Maximum supply voltage 最大電源電圧	-0.3	3.7	V
2	Maximum input voltage 最大入力電圧	-0.3	VDD+0.3	V
3	Storage temperature 保存温度	-40	+125	degC
4	Storage humidity 保存湿度 Note	45	85	%RH

Note: Refrain from dew condensation; 結露無きこと

5. Electrical Specification; 電気的仕様

No.	ITEM 項目	SPECIFICATION 仕様
1	Type	FM Stereo Transmitter with frequency synthesizer
2	FM Modulation	I/Q Modulation with 304kHz offset
3	Offset frequency from local oscillation frequency	-304kHz
4	Transmission frequency range	87.5 - 108.0 MHz
5	Antenna impedance アンテナインピーダンス	50-ohm
6	Operating supply voltage 動作電源電圧	DC +2.7V to + 3.6V
7	Operating Temperature 動作温度範囲	-30degC to +80degC

6. Electrical Characteristics; 電気的特性

6.1. Standard Test Condition; 標準試験条件

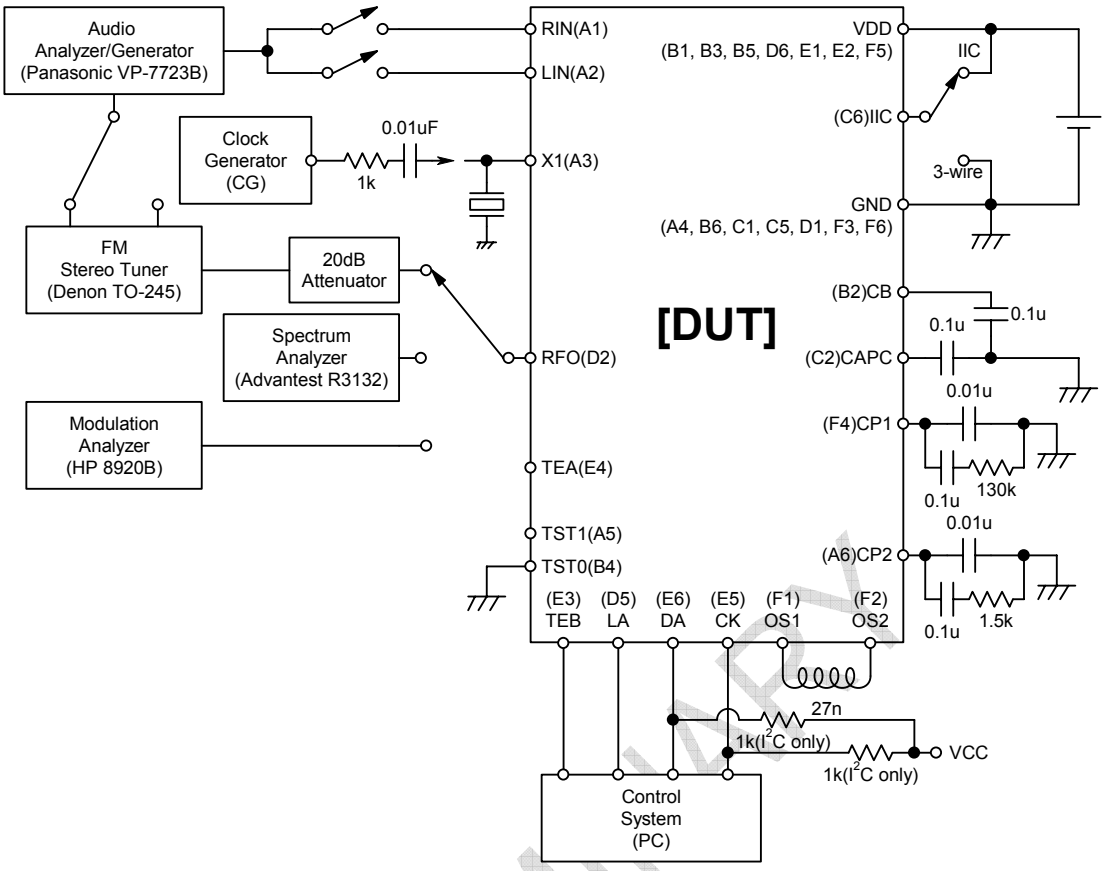
No.	ITEM 項目	SYMBOL 記号	CONDITION 試験条件
1	Standard supply voltage 基準電源電圧		DC +3.0V +/- 0.05V
2	Temperature 温度		+25 +/- 5degC
3	Relative humidity 相対湿度		65 +/- 5%RH
4	Demodulator's audio filter		HPF:100Hz LPF:15kHz（more than -42dB/oct）
5	Standard clock frequency 基準クロック周波数		32.768kHz (crystal or external clock tolerance +/-20ppm max.)
6	Modulation frequency 変調周波数	fi	1kHz unless otherwise specified
7	Standard signal level 標準入力信号電圧	Vi	90mVrms
8	Carrier frequency 搬送波周波数		98MHz

As far as there is not any specification, it measures in the above condition.

However, test may be done under the following conditions, when it is considered to have no effect on the test result.

Temperature: +5degC to 35degC, Relative Humidity: 45 to 85%RH.

6.2. Circuit of Measurement; 測定用接続図



Electrical characteristics are results of measurements conducted by our original JIG.
電気的特性は、弊社作製の治具によって測定されたものです。

6.3. Electrical Characteristics Item; 電気的特性項目

ITEM 項目	SYMBOL 記号	CONDITION 試験条件 (refer to register map)	MIN. 最小値	TYP. 標準値	MAX. 最大値	UNIT 単位
TX Frequency Range			87.5		108.0	MHz
TX Power Output (Absolute values are not guaranteed since these levels are just as reference)	PO	PL : 1	0.25	0.5		mW
		PL : 2	0.5	1		
		PL : 3	1	2		
TX offset Frequency from local oscillation frequency	foff			-304		kHz
Current Consumption 消費電流	Idd			36	45	mA
Standby Current スタンバイ電流	Istb			1.5	20	uA
Modulation Deviation	Dev.	EM : 0, AG : 0, SUBC : 0, PLT : 1	+/-50			kHz
Modulation Distortion	THD	Mono		0.4	1.0	%
		Stereo		0.4	1.0	
Modulation S/N Ratio	SNR	Mono	50	55		dB
		Stereo	50	55		
Stereo Separation	SEP		25	35		dB
Audio Frequency Response	FR	f = 50Hz - 15kHz, fi = 400Hz@0dB, Vi = 12mVrms	-3	0	1.5	dB
Audio Input Impedance	Zaf	f = 50Hz - 15kHz	50	60		kOhm
Pilot Tone Level	PL		9	10	11	%
Crystal oscillator	fXT	Frequency	32.768			kHz
	dXT	Tolerance	-20	0	20	ppm

Please set the specification of transmission power level is based on each country and local Wireless Telegraphy Act.
送信出力レベルの仕様は、各国および地方の電波法に基づいて設定してください。

7. Serial Interface; シリアルインターフェース

NS73 receives data either by 3-wire bus or I^2C bus, and transmits data by I^2C bus only. The I^2C or the 3-wire bus mode can be selectable by the level of Pin "IIC" as;

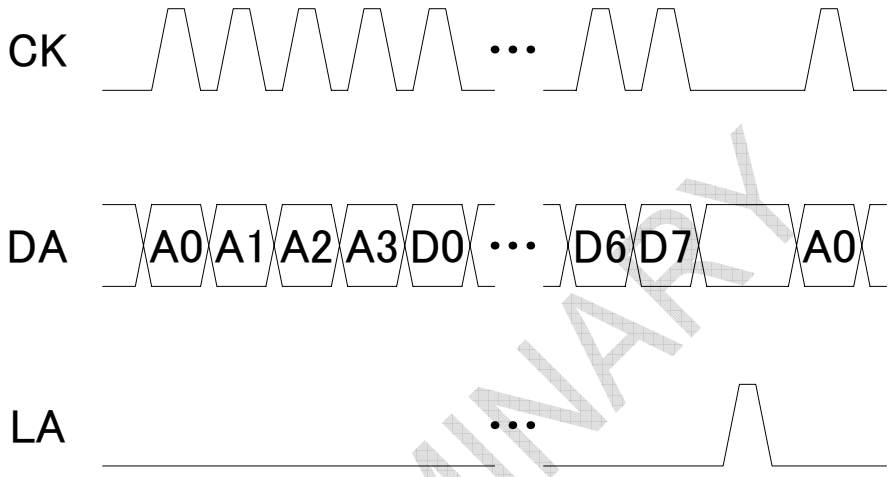
"IIC" = HIGH(VDD) -> I^2C mode

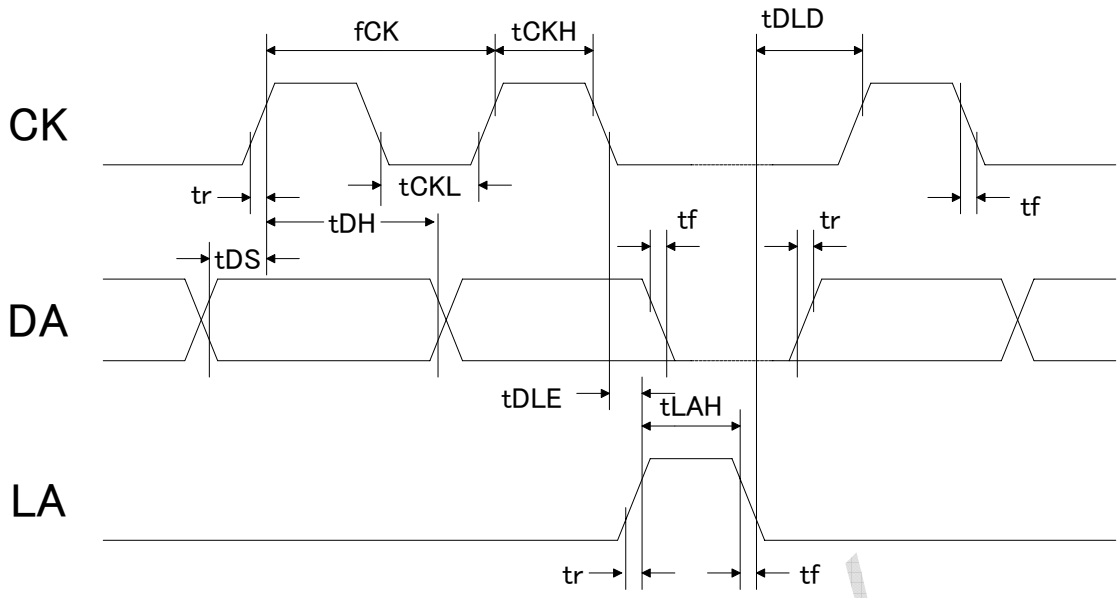
"IIC" = LOW(0V) -> 3-wire mode

7.1. 3-wire bus Mode; 3線シリアル方式

The 3-wire bus contains three signals as Clock(CK), Data(DA) and Latch(LA).Received data consists of 4 bits for address (A0 to A3) and 8 bits for data (D0 to D7).Received data will be transferred from A0 to A3, D0 to D7 (LSB First). Registers are set on the rising edge of LA. (Receiving only for 3-wire bus)

(The rising edge of LA settles the data into registers insides of NS73.)





AC characteristics

No.	Parameter	Symbol	Min.	Max.	Unit
1	CK frequency	fCK		1	MHz
2	Low period of the CK clock	tCKL	250		nS
3	High period of the CK clock	tCKH	250		nS
4	Rise time of CK, DA, LA	tr		125	nS
5	Fall time of CK, DA, LA	tf		125	nS
6	Data setup time	tDS	100		nS
7	Data hold time	tDH	100		nS
8	Latch enable time between CK clock	tDLE	0		nS
9	Latch disable time between CK clock	tDLD	0		nS
10	High period of LA pulse	tLAH	250		nS

DC characteristics

No.	Parameter	Symbol	Min.	Max.	Unit
1	Low level input voltage	VIL	-0.3	0.25VDD	V
2	High level input voltage	VIH	0.75VDD	VDD+0.3	V
3	Hysteresis of Schmitt trigger input	Vhys	0.05VDD		V
4	Input current (Input voltage 0.1~0.9VDDmax)	Ii		10	uA
5	Capacitance for each I/O pin	Ci		10	pF

7.2. I^2C bus Mode; I^2C 方式

I^2C bus consists of two wires as a serial data line (DA) and a serial clock line (CK). Serial 8-bit bi-directional data transfers can be made at up to 400 kbit/s in the Fast-mode. However, as the set-up time of data, 100nsec or more are necessary. Other devices connected to the same bus require more than 100nsec for data set-up time. It does not correspond to Hs-mode.

NOTE)
This IC CAN NOT be written in at a sequence of resister at a time. So Set data in register by register.

7.2.1. I^2C-bus Terminology; I^2C で使用される用語

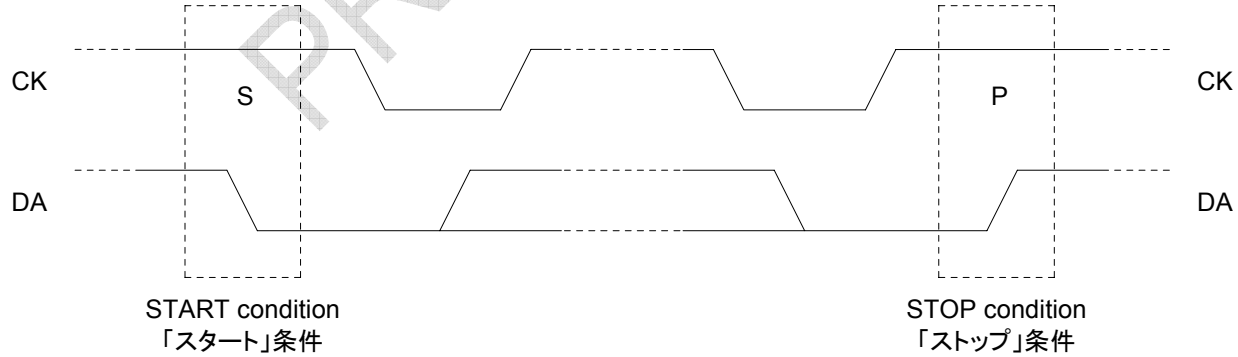
Following table shows the terminology of I^2C bus.
I^2C では下記用語が定義されています。

TERM 用 語	DESCRIPTION 説 明
Transmitter トランスミッタ	The device which sends data to the bus データをバスに送信するデバイス
Receiver レシーバ	The device which receives data from the bus データをバスから受信するデバイス
Master マスター	The device which initiates a transfer, generates clock signals and terminates a transfer データ転送を開始し、クロック信号を生成し、データ転送を終了するデバイス
Slave スレーブ	The device addressed by a master マスターからアドレスを指定されるデバイス

7.2.2. START Condition and STOP Condition; 「スタート」条件と「ストップ」条件

START condition is surely needed for the beginning of data communications. STOP condition is surely needed for the end of data communications. The situation, in which DA line changes from HIGH to LOW while CK is HIGH, is referred to as START condition. Moreover, the situation, a LOW to HIGH transition on the DA line while CK is HIGH, is referred to as STOP condition.

データ通信の始まりには「スタート」条件が、終わりには「ストップ」条件が必ず必要となります。CK が"H"のときに DA ラインが"H"から"L"に変化する状況を「スタート」条件と呼びます。また、CK が"H"のときに DA ラインが"L"から"H"に変化する状況を「ストップ」条件と呼びます。



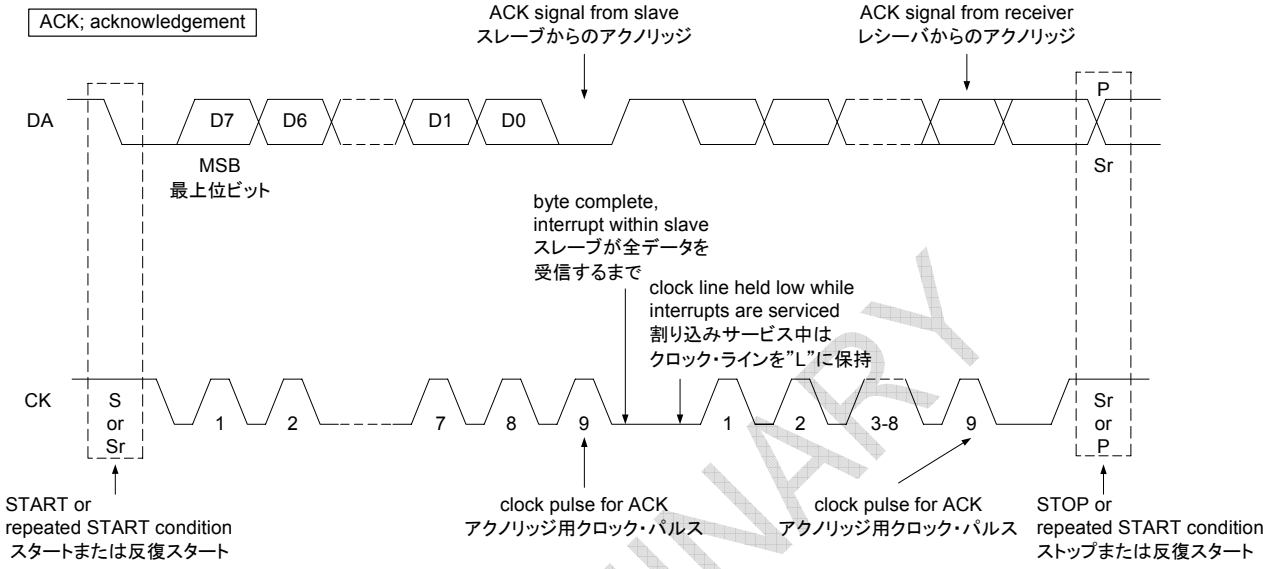
7.2.3. Data Transfer; データ転送

Every byte outputted on the DA line must be 8-bits long. The acknowledge bit is needed after each byte. Data is sequentially transmitted from most significant bit (MSB).

At data transfer, after the START condition(S), a slave address is sent. A data transfer is always terminated by the STOP condition (P) generated by the master.

DA ラインに出力される各バイトの長さは必ず 8 ビットになります。各バイトの後にはアクノリッジ・ビットが必要となります。データは最上位ビット(MSB)から順に送信されます。

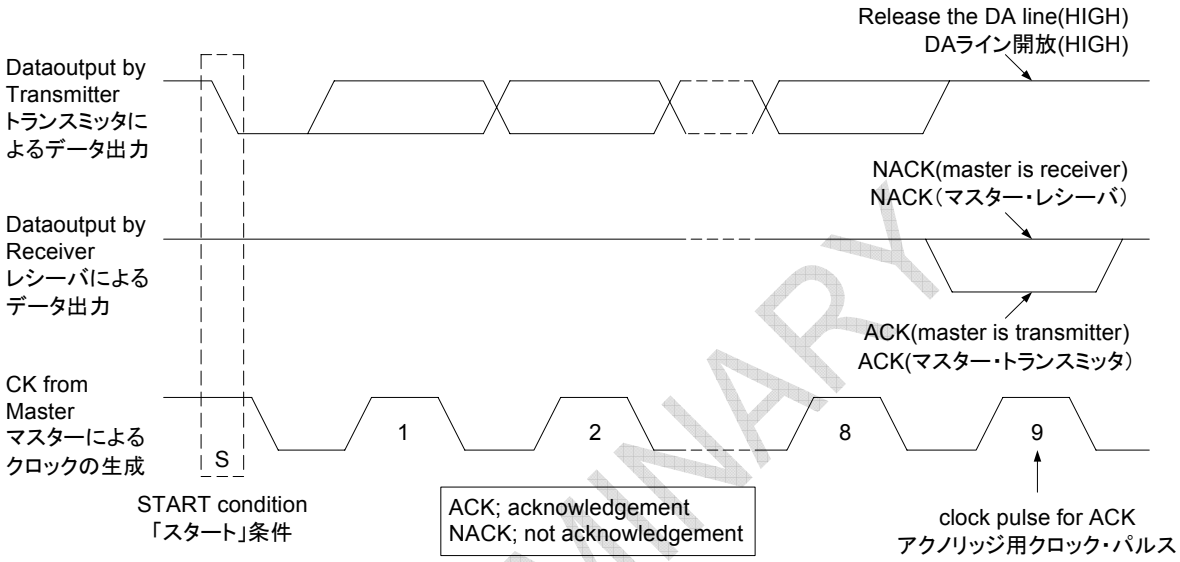
データ転送では、「スタート」条件（S)の後、スレーブのアドレスが送信されます。データ転送は必ずマスターが生成する「ストップ」条件（P)によって終了します。



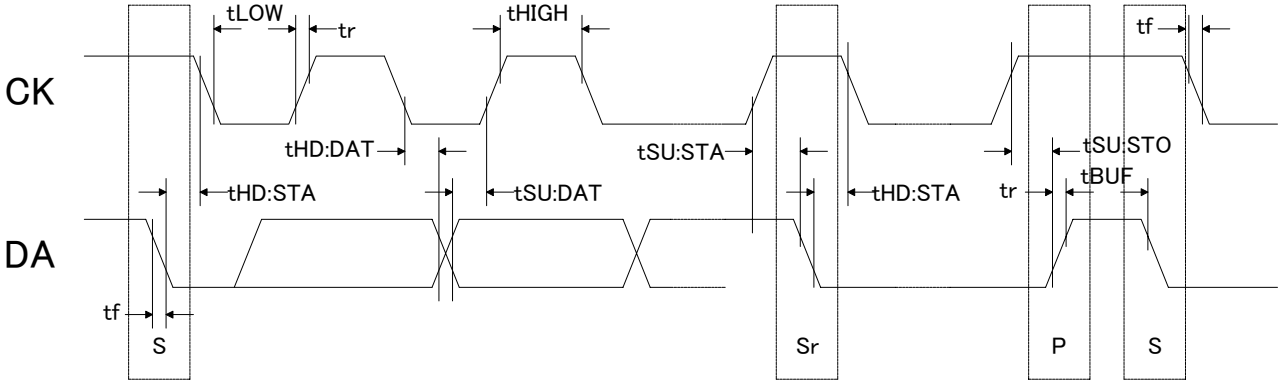
7.2.4. Acknowledge; アクノリッジ（受信確認）

When Acknowledge-related clock pulse is generated by the master, the transmitter releases the DA line “HIGH” during the acknowledge clock pulse. The Receiver outputs “LOW” during the acknowledge clock pulse “HIGH” per reception of one byte (8bit data). If the master-receiver is involved in a transfer, it must signal the end of data to the slave-transmitter by not generating the acknowledge on the last byte which is sent out of the slave.

マスターによってアクノリッジ用クロック・パルスが生成された場合、トランスミッタは DA ラインを開放します（DA ラインは"H"状態になります）。レシーバはデータを 1 バイト(8 ビット)受信するごとにアクノリッジ・クロック・パルスが"H"状態のときに、DA ラインを"L"にします。マスターがレシーバとなる場合、スレーブから送信されたデータの終わりにアクノリッジをしないことでマスターはスレーブにデータの終わりを知らせます。



7.2.5. Electrical Specification and Timing for I/O Stages



AC characteristics

No.	Parameter	Symbol	Min.	Max.	Unit
1	CK frequency	fCK		400	kHz
2	Hold time START condition	tHD:STA	250		nS
3	HIGH period of the CK clock	tHIGH		0.6	uS
4	LOW period of CK clock	tLOW		1.3	uS
5	Set-up time for a repeat condition	tSU:STA		0.6	uS
6	Set-up time for a stop condition	tSU:STO	0.6		uS
7	Data hold time	tHD:DAT	0	0.9	uS
8	Data set-up time	tSU:DAT	100		nS
9	Rise time of both DA and CK	tr		300	nS
10	Fall time of both DA and CK	tf		300	nS
11	Bus free time between a STOP and START condition	tBUF	1.3		uS

DC characteristics

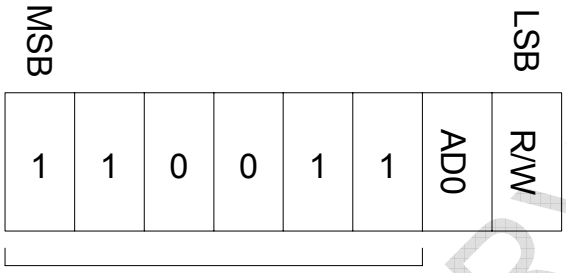
No.	Parameter	Symbol	Min.	Max.	Unit
1	Low level input voltage	VIL	-0.3	0.25VDD	V
2	High level input voltage	VIH	0.75VDD	VDD+0.3	V
3	Hysteresis of Schmitt trigger input	Vhys	0.05VDD		V
4	Low level output voltage at 3mA sink current	Vol		0.4	V
5	Input current (Input voltage 0.1~0.9VDDmax)	Ii		10	uA
6	Capacitance for each I/O pin	Ci		10	pF

7.2.6. Definition of Bits in a Byte; 1 バイト内の各ビット定義

7.2.6.1. Slave Address; スレーブ・アドレス

Slave address consists of the fixed address 110011 (unique to the chip) and of the value set by the LA pin. Therefore the LA pin must be connected either with VDD or VSS. It is also possible to control as “LATCH IN”. This address is 7 bits long followed by an eighth bit which is a data direction bit (R/W). When the data direction bit is "0", it indicates a transmission (WRITE). When the data direction bit is "1", it indicates a reception for data (READ).

スレーブ・アドレスはチップ固有の固定アドレス"110011"と LA 端子で設定される値で構成されます。したがって LA 端子を必ず HIGH または LOW に接続して下さい。LATCH IN として制御することも可能です。8 ビット目にはデータ方向ビット(R/W)が続きます。このデータ方向ビットが"0"であれば送信(書き込み)、"1"であれば受信(読み込み)を行います。



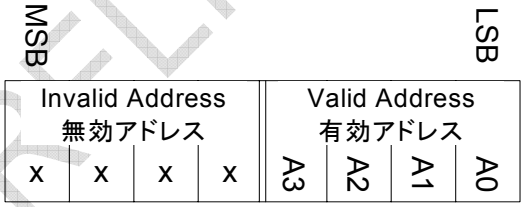
AD0	BIT
HIGH	1
LOW	0

R/W	BIT
READ	1
WRITE	0

7.2.6.2. Register Address; レジスタ・アドレス

The internal registers are 13 in full, so four bit data set at the MSB side are invalid.

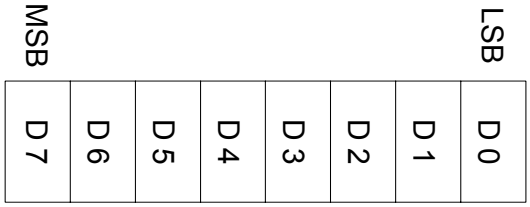
内部レジスタは全部で 13 個のため、MSB 側に設定された 4 ビットのデータは無効となります。



7.2.6.3. Register data; レジスタ・データ

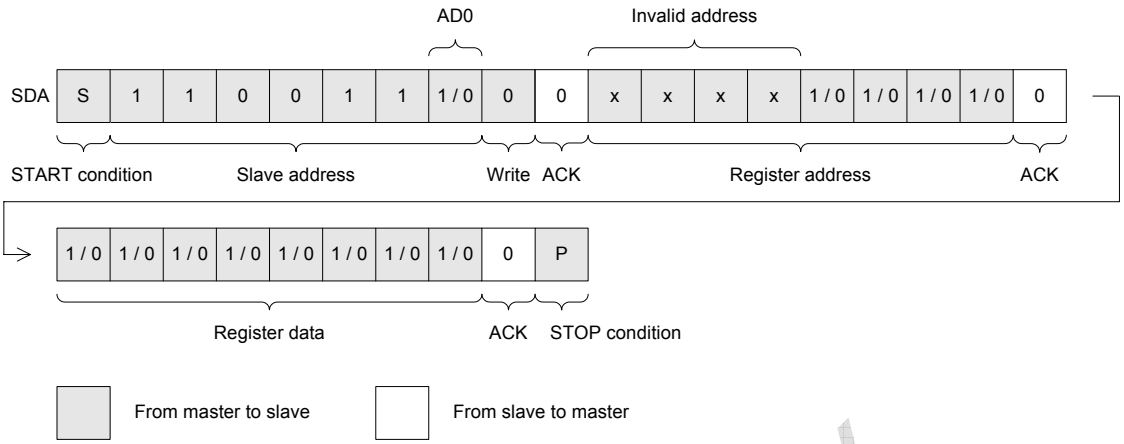
The data length of each register is 8 bit.

各レジスタのデータは 8 ビットで構成されています。

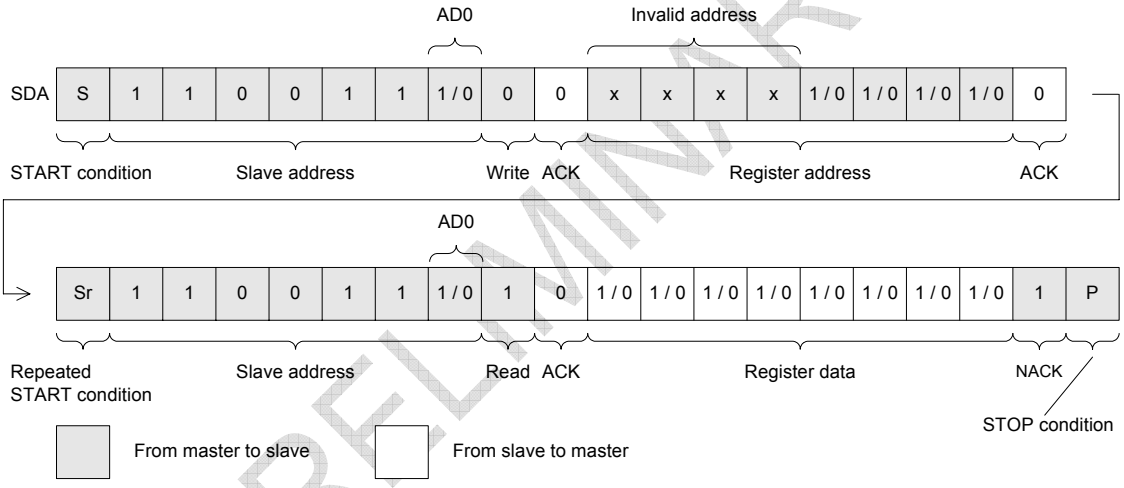


7.2.7. Command Format; コマンドフォーマット

7.2.7.1. Individual Register Data Writing; 個別レジスタ・データ書き込み



7.2.7.2. Individual Register Data Reading; 個別レジスタ・データ読み込み



8. Software Control Specification; ソフトウェア制御仕様

8.1. Register Settings(outline); レジスタ設定（概要）

Do software reset (set address "E" data "xxxx 0101(MSB First)") when turning IC power ON. Set all registers to an initial value before setting Register PE to "1". Register map shows detail of registers. Be sure to set initial value to the register which cell's color is gray at the register map. The register which cell's color is white is to define for yourself.

IC 電源 ON 時に、ソフトウェアリセットをかけてください。ソフトウェアリセット後、レジスタ PE を 1 に設定する前に、全レジスタを初期値に設定してください。レジスタの詳細は、レジスタ MAP を参照して下さい。レジスタ MAP の色枠のレジスタは、必ず初期値を設定して下さい。レジスタ MAP の白枠のレジスタは、お客様で設定して頂くレジスタです。

8.2. Standard Clock; 基準クロック

(1) When using a crystal oscillator, use one that the frequency stability is within +/-20ppm.
水晶発振の場合、安定度+/-20ppm 以下の水晶振動子を使用して下さい。

Reference crystal element

F[kHz]	CL[pF]	R1[kohm]	Co[pF]	C1[fF]
32.768	12.5	40 max	1.35 typ.	3.0 typ.

(2) When using an external clock, couple a capacitor and a resistor to the X1(F7) pin of the IC for clock input. Keep the input level of the clock between MIN = 0.4[Vp-p] to MAX = VDD [Vp-p]. Frequency stability is +/-20ppm max.
外部クロックの場合、X1(F7)端子にコンデンサと抵抗でカップリングして入力して下さい。クロックの入力レベルは、MIN=0.4[Vpp] ～ MAX=VDD[Vpp]、安定度は+/-20ppm 以内として下さい。

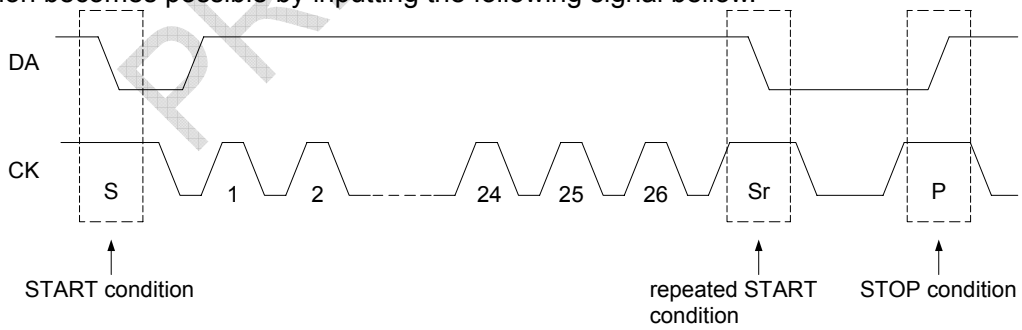
8.3. Muting

MUTE register behavior is deleting Pilot tone as well as Audio input. So using MUTE makes not Stereo.

To use muting as stereo condition, do in application controlling this IC, not use this register.

8.4. Reset for Serial Interface

In order to avoid incorrect operation after starting power supply, input the following signal bellow. When communication discontinuation occurs (reset microcomputer, etc), the usual operation becomes possible by inputting the following signal bellow.



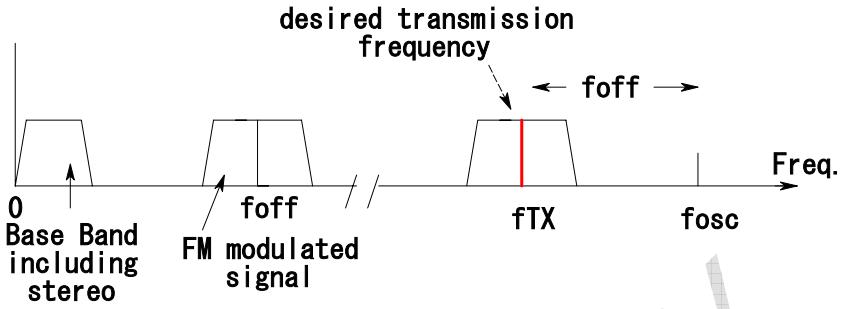
8.5. PLL Setting Method; PLL（P レジスタ）設定方法

Although the local oscillator is oscillating at 4 times of transmitted frequency, transmitted frequency can be used to calculate the number to program for the synthesizer because of the divided-by 4 pre-scaler between the local oscillator and the synthesizer.

It is also considered that the oscillation frequency(fosc) should be located above the transmission frequency(fTX).

Because the base band signal is modulated in FM with 304kHz offset(foff)

Following shows the frequency spectrum of NS73.



Therefore, the fosc should be (fTX + foff).

This is applied to decide divided-by N of synthesizer.

The reference frequency of the synthesizer is taken as 8.192kHz or frequency of divided-by its integer-N.

However, the FM channel steps such as 50kHz, 100kHz and 200kHz are not divisible by 32.768kHz and its divided-by N.

Then, we have to accept some error frequencies from proper transmission frequency.

In order to satisfy the +/-5kHz frequency allowance, the divided-by ratio (N) is calculated as;

Choose the reference frequency of synthesizer to 8.192kHz, i.e.,

N = (fTX + foff) / 0.008192M

and round off the N to zero decimal places (integer).

Convert N to Nh and Nb.

Set Nb to shift register of transmission with LSB first for 3-wire serial mode or MSB first for I^2C bus transmission.

For example) fTX=88.5MHz

N = (fTX + 0.304) / 0.008192 = (88.5 + 0.304) / (0.008192) = 10840.33 ...

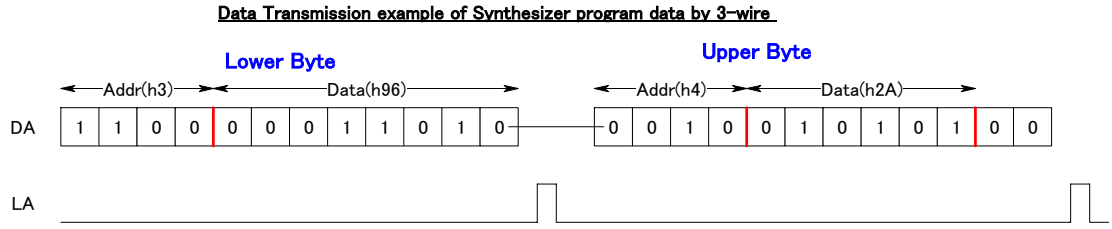
N = round(N,0) = 10840

Nh = 2A58h　　Nb = 10 1010 0101 1000b

Data transmission for 3-wire is; start “0001 1010 0101 01” -end of bit

Data transmission for I^2C is start “10 1010 0101 1000” -end of bit.

Total data transmission for above data to NS73 can be shown as below;



8.6. Register Map; レジスタマップ

Colored frames indicate the registers that must be set to “INITIAL” value.
網掛けしたレジスタは初期値を設定してください。

REGISTER	NAME	CONTENTS	SELECTION	ADDRESS				DATA								INITIAL (Hex)
				A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R0	PE	Power SW	OFF	0	0	0	0								0	0
			ON												1	
	PDX	Crystal SW	ON											0		0
			OFF											1		
	MUTE	Mute	OFF										0			0
			ON										1			
	S32K	For test	-									0				0
	EM	Pre-emphasis switch	ON								0					0
			OFF								1					
	EMS	Pre-emphasis Selection	50us							0						0
			75us							1						
	AG	Audio input level to get 100% modulation	100mV					0	0							0
			140mV					0	1							
			200mV					1	0							
R1	DEV	For test	-	0	0	0	1						1	0	0	4
	PLT	Pilot tone	ON									0				0
			OFF									1				
	-	For test	-							1	1					3
	SUBC	Forced subcarrier	ON						0							0
			OFF						1							
	HPF	For test	-					1								1
R2	PL	TX power level	0.5mW	0	0	1	0							0	1	1
			1.0mW											1	0	
			2.0mW											1	1	
	ULD	Unlock detect	OFF										0			1
			ON										1			
	RAMWEB	For test	-									0				0
	TMOD	For test	-					0	0	0	0					0
R3	P	Program data for Synthesizer	P[7:0]	0	0	1	1									Note
R4	P	Program data for Synthesizer	P[13:8]	0	1	0	0									
	FR	For test	-					0	0							0

REGISTER	NAME	CONTENTS	SELECTION	ADDRESS				DATA								INITIAL (Hex)
				A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R5	ID	For test	-	0	1	0	1								0	0
	TST	For test	-									0	0	0		0
	TSTREG	For test	-								0					0
	MBBO	For test	-							0						0
	TEN	For test	-						0							0
	PEAU	For test	-					0								0
R6	POLA	For test	-	0	1	1	0								0	0
	CIA	Main synthesizer charge pump current	1.25uA										0	1		1
			80uA										1	1		
	CIB	Clock generator charge pump current	320uA								1	1				3
	POLB	For test	-							0						0
	TESC	For test	-						0							0
	TESCC	For test	-					0								0
R7	TEOS	For test	-	0	1	1	1							0	0	0
	PDTEST	For test	-										0			0
	CPO	For test	-								0	0				0
	SMTES	For test	-							0						0
	PESY	For test	-						0							0
	PERF	For test	-					0								0
R8	CEX	Local oscillator frequency extension	Band0	1	0	0	0							0	0	2
			Band1											0	1	
			Band2											1	0	
			Band3											1	1	
	FMG	For test	-									1	0			2
	FA	For test	-							0	1					1
	TAS	For test	-					0	0							0
R9	PAB	For test	-	1	0	0	1								0	0
	MPTEST	For test	-													0
R10			-	1	0	1	0									
R11	SEL_TEST	For test	-	1	0	1	1							0	0	0
	SEL_DATA	For test	-								0	0	0			0
R14	-	-	-	1	1	1	0									0

Note : In the case of P = 888 (for example).
Change a decimal numbers to a binary-coded form.
P = 888 の場合
10 進数を 2 進数へ変換する。
888→00001101111000（ = R4[5],・・・,R2[0],R1[7],・・・,R1[0]）

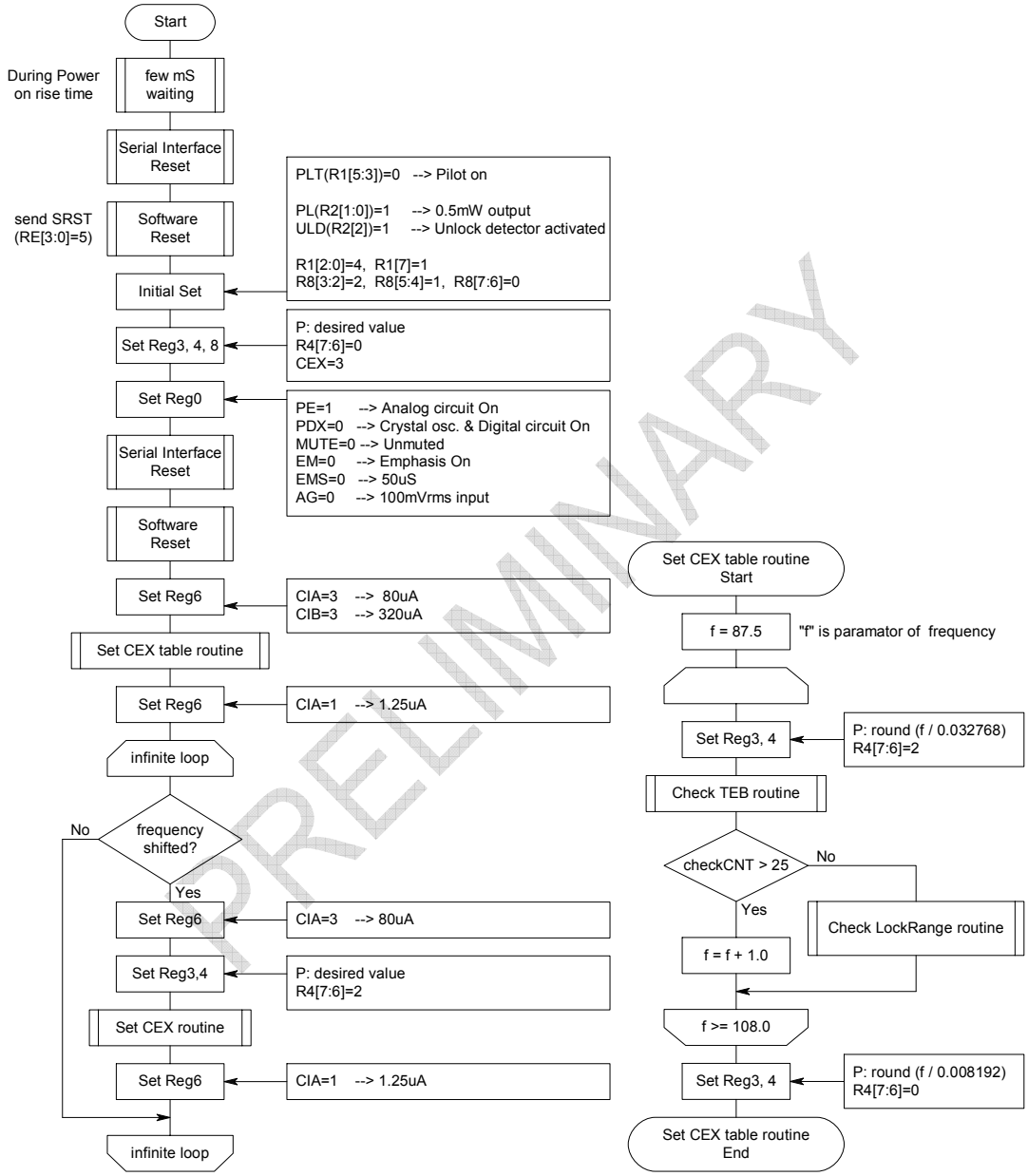
REGISTER	NAME	CONTENTS	SELECTION	ADDRESS				DATA								INITIAL (Hex)
				A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	
R3	P	Program data for Synthesizer	P[7:0]	0	0	1	1	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	
R4	P	Program data for Synthesizer	P[13:8]	0	1	0	0			**0**	**0**	**0**	**0**	**1**	**1**	
	FR	For test	-					0	0							0

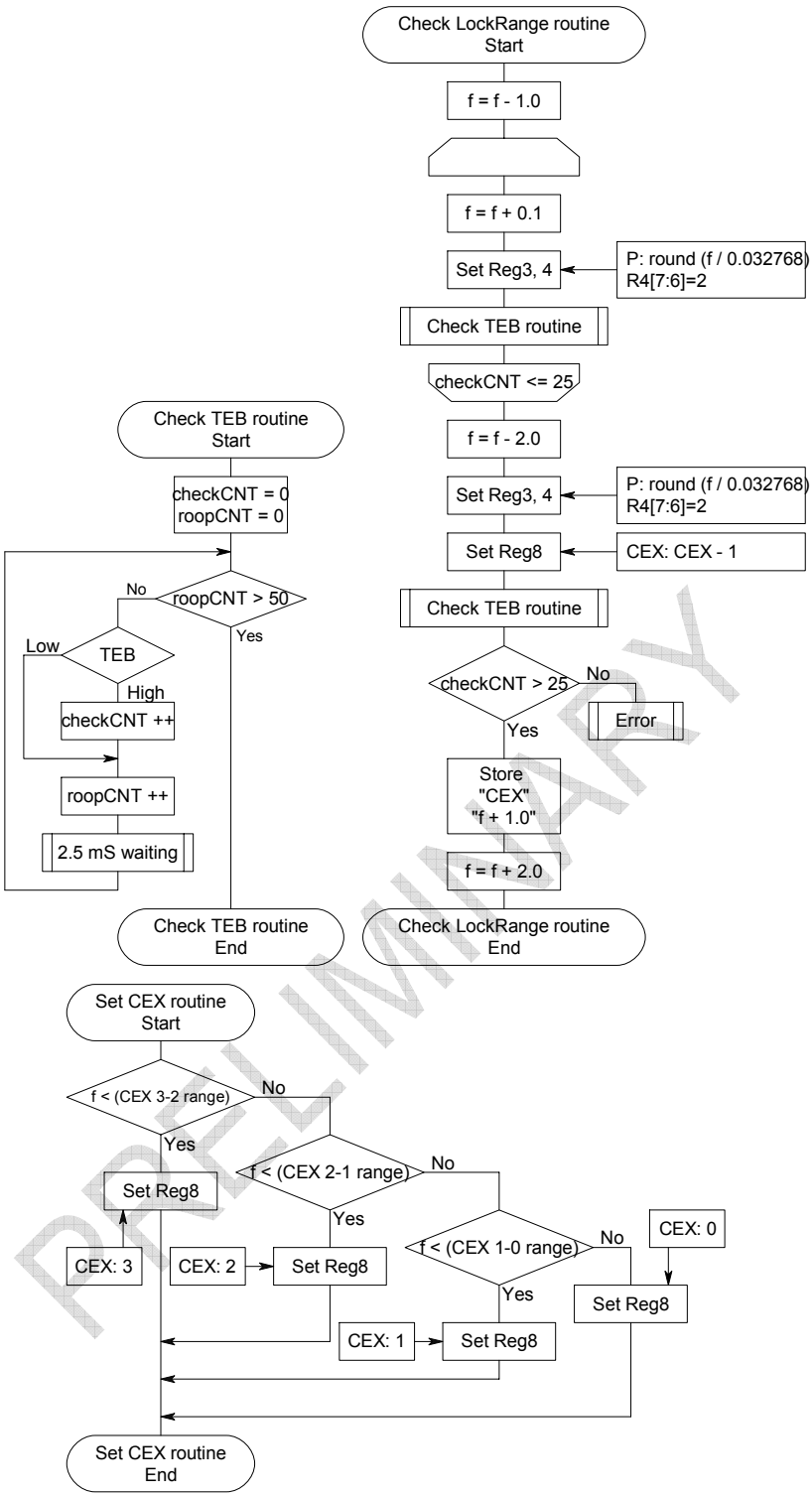
8.7. Controller basic operation routines

NS73 has power on reset circuit. Therefore, it takes few milli-seconds, until reaching the specified VDD.

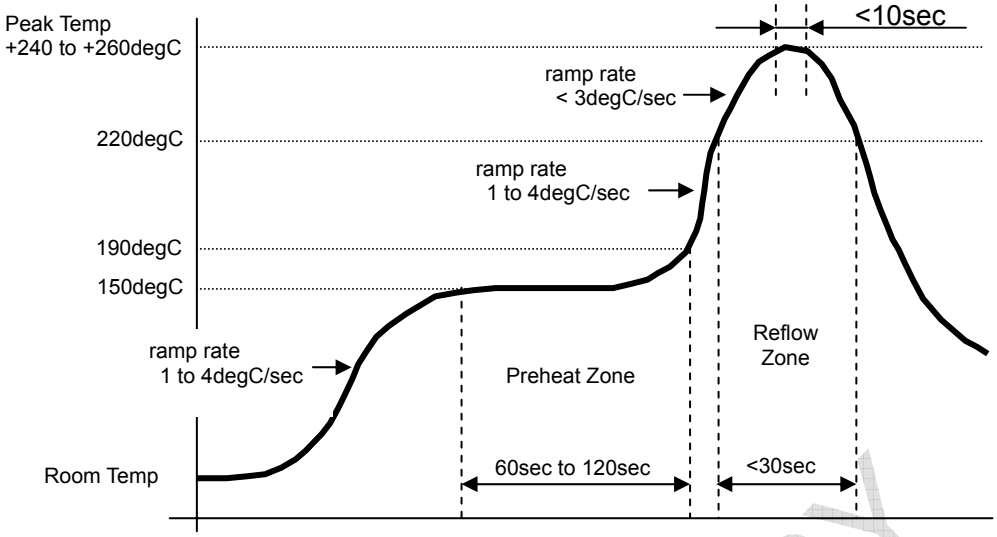
To make sure to reset, software reset can be applied.

Next step, set appropriate data to all registers, refer to register map.
During PE=0, the chip is in standby mode and data for all registers are backed up.
In PE=1 mode, chip will be activated and able to transmit signal.
The serial interface function is always operating even if PE=0.

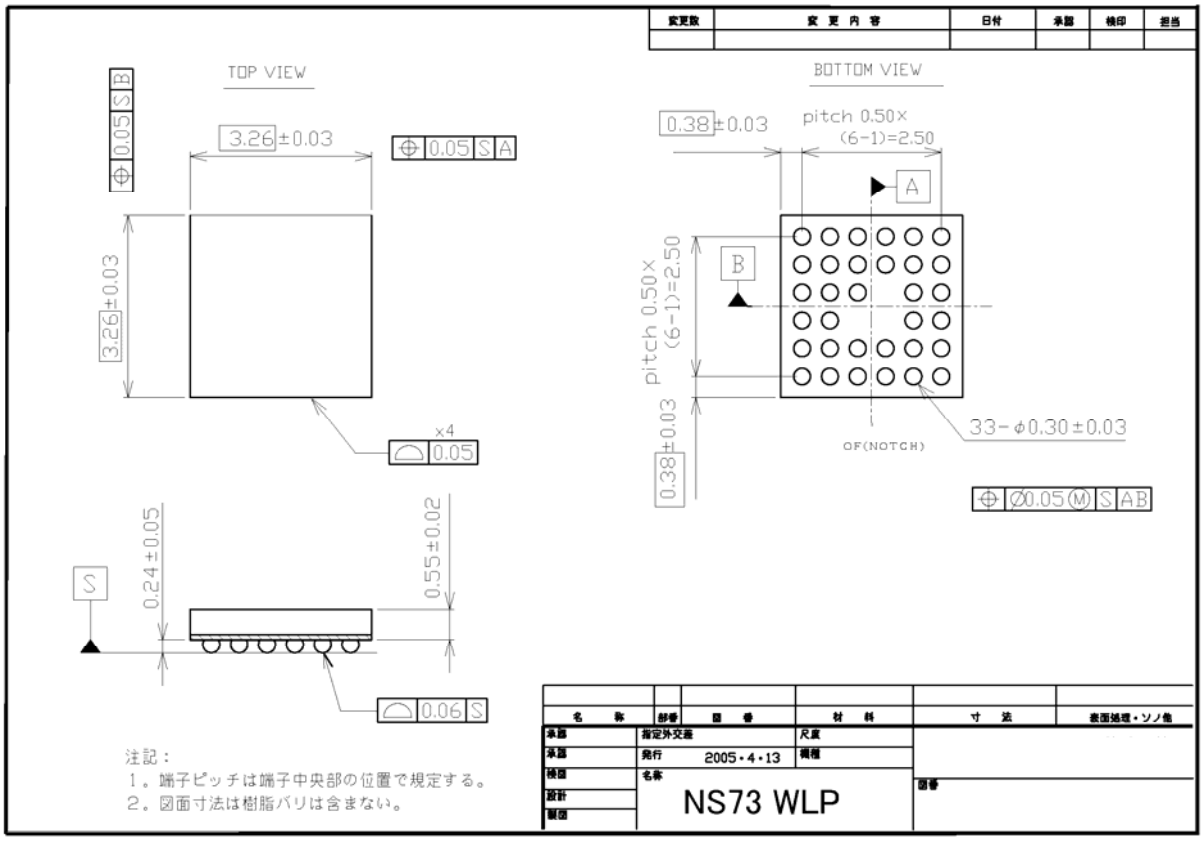




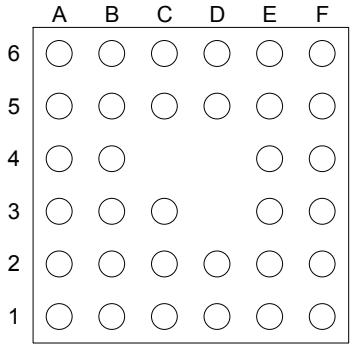
9. PbFREE Solder Reflow Profile; 鉛フリー・リフロープロファイル



10. Outer Dimension and Terminals for Connection; 外形寸法及び外部接続端子



11. Assignment of Pins; ピン配置

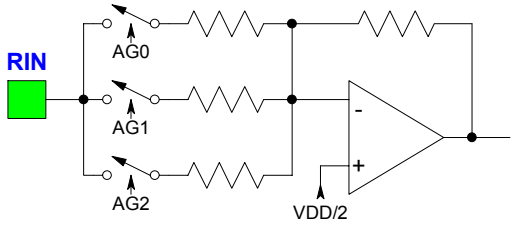
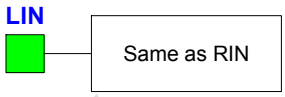
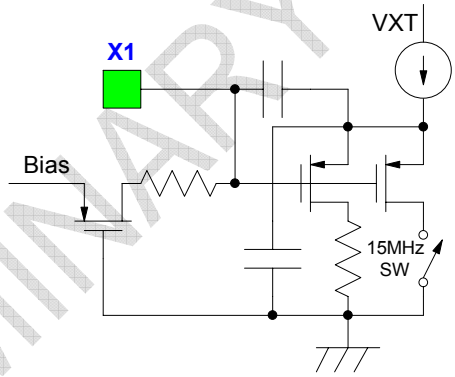
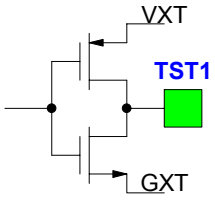
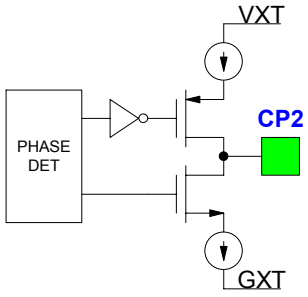


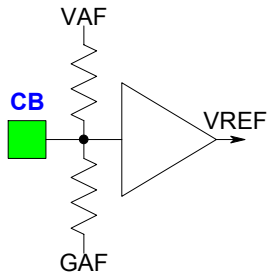
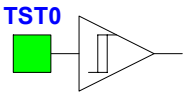
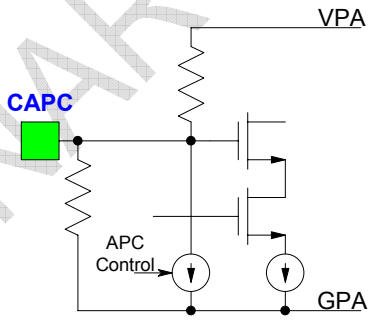
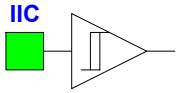
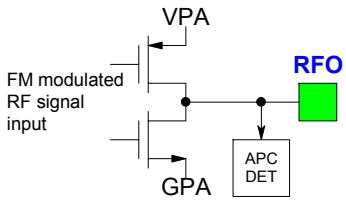
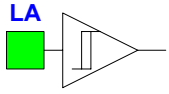
(Top View)

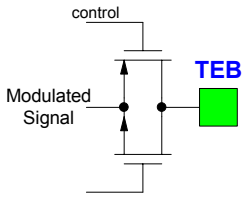
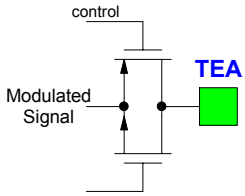
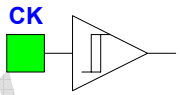
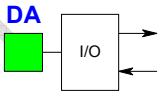
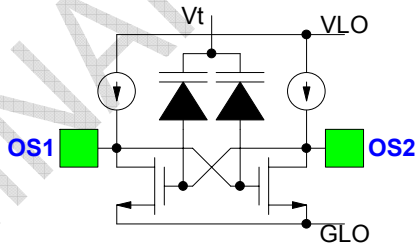
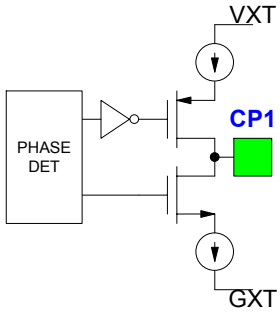
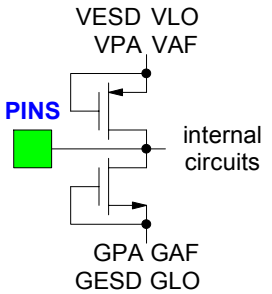
PIN NO.	PIN NAME	DESCRIPTION
A1	RIN	Audio Right signal input
A2	LIN	Audio Left signal input
A3	X1	Crystal or external signal Input
A4	GXT	Ground for Crystal oscillator
A5	TST1	Test output
A6	CP2	Charge Pump Output for Clock Gen.
B1	VAF	Audio VDD
B2	CB	De-coupling Capacitor for VDD/2
B3	VXT	VDD for Crystal oscillator
B4	TST0	Test Input
B5	VESD	VDD
B6	GNDD	Ground for Digital
C1	GAF	Audio Ground
C2	CAPC	Smoothing Capacitor for APC
C3	NC	Non Connection
C5	GESD	Ground
C6	IIC	I^2C or 3-wire I/F selector 0=3-wire, 1=I^2C
D1	GPA	RF Power amp ground
D2	RFO	RF Power output
D5	LA	Latch for 3-wire or Address for I^2C
D6	VDDD	Digital VDD
E1	VPA	RF Power amp VDD
E2	VLO	LO VDD
E3	TEB	Unlock Detect output
E4	TEA	PE output
E5	CK	Clock for I/O Input (Pull up R needed)
E6	DA	Data I/O for I/F (Pull up R needed)
F1	OS1*	LO tank circuit-1
F2	OS2*	LO tank circuit-2
F3	GLO	LO ground
F4	CP1	Charge Pump output for Main Synthesizer
F5	VSY	VDD for Synthesizer
F6	GSY	Ground for Synthesizer

*) Note: Pins F1(OS1) and F2(OS2) are only 100V HBM ESD protected.

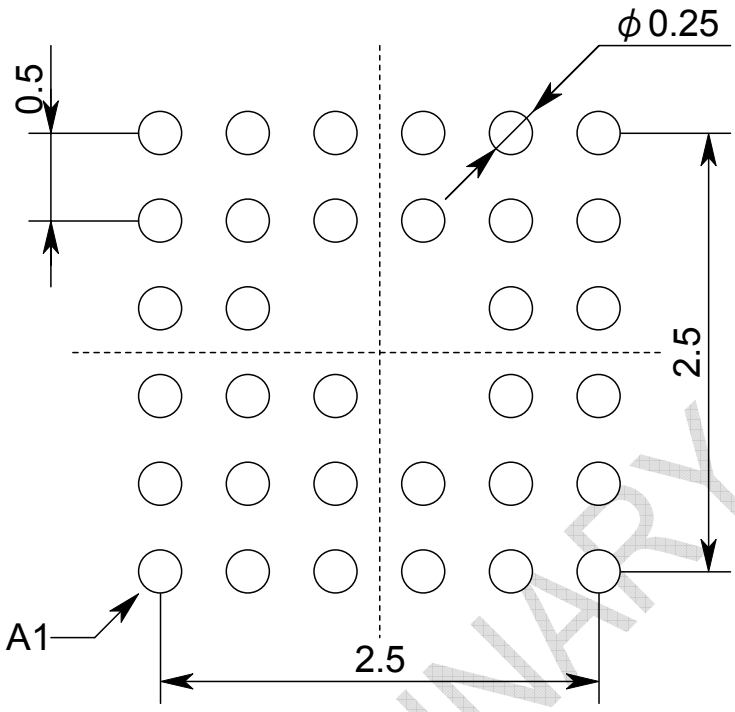
12. Internal Pin Configuration; 端子内部構成

PIN NO.	PIN NAME	DESCRIPTION
A1	RIN (AIP) [VDD/2]	Audio Right signal input 
A2	LIN (AIP) [VDD/2]	Audio Left Signal Input 
A3	X1 (AIP) [0.6V]	Crystal or external input connection 
A4	GXT (AIP) [0V]	Ground for Crystal Oscillator
A5	TST1 (DOP) [Logic level]	Logic test output. Open this pin. 
A6	CP2 (AOP) [HiZ]	Charge Pump output of synthesizer for system clock generation. 
B1	VAF (AIP) [VDD]	Power Supply for Audio block

PIN NO.	PIN NAME	DESCRIPTION
B2	CB (AIP) [VDD/2]	De-coupling cap. For Reference voltage 
B3	VXT (AIP) [VDD]	Power supply for Crystal Oscillator. Connect to power supply.
B4	TST0 (DIP) [Logic level]	Logic test input(Schmitt) Connect ground. 
B5	VESD (AIP) [VDD]	Power Supply for ESD diode. Connect to VDD.
B6	GNDD (AIP) [0V]	Ground for Digital block
C1	GAF (AIP) [0V]	Ground for Audio block
C2	CAPC (AIP) [2.2V]	Smoothing Capacitor for Automatic Power Control(APC) 
C3	NC	Non Connection
C5	GESD (AIP) [0V]	Ground for ESD diode. Connect to GNDD.
C6	IIC (DIP) [0V]	3-wire or I^2C bus serial interface selection. (Schmitt) 0= 3-wire 1= I^2C 
D1	GPA (AIP) [0V]	Ground for RF Power Amp.
D2	RFO (AOP) [VDD/2]	RF Power Amp output 
D5	LA (DIP) [Logic level]	LATCH input for 3-wire I/F ADDRESS extension for I^2C bus. 
D6	VDDD (AIP) [VDD]	Power Supply for Digital block
E1	VPA (AIP) [VDD]	Power Supply for RF Power Amp.
E2	VLO (AIP) [VDD]	Power Supply for Local Oscillator

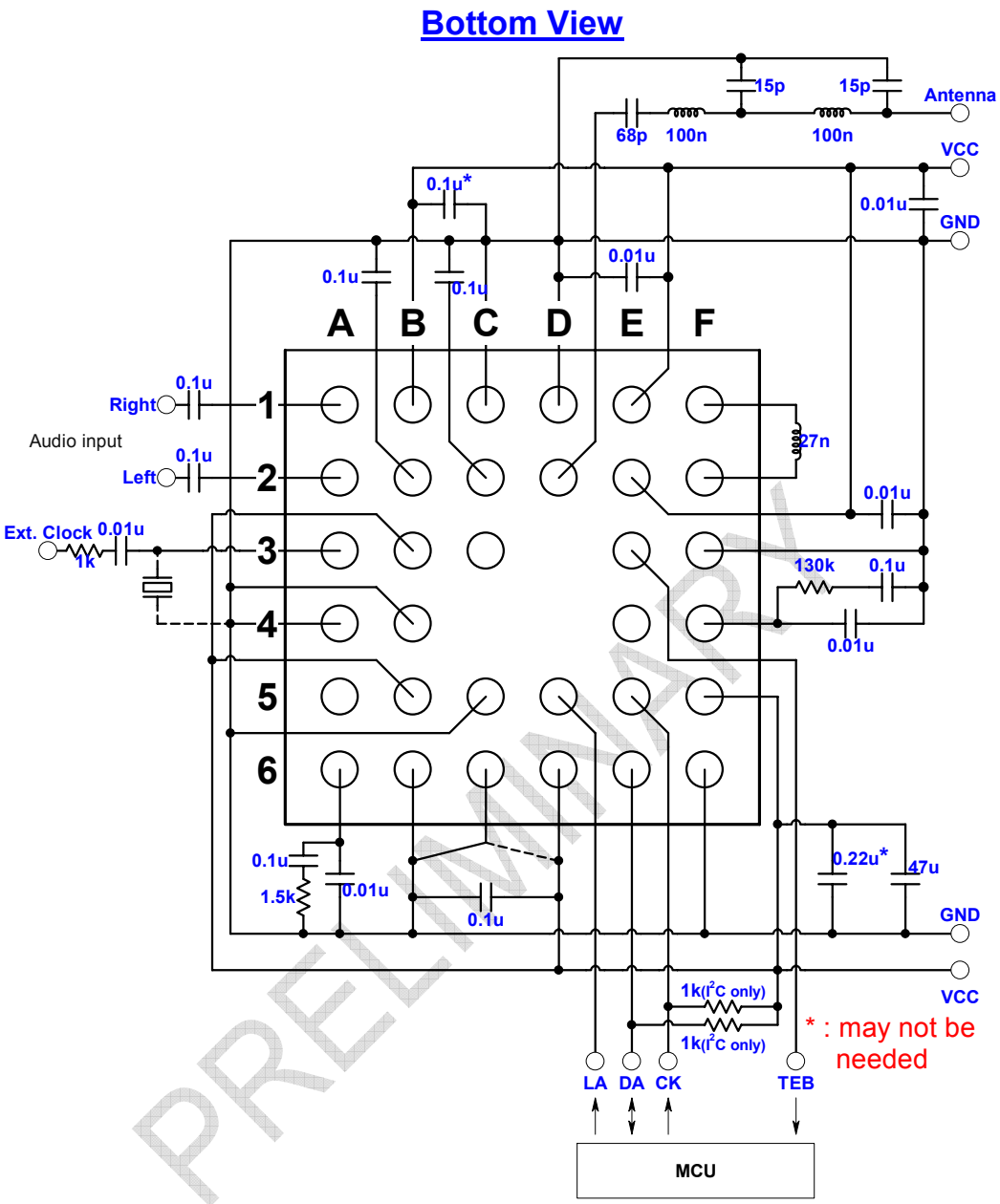
PIN NO.	PIN NAME	DESCRIPTION
E3	TEB (AIO) [Logic level]	Unlock Detect output 
E4	TEA (AIO) [Logic level]	PE output 
E5	CK (DIP) [Logic level]	Clock pulse input for serial I/F Pull up, 1k ohm, required 
E6	DA (DIOP) [Logic level]	DATA input for 3-wire DATA input & output for I^2C. Pull up, 1k ohm, required. 
F1	OS1 (AIP) [0.5V]	Inductor connection of Tank circuit 
F2	OS2 (AIP) [0.5V]	Inductor connection of Tank circuit
F3	GLO (AIP) [0V]	Ground for Local Oscillator
F4	CP1 (AOP) [HiZ]	Charge Pump output for Synthesizer 
F5	VSY (AIP) [VDD]	Power supply for Synthesizer. Connect to VDDD.
F6	GSY (AIP) [0V]	Ground for Frequency Synthesizer. Connect to GNDD.
All	AIP AOP AIO DIP DOP DIO	All pins should have ESD protection diodes as shown below; 

13. Recommended foot pattern; 推奨フットパターン



Foot Pattern (Top View)

14. Application Circuit ; 応用回路



15. Appearance Specification; 外観規格

(1) As for marking disappearance and partial marking lack, if the contents can be deciphered, the defect will be unquestioned.
表示の消え、欠けについて、表示内容が判読可能なものは不問とする。

(2) As for a position gap of marking, it should not overflow from a package.
表示の位置ズレについては、パッケージよりはみ出さないこと。

(3) Complete lack of marking, written mistakes and direction errors are regarded disqualified.
表示が無いものや記載に誤りがあるもの、方向に誤りがあるものは不合格とする。

(4) As for the crack and discoloration of a package, if the contents of marking can be deciphered, the defect will be unquestioned.
パッケージのキズや変色については、表示内容が判読可能なものは不問とする。

16. Notes of use ; 使用上の注意事項

16.1. Notes of designing the board; 設計時の注意事項

(1) Follow the conditions written in the specification.
本仕様書に記載されている条件は必ず守ってください。

(2) This IC should not be stressed when installed.
本製品を取り付けの際は応力がかからないような取り付けをお願いします。

(3) Keep this IC away from heat sources
本製品は熱源から離して設置してください。

(4) Use stable power supply and be careful not to add over voltage, opposite voltage, noise and spike.
供給電源には、安定したものを使用し、過電圧，逆電圧，雑音，スパイクなどが加わらないようにしてください。

(5) Keep this IC away from high-frequency noise area.
本製品の近辺には高周波雑音を発生する回路を配置しないよう願います。

(6) Follow the conditions of interface specifications when using control signals to control this IC.
本製品の制御に必要なコントロール信号については、インターフェース条件を必ず守ってください。

(7) Use the specified impedance for the input/output terminals.
各入出力端子は指定のインピーダンスでご使用ください。

16.2. Notes of installation; 実装上の注意事項

(1) Baking process cannot be done on the embossed tape. Please carry out the ICs on a tray specified by our company and conduct the baking process under the condition of +125degC, 4 hours. Please be sure to carry out reflowing within the appointed time [15.4 (1)].
エンボステープはベーキング処理が出来ません。ベーキング処理は弊社指定のトレイにて +125degC、4 時間を実施してください。必ず指定時間以内にリフロー半田付けを実施してください[15.4 (1)]。

(2) Please refer to the reflow conditions in data[9th section].
リフロー条件は添付のリフローデーター[第 9 項]を参考にしてください。

(3) This package should not be stressed or vibrated when reflowed.
リフロー中はパッケージに振動を与えないでください。

(4) Please make packaging circuit inside so that a light does not enter.
実装回路は、内部に光が入らないように作成してください。

(5) Refer to the recommended pattern when designing the board.
基板設計の際は推奨パターンを参考に作成願います。

16.3. Notes of usage conditions; 取り扱い時の注意事項

(1) Be careful against static electricity.
取り扱い時、静電気防止対策等の配慮を願います。

(2) Do not use an IC once fallen.
単体で落下した製品は使用しないでください。

(3) Follow the descriptions for power supplying.
供給電源については定格を必ず守ってください。

(4) Do not touch the pins directly by bare hands. May deteriorate the soldering strength.
端子に直接手を触れると、半田付け性が劣化しますのでご注意ください。

16.4. Notes of storage; 保管上の注意事項

(1) When stored in moisture-proof bag under storage conditions 5 to 30degC, 65% RH (Relative humidity) or less, the shelf life will be within 12 months (from date of shipping). After the bag opened, it must be reflowed to a PCB within 192 hours with the stored condition 5 to 30degC, 65% RH or less. When the appointed period has exceeded after opening the bag, please carry out the baking process on the tray specified by our company under the condition of +125degC, 4 hours.
防湿梱包状態で保存する場合，5～30degC，65% RH (相対湿度) 以下にて 12 ヶ月以内(出荷年月日から)、開封後は 5～30degC，65% RH 以下にて 192 時間以内にリフロー半田付けを実施してください。開封後、指定期間を超えた場合は+125degC、4 時間のベーキング処理を弊社指定のトレイにて実施してください。

(2) Store in an environment of no heat, high humidity, dust nor corrosive gas.
高温、多湿、塵埃、腐食性ガスのない環境で保管してください。

(3) Dropping or piling by bulk may cause damage.
落下やバラ積みは、破損の恐れがありますのでご注意ください。

16.5. Notes of others; その他の注意事項

(1) This specification sheet includes know how and copyrights we own. Please do not disclose this to any third party.
本仕様書は、弊社の著作権，ノウハウに関する内容が含まれていますので、第3者には開示しないように願います。

(2) Please do not use this product for purposes not agreed with NIIGATA SEIMITSU Co.,Ltd.
本製品を弊社と合意した用途以外の目的に使用しないでください。

(3) Be sure to provide an appropriate fail-safe function on your product to prevent secondary damages that may be caused by an abnormal function or a failure of our product. We assume no responsibility whatsoever for accidents resulting in injury or death, fire accidents and other serious accidents by unsuitable use.
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17. Revision; 改訂履歴

Date; 日付	Revision; 内容	Issued 担当	Approved 承認
2005/12/26	Change control routine	M.Tsubokawa	H.Miyagi
2005/12/21	First Edition	M.Tsubokawa	H.Miyagi