Wireless Sensor Networks
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TmoteSky Theory of Operations

Overview

Tmote Sky is the next-generation wireless sensor module (mote) platform for extremely low power, high data-rate, sensor network applications designed with the dual goal of fault tolerance and development ease. Tmote Sky boasts the largest on-chip RAM size (10kB) of any mote, the first IEEE 802.15.4 radio, and an integrated on-board antenna providing up to 125 meter range. Tmote Sky offers a number of integrated peripherals including a 12-bit ADC and DAC, Timer, I2C, SPI, and UART bus protocols, and a performance boosting DMA controller. Tmote Sky offers a robust solution with hardware protected external flash (1Mb in size), applications may be wirelessly programmed to the Tmote Sky module. In the event of a malfunctioning program, the module loads a protected image from flash. Toward development ease, Tmote Sky provides an easy-to-use USB protocol for programming, debugging and data collection. Designed with applications in mind, the Tmote Sky module is FCC certifiable and may be added into existing products.

With TinyOS support out-of-the-box, Tmote Sky leverages emerging wireless protocols and the open source software movement. Tmote Sky is part of a line of modules featuring on-board sensors to increase robustness while decreasing cost and package size.

CC2420 Transceiver

The RX side of the EM2420 transceiver uses a differential RF input into a broadband LNA. The amplified signal is downconverted to a 2 MHz IF and subsequently filtered and converted to digital format. The digital demodulator module performs automatic gain control, mirror suppression, channel filtering, symbol and frame synchronization, and signal power estimation. The demodulated binary data are buffered in an on-chip FIFO and are available via a serial interface.

In transmit mode (TX), the CC2420 transceiver buffers incoming serial data in the on-chip FIFO. These data are mapped using the 802.15.4 spreading sequence and fed to the O-QPSK digital modulator. DAC modules perform direct conversion on the modulator output to produce a 2.4 GHz analog signal. This signal is filtered and fed to an internal software-controlled PA. Balanced circuit designs throughout the transmitter help to preserve signal quality.

The CC2420 transceiver's main reference clock oscillator is built-in, requiring only an external clock resonator. The package also includes a frequency synthesizer using a fully integrated LC VCO and PLL loop filter. The antenna interface is often a simple LC matching network, consisting of only a few passive components. The high level of integration means that a typical design requires only a resonator, 2 capacitors, a bias resistor, and matching network.

Message processing and buffering features included in the transceiver package reduce the memory and processing load on the MPU. Independent incoming and outgoing FIFO memory provides message buffering and eases timing constraints. Automatic address decoding, CRC validation, and acknowledgement generation reduce the bookkeeping load on the microprocessor. A built-in encryption engine provides both stand-alone and in-line AES-128 encryption for tasks such as secure transmission and authentication. The physical interface consists of a four-wire, high-speed, synchronous serial connection for configuration and data. Four additional status lines provide an interrupt trigger and flow control information.

For more detailed description of CC2420 capabilities, consult CC2420 Datasheet at http://www.chipcon.com/files/CC2420_Data_Sheet_1_2.pdf

Protocol Stack Implementation

TinyOS protocol stack uses a CSMA-CA (carrier sense multiple access) MAC to arbitrate between transmitters. When a command to transmit is issued, the transmitter performs a randomized backoff period, followed by a clear channel assessment; if the channel is determined to be clear, the packet transmission follows. As a result of the randomized delay, packet setup delay and clear channel assessment, the minimum interval between packets is 4 ms. A maximum TinyOS packet length is 36 bytes; with 10 bytes reserved for header information; since the data is transmitted at 250 kbps, the maximum packet time is 1.2 ms.

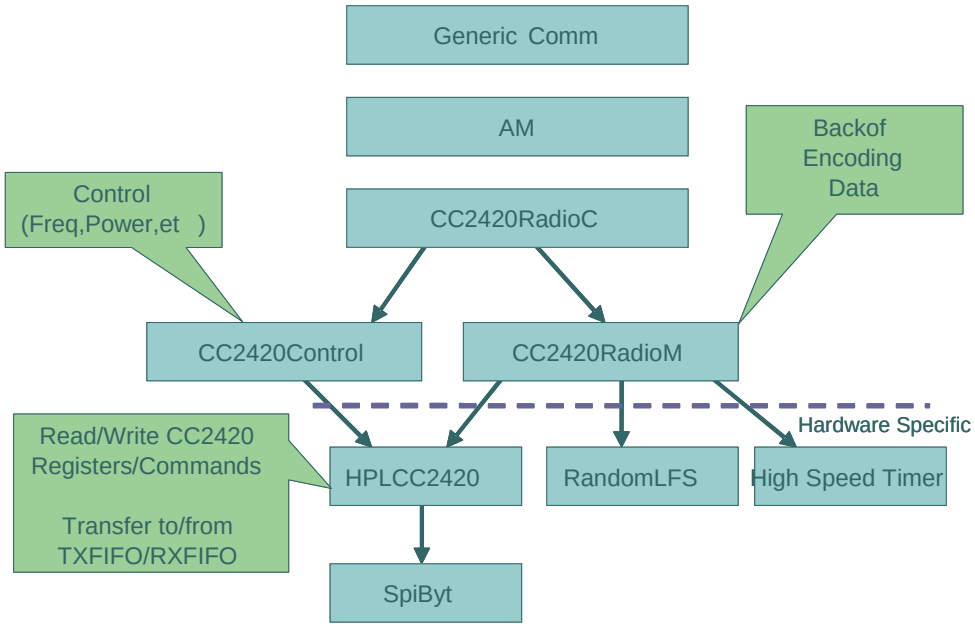

Figure 1: TinyOS radio stack implementation on TmoteSky

The protocol stack is best suited for low duty cycle operation, where the device spends 99% of the time asleep, and 1% of the time active. The microcontroller can transition from sleep to active mode in less than 6 microseconds; the radio can start receiving packets in as little as 1.6ms from turn on time.