

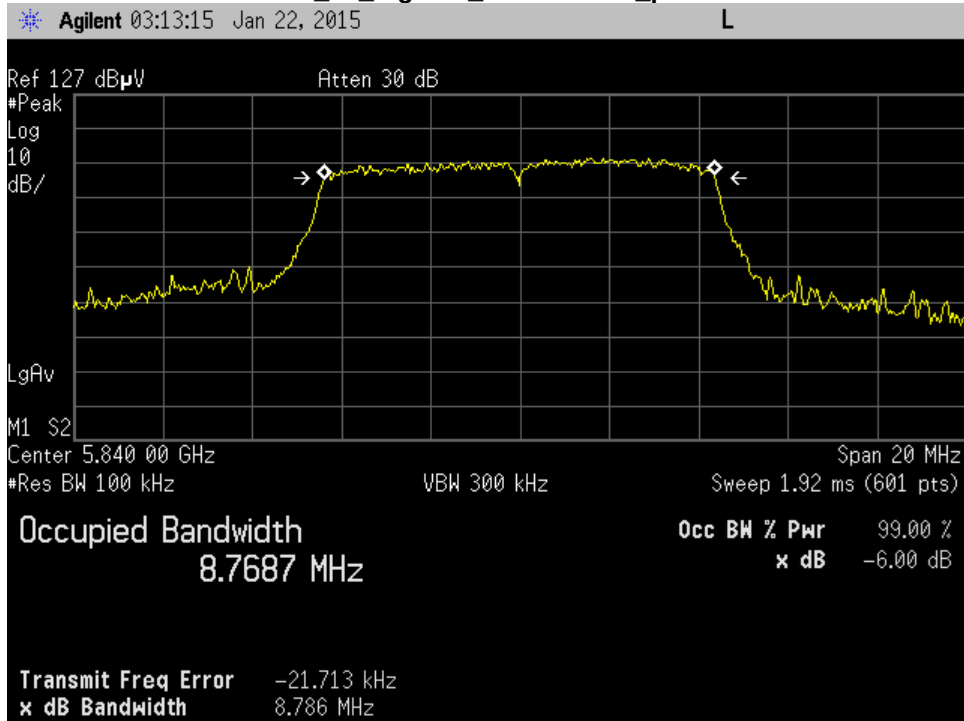


# **Annex D**

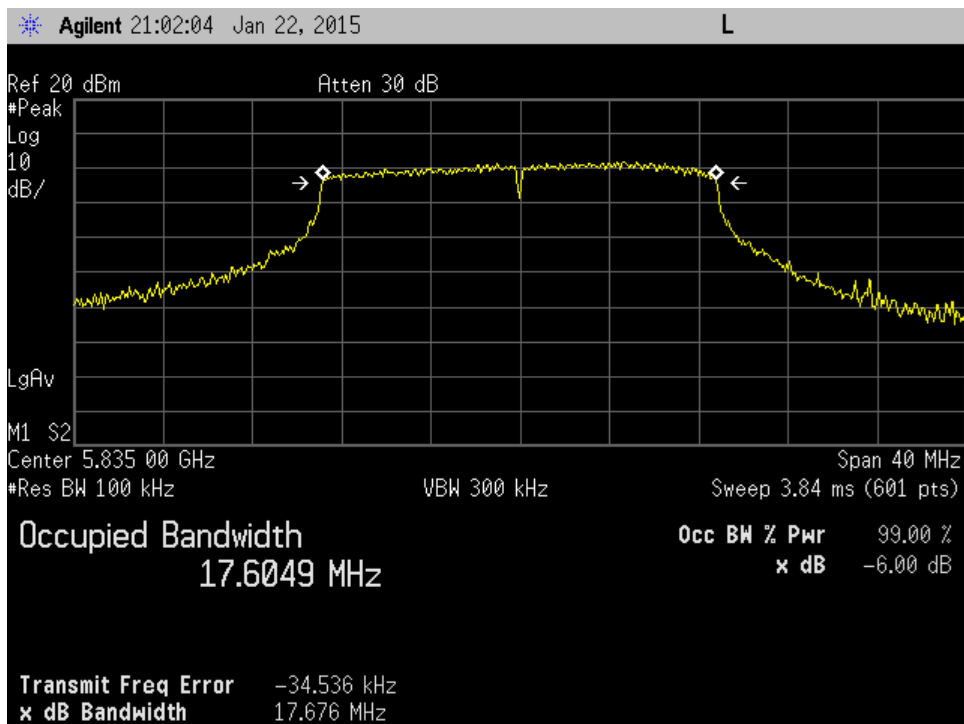
## **Occupied Bandwidth**



### OCC BW\_J1\_high ch\_bw=10 MHz \_p14a0028

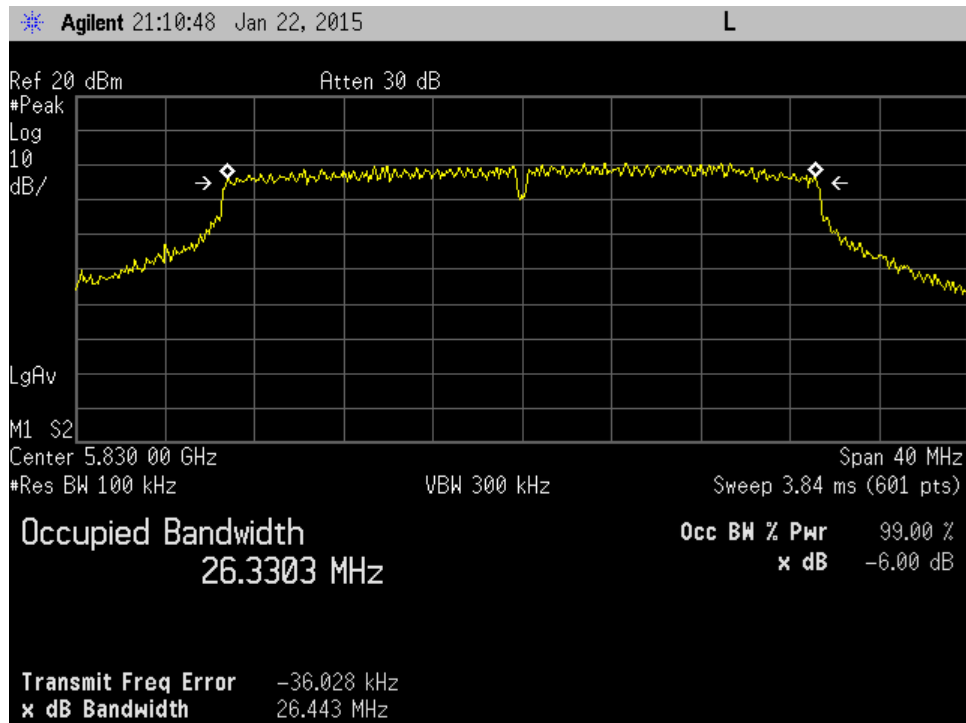


### OCC BW\_J1\_high ch\_bw=20 MHz \_p14a0028

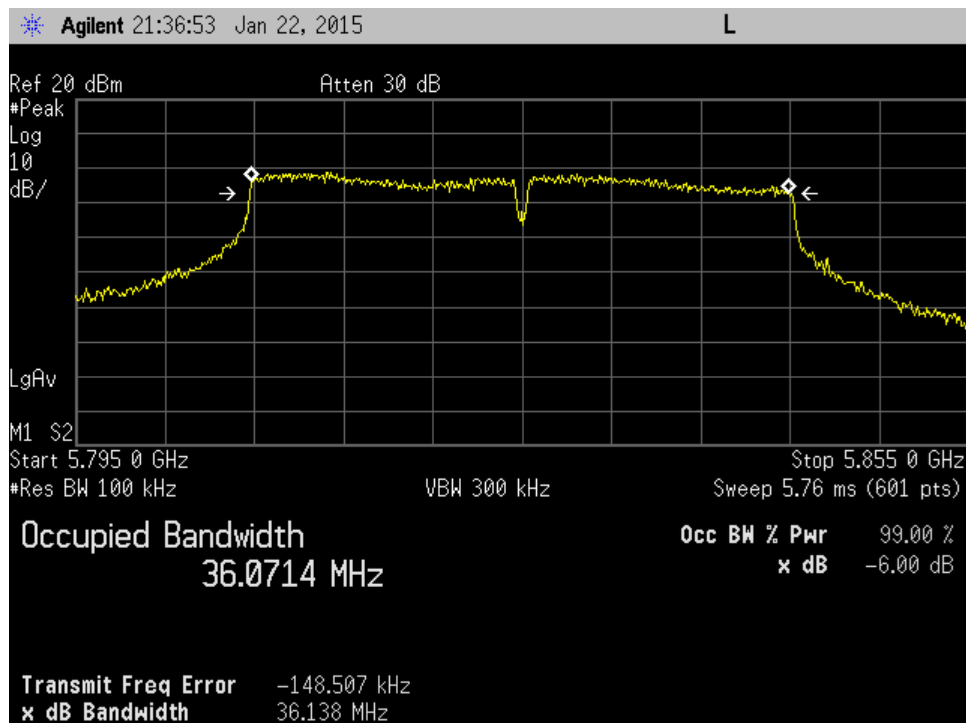




**OCC BW\_J1\_high ch\_bw=30 MHz \_p14a0028**

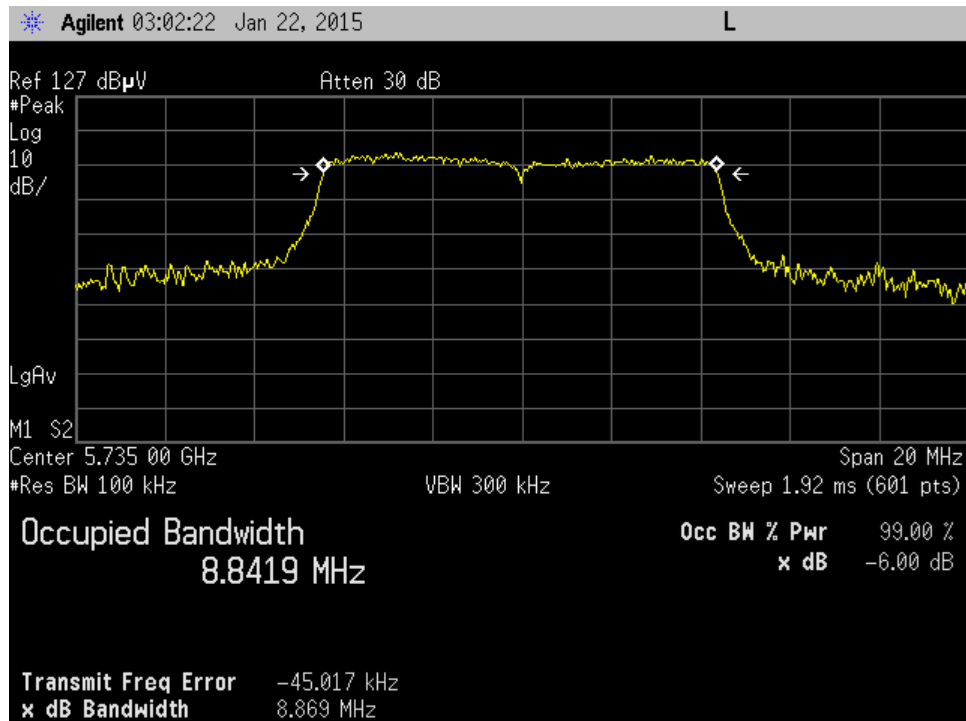


**OCC BW\_J1\_high ch\_bw=40 MHz \_p14a0028**

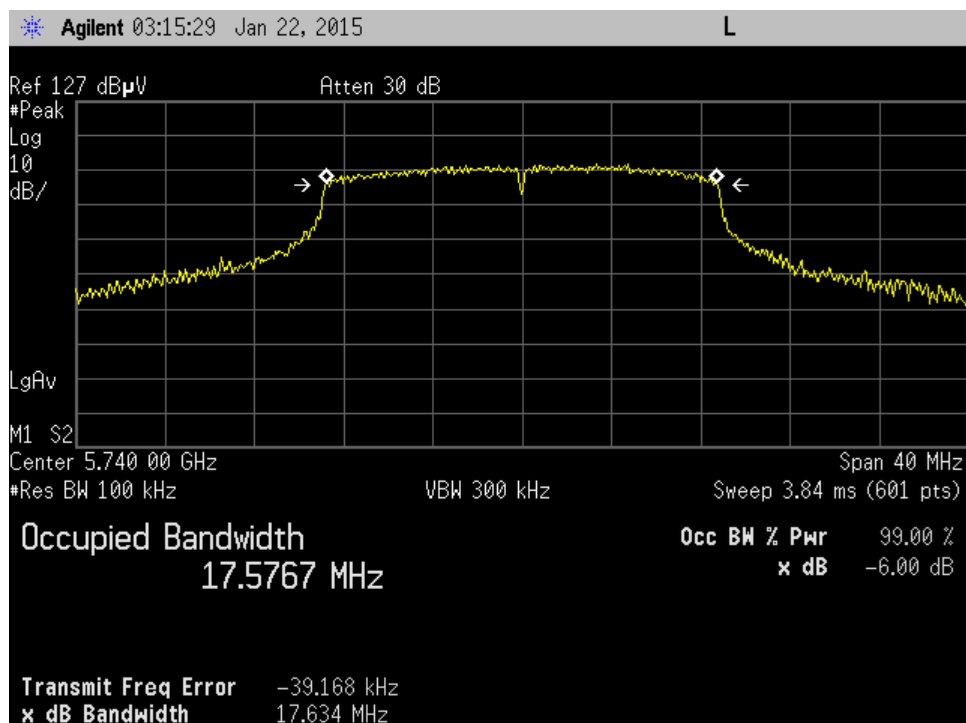




**OCC BW\_J1\_low ch\_bw=10 MHz \_p14a0028**

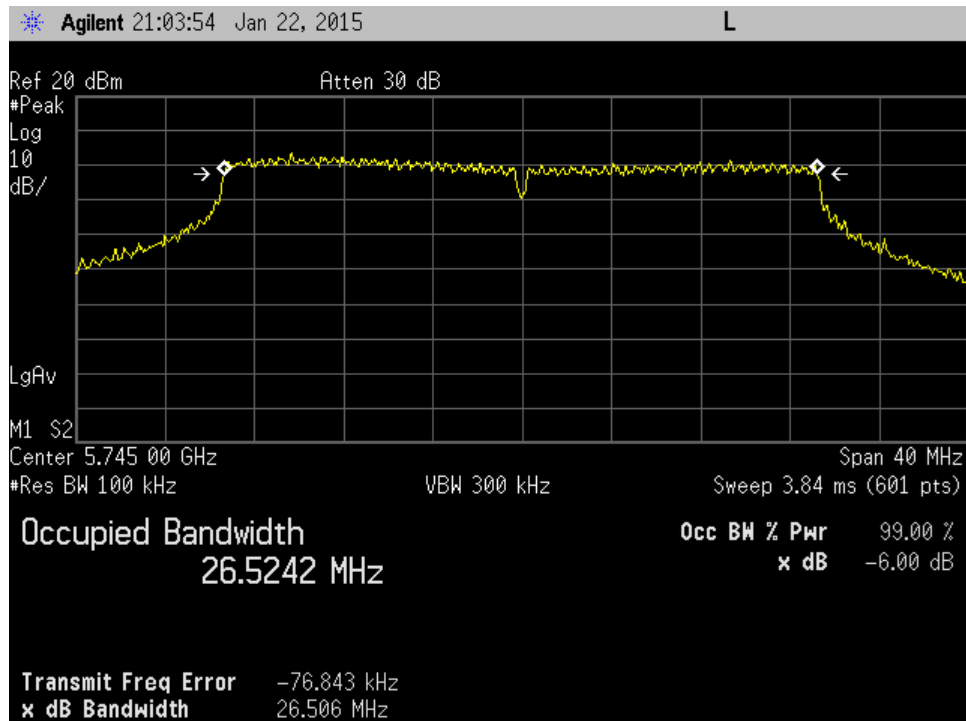


**OCC BW\_J1\_low ch\_bw=20 MHz \_p14a0028**

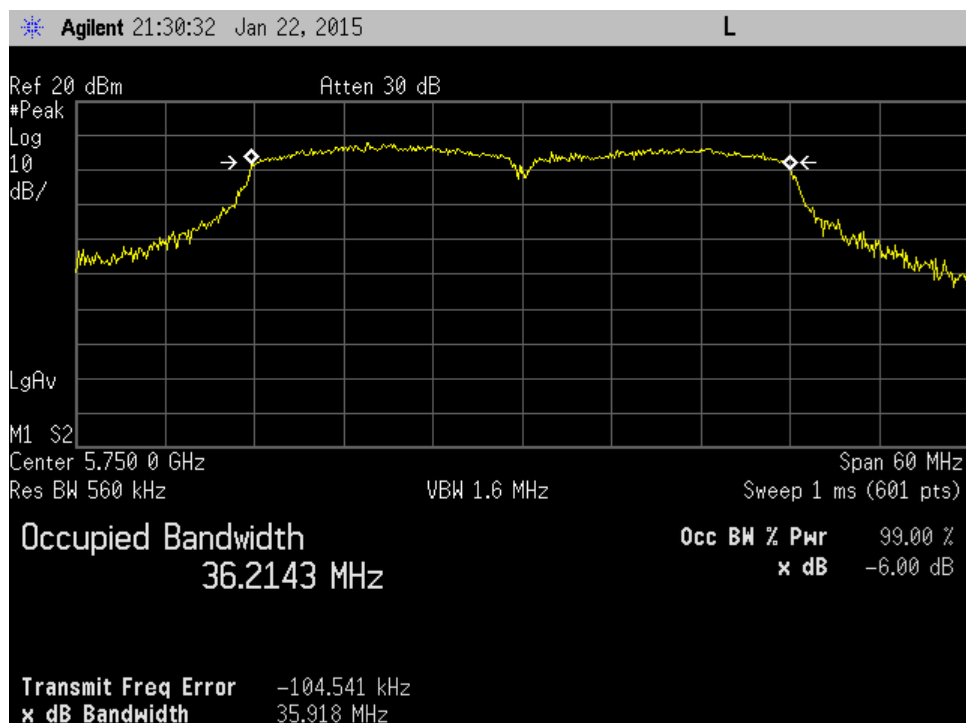




**OCC BW\_J1\_low ch\_bw=30 MHz \_p14a0028**

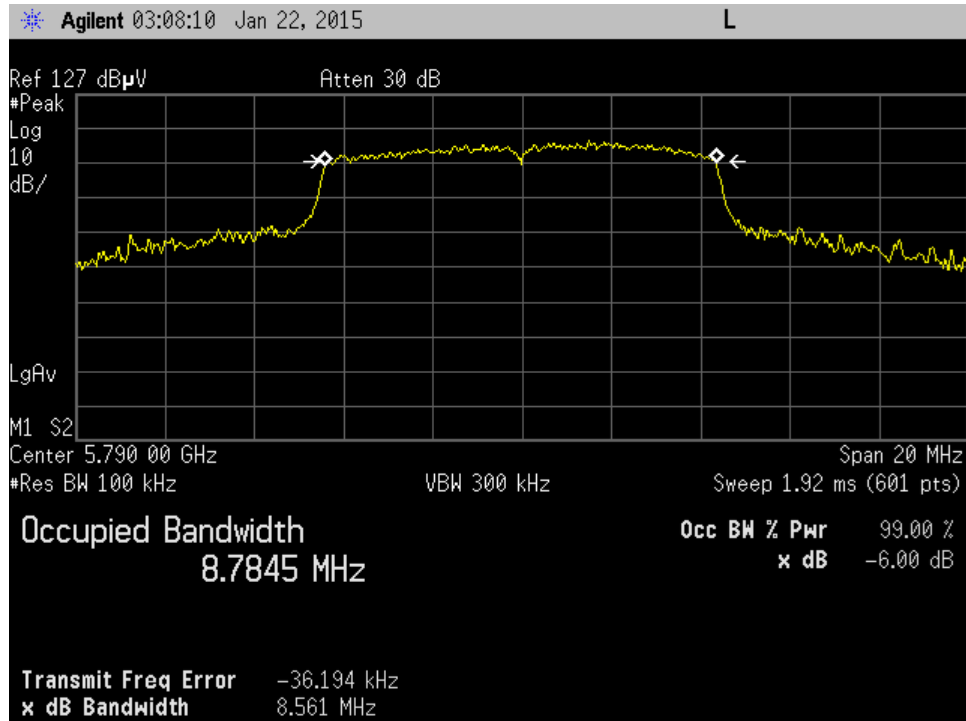


**OCC BW\_J1\_low ch\_bw=40 MHz \_p14a0028**

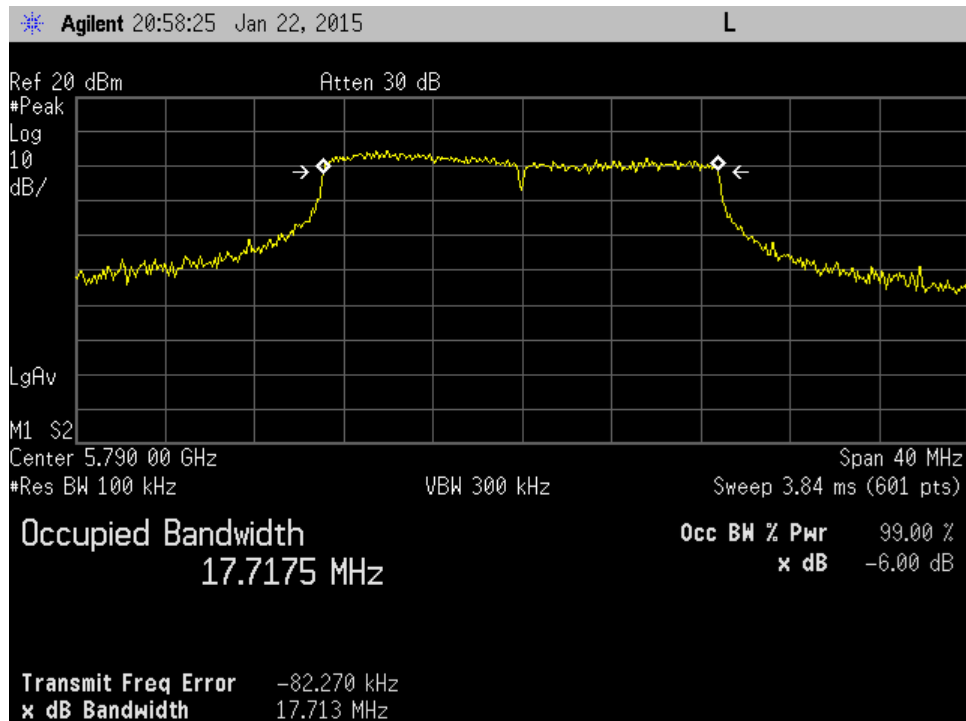




**OCC BW\_J1\_mid ch\_bw=10 MHz \_p14a0028**

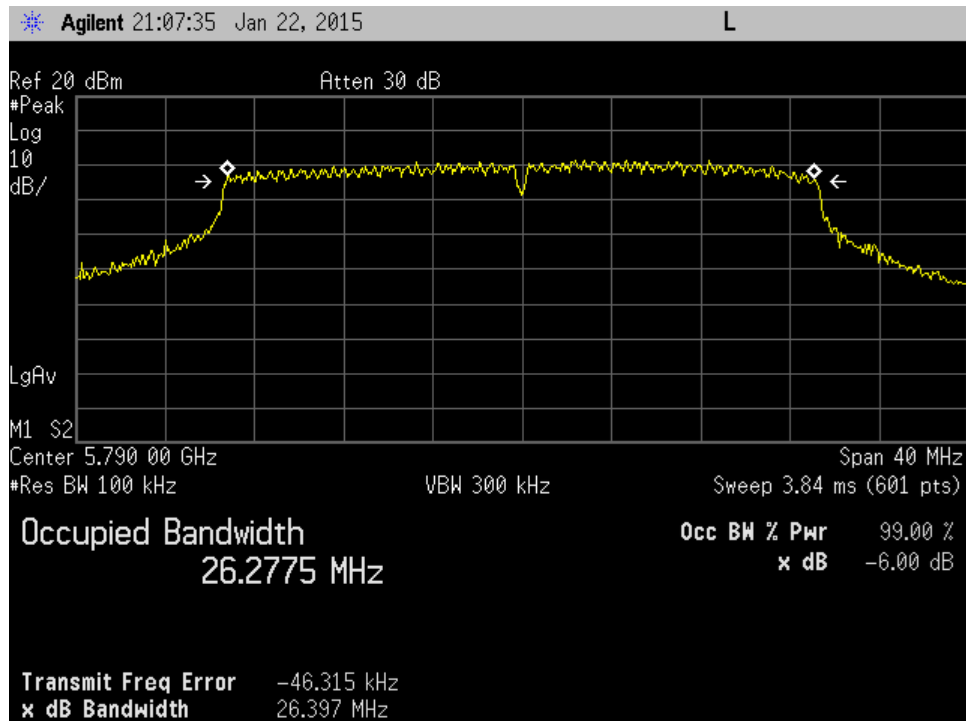


**OCC BW\_J1\_mid ch\_bw=20 MHz \_p14a0028**

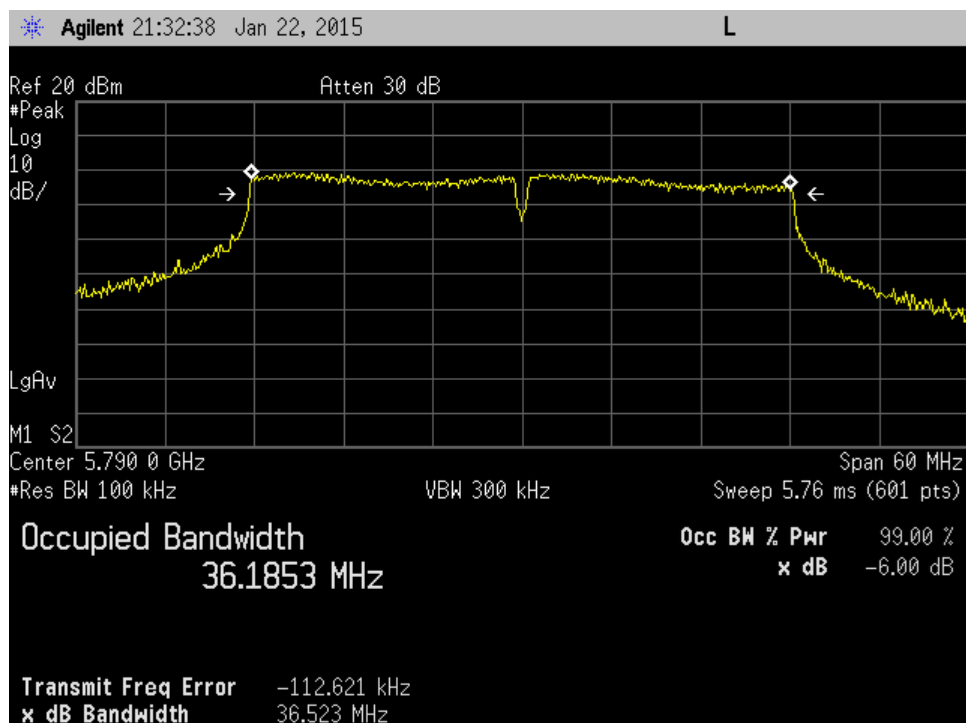




**OCC BW\_J1\_mid ch\_bw=30 MHz \_p14a0028**

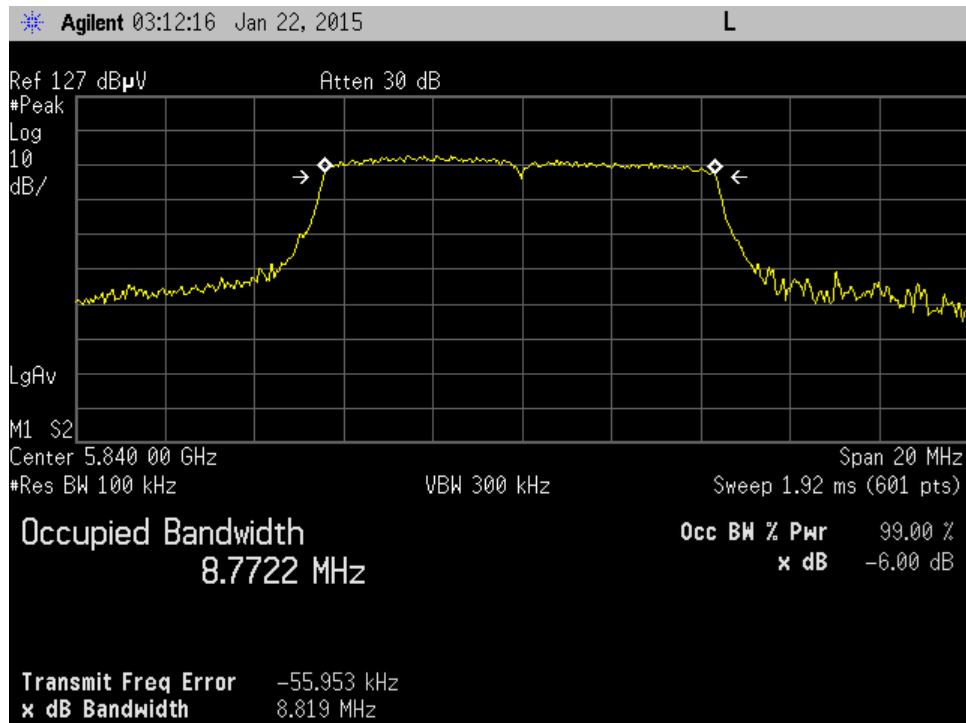


**OCC BW\_J1\_mid ch\_bw=40 MHz \_p14a0028**

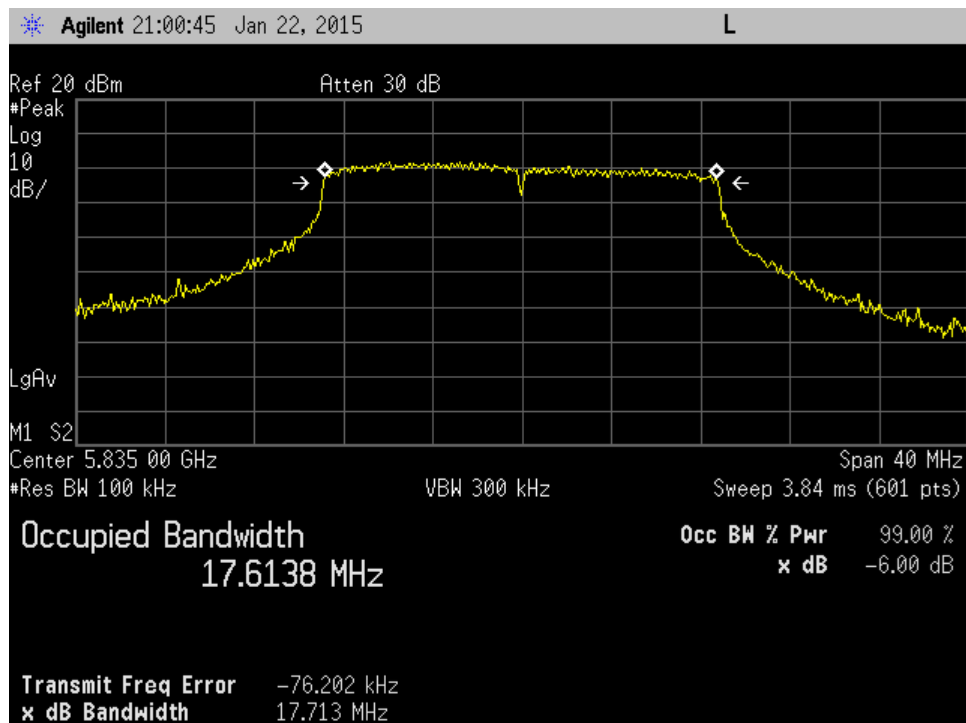




**OCC BW\_J3\_high ch\_bw=10 MHz \_p14a0028**

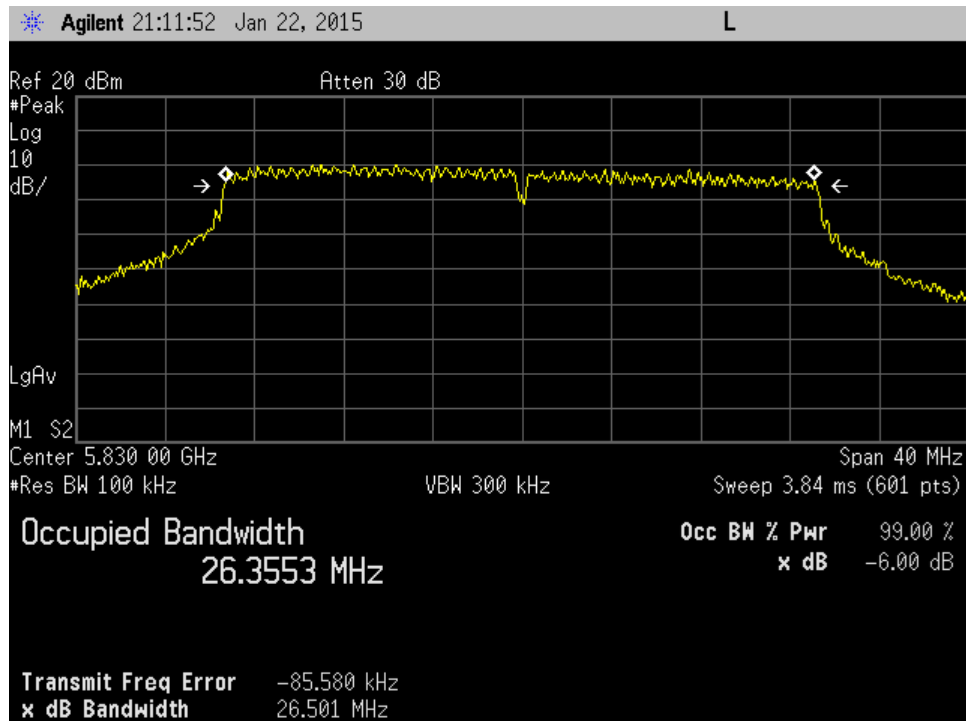


**OCC BW\_J3\_high ch\_bw=20 MHz \_p14a0028**

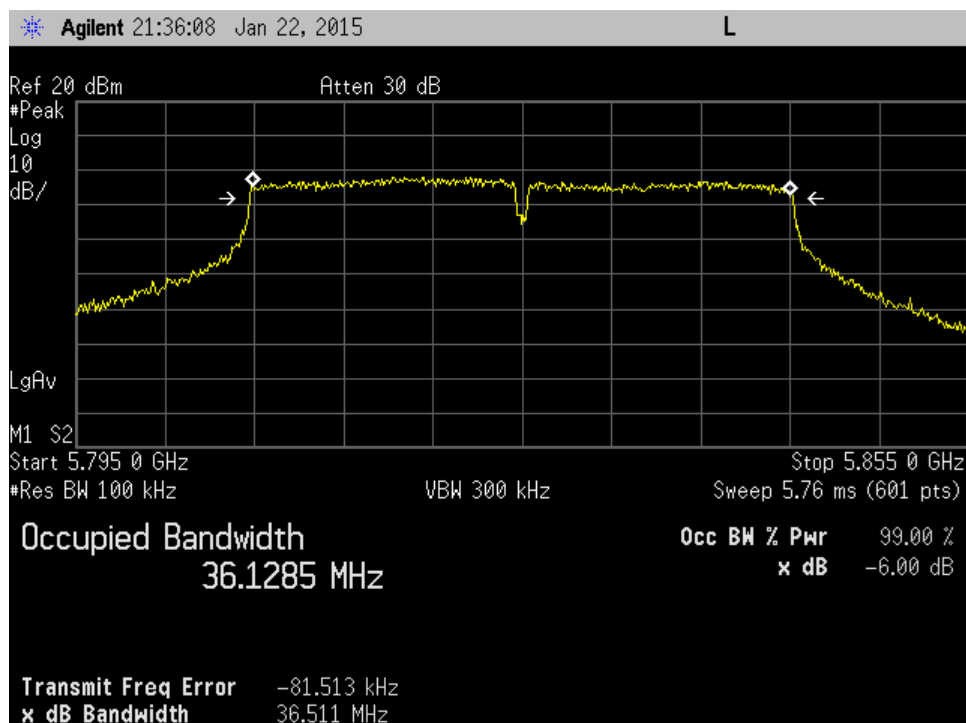




**OCC BW\_J3\_high ch\_bw=30 MHz \_p14a0028**

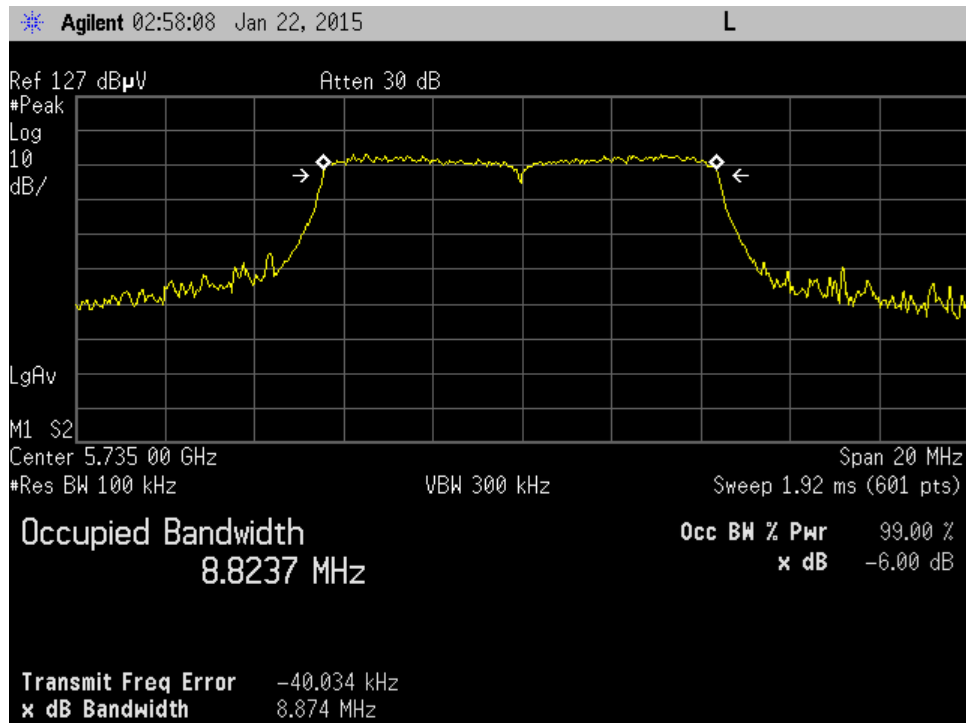


**OCC BW\_J3\_high ch\_bw=40 MHz \_p14a0028**

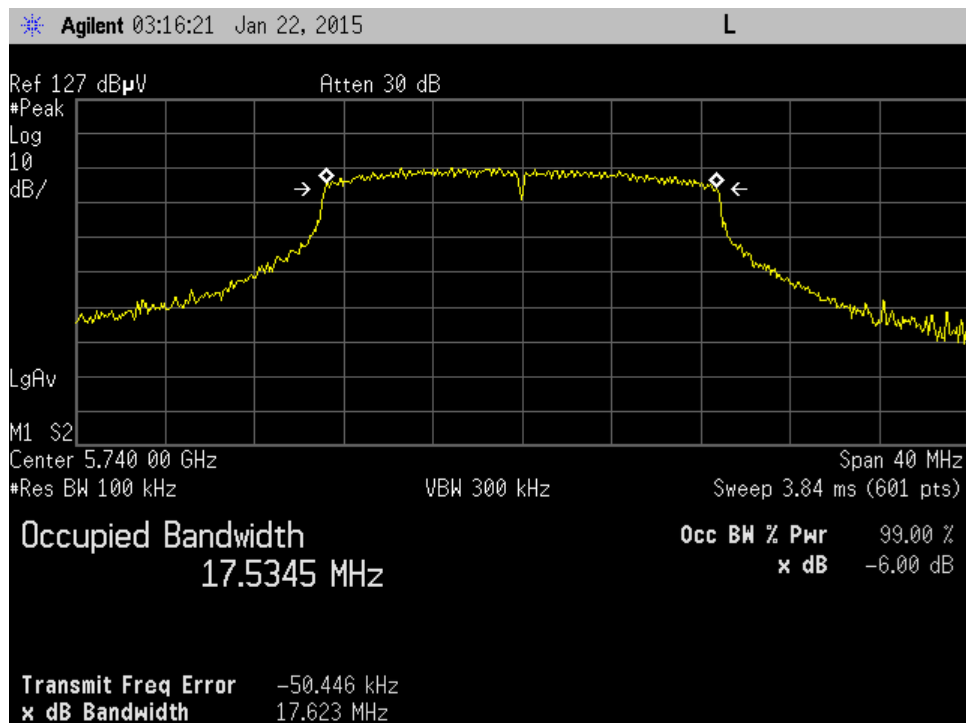




**OCC BW\_J3\_low ch\_bw=10 MHz \_p14a0028**

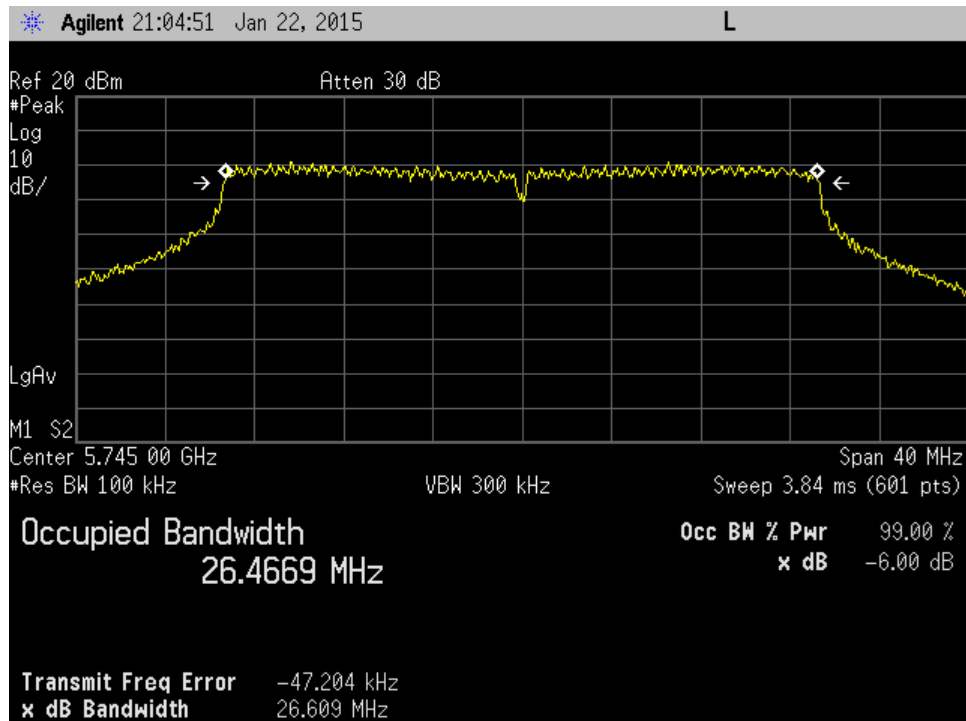


**OCC BW\_J3\_low ch\_bw=20 MHz \_p14a0028**

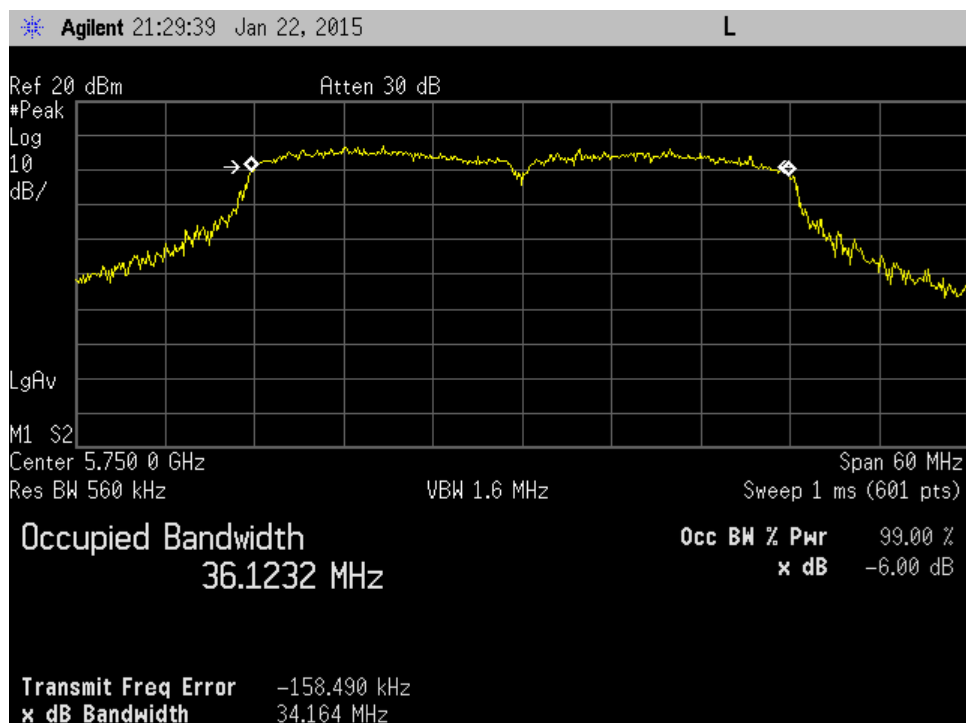




**OCC BW\_J3\_low ch\_bw=30 MHz \_p14a0028**

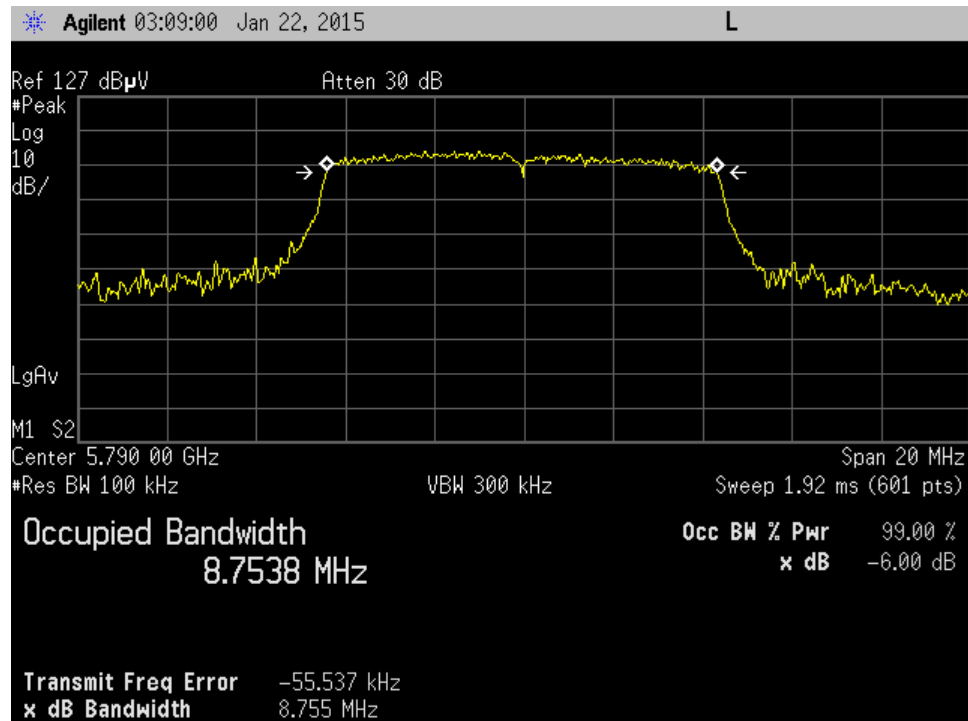


**OCC BW\_J3\_low ch\_bw=40 MHz \_p14a0028**

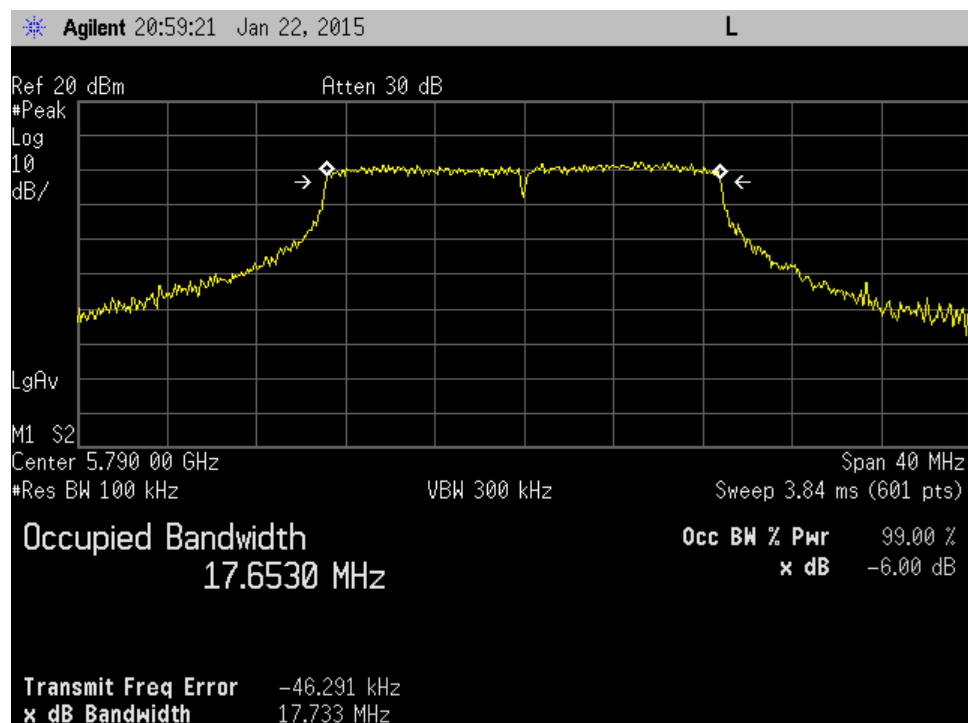




**OCC BW\_J3\_mid ch\_bw=10 MHz \_p14a0028**

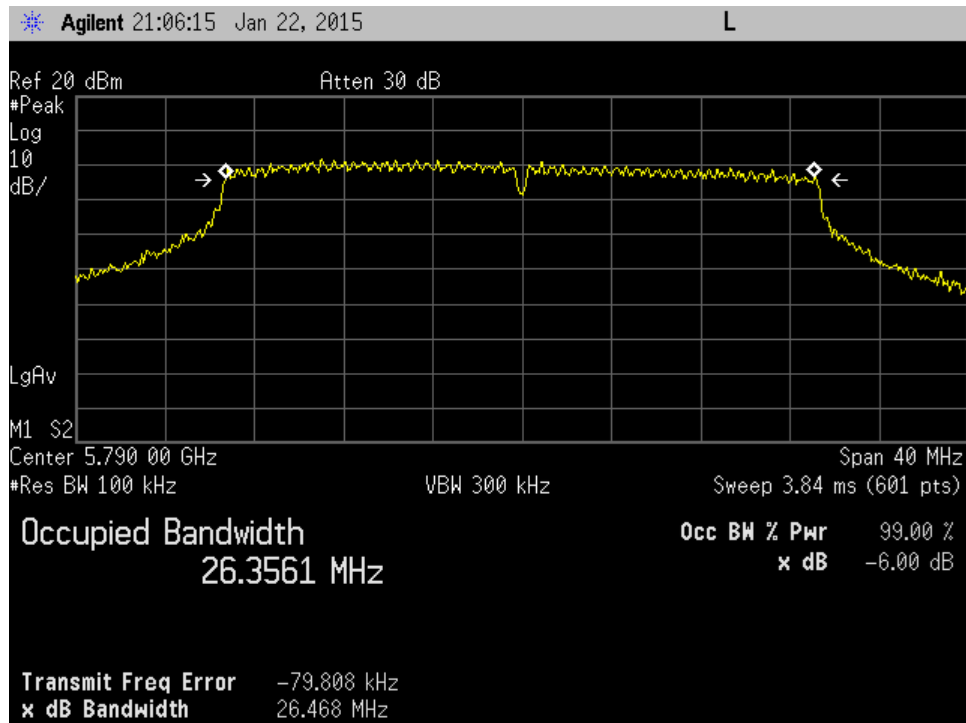


**OCC BW\_J3\_mid ch\_bw=20 MHz \_p14a0028**





**OCC BW\_J3\_mid ch\_bw=30 MHz \_p14a0028**



**OCC BW\_J3\_mid ch\_bw=40 MHz \_p14a0028**

