

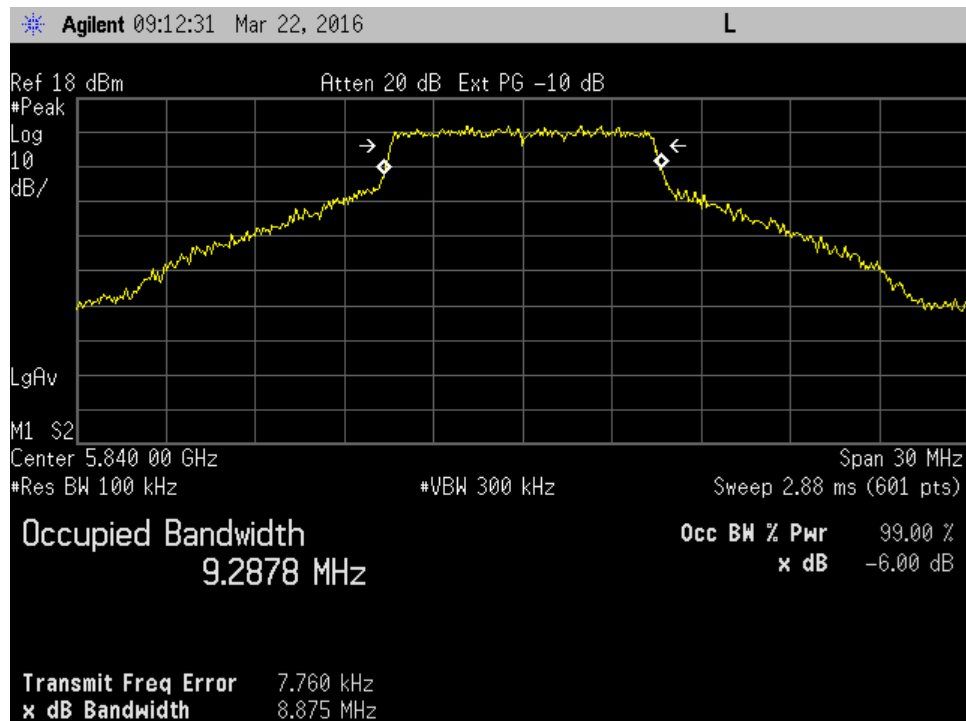


Annex C

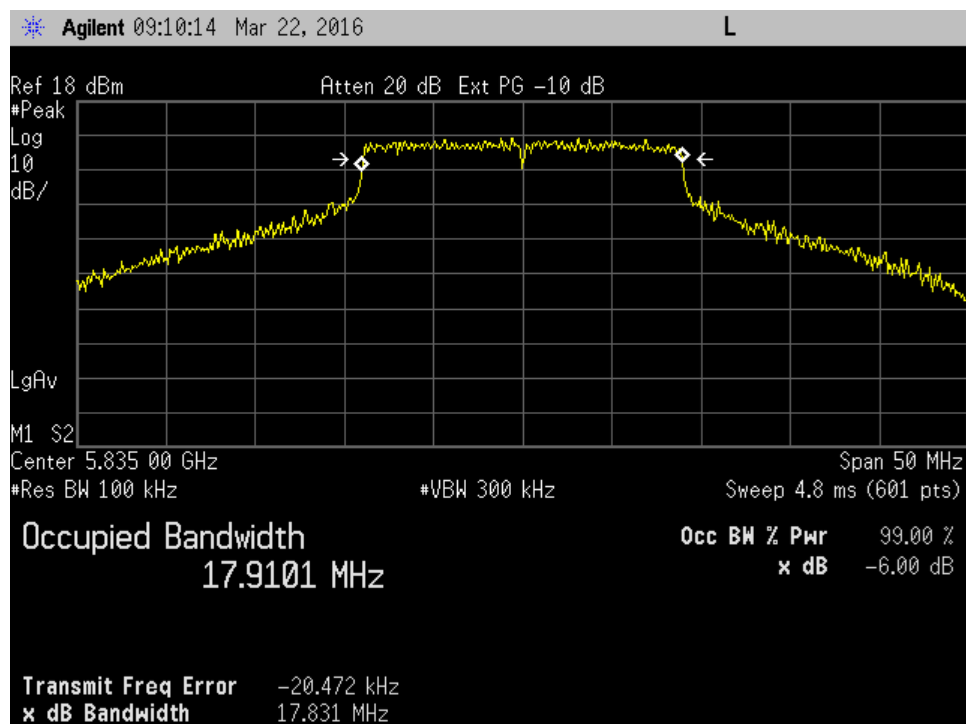
Occupied Bandwidth



high ch port 1 10MHz BW

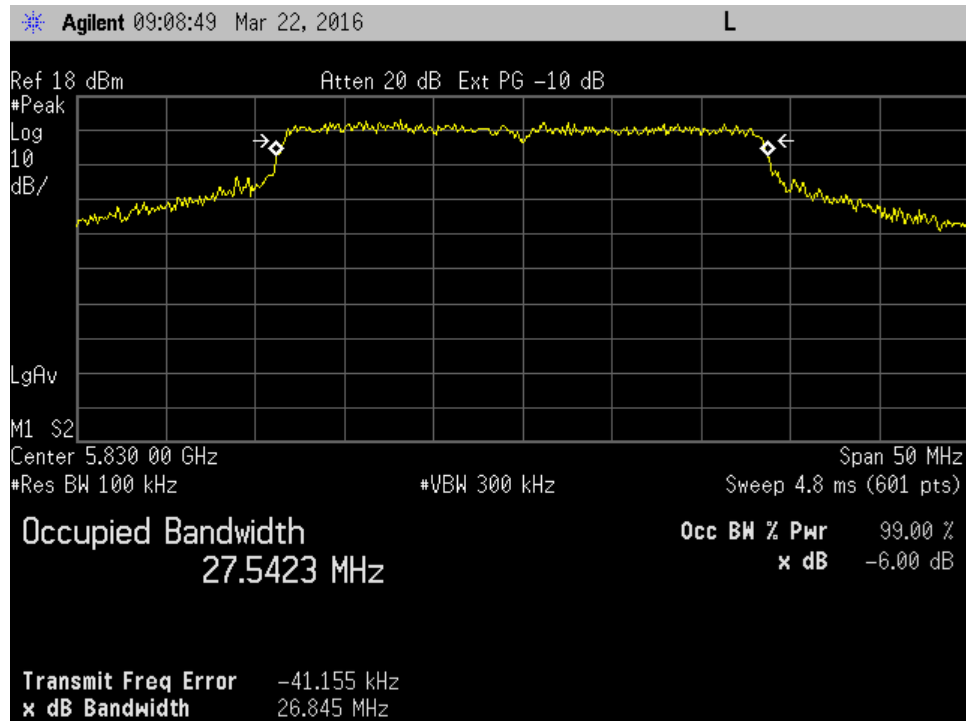


high ch port 1 20MHz BW

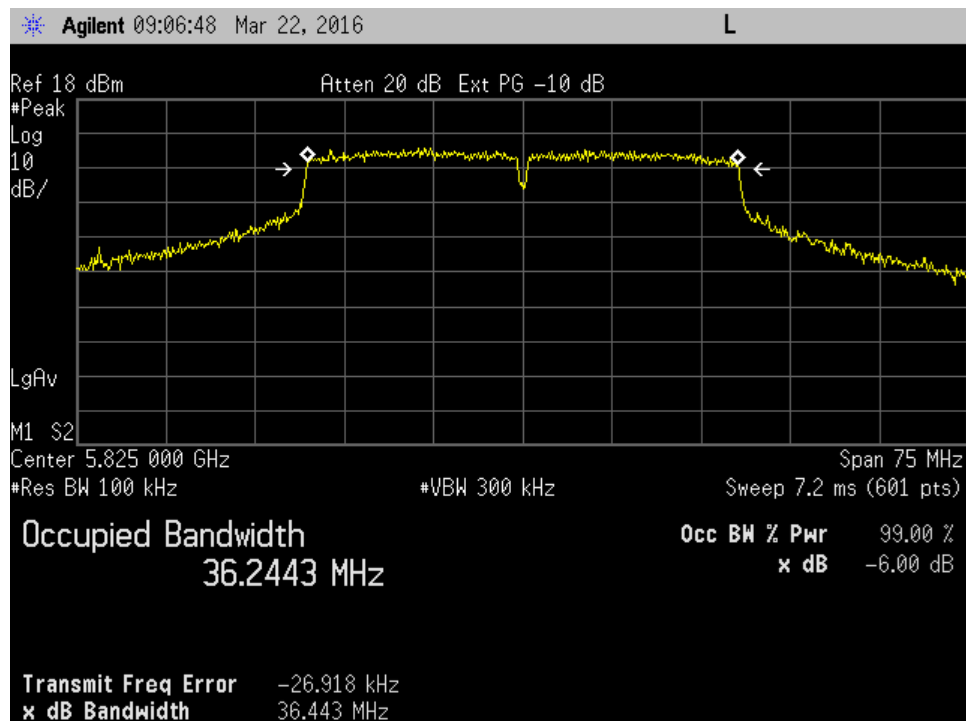




high ch port 1 30MHz BW

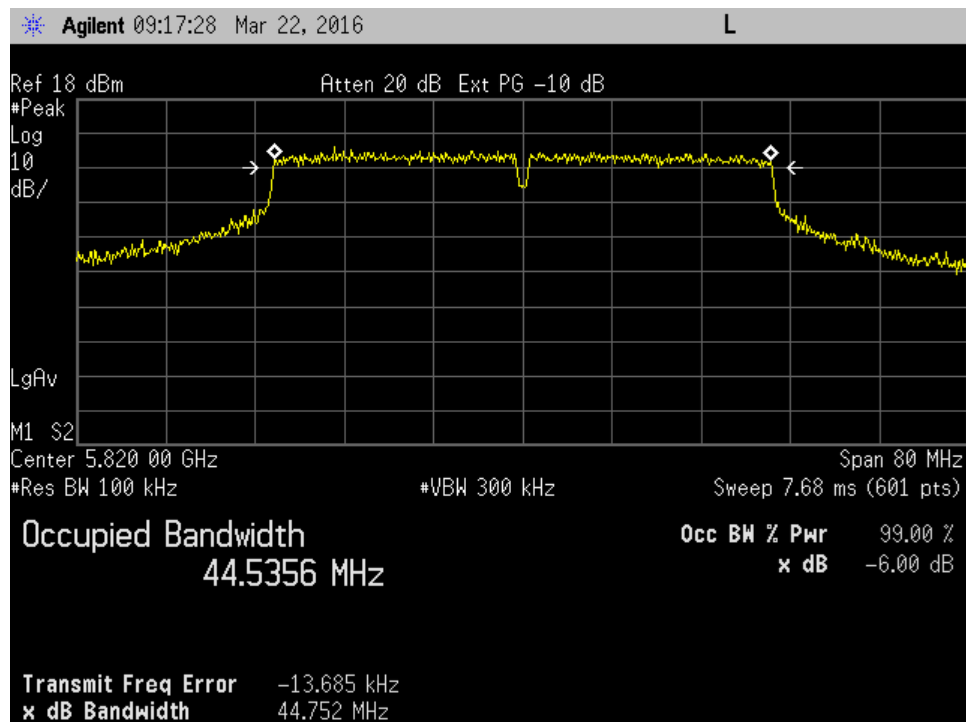


high ch port 1 40MHz BW

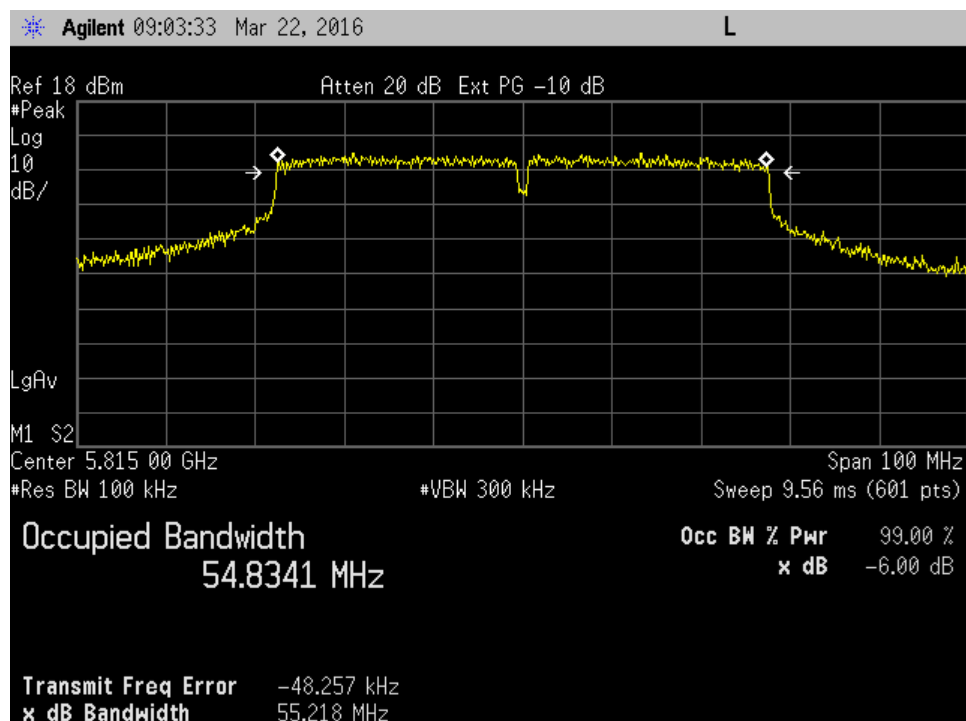




high ch port 1 50MHz BW

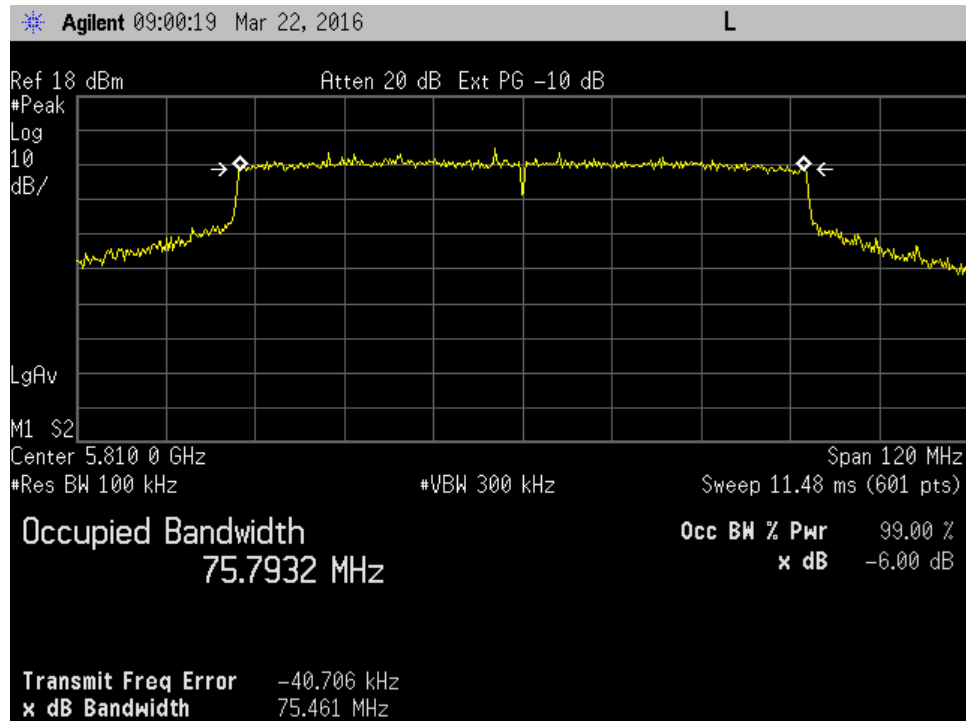


high ch port 1 60MHz BW

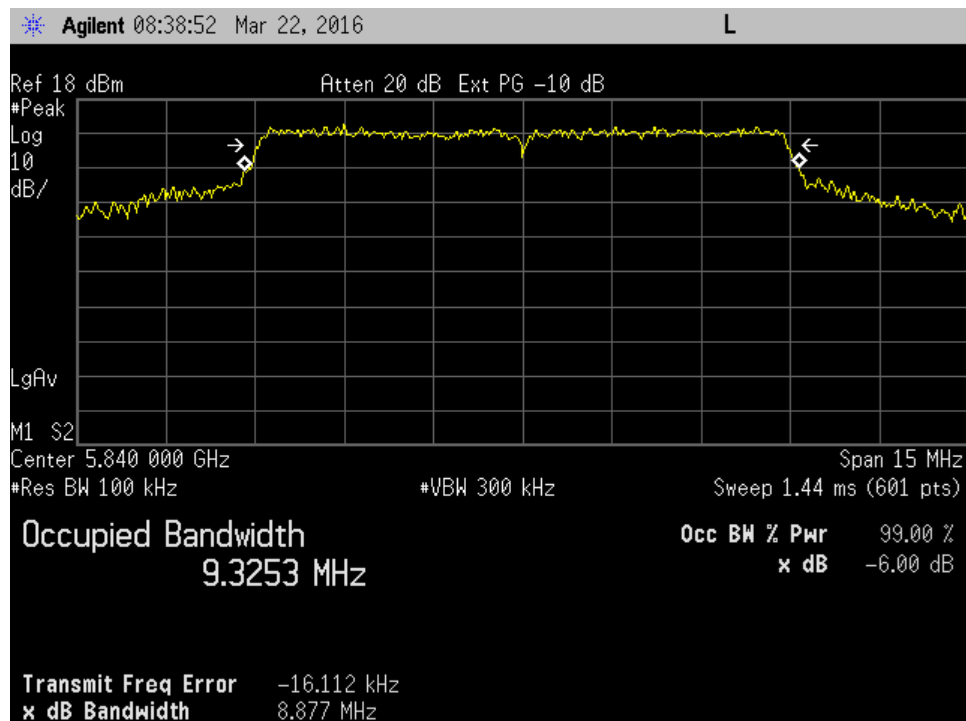




high ch port 1 80MHz BW

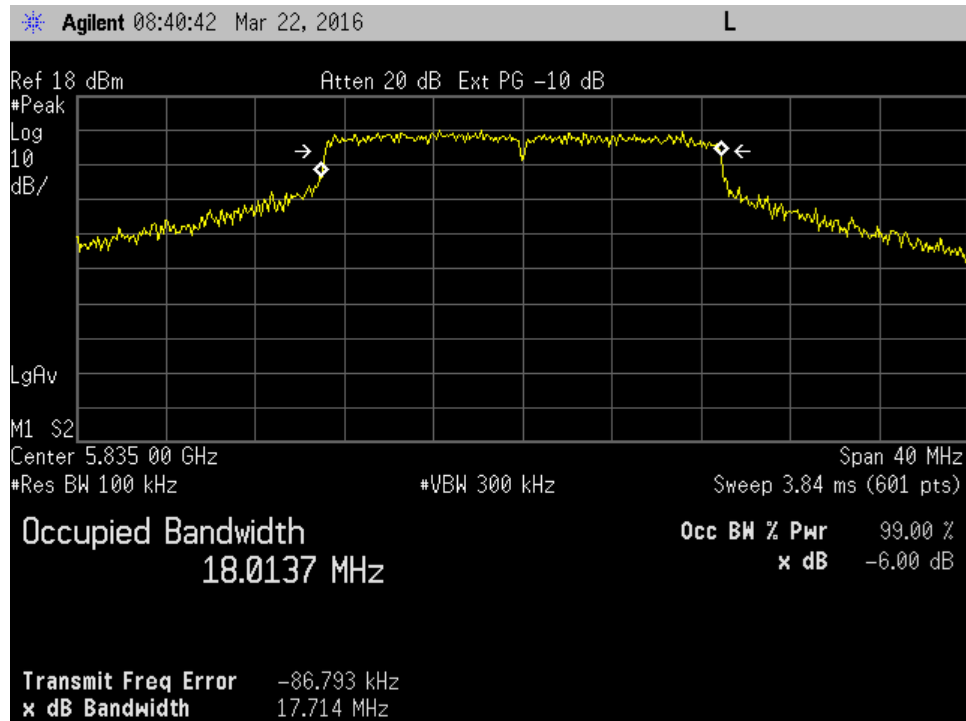


high ch port 2 10MHz BW

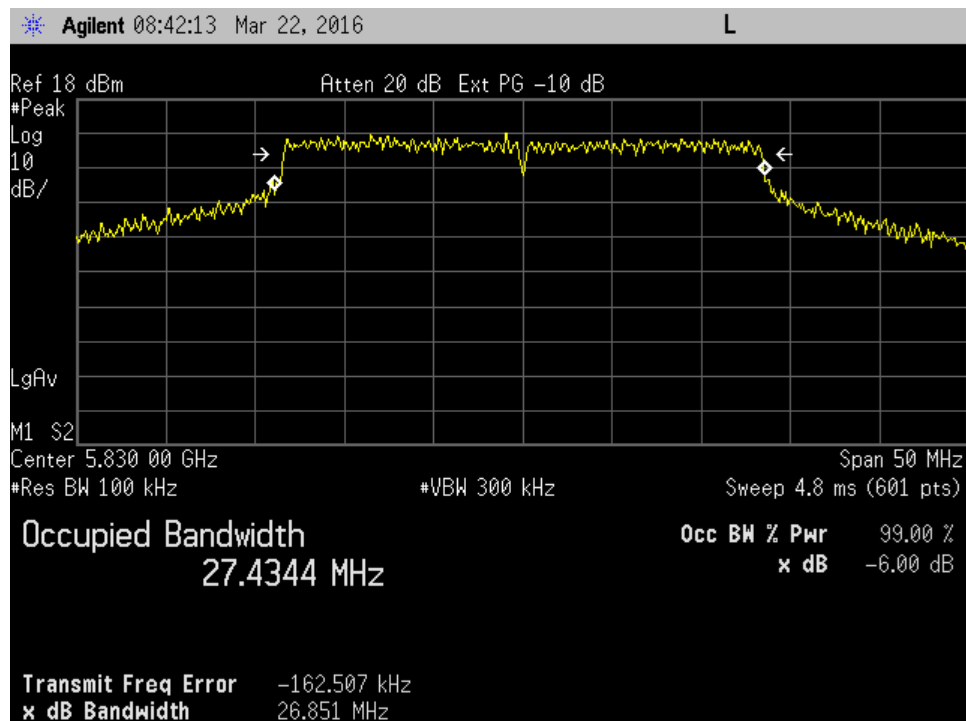


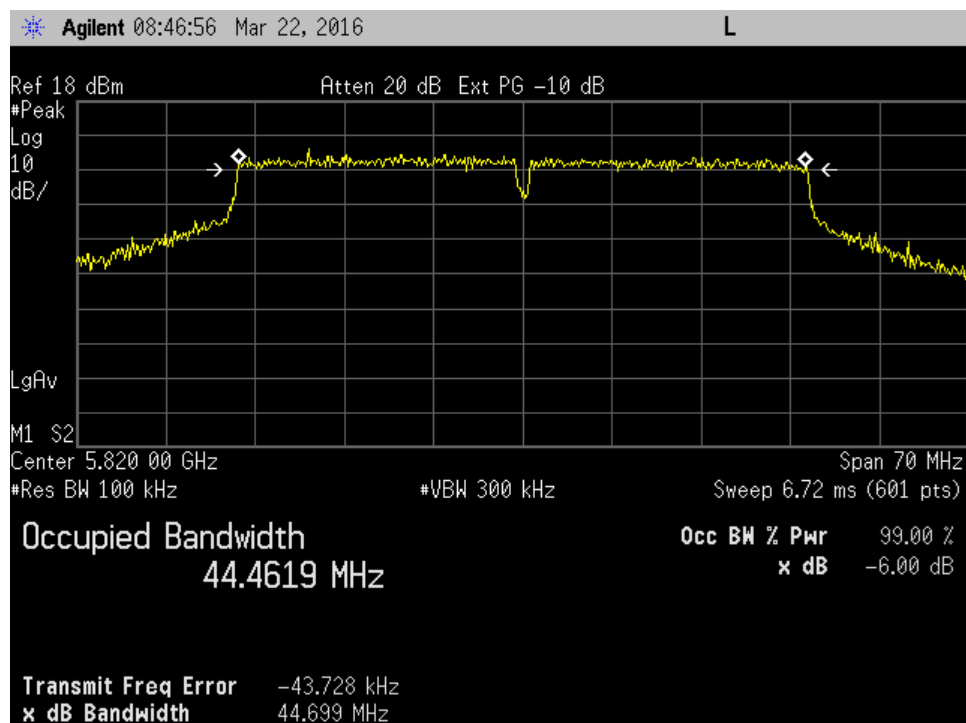
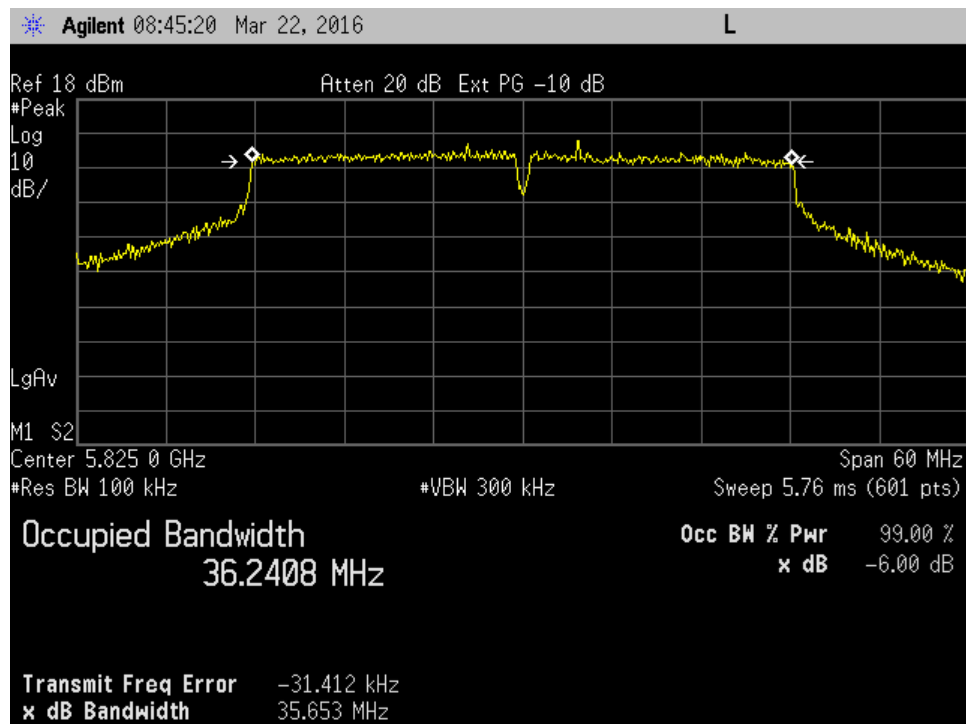


high ch port 2 20MHz BW



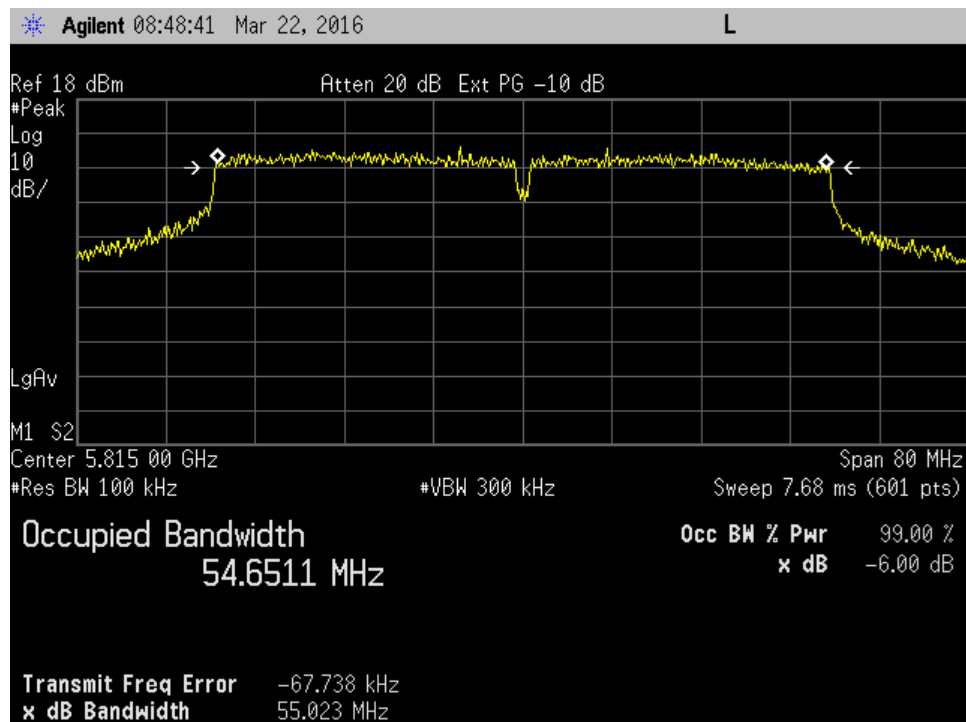
high ch port 2 30MHz BW



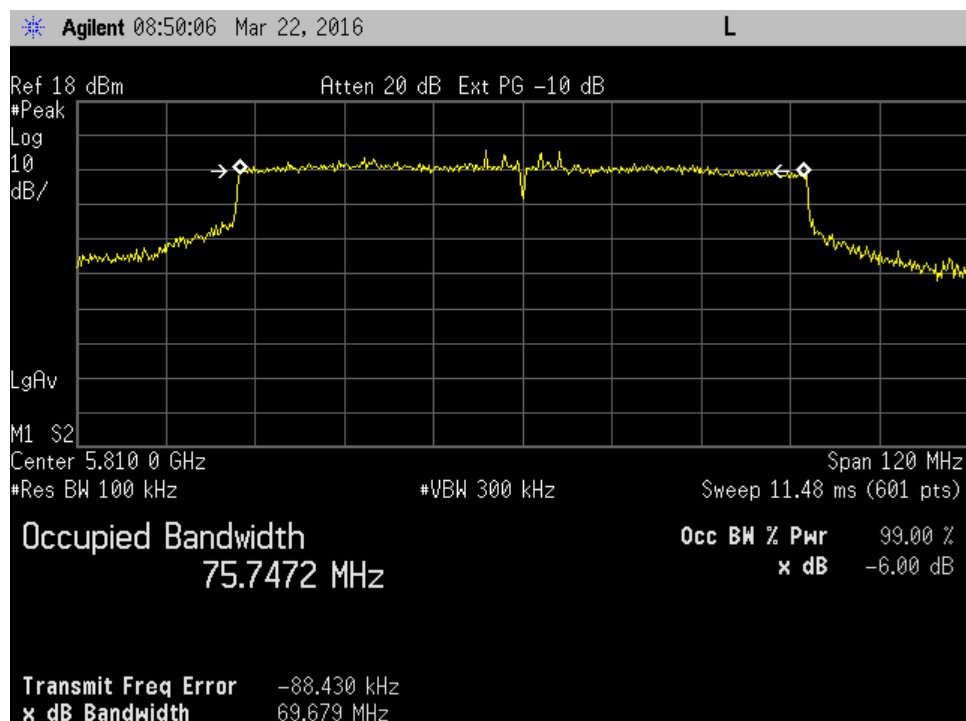




high ch port 2 60MHz BW

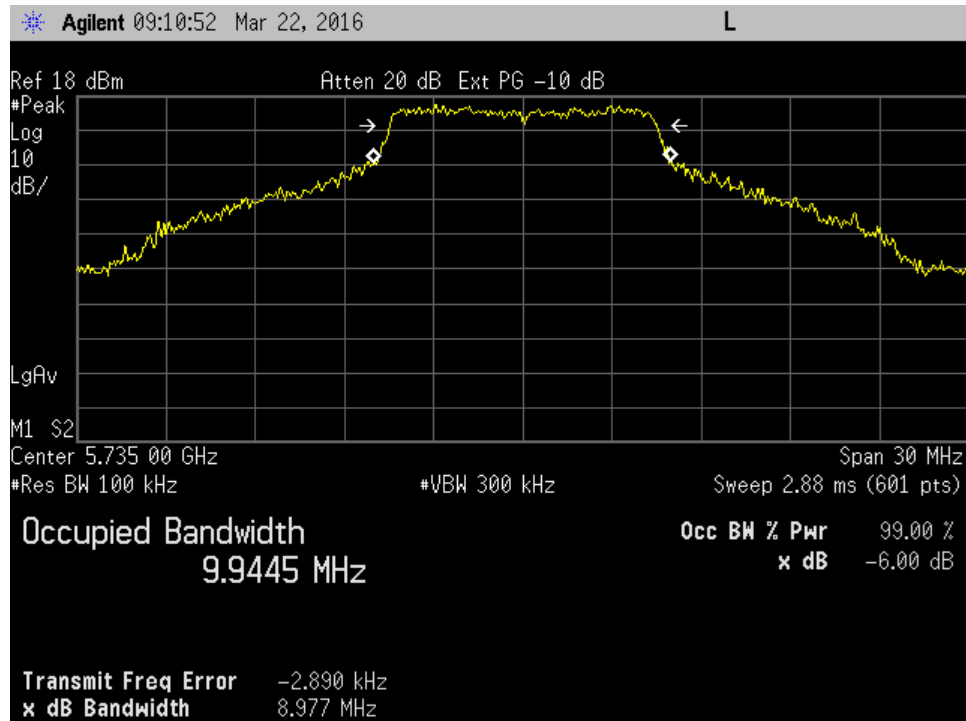


high ch port 2 80MHz BW

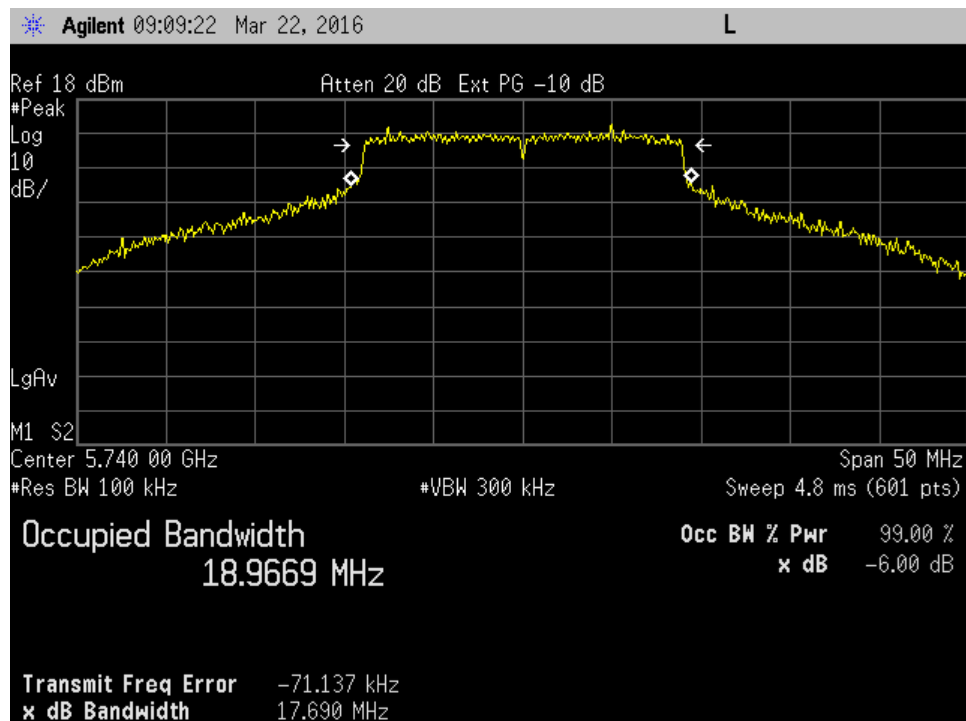




low ch port 1 10MHz BW

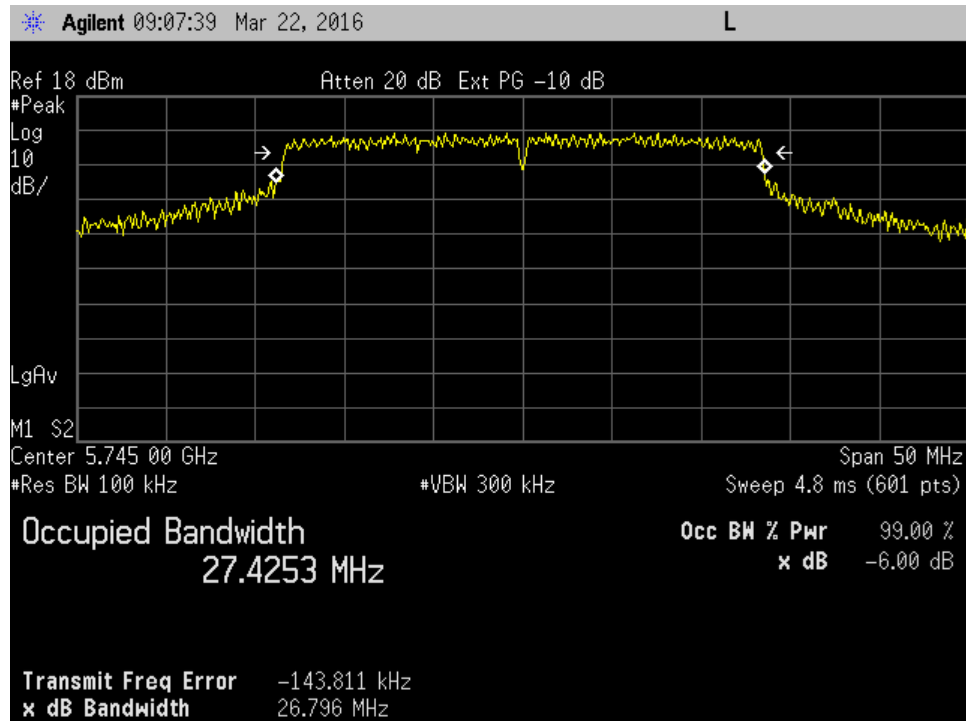


low ch port 1 20MHz BW

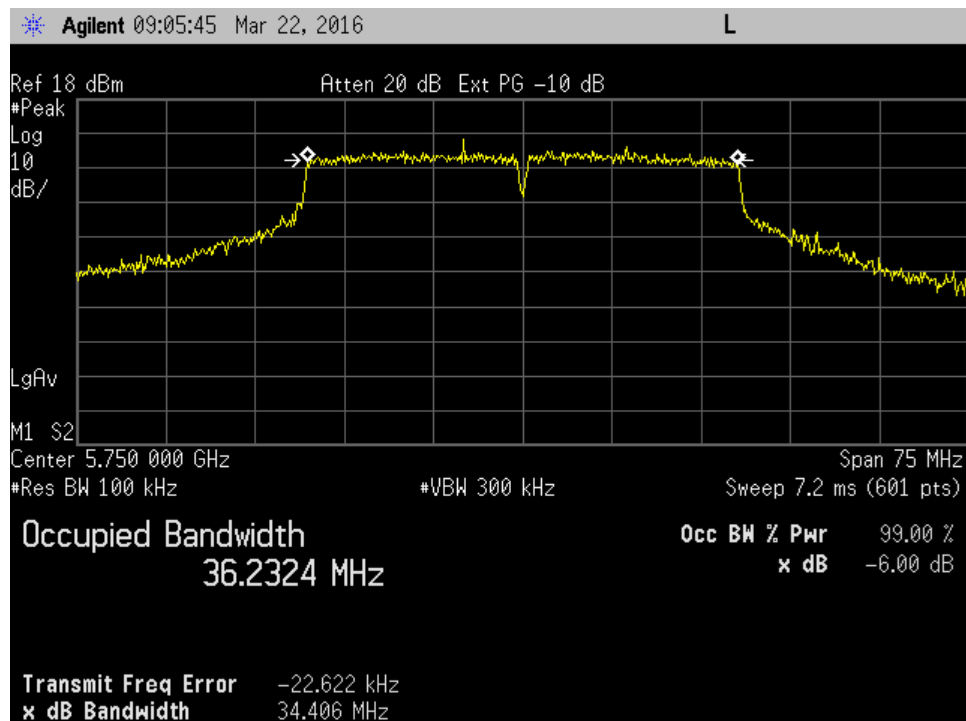




low ch port 1 30MHz BW

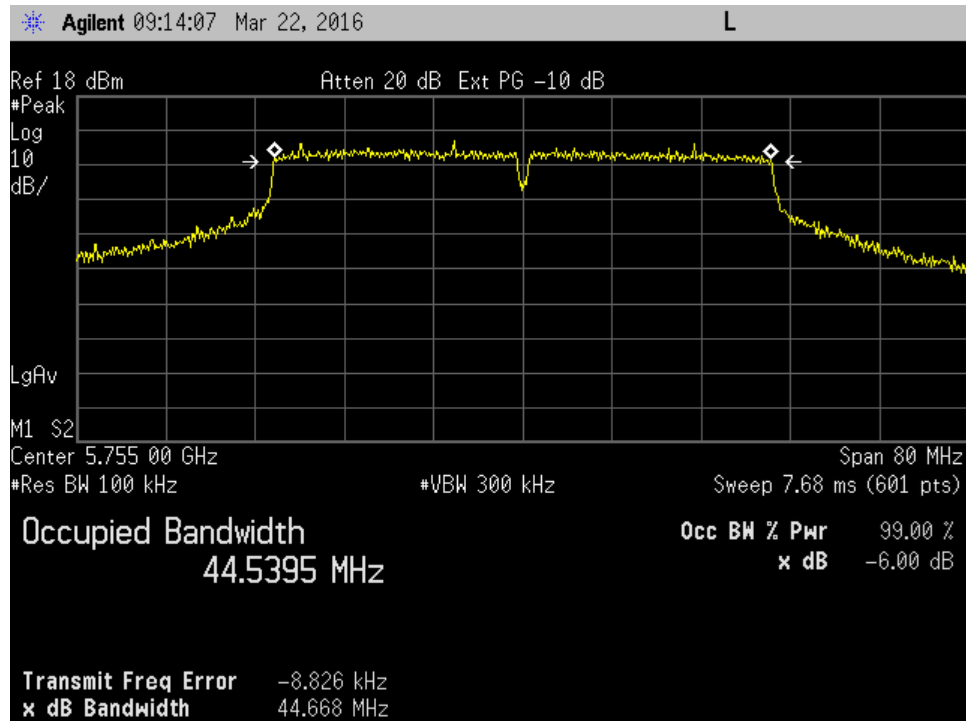


low ch port 1 40MHz BW

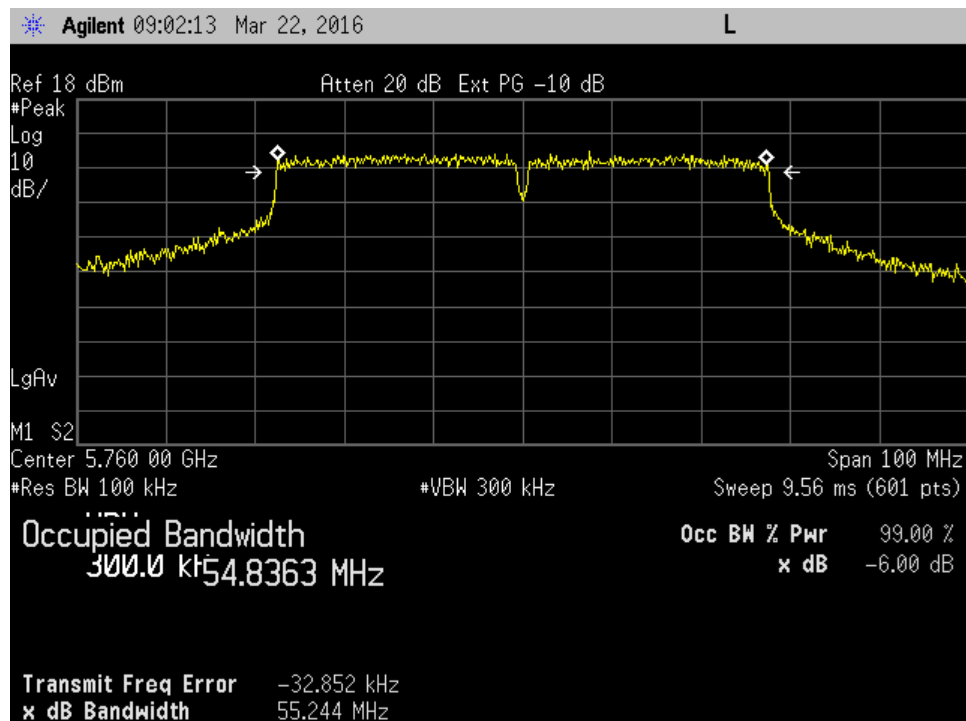




low ch port 1 50MHz BW

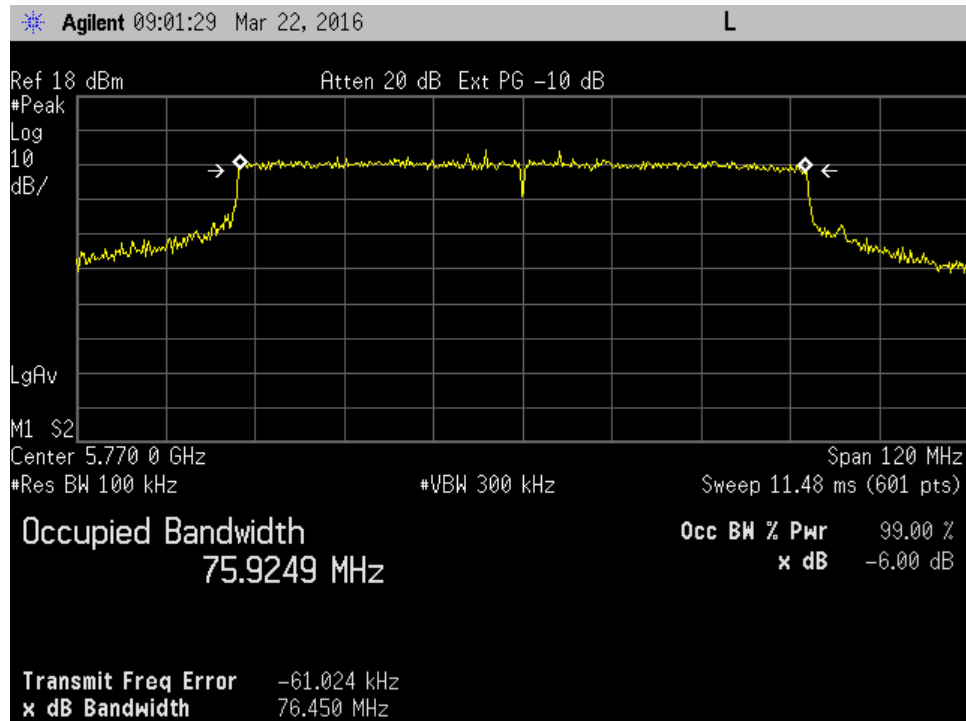


low ch port 1 60MHz BW

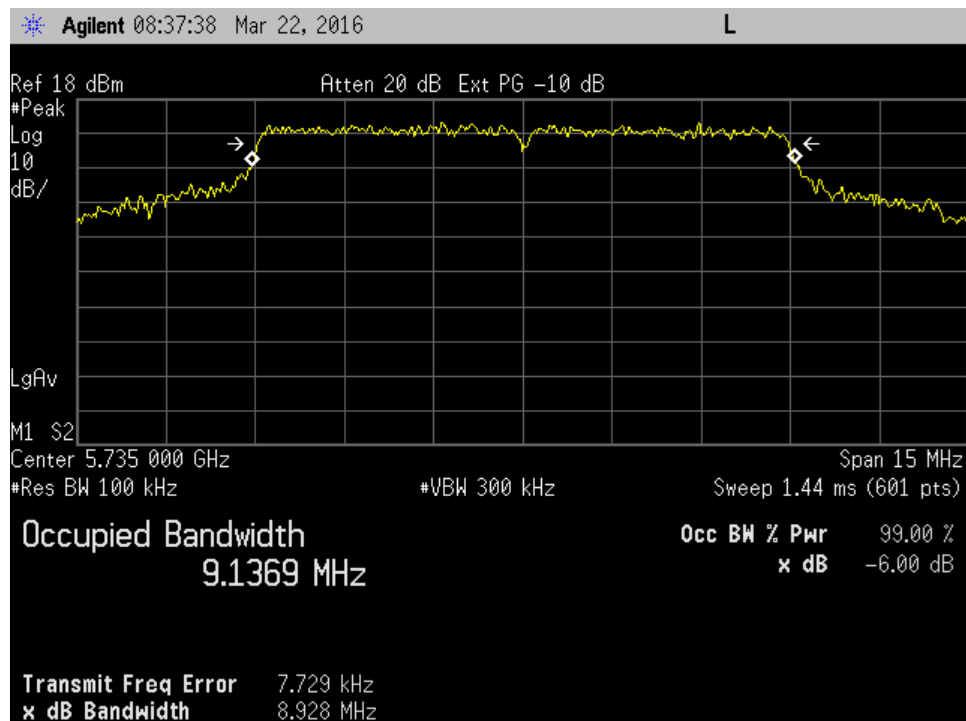




low ch port 1 80MHz BW

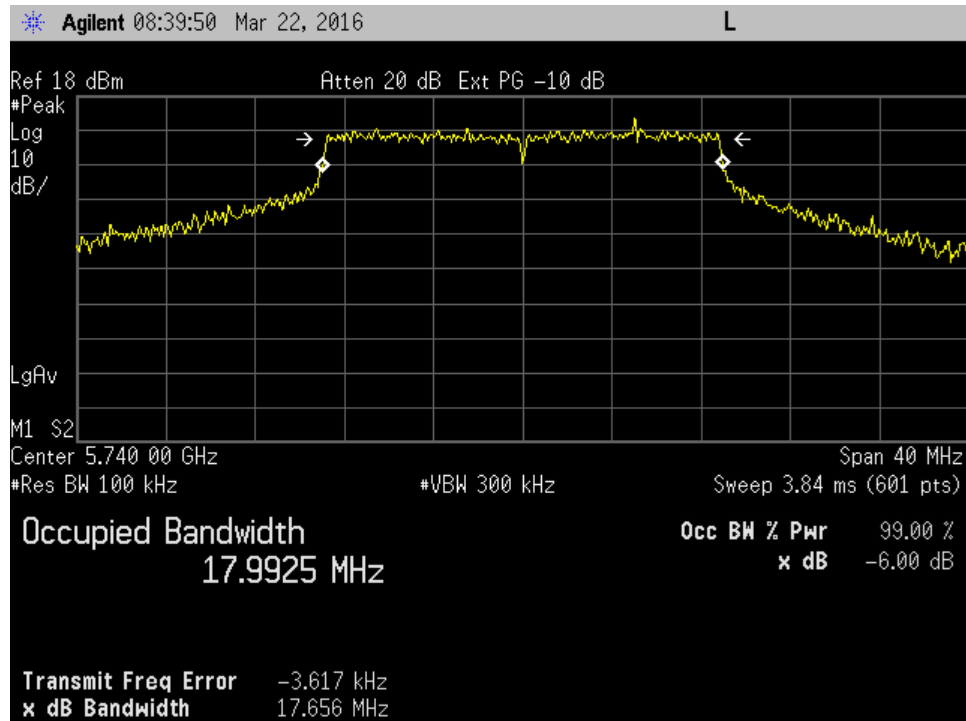


low ch port 2 10MHz BW

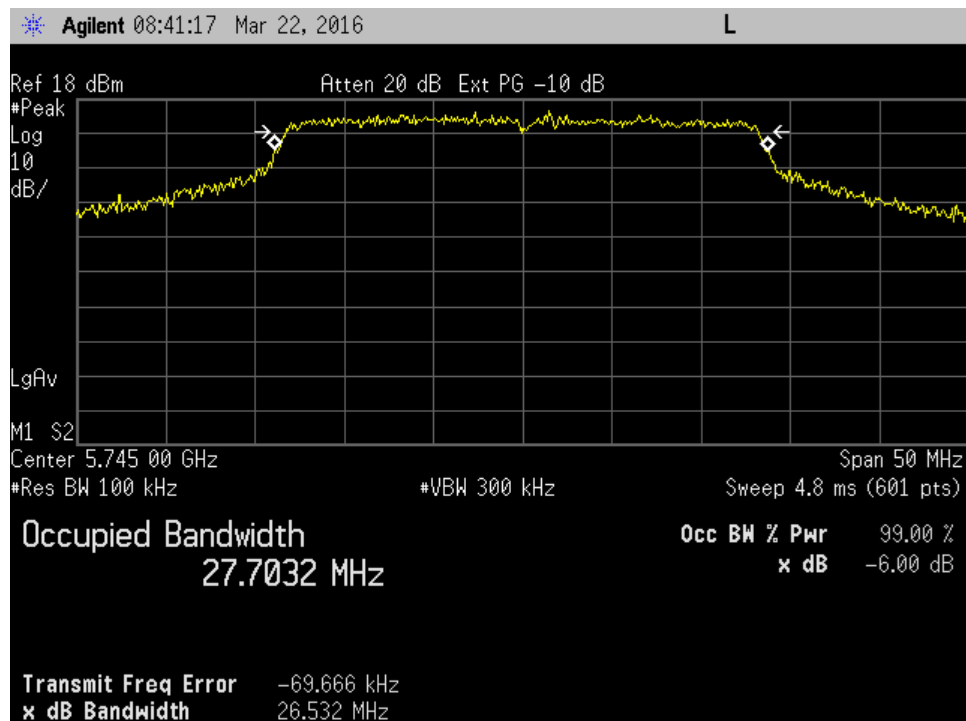




low ch port 2 20MHz BW

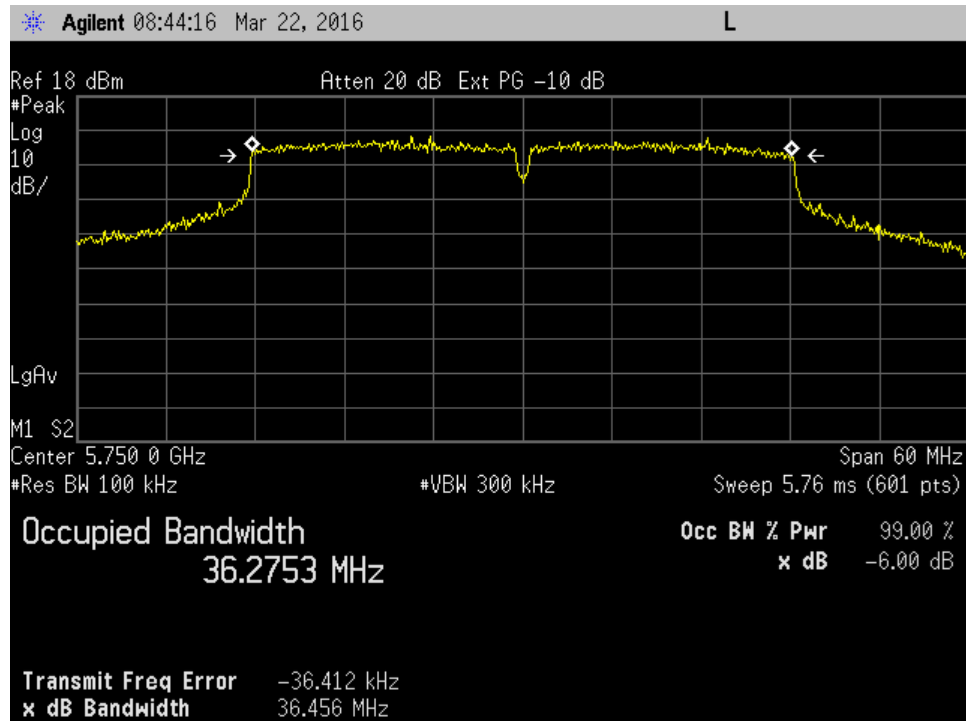


low ch port 2 30MHz BW

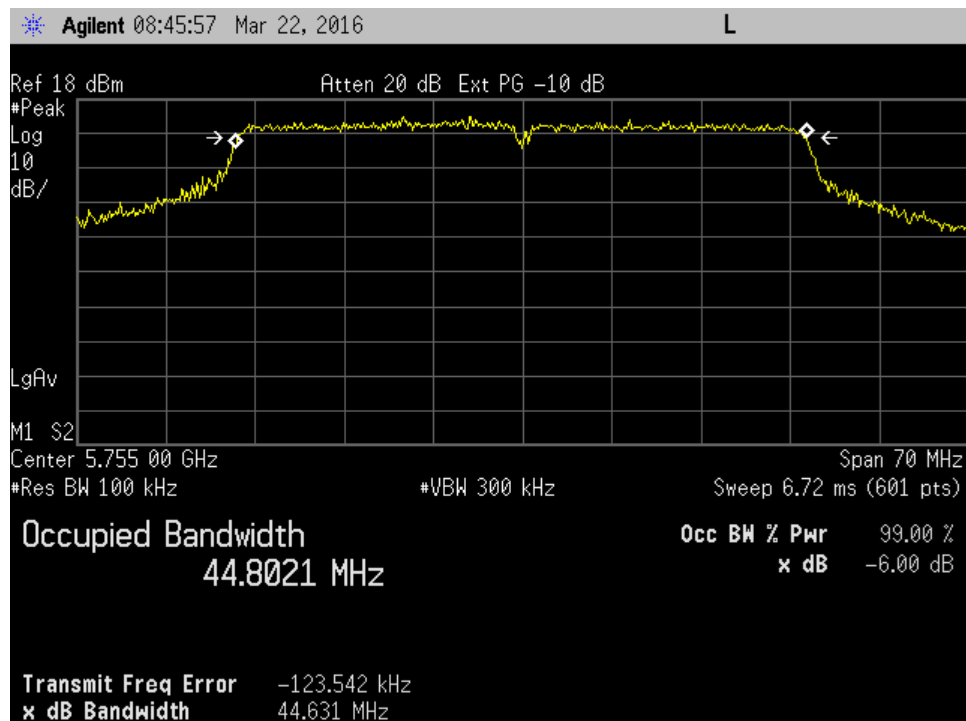




low ch port 2 40MHz BW

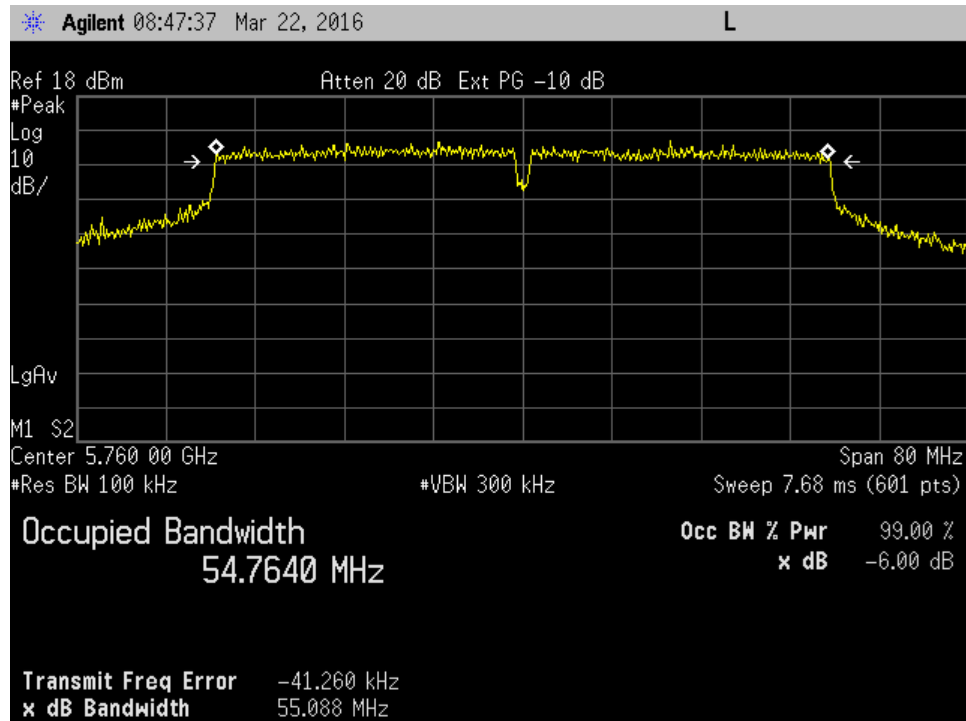


low ch port 2 50MHz BW

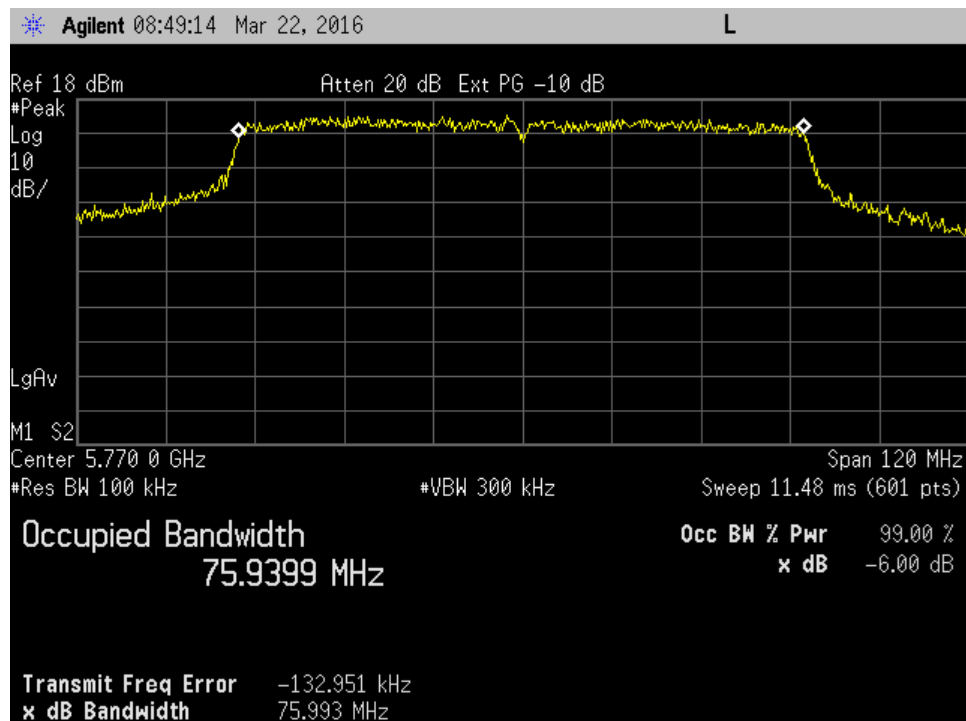




low ch port 2 60MHz BW

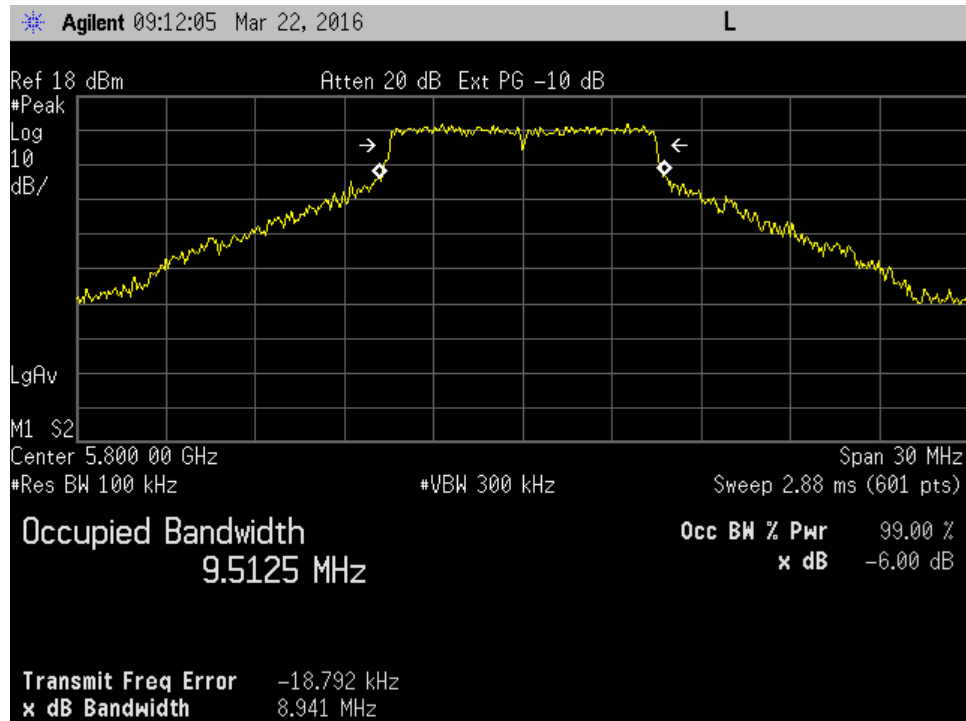


low ch port 2 80MHz BW

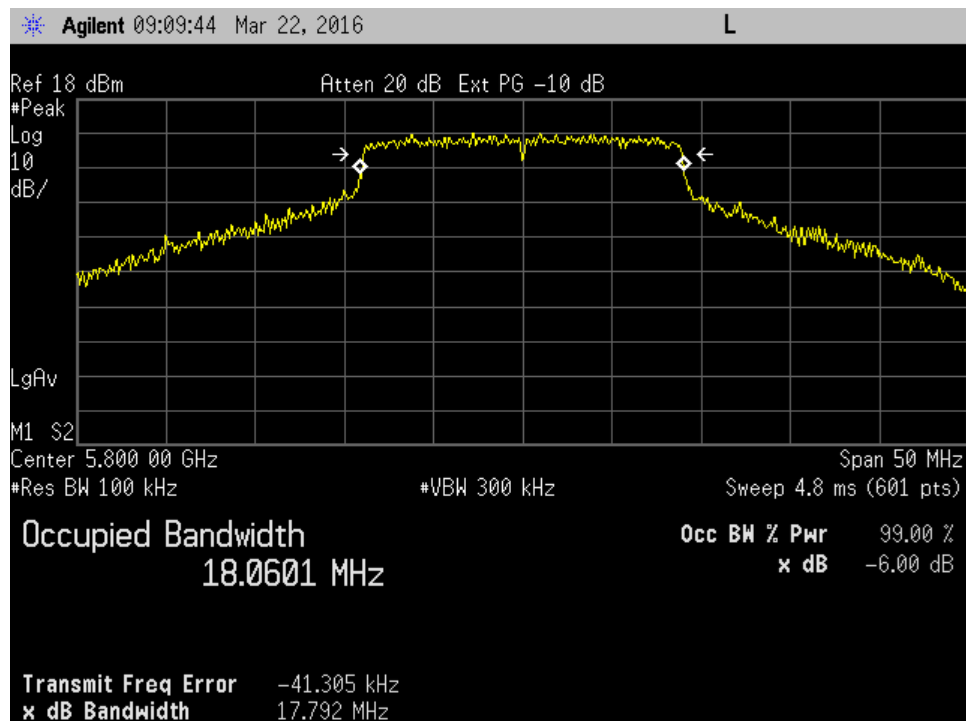




mid ch port 1 10MHz BW

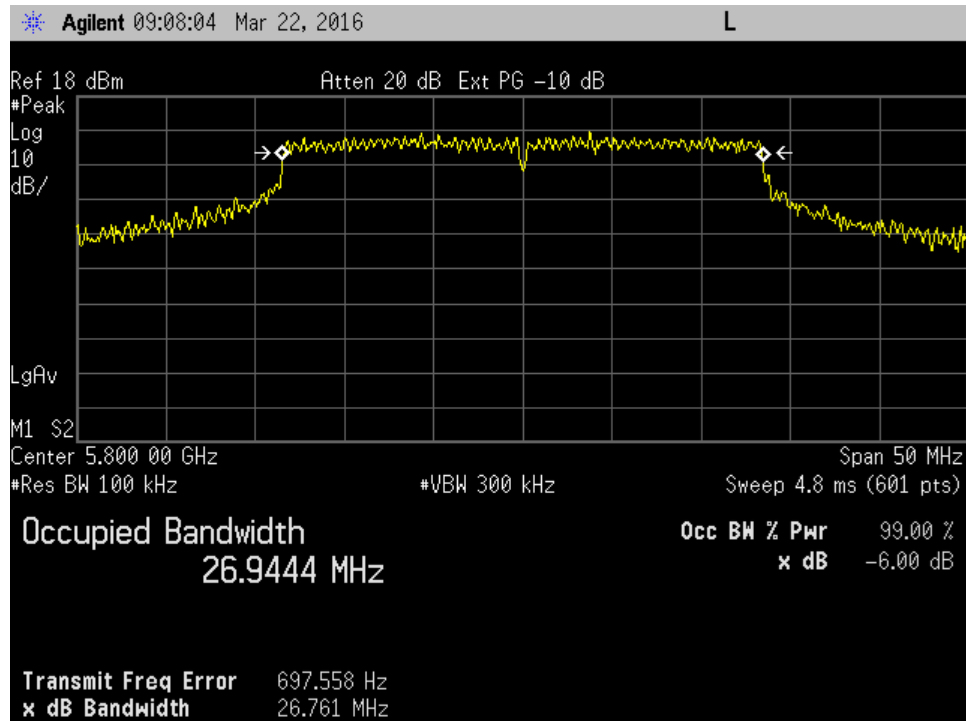


mid ch port 1 20MHz BW

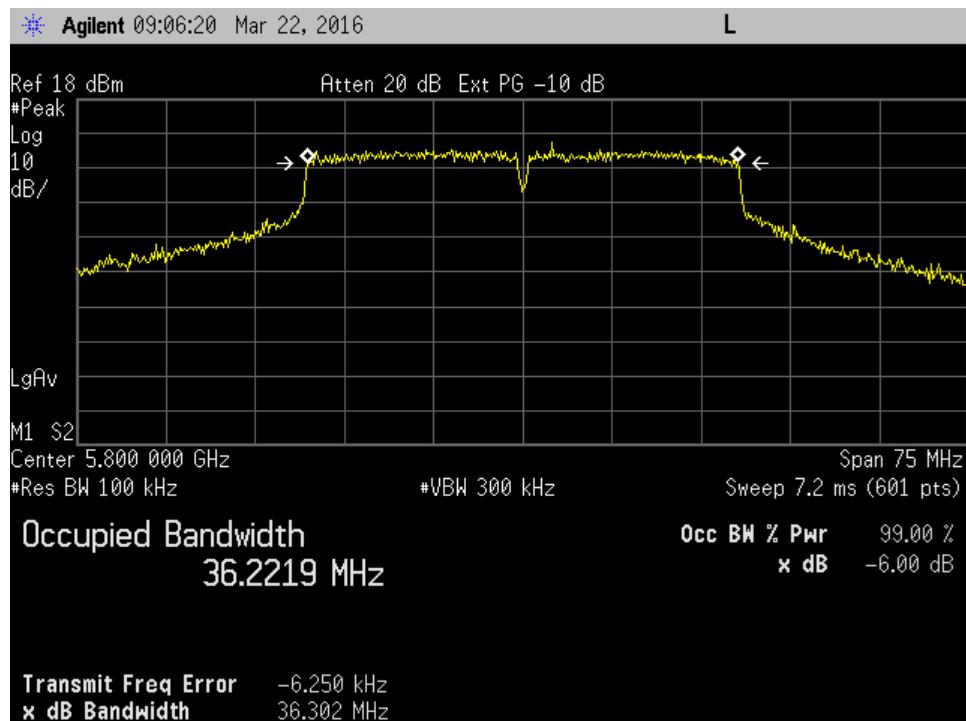




mid ch port 1 30MHz BW

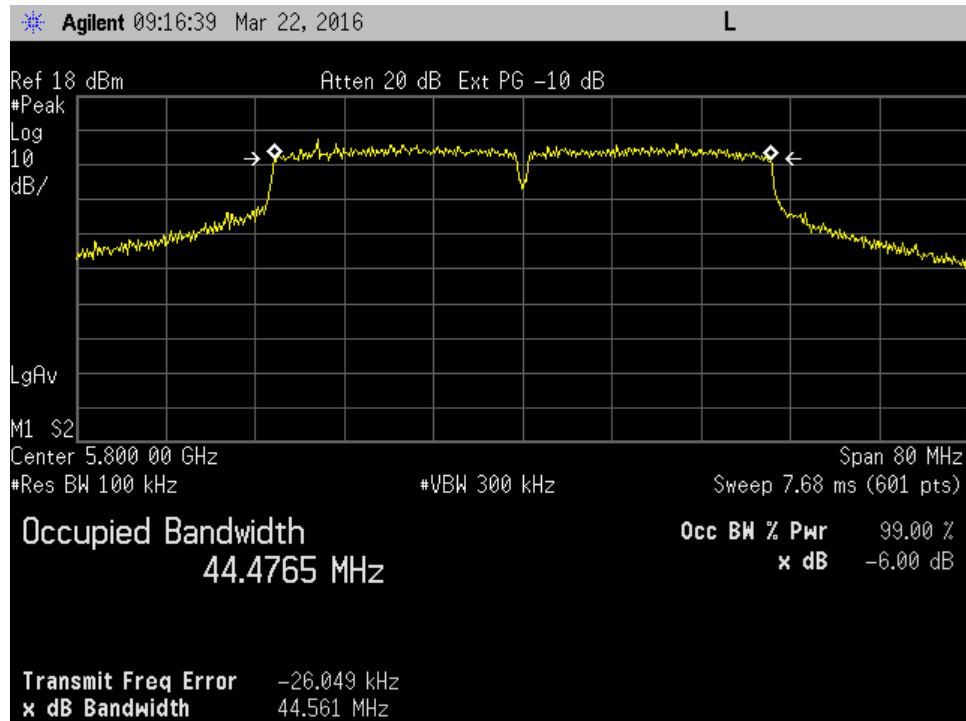


mid ch port 1 40MHz BW

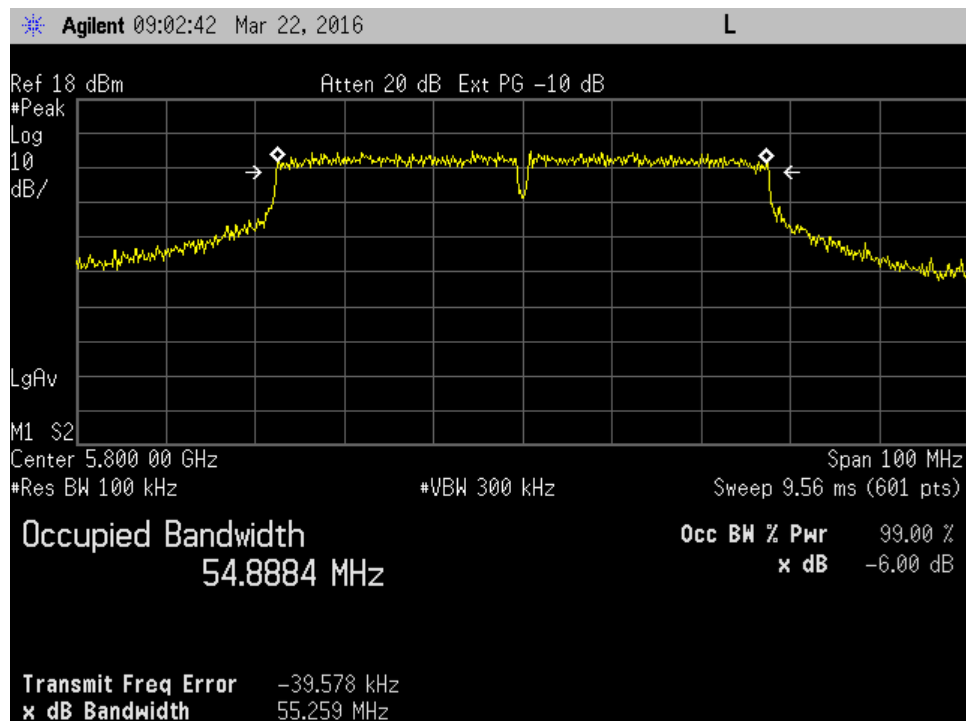




mid ch port 1 50MHz BW

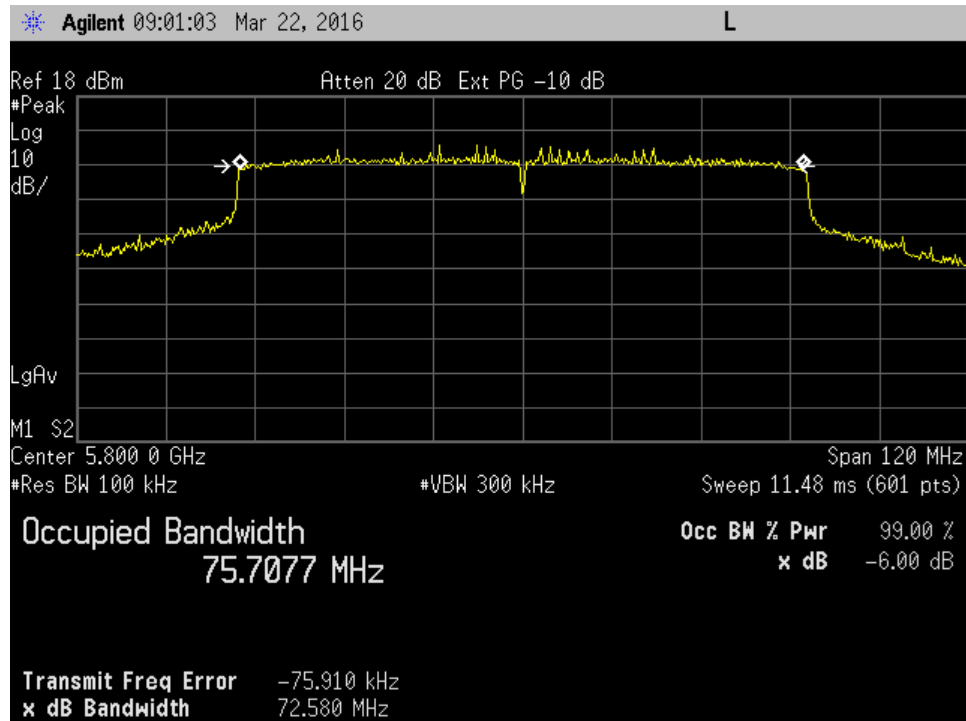


mid ch port 1 60MHz BW

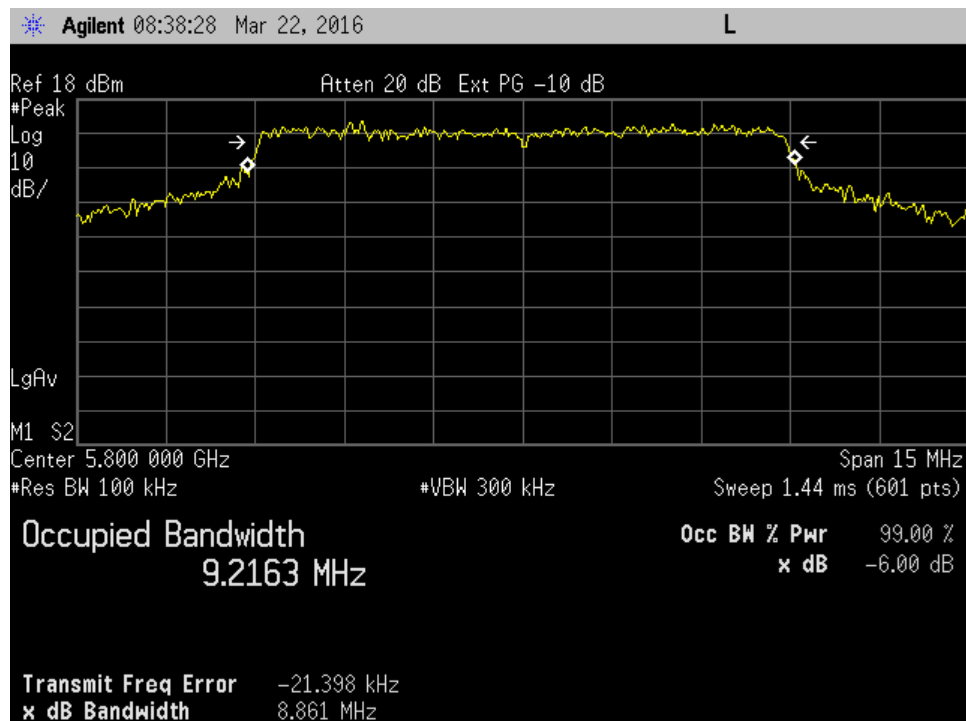




mid ch port 1 80MHz BW

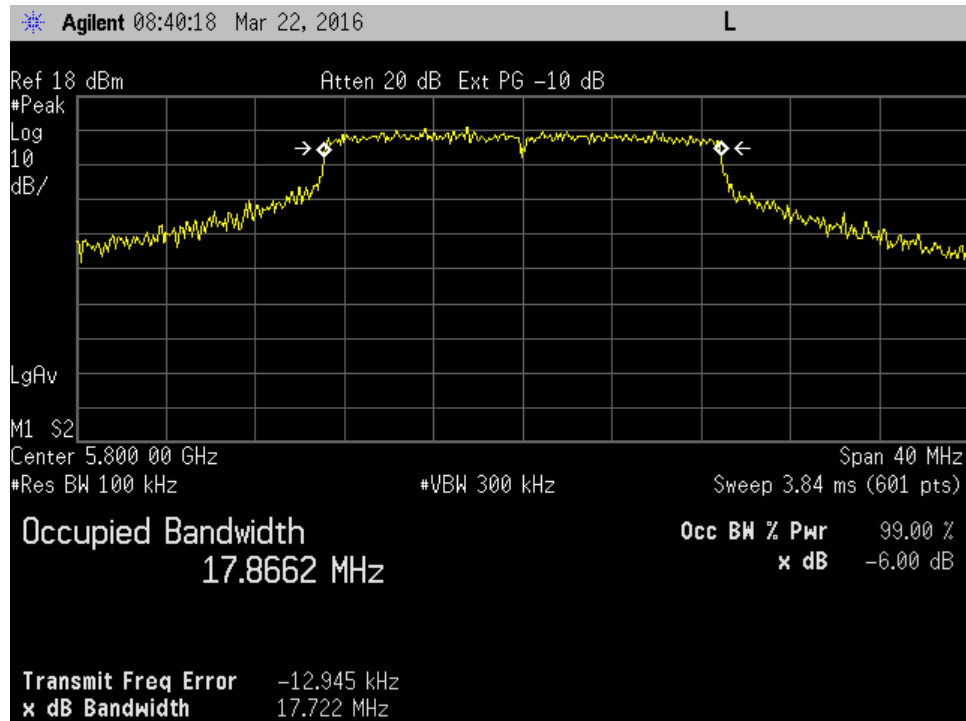


mid ch port 2 10MHz BW

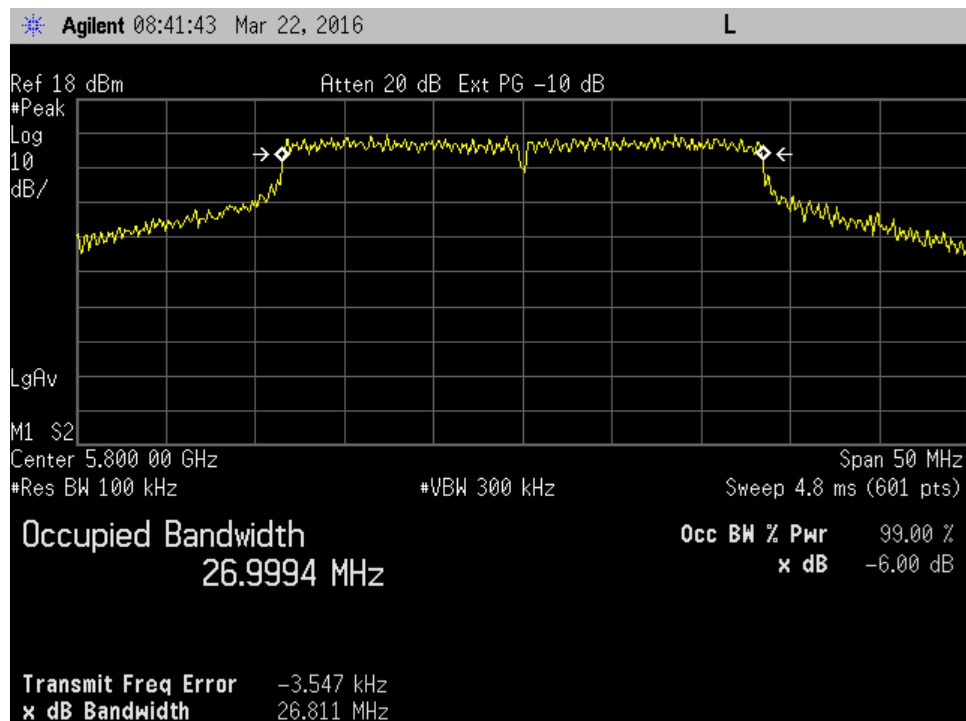




mid ch port 2 20MHz BW

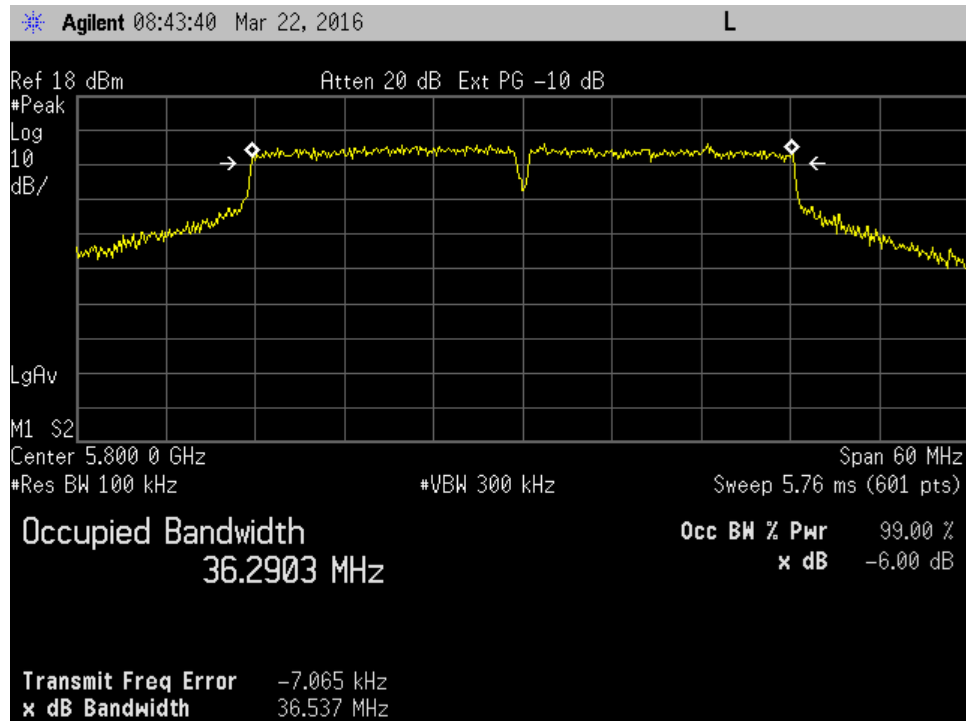


mid ch port 2 30MHz BW

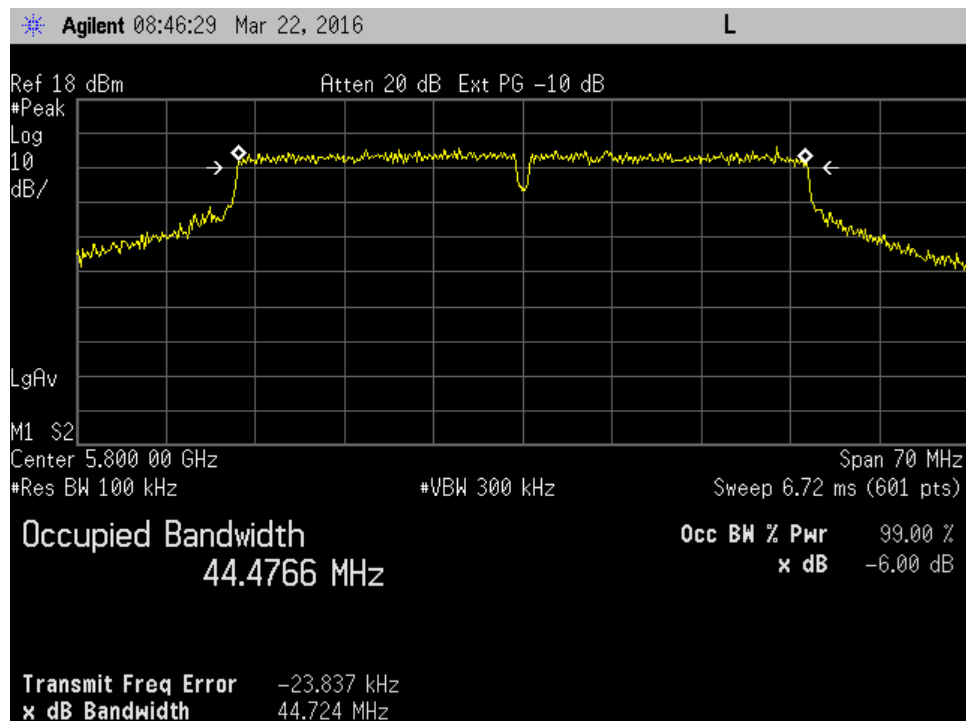




mid ch port 2 40MHz BW

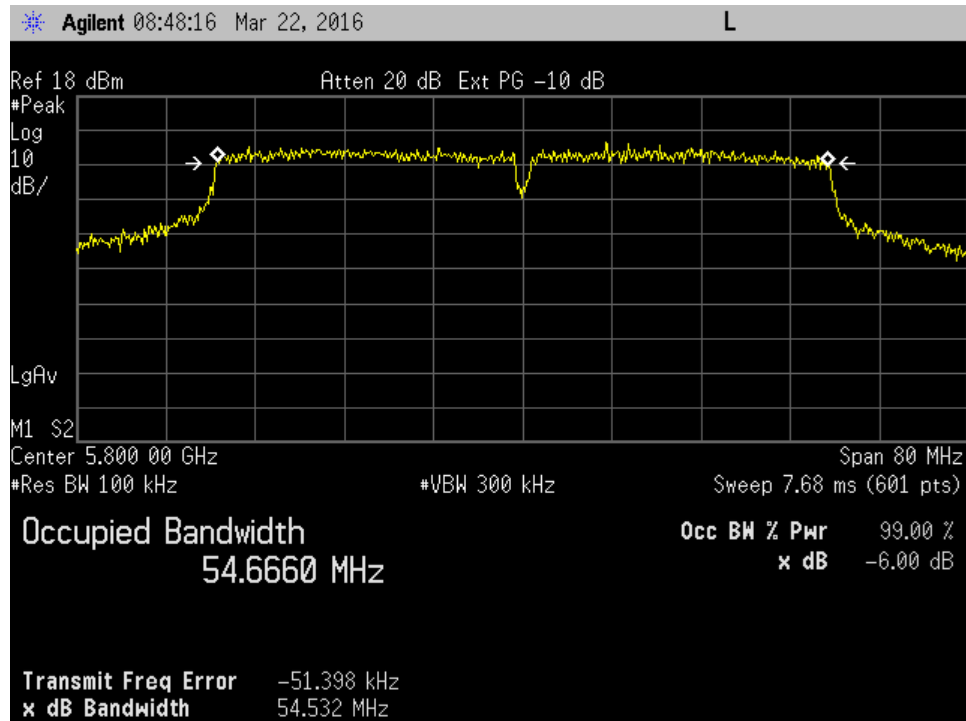


mid ch port 2 50MHz BW





mid ch port 2 60MHz BW



mid ch port 2 80MHz BW

