Circuit Description and Theory of Operation

NOTE: Refer to Block Diagram (Fig 4.1) and circuit schematics during the following description.

The DVX-750 VHF radio module operates as an airborne VHF COMM transceiver allowing a flight crew to aurally communicate with Air Traffic Control (ATC), other ground stations, or different aircraft in the VHF aeronautical band. It also operates as an airborne ILS/VOR receiver for radio aided navigation and guidance. The DVX-750 must be hosted by a PFD (Primary Flight Display) chassis, which provides conditioned DC power and digital interface to control radio functions.

The DVX-750 consists of two internal printed circuit boards, the “RF Board” (Part# 310-00116-00x) and the “Digital Board” (Part# 310-00115-00x). The concept is to for analog signal processing to occur on the RF board and digital processing to be performed on the Digital Board.

The choice was made to do the analog-to-digital conversions on the Digital board with carefully matched analog differential signals interfacing between the two boards thru a 50-mil pitch stacking connector. The transmitted signal is generated digitally and converted to analog on the Digital board and sent to the RF board, while the received signals, which represent the entire operational radio band for each receiver, are fed into the Digital board as differential analog signals and immediately converted to digital format to be channelized and demodulated by the digital downconverter and signal processor. While there can only be one transmitted signal at a time, there can be as many as eight receivers operating simultaneously. Note that nothing changes on the RF board when a receiver frequency is changed, since the entire radio band is fed into the Digital board. The receivers are identified as:

Nav Rcvr – Tuned to condition and pass only the 108Mhz to 118Mhz Localizer and VOR Navigation bands such that the digitizer on the Digital board can undersample the RF signal without Nyquist alias signals appearing from out-of-band interference. The analog circuitry on the RF board provides the necessary filtering of signals that would appear in the Nyquist bands, and it applies the gain needed to optimize sensitivity based on signal strength of the in-band signals..

Glideslope Rcvr – Tuned to pass the 326 to 335 Mhz Glideslope signal band, it also provides sufficient filtering to allow the digitizer to undersample the received RF without causing Nyquist alias responses from out-of-band interference.

Marker Beacon Rcvr – Very tightly tuned to pass only a single channel at 75Mhz, this receiver includes a custom crystal filter and also allows undersampling of the RF signal.

Comm Rcvr – Tuned to pass only the 118 to 137Mhz VHF aeronautical band, this receiver interfaces to a T/R switch, allowing it to share the same antenna with the 16W

Comm transmitter. It also provides anti-aliasing filtering and optimizes gain for sensitivity without allowing signals to overload the A/D converters doing the

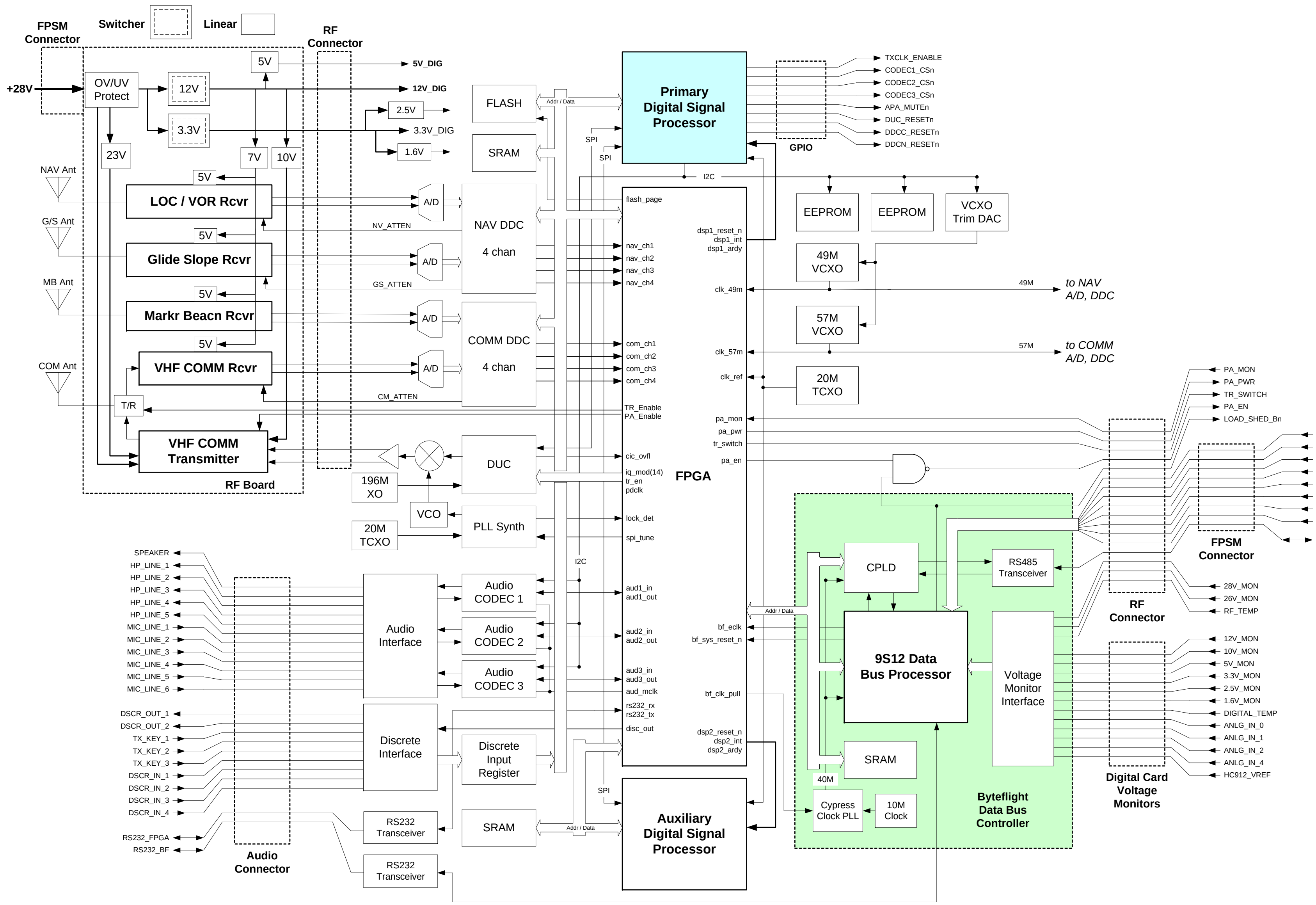

Figure 4.1 – VHF Nav/Com Block Diagram

Circuit Description by Functional Group (refer to the block diagram Figure 4.1):

1. Nav Receiver :

The Nav Receiver connects to a VOR/Localizer antenna via BNC connector J1 at the rear of the DVX-750 module. For lightning protection the input signal is immediately bypassed by gas-discharge tube G1 if the voltage exceeds 90V peak. The desired radio signal or any remaining pulse from a lightning strike, passes thru a 2000V series DC blocking capacitor to shunt choke L95, which shorts out any remaining remnant of a lightning strike without significantly loading the desired radio signals.

Next the received signal is bandpass filtered (includes L2, L15, L26 etc) to reduce the level of interference from the FM radio band (88Mhz to 108Mhz) before applying the signal to the first stage LNA amplifier, U1. Just in front of the LNA is a PIN diode attenuator, D3, which is autonomously activated when the RF monitor U22 senses an overload condition (e.g. when an adjacent aircraft is transmitting). The FM rejection filter has a switchable high end notch, which cuts the passband from 10Mhz to approximately 5Mhz when a VHF Comm transmitter is keyed on the same aircraft. This avoids self-interference with Localizer reception, which is especially critical during final approach.

After the LNA is a 6^{th} order LC bandpass filter (includes L10, L5, L23, L6, etc) which provides more rejection of out-of-band interfering signals. Following this is a switchable attenuator (U4, R13, R14, etc) providing either 0dB or 12dB attenuation which is switched in when the A-to-D converter (U20) on the Digital board approaches an overload condition.

The last two amplifier stages (U3 and U2) provide gain to enhance sensitivity and are separated by a differential bandpass filter which further suppresses out-of-band interference.

The signal was converted from single ended (unbalanced) to balanced at transformer (T2) just after the LNA, so the interface between the RF board and Digital board is a 200 ohm differential pair transmission line. The differential pair is shielded by the six adjacent pins as it passes thru stacking connector J5.

On the Digital board the signal is transformer coupled by T3, then passes thru a single tuned LC stage (L5 and C68) providing some suppression of digital noise and clock signals. U20 converts the analog signal to a 12-bit parallel data stream. The digital downconverter IC, U12 provides carrier lock, channelization filtering and AGC, and AM demodulation and audio formatting and mixing is performed digitally in DSP1, U19. Audio signals are routed to the correct output channel via CODECs U42, U44 or U50 and associated output amplifiers which convert the digital output to audio signals suitable for driving headphones, speakers or other audio devices.

2. Glideslope Receiver :

The Glideslope Receiver connects to the Glideslope antenna via BNC connector J3 at the rear of the DVX-750 module. The input signal is lightning protected by the same combination of components used in the Nav receiver (see previous description), using a gas-discharge tube, 2000V series capacitor and RF choke to ground.

Next the received signal is bandpass filtered (L28, L32 and associated tuning capacitors) to reduce the level of out-of-band interference before feeding the LNA. There is no provision for adjusting front-end gain or damping signal overloads since nearby frequencies are not generated on an aircraft.

The LNA output feeds a SAW filter via LC matching elements. The SAW filter passband is 315 to 335MHz which provides anti-alias filtering such that the digitizer can undersample the RF signal without creating alias bands outside the Glideslope frequency band. The SAW filter output is applied to transformer T5 to feed differential amplifier U5. Next a differential filter (L98, L99, etc), and a 12dB gain step is applied before final amplification at U7 and transmission to the Digital board via J5.

On the Digital board the signal is transformer coupled by T2, LC filtered by L4 and C67, and A-to-D converted by U20. Processing by the DDC is nearly identical to the Nav receiver.

3. Marker Beacon Receiver:

The Marker Beacon signal is locally generated at 3miles, 1mile and ½ mile from the end of the runway, and is always at 75MHz. The distance is indicated to the pilot by different audio frequency tones which are AM modulated onto the 75MHz carrier.

The Marker Beacon Receiver connects to the Marker Beacon antenna via BNC connector J4 at the rear of the DVX-750 module. The input signal is lightning protected by the same combination of components used in the Nav and Glideslope receivers (see description in section 1 above), using a gas-discharge tube, 2000V series capacitor and RF choke to ground.

Next the received signal is bandpass filtered (L34, L39 and associated tuning capacitors) to reduce the level of out-of-band interference before feeding the LNA. Large signals are handled by desensitizing the entire receiver, which shifts the available dynamic range high enough to accommodate adjacent TV channels 4 & 5. The signal amplitude is dropped in R43 and R44 prior to the overload protection diode at D7 and the LNA, U11. There is no switchable gain anywhere in the Marker Beacon receiver.

The output of the LNA feeds a crystal filter, FL3 which attenuates the strong TV signals sufficiently to avoid overloading the ADC. A final filter (L35, C89, and C90) provide anti-alias filtering before the last amplifier U10 sends the signal to the Digital board via J5.

On the Digital board the signal is transformer coupled by T4, LC filtered by L9 and C109, and A-to-D converted by U36. Processing by the DDC, U45 is nearly the same as for the Glideslope receiver, and AM detection and audio output is performed by DSP1 and the selected CODEC and audio output circuitry as described in section 1 above.

4. Comm Receiver :

The VHF Communication Receiver connects to the T/R switch (implemented with PIN diodes D11, D12 and D13) which connects to a VHF antenna via BNC connector J6 and allows the same antenna to be utilized for transmission or reception. See T/R switch description.

The received signal is bandpass filtered (includes L60, L40, L62 etc) to reduce the level of interference from the FM radio band (88Mhz to 108Mhz) before applying the signal to the first stage LNA amplifier, U12. Just in front of the LNA is a PIN diode attenuator, D10, which is autonomously activated when the RF monitor U31 senses an input overload. The Comm receiver front-end is also contolled by the A/D converter (U37 on the Digital card) to switch in 12 dB of attenuation (using R60 and D9) along with 12dB further along to produce a 24dB stepped attenuation to handle large in-band signals (or leakage of out-of-band signals).

After the LNA is a 6th order LC bandpass filter (includes L46, L43, L64, L44, etc) which provides more rejection of out-of-band interfering signals. Following this is a switchable attenuator (U15, R64, R65, etc) providing either a 0dB or 12dB attenuation which is activated at the same time as the front-end attenuator (using R60 and D9).

The last two amplifier stages (U14 and U13) provide gain to enhance sensitivity and are separated by a differential bandpass filter (L47, L66, etc) which further suppresses out-of-band interference.

The signal was converted to a balanced differential signal at transformer (T10) just after the first amplifier and continued to be processed as a differential signal from there on, so the interface between the RF board and Digital board is a 200 ohm differential pair transmission line. The differential pair is shielded by the six adjacent pins as it passes thru stacking connector J5.

On the Digital board the signal is transformer coupled by T5, then passes thru a single tuned LC stage (L10 and C110) providing some suppression of digital noise and clock signals. U37 converts the analog signal to a 14-bit parallel data stream which feeds DDC, U45. the DDC provides carrier lock, channelization filtering and AGC. AM demodulation and audio formatting and mixing is performed digitally in DSP1, U19. Audio signals are routed to the correct output channel via CODECs U42, U44 or U50 and associated output amplifiers which convert the digital output to audio signals suitable for driving headphones, speakers or other audio devices.

5. T/R Switch:

BNC connector J6 provides both input and output for the VHF Comm transceiver, and therefore, use of the same antenna. When set to the “transmit” position, the nominal 16W (55W peak) transmitter output is applied via PIN diode D13 and passes thru the transmitter harmonic filter to the BNC, while the receiver is protected from the high voltage (150V peak- to-peak) by L70 and by D12 shunting any leakage signal to ground. In the “receive” state D13 is shut off, becoming a high impedance which keeps the PA from loading the input signal. The series impedance of L70 is now cancelled by C196 forming a nominal 50-ohm path between antenna input and the Comm receiver. The array of chokes and resistors surrounding these components apply the correct DC bias to the PIN diodes to switch from “receive” to “transmit” when discrete logic signal T_RN changes. Q6 and Q10 translate the 3Volt logic signal to the 24V drive signals used by the T/R switch.

6. Harmonic Output Filter

L83, L86, and associated capacitors form a VHF band (118 – 137 MHz) filter with L91 creating a notch in the frequency range where the 2^{nd} harmonic falls. Above the 2^{nd} harmonic, the tuning provided by L83 and L86 is sufficient to suppress harmonic output of the final amplifier. G4 is a gas-discharge tube with a 240V trigger voltage to clamp lightning surge voltages to ground at the input BNC. The Bandpass nature of the harmonic suppression filter is sufficient to attenuate the residual lightning surge allowed by the GDT (i.e. 240V and more during activation of the GDT).

7. VHF Power Amplifier (PA):

The RF board receives a signal created on the Digital board by the Digital Upconverter (DUC). The signal enters via J5 as a differential signal at about -1dBm and is transformer coupled by T12. Transmitted signal level is adjusted by attenuator R75, R76, R77 and R81. Clock noise, spurious DUC output, and digital noise is suppressed by a differential input filter (L67, L75/L76, L74/L82, etc) then a driver signal of approximately 200mW is generated by U17 and U18. This differential signal is applied to the intermediate stage push-pull amplifier Q5, a 40W RF MOSFET and then to Q4 which is a 90 Watt MOSFET device. Bias voltage, “FET_BIAS” is switched off by Q13 when not transmitting and is applied to Q5 via the coupling transformer and to Q4 via RF chokes. Inductors L90 and L87 along with C231, C229, C227, C219 etc, provide impedance matching of the RF MOSFETs. The push-pull output is coupled to the 50-ohm single-ended output by the rigid coaxial transformer T16.

8. Transmit signal generator:

The Digital Upconverter (DUC) U46 has a 48-bit internal direct digital synthesizer (DDS) and an integrated 14-bit digital-to-analog converter, allowing it to output a differential analog signal ready for amplification and transmission. The DUC is fed a digital audio baseband via a 14-pin input bus, which is applied to the DDS output to create AM modulation (i.e. it multiplies the carrier amplitude). The audio signal from the selected input source ("MIC_LINE_1 to 6) is digitized in an audio CODEC and formatted for the DUC by DSP1. The current-source output from the DUC is coupled and filtered (L18, L19, L14, L15, L13 and associated capacitors), amplified by U38, then filtered (L601, L602 and associated caps), amplified again at U601 then applied to mixer U641. The LO for the mixer comes from a phase-locked loop synthesizer formed primarily by U630 and U602, then amplified at U640, and filtered (L721, L723, L724 and associated caps). The DUC output is always at 53MHz, while the synthesizer output varies from 171 to 190 MHz, thus producing the required range of carrier frequencies of 118-137 MHz, which is Bandpass filtered (L695, L643, L691 etc) and amplified to drive the connection to the RF board via J6.

Transmitter frequency stability and accuracy: TCXO Y64 provides a frequency stability of 1.5ppm for the PLL synthesizer, and XO Y65 (a 50ppm device) provides frequency accuracy for the DUC clock. To compensate for the poorer accuaracy of Y65 the pdclk signal from the DUC is monitored in FPGA U33 and compared to the output of reference oscillator Y4, which is also a 1.5ppm device. Frequency errors are then compensated by offsetting the frequency commands that are written by DSP1 to the DDS registers inside U46.

Receiver frequency stability and accuracy: VCXOs Y1 and Y3 provide the processing clocks for the receiver ADC and the DDC chips. These are less accurate than the 20MHz TCXO, Y4, so the clock frequencies are compared by counters in U33 and adjustments are made via the DAC (U25) to pull the VCXO clock sources to approximate the 1.5ppm accuracy of the TCXO.

9. Data Bus Interface:

Small amounts of data need to be sent and received by the VHF radio module, such as outputting computed navigational data (to the host ACR) for display on the PFD, or setting operating frequencies (from host PFD's ACR computer). This data is transferred via a Byteflight databus. The physical layer is RS485 compliant (120 ohm differential shielded pair) and the data packets are similar to Ethernet (10 Mbps) but are sent in assigned time-slots vs the random access used in IEEE 802.x protocols. The Motorola 9S12 Data Bus Processor is specifically made to conduct communication via the Byteflight interface. Byteflight is a multi-node databus capable of supporting over 100 devices on the same physical cable so the VHF radio module is likely to be one of many devices sharing a common databus when operating in a PFD. An RS-232 serial interface is also provided for automated test functions, but is not active when configured for operational use.

10. Power Supply, Distribution and Regulation:

28V_In - Primary input power to the Nav/Com module is the 28VDC directly from the aircraft power bus, which may varies from 20V to 30.5V as the battery charge level changes. The raw input is clamped by an overvoltage/undervoltage protection circuit using Q1. If voltage exceeds 30V the input voltage is clamped at 30V, but if voltage drops below 11V the input voltage is shut off by Q1. D4 and D5 sense the input voltage.

26V_PA – The conditioned primary power is fed to the transmitter PA (Q4) via FET switch Q14 which can be shut off under software control (if any potentially dangerous anomaly is detected) or autonomously when an overtemperature condition is sensed by thermal sensor U30. PA power is further conditioned by common-mode choke T17 and bypass caps C220, C246 and C364, and is protected against device failure by fuse F2.

23V_DR – Power to the intermediate stage amplifier, Q5, is regulated down to 23V by U32 and isolated by common-mode choke T11.

12V – A synchronous switching power supply controller U401 controls MOSFET switching transistors M401 and M402 to create both 3.3V and 12V outputs. M401 is involved in generating 12V. The 12V output is used directly by the audio circuitry on the Digital Board and is fed thru the connector J5 via common-mode choke T7, and is used to create secondary voltages on the RF Board.

10.3V – 12V is regulated down to 10.3V by U33 to drive differential amplifiers U17 and U18 in the transmitter. Q13 disconnects power to U18 to save power when not transmitting.

5.3V - The 12V output is also regulated down to 7V by U27, then at the input to each receiver it is regulated down to 5.3V. The two stages maximize isolation of power to the receivers.

3.3V – Also an output of the switching power supply implemented by U401 and M402, 3.3V is only consumed on the Digital Board, and is fed to connector J5 via common-mode choke T4. 3.3V is primary power for most of the Digital board, but linear regulators U9, U15 and U16 also make 2.5V and U4 and U10 create 1.6V core voltages for digital ICs.