

Detailed description of modulation system

There are two modulation schemes, 2-FSK and 4-FSK. The details are as follows:

Parameter	Requirement	Notes
Transmit power	<10.8 dBm EIRP	FCC limit
Frequency accuracy	$\pm 2.5\text{ppm} = \pm 1.5\text{kHz}$	
Modulation – low rate	2FSK in 31.25kHz channel	Symbol rate 8.333kSym/s
Modulation filtering	Gaussian with BT = 0.5	
Deviation error	$\leq \pm 15\%$ of nominal	
Adjacent channel power, channel $n \pm 1, 2$	$\leq -60\text{dBc}$	
Adjacent channel power, channel $n \geq \pm 3$	$\leq -83\text{dBc}$	4 exceptions allowed
Frequency lock time	$\leq 3\text{s}$	At power-up
Transmitter residual FM	$\leq 50\text{Hz rms}$	
Transmitter microphony	$\leq 1\text{kHz peak}$	Under normal handling
Out of band spurious emissions $f < 960\text{MHz}$	$\leq -49.2\text{dBm EIRP}$	$\leq 200\mu\text{V/m}$ at 3m in 120kHz
Out of band spurious emissions $960\text{MHz} < f < 6.14\text{GHz}$	$\leq -41.3\text{dBm EIRP}$	$\leq 500\mu\text{V/m}$ at 3m in 1MHz

DC voltages and currents into final radio amplifying device

Final radio amplifying device is supplied from a DC bias control circuit. The DC voltage is kept below 2.8Volts (typically 2.3V) and the DC current is kept below 18mA (typically 15mA).

DC voltage supply to the bias circuit is from a $3.3\text{V} \pm 5\%$ regulated supply line.

Means for determining and stabilising frequency, suppression of spurious radiation, limiting modulation and limiting power

Means for determining and stabilising frequency:

Transmit modulation is generated using a discrete Voltage Control Oscillator (VCO) and Phase Lock Loop (PLL) based frequency synthesiser.

A 10MHz VC-TCXO (Voltage Control – Temperature Compensated Crystal Oscillator) is used as reference to the PLL.

Suppression of spurious radiation:

As stated below, various radio design techniques are applied to ensure spurious radiation is kept well below the specification limits.

1. All transmit stages including the final amplifying stage is designed inside the screening cans.
2. Use of L-C-R (Inductor, Resistor, Capacitor) filters and de-coupling capacitors at various stages of the design.
3. Where possible, band-pass circuit topology/matching was used in the cascaded radio design.
4. A low-pass filter is designed in after the final radio amplifying stage to provide additional suppression of spurious radiation above the transmit frequency.
5. Combination of PIN diode attenuator with DC bias controlling of the final radio amplifying stage is used to attenuated VCO signals below specification limits during power-up and locking the frequency synthesiser circuits of the radio.

Limiting modulation:

DAC (Digital-to-Analogue) output is Gaussing filtered to keep the modulation within the limits.

Limiting power:

DC bias control techniques are used on all stages of the transmit radio design to ensure transmit power is kept below the specification limits. Additionally, the radio was design to

transmit at least 3dB below 10.8dBm EIRP (specification allowed maximum) under the worst case conditions.