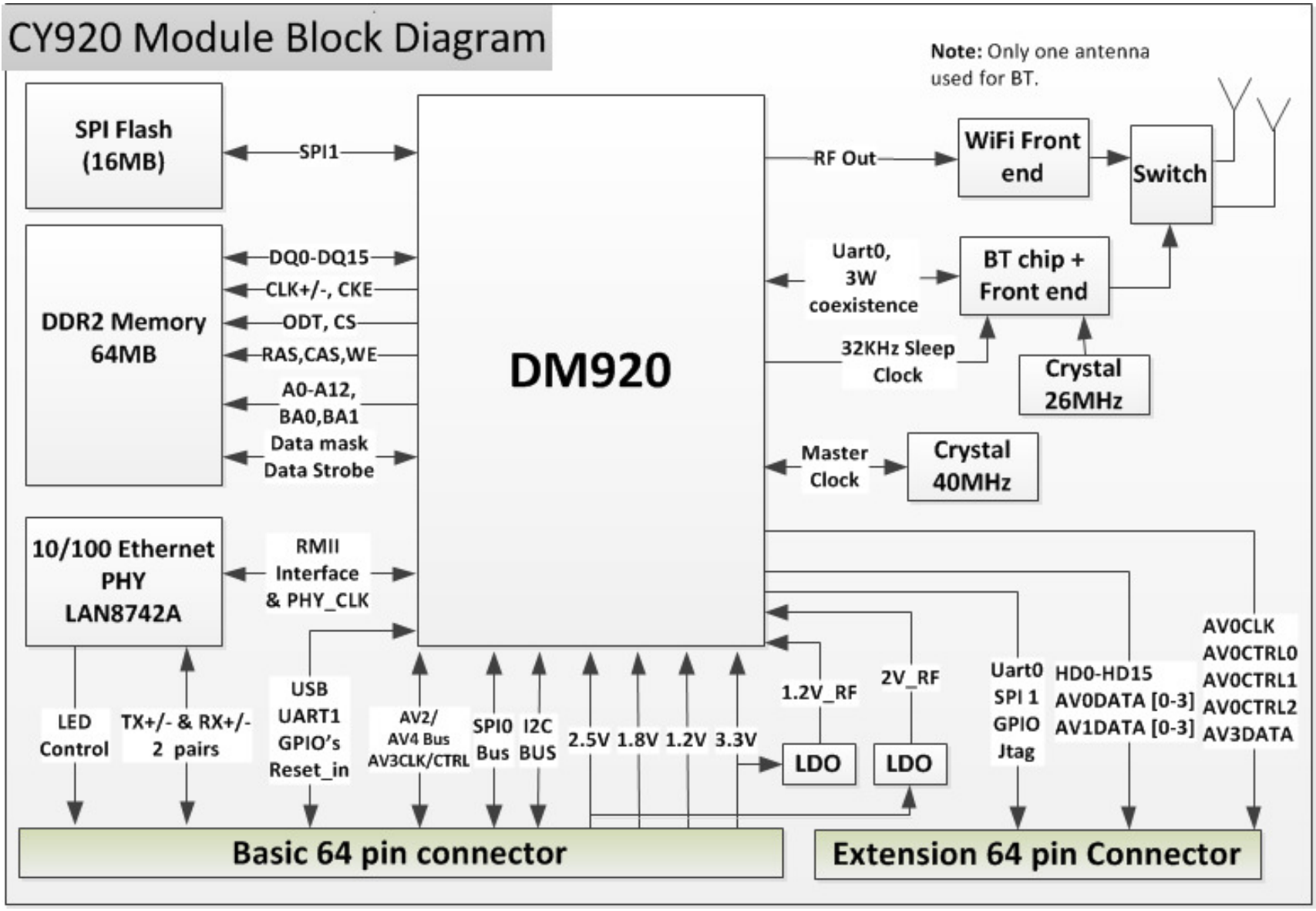
CY920 Module Block Diagram



MICROCHIP CONFIDENTIAL	Project: CY920 Module	Revision: PVT
	Title: BLOCK DIAGRAM	Friday, June 27, 2014
	Engineer: Chetan Bohra Checked: Sujith/Sanjay	Sheet 1 of 9 Size A

NOTE: SKU-24C is identical to SKU-C

REMARK:
Resistors R127 ~ R131, R133 should be close to SPI flash.
Signal from DM920 to SPI should be as short as possible.

SKU-A (-)
SKU-B (POP)
SKU-C (POP)

UART, SPI, I2C, I2S

UART
JTAG
SPI0
I2C
SPI1

HDMI CONTROL SIGNALS
HDMI CONTROL SIGNALS
HDMI CONTROL SIGNALS

I2S

EXTENSION CONNECTOR

SPI Flash

MX25L12835FMI-10G

DDR2 MEMORY

OPTION (DO NOT POP)

0.9 Volts output
300mA max
SOT-23-5

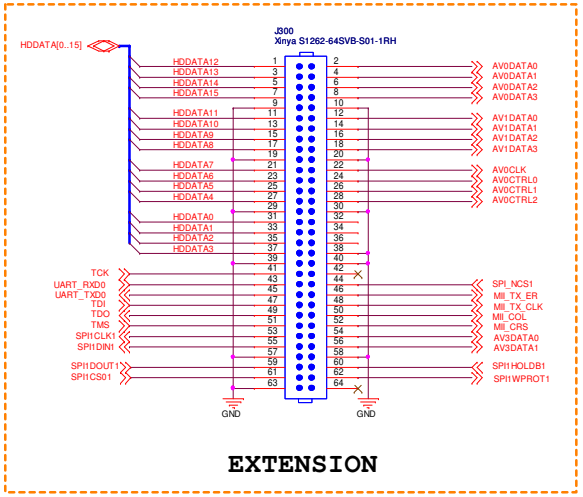
M14D5121632A -2.5BG2K

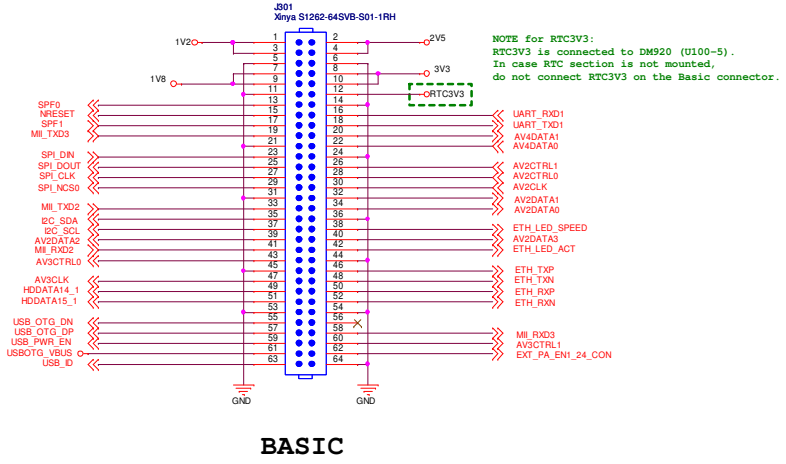
[DM920] Boot Options

SPI0DOUT	SPI1DIN	SPI1DOUT	Boot Mode
0	0	0	SPI Flash boot (NOR Flash, single lane mode, normal read in firmware mode) through SPI1)
0	0	1	I2C EEPROM boot (micro-boot, secondary boot) through I2C
0	1	0	SPI Slave boot (via Host) through SPI0
0	1	1	Reserved
1	0	0	SPI Flash boot (NOR Flash, single lane mode, Fast Read mode) through SPI1
1	0	1	Reserved
	1	0	
	1	1	

MICROCHIP CONFIDENTIAL

Project: CY920 Module		Revision: PVT
Title: DM920 MEMORY/FLASH		Friday, June 27, 2014
Engineer: Chetan Bohra	Checked: Sujith/Sanjay	Sheet 2 of 9
		Size C



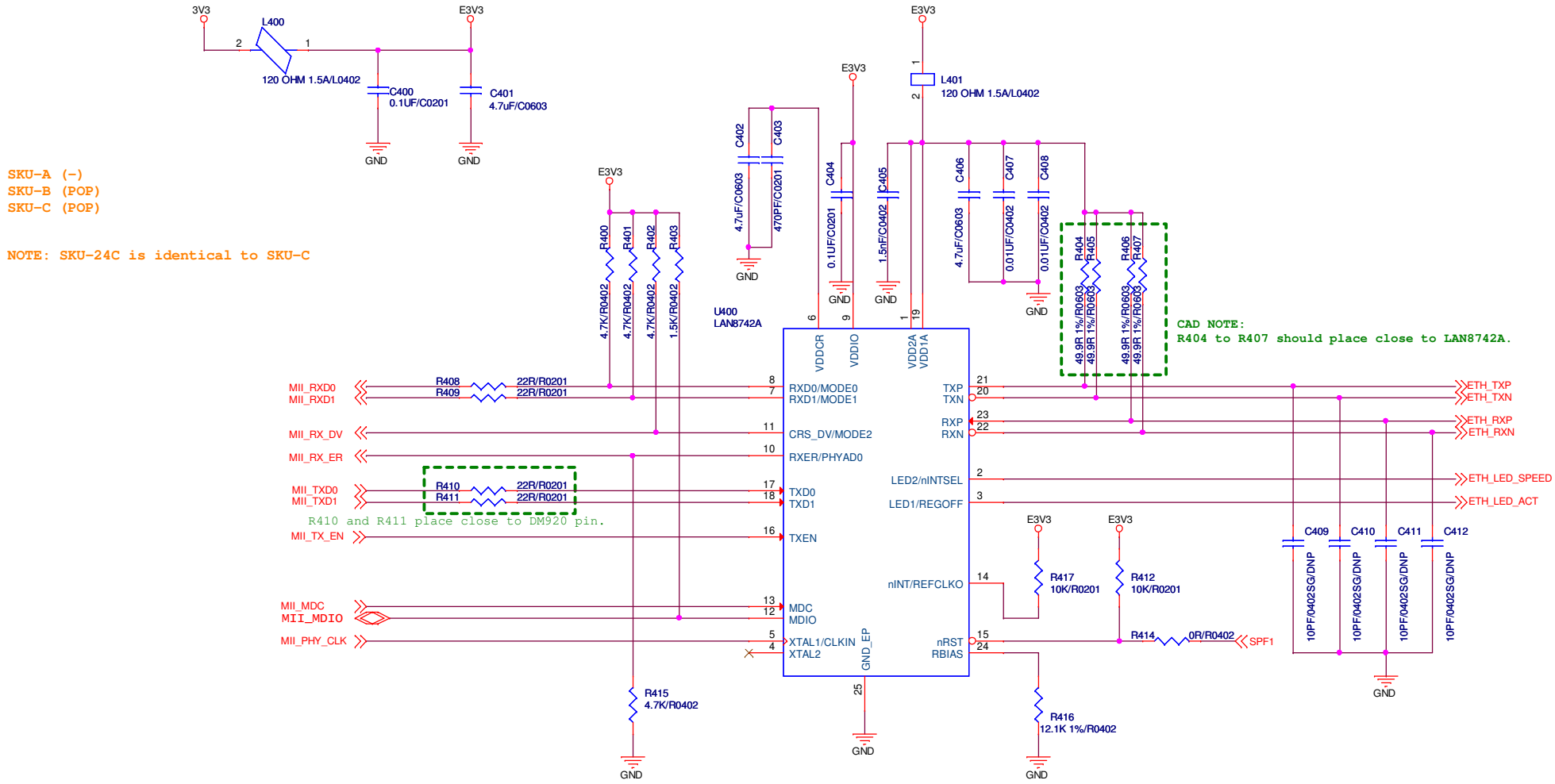


GPIO CY920 Mapping V2.0 (BSEL using GPIO Mode) (BSEL mode select needs H/w change also)

GPIO Number	DM920 Pin name	connected to where	Group	Group Select	Assigned Function
0	MIICRS	BT/Extension	A	2	WLAN_ACTIVE
1	MIICOL	BT/Extension	A	2	BT_PRIORITY
2	MIITXER	BT/Extension	A	2	BT_ACTIVE
3	MITXCLK	BT/Extension	A	2	BT LDO_ON
4	AV3CLK	Basic	B	4	SPI_E_SDO (FREE)
5	AV3CTRL0	Basic	B	4	SPI_E_CLK (FREE)
6	AV3CTRL1	Basic	B	4	SPI_E_SDI (FREE) (Expansion FlashCS)
7	AV0CTRL2	extension (If no HD)	B	4	FREE
8	MIITXD2	Basic	C	4	Factory Reset
9	MIITXD3	Basic	C	4	IR Input
10	MIIRXD2	Basic	C	4	Host NIREQ
11	MIIRXD3	Basic /BT	C	4	SPI_E_NCS (FREE)
12	HDDATA12	extension(If no HD)	D	7	FREE
13	HDDATA13	extension(If no HD)	D	7	FREE
14	HDDATA14	Basic/extension(If no HD)	D	7	FREE
15	HDDATA15	Basic/extension(If no HD)	D	7	FREE
16	SF0	Basic	E	3	HD_INT
17	SF1	Ethernet chip	E	3	NETH_RESET (Not free when ethernet used)
18	EXT_PA_EN1_5	Basic	F	5	FEM BSEL (Not free used in module)
19	EXT_PA_EN1_24	Basic	F	5	FREE

GPIO CY920 Mapping V2.0 (BSEL using Hardware Mode) (BSEL mode select needs H/w change also)

GPIO Number	DM920 Pin name	connected to where	Group	Group Select	Assigned Function
0	MIICRS	BT/Extension	A	2	WLAN_ACTIVE
1	MIICOL	BT/Extension	A	2	BT_PRIORITY
2	MIITXER	BT/Extension	A	2	BT_ACTIVE
3	MITXCLK	BT/Extension	A	2	BT LDO_ON
4	AV3CLK	Basic	B	4	SPI_E_SDO (FREE)
5	AV3CTRL0	Basic	B	4	SPI_E_CLK (FREE)
6	AV3CTRL1	Basic	B	4	SPI_E_SDI (FREE) (Expansion FlashCS)
7	AV0CTRL2	extension (If no HD)	B	4	FREE
8	MIITXD2	Basic	C	4	Factory Reset
9	MIITXD3	Basic	C	4	IR Input
10	MIIRXD2	Basic	C	4	Host NIREQ
11	MIIRXD3	Basic /BT	C	4	SPI_E_NCS (FREE)
12	HDDATA12	extension(If no HD)	D	7	FREE
13	HDDATA13	extension(If no HD)	D	7	FREE
14	HDDATA14	Basic/extension(If no HD)	D	7	FREE
15	HDDATA15	Basic/extension(If no HD)	D	7	FREE
16	SF0	Basic	E	3	HD_INT
17	SF1	Ethernet chip	E	3	NETH_RESET (Not free when ethernet used)
18	EXT_PA_EN1_5	Basic	F	5	Not Available
19	EXT_PA_EN1_24	Basic	F	5	FEM BSEL (Not free used in module)



MICROCHIP CONFIDENTIAL	Project: CY920 Module	Revision: PVT
	Title: ETHERNET PHY	Friday, June 27, 2014
	Engineer: Chetan Bohra Checked: Sujith/Sanjay	Sheet 4 of 9 — Size C

NOTE: SKU-24C is identical to SKU-C

SKU-A (-)
SKU-B (POP)
SKU-C (POP)

U100-7
DM920
VIDEO, HD

HDDATA[0..15]

EXTENSION CONNECTOR

HDDATA0 R502 220R/R0201 HD0 H4
HDDATA1 R503 220R/R0201 HD1 K6
HDDATA2 R511 220R/R0201 HD2 H5
HDDATA3 R513 220R/R0201 HD3 H3
HDDATA4 R504 220R/R0201 HD4 J4
HDDATA5 R515 220R/R0201 HD5 J5
HDDATA6 R505 220R/R0201 HD6 L6
HDDATA7 R506 220R/R0201 HD7 J2
HDDATA8 R507 220R/R0201 HD8 J1
HDDATA9 R516 220R/R0201 HD9 K1
HDDATA10 R508 220R/R0201 HD10 K4
HDDATA11 R509 220R/R0201 HD11 K5
HDDATA12 R518 220R/R0201 HD12 L4
HDDATA13 R519 220R/R0201 HD13 K3
HDDATA14 R520 220R/R0201 HD14 K2
HDDATA15 R521 220R/R0201 HD15 L5

HDDATA0 HDDATA1 HDDATA2 HDDATA3 HDDATA4 HDDATA5 HDDATA6 HDDATA7 HDDATA8 HDDATA9 HDDATA10 HDDATA11 HDDATA12 HDDATA13 HDDATA14 HDDATA15

HDDATA14_1 R805 0R/R0201
HDDATA15_1 R806 0R/R0201

BASIC CONNECTOR

DO NOT POP

DM3V3
D500 BAT54/DNP
RTC3V3
C500 100NF/DNP
GND
C501 32.768KHz/DNP
15PF 2% HIQ/DNP
Y500
R807 20M/DNP
C503 15PF 2% HIQ/DNP
R533 510K/DNP

DM920 CLOCK & RESET

U100-5
DM920

CLOCK & RESET

A18 RTCVDD33
A19 RTCVSSD
A20 RTCXTALI
B17 RTCXTALO
F20 REFCLK
E20 REFSEL

BT_32K

NRES1V2REF B19
NRESVARIOREF C20
NRES1V2O B18
NRES_VARIO_O B20
NRESET P15

DM3V3
DM1V2
R500 13K 1%/R0201
R501 3K 1%/R0201
R512 20K 1%/R0201
R510 10K/R0201
R534 0R/0201
R536 0R/0201
R535 0R/0201
R514 10K/R0201
RESET
R517 100R/R0201
NRESET
C502 1NF/C0201
GND

SPF0 L20
SPF1 L19
SPF2 L17
SPF3 L16
TEST1 D13
R522 10K/R0201

VDD25_SYSPLL C17
VSS25_SYSPLL E16
VDD25_ETHPLL E17
VSS25_ETHPLL D16
VDD25_HDPLL D18
VSS25_HDPLL D17
VDD25_AVPLL C19
VSS25_AVPLL E19
VDD25_DDRPLL D20
VSS25_DDRPLL D19

C504 0.1UF/C0201
C507 0.1UF/C0201
C508 0.1UF/C0201
C509 0.1UF/C0201
C512 0.1UF/C0201
R523 100R/R0201
R524 100R/R0201
R525 100R/R0201
R526 100R/R0201
R527 100R/R0201

2V5
FB500
120 OHM 1.5A/L0402
C505 470PF/C0201
C506 10UF/C0603

CAD NOTE: PLL pins
Place all the discrete components for these PLLs
close to DM920 chip to have minimal jitter on PLLs.

3V3
FB501
120 OHM 1.5A/L0402
USB_3V3A
C513 10UF/C0603
C515 0.1UF/C0201
C516 10UF/C0603

USB_3V3A
C517 1UF/C0402
C518 1UF/C0402
VDDPLL
USB_VBUS

U100-3
DM920

USB OTG

G12 USBVDD33A
E15 USBVDDPLL
G14 USBVDD33PLLREF
G13 VBUS
A15 USBDP
A14 USBDM
B15 ID
C15 USBVBUSDRV
D15 NC
H13 NC
A16 XTAL1
A17 XTAL2
B16 RBIAS
J13 USBVSSA
L15 USBVSSPLL
K15 USBVSSREF

USB_OTG_DP
USB_OTG_DN
USB_ID
USB_PWR_EN
R528 100R/R0201
DM_USB_PWR_EN
USB_XTAL1
USB_RBIAS
R530 0R/R0201
R531 12K 1%/R0201

USBOTG_VBUS
USB_VBUS
R529 1K 1%/R0402
C519 0.1UF/DNP
C520 0.1UF/C0201

ETHERNET

G20 MIIRXD0
H20 MIIRXD1
H19 MIIRXD2
H18 MIIRXD3
J17 MIIRXCLK
J19 MIIRXDV
H17 MIIRXER
F17 MIITXD0
F16 MIITXD1
G16 MIITXD2
G17 MIITXD3
G19 MIITXCLK
F19 MIITXEN
F18 MIITXER
J16 MIICOL
H16 MIICRS
K19 MIIMDC
K20 MIIMDIO
J20 MIIPHYCLK

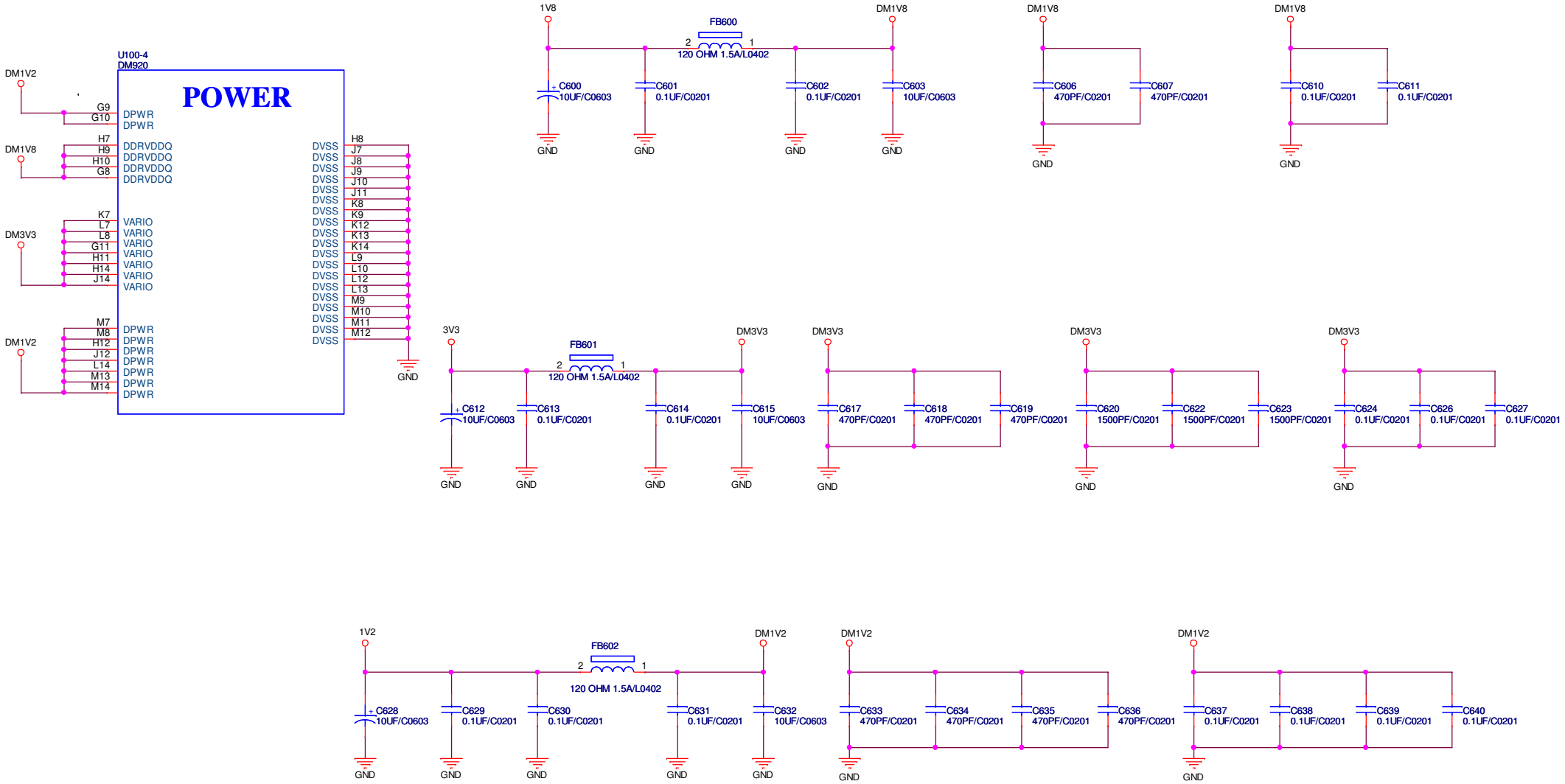
MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3
MII_RX_DV MII_RX_ER
MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3
MII_TX_CLK MII_TX_EN MII_TX_ER
MII_COL MII_CRS
MII_MDC MII_MDIO
R532 22R/R0201
MII_PHY_CLK

CAD NOTE:
R532 should place close to the driver (DM920).

CAD NOTE:
*AVOID RUNNING ANY HIGH SPEED TRACE NEAR USB_RBIAS AND R531
*PLACE THE BYPASS CAPS CLOSE TO THE CORRESPONDING PINS
Place R531 close to the IC pin.

MICROCHIP
MICROCHIP CONFIDENTIAL

Project: CY920 Module		Revision: PVT
Title: DM920 USB,Ethernet,Clock & HD		Friday, June 27, 2014
Engineer: Chetan Bohra	Checked: Sujith/Sanjay	Sheet 5 of 9 / Size C



MICROCHIP CONFIDENTIAL

	Project: CY920 Module	Revision: PVT
	Title: DM920 POWER SECTION	Friday, June 27, 2014
	Engineer: Chetan Bohra Checked: Sujith/Sanjay	Sheet 6 of 9 / Size C

RF Interface

Decoupling caps should place closely to IC power pins.

Note:
Connect L701 directly after L803.

Note:
R702 and R703 place as close as possible to the IC.

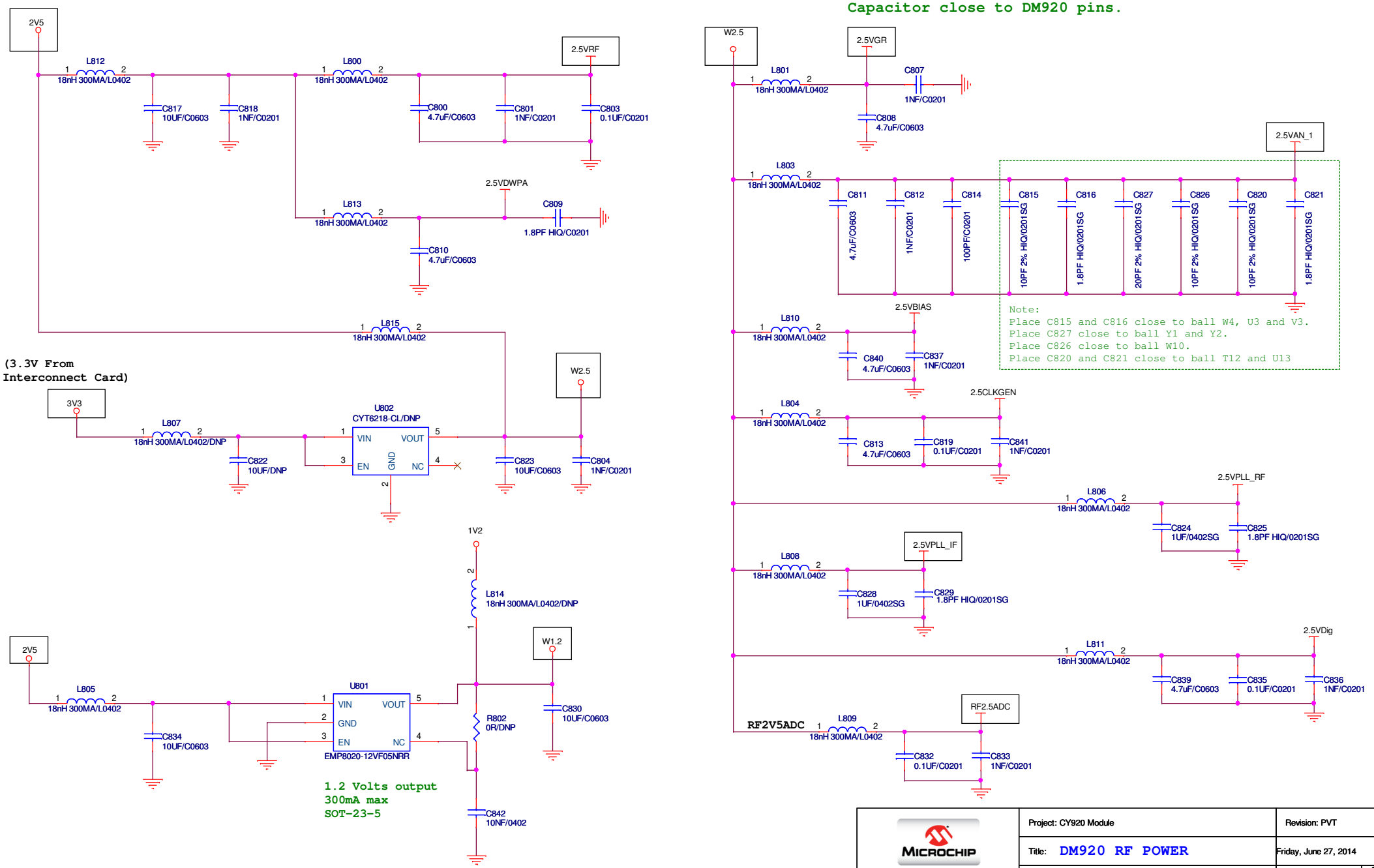
Delay needs to be matched.

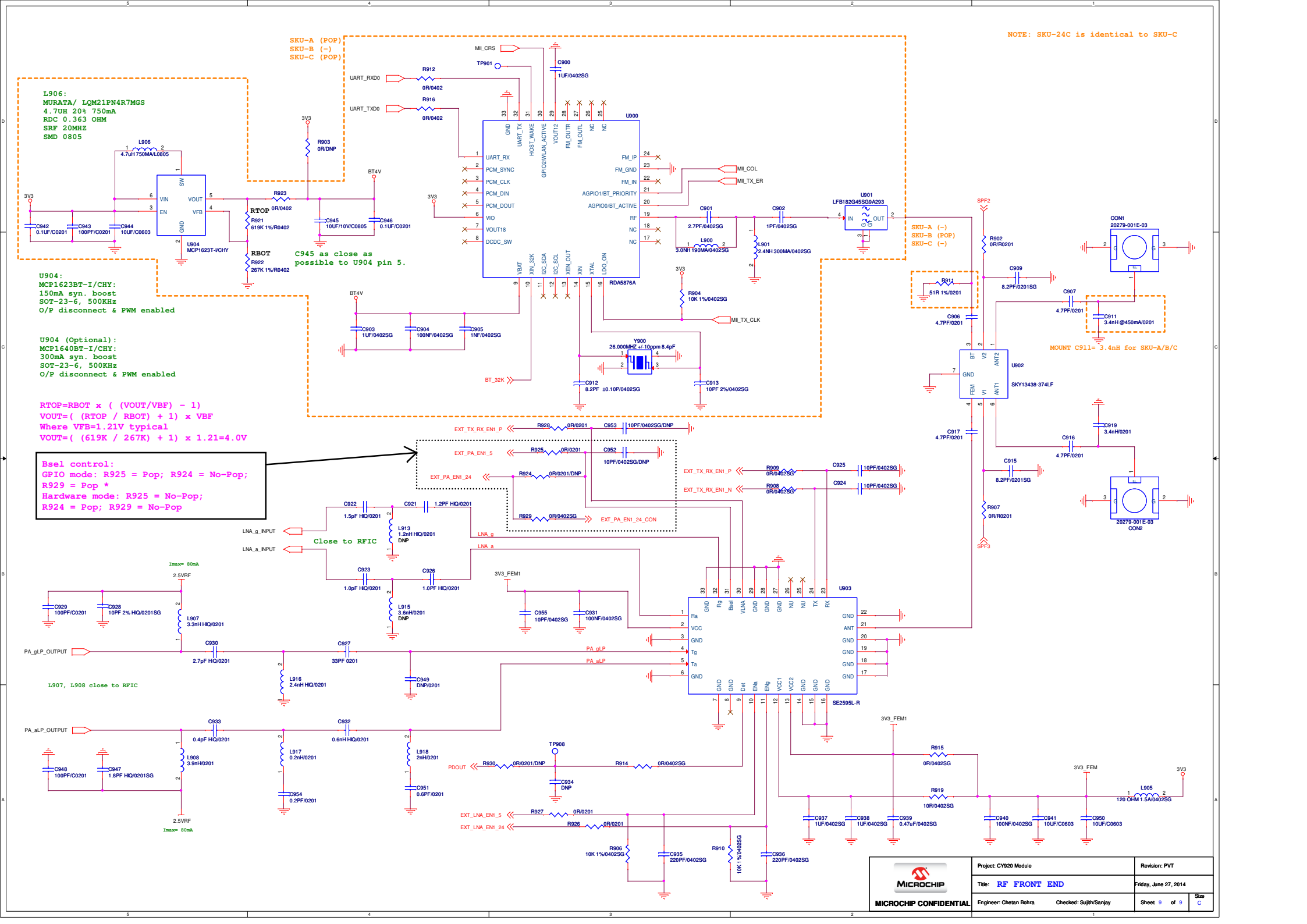
C730 close to pin T18.

U100-6
DM920

Project: CY920 Module			Revision: PVT
Title: DM920 RF SECTION			Friday, June 27, 2014
Engineer: Chetan Bohra	Checked: Sujith/Sanjay	Sheet 7 of 9	Size C

MICROCHIP CONFIDENTIAL


Capacitor close to DM920 pins.
2V5
L812
18nH 300MA/L0402
C817
10UF/C0603
C818
1NF/C0201
L800
18nH 300MA/L0402
C800
4.7uF/C0603
C801
1NF/C0201
2.5VRF
C803
0.1UF/C0201
2.5VDWPA
L813
18nH 300MA/L0402
C809
1.8PF HIQ/C0201
C810
4.7uF/C0603
L815
18nH 300MA/L0402
(3.3V From
Interconnect Card)
3V3
L807
18nH 300MA/L0402/DNP
C822
10UF/DNP
U802
CYT6218-CL/DNP
VIN
VOUT
EN
GND
NC
C823
10UF/C0603
W2.5
C804
1NF/C0201
1V2
L814
18nH 300MA/L0402/DNP
2V5
L805
18nH 300MA/L0402
C834
10UF/C0603
U801
VIN
VOUT
GND
EN
NC
EMP8020-12VF05NRR
R802
0R/DNP
W1.2
C830
10UF/C0603
1.2 Volts output
300mA max
SOT-23-5
C842
10NF/0402
W2.5
L801
18nH 300MA/L0402
2.5VGR
C807
1NF/C0201
C808
4.7uF/C0603
2.5VAN_1
L803
18nH 300MA/L0402
C811
4.7uF/C0603
C812
1NF/C0201
C814
100PF/C0201
C815
10PF 2% HIQ/0201SG
C816
1.8PF HIQ/0201SG
C827
20PF 2% HIQ/0201SG
C826
10PF 2% HIQ/0201SG
C820
10PF 2% HIQ/0201SG
C821
1.8PF HIQ/0201SG
Note:
Place C815 and C816 close to ball W4, U3 and V3.
Place C827 close to ball Y1 and Y2.
Place C826 close to ball W10.
Place C820 and C821 close to ball T12 and U13
2.5VBIAS
L810
18nH 300MA/L0402
C840
4.7uF/C0603
C837
1NF/C0201
2.5CLKGEN
L804
18nH 300MA/L0402
C813
4.7uF/C0603
C819
0.1UF/C0201
C841
1NF/C0201
2.5VPLL_RF
L806
18nH 300MA/L0402
C824
1UF/0402SG
C825
1.8PF HIQ/0201SG
2.5VPLL_IF
L808
18nH 300MA/L0402
C828
1UF/0402SG
C829
1.8PF HIQ/0201SG
2.5VDig
L811
18nH 300MA/L0402
C839
4.7uF/C0603
C835
0.1UF/C0201
C836
1NF/C0201
RF2.5ADC
RF2V5ADC
L809
18nH 300MA/L0402
C832
0.1UF/C0201
C833
1NF/C0201
MICROCHIP
MICROCHIP CONFIDENTIAL
Project: CY920 Module
Revision: PVT
Title: DM920 RF POWER
Friday, June 27, 2014
Engineer: Chetan Bohra
Checked: Sujith/Sanjay
Sheet 8 of 9
Size C


NOTE: SKU-24C is identical to SKU-C
SKU-A (POP)
SKU-B (-)
SKU-C (POP)
L906:
MURATA/ LQM21PN4R7MGS
4.7UH 20% 750mA
RDC 0.363 OHM
SRF 20MHZ
SMD 0805
U904:
MCP1623BT-I/CHY:
150mA syn. boost
SOT-23-6, 500KHz
O/P disconnect & PWM enabled
U904 (Optional):
MCP1640BT-I/CHY:
300mA syn. boost
SOT-23-6, 500KHz
O/P disconnect & PWM enabled
RTOP=RBOT x ((VOUT/VBF) - 1)
VOUT=((RTOP / RBOT) + 1) x VBF
Where VFB=1.21V typical
VOUT=((619K / 267K) + 1) x 1.21=4.0V
Bsel control:
GPIO mode: R925 = Pop; R924 = No-Pop;
R929 = Pop *
Hardware mode: R925 = No-Pop;
R924 = Pop; R929 = No-Pop
C945 as close as possible to U904 pin 5.
Close to RFIC
L907, L908 close to RFIC
MOUNT C911= 3.4nH for SKU-A/B/C
U900
RDA5876A
U901
LFB182G45SG9A293
U902
SKY13438-374LF
U903
SE2595L-R
CON1
20279-001E-03
CON2
20279-001E-03
MICROCHIP CONFIDENTIAL
Project: CY920 Module
Revision: PVT
Title: RF FRONT END
Friday, June 27, 2014
Engineer: Chetan Bohra
Checked: Sujith/Sanjay
Sheet 9 of 9
Size C