

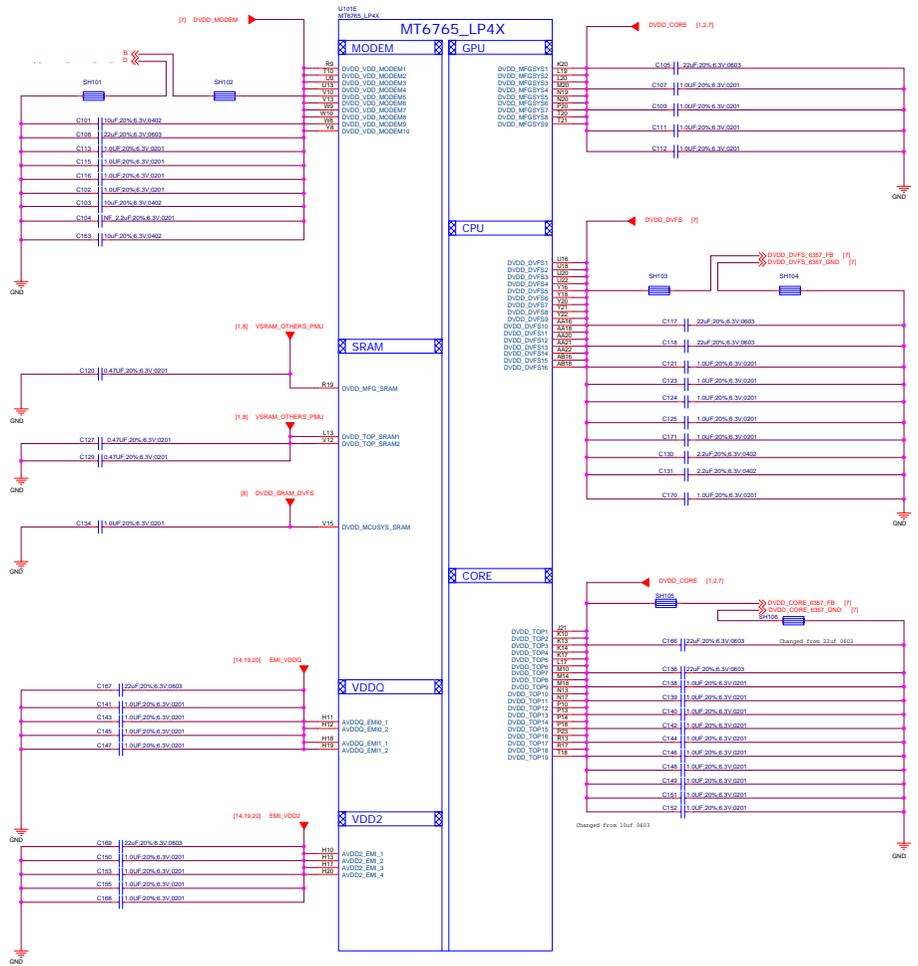
This schematic is for DH35 Project.

LM-K510EMW Works with:

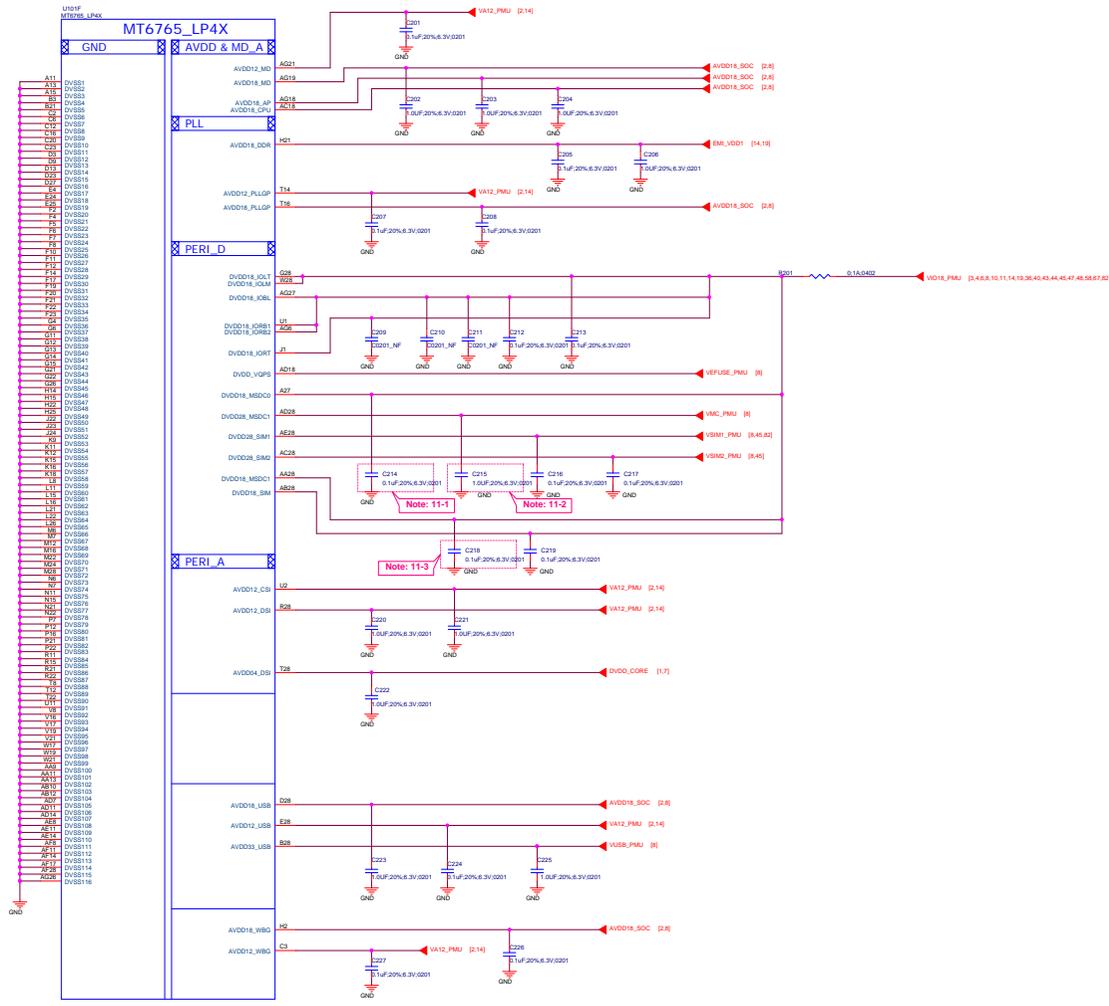
GSM quad band(GSM850/GSM900/DCS1800/PCS1900):

UMTS band(UMTS 1/2/5/8)

LTE FCC band 1,3,7,8,20,28: LTE TDD band 38.



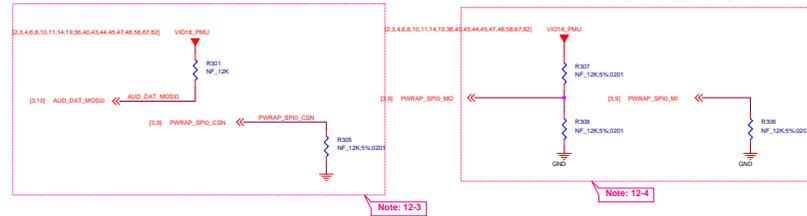
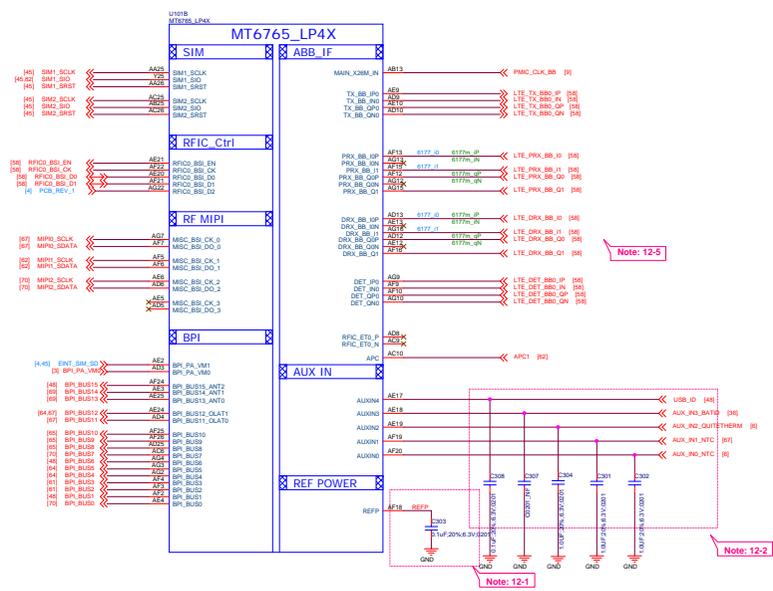
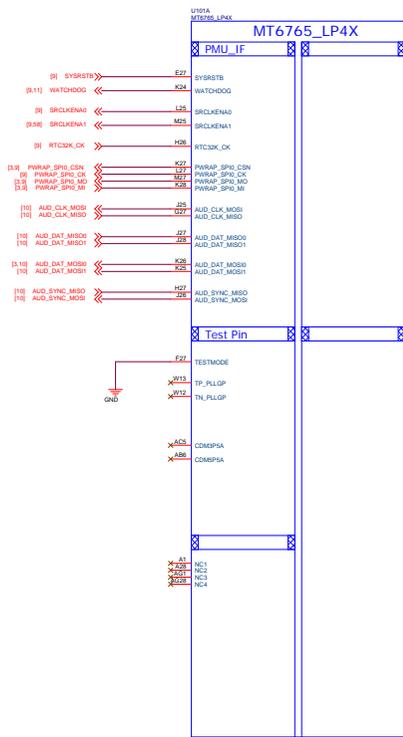
111x		02_BB_POWER_IO		REV: V10
DOCUMENT NO.:	Design Name			Size D
DEPARTMENT:	WINGTECH	DESIGNER: YL		
Date: Tuesday, December 17, 2019		Sheet	1	of 83



Schematic design notice of "11_BB_POWER_IO" page.

- Note 11-1: C214 closed DVDD18_MSDC0 150ml
- Note 11-2: C215 closed DVDD28_MSDC1 150ml
- Note 11-3: C218 closed DVDD18_MSDC1 150ml

111x	02_BB_POWER_IO	REV: V10
DOCUMENT NO.: Design Name		Size D
DEPARTMENT: WINGTECH-SH	DESIGNER: YL	
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Schematic design notice of "12_BB_1" page.

Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-3: *PWRAP_SPI0_CSN and *AUD_DAT_MOSI0 are bootstrap pin to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP_JTAG	JTAG Function
default=PU	default=PD		
HI	LO	N/A	N/A
HI	HI	(By est. PD)	SP10+EINT8
LO	LO	(By est. PD)	SP10+EINT8
LO	HI	(By est. PD)	MSDC1
			MD_JTAG
			SP1+SPI3
			N/A
			N/A

Note 12-4: PWRAP_SPI0_MI / PWRAP_SPI0_MO is DDR type feature in bootstrap

PWRAP_SPI0_MI	PWRAP_SPI0_MO	Booting interface
default=PU	default=PD	DDR
LO	LO	LPDDR3
LO	HI	N/A
HI	LO	LPDDR4X
HI	HI	LPDDR4

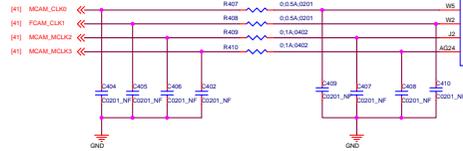
Note 12-5: Please set unused IQ pins in NC

Depth Camera 2M

Micro Camera 2M

Main Camera 32M

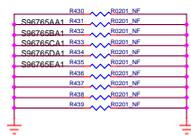
Wide Camera 5M
Front Camera 13M



Note: 13-1

Board ID

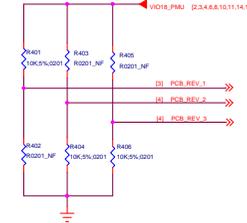
Model	REGION	WT CODE	PCB_INDICATOR_1	PCB_INDICATOR_2	PCB_INDICATOR_3	PCB_INDICATOR_4 (STM_CMBD)	PCB_INDICATOR_5 (DOR3+EMMC)



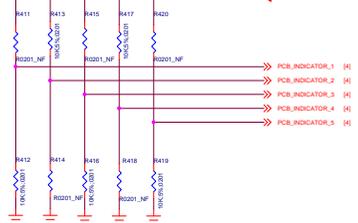
STAGE ID

PCBA VERSIONS	PCB REV			
	REV_1	REV_2	REV_3	
1_90	0	0	0	0
1_91	A	1	0	0
1_10	B	0	1	0
1_92	C	1	1	0
1_11	D	0	0	1
UNDETERMINED	1.0	1	0	1

PCB REV



PCB INDICATOR

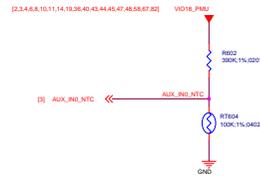


Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5].
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

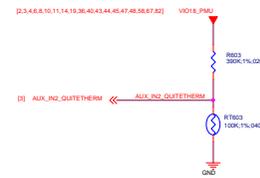
111x	04_BB_2_MIP1&GPIO	REV: V10
DOCUMENT NO.:	Design Name	Size: D
DEPARTMENT:	WINGTECHSH	DESIGNER: YL
Date:	Tuesday, December 17, 2019	Sheet 4 of 83

The pull up resister need to be 1% accuracy NTC=100K



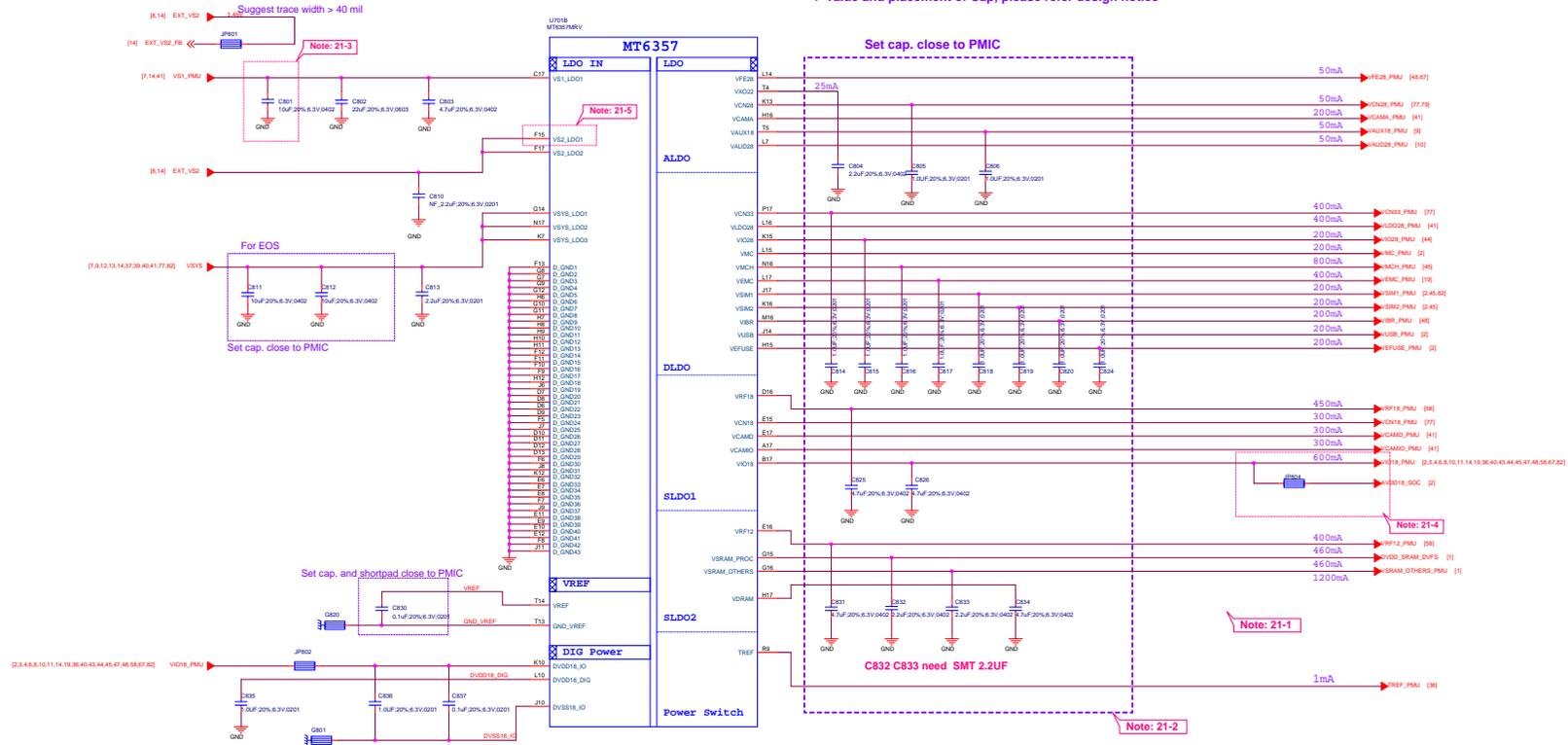
Thermistor to sense AP temperature

1. RT804 must keep a distance about 6-8 mm away from AP and far from other heat sources 40 mm at least.
2. The distance is the shortest distance from package edge to edge.



Quite thermistor

1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.
2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm)
=> value and placement of Cap, please refer design notice



Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

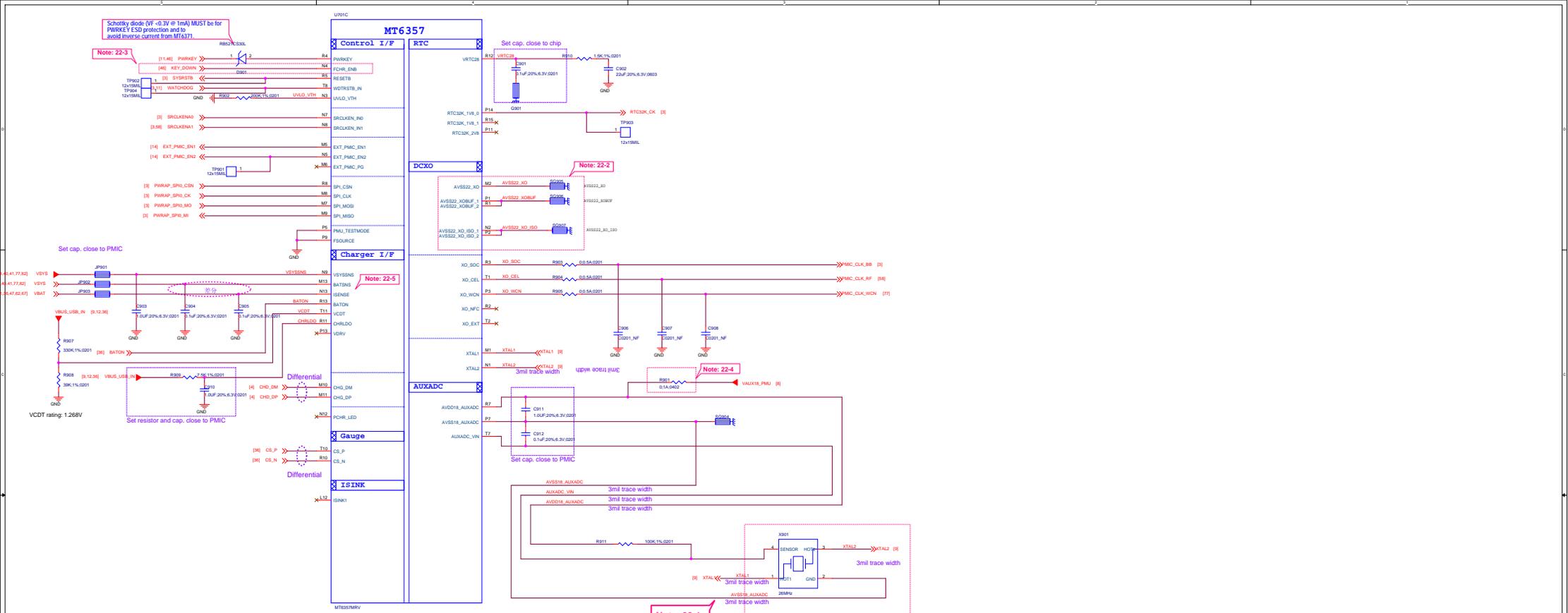
Note 21-3: Ext Buck BOM option

	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C801	10uF	22uF

Note 21-4: Please set R803 and R803 close to C826, making star connection among VIO18_PMU, AVDD18_SOC and EMI_VDD1 near to LDO cap. C826

Please also refer to MT6357 design notice for further detail design information

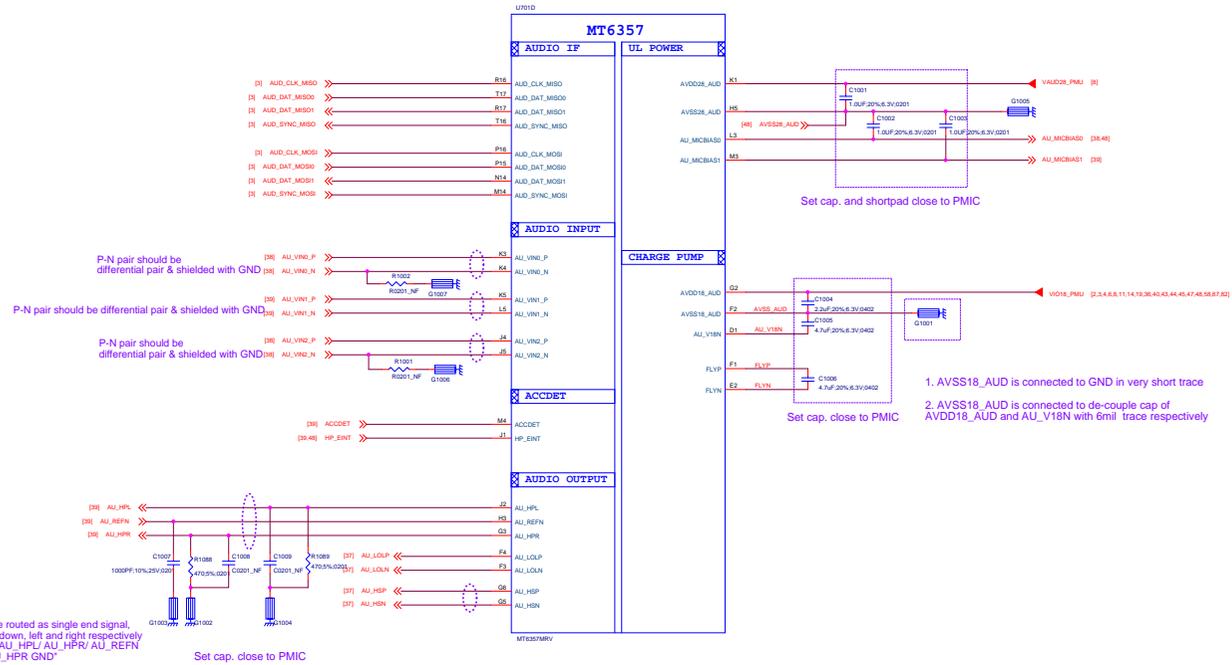
Note 21-5: Please also connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V



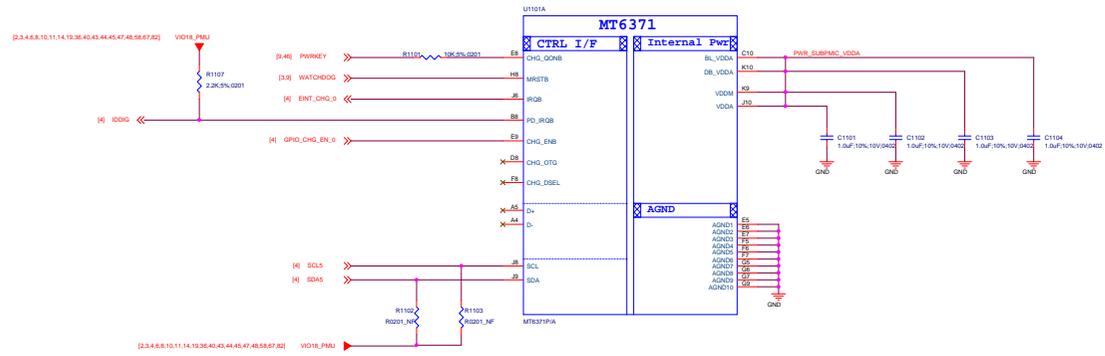
Schematic design notice of "22_POWER_MT6357-IF"

- Note 22-1: Please implement 2520 & 2016 Size TMS PCB co-layout. Please refer to MT6762_MT6357 Co-Clock Design Notice for co-layout guide
- Note 22-2: 1. Please Connect P1 and R1 ball first and then to GND
2. Please Connect P2 and N2 ball first and then to GND
3. Please connect DCXO GND to main GND by independent L1-2 GND via.; DO NOT connect it through L1 GND
- Note 22-3: Let floating if disable HOMEKEY function
- Note 22-4: Please follow MT6762_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD. Please route VAUX18_PMU with well-ground shielding if using 0 ohm to replace BEAD for AVDD18_AUXADC

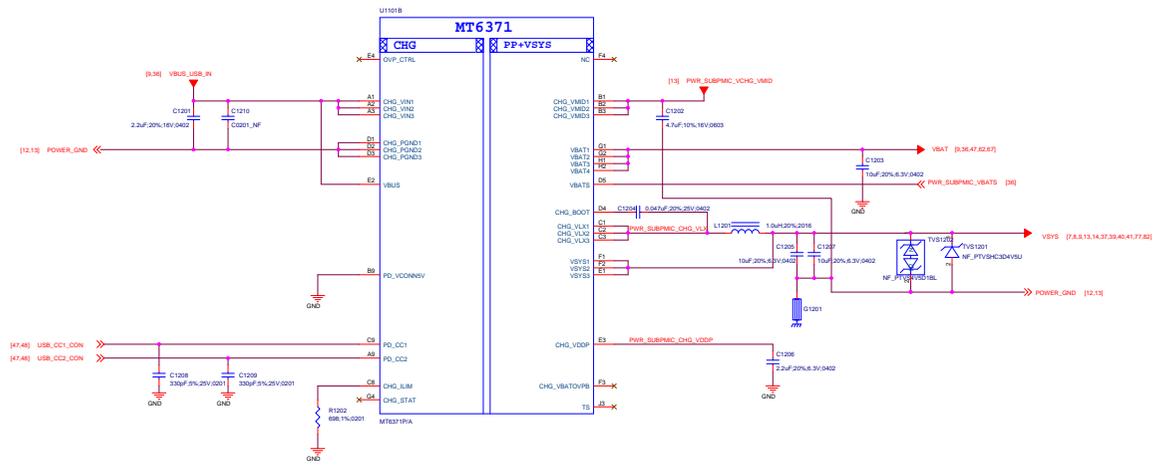
- Note 22-5: Please connect to battery connector



- AU_HPL and AU_HPR should be routed as single end signal, and be guarded by GND, up and down, left and right respectively
 - The suggested layout pattern of AU_HPL/ AU_HPR/ AU_REFN is " GND AU_HPL AU_REFN AU_HPR GND"



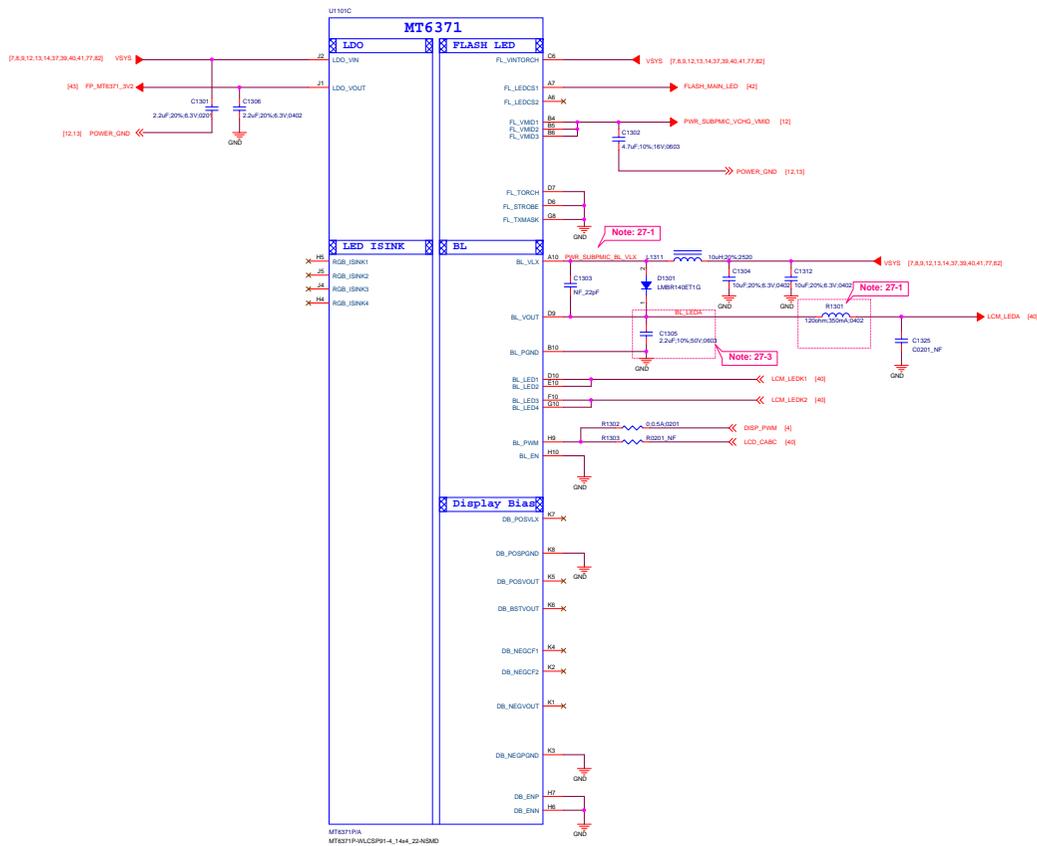
1114	11_POWER_SubPMIC-General	REV: V10
DOCUMENT NO.:	Design Name	Size: D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
Date:	Tuesday, December 17, 2019	Sheet 11 of 83



Schematic design notice of "26_POWER_SubPMIC-Charger + PP" page.

Note 26-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

F111+12_POWER_SubPMIC-Charger + PP		REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
WINGTECH		
Date:	Tuesday, December 17, 2019	Sheet 12 of 82



Schematic design notice of "27_POWER_SubPMIC-HV powers" page:

Note 27-1: To minimize RF de-sense, it is recommended to reserve 0-ohm and 0402 cap for BOM fine tuning.

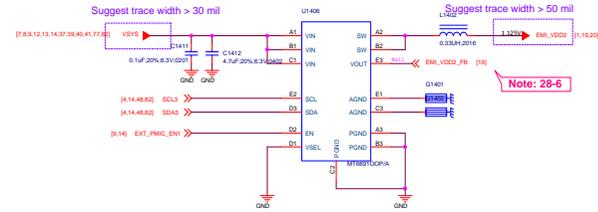
Note 27-2: To minimize RF de-sense, it is recommended to reserve 0-ohm and 0201 cap. for BOM fine tuning.

Note 27-3: C2705 could be replaced with C / 1 / uF / 50V + C / 1 / uF / 50V

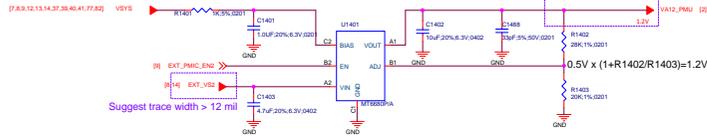
1114 13_POWER_SubPMIC-HV powers		REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT: WINGTECHSH	DESIGNER: YL	
Date: Tuesday, December 17, 2019		Sheet 13 of 53

Ext. buck LPDDR4X/LPDDR4 VDRAM Note: 28-4

MT6691OOP/A / Ext. buck LP4X/LP4 VDRAM (VDD2)
I2C address: 0x57 (Write:0xA8, Read:0xAF)

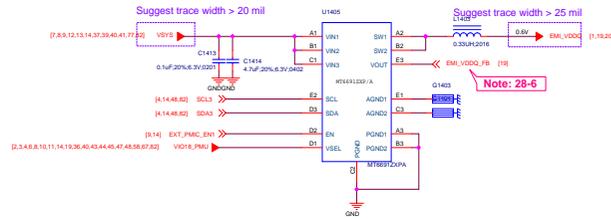


LDO for VA12 Note: 28-1

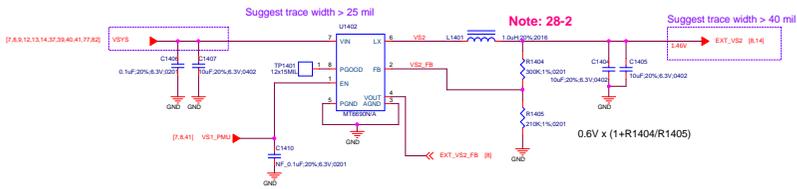


Ext. buck LPDDR4X VDDQ Note: 28-4

MT6691ZXP/A / Ext. buck LP4X VDRAM (VDDQ)
I2C address: 0x50 (Write:0xA0, Read:0xA1)

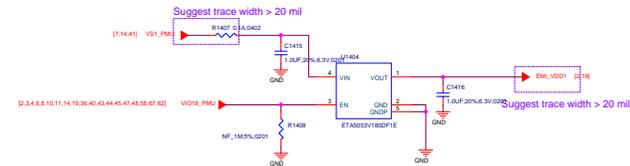


Ext. Buck for VS2



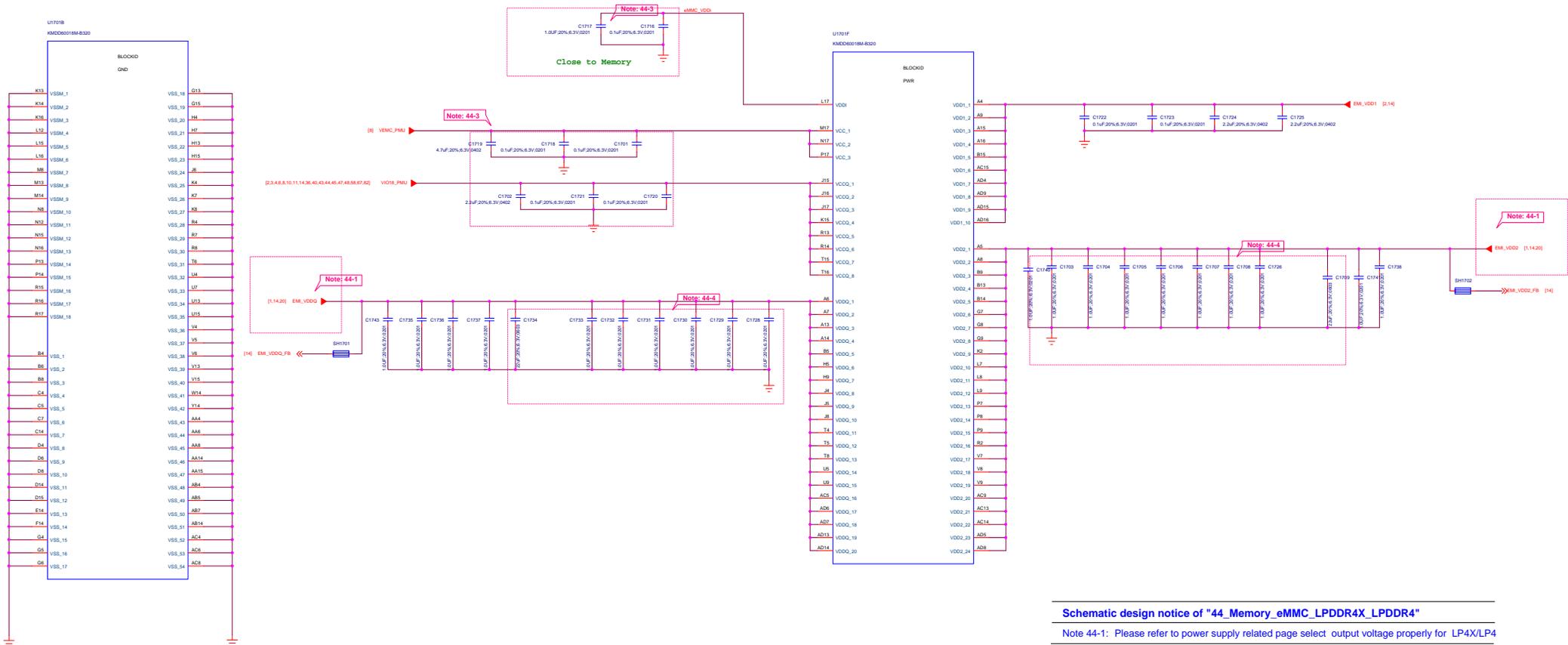
NOTE: Do not use VCAMD 1.3/1.5/1.8 when VS2 BUCK applied

LPDDR4X/LPDDR4 VDD1 1.8V LDO Note: 28-5



Schematic design notice of "28_POWER_ThirdParty-Power"

- Note 28-1: VA12 Layout placement please close to AP
- Note 28-2: VS2 Buck Layout placement please close to PMIC MT6357
- Note 28-3: VCN33 LDO Layout placement please close to MT6631
- Note 28-4: 1.MT6691OOP/A Buck Layout Placement please close to LP4X/LP4
2.MT6691ZXP/A Buck Layout Placement please close to LP4X
3.If DRAM Application is LPDDR4 , MT6691ZXP/A NC
- Note 28-5: U2810 LDO Layout Placement Please close to LPDDR4X/LPDDR4 VDD1 power ball
- Note 28-6: For EMI_VDD2_FB and EMI_VDDQ_FB, please follow MMD rule



Schematic design notice of "44_Memory_eMMC_LPDDR4X_LPDDR4"

Note 44-1: Please refer to power supply related page select output voltage properly for LP4X/LP4

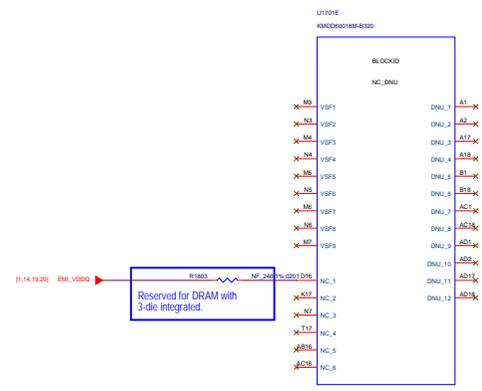
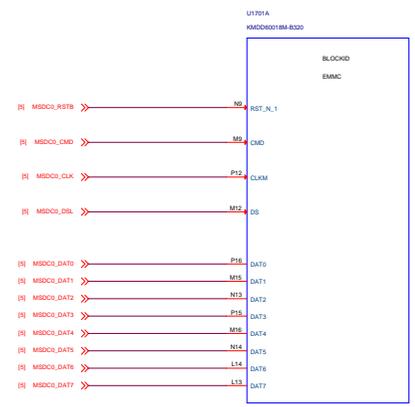
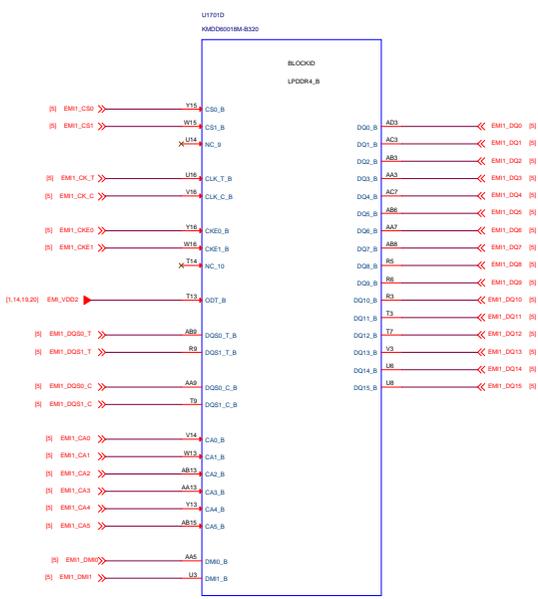
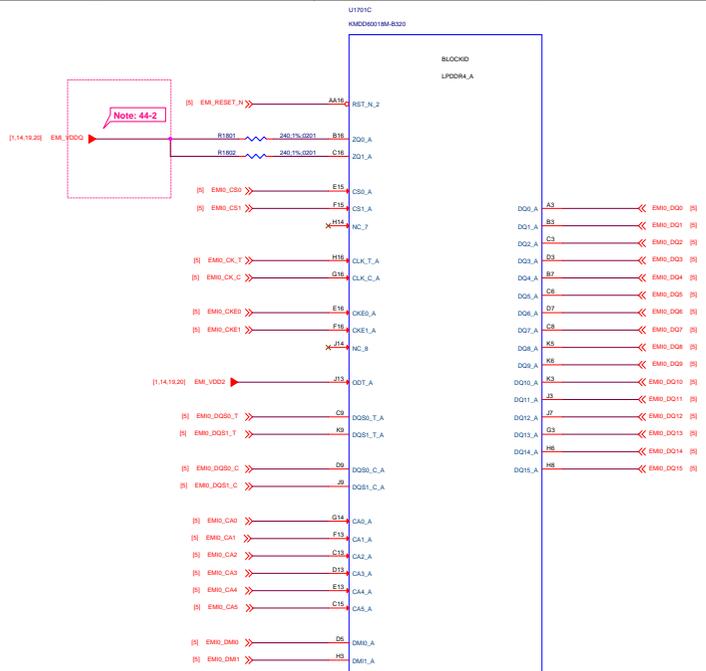
Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC (>10uF, at PMIC page);
please also refer to MMD and layout guide for placement.

Note 44-6: R4437/R4438 could be replaced with 0-ohm / 0402 * 3 for LP4 DRAM

File:	17_Memory_LPDDR4_POWER	REV:	V10
DOCUMENT NO.:	Design Home	Size:	D
DEPARTMENT:	WINTECH-SH	DESIGNER:	LIFENGLER
WINTECH			
Date:	Tuesday, December 17, 2019	Sheet:	19 of 65



Schematic design notice of "44_Memory_eMMC_LPDDR4_LPDDR4"

Note 44-1: Please refer to power supply related page select output voltage properly for LP4X/LP4

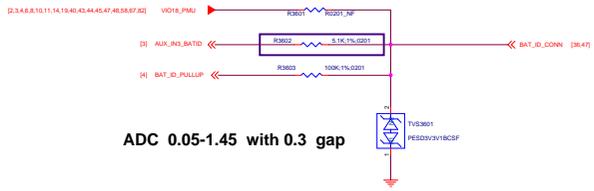
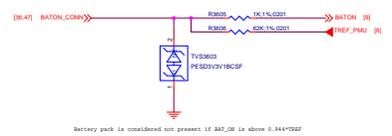
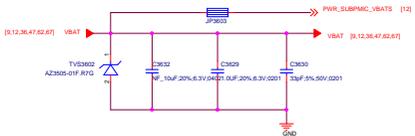
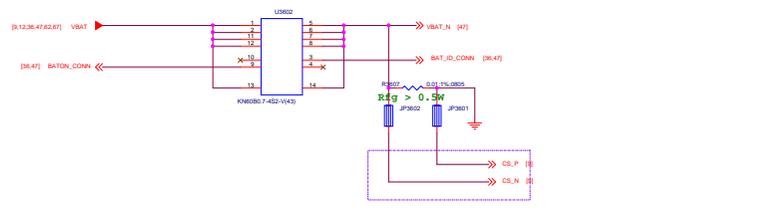
Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

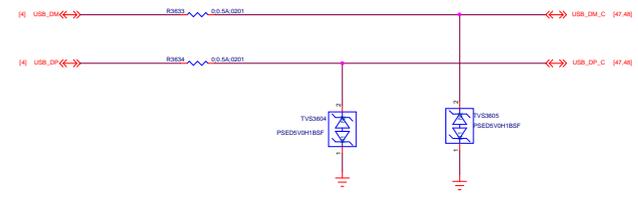
Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC (>10uF, at PMIC page); please also refer to MMD and layout guide for placement.

Note 44-6: R4437/R4438 could be replaced with 0-ohm / 0402 * 3 for LP4 DRAM

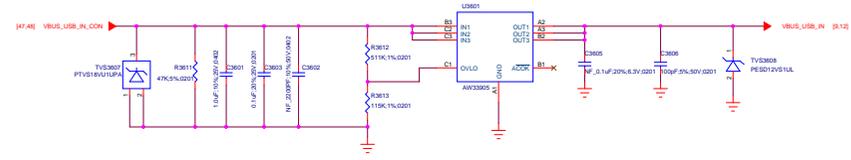
Battery Connector



USB DP/DM



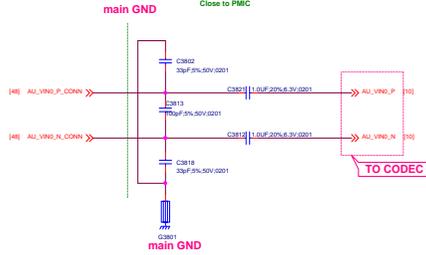
OVP_VBUS



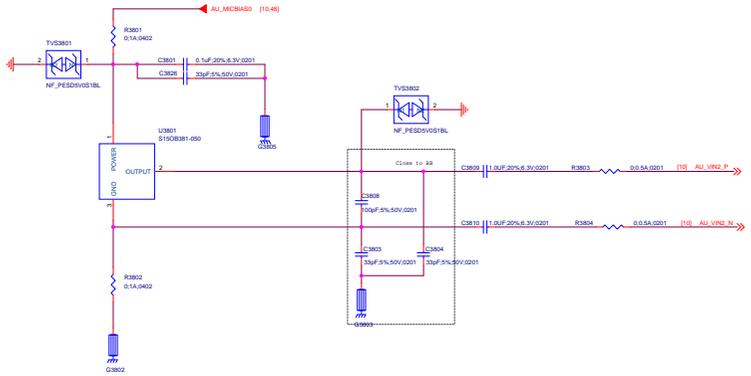
Surge VBUS: ±100V with Overvoltage Protection up to 29V
 DC
 $V_{ovp} = 6.5V$ when $R_{3612} = 511K$ $R_{3613} = 115K$
 $V_{ovp} = 1.2 * (1 + R_{3612} / R_{3613})$

111x	36_Battery/USB IF	REV: V10
DOCUMENT NO.: Design Name		Size D
DEPARTMENT: WINGTECH-SH	DESIGNER: YL	
Date: Tuesday, December 17, 2019	Sheet	36 of 53

MAIN MIC



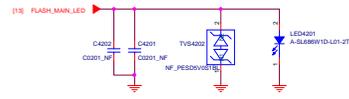
AUX MIC



MIC LABEL

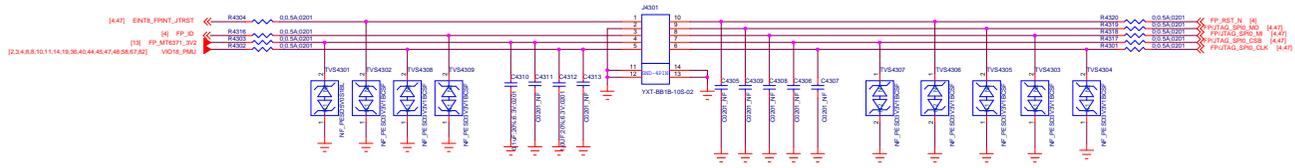


Title	38_MIC	REV:	V10
DOCUMENT NO.:	Design Name	Size	D
DEPARTMENT:	WINGTECH-SH	DESIGNER:	YL
Date:	Tuesday, December 17, 2019	Sheet	38 of 53



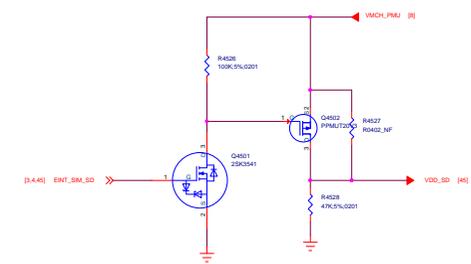
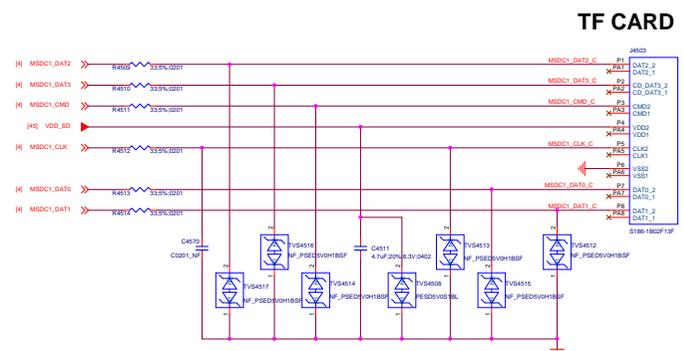
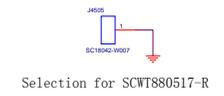
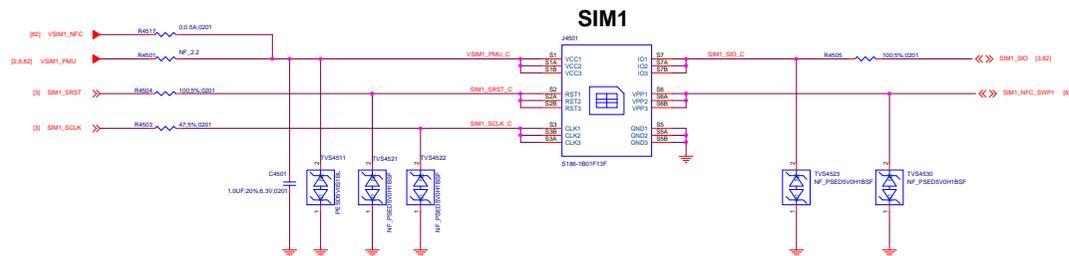
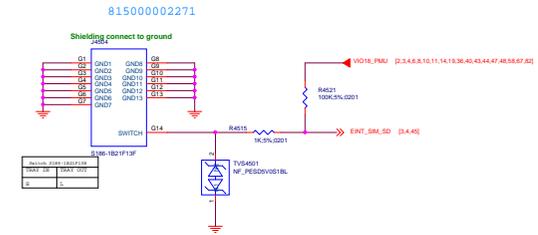
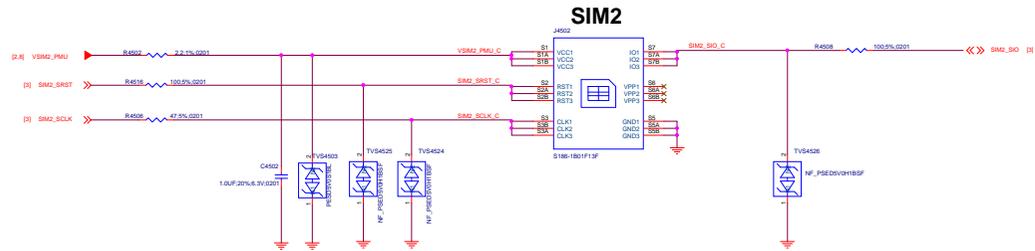
Title	42_FlashRGB	REV: V10
DOCUMENT NO.:	Design Name	Size: 0
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
WINGTECH		
Date:	Tuesday, December 17, 2019	Sheet: 42 of 83

Fingerprint



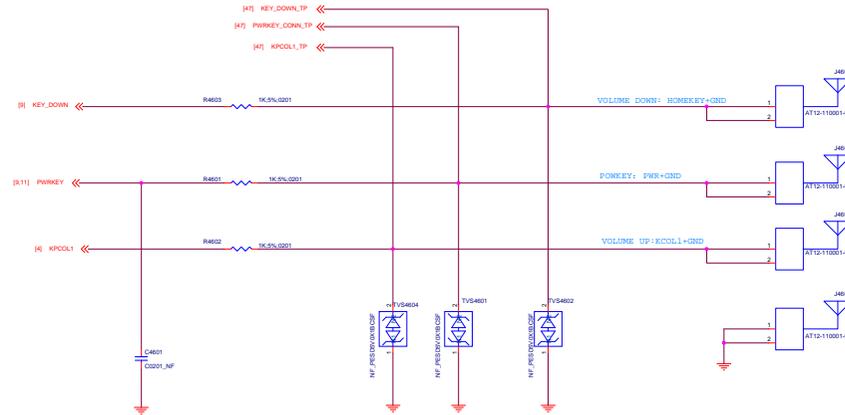
Fingerprint

1114	43.Fingerprint	REV: V10
DOCUMENT NO.:	Design Name	Size D
DEPARTMENT:	WINGTECH-SH	DESIGNER: YL
		
Date:	Tuesday, December 17, 2019	Sheet 43 of 43

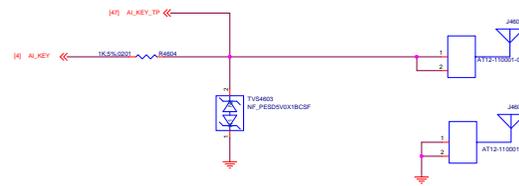


Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY



AI KEY

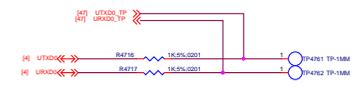
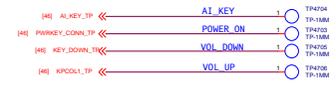
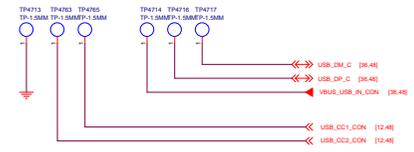
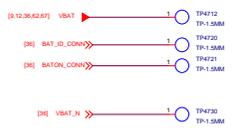


BATTERY

USB

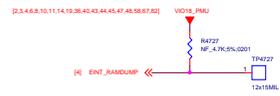
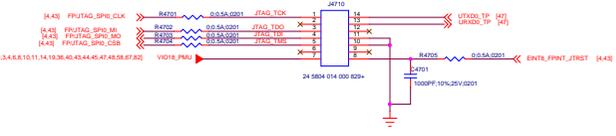
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UART

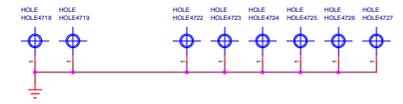


JTAG

HOLE



PTH



NPTH

4720 4721

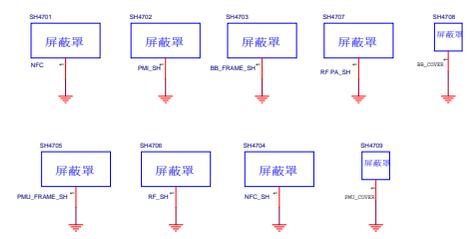
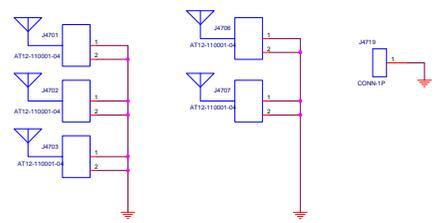
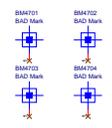
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Waterproof

SN Label

GND SHRAPNEL

SHIELDING

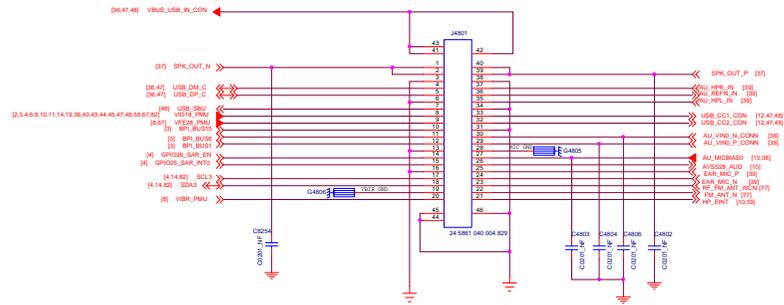


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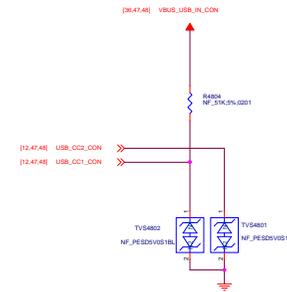
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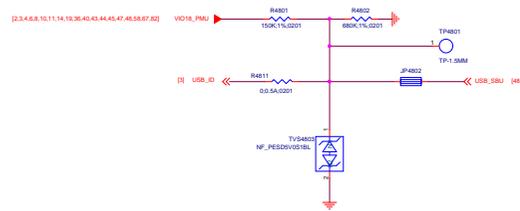
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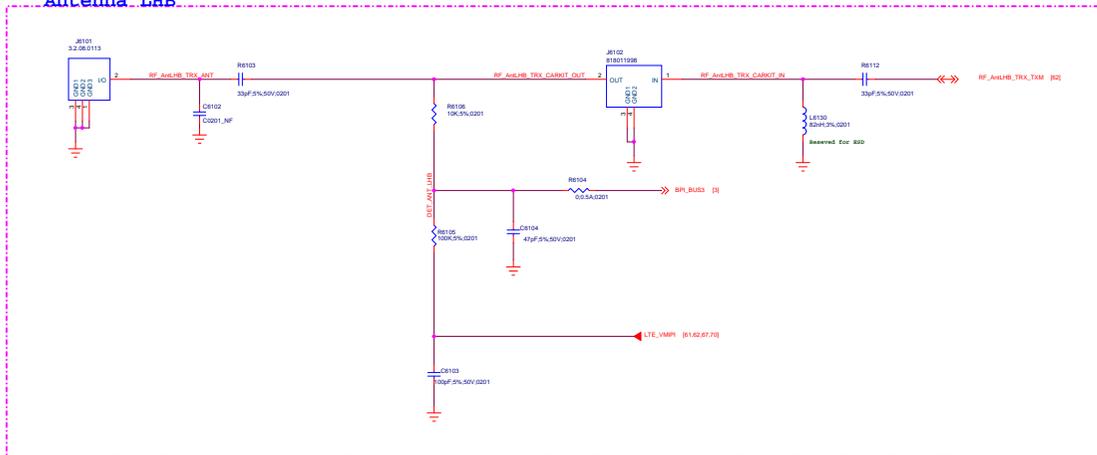
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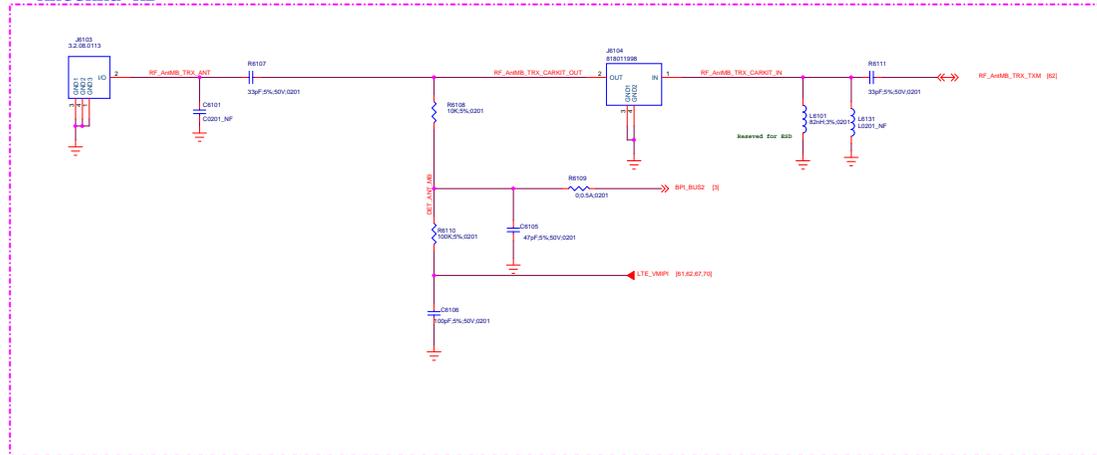
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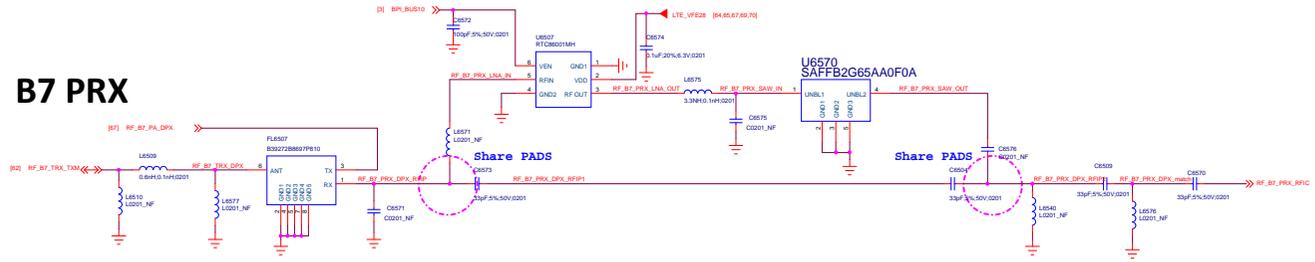
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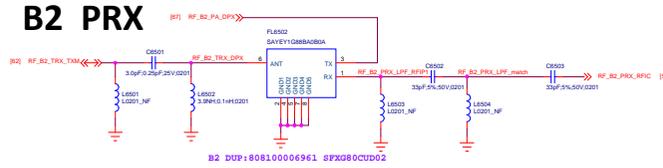
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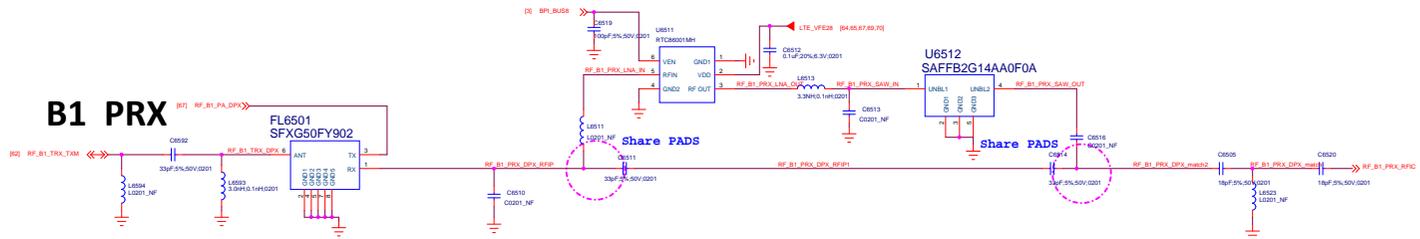
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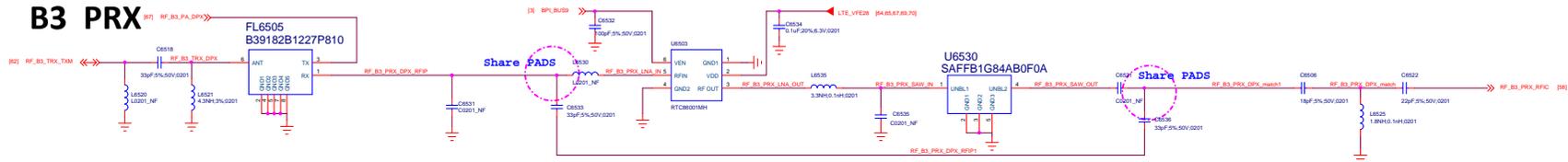
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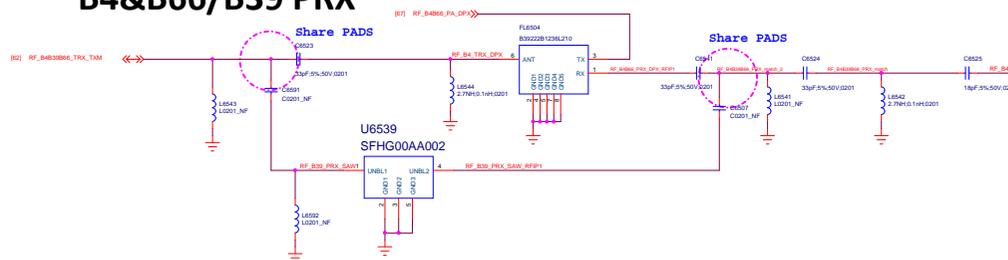
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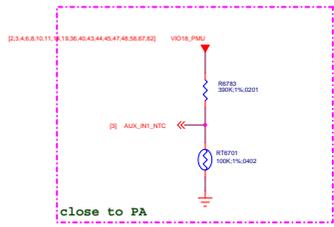


B3 PRX

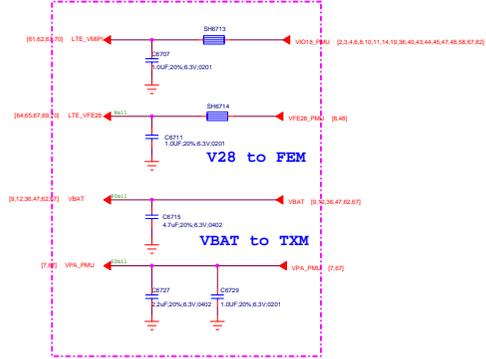


B4&B66/B39 PRX





Power Net Connection



B28A TX

B2 TX

B4 TX/B66 TX

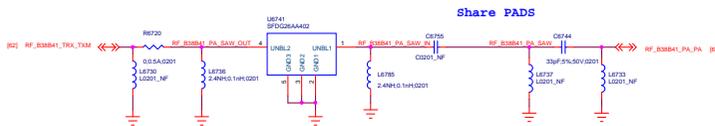
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B3 TX

B40 TRX

B38TRX



B7 TX

B38/40 PRX

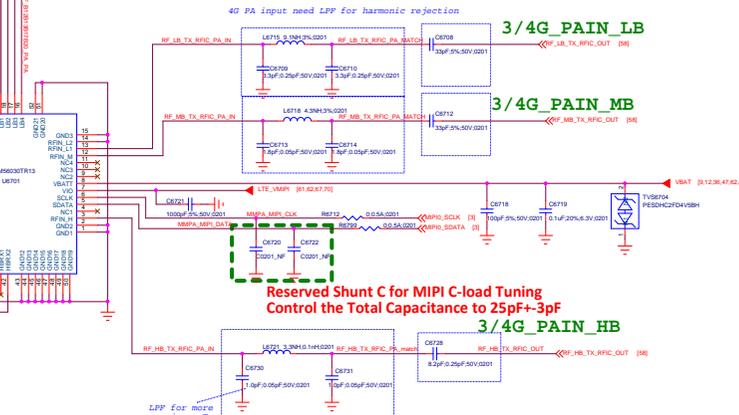
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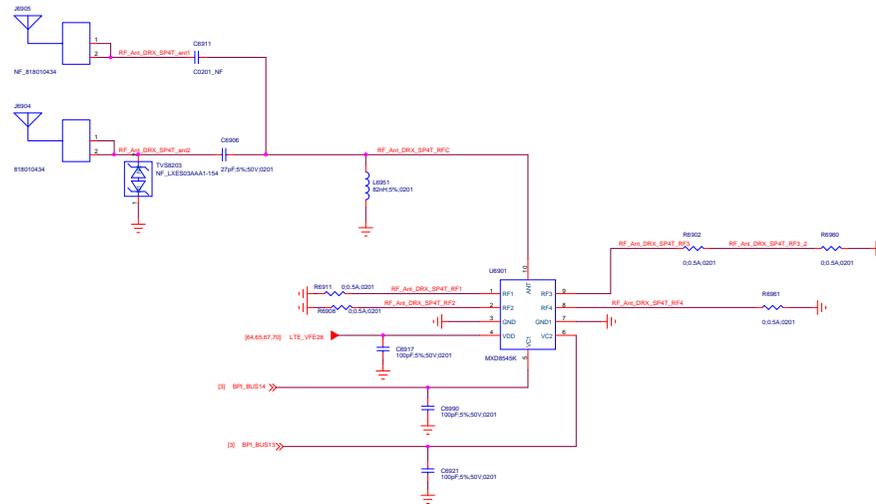
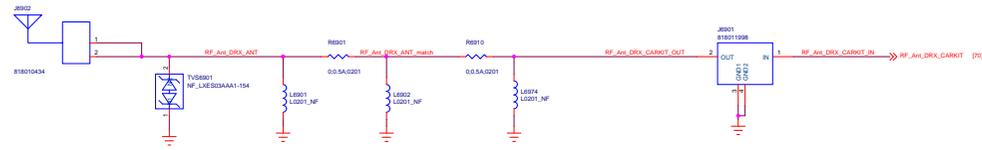
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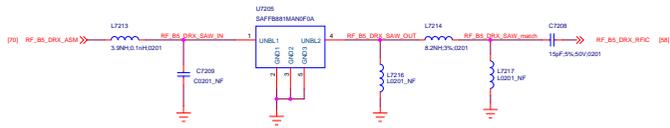
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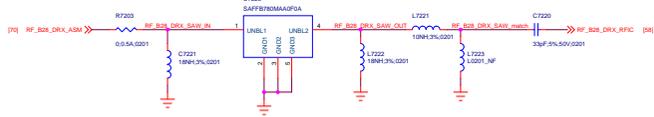
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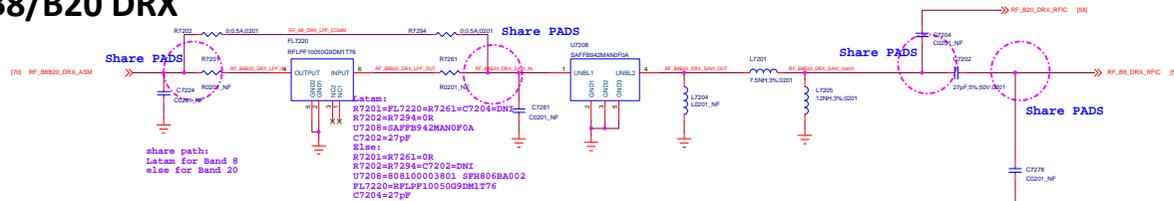
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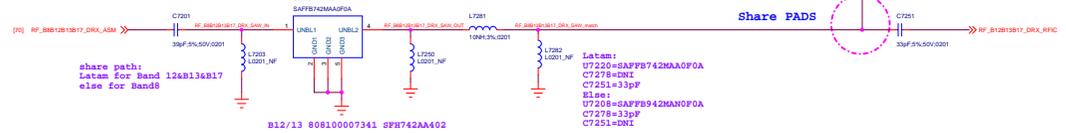
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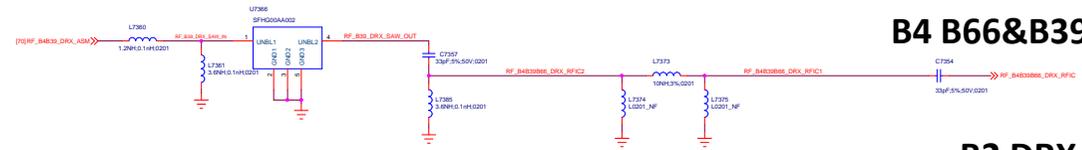
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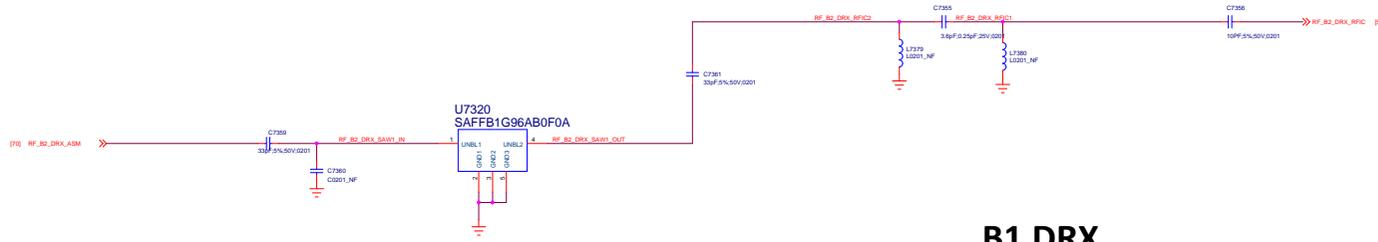
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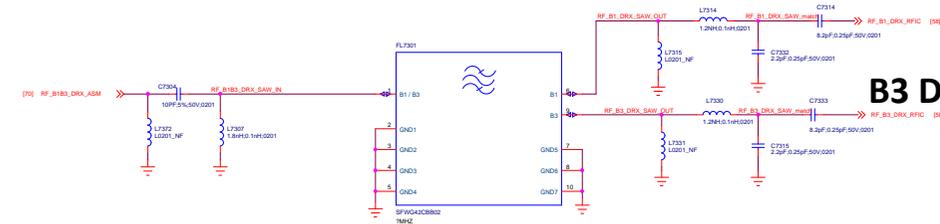
B4 B66&B39 DRX



B2 DRX



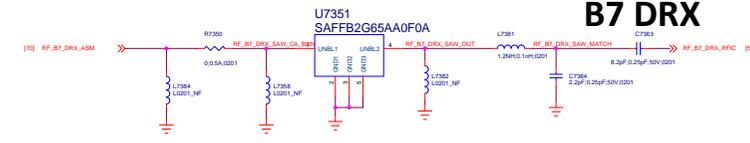
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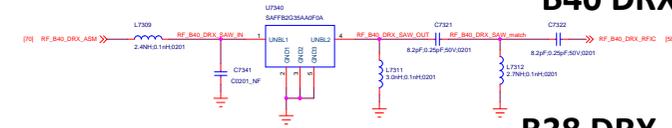
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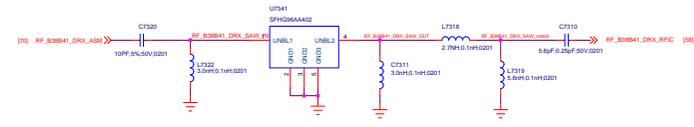
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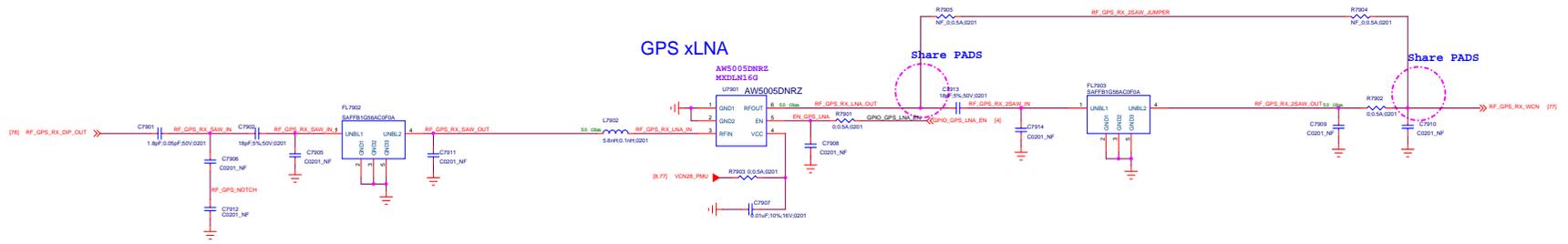


B40 DRX



B38 DRX





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