PERFECT WIRELESS EXPERIENCE

SC126

Hardware Guide

V1.2

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Contact

Website: https://www.fibocom.com

Address: Floor 10-14, Block A, Building 6, Shenzhen International Innovation Valley, Dashiyi Road, Xili Community, Xili Street, Nanshan District, Shenzhen

Tel: 0755-26733555

Safety Instruction

Do not operate wireless communication products in areas where use of radio is not recommended without proper equipment certification. These areas include environments where radio interference may occur, such as flammable and explosive environments, and medical equipment, aircraft, or any other equipment that may be subject to any form of radio interference.

Any driver or operator of a vehicle must not operate a wireless communication product while controlling the vehicle. Doing so will reduce the driver's control and operation of the vehicle, posing a safety risk.

The wireless communication product does not guarantee a valid connection under any circumstances, for example, when the (U)SIM is in arrears or invalid. In case of emergency, use the emergency call function in power-on state, and make sure the equipment is in an area with sufficient signal strength.

Contents

Applicable Models

No.	Applicability Model	Description
1	SC126-NA-10	16GB e.MMC+16Gb LPDDR4X.SDRAM, 4G frequency band, Android 12, applicable in North America
2	SC126-EAU-10	16GB e.MMC+16Gb LPDDR4X.SDRAM, 4G frequency band, Android 12, applicable in Europe
3	SC126-CN-10	16GB e.MMC+16Gb LPDDR4X.SDRAM, 4G frequency band, Android 12, applicable in China

Change History

V1.2 （2022-07-30）	Added CN RF parameters
V1.1 (2022-06-13)	Revised some description errors and added EAU RF parameters.
V1.0 (2022-04-06)	Initial version

1 Foreword

1.1 Description

This document describes the electrical characteristics, RF performance, structure size, application environment, etc. of SC126 series module (hereinafter referred to as module). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of the module and develop products.

1.2 Reference Standards

This product is designed with reference to the following standards:

- 3GPP TS 51.010-1 V10.5.0: Mobile Station (MS) conformance specification; Part 1: Conformance specification
- 3GPP TS 34.121-1 V10.8.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V10.1.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V10.6.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit(USAT)

- 3GPP TS 36.124V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)
- 3GPPTS27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- IEEE 802.11n WLAN MAC and PHY, October 2009 + IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- IEEE Std 802.11b, IEEE Std 802.11a, IEEE Std 802.11g, IEEE Std 802.11n, IEEE Std 802.11ac, IEEE Std 802.11ax;
- IEEE 802.11-2007 WLAN MAC and PHY, June 2007
- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 +HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.2.0, November 7, 2014
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.0.2, December 07,2017
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/5.1.0, December 07,2018

2 Product Overview

2.1 General Description

The module integrates core components such as Baseband, eMCP, PMU, Transceiver, PA; it supports long distance multi-mode communication such as FDD/TDD-LTE, WCDMA, GSM and WIFI/BT short-distance radio transmission technology, as well as GNSS wireless positioning technology. The module is embedded with Android operating system and supports various interfaces such as MIPI/USB/UART/SPI/I^{2}C. It is the optimal solution for the core system of wireless smart products. Its corresponding network modes and frequency bands are as follows:

Table 1. SC126-NA supported bands

Mode	Band
FDD-LTE	Band 2/4/5/7/12/13/17/25/26/66/71
TDD-LTE	Band 41 (2496-2690MHz)
WIFI802.11a/b/g/n/ac	2402-2482MHz; 5170-5835MHz
BT5.0	2402-2480MHz
GNSS	GPS/GLONASS/BeiDou

Table 2. SC126-EAU supported bands

Mode	Band
GSM	GSM850/EGSM900/DCS1800/PCS1900
WCDMA	Band 1/2/3/5/8
FDD-LTE	Band 1/2/3/4/5/7/8/20/28
TDD-LTE	Band 38/40/41 (2496-2690MHz)
WIFI802.11a/b/g/n/ac	2402-2482MHz; 5170-5835MHz

Mode	Band
BT5.0	2402-2480MHz
GNSS	GPS/GLONASS/BeiDou

Table 3. SC126-CN supported bands

Mode	Band
GSM	EGSM900/DCS1800
WCDMA	Band 1/8
FDD-LTE	Band 1/3/5/8
TDD-LTE	Band 34/39/38/40/41(2496-2690MHz)
WIFI802.11a/b/g/n/ac	2402-2482MHz;5170-5835MHz
BT5.0	2402-2480MHz
GNSS	GPS/GLONASS/BeiDou

2.2 Main Performance

The module is available in LCC + LGA package with 262 pins, including 146 LCC pins and 116 LGA pins. The dimension is 40.5 (±0.15)mm × 40.5 (±0.15)mm × 2.55 (±0.2)mm. It can be embedded in various M2M applications. It is suitable for the development of smart devices such as smart POS, cash registers, robots, UAVs, smart homes, security monitoring, multimedia terminals, ECR, and face payment terminals. The following table describes the detailed performance.

Table 4. Performance specifications

Performance	Description
Power Supply	DC: 3.5-4.4V, typical voltage: 3.8V
Application	ARM® Cortex-A53 Quad-core 64-bit CPU up to 2.0GHz

Performance	Description
processor	
Memory	16Gb LPDDR4X+16GB eMMC Flash[1)]
Power class	Class 4 (33dBm ±2dB) for GSM850/EGSM900 Class 1 (30dBm ±2dB) for DCS1800/PCS1900 Class E2 (27dBm±3dB) for GSM850/EGSM900 8-PSK Class E2 (26dBm±3dB) for DCS1800/PCS1900 8-PSK Class 3 (24dBm+1/-3dB) for WCDMA bands Class 3 (23dBm ±2dB) for LTE FDD bands Class 3 (23dBm ±2dB) for LTE TDD bands
GSM/GPRS/EDGE features	R99: CSD transmission rate: 9.6kbps, 14.4kbps GPRS: Support GPRS multi-slot class 33 Coding formats: CS-1/CS-2/CS-3 and CS-4 Up to 5 Rx time slots per frame EDGE: Support EDGE multi-slot class 33 Support GMSK and 8-PSK Uplink encoding format: CS 1-4 and MCS 1-9 Downlink encoding format: CS 1-4 and MCS 1-9
WCDMA features	Support 3GPP R8 DC-HSPA+ Support 16-QAM, 64-QAM and QPSK modulation CAT7 HSUPA: maximum uplink rate 5.76Mbps CAT14 HSDPA: maximum downlink rate 42Mbps

Performance	Description
LTE features	Support FDD/TDD R10 Support FDD/TDD CAT4 Support 1.4-20M RF bandwidth Downlink support 2 × 2 MIMO Maximum uplink rate 50Mbps, maximum downlink rate 150Mbps
WLAN features	Support 2.4G and 5G WLAN wireless communication, support 802.11a, 802.11b, 802.11g, 802.11n and 802.11ac, the maximum rate is up to 433Mbps
Bluetooth features	BT5.0 (BR/EDR + BLE)
Satellite positioning	GPS/GLONASS/BeiDou
LCD Interface	4-Lane MIPI_DSI interface Support for 1080P maximally
Camera interface	Two 4-Lane MIPI_CSI interfaces, which can be configured as 4+4 Lanes or 4+2+1 Lanes ISPx2 (13MP+13MP or 25MP)
Audio interface	Input: 3 analog MIC inputs Output: Stereo headphone output Differential receiver output Differential Lineout output, which requires an external audio PA
USB interface	One USB 3.1 interface that is downward compatible with USB 2.0 interface USB 3.1 interface supports the SS (5 Gbps) mode but does not support software download. USB 2.0 interface supports the HS (480 Mbps) mode and software download, and is downward compatible with FS and LS interface. USB supports the OTG function and HUB extensible interface supports USB OTG.

Performance	Description
(U)SIM interface	Two (U)SIM card interfaces, support (U)SIM card: 1.8/3V adaptive Support dual-SIM dual-standby and hot plugging
UART interface	Three UART serial interfaces, with the maximum rate up to 4Mbps One 4-line serial interface, supports hardware flow control One 2-line serial interface One 2-lane debug serial interface
SDIO Interface	Support SD3.0 and 4-bit SDIO; SD card supports hot plugging
I²C interface	4 sets of I²C interfaces for TP, camera, sensor, etc.
ADC Interfaces	One general ADC
RTC	Support
Antenna Interface	MAIN antenna, DRX antenna, GNSS antenna, WIFI/BT antenna
Physical characteristics	Dimensions: 40.5 (±0.15)mm × 40.5 (±0.15)mm × 2.55 (±0.2)mm Packaging: 146 LCC pins +116 LGA pins Weight: ~9.7 g
Temperature range	Operating temperature: -30°C to 75°C[2)] Storage temperature: -40°C to -85°C
Software update	USB/OTA/SD
RoHS	RoHS compliant

1) The storage capacity varies according to the actual model.
2) When the module is operating within this temperature range, the functions of it are normal and the relevant performance meets the 3GPP standard.

2.3 Function Block Diagram

Function block diagram shows the main hardware features of the module, including:

- Baseband
- Wireless transceiver
- Power Management
- Memory
- Peripheral interface
  - Communication expansion interface (USB/UART/I²C/SD)
  - (U)SIM card interface
  - MIPIDSI interface
  - MIPICSI interface
  - Analog audio interface

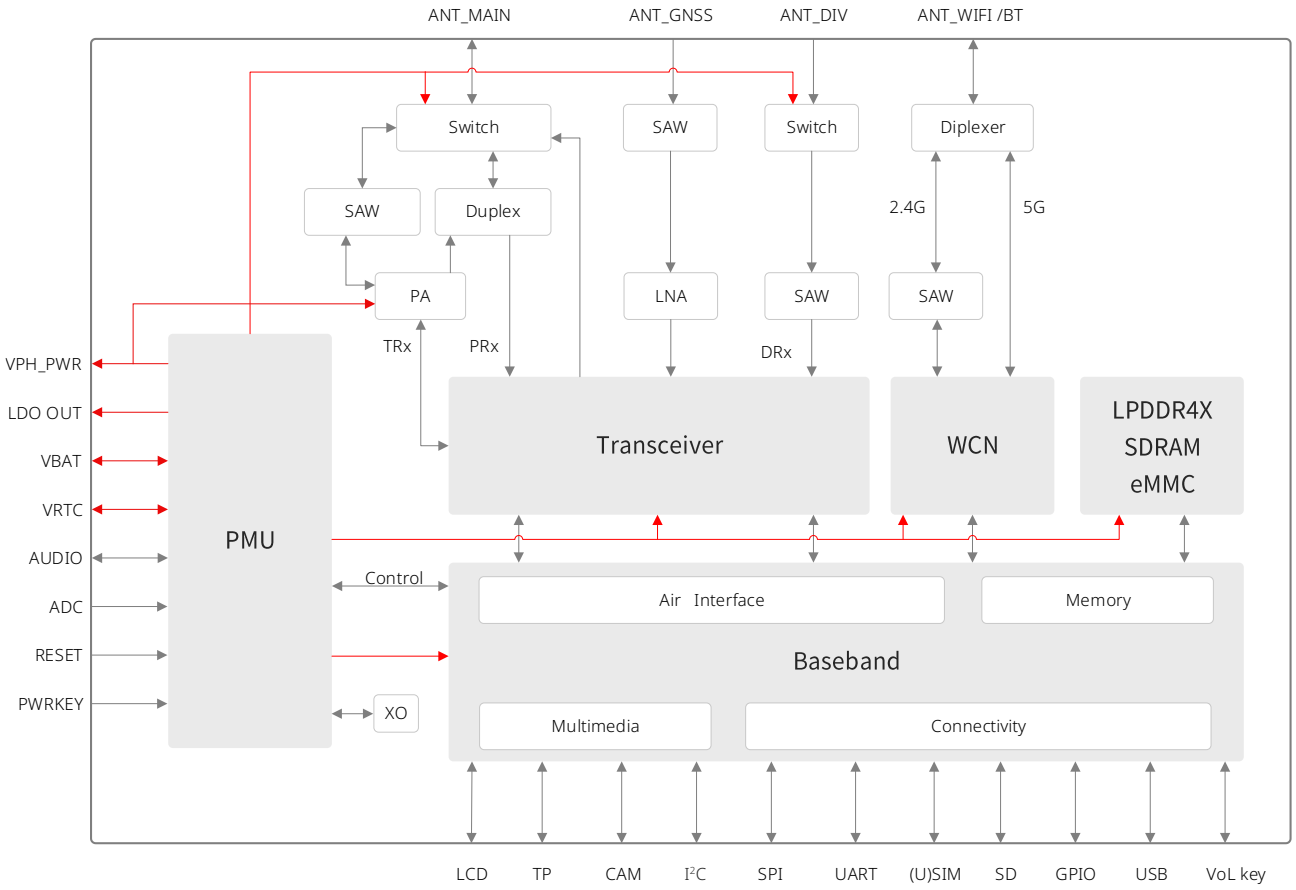

Figure 1. Function block diagram

2.4 Pin Definition

2.4.1 Pin Distribution

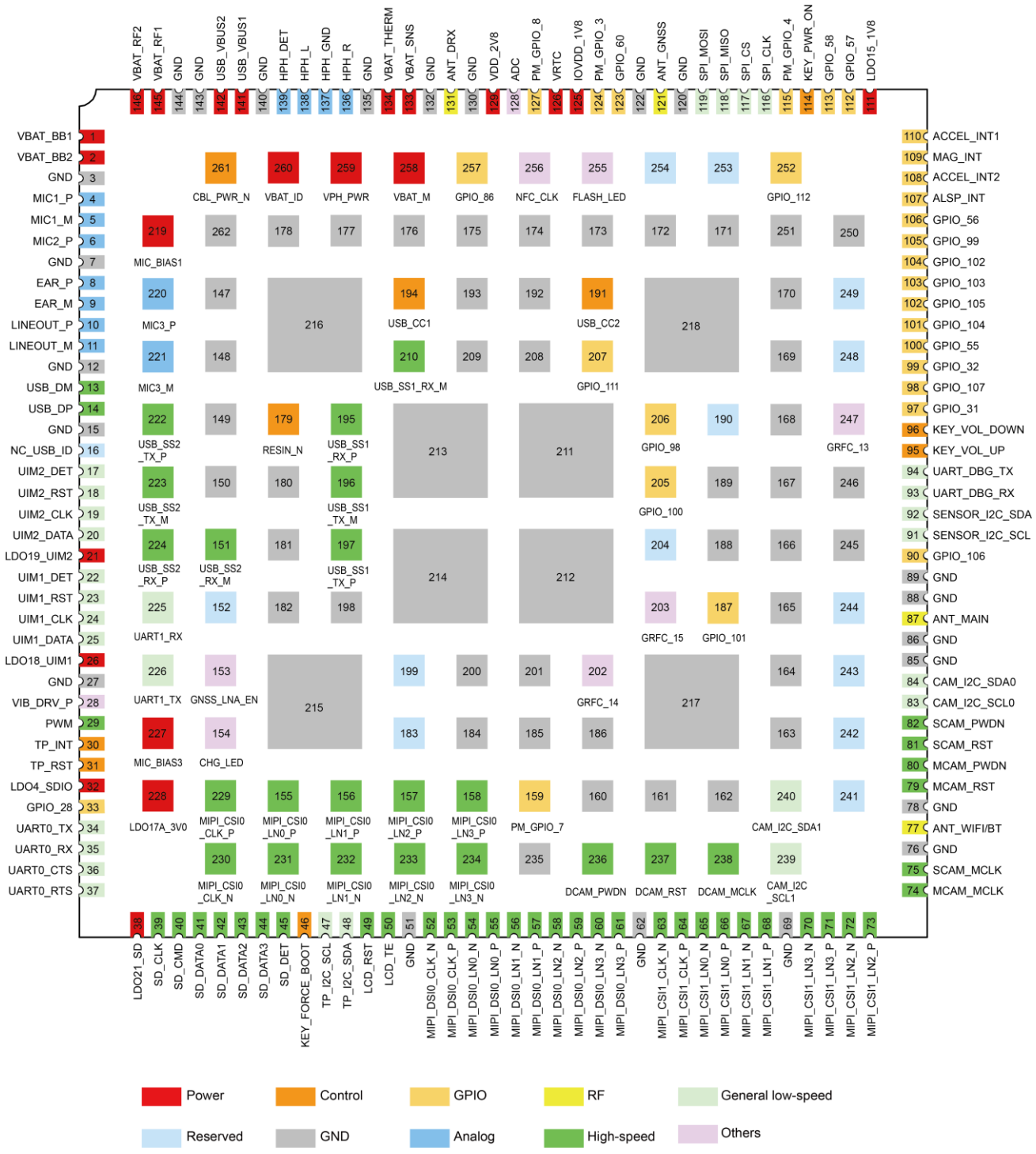

Figure 2. Pin distribution

"NC" indicates No Connect, and the pin for this position is reserved and does not need to be connected.

2.4.2 Pin Description

Table 5. I/O parameters description

Type	Description
I/O	Input/Output
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output
OD	Open drain

Module pins are described in the following table:

Table 6. Description of module pins

Pin Name	Pin No.	I/O	Pin Description	Remarks
Power interface				
VBAT	1, 2, 145, 146	PI	Main power supply	--
VRTC	126	PI/PO	RTC power supply	--
VDD_2V8	129	PO	2.8V voltage output	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
LDO15_1V8	111	PO	LDO L15 1.8V power output	--
VPH_PWR	259	PO	General-purpose peripheral power output	--
LDO19_UIM2	21	PO	UIM2 card power supply	--
LDO18_UIM1	26	PO	UIM1 card power supply	--
IOVDD_1V8	125	PO	LDO 1.8V power output	--
LDO17A_3V0	228	PO	LDO L17 3.0V power output	--
LDO4_SDIO	32	PO	LDO L4 SD pull-up power output	--
LDO21_SD	38	PO	LDO L21 2.9V SD card power output	--
Motor interface				
VIB_DRV_P	28	PO	Motor driver pin	- -
Ground				
GND	3, 7, 12, 15, 27, 51, 62, 69, 76, 78, 85, 86, 88, 89, 120, 122, 130, 132, 135, 140, 143, 144, 147, 148, 149, 150, 160, 161, 162, 163, 164, 165, 166, 167, 168, 169, 170, 171, 172, 173, 174, 175, 176, 177, 178, 180, 181, 182, 184, 185, 186, 188, 189, 192, 193, 198, 200, 201, 208, 209, 211, 212, 213, 214, 215, 216, 217, 218, 235, 245, 246, 250, 251, 262			74
Battery Supply Interface				
VBAT_SNS	133	AI	Battery positive detection	Connected to the positive pole of the battery.
VBAT_M	258	AI	Battery negative detection	Connected to the

Pin Name	Pin No.	I/O	Pin Description	Remarks
				negative pole of the battery. Keep the unused pins unconnected.
VBAT_THERM	134	AI	Battery temperature detection	Connect the pin to GND with 47KΩ resistor if the pin is unused
VBAT_ID	260	AI	Battery ID pin	Connect the pin to GND with 100KΩ resistor if the pin is unused
Button				
KEY_FORCE_BOOT	46	DI	Force download key	Active high
KEY_VOL_UP	95	DI	Volume +	Active low
KEY_VOL_DOWN	96	DI	Volume -	Active low
KEY_PWR_ON	114	DI	Power key	Active low
RESIN_N	179	DI	Reset key	Active low
CBL_PWR_N	261	DI	Auto power-on pin	Active low
(U)SIM card interface				
UIM2_DET	17	DI	UIM2 hot plugging detection	Active high by default
UIM2_RST	18	DO	UIM2 reset signal	--
UIM2_CLK	19	DO	UIM2 clock signal	--
UIM2_DATA	20	DI/DO	UIM2 data signal	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
UIM1_DET	22	DI	UIM1 hot plugging detection	Active high by default
UIM1_RST	23	DO	UIM1 reset signal	--
UIM1_CLK	24	DO	UIM1 clock signal	--
UIM1_DATA	25	DI/DO	UIM1 data signal	--
SD card interface				
SD_DET	45	DI	SD card detection	Active low by default
SD_DATA3	44	DI/DO	SD card data bit 3	--
SD_DATA2	43	DI/DO	SD card data bit 2	--
SD_DATA1	42	DI/DO	SD card data bit 1	--
SD_DATA0	41	DI/DO	SD card data bit 0	--
SD_CMD	40	DI/DO	SD card command interface	--
SD_CLK	39	DO	SD card clock	--
I^2C interface				
TP_I2C_SCL	47	DO	TP I^2C clock signal	Dedicated for TP
TP_I2C_SDA	48/183	DI/DO	TP I^2C data signal	
CAM_I2C_SCL0	83	DO	CAM0 I^2C clock signal	For camera only
CAM_I2C_SDA0	84	DI/DO	CAM0 I^2C data signal	
CAM_I2C_SCL1	239	DO	CAM1/2 I^2C clock signal	For camera only
CAM_I2C_SDA1	240	DI/DO	CAM1/2 I^2C data signal	
SENSOR_I2C_SCL	91	DO	Sensor I^2C clock	For sensor only
SENSOR_I2C_SDA	92	DI/DO	Sensor I^2C data	

Pin Name	Pin No.	I/O	Pin Description	Remarks
USB interface				
USB_VBUS	141, 142	PI	USB 5V power supply	--
USB_DM	13	AI/AO	USB 2.0 differential data signal-	--
USB_DP	14	AI/AO	USB 2.0 differential data signal+	--
USB_SS1_RX_M	210	AI	USB 3.1 differential data receiving-	--
USB_SS1_RX_P	195	AI	USB 3.1 differential data receiving+	
USB_SS1_TX_M	196	AO	USB 3.1 differential data sending-	
USB_SS1_TX_P	197	AO	USB 3.1 differential data sending+	
USB_SS2_RX_M	151	AI	USB 3.1 differential data receiving-	
USB_SS2_RX_P	224	AI	USB 3.1 differential data receiving+	
USB_SS2_TX_M	223	AO	USB 3.1 differential data sending-	
USB_SS2_TX_P	222	AO	USB 3.1 differential data sending+	
USB_CC1	194	AI/AO	USB_CC1	
USB_CC2	191	AI/AO	USB_CC2	

Pin Name	Pin No.	I/O	Pin Description	Remarks
UART interface				
UART0_TX	34	DO	UART0 serial interface data sending signal	--
UART0_RX	35	DI	UART0 serial interface data receiving signal	--
UART0_CTS	36	DI	UART0 serial interface CTS signal	--
UART0_RTS	37	DO	UART0 serial interface RTS signal	--
UART_DBG_RX	93	DI	Debugging serial interface UART_RX	--
UART_DBG_TX	94	DO	Debugging serial interface UART_TX	--
UART1_RX	225	DI	Serial interface UART1_RX	--
UART1_TX	226	DO	Serial interface UART1_TX	--
SPI Interface				
SPI_CLK	116	DO	SPI clock	--
SPI_CS	117	DO	SPI chip select	--
SPI_MISO	118, 253	DI	SPI Master In Slave Out	--
SPI_MOSI	119, 254	DO	SPI Master output Slave input	--
LCD Interface				
MIPI_DSI0_CLK_N	52	AO	LCD MIPI-DSI signal	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
MIPI_DSI0_CLK_P	53	AO		--
MIPI_DSI0_LN0_N	54	AO		--
MIPI_DSI0_LN0_P	55	AO		--
MIPI_DSI0_LN1_N	56	AO		--
MIPI_DSI0_LN1_P	57	AO		--
MIPI_DSI0_LN2_N	58	AO		--
MIPI_DSI0_LN2_P	59	AO		--
MIPI_DSI0_LN3_N	60	AO		--
MIPI_DSI0_LN3_P	61	AO		--
PWM	29	DO	LCD backlight brightness PWM control	--
LCD_RST	49	DO	LCD reset signal	--
LCD_TE	50	DI	LCD swipe synchronization signal	--
TP Interface				
TP_INT	30	DI	TP interrupt	--
TP_RST	31	DO	TP reset signal	--
Camera interface				
MIPI_CSI0_CLK_P	229	AI	Camera MIPI-CSI0 interface. Keep the unused pins unconnected.	--
MIPI_CSI0_CLK_N	230	AI		--
MIPI_CSI0_LN0_N	231	AI		--
MIPI_CSI0_LN0_P	155	AI		--
MIPI_CSI0_LN1_N	232	AI		--

Pin Name	Pin No.	I/O	Pin Description	Remarks
MIPI_CSI0_LN1_P	156	AI		--
MIPI_CSI0_LN2_N	233	AI		--
MIPI_CSI0_LN2_P	157	AI		--
MIPI_CSI0_LN3_N	234	AI		--
MIPI_CSI0_LN3_P	158	AI		--
MIPI_CSI1_CLK_N	63	AI		--
MIPI_CSI1_CLK_P	64	AI		--
MIPI_CSI1_LN0_N	65	AI		--
MIPI_CSI1_LN0_P	66	AI		--
MIPI_CSI1_LN1_N	67	AI	Camera MIPI-CSI1 interface. Keep the unused pins unconnected.	--
MIPI_CSI1_LN1_P	68	AI		--
MIPI_CSI1_LN3_N	70	AI		--
MIPI_CSI1_LN3_P	71	AI		--
MIPI_CSI1_LN2_N	72	AI		--
MIPI_CSI1_LN2_P	73	AI		--
MCAM_MCLK	74	DO	Camera 1 clock signal	--
MCAM_RST	79	DO	Camera 1 reset signal	--
MCAM_PWDN	80	DO	Camera 1 shutdown signal	--
SCAM_MCLK	75	DO	Camera 2 clock signal	--
SCAM_RST	81	DO	Camera 2 reset signal	--
SCAM_PWDN	82	DO	Camera 2 shutdown signal	--
DCAM_PWDN	236	DO	Camera 3 shutdown signal	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
DCAM_RST	237	DO	Camera 3 reset signal	--
DCAM_MCLK	238	DO	Camera 3 clock signal	--
Audio interface				
MIC1_P	4	AI	Main MIC input+	--
MIC1_M	5	AI	Main MIC input-	--
MIC2_P	6	AI	Headphone MIC input+	--
MIC3_P	220	AI	Secondary MIC input+	--
MIC3_M	221	AI	Secondary MIC input-	--
EAR_P	8	AO	Receiver output+	--
EAR_M	9	AO	Receiver output-	--
LINEOUT_P	10	AO	Differential Lineout output+	It requires an external audio PA.
LINEOUT_M	11	AO	Differential Lineout output-	
HPH_R	136	AO	Headphone right channel output	--
HPH_GND	137	/	Headphone reference ground	It requires to be grounded.
HPH_L	138	AO	Headphone left channel output	--
HPH_DET	139	AI	Headphone plug detection	--
MIC_BIAS1	219	PO	Main MIC bias voltage 1	An external MIC bias circuit needs to be added for the module.
MIC_BIAS3	227	PO	Secondary MIC bias voltage 3	

Pin Name	Pin No.	I/O	Pin Description	Remarks
Antenna interface				
ANT_MAIN	87	AI/AO	Main antenna	--
ANT_DRX	131	AI	Diversity antenna	--
ANT_WIFI/BT	77	AI/AO	WIFI/BT Antenna	--
ANT_GNSS	121	AI	GNSS Antenna	--
GPIO Interface				
GPIO_28	33	DI/DO	Ordinary GPIO, 1.8V power domain	B-PD: nppukp
GPIO_31	97	DI/DO		B-PD: nppukp
GPIO_32	99	DI/DO		B-PD: nppukp
GPIO_55	100	DI/DO		B-PD:nppukp; used internally as bootconfig, which cannot be pulled up
GPIO_56	106	DI/DO		B-PD: nppukp
GPIO_57	112	DI/DO		B-PD:nppukp; used internally as bootconfig, which cannot be pulled up
GPIO_58	113	DI/DO		B-PD: nppukp
GPIO_60	123	DI/DO		B-PD:nppukp; used internally as bootconfig, which cannot be

Pin Name	Pin No.	I/O	Pin Description	Remarks
				pulled up
GPIO_86	257	DI/DO		B-PD: nppukp
GPIO_98	206	DI/DO		B-PD: nppukp
GPIO_99	105	DI/DO		B-PD: nppukp
GPIO_100	205	DI/DO		B-PD: nppukp
GPIO_101	187	DI/DO		B-PD: nppukp
GPIO_102	104	DI/DO		B-PD: nppukp
GPIO_103	103	DI/DO		B-PD: nppukp
GPIO_104	101	DI/DO		B-PD: nppukp
GPIO_105	102	DI/DO		B-PD: nppukp
GPIO_106	90	DI/DO		B-PD: nppukp
GPIO_107	98	DI/DO		B-PD: nppukp
GPIO_111	207	DI/DO		B-PD:nppukp; used internally as bootconfig, which cannot be pulled up
GPIO_112	252	DI/DO		B-PD: nppukp
PM_GPIO_4	115	DI/DO		B-PD: nppukp; PMIC GPIO
PM_GPIO_3	124	DI/DO		B-PD: nppukp; PMIC GPIO
PM_GPIO_7	159	DI/DO		B-PD: nppukp; PMIC GPIO

Pin Name	Pin No.	I/O	Pin Description	Remarks
PM_GPIO_8	127	DI/DO		B-PD: nppukp; PMIC GPIO
LED interface				
CHG_LED	154	PO	Charge indicator	--
FLASH_LED	255	PO	Flash	--
RG_GRN	248	PO	RG light beads-GRN	--
RG_RED	249	PO	RG light beads-RED	--
INT Interface				
ALSP_INT	107	DI	Ambient light sensor interrupt signal	--
ACCEL_INT2	108	DI	G-Sensor interrupt signal 2	--
MAG_INT	109	DI	Magnetic sensor interrupt signal	--
ACCEL_INT1	110	DI	G-Sensor interrupt signal 1	--
Other Interfaces				
ADC	128	AI	ADC input	--
GNSS_LNA_EN	153	DO	GNSS_LNA enable	Don't suggest using it as GPIO.
NFC_CLK	256	AO	NFC clock	--
GRFC_13	247	DI/DO	Ordinary GPIO, 1.8V power domain	--
GRFC_14	202	DI/DO	Ordinary GPIO, 1.8V power domain	--
GRFC_15	203	DI/DO	Ordinary GPIO, 1.8V power	--

Pin Name	Pin No.	I/O	Pin Description	Remarks
			domain	
Reserved	16, 152, 190, 199, 204, 241, 242, 243, 244			--

Table 7. QUP interface description

Pin Name	GPIO	QUP Config		Function 1	Function 2	Function 3	Function 4
36	GPIO_0	QUP SE0	L0	UART_CTS	SPI_MISO	I2C_SDA	I3C_SDA
37	GPIO_1		L1	UART_RTS	SPI_MOSI	I2C_SCL	I3C_SCL
34	GPIO_2		L2	UART_TX	SPI_SCLK		
35	GPIO_3		L3	UART_RX	SPI_CS_0		
80	GPIO_4	QUP SE1	L0	UART_CTS	SPI_MISO	I2C_SDA	
82	GPIO_5		L1	UART_RTS	SPI_MOSI	I2C_SCL	
226	GPIO_69		L2	UART_TX	SPI_SCLK		
225	GPIO_70		L3	UART_RX	SPI_CS_0		
48, 183	GPIO_6	QUP SE2	L0	UART_CTS	SPI_MISO	I2C_SDA	
47	GPIO_7		L1	UART_RTS	SPI_MOSI	I2C_SCL	
31	GPIO_71		L2	UART_TX	SPI_SCLK		
30	GPIO_80		L3	UART_RX	SPI_CS_0		
95	GPIO_96	QUP SE4	L0	UART_CTS	SPI_MISO	I2C_SDA	

Pin Name	GPIO	QUP Config		Function 1	Function 2	Function 3	Function 4
96	GPIO_97	QUP SE5	L1	UART_RTS	SPI_MOSI	I2C_SCL	
94	GPIO_12		L2	UART_TX	SPI_SCLK		
93	GPIO_13		L3	UART_RX	SPI_CS_0		
118, 253	GPIO_14		L0	UART_CTS	SPI_MISO	I2C_SDA	
119, 254	GPIO_15		L1	UART_RTS	SPI_MOSI	I2C_SCL	
116	GPIO_16		L2	UART_TX	SPI_SCLK		
117	GPIO_17		L3	UART_RX	SPI_CS_0		

The QUP interfaces in the same group cannot be configured in different types at the same time, for example, UART and I²C interfaces.

3 Application Interfaces

3.1 Power Supply

The module provides four VBAT pins for connecting to external power supply source. The input range of power is 3.5V to 4.4V and the recommended value is 3.8V. The performance of the power supply such as its load capacity, ripple etc. will directly affect the operating performance and stability of the module. The peak current of the module can reach 3A. If the power supply capacity is insufficient, the power supply transient voltage drops below 3.5V, which may cause the module power-off or restart. The power supply voltage drop is shown in the following figure:

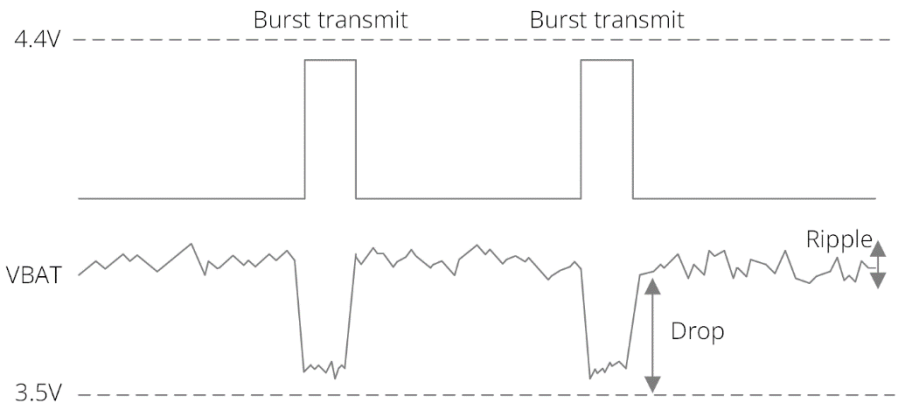

Figure 3. Voltage drop

3.1.1 Power input

External power source supplies the module by VBAT pins. To ensure the power transient voltage is no less than 3.5V, it is recommended to connect two 220μF tantalum capacitors with low ESR and filter capacitors of 1μF, 100nF, 39pF and 33pF in parallel to the VBAT input of the module. Besides, the PCB route of VBAT should be as short and wide as possible (no less than 3mm) and the ground plane of the power section should be flat to reduce the equivalent impedance of the VBAT route and avoid significant voltage drop at high currents at maximum transmit power.

Table 8. Power supply

Parameter	Minimum Value	Typical Value	Maximum Value	Unit
VBAT input voltage	3.5	3.8	4.4	V
VBAT operating current	-	-	3	A

The voltage range of VBAT power supply must be between 3.5V and 4.4V, including the superimposed value of ripple, drop, instantaneous overshoot and other voltages.

The following figure shows the reference design of power circuit.

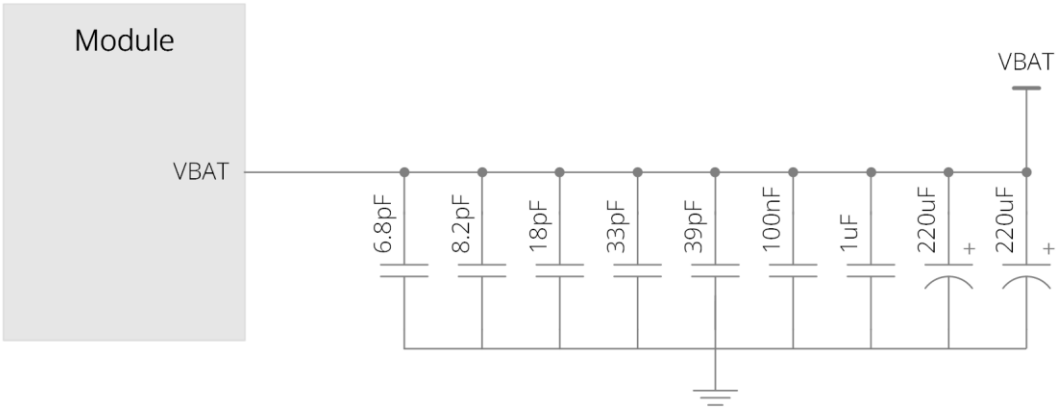

Figure 4. Reference design of power circuit

The following table describes the filter capacitor design of power supply.

Table 9. Filter capacitor design of power supply

Recommended Capacitor	Application	Description
220μF×2	Regulating	To reduce power fluctuations during module

Recommended Capacitor	Application	Description
	capacitor	operation, low ESR capacitors are required. LDO or DCDC power supply requires capacitor with a capacitance of no less than 440μF. Battery power supply requires capacitors with a capacitance of 100-220μF.
1μF, 100nF	Low frequency filter capacitors	Filter out interference caused by clock and digital signals
39pF, 33pF, 18pF, 8.2pF, 6.8pF	Decoupling capacitor	Filter high frequency interference

3.1.2 VRTC

VRTC is the power supply of the internal RTC clock of the module. When powered on VBAT pin, the VRTC pin will output voltage. When VBAT is disconnected, if the real-time clock needs to be maintained, it needs to be powered by an external power source (such as a coin battery). The VRTC parameters are as follows:

Table 10. VBATBK parameters

Parameter	Minimum Value	Typical Value	Maximum Value	Unit
VRTC output voltage	2.45	3.0	3.35	V
VRTC input voltage (clock works well)	2.8	3.0	3.35	V
VRTC input current (clock works well)	9	--	200	uA

The VRTC power supply uses the following reference circuit when powered by an external power source:

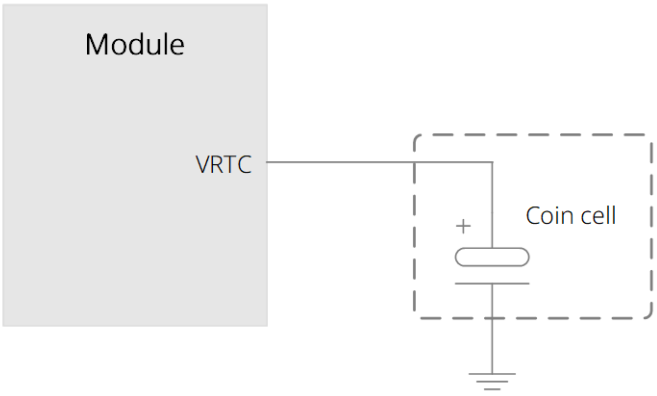

Figure 5. Reference circuit of VRTC power supply

3.1.3 VPH_PWR

The module supports the output of VPH_PWR as the peripheral power supply, and the voltage is the same as that of VBAT. It can be used for the power supply of LCD, backlight, and other peripherals.

3.1.4 Power output

The module provides multiple power outputs for peripheral circuits. 33pF and 10pF capacitors can be connected in parallel to avoid high frequency interference effectively.

Table 11. Power output

Pin Name	Default Voltage (V)	Drive Current (mA)
VDD_2V8	2.8	500
LDO15_1V8	1.8	400
VPH_PWR	=VBAT	1000
LDO19_UIM2	1.8/3.0	100
LDO18_UIM1	1.8/3.0	100
IOVDD_1V8	1.8	300
LDO17A_3V0	3.0	200

Pin Name	Default Voltage (V)	Drive Current (mA)
LDO4_SDIO	1.8/2.95	20
LDO21_SD	2.95	800

3.2 Control Signal

3.2.1 Power On/Off

The module provides two-way power-on/off control signals to control module's power-on/off, restart and sleep/wakeup.

Table 12. Power-on/off control signal

Pin Name	Pin No.	I/O	Description	Remarks
KEY_PWR_ON	114	DI	Active low, used to power on/off and restart the module, make the module to sleep, and wake up the module	--
CBL_PWR_N	261	DI	Active low, used to power on the module only	--

3.2.1.1 Power-On

After the module's VBAT pin is powered on, pull down KEY_PWR_ON pin for 2s–8s to trigger module to start. The keystroke and OC driver power-on reference circuit are designed as follows:

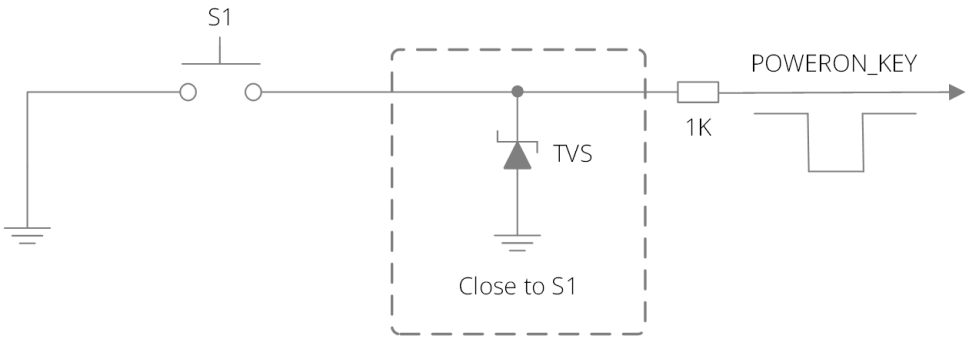

Figure 6. Keystroke power-on reference circuit

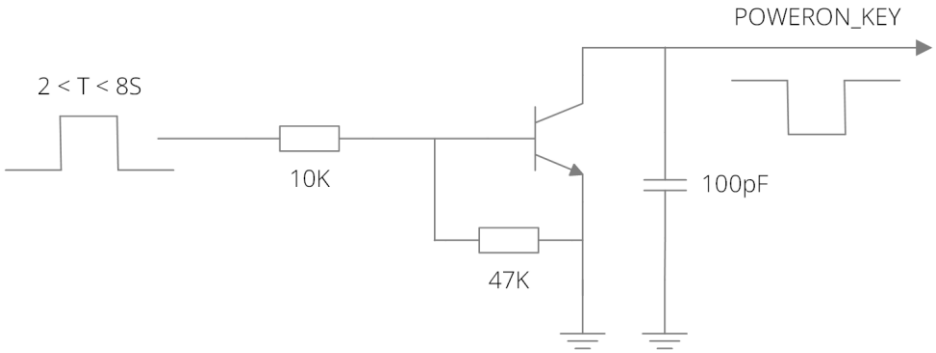

Figure 7. OC driver power-on reference circuit

The CBL_PWR_N pin is connected to the ground through a 1K resistor, and the module can be started up automatically after power-on. The following figure shows the reference circuit for automatic startup upon power-on.

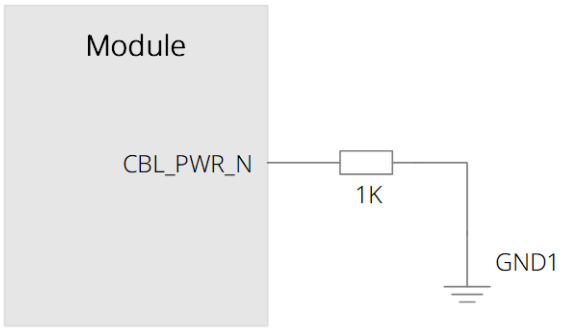

Figure 8. CBL power-on reference circuit

Power on sequence is shown as follows:

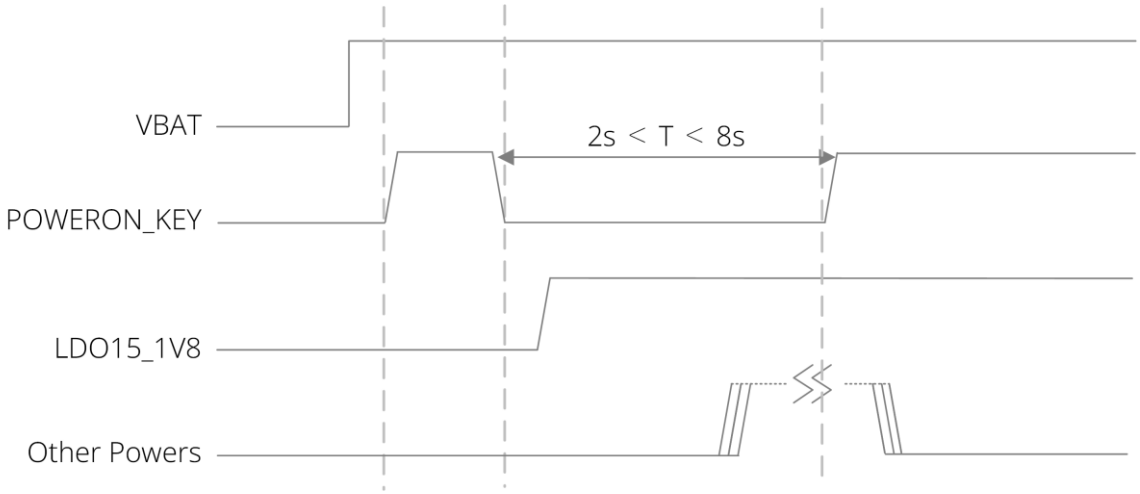

Figure 9. Startup timing sequence

3.2.1.2 Power-off and Reset

Normal power off: When the module is in operating mode, pull down KEY_PWR_ON pin for more than 2s. A dialog box is displayed, prompting you to power off or restart the module.

Forced power off: Pull down KEY_PWR_ON pin for 9s to 15s, and the module will be forcibly powered off. The forced power off timing is as follows:

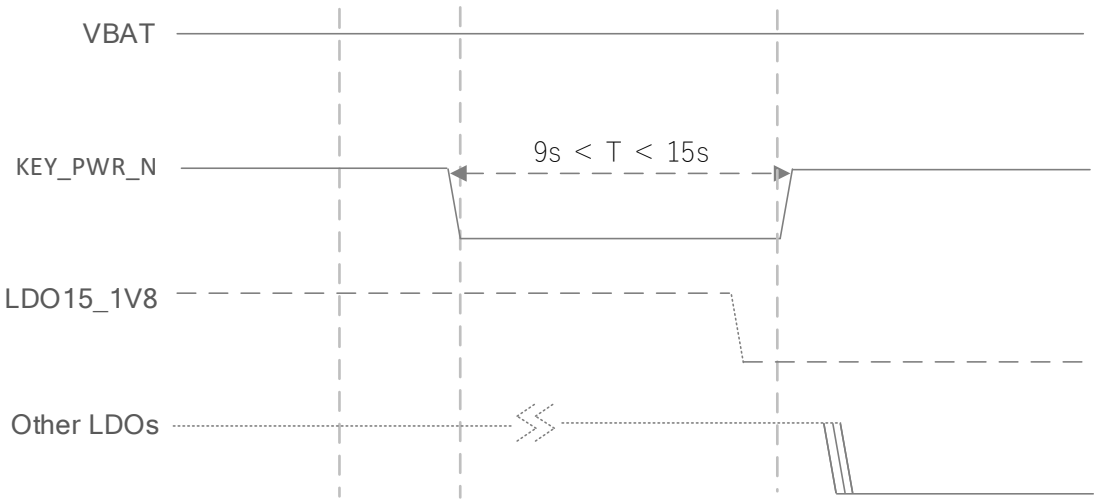

Figure 10. Power-off timing

When the system is abnormal or crashes, you can forcibly reset the module. The normal power-off method is recommended in normal cases, because forced reset may cause data loss and other anomalies.

Reset: Pull down RESET_N pin for 4s.

3.2.1.3 Sleep/Wakeup

When module is in standby mode, pull down KEY_PWR_ON pin for 0.5s and the module will enter sleep mode. The system supports automatic sleep. The time from standby to sleep can be configured through software.

When module is in sleep mode, pull down KEY_PWR_ON pin for 0.5s and the module can be woken up.

3.2.1.4 Volume Control

KEY_VOL_UP and KEY_VOL_DOWN pins are used as the volume down key and volume up key; the volume key circuit design can be referred to the power-on circuit design.

3.3 USB interface

The module supports one USB 3.1 interface that is downward compatible with USB 2.0 interface. USB 3.1 interface supports SS (5Gbps) mode, but does not support software download.

USB 2.0 interface supports the HS (480Mbps) mode and software download, and is downward compatible with FS and LS interface.

USB supports OTG function and HUB expansion interface. The pin definition of the USB interface is as follows:

Table 13. USB 3.1 pin definition

Pin Name	Pin No.	I/O	Description	Remarks
USB_SS1_RX_M	210	AI	USB 3.1 differential data receiving-	--
USB_SS1_RX_P	195	AI	USB 3.1 differential data receiving+	--
USB_SS1_TX_M	196	AO	USB 3.1 differential data sending-	--
USB_SS1_TX_P	197	AO	USB 3.1 differential data sending+	--
USB_SS2_RX_M	151	AI	USB 3.1 differential data receiving-	--
USB_SS2_RX_P	224	AI	USB 3.1 differential data receiving+	--
USB_SS2_TX_M	223	AO	USB 3.1 differential data sending-	--
USB_SS2_TX_P	222	AO	USB 3.1 differential data sending+	--
USB_CC1	194	AI/AO	USB_CC1	--
USB_CC2	191	AI/AO	USB_CC2	--

Table 14. USB 2.0 pin definition

Pin Name	Pin No.	I/O	Description	Remarks
USB_VBUS	141, 142	PI/PO	USB 5V power supply	--

Pin Name	Pin No.	I/O	Description	Remarks
USB_DM	13	AI/AO	USB 2.0 differential data signal-	--
USB_DP	14	AI/AO	USB 2.0 differential data signal+	--

The reference circuit design of the USB 3.1 (Type-C) interface is as follows:

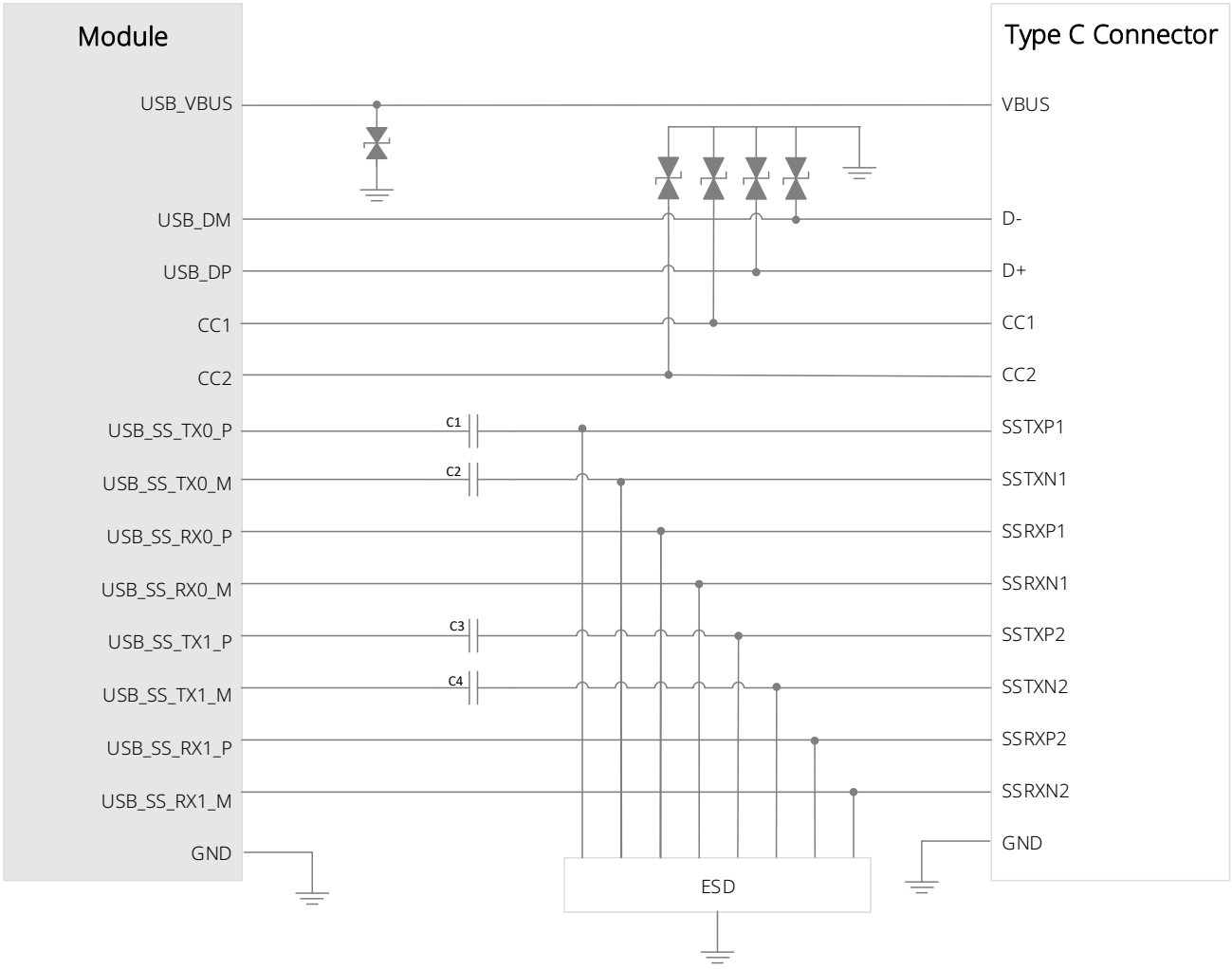

Figure 11. USB 3.1 reference circuit design

The reference circuit design of the USB 2.0 interface is as follows:

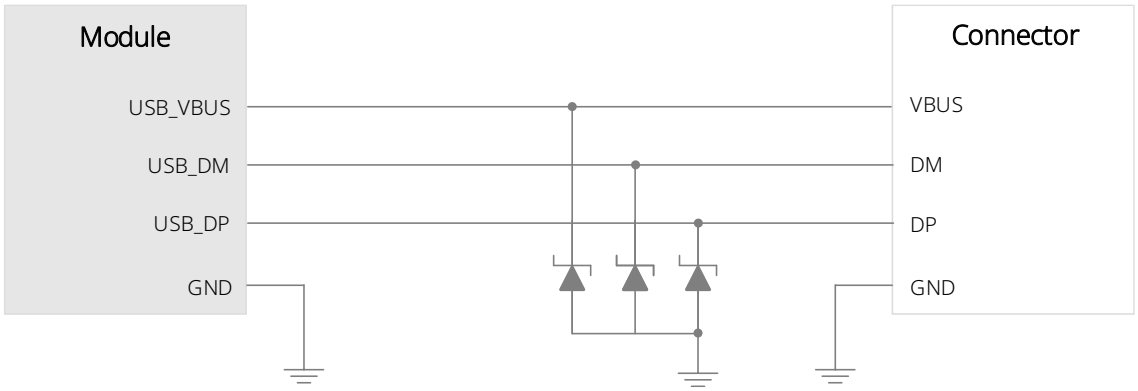

Figure 12. USB 2.0 reference circuit design

Precautions for USB design:

- The junction capacitor for ESD protection device of USB_DP/DM must be less than 2pF.
- USB_DP and USB_DM are high-speed differential signal lines. The highest transmission rate is 480Mbps. Please pay attention to the following requirements during PCB layout:
  - USB_DP and USB_DM signal cables should be parallel and equal in length (differential cable length differences should be controlled within 2mm), while the right-angle route shall be avoided, and differential 90Ω impedance shall be controlled.
  - USB2.0 differential signal cables should be fully grounded.
- Support OTG function: The VBUS interface of the module provides 5V output as OTG power supply.
- The module supports charging function by default, but does not support fast charging.

Precautions for USB 3.1 design:

- USB 3.1 is a high-speed signal cable and needs to be well-shielded (differential cable surrounded by grounding lines should be fully grounded), and follows the principle of high-speed differential cable routing.
- Control the differential impedance, make it 90Ω±10% and ensure that the differential cable length differences is within 0.7mm.

- The parasitic capacitance of ESD device must be less than 0.5pF.

3.4 UART

The module defines three sets of UART ports, which are all in 1.8V voltage domain. The pin definition is as follows:

Table 15. UART pin definition

Pin Name	Pin No.	I/O	Description	Remarks
UART0_TX	34	DO	UART0 serial interface data sending signal	--
UART0_RX	35	DI	UART0 serial interface data receiving signal	--
UART0_CTS	36	DI	UART0 serial interface CTS signal	--
UART0_RTS	37	DO	UART0 serial interface RTS signal	--
UART_DBG_RX	93	DI	Debugging serial interface UART_RX	--
UART_DBG_TX	94	DO	Debugging serial interface UART_TX	--
UART1_RX	225	DI	Serial interface UART1_RX	--
UART1_TX	226	DO	Serial interface UART1_TX	--

The voltage domain of each serial port is 1.8V; when communicating with other voltage domain serial ports, it is necessary to add a level-shifting chip with the following reference circuit design:

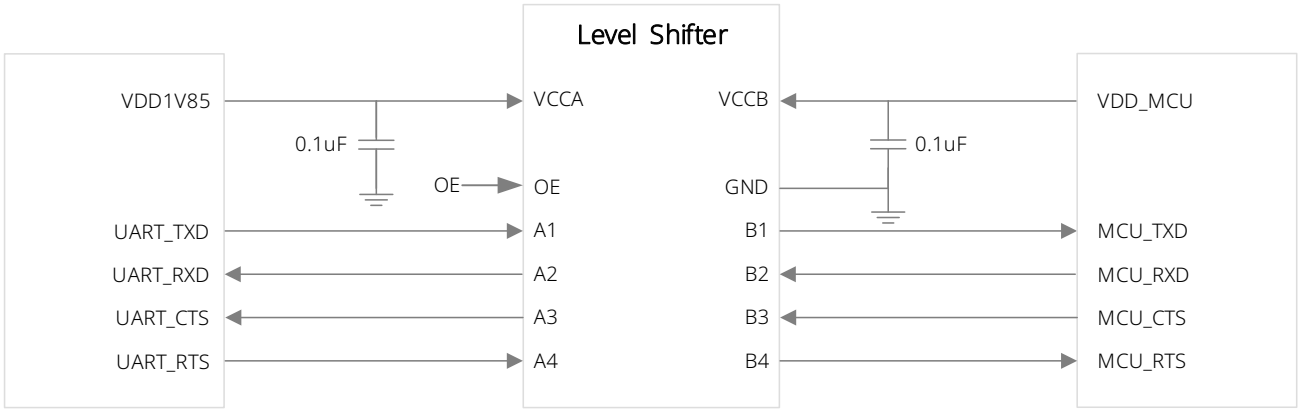

Figure 13. Level conversion reference circuit

3.5 SPI

By default, the module provides one set of SPI interfaces that support primary/secondary mode. The pin definition is as follows:

Table 16. SPI pin definition

Pin Name	Pin No.	I/O	Description	Remarks
SPI_CLK	116	DO	SPI clock	--
SPI_CS	117	DO	SPI chip select	--
SPI_MISO	118, 253	DI	SPI Master In Slave Out	--
SPI_MOSI	119, 254	DO	SPI Master output Slave input	--

3.6 SD

The module supports one SD interface. The pin definition is as follows:

Table 17. Definition of SD interface pins

Pin No.	Pin Name	I/O	Description	Remarks
SD_DET	45	DI	SD card detection	Active low by default

Pin No.	Pin Name	I/O	Description	Remarks
SD_DATA3	44	DI/DO	SD card data bit 3	--
SD_DATA2	43	DI/DO	SD card data bit 2	--
SD_DATA1	42	DI/DO	SD card data bit 1	--
SD_DATA0	41	DI/DO	SD card data bit 0	--
SD_CMD	40	DI/DO	SD card command interface	--
SD_CLK	39	DO	SD card clock	--
LDO21_SD	38	PO	LDO L21 2.9V power output	--
LDO4_SDIO	32	PO	LDO L4 SDIO pull up power output	--

SD interface reference circuit design is as follows:

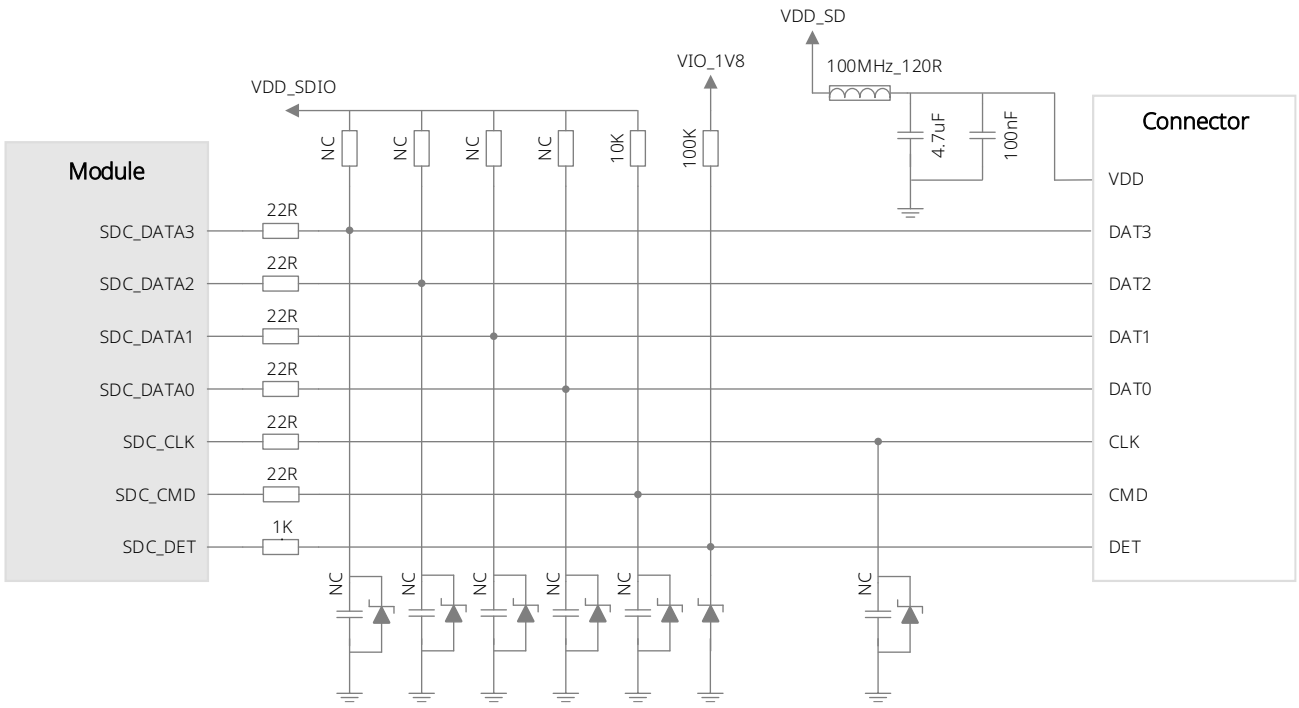

Figure 14. SD reference circuit

- LDO21_SD is the SD card peripheral driving power and can provide about 800mA current. Pay attention to control the width of cable, which should be larger than 0.8mm.
- Pull up SD_DET with LDO15_1V8 power supply.
- SD is a high-speed digital signal line and must be shielded. Their length must be equal during layout.
- Note that the length of the SD card clock and signal cables should not exceed 50mm, and the TVS tube should be a device with a parasitic capacitance less than 0.5pF.

3.7 SIM

The module supports two (U)SIM cards that support dual card dual standby. The pin definition is as follows:

Table 18. Definition of SIM interface pins

Pin No.	Pin Name	I/O	Description	Remarks
UIM1_DET	22	DI	（U）SIM1 card detection	Active high by default
UIM1_RST	23	DO	（U）SIM1 reset	--
UIM1_CLK	24	DO	（U）SIM1 clock	--
UIM1_DATA	25	DI/DO	（U）SIM1 data	--
UIM2_DET	17	DI	（U）SIM2 card detection	Active high by default
UIM2_RST	18	DO	（U）SIM2 reset	--
UIM2_CLK	19	DO	（U）SIM2 clock	--
UIM2_DATA	20	DI/DO	（U）SIM2 data	--

SIM reference circuit design is as follows:

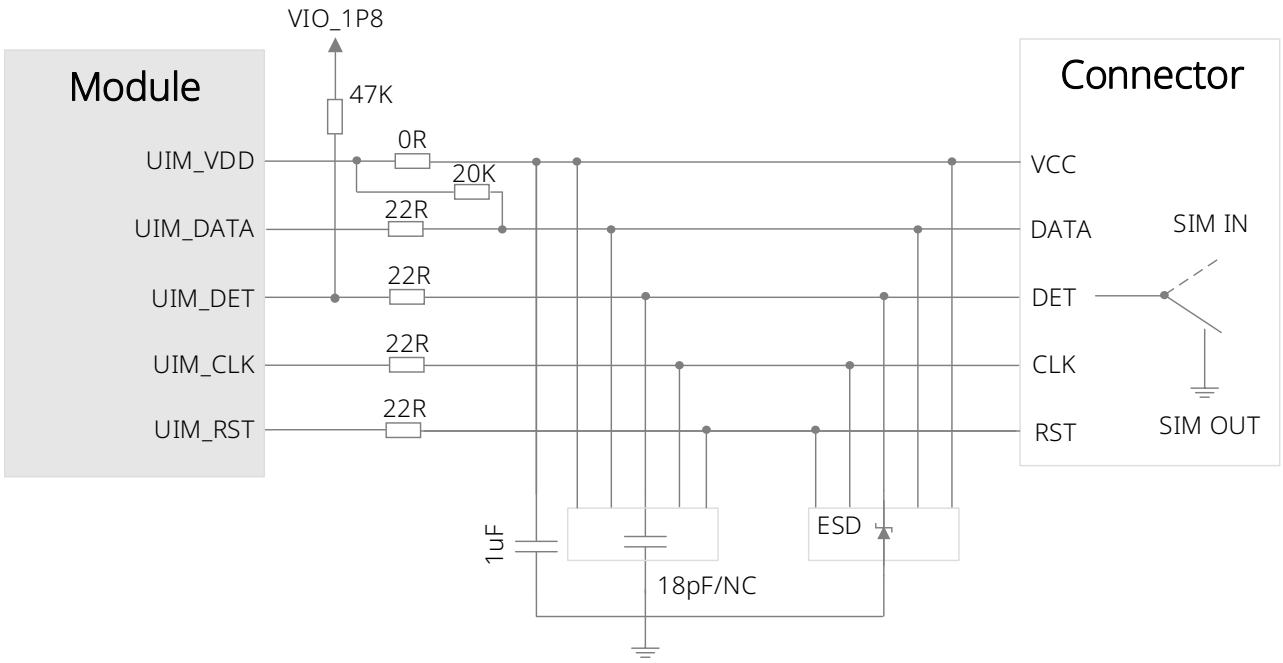

Figure 15. SIM reference circuit

3.8 GPIO

The module has rich GPIO resources and the interface level is 1.8V. The pin definition is as follows:

Table 19. GPIO list

Pin Name	Pin No.	Reset Status	Interrupt Function
GPIO_28	33	B-PD: nppukp	YES
GPIO_31	97	B-PD: nppukp	YES
GPIO_32	99	B-PD: nppukp	YES
GPIO_55	100	B-PD: nppukp	NO
GPIO_56	106	B-PD: nppukp	NO
GPIO_57	112	B-PD: nppukp	NO
GPIO_58	113	B-PD: nppukp	NO

Pin Name	Pin No.	Reset Status	Interrupt Function
GPIO_60	123	B-PD: nppukp	NO
GPIO_86	257	B-PD: nppukp	YES
GPIO_98	206	B-PD: nppukp	NO
GPIO_99	105	B-PD: nppukp	YES
GPIO_100	205	B-PD: nppukp	NO
GPIO_101	187	B-PD: nppukp	YES
GPIO_102	104	B-PD: nppukp	YES
GPIO_103	103	B-PD: nppukp	YES
GPIO_104	101	B-PD: nppukp	YES
GPIO_105	102	B-PD: nppukp	YES
GPIO_106	90	B-PD: nppukp	YES
GPIO_107	98	B-PD: nppukp	YES
GPIO_111	207	B-PD: nppukp	NO
GPIO_112	252	B-PD: nppukp	YES
PM_GPIO_4	115	B-PD: nppukp	YES
PM_GPIO_3	124	B-PD: nppukp	YES
PM_GPIO_7	159	B-PD: nppukp	YES
PM_GPIO_8	127	B-PD: nppukp	YES

Table 20. Parameter description

Parameter	Description
B	Bidirectional digital with CMOS input
NP	pdpukp: defaulted to no-pull with programmable options

Parameter	Description
	following the colon (:).
PD	nppukp: defaulted to pull-down with programmable options following the colon (:).
PU	nppdkp: defaulted to pull-up with programmable options following the colon (:).
KP	nppdpu: defaulted to keeper with programmable options following the colon (:).

3.9 I²C

The module provides 4 sets of I²C interfaces for TP, camera, sensor and peripheral. The I²C pin definition is shown in the following table:

Table 21. I²C interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
TP_I2C_SCL	47	OD	TP I²C clock signal	Dedicated for TP
TP_I2C_SDA	48, 183	OD	TP I²C data signal	
CAM_I2C_SCL0	83	OD	I²C clock signal of camera 0	For camera only
CAM_I2C_SDA0	84	OD	I²C data signal of camera 0	
CAM_I2C_SCL1	239	OD	I²C clock signal of camera 1/2	For camera only
CAM_I2C_SDA1	240	OD	I²C data signal of camera 1/2	
SENSOR_I2C_SCL	91	OD	Sensor I²C clock	For sensor only

Pin Name	Pin No.	I/O	Description	Remarks
SENSOR_I2C_SDA	92	OD	Sensor I²C data	

When I²C has more than one peripheral, please ensure the uniqueness of every peripheral address. If one of the peripherals has high requirement for timeliness, do not set the peripherals to share one set of I²C interfaces.

3.10 ADC

The module provides one ADC interface and its maximum resolution is 15 bits. The pin definition is as follows:

Table 22. ADC interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
ADC	128	AI	ADC input	Maximum input voltage range of 1.8V

3.11 Battery Supply Interface

Table 23. Battery interface pin definition

Pin Name	Pin Name	I/O	Description	Remarks
VBAT_SNS	133	AI	Battery positive detection	Connected to the positive pole of the battery.
VBAT_M	258	AI	Battery negative detection	Connected to the negative pole of the battery. Keep the unused pins unconnected.
VBAT_THERM	134	AI	Battery temperature	Connect the pin to GND with

Pin Name	Pin Name	I/O	Description	Remarks
			detection	10KΩ resistor if the pin is unused.
VBAT_ID	260	AI	Battery ID pin	Connect the pin to GND with 100KΩ resistor if the pin is unused

3.11.1 Charging Description

TBD

3.12 Motor Driver Interface

Table 24. Motor interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
VIB_DRV_P	28	PO	Motor driver pin	Connect the positive terminal of the motor

3.13 LCD

The screen interface is based on MIPI_DSI standard and supports one set of 4-Lane high-speed differential data transmission. It supports 1080P resolution.

Table 25. LCD pin definition

Pin Name	Pin No.	I/O	Description	Remarks
MIPI_DSI0_CLK_N	52	AO	LCD MIPI-DSI signal	--
MIPI_DSI0_CLK_P	53	AO		--

Pin Name	Pin No.	I/O	Description	Remarks
MIPI_DSI0_LN0_N	54	AO		--
MIPI_DSI0_LN0_P	55	AO		--
MIPI_DSI0_LN1_N	56	AO		--
MIPI_DSI0_LN1_P	57	AO		--
MIPI_DSI0_LN2_N	58	AO		--
MIPI_DSI0_LN2_P	59	AO		--
MIPI_DSI0_LN3_N	60	AO		--
MIPI_DSI0_LN3_P	61	AO		--
PWM	29	DO	LCD backlight brightness PWM control	--
LCD_RST	49	DO	LCD reset signal	--
LCD_TE	50	DI	LCD swipe synchronization signal	--
VDD_2V8	129	PO	2.8V voltage output	--
LDO15_1V8	111	PO	LDO L15 1.8V power output	--

The reference circuit of LCD interface is as follows:

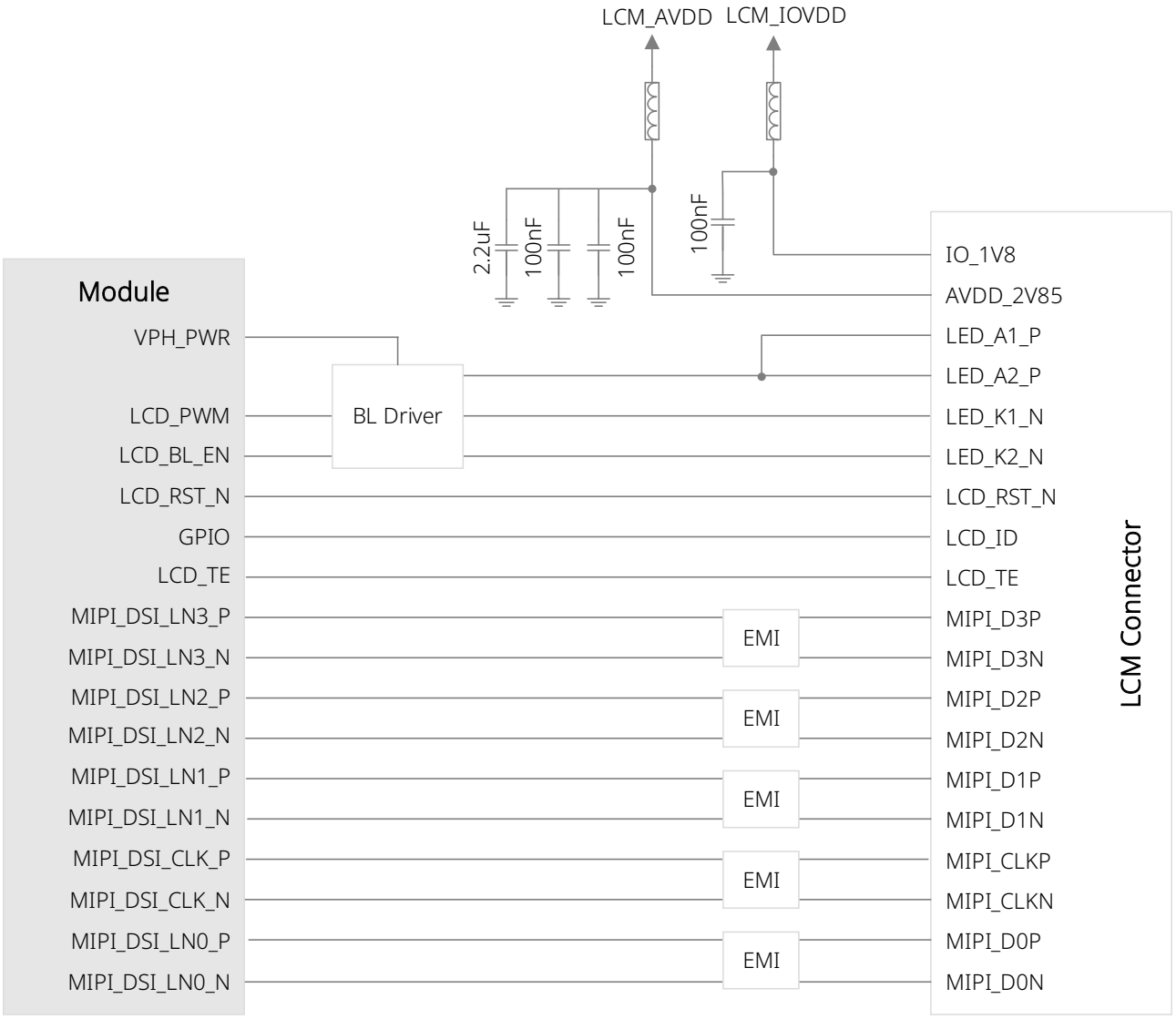

Figure 16. LCD reference circuit

Precautions for LCD design:

- MIPI is a high-speed signal line. It is recommended to connect the common mode inductor in series near the LCD connector to reduce the EMI (electromagnetic interference) of the circuit;
- MIPI routing is recommended to be designed in the inner layer, and connected using GND in three dimensions;
- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance ±10%;

- The total length of the cable shall not exceed 300mm;
- The intra lane match of MIPI signal cable must be controlled within 0.67mm;
- The inter lane match of MIPI signal cable must be controlled within 1.3mm;
- EMI components are optional, and the whole routing stray capacitance should be controlled under 1pF;
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width.

3.14 TP

The module provides one set of I²C interfaces that can be used to connect to the TP and the module provides power, interrupt, reset pins required for the TP. The pin definition of the module is shown in the following table:

Table 26. TP pin definition

Pin Name	Pin No.	I/O	Description	Remarks
VDD_2V8	129	PO	2.8V voltage output	--
LDO15_1V8	111	PO	LDO L15 1.8V power output	--
TP_INT	30	DI	TP interrupt	--
TP_RST	31	DO	TP reset signal	--
TP_I2C_SCL	47	DO	TP I²C clock signal	--
TP_I2C_SDA	48, 183	DI/DO	TP I²C data signal	--

TP reference circuit design is as follows:

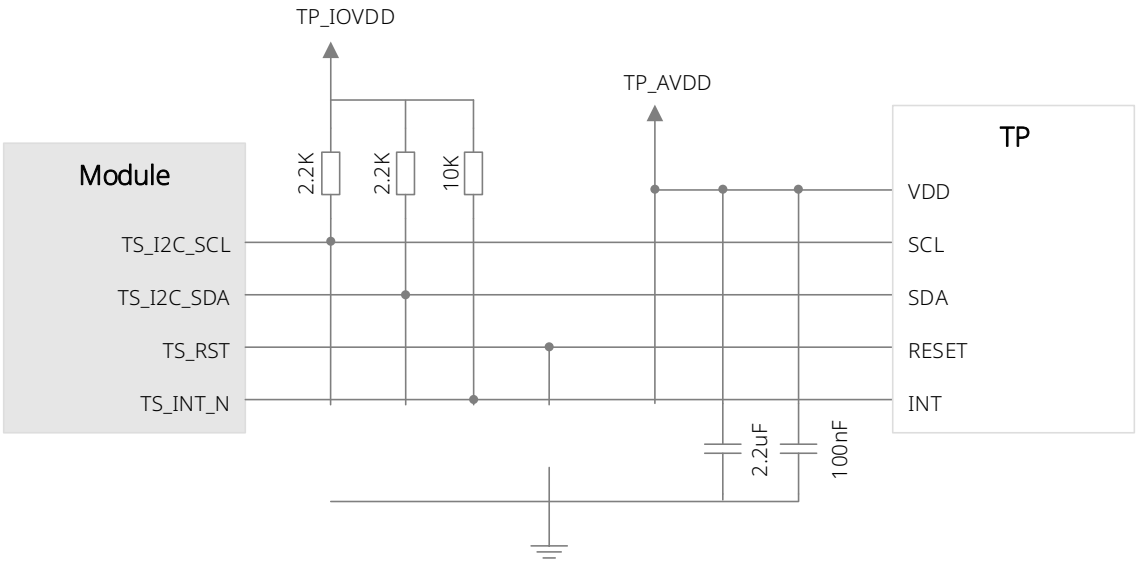

Figure 17. TP reference circuit design

3.15 Camera

The camera interface of module is based on the MIPI_CSI standard, and can support two (4 Lane + 4 Lane) or three (4 Lane + 2 Lane + 1 Lane) cameras. The maximum resolution is 25MP. The pin definition of camera interface is as follows:

Table 27. Camera interface pin definition

Pin Name	Pin No.	I/O	4-lane+2-lane+1-lane
MIPI_CSI0_CLK_P	229	AI	4-lane camera MIPI-CSI0 interface. Keep the unused pins unconnected.
MIPI_CSI0_CLK_N	230	AI	
MIPI_CSI0_LN0_N	231	AI	
MIPI_CSI0_LN0_P	155	AI	
MIPI_CSI0_LN1_N	232	AI	
MIPI_CSI0_LN1_P	156	AI	
MIPI_CSI0_LN2_N	233	AI	
MIPI_CSI0_LN2_P	157	AI	

Pin Name	Pin No.	I/O	4-lane+2-lane+1-lane
MIPI_CSI0_LN3_N	234	AI	
MIPI_CSI0_LN3_P	158	AI	
MIPI_CSI1_CLK_N	63	AI	2-lane camera CSI1 interface. Keep the unused pins unconnected.
MIPI_CSI1_CLK_P	64	AI	
MIPI_CSI1_LN0_N	65	AI	
MIPI_CSI1_LN0_P	66	AI	
MIPI_CSI1_LN1_N	67	AI	
MIPI_CSI1_LN1_P	68	AI	
MIPI_CSI1_LN3_N	70	AI	1-lane camera CSI2-M interface
MIPI_CSI1_LN3_P	71	AI	
MIPI_CSI1_LN2_N	72	AI	
MIPI_CSI1_LN2_P	73	AI	
MCAM_MCLK	74	DO	Camera 0 clock signal
MCAM_RST	79	DO	Camera 0 reset signal
MCAM_PWDN	80	DO	Camera 0 shutdown signal
SCAM_MCLK	75	DO	Camera 1 clock signal
SCAM_RST	81	DO	Camera 1 reset signal
SCAM_PWDN	82	DO	Camera 1 shutdown signal
DCAM_PWDN	236	DO	Camera 2 shutdown signal
DCAM_RST	237	DO	Camera 2 reset signal
DCAM_MCLK	238	DO	Camera 2 clock signal
CAM_I2C_SCL0	83	DO	I^2C clock signal of camera 0

Pin Name	Pin No.	I/O	4-lane+2-lane+1-lane
CAM_I2C_SDA0	84	DI/DO	I²C data signal of camera 0
CAM_I2C_SCL1	239	DO	I²C clock signal of camera 1/2
CAM_I2C_SDA1	240	DI/DO	I²C data signal of camera 1/2
IOVDD_1V8	125	PO	LDO 1.8V power output
VDD_2V8	129	PO	2.8V voltage output
External LDO			
VDD_1V2	--	--	The module does not have this power supply, so it needs to be provided by an external high-power noise suppression ratio LDO
VDDAF_2V8	--	--	

3.15.1 Camera 0

The reference circuit design of camera 0 is as follows:

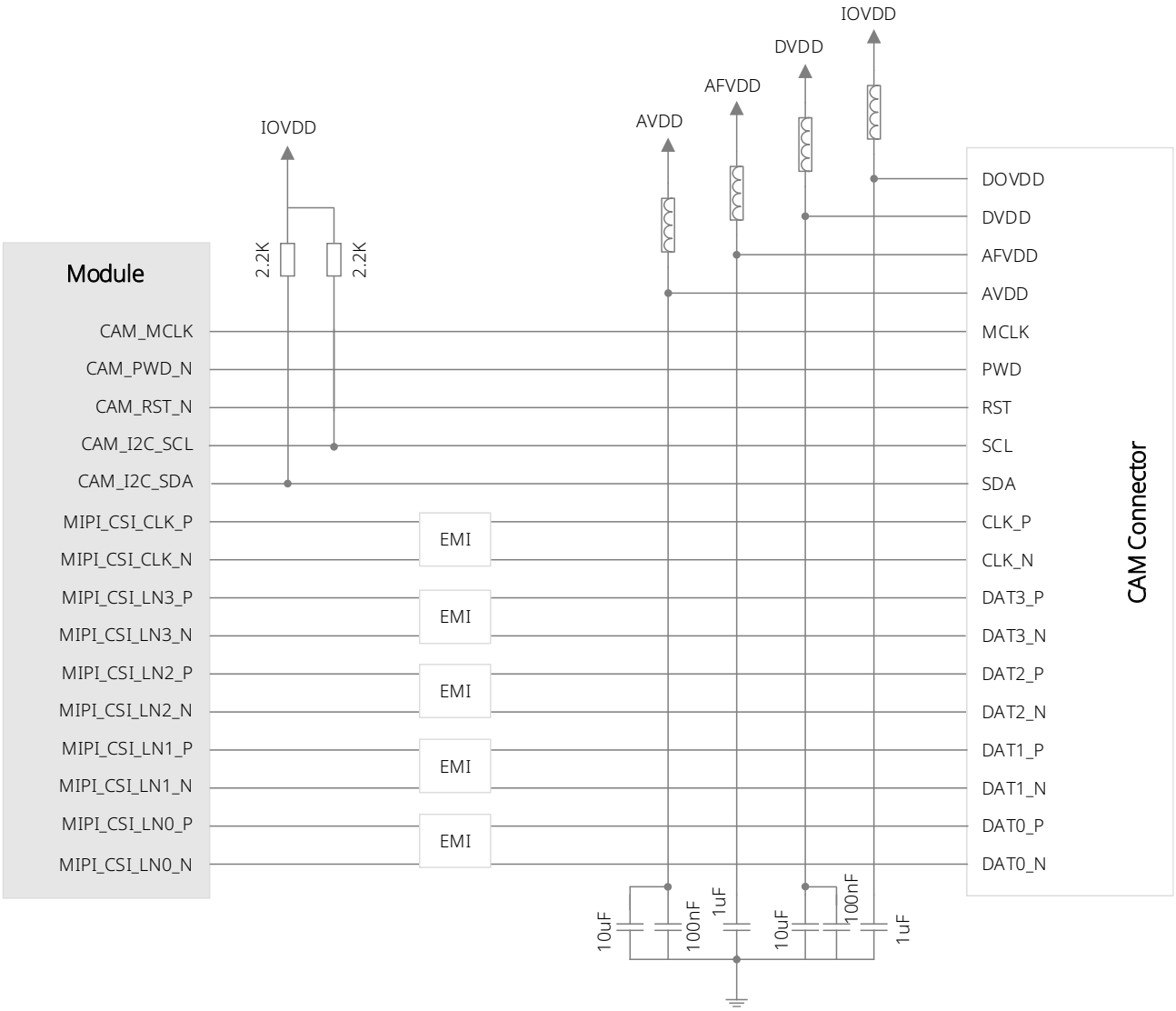

Figure 18. Reference circuit design of camera 0

3.15.2 Camera 1

The reference circuit design of camera 1 is as follows:

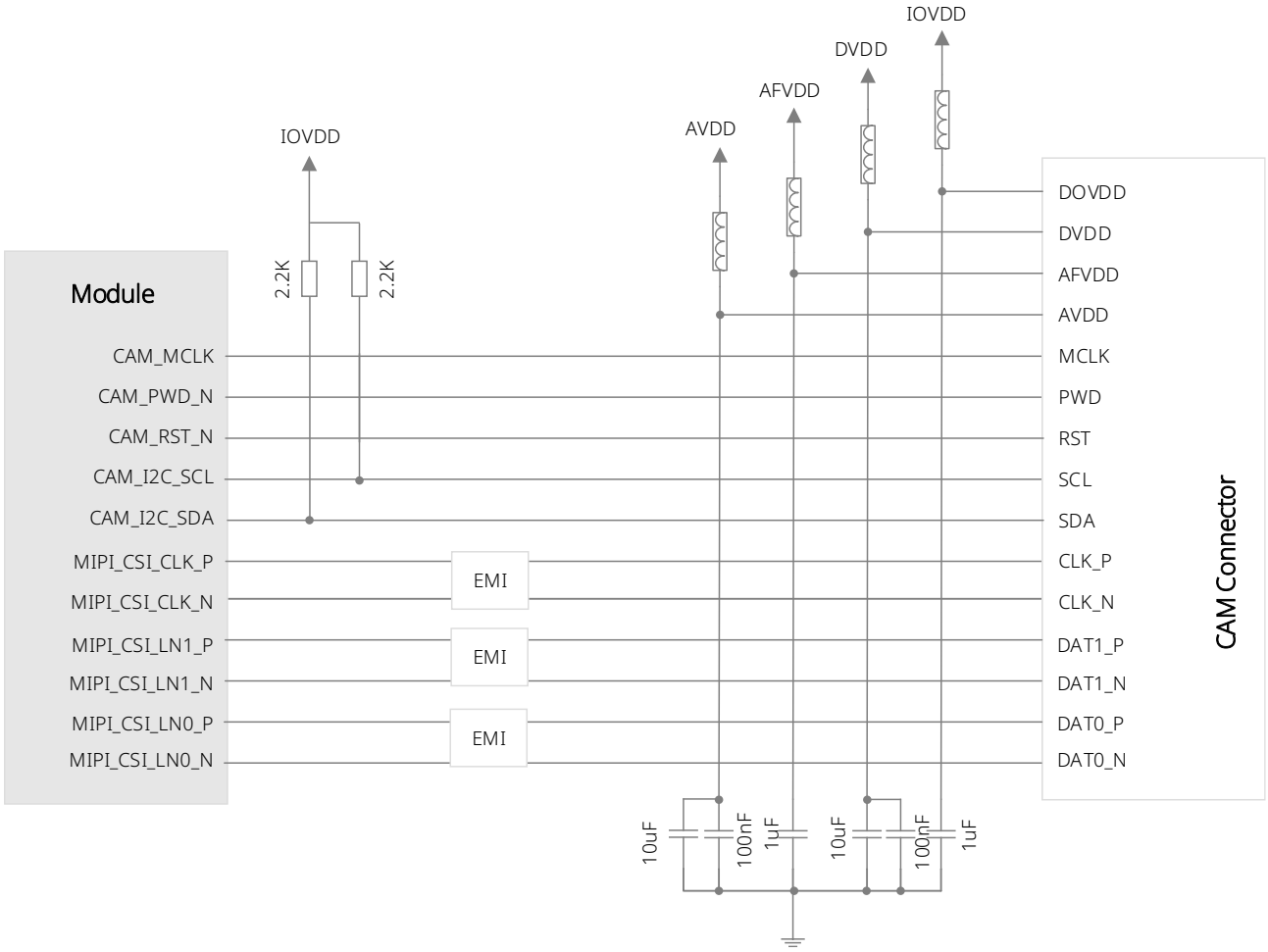

Figure 19. Reference circuit design of camera 1

3.15.3 Camera 2

The reference circuit design of camera 2 is as follows:

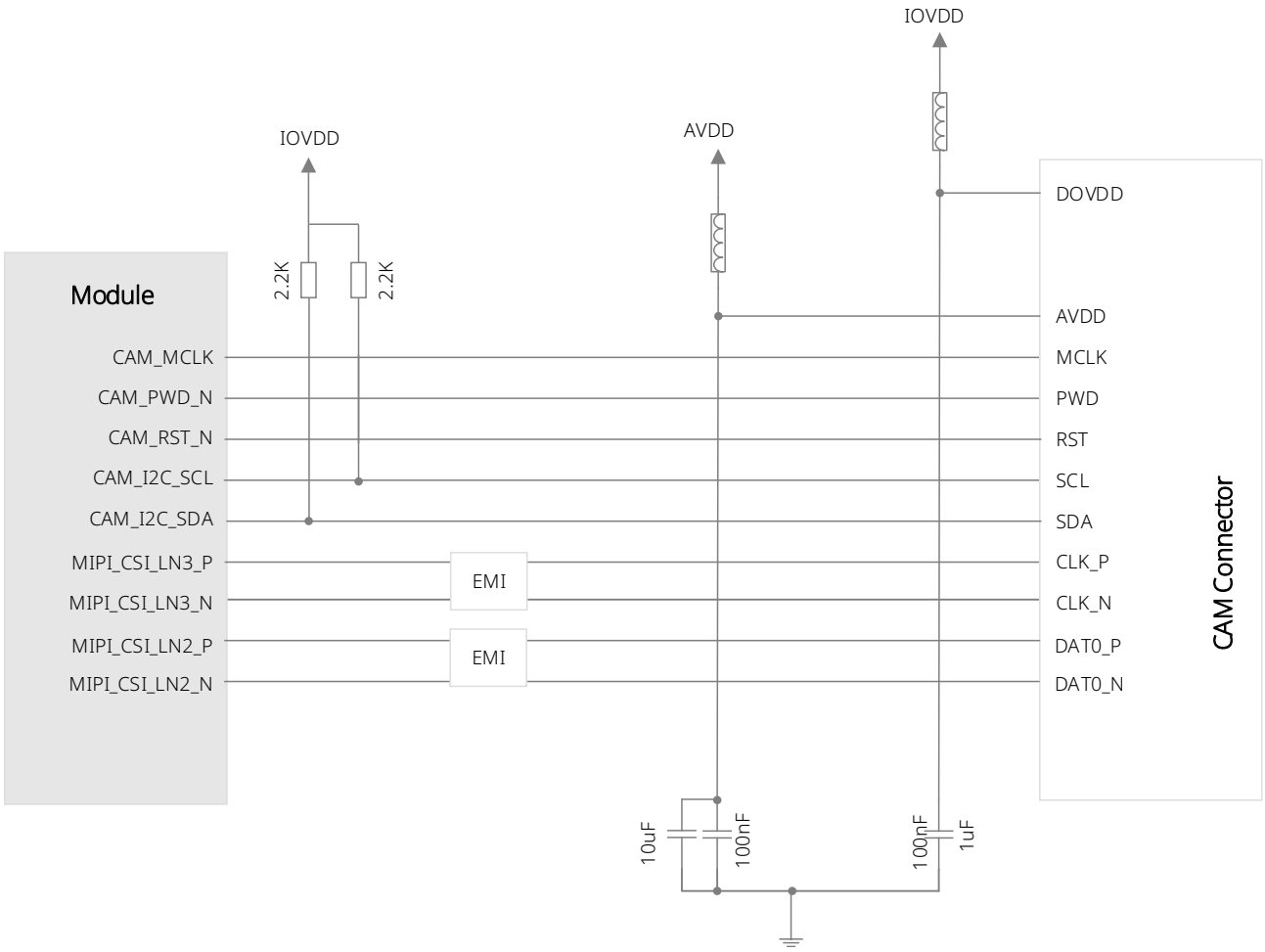

Figure 20. Reference circuit design of camera 3

3.15.4 Design Considerations

MIPI_CSI is a high-speed signal line. Pay attention to the following points during PCB layout.

- MIPI is a high-speed signal line. It is recommended to connect the common mode inductor in series near the camera connector to reduce the EMI (electromagnetic interference) of the circuit;
- MIPI routing is recommended to be designed in the inner layer, and connected using GND in three dimensions;

- The MIPI signal line needs to be controlled with a 100Ω differential impedance with tolerance ±10%;
- The total length of the cable shall not exceed 300mm;
- The intra lane match of MIPI signal cable must be controlled within 0.67mm;
- The inter lane match of MIPI signal cable must be controlled within 1.3mm;
- It is recommended that the space of intra-lane differential line should be 1 times of the route width and the space between differential line and other routes should be controlled 2.5 times of the route width ;

Design considerations for other signal cable:

- CAM_MCLK is a high-speed clock signal cable and requires fully grounded.
- The camera AVDD power supply routing should be away from interference sources to avoid interference of power noise;
- It is recommended to add LDO with high PSRR ability to the camera AVDD power supply;
- VDD_1V2 and VDDAF_2V8 should be provided by external high-power noise reduction ratio LDO.
- If you need both two cameras to work at the same time, don't choose to share I2C. If you need to share I^2C, confirm that the I^2C addresses of the two cameras are unique.

3.16 Audio

3.16.1 Definition of Audio Interface

The module supports analog audio interface, and has 3 inputs and 3 outputs. Pin definition is as follows:

Table 28. Audio interface pin definition

Pin Name	Pin No.	I/O	Description	Remarks
MIC1_P	4	AI	Main MIC input+	--
MIC1_M	5	AI	Main MIC input-	--
MIC2_P	6	AI	Headphone MIC input+	--
MIC3_P	220	AI	Secondary MIC input+	--
MIC3_M	221	AI	Secondary MIC input-	--
EAR_P	8	AO	Receiver output+	--
EAR_M	9	AO	Receiver output-	--
LINEOUT_P	10	AO	Differential Lineout output+	It requires an external audio PA.
LINEOUT_M	11	AO	Differential Lineout output-	
HPH_R	136	AO	Headphone right channel output	--
HPH_GND	137	/	Headphone reference ground	It requires to be grounded.
HPH_L	138	AO	Headphone left channel output	--
HPH_DET	139	AI	Headphone plug detection	--
MIC_BIAS1	219	PO	Main MIC bias voltage 1	An external MIC bias circuit needs to be added for the module.
MIC_BIAS3	227	PO	Secondary MIC bias voltage 3	

Audio Interface Design Consideration:

- The MIC_BIAS bias circuit needs to be added to the main and secondary MICs outside the module; the headphone MIC is already set internally, so that you do not need to add it;
- The reference ground of the headphone should be grounded near the connector;
- It is recommended to use receiver with 32Ω impedance;
- Reduce noise and improve audio quality, the following approaches are recommended:
  - Keep audio PCB routing away from the antenna and high-frequency digital signal;
  - Reserve LC filter circuit in audio circuit to reduce EMI;
  - Shield the audio routing.

3.16.2 MIC Circuit Design

It is recommended to use a silicon MIC, and the reference design circuit is as follows:

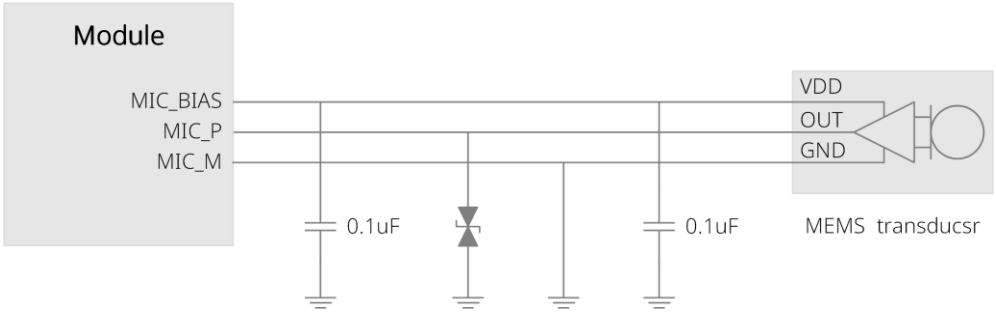

Figure 21. Microphone circuit design

3.16.3 Receiver Circuit Design

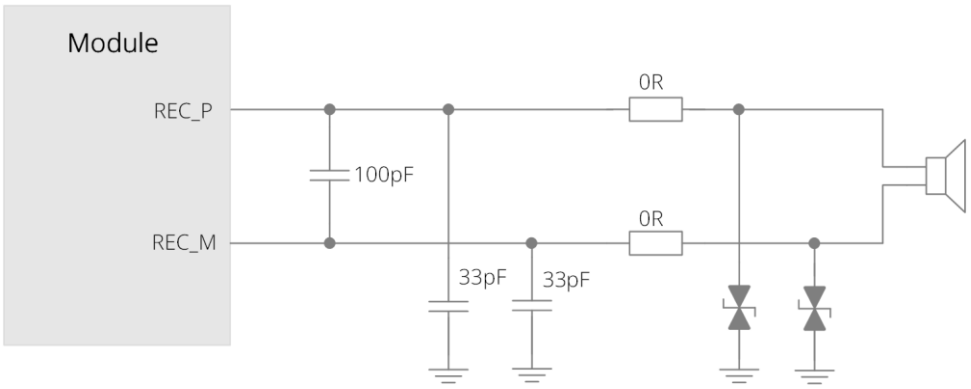

Figure 22. Receiver circuit design

3.16.4 Headphone Interface Circuit Design

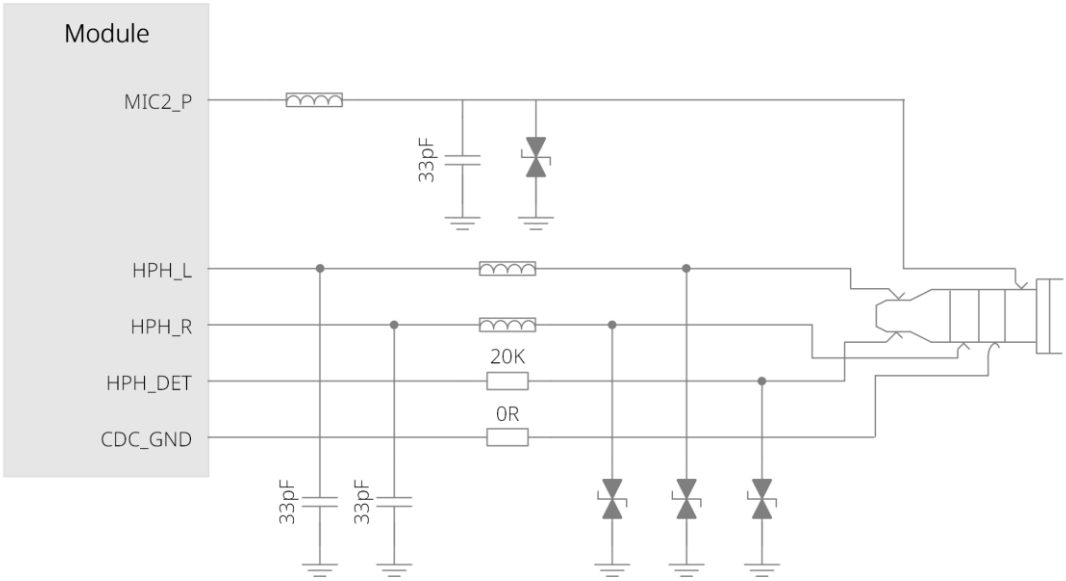

Figure 23. Headphone interface circuit design

Use a bi-directional TVS tube for the ESD protection device of the headphone interface.

3.17 Force Download Interface

The module provides KEY_FORCE_BOOT pin as an emergency download interface.

Connect the KEY_FORCE_BOOT pin with LDO15_1V8 pin when powering on, and the module can enter the emergency download mode, which is used for the final processing mode when the product fails to power on or run normally. To facilitate the subsequent software upgrade and product debugging, please reserve this pin. The reference circuit is as follows:

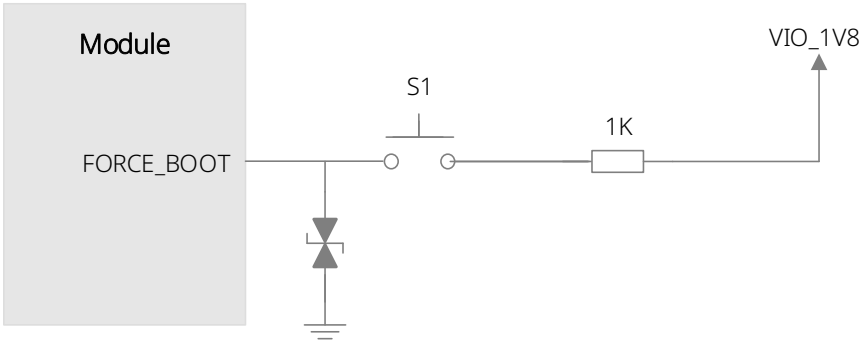

Figure 24. Design of forced download interface

4 Antenna Interface

The module supports 2G/3G/4G main antenna/diversity reception antenna, WIFI/BT antenna and GNSS antenna.

4.1 MAIN/DRX Antenna

The module provides two 2G/3G/4G antenna interfaces. The ANT_MAIN is used to receive and transmit RF signal, and the ANT_DRX is used for diversity reception.

Table 29. MAIN/DRX antenna interface definition

Pin Name	Pin No.	I/O	Description	Remarks
ANT_MAIN	87	AI/AO	2G/3G/4G main antenna interface	--
ANT_DRX	131	AI	4G diversity antenna interface	--

4.1.1 Operating Bands

Table 30. SC126-NA operating band

Mode	Band	TX (MHz)	RX (MHz)
LTE FDD	Band 2	1850-1910	1930-1990
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 12	698-716	728-746
	Band 13	777-787	746-756
	Band 17	704-716	734-746
	Band 25	1850-1915	1930-1995

Mode	Band	TX (MHz)	RX (MHz)
	Band 26	814-849	859-894
	Band 66	1710-1780	2110-2180
	Band 71	663-698	617-652
LTE TDD	Band 41	2496-2690	2496-2690

Table 31. SC126-EAU operating band

Mode	Band	TX (MHz)	RX (MHz)
GSM	850	824-849	869-894
	900	880-915	925-960
	1800	1710-1785	1805-1880
	1900	850-1910	1930-1990
WCDMA	Band 1	1920-1980	2110-2170
	Band 2	1850-1910	1930-1990
	Band 3	1710-1785	1805-1880
	Band 5	824-849	869-894
	Band 8	880-915	925-960
LTE FDD	Band 1	1920-1980	2110-2170
	Band 2	1850-1910	1930-1990
	Band 3	1710-1785	1805-1880
	Band 4	1710-1755	2110-2155
	Band 5	824-849	869-894
	Band 7	2500-2570	2620-2690
	Band 8	880-915	925-960

Mode	Band	TX (MHz)	RX (MHz)
	Band 20	832-862	791-821
	Band 28	703-748	758-803
LTE TDD	Band 38	2570-2620	2570-2620
	Band 40	2300-2400	2300-2400
	Band 41	2496-2690	2496-2690

Table 32. SC126-CN operating band

Mode	Band	TX（MHz）	RX（MHz）
GSM	900	880-915	925-960
	1800	1710-1785	1805-1880
WCDMA	Band 1	1920-1980	2110-2170
	Band 8	880-915	925-960
LTE FDD	Band 1	1920-1980	2110-2170
	Band 3	1710-1785	1805-1880
	Band 5	824-849	869-894
	Band 8	880-915	925-960
LTE TDD	Band 34	2010-2025	2010-2025
	Band 38	2570-2620	2570-2620
	Band 39	1880 – 1920	1880 - 1920
	Band 40	2300-2400	2300-2400
	Band 41	2496-2690	2496-2690

4.1.2 Circuit Reference Design

For use of the module, the antenna pin and the RF connector or antenna feed point on the main board should be connected via an RF route. A microstrip is recommended as the RF cable, the insertion loss must be within 0.2 dB, and the impedance must be 50 Ω. A π-type circuit is reserved between the module and the antenna connector (or feed point) for antenna debugging. Two parallel devices are directly connected across the RF route without branch pulled out. The reference circuit is shown below:

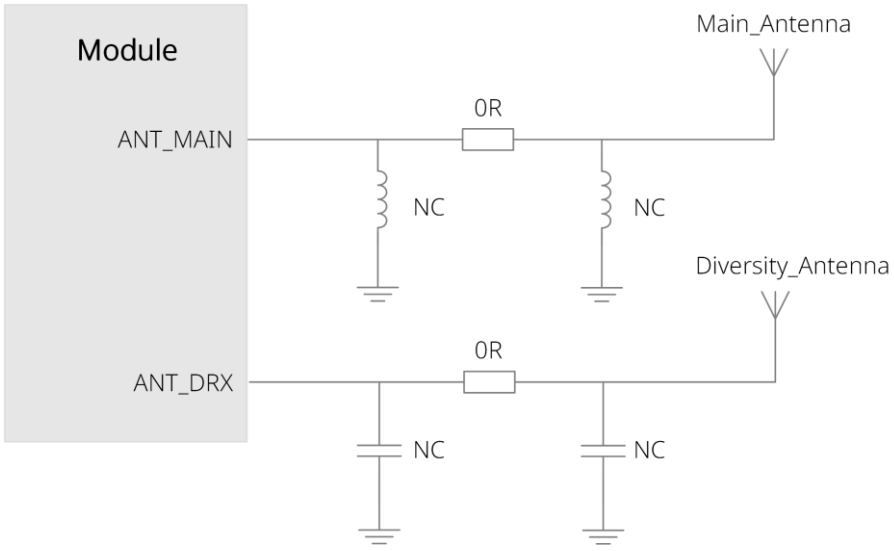

Figure 25. Antenna reference circuit

4.2 WIFI/BT Antenna

Microstrip route is recommended for the WIFI/BT RF route, with insertion loss within 0.2dB and impedance at 50Ω.

Table 33. WIFI/BT antenna interface definition

Pin Name	Pin No.	I/O	Description	Remarks
WIFI/BT_ ANT	77	AI/AO	WIFI/BT antenna interface	--

4.2.1 Operating Bands

Table 34. Operating band

Mode	Frequency	Unit
WIFI	2402 - 2482	MHz
	5170 - 5835	MHz
BT	2402 - 2480	MHz

4.2.2 Circuit Reference Design

The reference circuit of WIFI/BT antenna is shown as follows:

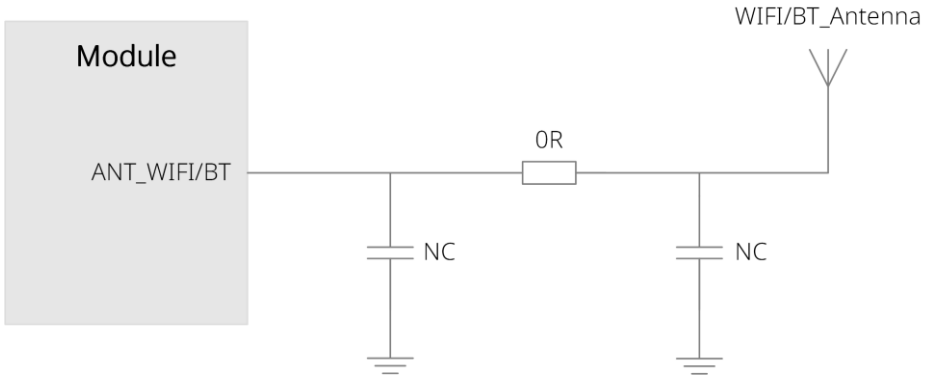

Figure 26. Antenna reference circuit

4.3 GNSS Antenna

GNSS supports GPS, GLONASS, and BeiDou.

Table 35. GNSS antenna interface definition

Pin Name	Pin No.	I/O	Description	Remarks
GNSS_ANT	121	I/O	GNSS antenna interface	--

4.3.1 GNSS operating frequency

Table 36. GNSS operating frequency

Mode	Frequency	Unit
GPS	1575.42±1.023	MHz
GLONASS	1597.42 - 1605.8	MHz
BeiDou	1561.098±2.046	MHz

4.3.2 Circuit Reference Design

The module has a built-in LNA. The passive antenna is used in the design of the device. Microstrip route is recommended for the GNSS RF route, with insertion loss within 0.2dB and impedance at 50Ω. The GNSS antenna reference design is shown as follows:

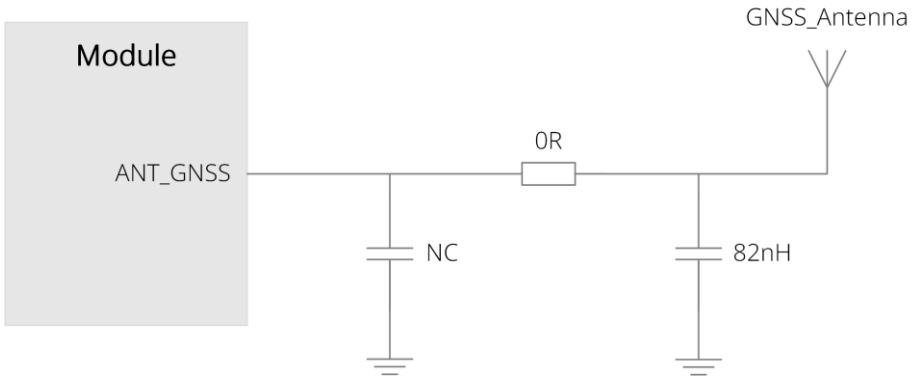

Figure 27. GNSS passive antenna reference circuit

For passive antenna, it is recommended to add a TVS with a junction capacitance of less than 0.5pF; CJ: 0.5pF; clamping voltage: 5.0V. Recommended unit: ESD9D5U.

The active antenna reference circuit is shown in the following figure:

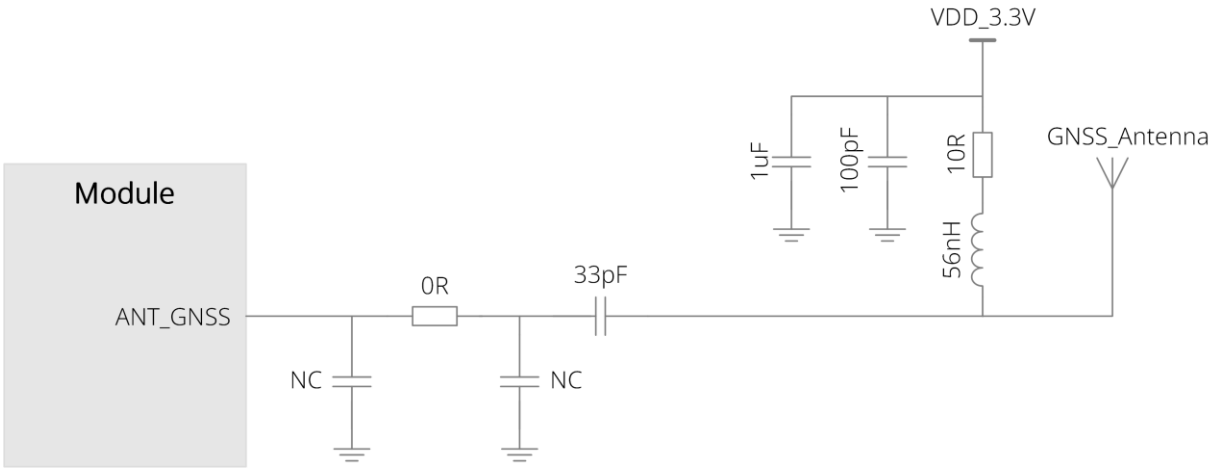

Figure 28. GNSS active antenna connection

The power of the active antenna is fed from the antenna's signal line through a 56nH inductor. Common active antennas supply power is from 3.3-5.0V. The active antenna itself consumes very little power, but requires a stable and clean power supply. It is recommended that a high-PSRR LDO be used to power the antenna.

4.4 Antenna Requirements

The module provides four antenna interfaces: main, diversity, WIFI/BT and GNSS. The antenna requirements are as follows:

Table 37. Antenna requirements

Module Antenna Requirement	
Standard	Antenna Requirement
LTE/WCDMA/GSM	VSWR: < 2 (typical) Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss:< 1dB (0.6-1GHz)

Module Antenna Requirement	
	Insertion loss:< 1.5dB (1.4-2.2GHz) Insertion loss:< 2dB (2.3-2.7GHz)
WIFI/BT	VSWR: ≤ 2 Gain (dBi): 1 Max input power (W): 5 Input impedance (Ω): 50 Polarization type: vertical direction Insertion loss: < 1dB
GNSS	Frequency range: 1559MHz - 1607MHz Polarization type: right-circular or linear polarization VSWR: < 2 (typical) Passive antenna gain: > 0dBi Active antenna NF: < 1.5dB (typical) Active antenna gain: > -2dBi
Isolation between GPS and main antenna	>20dB
Isolation between WIFI and LTE antenna	>20dB

5 RF PCB Layout Design Guide

For user PCB, the characteristic impedance of all RF signal routes should be controlled at 50Ω. In general, the impedance of the RF signal route is determined by the dielectric constant of the material, the route width (W), the ground clearance (S) and the height of the reference ground plane (H). The control of the characteristic impedance of the PCB usually is implemented in two ways: microstrip route and coplanar waveguide. To illustrate the design principles, the following figures show the structural designs of microstrip route and coplanar waveguide when the impedance line is at 50Ω.

- Microstrip cable complete structure

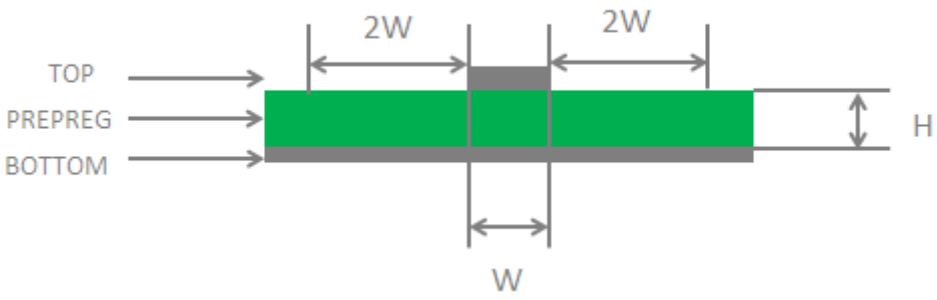

Figure 29. Two-layer PCB microstrip line structure

- Coplanar waveguide complete structure

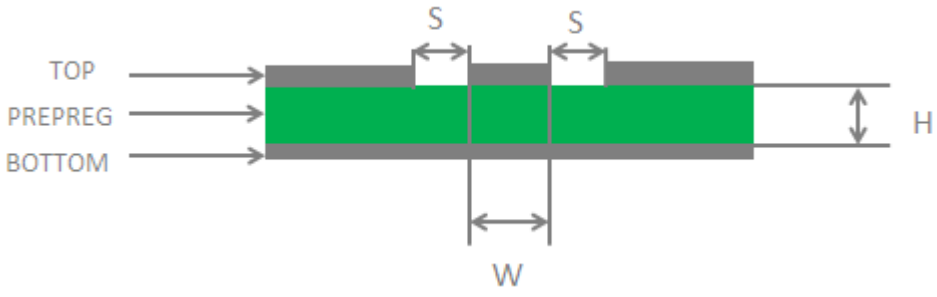

Figure 30. Two-layer PCB coplanar waveguide structure

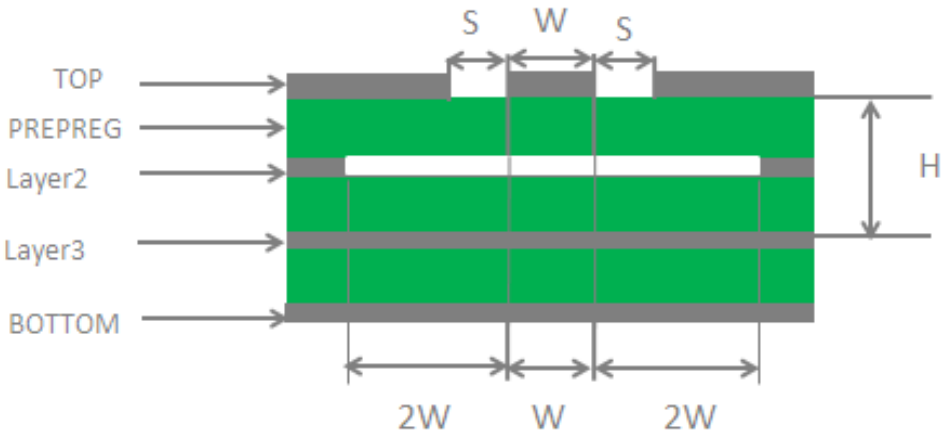

Figure 31 Four-layer PCB coplanar waveguide structure (see ground layer 3)

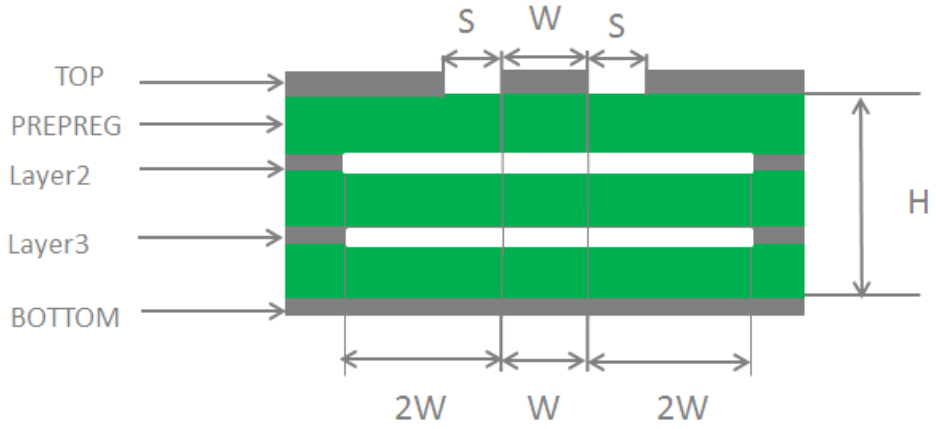

Figure 32. Four-layer PCB coplanar waveguide structure (see ground layer 4)

In the design of RF antenna interface circuit, in order to ensure good performance and reliability of the RF signal, it is recommended to observe the following principles:

Design principles:

- The impedance simulation tool should be used to accurately control the RF signal line at 50Ω impedance.
- The GND pin adjacent to the RF pin should not have thermal welding plate and should be in full contact with the ground.

- The distance between the RF pin and the RF connector should be as short as possible. At the same time, avoid the right-angle route. The recommended route angle is 135 degrees.
- When building connector package, keep the signal pin away from the ground.
- The reference ground plane of the RF signal line should be complete; a certain number of ground holes are added around the signal line and the reference ground to help improve the RF performance;
- and the distance between the ground holes and the signal line should be at least 2 times of the line width (2*W).

6 WIFI and Bluetooth

6.1 WIFI Overview

The module supports 2.4G and 5G WLAN wireless communications and 802.11a, 802.11b, 802.11g, 802.11n, 802.11ac standards, with a maximum rate up to 433Mbps. Its characteristics are as follows:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI
- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0-8 for VHT20
- Support MCS 0-9 for VHT40 and VHT80

6.2 WIFI Performance

Test condition: 3.8V power supply, environment temperature 25°C.

Table 38. WIFI transmitting power

Frequency	Mode	Data Rate	Bandwidth	TX Power (dBm)
2.4G	802.11b	1Mbps	20	17±3
		11Mbps	20	17±3
	802.11g	6Mbps	20	17±3
		54Mbps	20	16±3

Frequency	Mode	Data Rate	Bandwidth	TX Power (dBm)
5G	802.11n	MCS0	20	14±3
		MCS7	20	13±3
		MCS0	40	14±3
		MCS7	40	13±3
	802.11a	6Mbs	20	15±3
		54Mbps	20	14±3
	802.11n	MCS0	20	16±3
		MCS7	20	13±3
		MCS0	40	14±3
		MCS7	40	13±3
	802.11ac	MCS0	20	16±3
		MCS8	20	13±3
		MCS0	40	14±3
		MCS9	40	12±3
		MCS0	80	13±3
		MCS9	80	11±3

Table 39. WIFI receiving sensitivity

Frequency	Mode	Data Rate	Bandwidth (MHz)	Sensitivity (dBm)*
2.4G	802.11b	1Mbps	20	-91
		11Mbps	20	-87
	802.11g	6Mbps	20	-87
		54Mbps	20	-72

Frequency	Mode	Data Rate	Bandwidth (MHz)	Sensitivity (dBm)*
5G	802.11n	MCS0	20	-88
		MCS7	20	-64
		MCS0	40	-86
		MCS7	40	-62
	802.11a	6Mbps	20	-90
		54Mbps	20	-74
	802.11n	MCS0	20	-89
		MCS7	20	-70
		MCS0	40	-86
		MCS7	40	-67
	802.11ac	MCS0	20	-90
		MCS8	20	-67
		MCS0	40	-87
		MCS9	40	-62
		MCS0	80	-83
		MCS9	80	-58

The sensitivity here is a typical value.

6.3 Bluetooth Overview

The module supports BT5.0 (BR/EDR + BLE) standards. The modulation method supports GFSK, 8-DPSK and π/4-DQPSK.BR/EDR. Channel bandwidth is 1MHz and can

accommodate 79 channels. The BLE channel bandwidth is 2MHz and can accommodate 40 channels. Its main features are as follows:

- BT 5.0 + BR/EDR + BLE
- Support for ANT protocol
- Support for BT-WLAN coexistence operation, including optional concurrent receive
- Up to 3.5 piconets (master, slave and page scanning)

Table 40. BT rate and version information

Version	Data Rate	Throughput	Note
BT1.2	1Mbit/s	> 80Kbit/s	--
BT2.0 + EDR	3Mbit/s	> 80Kbit/s	--
BT3.0 + HS	24Mbit/s	Refer to 3.0+HS	--
BT4.2 LE	24Mbit/s	Refer to 4.2 LE	--
BT5.0	24Mbit/s	Refer to 5.0	--

6.4 Bluetooth Performance

Test condition: 3.8V power supply, environment temperature 25°C.

Table 41. BT performance indicators

Type	DH-5	2-DH5	3-DH5	BLE	Unit
Transmitting power	11±2.5	10±2.5	10±2.5	6±2.5	dBm
Receiving sensitivity	-88	TBD	TBD	TBD	dBm

7 GNSS

7.1 Overview

The module supports multiple positioning systems including GPS, GLONASS and BeiDou. The module is embedded with LNA which can effectively improve the sensitivity of GNSS.

7.2 GNSS Performance

Test condition: 3.8V power supply, environment temperature 25°C.

Table 42. GNSS positioning performance

Parameter	Description	Typical Result	Unit
Sensitivity	Acquisition	-157	dBm
	Tracking	-145	dBm
C/No	-130 dBm	39	dB-Hz
TTFF	Cold Start	44	s
	Warm Start	40	s
	Hot Start	2.5	s
CEP	Static accuracy (95% @-130dbm)	5	m

8 Electricity, Reliability and RF Performance

8.1 Recommended Parameters

Table 43. Recommended parameters

Parameter	Min	Normal	Max	Unit
Battery voltage	3.5	3.8	4.4	V
USB_VBUS	4.75	5	5.25	V
RTC voltage	2.45	3.0	3.35	V
Operating temperature	-30	25	75	°C
Storage temperature	-40	25	85	°C

8.2 Operating Current

Test condition: 3.8V power supply, environment temperature 25°C.

Table 44. SC126-NA operating current

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Static leakage current	Leakage current before power on	40	uA
	Normal power-off	Power off leakage current	44	
I_{sleep}	Radio Off	AT+CFUN=4 airplane Mode	8	mA
	TDD LTE	DPC (Default Paging Cycle) = #256	8	

Parameter	Description	Condition	Typical Result	Unit
	FDD LTE	DPC (Default Paging Cycle) = #256	8	
$I_{LTE-RMS}$	FDD data RMS Current	Band2@max power (10MHz,1RB)	774	mA
		Band4@max power (10MHz, 1RB)	773	
		Band5@max power (10MHz, 1RB)	850	
		Band7@max power (10MHz, 1RB)	830	
		Band12@max power (10MHz, 1RB)	900	
		Band13@max power (10MHz, 1RB)	990	
		Band17@max power (10MHz, 1RB)	TBD	
		Band25@max power (10MHz, 1RB)	780	
		Band26@max power (10MHz, 1RB)	TBD	
		Band66@max power (10MHz, 1RB)	845	
		Band71@max power (10MHz, 1RB)	TBD	

Parameter	Description	Condition	Typical Result	Unit
	TDD data RMS Current	Band41@max power (10MHz,1RB)	500	mA

Table 45. SC126-EAU operating current

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Static leakage current	Leakage current before power on	40	uA
	Normal power-off	Power off leakage current	44	
I_{sleep}	Radio Off	AT+CFUN=4 airplane Mode	8	mA
	GSM	MFRMS=5	8	
	WCDMA	DRX=8	8	
	TDD LTE	DPC (Default Paging Cycle)=#256	8	
	FDD LTE	DPC (Default Paging Cycle)=#256	8	
$I_{GSM-RMS}$	GSM voice RMS Current	GSM850@ PCL=5	249	mA
		GSM850@ PCL=19	90	
		EGSM900@ PCL=5	254	
		EGSM900@ PCL=19	90	
		DCS1800@ PCL=0	210	
		DCS1800@ PCL=15	90	
		PCS1900@ PCL=0	210	

Parameter	Description	Condition	Typical Result	Unit
		PCS1900@ PCL=15	90	
$I_{GSM-MAX}$	GSM voice Peak current	GSM850@ PCL=5	2400	mA
		EGSM900@ PCL=5	2400	
		DCS1800@ PCL=0	1700	
		DCS1900@ PCL=0	1700	
$I_{GPRS-RMS}$	GPRS data RMS Current	GSM850@ Gamma=3(1UL/4DL)	246	
		GSM850@ Gamma=3(4UL/1DL)	640	
		EGSM900@ Gamma=3(1UL/4DL)	245	
		EGSM900@ Gamma=3(4UL/1DL)	631	
		DCS1800@ Gamma=3(1UL/4DL)	190	
		DCS1800@ Gamma=3(4UL/1DL)	500	
		PCS1900@ Gamma=3(1UL/4DL)	170	
		PCS1900@ Gamma=3(4UL/1DL)	500	
$I_{EGPRS-RMS}$	EGPRS data RMS Current	GSM850@ Gamma=6(1UL/4DL)	180	mA
		GSM850@ Gamma=6(4UL/1DL)	446	
		EGSM900@ Gamma=6(1UL/4DL)	180	

Parameter	Description	Condition	Typical Result	Unit
		EGSM900@ Gamma=6(4UL/1DL)	430	
		DCS1800@ Gamma=5(1UL/4DL)	170	
		DCS1800@ Gamma=5(4UL/1DL)	500	
		PCS1900@ Gamma=5(1UL/4DL)	200	
		PCS1900@ Gamma=5(4UL/1DL)	510	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band1@ max power	597	mA
		Band2@ max power	585	
		Band3@ max power	569	
		Band5@ max power	686	
		Band8@ max power	670	
$I_{LTE-RMS}$	FDD data RMS Current	Band1@ max power(10MHz,1RB)	695	mA
		Band2@ max power(10MHz,1RB)	622	
		Band3@ max power(10MHz,1RB)	690	
		Band4@ max power(10MHz,1RB)	675	
		Band5@ max	640	

Parameter	Description	Condition		Typical Result	Unit
		power(10MHz,1RB)			
		Band7@ power(10MHz,1RB)	max	720	
		Band8@ power(10MHz,1RB)	max	604	
		Band20@ power(10MHz,1RB)	max	600	
		Band28@ power(10MHz,1RB)	max	614	
	TDD data RMS Current	Band38@ power(10MHz,1RB)	max	348	mA
		Band40@ power(10MHz,1RB)	max	378	
		Band41@ power(10MHz,1RB)	max	396	

Table 46. SC126-CN operating current

Parameter	Description	Condition	Typical Result	Unit
I_{off}	Static leakage current	Leakage current before power on	40	uA
	Normal power-off	Power off leakage current	44	
I_{sleep}	Radio Off	AT+CFUN=4 airplane Mode	8	mA
	GSM	MFRMS=5	7	
	WCDMA	DRX=8	8	

Parameter	Description	Condition	Typical Result	Unit
	TDD LTE	DPC (Default Paging Cycle)=#256	8	
	FDD LTE	DPC (Default Paging Cycle)=#256	8	
$I_{GSM-RMS}$	GSM voice RMS Current	EGSM900@ PCL=5	254	mA
		EGSM900@ PCL=19	90	
		DCS1800@ PCL=0	210	
		DCS1800@ PCL=15	90	
$I_{GSM-MAX}$	GSM voice Peak current	EGSM900@ PCL=5	2400	mA
		DCS1800@ PCL=0	1700	
$I_{GPRS-RMS}$	GPRS data RMS Current	EGSM900@ Gamma=3(1UL/4DL)	245	
		EGSM900@ Gamma=3(4UL/1DL)	631	
		DCS1800@ Gamma=3(1UL/4DL)	190	
		DCS1800@ Gamma=3(4UL/1DL)	500	
$I_{EGPRS-RMS}$	EGPRS data RMS Current	EGSM900@ Gamma=6(1UL/4DL)	180	mA
		EGSM900@ Gamma=6(4UL/1DL)	430	
		DCS1800@	170	

Parameter	Description	Condition		Typical Result	Unit
		Gamma=5(1UL/4DL)			
		DCS1800@ Gamma=5(4UL/1DL)		500	
$I_{WCDMA-RMS}$	WCDMA RMS Current	Band1@ max power		597	mA
		Band8@ max power		670	
$I_{LTE-RMS}$	FDD data RMS Current	Band1@ power(10MHz,1RB)	max	695	mA
		Band3@ power(10MHz,1RB)	max	690	
		Band5@ power(10MHz,1RB)	max	640	
		Band8@ power(10MHz,1RB)	max	604	
	TDD data RMS Current	Band34@ power(10MHz,1RB)	max	365	
		Band38@ power(10MHz,1RB)	max	348	mA
		Band39@ power(10MHz,1RB)	max	368	
		Band40@ power(10MHz,1RB)	max	378	
		Band41@ power(10MHz,1RB)	max	396	

8.3 RF Transmit Power

The transmit power of each band of the module is shown in the following table:

Test condition: 3.8V power supply, environment temperature 25°C, LTE power test performed with 12MHz bandwidth.

Table 47. RF transmitting power

Mode	Band	Max Power (dBm)	Min Power (dBm)
GSM	850 (GMSK)	33±2	5±5
	900 (GMSK)	33±2	5±5
	1800 (GMSK)	30±2	0±5
	1900 (GMSK)	30±2	0±5
	850 (8PSK)	27.0±3	5±5
	900 (8PSK)	27.0±3	5±5
	1800 (8PSK)	26.0±3	0±5
	1900 (8PSK)	26.0±3	0±5
WCDMA	Band 1	24+1/-3	<-49
	Band 2	24+1/-3	<-49
	Band 3	24+1/-3	<-49
	Band 5	24+1/-3	<-49
	Band 8	24+1/-3	<-49
LTE FDD	Band 1	23.0±2	<-39
	Band 2	23.0±2	<-39
	Band 3	23.0±2	<-39
	Band 4	23.0±2	<-39
	Band 5	23.0±2	<-39

Mode	Band	Max Power (dBm)	Min Power (dBm)
	Band 7	23.0±2	<-39
	Band 8	23.0±2	<-39
	Band 12	23.0±2	<-39
	Band 13	23.0±2	<-39
	Band 17	23.0±2	<-39
	Band 20	23.0±2	<-39
	Band 25	23.0±2	<-39
	Band 26	23.0±2	<-39
	Band 28	23.0±2	<-39
	Band 66	23.0±2	<-39
	Band 71	23.0±2	<-39
LTE TDD	Band 34	23.0±2	<-39
	Band 38	23.0±2	<-39
	Band 39	23.0±2	<-39
	Band 40	23.0±2	<-39
	Band 41	23.0±2	<-39

8.4 RF Receiver Sensitivity

The sensitivity of each frequency band of the module is shown in the following table:

Test condition: 3.8V power supply, environment temperature 25°C, LTE power test performed with 10MHz bandwidth. For RB configuration, see 3GPP standard.

Table 48. SC126-NA RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit

Mode	Band	Primary	Diversity	PRX + Div	3GPP Requirement	Unit
LTE FDD	Band 2	-99.2	-99.4	-101.7	-94.3	dBm
	Band 4	-97.4	-98.8	-99.9	-96.3	dBm
	Band 5	-99.8	-99.6	-102.1	-94.3	dBm
	Band 7	-98	-99.6	-100.5	-94.3	dBm
	Band 12	-99.2	-99	-101.5	-93.3	dBm
	Band 13	-98.6	-98.5	-101	-93.3	dBm
	Band 17	-99.2	-99.2	-101.7	-93.3	dBm
	Band 25	-99.2	-99.1	-101.6	-92.8	dBm
	Band 26	-99.8	-99.8	-103.3	-93.8	dBm
	Band 66	-97.8	-99	-100.3	-95.8	dBm
	Band 71	-99.3	-98.8	-101.3	-93.5	dBm
LTE TDD	Band 41	-96.1	-97.2	-98.6	-94.3	dBm

Table 49. SC126-EAU RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX+Div	3GPP Requirement	Unit
GSM	850	-107.8	-	-	-102	dBm
	900	-109.2	-	-	-102	dBm
	1800	-107.9	-	-	-102	dBm
	1900	-106.6	-	-	-102	dBm
WCDMA	Band 1	-107.4	-	-	-106.7	dBm
	Band 2	-108.2	-	-	-104.7	dBm
	Band 3	-109.5	-	-	-103.7	dBm
	Band 5	-108.4	-	-	-104.7	dBm

	Band 8	-109.9	-	-	-103.7	dBm
LTE FDD	Band 1	-96.5	-97.7	-99	-96.3	dBm
	Band 2	-96.4	-97.9	-98.9	-94.3	dBm
	Band 3	-97.5	-97.8	-100	-93.3	dBm
	Band 4	-96.7	-97.7	-99.2	-96.3	dBm
	Band 5	-97.5	-98.7	-100	-94.3	dBm
	Band 7	-95.6	-97.3	-98.1	-94.3	dBm
	Band 8	-98.5	-99	-101	-93.3	dBm
	Band 20	-97.8	-97.8	-99.3	-93.3	dBm
	Band 28	-97	-98	-99.5	-94.8	dBm
LTE TDD	Band 38	-96.3	-96.6	-98.8	-96.3	dBm
	Band 40	-96.3	-97.8	-98.8	-96.3	dBm
	Band 41	-94.3	-96.7	-96.8	-94.3	dBm

Table 50. SC126-CN RF receiving sensitivity

Mode	Band	Primary	Diversity	PRX+Div	3GPP Requirement	Unit
GSM	900	-109.2	-	-	-102	dBm
	1800	-107.9	-	-	-102	dBm
WCDMA	Band 1	-107.4	-	-	-106.7	dBm
	Band 8	-109.9	-	-	-103.7	dBm
LTE FDD	Band 1	-96.5	-97.7	-99	-96.3	dBm
	Band 3	-97.5	-97.8	-100	-93.3	dBm
	Band 5	-97.5	-98.7	-100	-94.3	dBm
	Band 8	-98.5	-99	-101	-93.3	dBm

	Band 34	-96.7	-96.8	-99.2	-96.3	dBm
	Band 38	-96.3	-96.6	-98.8	-96.3	dBm
LTE TDD	Band 39	-97.2	-97.3	-99.7	-96.3	dBm
	Band 40	-96.3	-97.8	-98.8	-96.3	dBm
	Band 41	-94.3	-96.7	-96.8	-94.3	dBm

8.5 Electrostatic Protection

In the application of the module, static electricity generated by human body and static electricity generated by friction between micro-electronics are discharged to the module through various channels and may cause damage to the module. Therefore, ESD protection should be taken seriously. In the process of R&D, production assembly and testing, especially in product design, ESD protection measures should be taken. For example, ESD protection should be added at the designed circuit interfaces and at the points susceptible to electrostatic discharge or impact. Anti-static gloves should be worn during production.

The following table lists ESD performance parameters (Temperature: 25°C, Humidity: 45%–65%):

Table 51. ESD performance

Test Point	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	KV
Antenna Interface	±5	±10	KV
Other interfaces	±0.5	±1	KV

9 Structure Specifications

9.1 Product Appearance

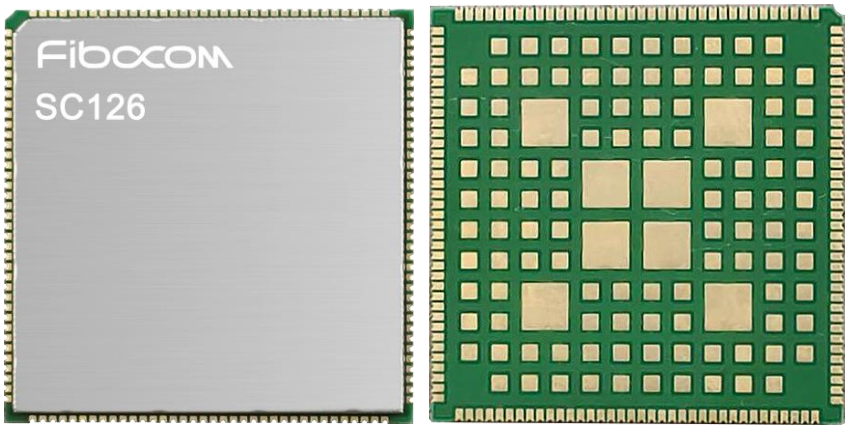

Figure 33. Product appearance

9.2 Structural Dimensions

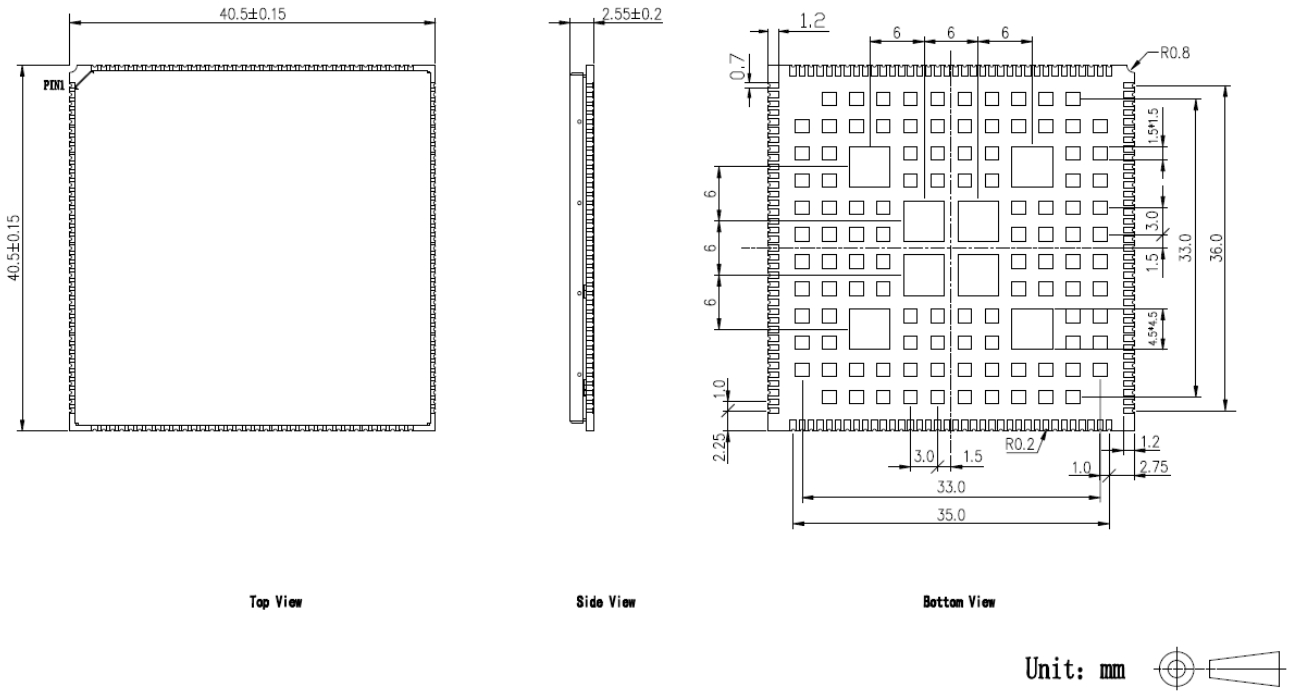

Figure 34. Structural dimensions

9.3 Recommended PCB Soldering Pad Design

For PCB soldering pad and stencil design, please refer to *Fibocom_SC126_SMT Design Guide*.

9.4 Recommended Thermal Design

For recommended module and peripheral thermal design, see *Fibocom_SC126_Thermal Design Guide*.

10 Production and Storage

10.1 SMT

See *Fibocom_SC126_SMT Design Guide*.

10.2 Packaging and Storage

See *Fibocom_SC126_SMT Design Guide*.

11 Regulatory statement

11.1 FCC Regulatory Compliance

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).

3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations.

4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting, and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Fibocom wires Inc. that they wish

to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: ZMOSC126NA”.

The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,

(2) The transmitter module may not be co-located with any other transmitter or antenna.

(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	Bands	Peak Gain
Dipole	LTE B2	4.0 dBi
Dipole	LTE B4	3.0 dBi
Dipole	LTE B5	3.0 dBi
Dipole	LTE B7	4.0 dBi
Dipole	LTE B12	3.0 dBi
Dipole	LTE B13	3.0 dBi
Dipole	LTE B17	3.0 dBi
Dipole	LTE B25	4.0 dBi
Dipole	LTE B26	3.0 dBi
Dipole	LTE B66	3.0 dBi
Dipole	LTE B71	3.0 dBi
Dipole	LTE B41	4.0 dBi

Antenna type	Bands	Peak Gain
Dipole	BT/WIFI 2.4G	1.83 dBi
Dipole	U-NII-1	4.29 dBi
Dipole	U-NII-2A	4.43 dBi
Dipole	U-NII-2C	3.68 dBi
Dipole	U-NII-3	1.47 dBi

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.

- Increase the separation between the equipment and receiver

- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.

- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15, part 22, part 24, part 27, part 90 requirements for Modular Approval.

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and

2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

11.2 Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:

(1) This device may not cause interference; and

(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such

that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC:21374-SC126NA”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante:
"Contient des IC: 21374-SC126NA".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module. Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Appendix A Acronyms and Abbreviations

Table 52. Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-rate
bps	Bits Per Second
CS	Coding Scheme
DRX	Discontinuous Reception
FDD	Frequency Division Duplexing
GMSK	Gaussian Minimum Shift Keying
HSDPA	High Speed Down Link Packet Access
IMEI	International Mobile Equipment Identity
Imax	Maximum Load Current
LED	Light Emitting Diode
LSB	Least Significant Bit
LTE	Long Term Evolution
ME	Mobile Equipment
MS	Mobile Station
MT	Mobile Terminated
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying

Abbreviation	Description
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized RMS
RMS	Root Mean Square
RTC	Real Time Clock
Rx	Receive
SMS	Short Message Service
TDMA	Time Division Multiple Access
TE	Terminal Equipment
TX	Transmitting Direction
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver & Transmitter
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USSD	Unstructured Supplementary Service Data
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
VIHmax	Maximum Input High Level Voltage Value
VIHmin	Minimum Input High Level Voltage Value
VILmax	Maximum Input Low Level Voltage Value
VILmin	Minimum Input Low Level Voltage Value
VImax	Absolute Maximum Input Voltage Value

Abbreviation	Description
VImin	Absolute Minimum Input Voltage Value
VOHmax	Maximum Output High Level Voltage Value
VOHmin	Minimum Output High Level Voltage Value
VOLmax	Maximum Output Low Level Voltage Value
VOLmin	Minimum Output Low Level Voltage Value
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Appendix B GPRS Encoding Scheme

Table 53. GPRS encoding scheme

Encoding Method	CS-1	CS-2	CS-3	CS-4
Rate	1/2	2/3	3/4	1
USF	3	3	3	3
Pre-coded USF	3	6	6	12
Radio Block excl. USF and BCS	181	268	312	428
BCS	40	16	16	16
Tail	4	4	4	-
Coded Bits	456	588	676	456
Punctured Bits	0	132	220	-
Data Rate Kb/s	9.05	13.4	15.6	21.4

Appendix C GPRS Multi-timeslot

In the GPRS standard, 29 types of GPRS multi-timeslot modes are defined for mobile stations. The multi-timeslot class defines the maximum uplink and downlink rates, represented by 3+1 or 2+2. The first number represents the number of downlink timeslots and the second number represents the number of uplink timeslots. Active timeslot represents the total number of timeslots that the GPRS device can use for both uplink and downlink communications at the same time.

Table 54. Multislot allocation of different classes

Multislot Class	Downlink Slots	Uplink Slots	Active Slots
1	1	1	2
2	2	1	3
3	2	2	3
4	3	1	4
5	2	2	4
6	3	2	4
7	3	3	4
8	4	1	5
9	3	2	5
10	4	2	5
11	4	3	5
12	4	4	5
33	5	4	6

Appendix D EDGE Modulation and Encoding Method

Table 55. EDGE modulation and encoding method

Coding Scheme	Modulation	Coding Family	1 Timeslot	2 Timeslot	4 Timeslot
CS-1	GMSK	/	9.05kbit/s	18.1kbit/s	36.2kbit/s
CS-2	GMSK	/	13.4kbit/s	26.8kbit/s	53.6kbit/s
CS-3	GMSK	/	15.6kbit/s	31.2kbit/s	62.4kbit/s
CS-4	GMSK	/	21.4kbit/s	42.8kbit/s	85.6kbit/s
MCS-1	GMSK	C	8.80kbit/s	17.6kbit/s	35.2kbit/s
MCS-2	GMSK	B	11.2kbit/s	22.4kbit/s	44.8kbit/s
MCS-3	GMSK	A	14.8kbit/s	29.6kbit/s	59.2kbit/s
MCS-4	GMSK	C	17.6kbit/s	35.2kbit/s	70.4kbit/s
MCS-5	8-PSK	B	22.4kbit/s	44.8kbit/s	89.6kbit/s
MCS-6	8-PSK	A	29.6kbit/s	59.2kbit/s	118.4kbit/s
MCS-7	8-PSK	B	44.8kbit/s	89.6kbit/s	179.2kbit/s
MCS-8	8-PSK	A	54.4kbit/s	108.8kbit/s	217.6kbit/s
MCS-9	8-PSK	A	59.2kbit/s	118.4kbit/s	236.8kbit/s