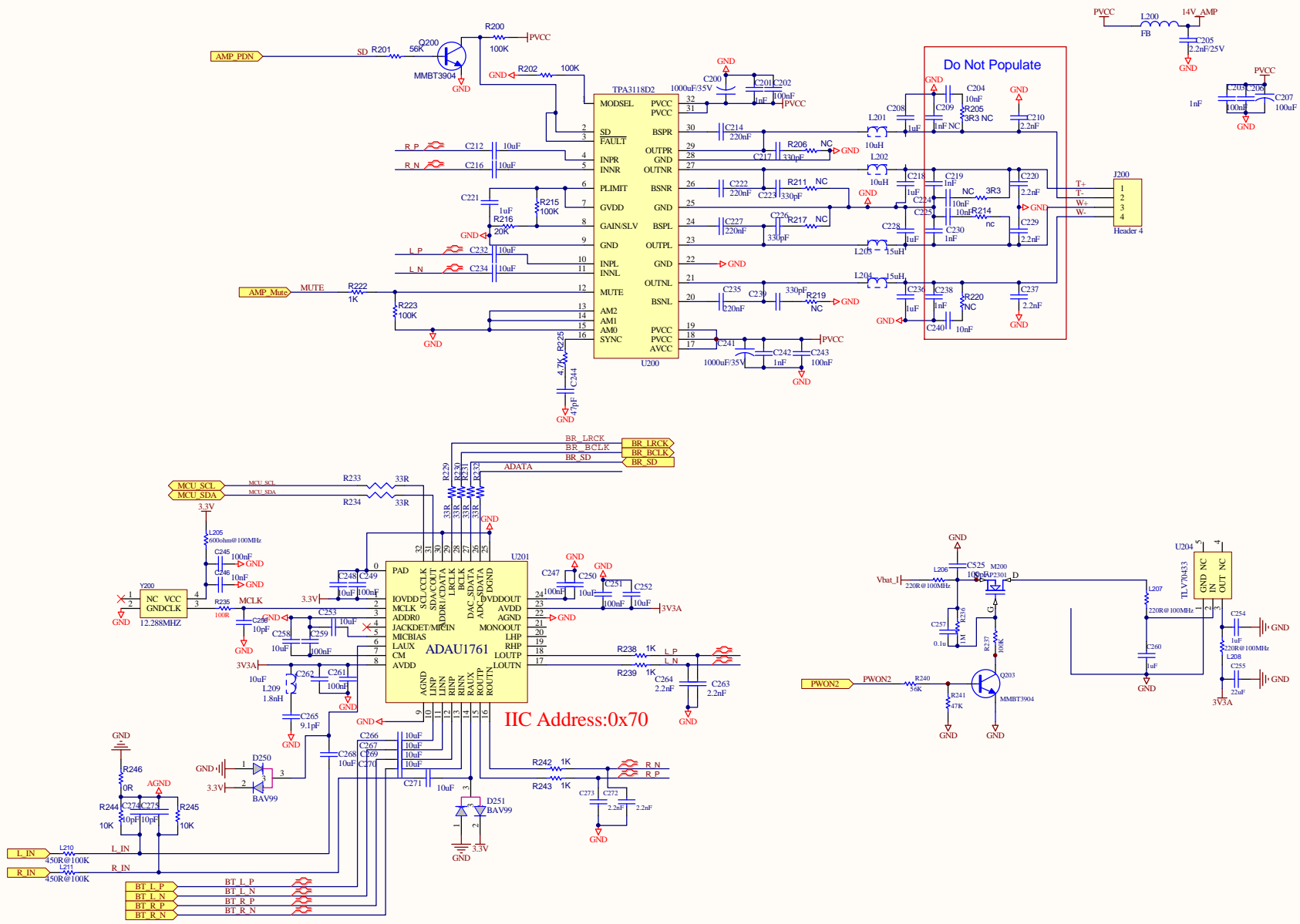
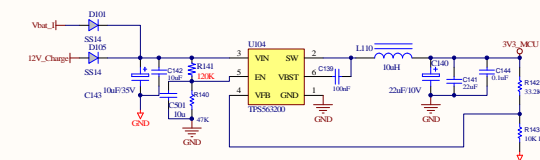
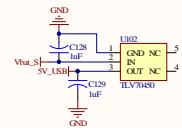
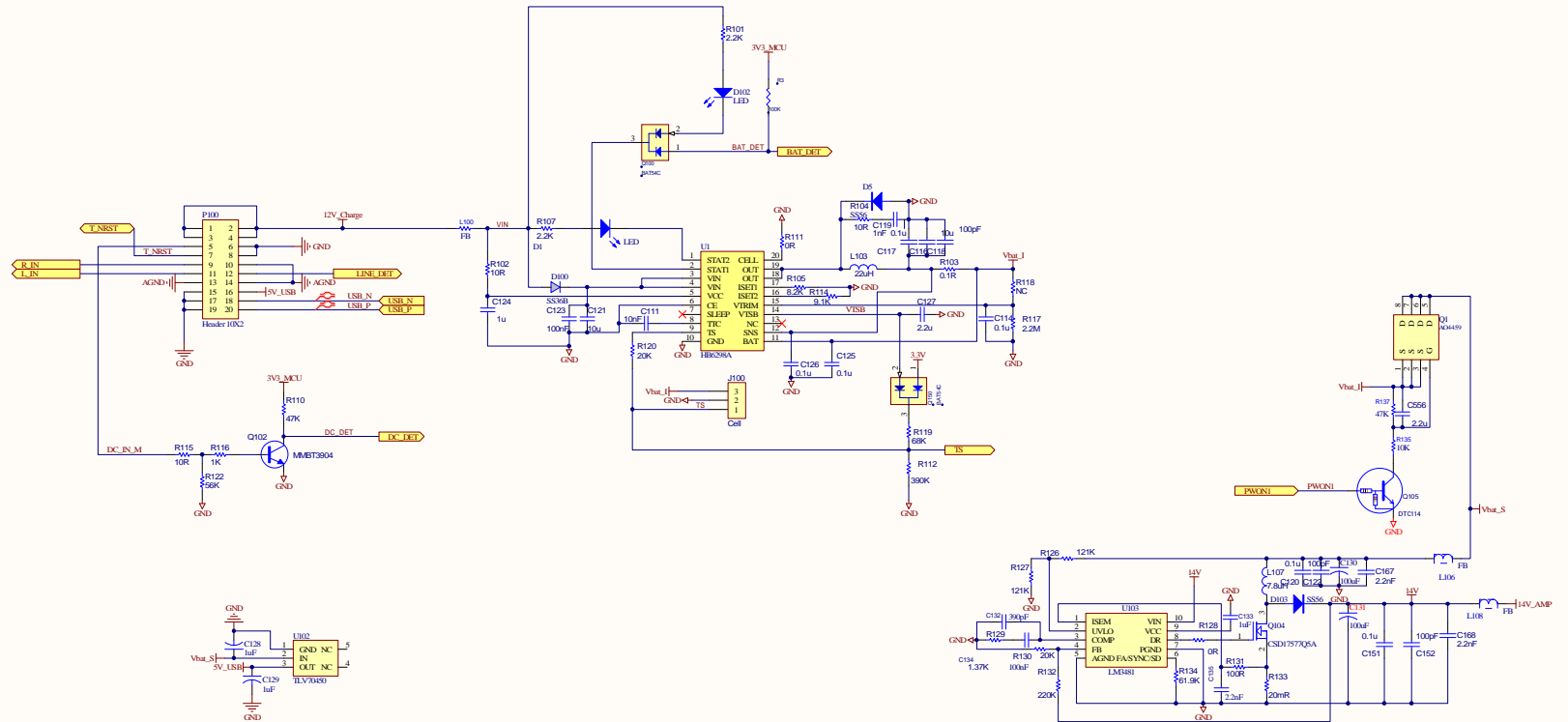


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Date:	2015-7-16	Sheet of
File:	D:\Project\...\Signal flowchart.SchDoc	Drawn By:



REV.	ECN No.	DESCRIPTION	Date	APPRO

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 Document Number: Mos audio-AMP Vm10.schdoc Sheet:
 Project: State:
 Drawn by: PL Checked: HW Manager Checked: R&D Director Approved:
 Date: Date: Date: Date:



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Document Number: MOS_AUDIO-power_Vm10.schdoc

Project: Musicbox XS

Drawn by: Gary

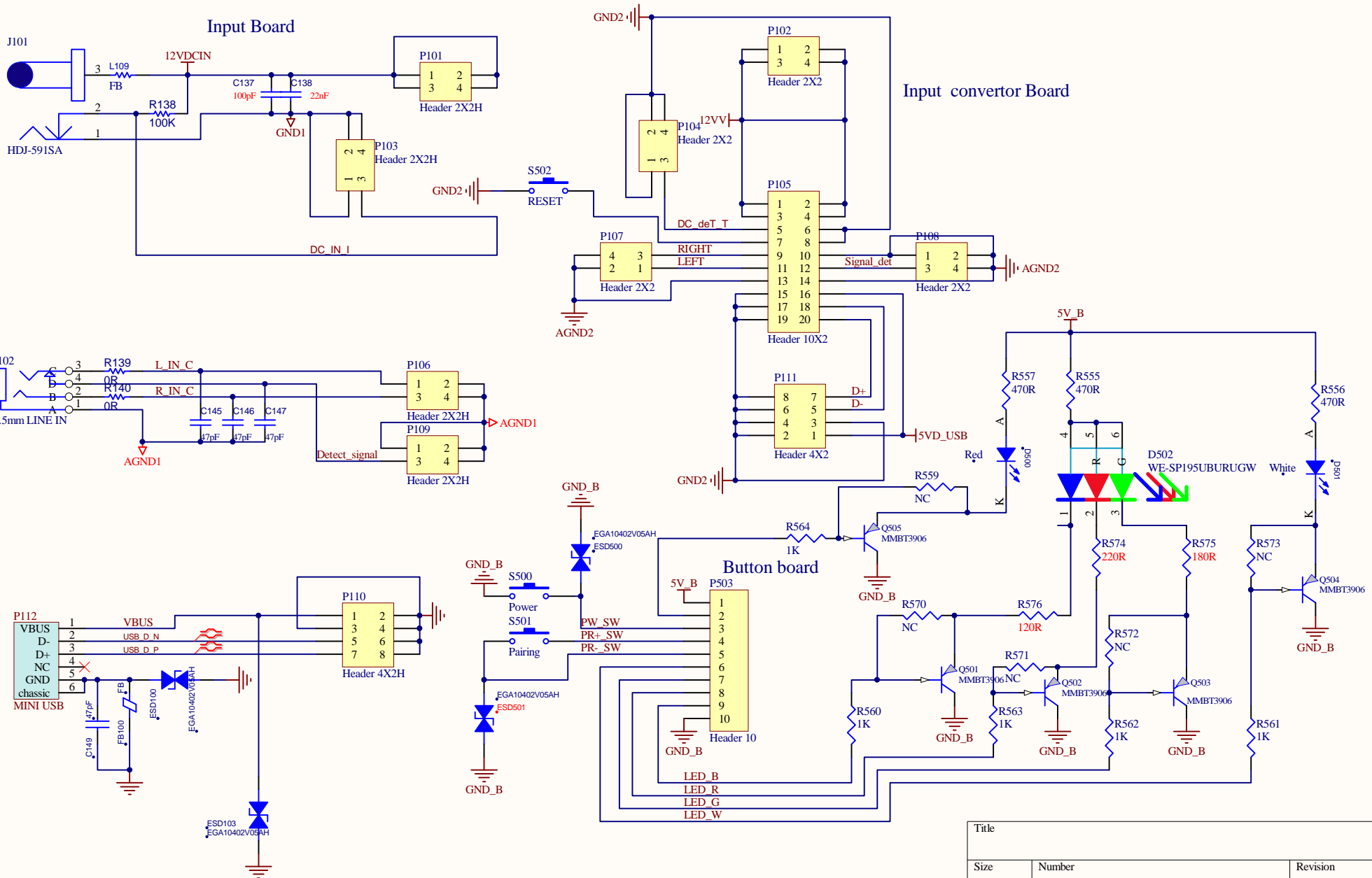
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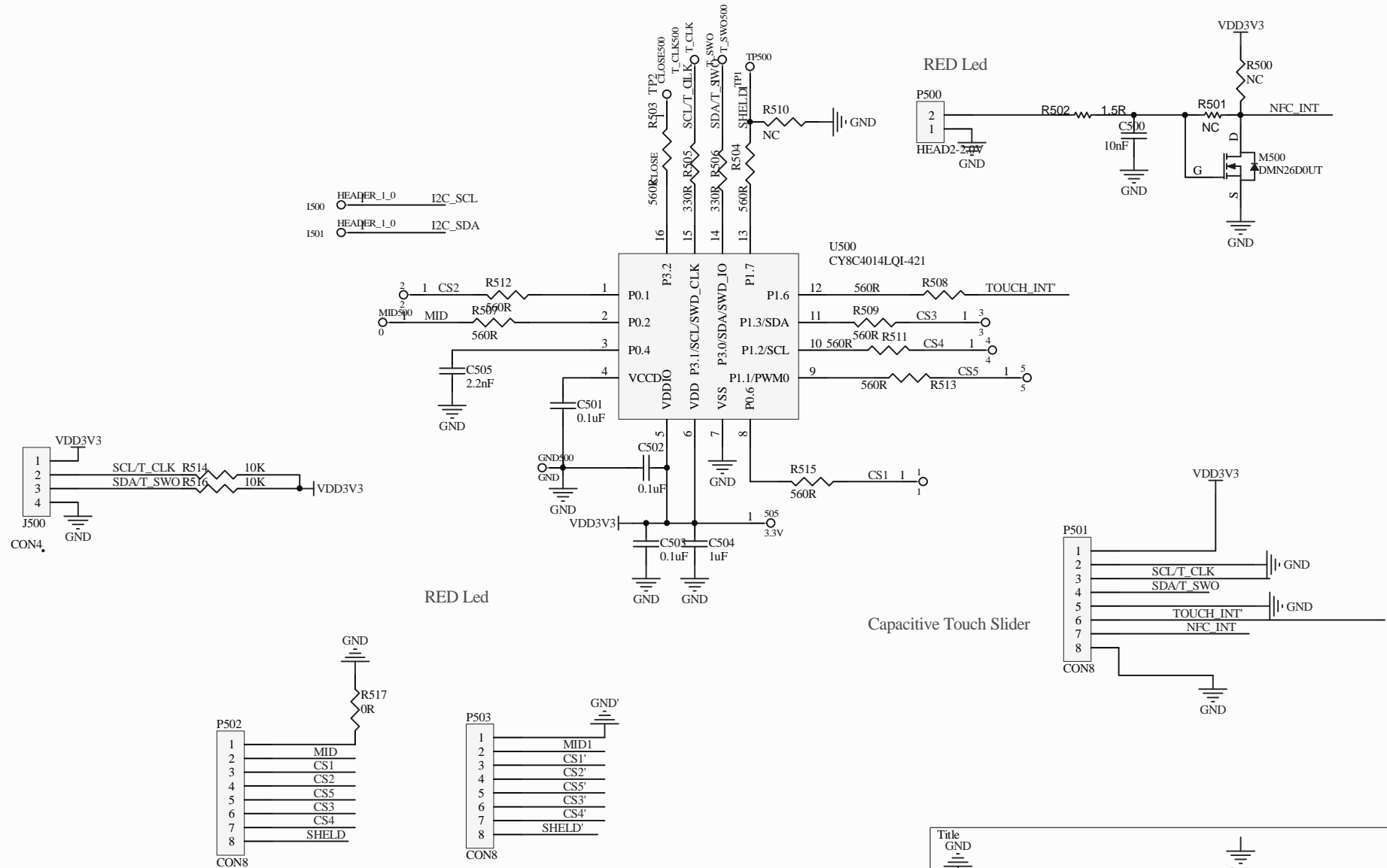
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R&D Director Approved by:

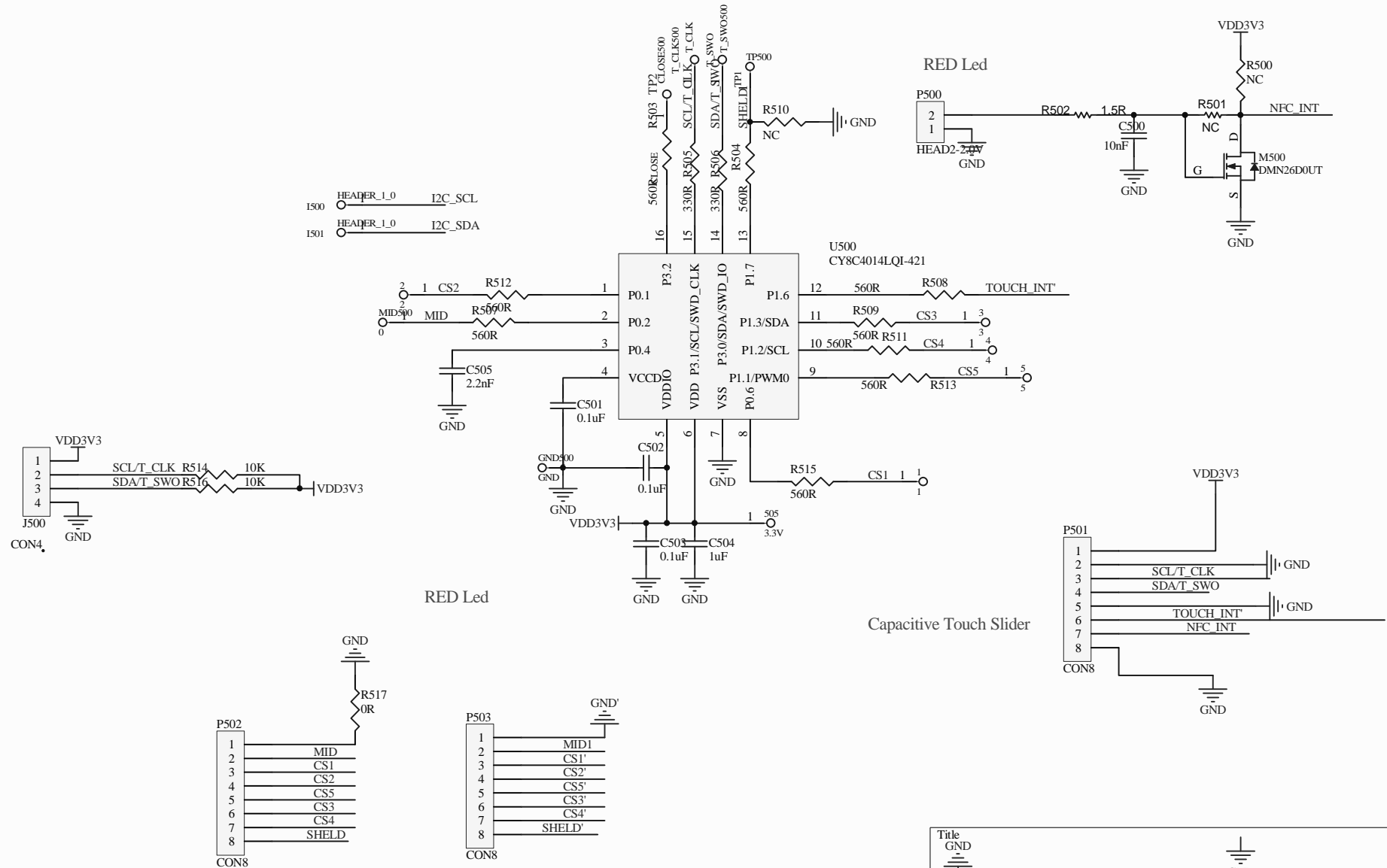
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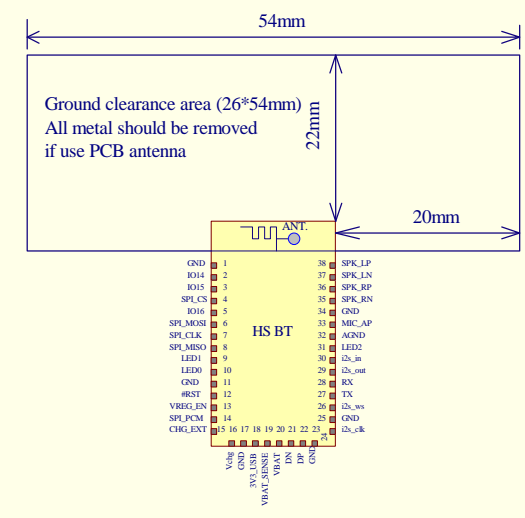
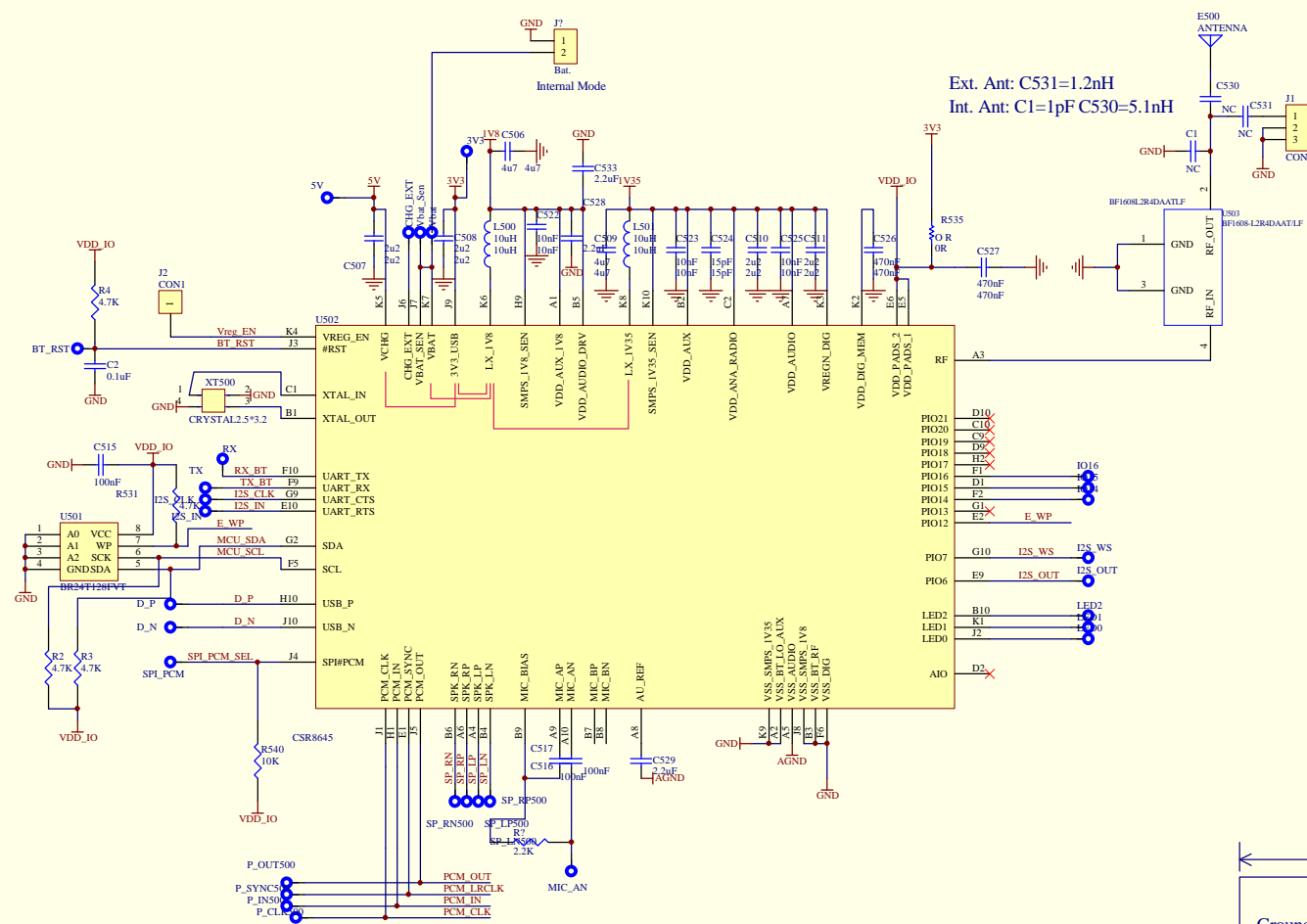
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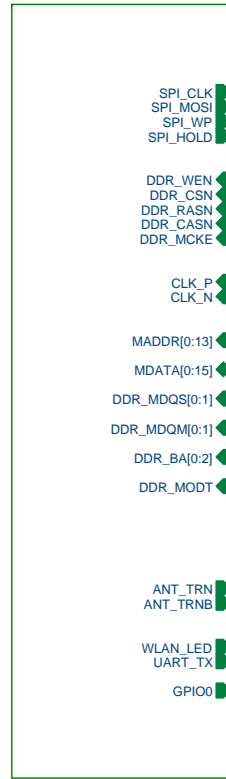


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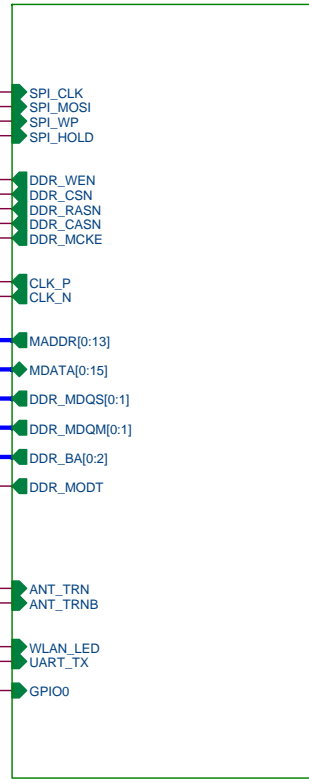
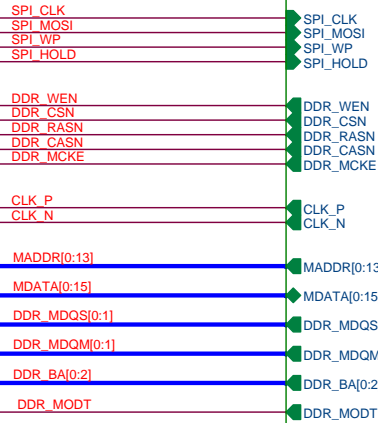


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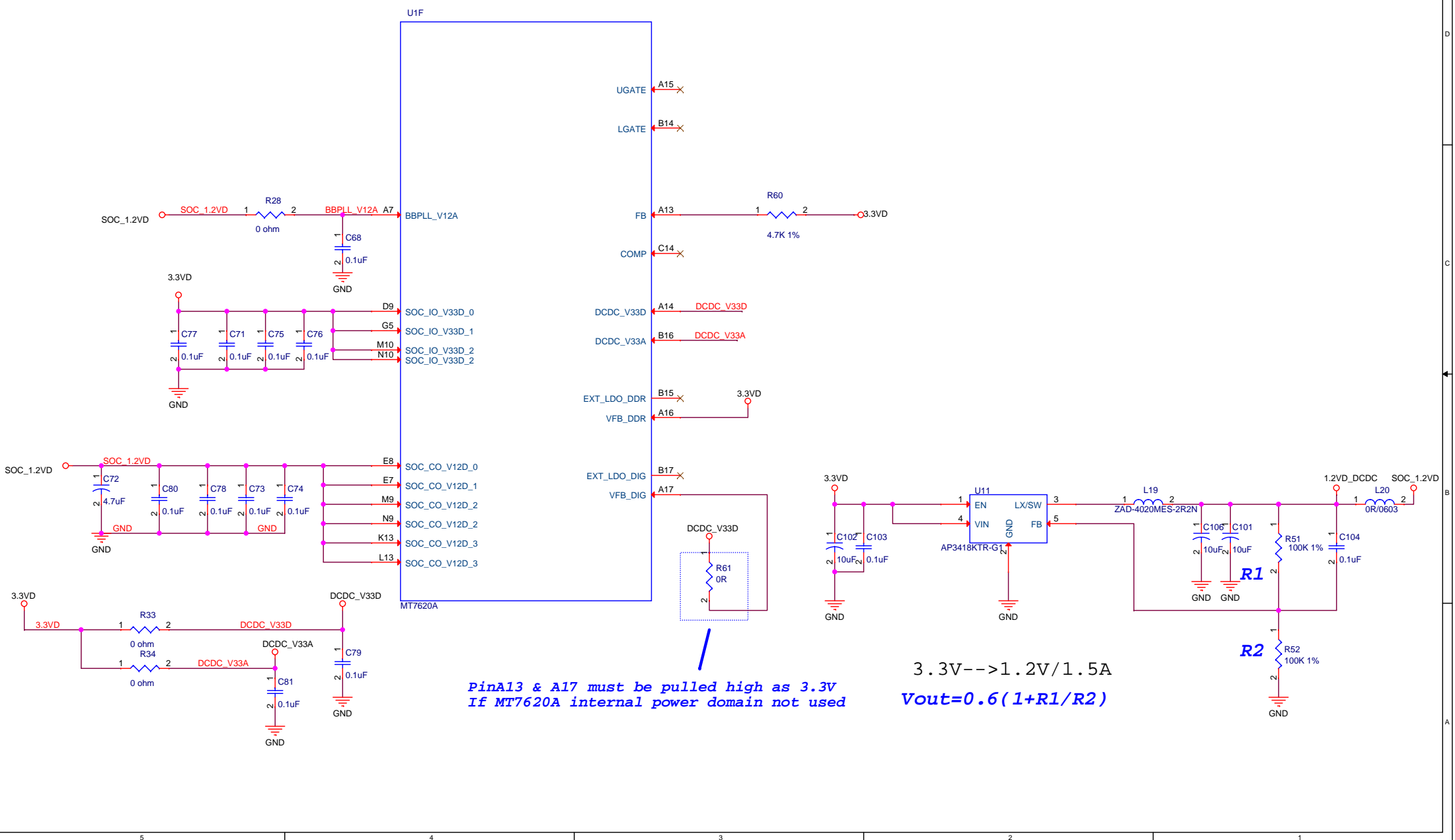
2-MEMORY



2-MEMORY

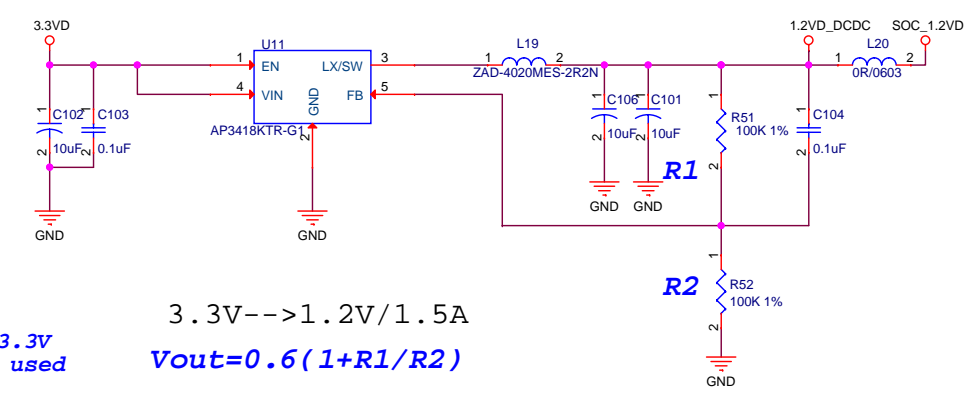
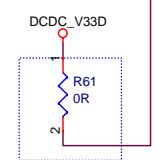


1-CPU-MT7620A

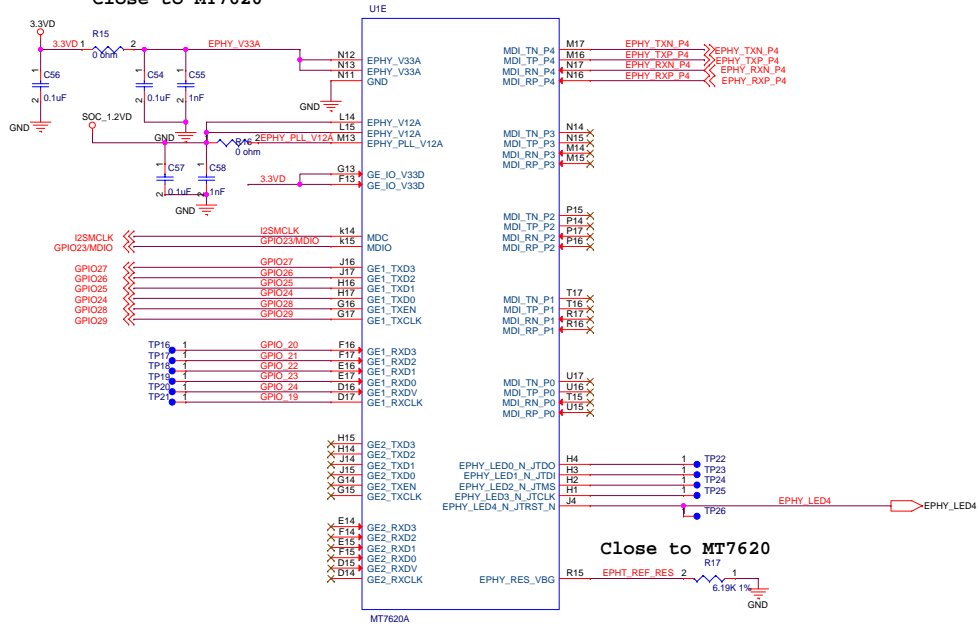


*PinA13 & A17 must be pulled high as 3.3V
If MT7620A internal power domain not used*

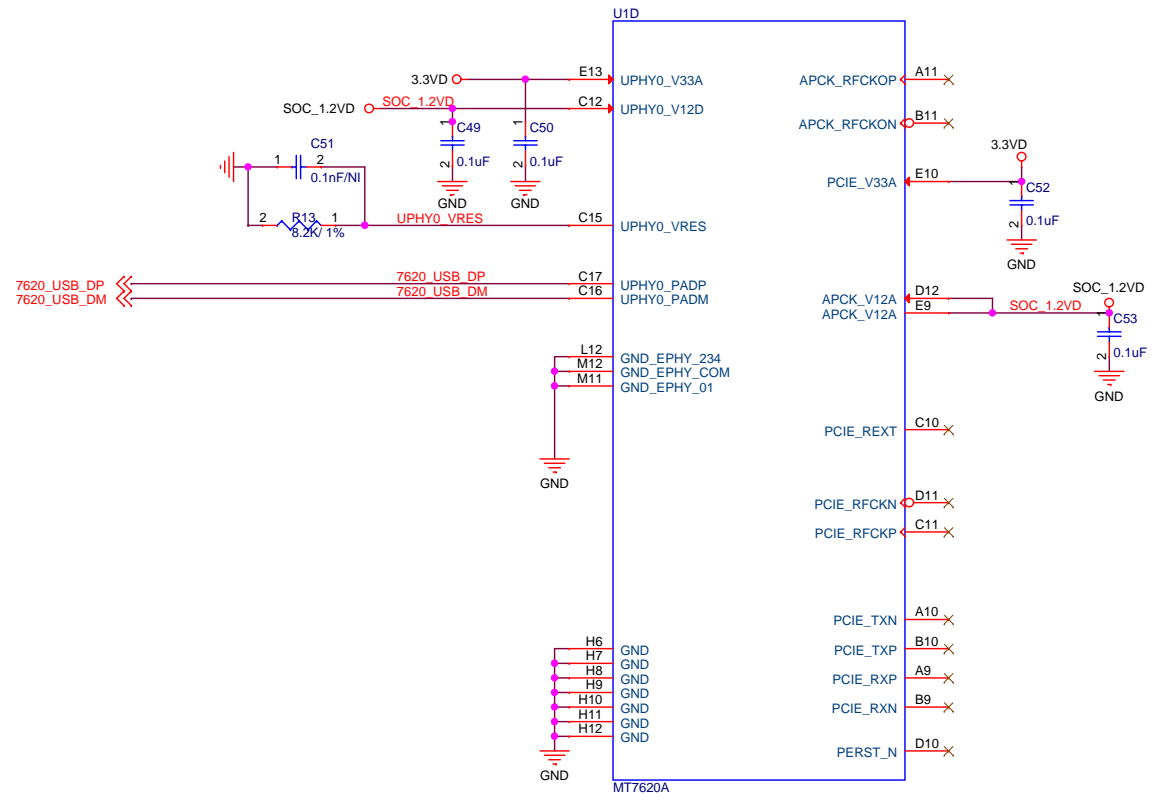
*3.3V-->1.2V/1.5A
Vout=0.6(1+R1/R2)*

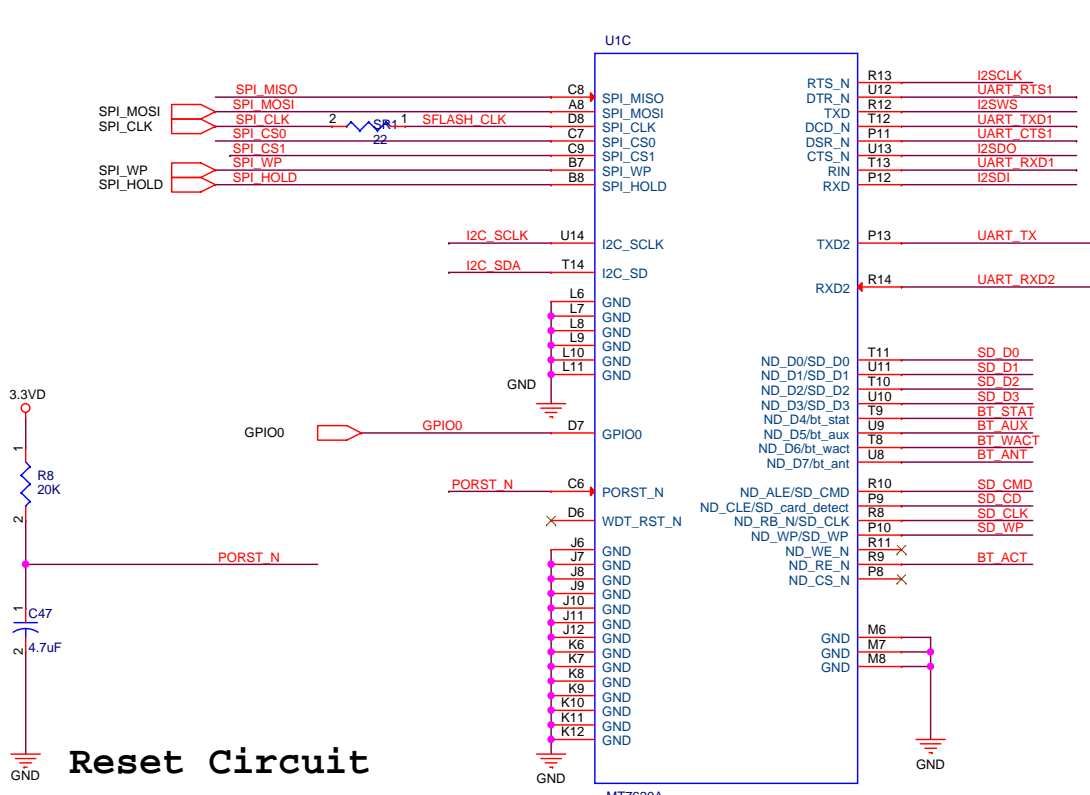


Close to MT7620

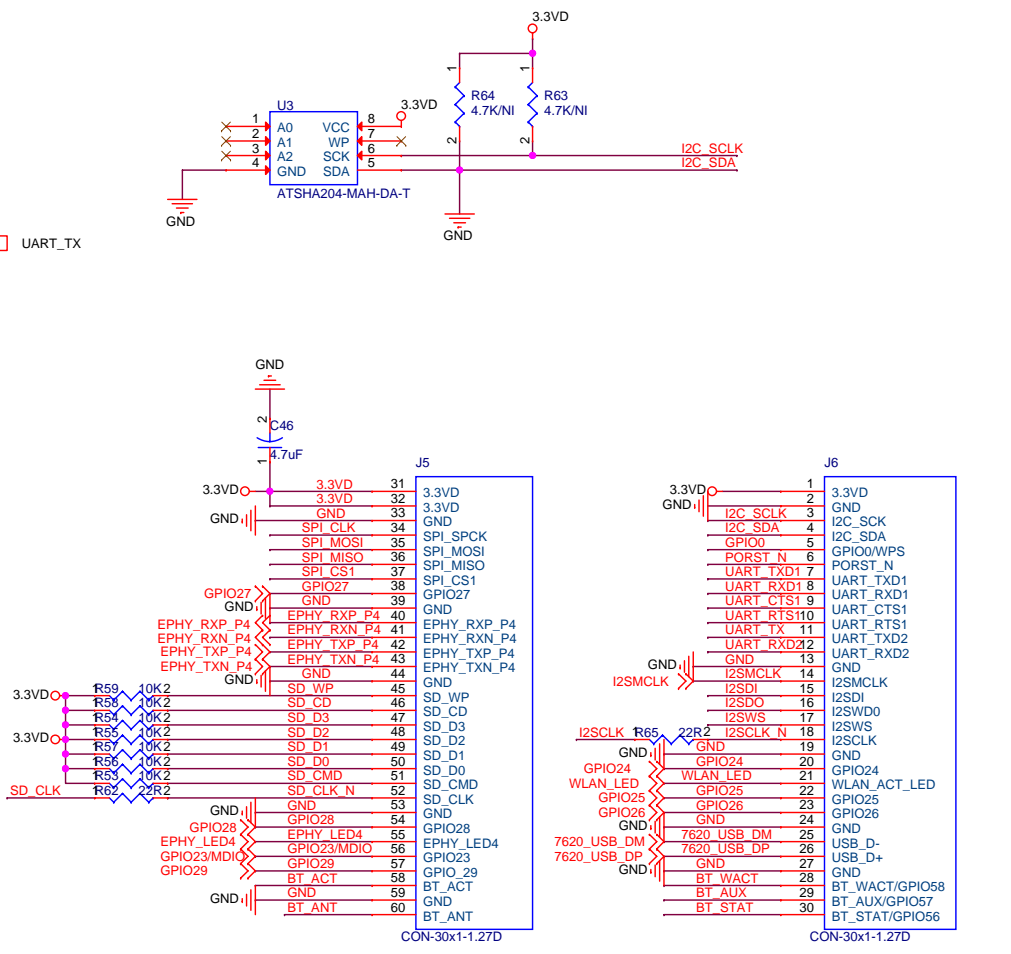
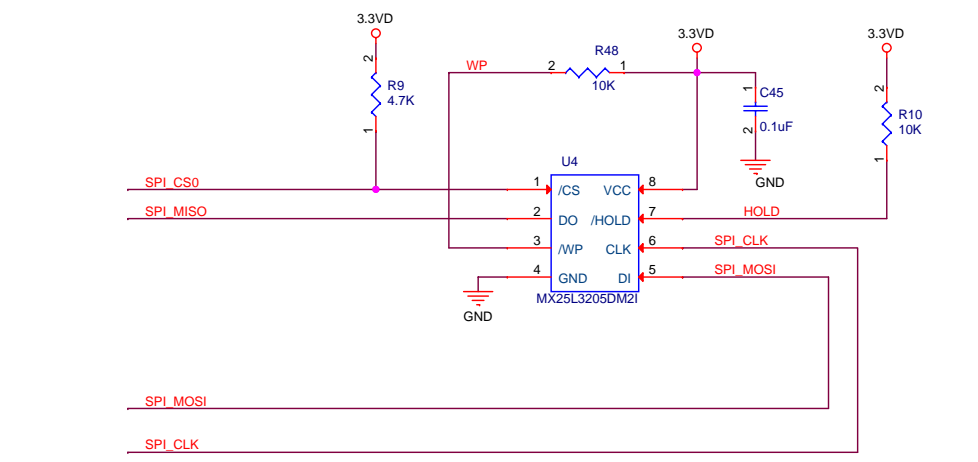


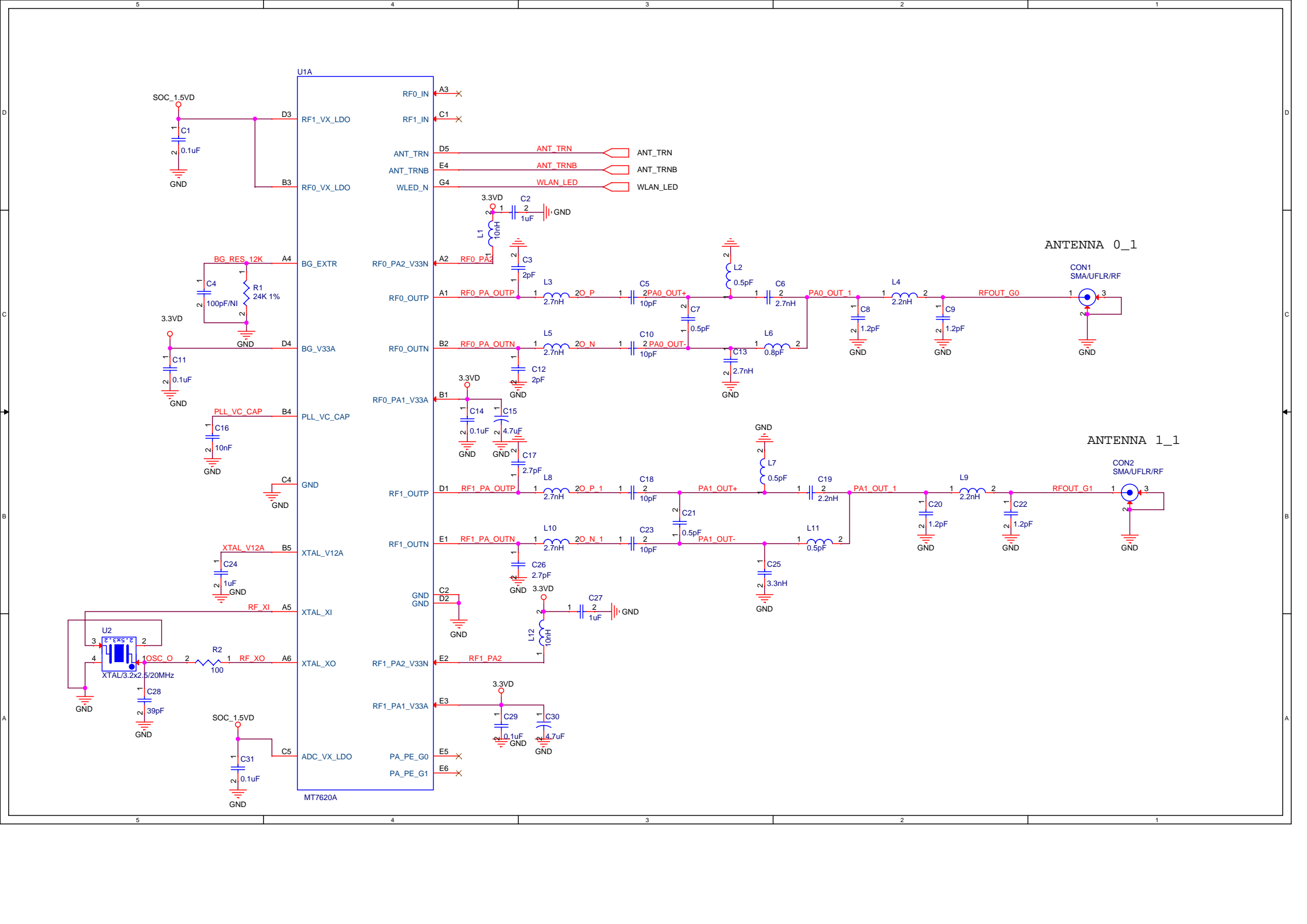
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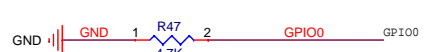
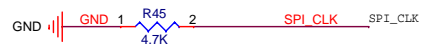
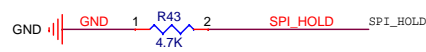
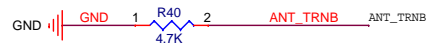
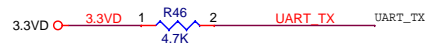
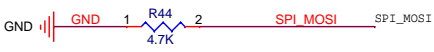
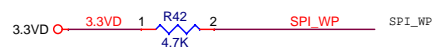
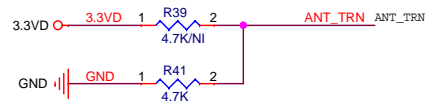
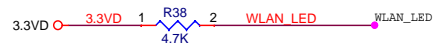
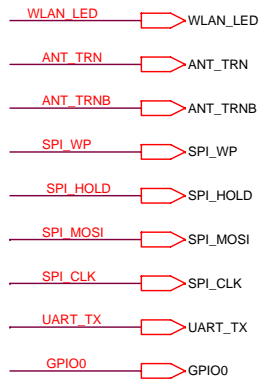




Reset Circuit







MT7620 Boot Up Strapping

Pin Name	Description	Value
WLAN_ACT_LED	DRAM_FROM_EE For non scan mode:	0: DRAM configuration from EEPROM 1: DRAM configuration from Auto Detect
ANT_TRN	DBG_JTAG_MODE	0: EPHY_LED 1: JTAG MODE
ANT_TRNB	XTAL_FREQ_SEL	0: 20MHz
{SPI_WP, SPI_HOLD}	DRAM_TYPE	01: DDR1 (CPU/3) TSOP 10: DDR2 (CPU/3) FBGA 11: SDRAM (CPU/5) (LVTTL 3.3 V) TSOP Package
{SPI_MOSI SPI_CLK, TXD2, GPIO0 }	CHIP_MODE[3:0]	A vector to set chip function/test/debug modes. In non-test/debug operation, 0010: Normal mode (boot from SPI 3Byte Addr)

MDATA[0:15]

MDATA[0:15]

MADDR[0:13] MADDR[0:13]

DDR_BA0
DDR_BA1
DDR_BA2
DDR_MCKE

DDR_CSN
DDR_RASN
DDR_CASN
DDR_WEN

