LS RESEARCH
Wireless Product Development

900 MHz Transceiver Module

Prepared by

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1 Introduction

1.1 Purpose & Scope

The purpose of this document is to provide a top level block diagram and theory of operation for a 900 MHz radio module with typical output power of ~ .75 watt.

1.2 Background / Technology

The radio solution will revolve around the Atmel AT86RF212, which is a low-power, low-voltage 900 MHz transceiver specially designed for low-cost IEEE 802.15.4, ZigBee™, and high data rate ISM applications. An additional power amplifier, filtering, antenna diversity switching will be provided in the LSR ModFlex module form factor.

Figure 1 shows High Level Block Diagram

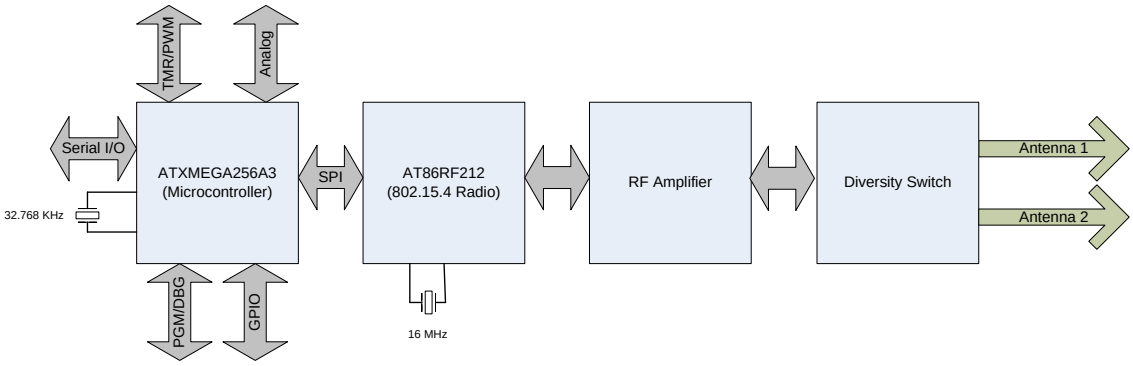

Figure 1: Module Block Diagram

Figure 2 provides some High-level specifications for module design.

SPECIFICATIONS	NELSON MODULE
Frequency	906 – 924 MHz
TX Power	+28 dBm
Rx Diversity	Hardware implemented
Operating Temp	-40 to +85C

Figure 2: Module General Specifications

2 Module Theory of Operation

2.1 Overview

The module was developed and optimised for a maximum output power.

2.2 Theory of Operation

The radio Block Diagram is shown below in Figure 3.

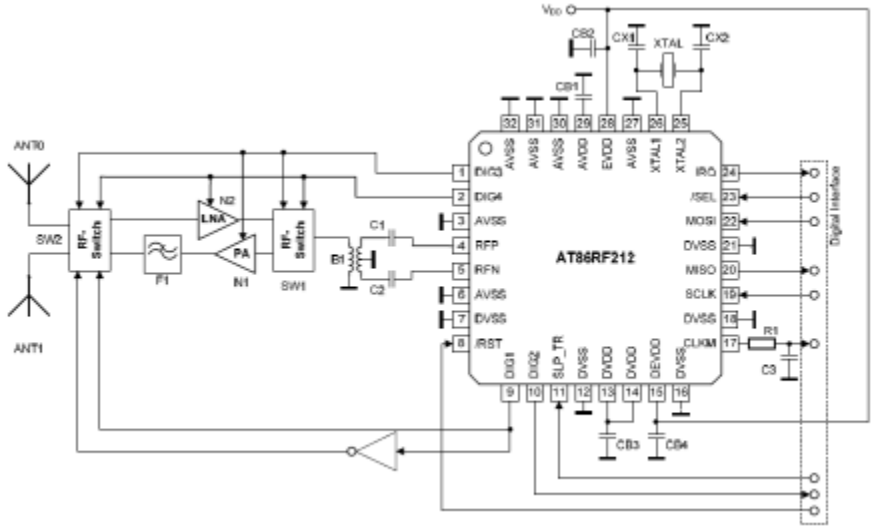

Figure 3 Radio Block Diagram

The module contains a direct sequence spread spectrum transceiver operating in the 902 - 928 MHz ISM band. The system is based on the IEEE 802.15.4-2006 standard, with 10 channels spaced at 2 MHz intervals in the ISM band. The system can operate in several modes. 1) BPSK modulation with each bit mapped by a 15-chip PN sequence at a chip rate of 600 kcps, a symbol rate of 40 ksps, and a bit rate of 40 kbps. The chip sequences are modulated onto the carrier using BPSK modulation with raised cosine pulse shaping (roll-off factor = 1). 2) OQPSK modulation with each symbol mapped by a 16-chip PN sequence at a chip rate of 1000 kcps, a symbol rate of 62.5ksps, and a bit rate of 250 kbps. At the chip rate of 1000 kcps, half-sine pulse shaping is used. 3)OQPSK modulation with each symbol mapped by a 4-chip PN sequence at a chip rate of 1000kcps, a symbol rate of 250 ksps, and a bit rate of 1Mbps. At the chip rate of 1000 kcps, half-sine pulse shaping is used.

The radio is a Atmel AT86RF212 single-chip RF transceiver which provide a radio interface between the RF Front-End and the microcontroller. It is comprised of an analog part, digital modulation and demodulation, including time and frequency synchronization as well as data buffering. The Atmel AT86RF212 supports the IEEE 802.15.4 standard BPSK modulation.

On-chip regulators provide the chips regulated supply for its analog and digital components. It frequency accuracy is derived from a 16.0 MHz 10 ppm crystal.

The RF Front-End is a provided by a RFMD RF3858 which supplies a transmit power amplifier, receiver low noise amplifier and antenna switching. Only receive diversity is allowed and must be implemented by the user.

The microcontroller is an Atmel ATXMEGA256A3 which controls the radio and interfaces the digital circuits outside of the module. The XMEGA A3 is a family of low power, high performance and peripheral rich CMOS 8/16-bit microcontrollers based on the AVR® enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the XMEGA A3 achieves throughputs approaching 1 Million Instructions Per Second (MIPS), thus allowing the system designer to optimize power consumption versus processing speed. The microcontroller uses a 32.768 KHz crystal for a real time clock.