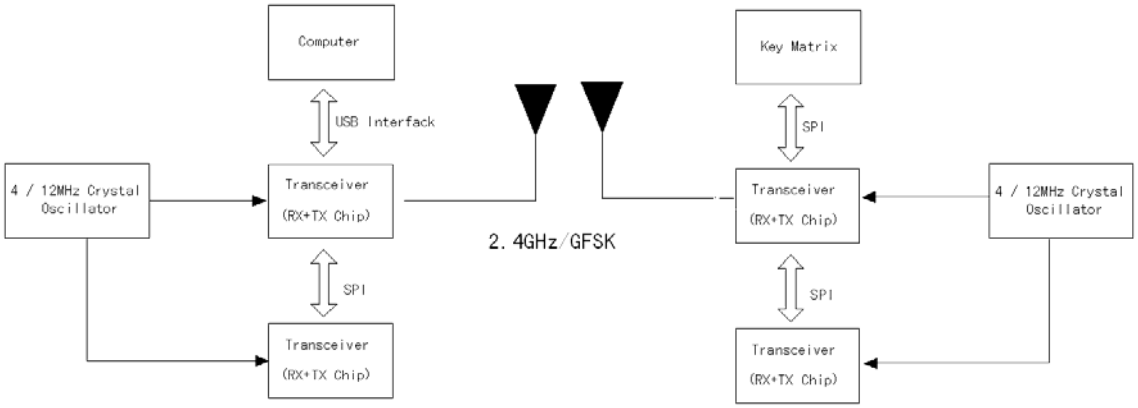
– Operating Description –

The RF transceiver block is a self-contained, fast-hopping GFSK data modem, optimized for use in the widely available 2.4 GHz ISM band. It contains transmit, receive, VCO and PLL functions, including an on-chip channel filter and resonator, thus minimizing the need for external components. The receiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments. Transmit power is digitally controlled. The low-IF receiver architecture results in sensitivity to -80 dBm or better, with impressive selectivity.

The framer register settings determine the over-the-air formatting characteristics. Transmit data is easily sent over-the-air as a complete frame of data, with preamble, address, payload, and CRC. Receiving data is just the opposite, using the preamble to train the receiver clock recovery, then the address is checked, then the data is reverse formatted for receive, followed by CRC. All of this is done in hardware to ease the programming and overhead requirements of the baseband MCU.

<2.4 RF Wireless Keyboard>



<Common Physical Layer Specification>

Operating Frequency	2402 ~ 2480 MHz
Carrier Spacing	2MHz
Channel	79 Channels
Duplexing	Half Duplexing
Data rate	1 Mbps
Band width	1 MHz
Senstivity	- 85dBm

※ This device support 79 channels, however It uses 16 channels among 79 channels to avoid channel noise randomly.