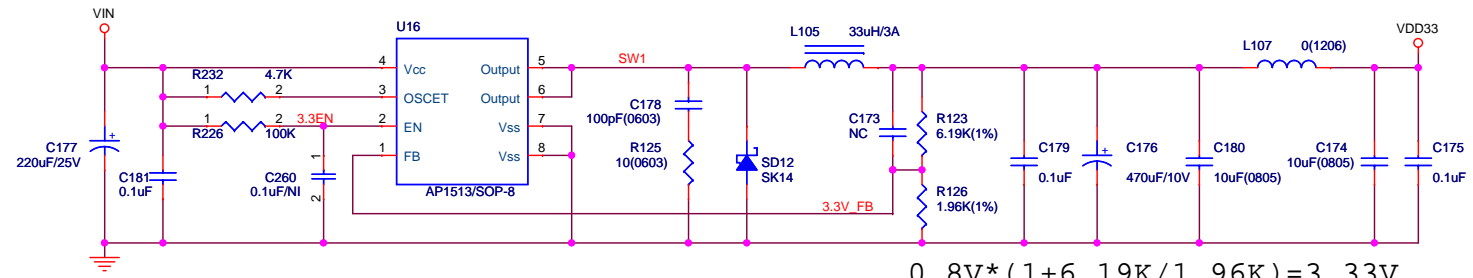
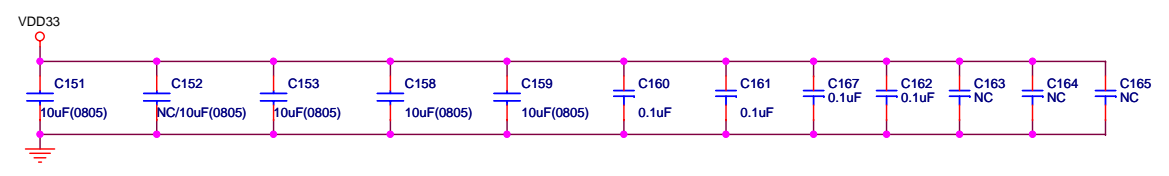
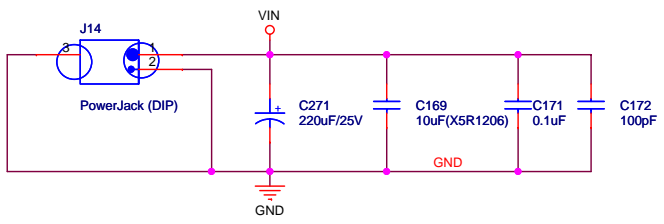
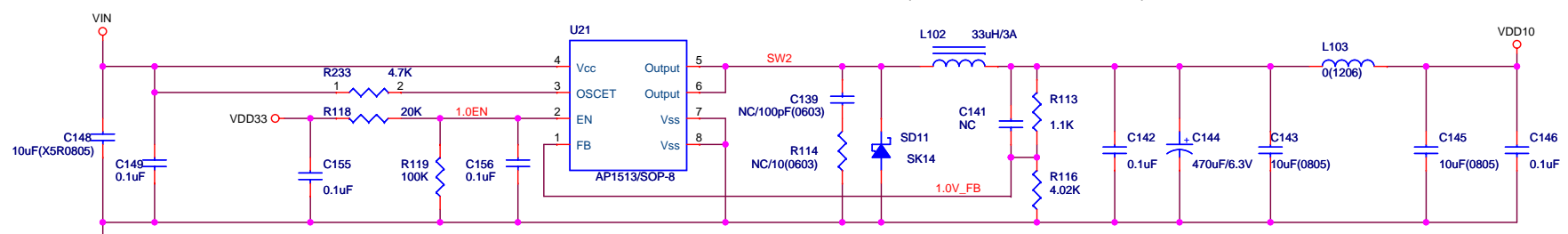


RTL8196C GPIO definition			
RTL8196C pin	GPIO Name	I/O	Function
pin 100	GPIOA2	O	PD#
pin 98	GPIOA6	O	SYSTEMLED
pin 96	GOIPA3	I	WPS
Pin 97	GOIPA4	O	WPSLED
pin 99	GPIOA5	I	Reset/Default
pin 109	GPIOC0	I	CLKREQ#
pin 108	GPIOB7	I	WAKE#
pin 67	Cannot use		

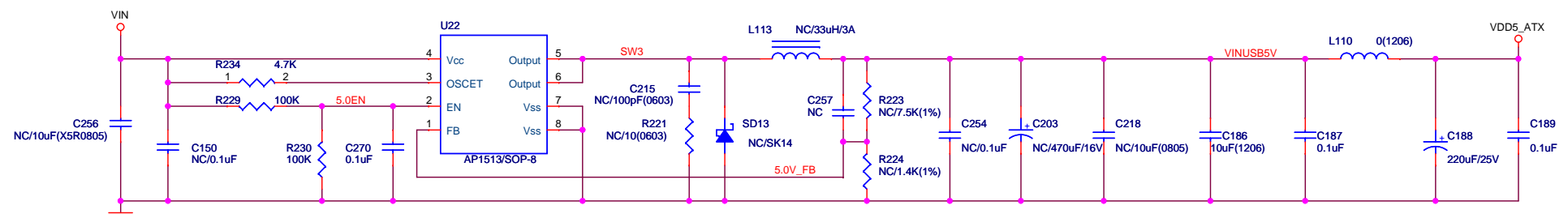
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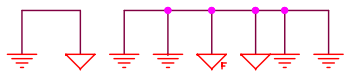
$$0.8V * (1 + 6.19K / 1.96K) = 3.33V$$



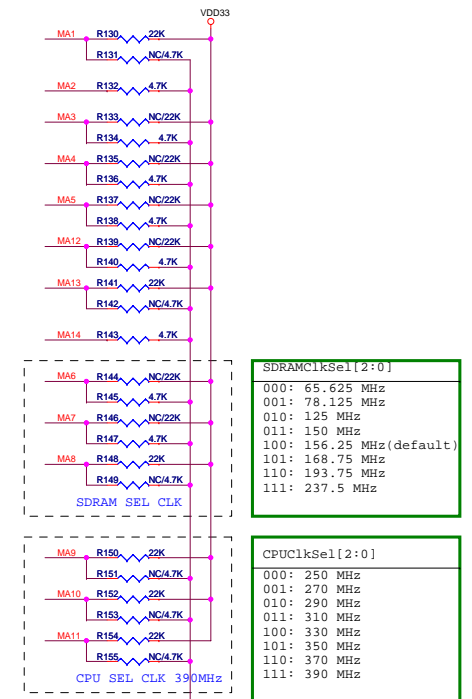
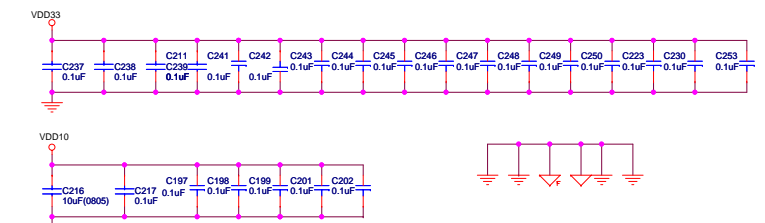
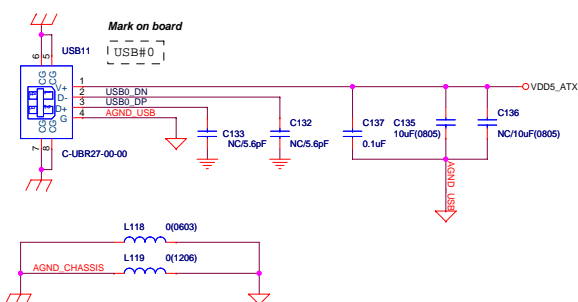
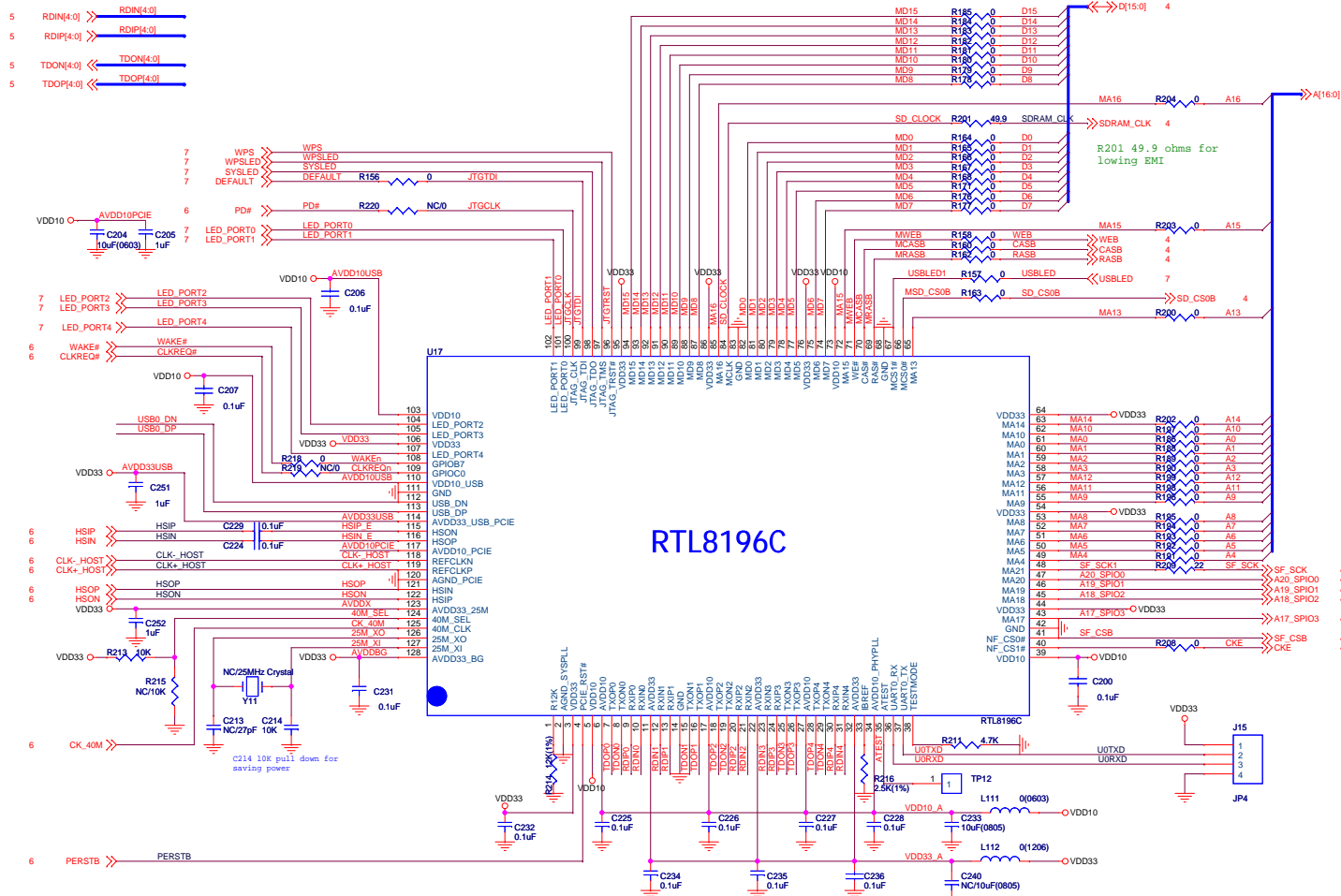
$$0.8V * (1 + 1.1K / 4.02K) = 1.02V$$



$$0.8V * (1 + 7.5K / 1.4K) = 5.09V$$



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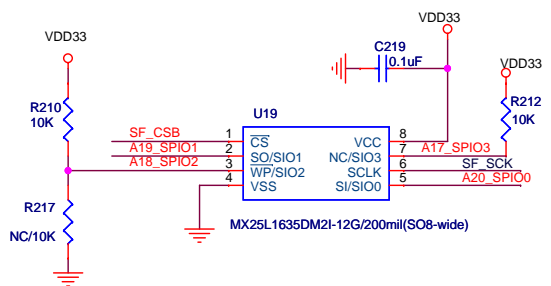
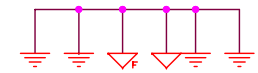
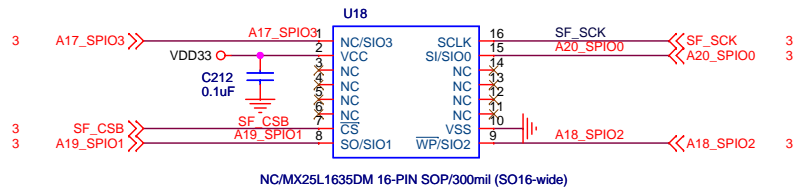
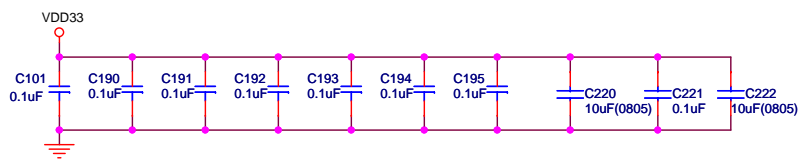
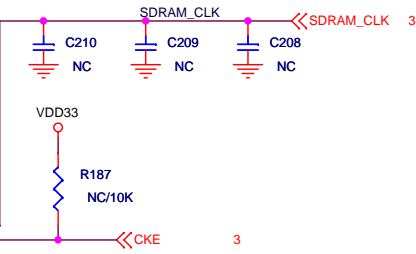
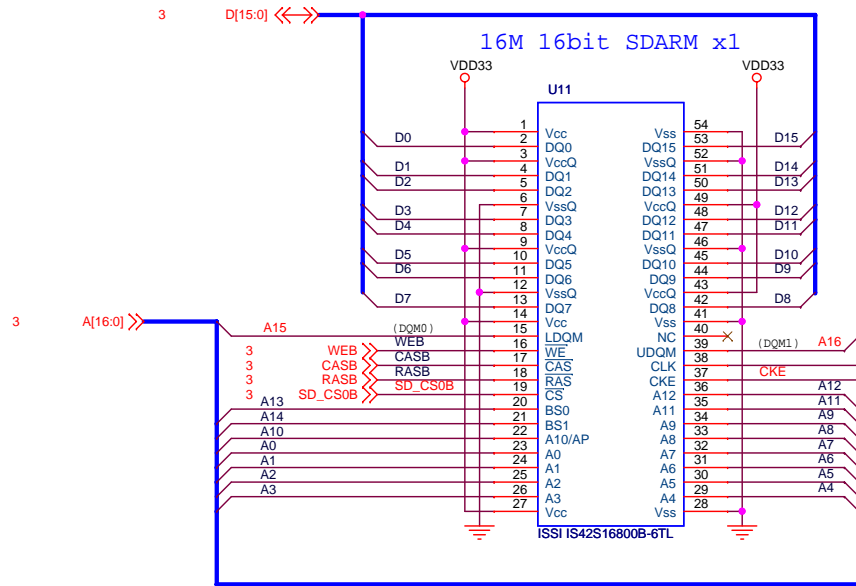
SDRAMclkSel[2:0]

000:	65.625 MHz
001:	78.125 MHz
010:	125 MHz
011:	150 MHz
100:	156.25 MHz (default)
101:	168.75 MHz
110:	193.75 MHz
111:	237.5 MHz

CPUClkSel[2:0]

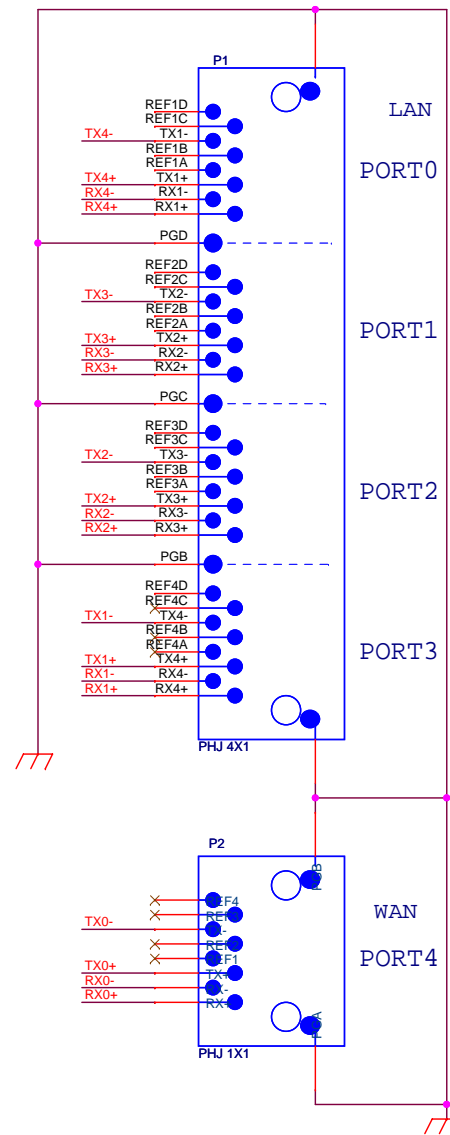
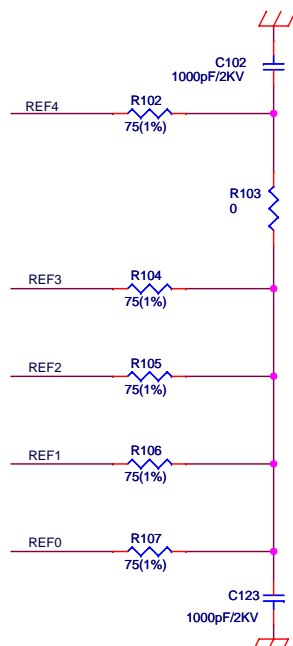
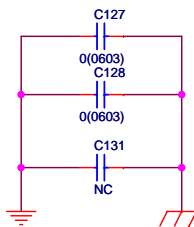
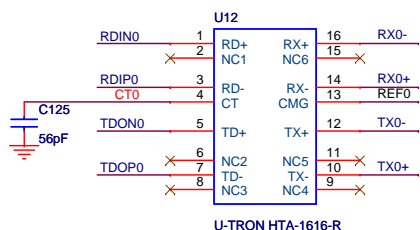
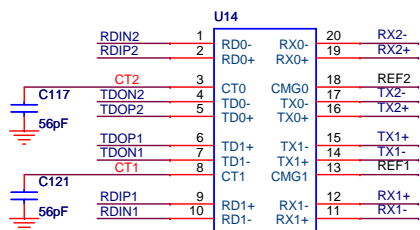
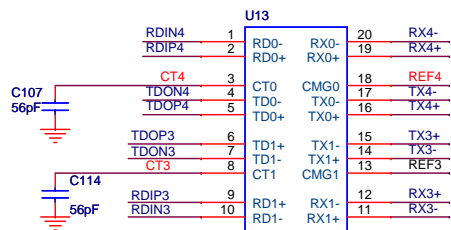
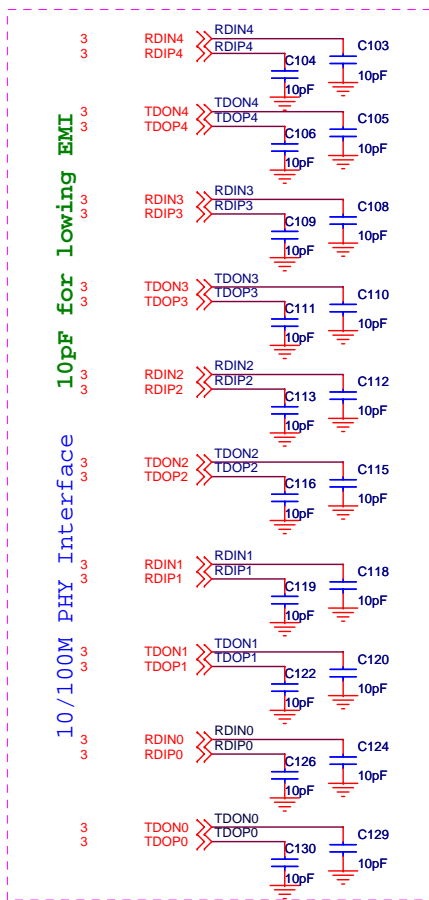
000:	250 MHz
001:	270 MHz
010:	290 MHz
011:	310 MHz
100:	330 MHz
101:	350 MHz
110:	370 MHz
111:	390 MHz

Signal	Function	Description
MA1	BOOTSEL	0: NOR Flash (default) 1: SPI Flash
MA3	ClkIx_from_clkm	0: default 1: Clk_lx come from clk_m
MA4	Enable external reset	0: disable (default) 1: enable
MA5	SYNC_LX_OC	0: default 1: set SYNC_OC=SYNC_LX =SYNC_LX_OC for testing
MA[6:8]	(DRAM SEL CLK) clk_m2x_freq_sel[0:2]	H/W strap can set 3 bits[0:2]
MA[9:11]	(CPU SEL CLK) clk_cpu_freq_sel[1:3]	H/W strap can set 3 bits[1:3]
MA12	ck_cpu_div_sel	0: default 1: pll_cpu divide by 2
MA13	en_router_mode	0: 1 port AP mode 1: 5 port router mode(default)

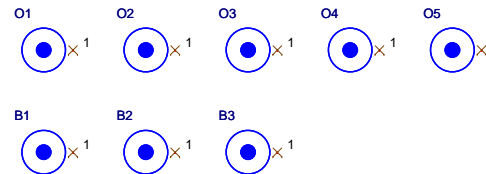
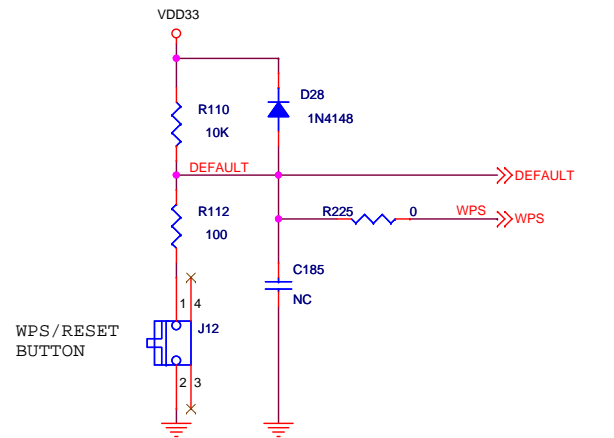
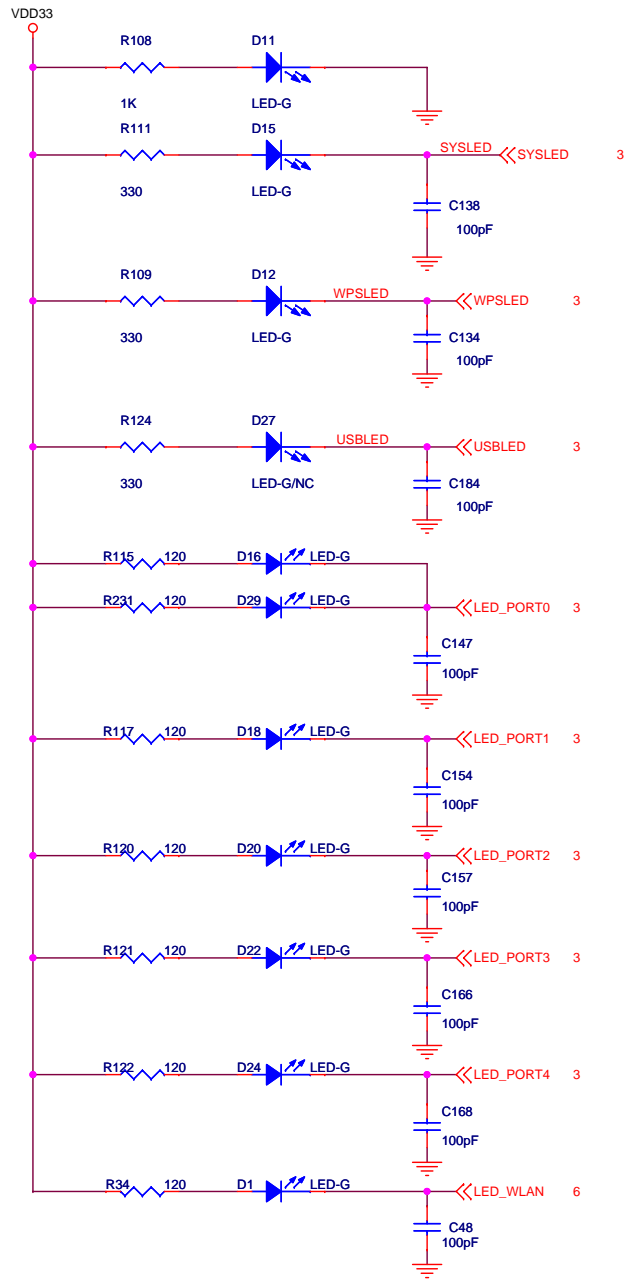


SPI Flash	Single I/O	Quad I/O
8/16 pins SPI	R210=10K R212=10K	R210=NC R212=NC

3 RDIN[4:0] << RDIN[4:0]
 3 RDIP[4:0] << RDIP[4:0]
 3 TDON[4:0] >> TDON[4:0]
 3 TDOP[4:0] >> TDOP[4:0]



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Version	Major change	Issue date
V100	RTL8196C and RTL8192CE 10/100M AP/Router first issue	06/02/2010

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