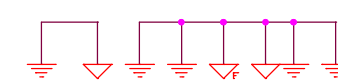
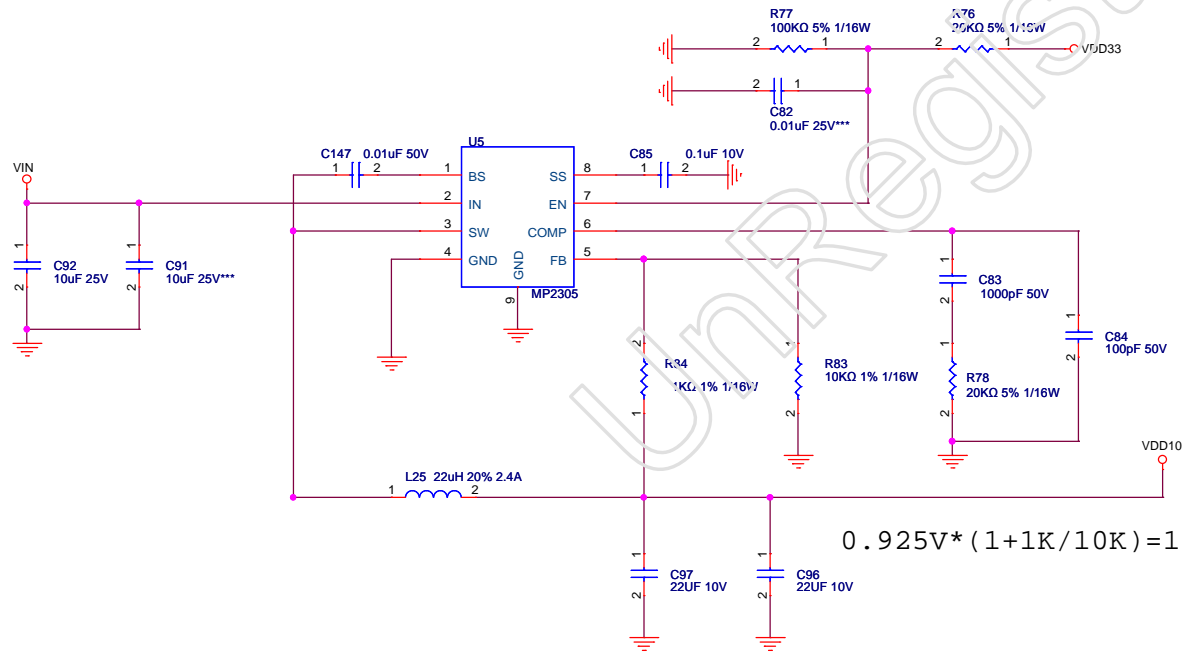
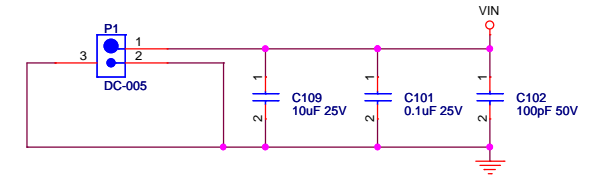
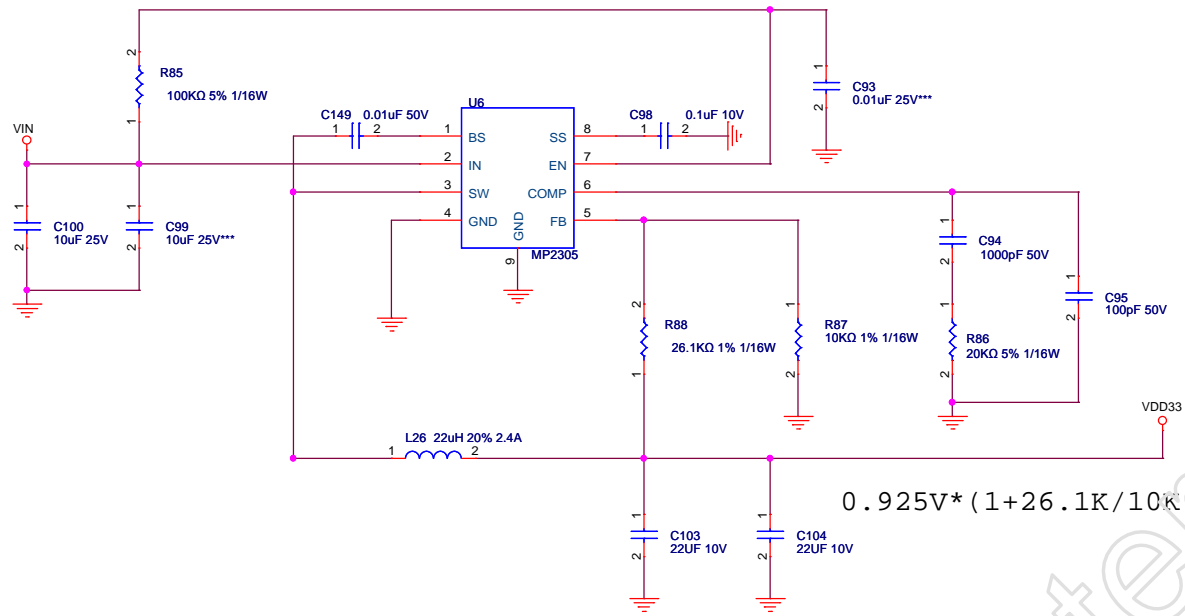


Version	Major change	Issue date
V100	RTL8196C and RTL8192CE 10/100M AP/Router first issue	06/02/2010

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A	Revision History	1.0
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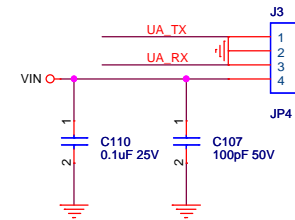
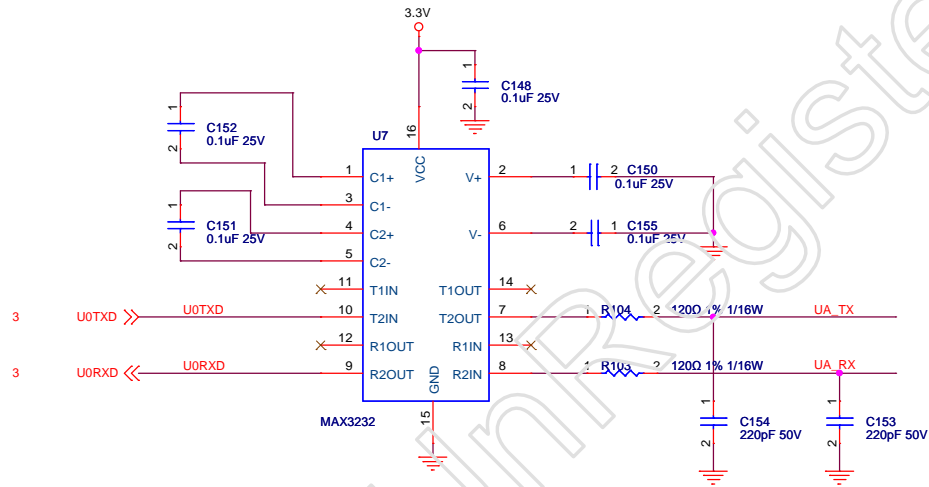
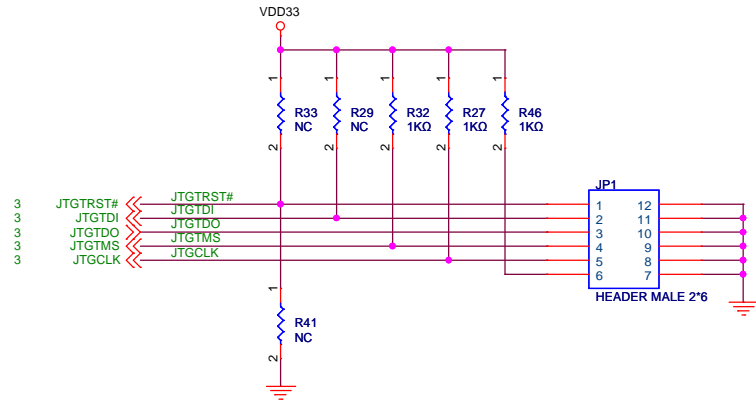
UnRegistered



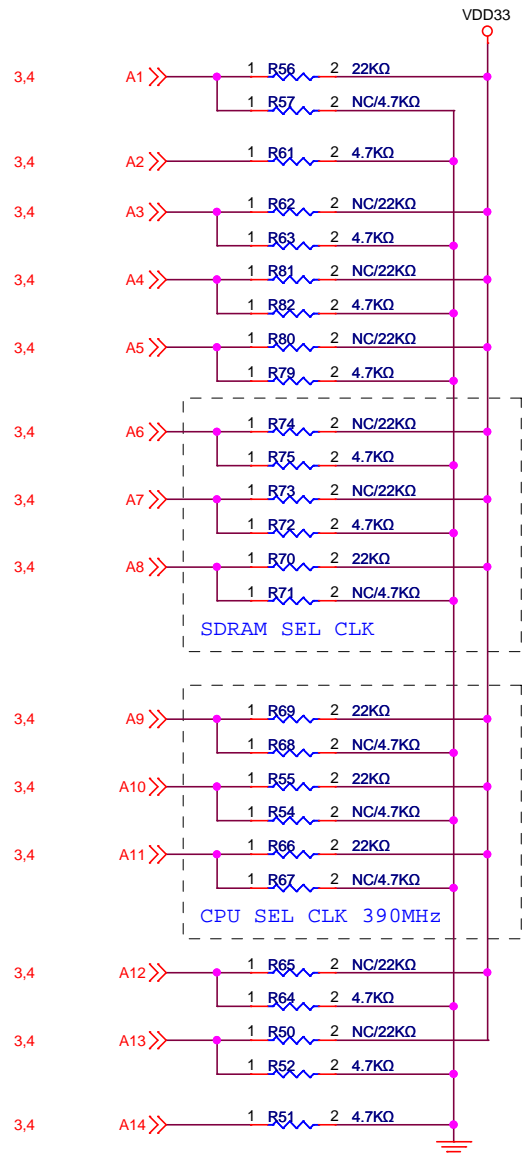
Prepared by binupt		
Issued Date : 2010/11/08		
Title WA518N		
Size B	Document Number POWER	Rev 1.0
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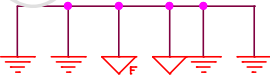


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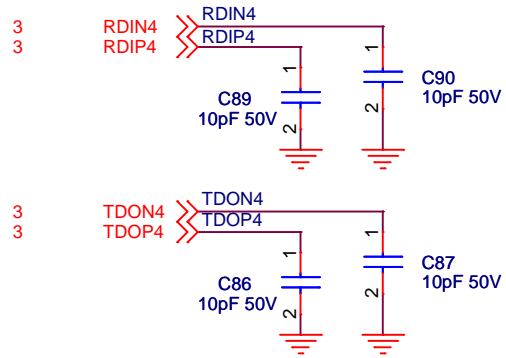
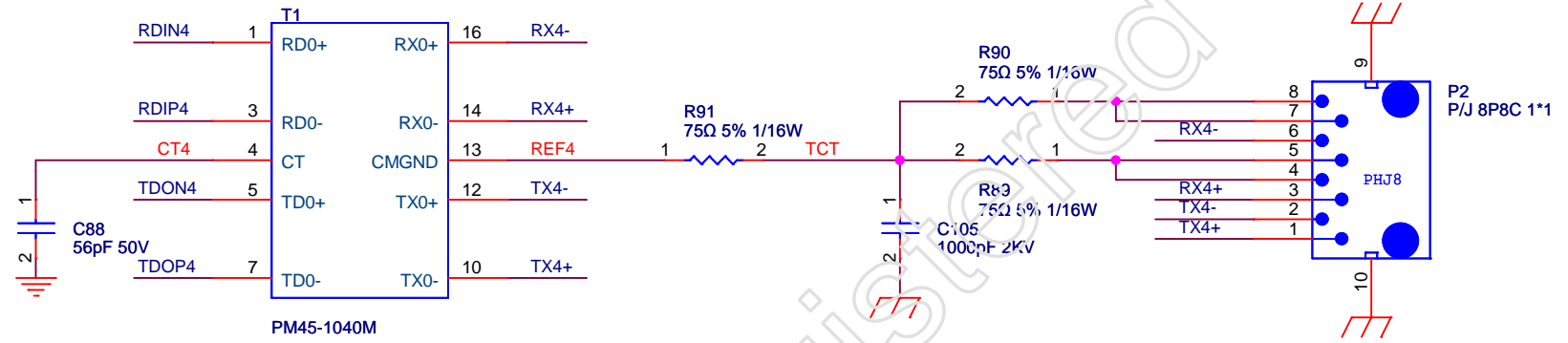
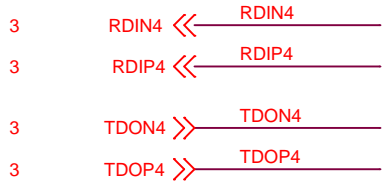
SDRAMclkSel[2:0]	
000:	65.625 MHz
001:	78.125 MHz
010:	125 MHz
011:	150 MHz
100:	156.25 MHz (default)
101:	168.75 MHz
110:	193.75 MHz
111:	237.5 MHz

CPUclkSel[2:0]	
000:	250 MHz
001:	270 MHz
010:	290 MHz
011:	310 MHz
100:	330 MHz
101:	350 MHz
110:	370 MHz
111:	390 MHz

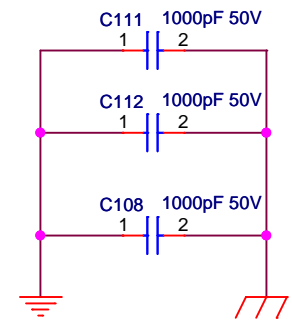


Signal	Function	Description
MA1	BOOTSEL	0: NOR Flash (default) 1: SPI Flash
MA3	Clklx_from_clkm	0: default 1: Clk_lx come from clk_m
MA4	Enable external reset	0: disable (default) 1: enable
MA5	SYNC_LX_OC	0: default 1: set SYNC_OC=SYNC_LX =SYNC_LX_OC for testing
MA[6:8]	(DRAM SEL CLK) clk_m2x_freq_sel[0:2]	H/W strap can set 3 bits[0:2]
MA[9:11]	(CPU SEL CLK) clk_cpu_freq_sel[1:3]	H/W strap can set 3 bits[1:3]
MA12	ck_cpu_div_sel	0: default 1: pll_cpu divide by 2
MA13	en_router_mode	0: 1 port AP mode 1: 5 port router mode (default)

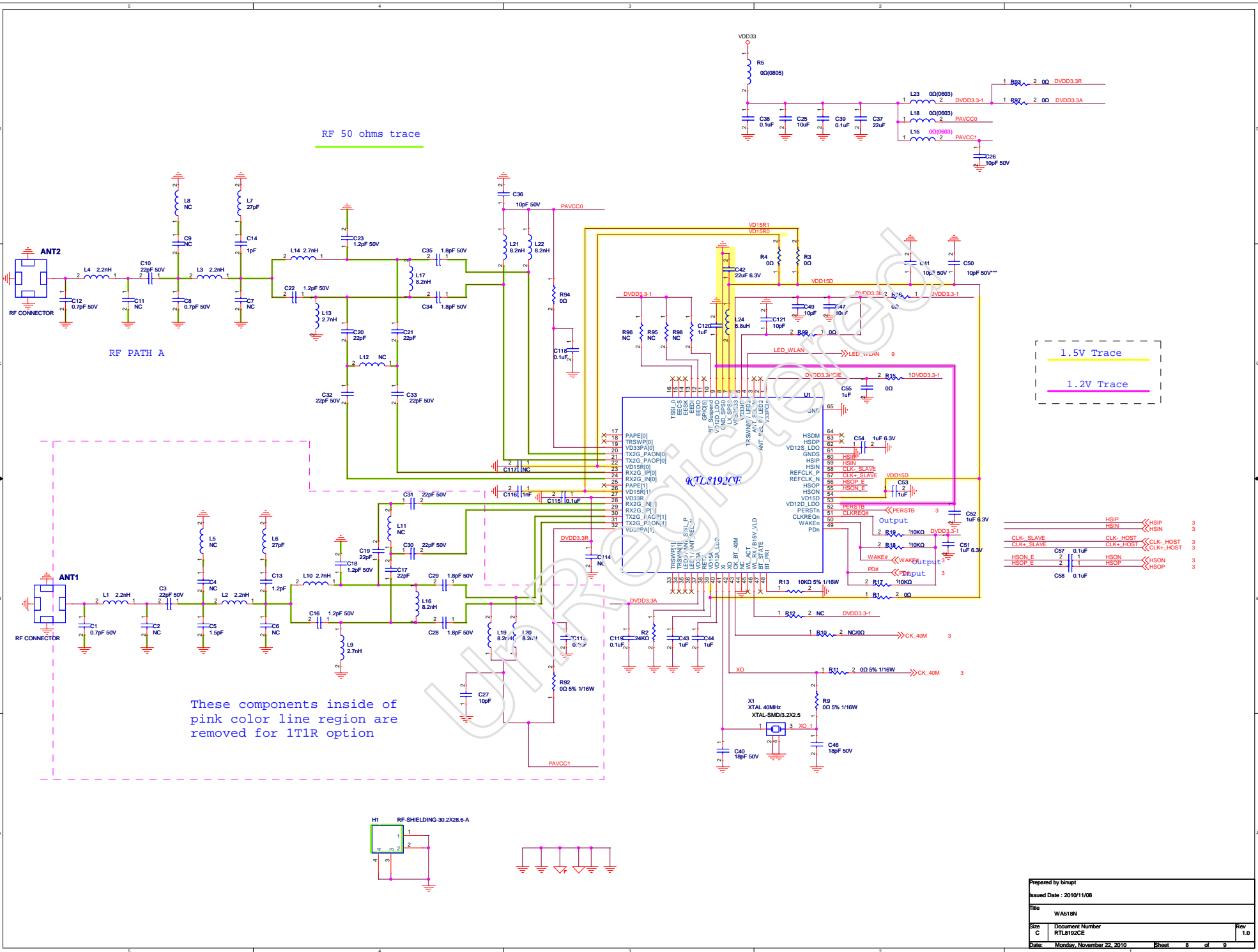
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10pF for lowering EMI



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RF 50 ohms trace

RF PATH A

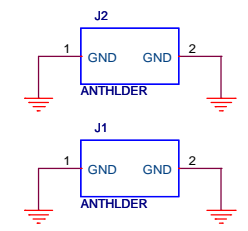
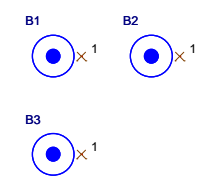
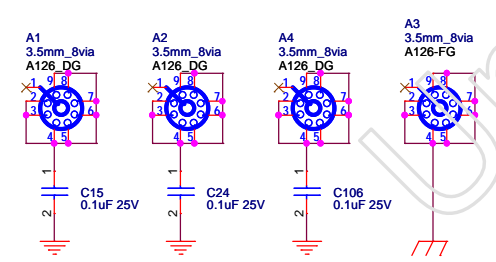
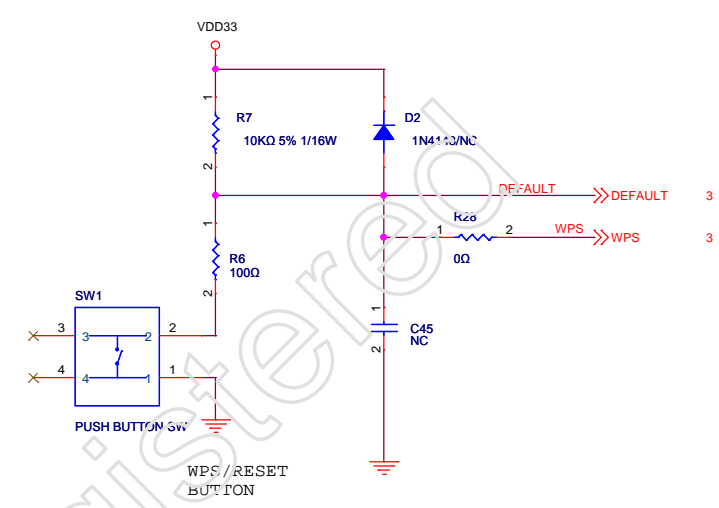
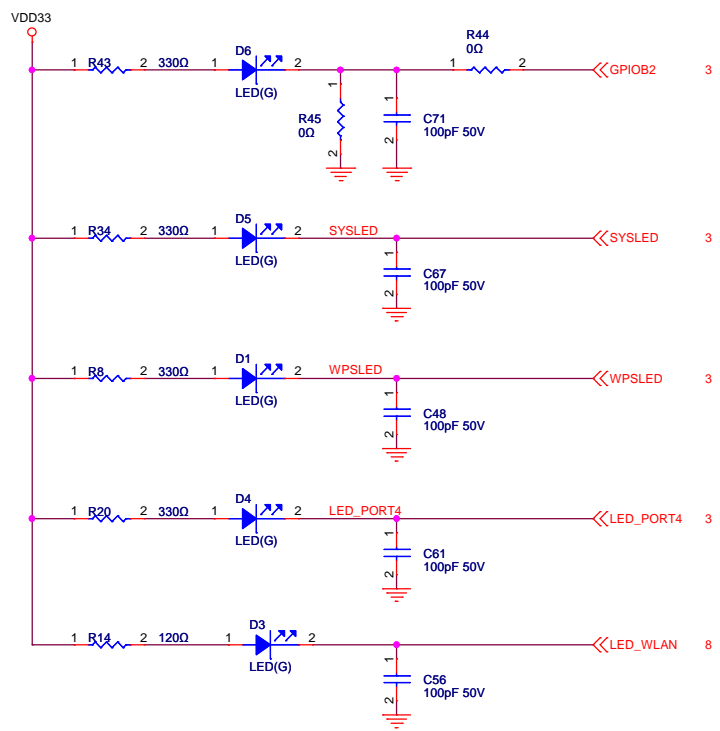
These components inside of pink color line region are removed for 1T1R option

1.5V Trace  
1.2V Trace

- H5IP << H5IP 3
- CLK+ SLAVE << CLK+ HOST 3
- CLK- SLAVE << CLK- HOST 3
- H5ON\_E << H5ON 3
- H5OP\_E << H5OP 3
- C57 0.1uF
- C58 0.1uF

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