CC2651R3SIPA SimpleLink™ Multiprotocol 2.4 GHz Wireless System-in-Package Module with integrated Antenna & 352-KB Memory

1 Features

Wireless microcontroller

- Powerful 48-MHz Arm® Cortex®-M4 processor
- 352KB flash program memory
- 32KB of ultra-low leakage SRAM
- 8KB of Cache SRAM (Alternatively available as general-purpose RAM)
- Programmable radio includes support for 2-(G)FSK, 4-(G)FSK, MSK, *Bluetooth*® 5.2 Low Energy, IEEE 802.15.4 PHY and MAC
- Supports over-the-air upgrade (OTA)

Low power consumption

- MCU consumption:
  - 3.60 mA active mode, CoreMark
  - 61 µA/MHz running CoreMark
  - 0.8 µA standby mode, RTC, 32KB RAM
  - 0.1 µA shutdown mode, wake-up on pin
- Radio Consumption:
  - 6.8 mA RX
  - 7.1 mA TX at 0 dBm
  - 9.6 mA TX at +5 dBm

Wireless protocol support

- Zigbee®
- *Bluetooth*® 5.2 Low Energy
- SimpleLink™ TI 15.4-stack
- Proprietary systems

High performance radio

- -104 dBm for *Bluetooth*® Low Energy 125-kbps
- Output power up to +5 dBm with temperature compensation

Regulatory compliance

- Regulatory certification for compliance with worldwide radio frequency:
  - ETSI RED (Europe) / RER (UK)
  - ISED (Canada)
  - FCC (USA)

MCU peripherals

- Digital peripherals can be routed to any GPIO
- Four 32-bit or eight 16-bit general-purpose timers
- 12-bit ADC, 200 kSamples/s, 8 channels
- 8-bit DAC
- Two comparators
- Programmable current source
- UART, SSI, I^2C, I^2S
- Real-time clock (RTC)
- Integrated temperature and battery monitor

Security enablers

- AES 128-bit cryptographic accelerator
- True random number generator (TRNG)
- Additional cryptography drivers available in Software Development Kit (SDK)

Development tools and software

- LP-CC2651R3SIPA Development Kit
- SimpleLink™ CC13xx and CC26xx Software Development Kit (SDK)
- SmartRF™ Studio for simple radio configuration
- SysConfig system configuration tool

Operating range

- On-chip buck DC/DC converter
- 1.8-V to 3.8-V single supply voltage
- T_j: -40 to +105°C

Package

- 7-mm × 7-mm MOU (32 GPIOs)
- RoHS-compliant package

2 Applications

- 2400 to 2480 MHz ISM and SRD systems [1]
- Building automation
  - Building security systems – motion detector, electronic smart lock, door and window sensor, garage door system, gateway
  - HVAC – thermostat, wireless environmental sensor, HVAC system controller, gateway
  - Fire safety system – smoke and heat detector, fire alarm control panel (FACP)
  - Video surveillance – IP network camera
  - Elevators and escalators – elevator main control panel for elevators and escalators
- Industrial transport – asset tracking
- Factory automation and control
- Medical
- Electronic point of sale (EPOS) – Electronic Shelf Label (ESL)
- Communication equipment
  - Wired networking – wireless LAN or Wi-Fi access points, edge router , small business router
- Personal electronics
  - Portable electronics – RF smart remote control
  - Home theater & entertainment – smart speakers, smart display, set-top box
  - Connected peripherals – consumer wireless module, pointing devices, keyboards and keypads
  - Gaming – electronic and robotic toys
  - Wearables (non-medical) – smart trackers, smart clothing

3 Description

The SimpleLink™ CC2651R3SIPA device is a multiprotocol 2.4-GHz wireless microcontroller (MCU) supporting Zigbee®, Bluetooth® 5.2 Low Energy, IEEE 802.15.4g, TI 15.4-Stack (2.4 GHz). The CC2651R3SIPA is based on an Arm® Cortex® M4 main processor and optimized for low-power wireless communication and advanced sensing in grid infrastructure, building automation, retail automation, personal electronics and medical applications.

The CC2651R3SIPA is an ultra-compact 7-mm x 7-mm certified wireless module 2.4 GHz with integrated antenna, DCDC components, Balun, and high frequency crystal oscillator.

The CC2651R3SIPA has a software defined radio powered by an Arm® Cortex® M0, which allows support for multiple physical layers and RF standards. The device supports operation in the 2360 to 2500-MHz frequency band. The CC2651R3SIPA supports +5 dBm TX at 9.6 mA in the 2.4-GHz band. CC2651R3SIPA has a receive sensitivity of -104 dBm for 125-kbps Bluetooth® Low Energy Coded PHY.

The CC2651R3SIPA has a low sleep current of 0.9 µA with RTC and 32KB RAM retention.

TI has a product life cycle policy with a commitment to product longevity and continuity of supply.

The CC2651R3SIPA device is part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, Bluetooth® Low Energy, Thread, Zigbee, Wi-SUN®, Amazon Sidewalk, mioty, Sub-1 GHz MCUs, and host MCU.CC2651R3SIPA is part of a scalable portfolio with flash sizes from 32KB to 704KB with pin-to-pin compatible package options. The common SimpleLink™CC13xx and CC26xx Software Development Kit (SDK) and SysConfig system configuration tool supports migration between devices in the portfolio. A comprehensive number of software stacks, application examples and SimpleLink™ Academy training sessions are included in the SDK. For more information, visit wireless connectivity.

Device Information

PART NUMBER (1)	PACKAGE	BODY SIZE (NOM)
CC2651R3SIPAT0MOUR	QFM (59)	7.00 mm × 7.00 mm

(1) For the most current part, package, and ordering information for all available devices, see the Package Option Addendum in Section 13, or see the TI website.

[1] See *RF Core* for additional details on supported protocol standards, modulation formats, and data rates.

4 Functional Block Diagram

Figure 4-1 shows the functional block diagram of the CC2651R3SIPA module.

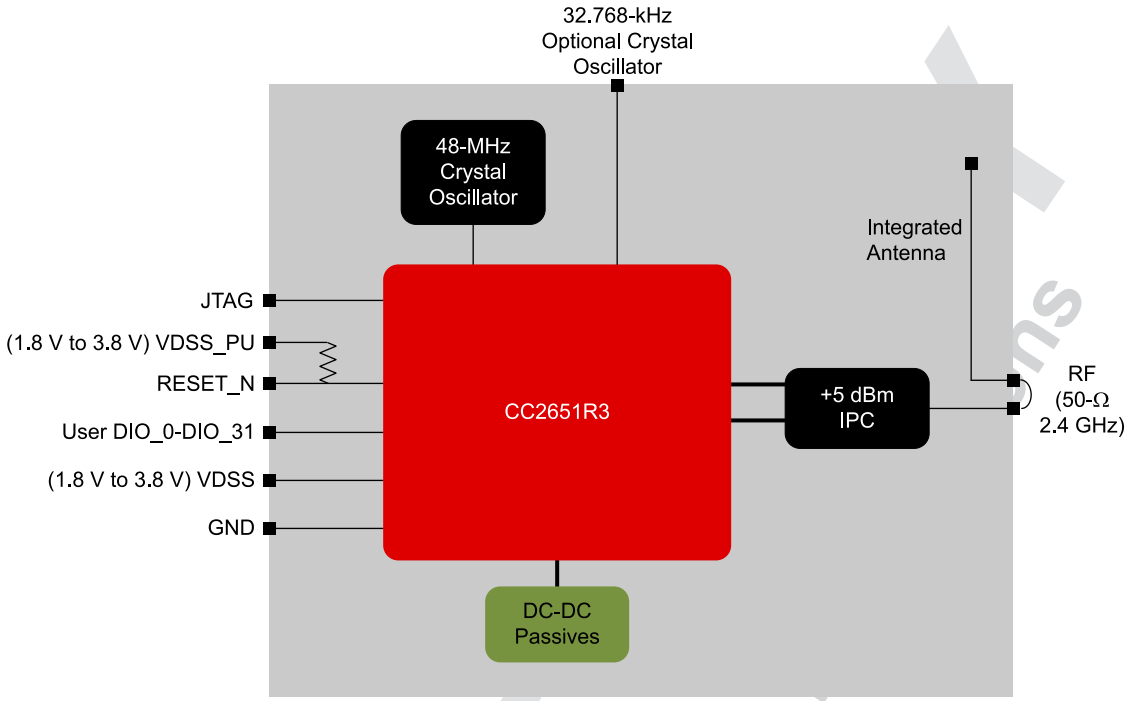

Figure 4-1. CC2651R3SIPA Block Diagram

Figure 4-2 shows an overview of the CC2651R3SIPA hardware.

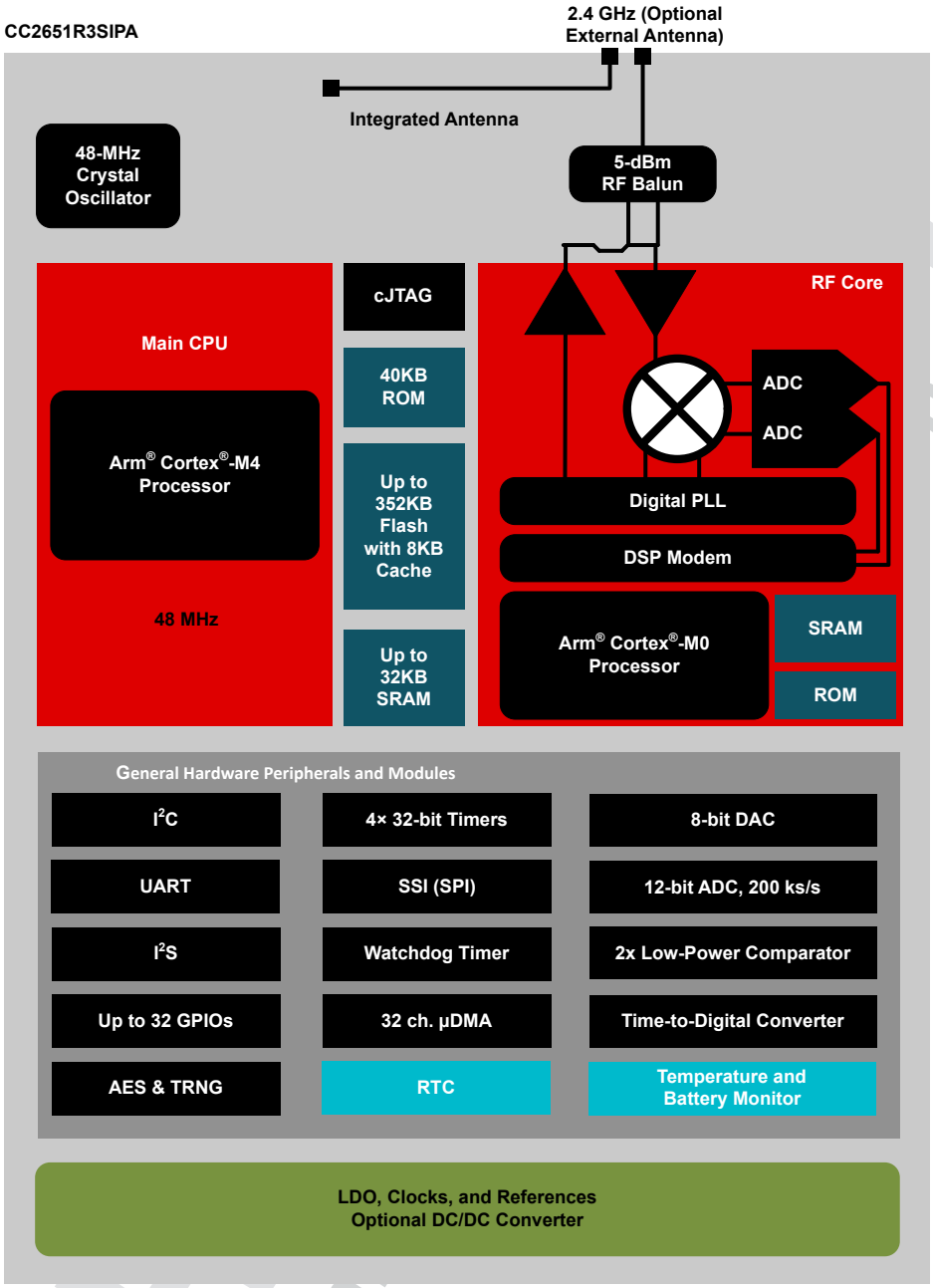

Figure 4-2. CC2651R3SIPA Hardware Overview

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (February 2022) to Revision A (June 2022)	Page
• Updated numbering of sections, figures, and tables throughout the data sheet	1
• Updated formatting throughout data sheet to match current documentation standards	1
• Devices are now PRODUCTION DATA	1

6 Device Comparison

Device	RADIO SUPPORT										FLASH (KB)	RAM + Cache (KB)	GPIO	PACKAGE SIZE			
	Sub-1 GHz Prop.	2.4 GHz Prop.	Wireless M-Bus	Wi-SUN®	Sidewalk	*Bluetooth*® LE	ZigBee	Thread	Multiprotocol	+20 dBm PA				4 x 4 mm VQFN (32)	5 x 5 mm VQFN (32)	5 x 5 mm VQFN (40)	7 x 7 mm VQFN (48)
CC1310	X		X								32-128	16-20 + 8	10-30	X	X		X
CC1311R3	X		X								352	32 + 8	22-30			X	X
CC1311P3	X		X							X	352	32 + 8	26				X
CC1312R	X		X	X							352	80 + 8	30				X
CC1312R7	X		X	X	X				X		704	144 + 8	30				X
CC1352R	X	X	X	X		X	X	X	X		352	80 + 8	28				X
CC1352P	X	X	X	X		X	X	X	X	X	352	80 + 8	26				X
CC1352P7	X	X	X	X	X	X	X	X	X	X	704	144 + 8	26				X
CC2640R2F						X					128	20 + 8	10-31	X	X		X
CC2642R						X					352	80 + 8	31				X
CC2642R-Q1						X					352	80 + 8	31				X
CC2651R3		X				X	X				352	32 + 8	23-31			X	X
CC2651P3		X				X	X			X	352	32 + 8	22-26			X	X
CC2652R		X				X	X	X	X		352	80 + 8	31				X
CC2652RB		X				X	X	X	X		352	80 + 8	31				X
CC2652R7		X				X	X	X	X		704	144 + 8	31				X
CC2652P		X				X	X	X	X	X	352	80 + 8	26				X
CC2652P7		X				X	X	X	X	X	704	144 + 8	26				X

Module	ANTENNA		RADIO SUPPORT			CERTIFICATIONS			FLASH (KB)	RAM + Cache (KB)	GPIO	PACKAGE SIZE		
	External	Integrated	*Bluetooth*® LE	ZigBee	+10 dBm PA	FCC/IC	CE	Japan				7 x 7 QFM (73)	7 x 7 QFM (59)	16.9 x 11.0 QFM (29)
CC2650MODA		X	X	X		X	X	X	128	20+8	15			X
CC2651R3SIPA	X	X	X	X		X	X		352	32 + 8	32		X	
CC2652RSIP	X		X	X		X	X		352	80 + 8	32	X		
CC2652PSIP	X		X	X	X	X	X		352	80 + 8	30	X		

7 Terminal Configuration and Functions

7.1 Pin Diagram

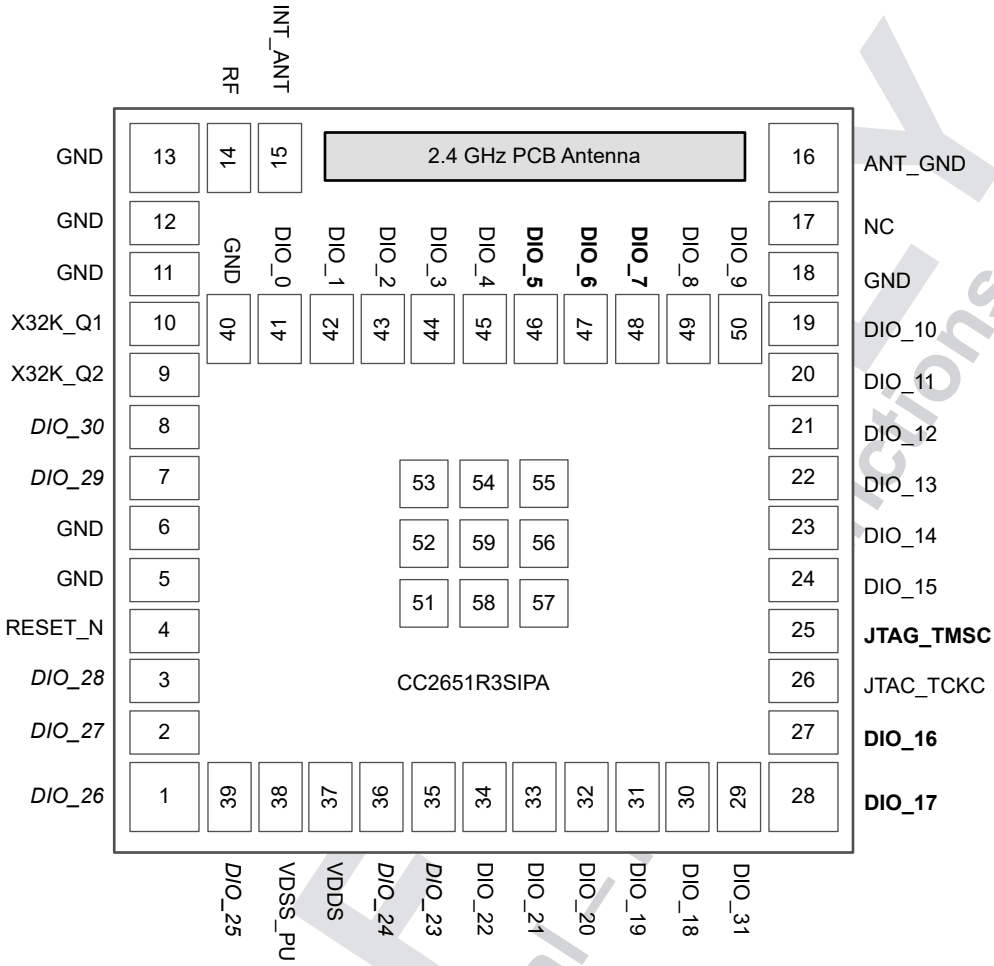


Figure 7-1. MOU (7-mm × 7-mm) Pinout, 0.5-mm Pitch (Top View)

The following I/O pins marked in Figure 7-1 in **bold** have high-drive capabilities:

- Pin 25, JTAG_TMSC
- Pin 27, DIO_16
- Pin 28, DIO_17
- Pin 46, DIO_5
- Pin 47, DIO_6
- Pin 48, DIO_7

The following I/O pins marked in Figure 7-1 in *italics* have analog capabilities:

- Pin 1, DIO_26
- Pin 2, DIO_27
- Pin 3, DIO_28
- Pin 7, DIO_29
- Pin 8, DIO_30
- Pin 35, DIO_23
- Pin 36, DIO_24
- Pin 39, DIO_25

7.2 Signal Descriptions – SIPA Package

Table 7-1. Signal Descriptions – SIPA Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
ANT_GND	16	—	—	Antenna GND
DIO_0	41	I/O	Digital	GPIO
DIO_1	42	I/O	Digital	GPIO
DIO_10	19	I/O	Digital	GPIO
DIO_11	20	I/O	Digital	GPIO
DIO_12	21	I/O	Digital	GPIO
DIO_13	22	I/O	Digital	GPIO
DIO_14	23	I/O	Digital	GPIO
DIO_15	24	I/O	Digital	GPIO
DIO_16	27	I/O	Digital	GPIO, JTAG_TDO, high-drive capability
DIO_17	28	I/O	Digital	GPIO, JTAG_TDI, high-drive capability
DIO_18	30	I/O	Digital	GPIO
DIO_19	31	I/O	Digital	GPIO
DIO_2	43	I/O	Digital	GPIO
DIO_20	32	I/O	Digital	GPIO
DIO_21	33	I/O	Digital	GPIO
DIO_22	34	I/O	Digital	GPIO
DIO_23	35	I/O	Digital or Analog	GPIO, analog capability
DIO_24	36	I/O	Digital or Analog	GPIO, analog capability
DIO_25	39	I/O	Digital or Analog	GPIO, analog capability
DIO_26	1	I/O	Digital or Analog	GPIO, analog capability
DIO_27	2	I/O	Digital or Analog	GPIO, analog capability
DIO_28	3	I/O	Digital or Analog	GPIO, analog capability
DIO_29	7	I/O	Digital or Analog	GPIO, analog capability
DIO_3	44	I/O	Digital	GPIO
DIO_30	8	I/O	Digital or Analog	GPIO, analog capability
DIO_31(1)	29	I/O	Digital	Supports only peripheral functionality. Does not support general purpose I/O functionality.
DIO_4	45	I/O	Digital	GPIO
DIO_5	46	I/O	Digital	GPIO, high-drive capability
DIO_6	47	I/O	Digital	GPIO, high-drive capability
DIO_7	48	I/O	Digital	GPIO, high-drive capability
DIO_8	49	I/O	Digital	GPIO
DIO_9	50	I/O	Digital	GPIO
GND	5	—	—	GND
GND	6	—	—	GND
GND	11	—	—	GND
GND	12	—	—	GND
GND	13	—	—	GND
GND	18	—	—	GND
GND	40	—	—	GND
GND	51-59	—	—	GND
INT_ANT	15		RF	RF connection to integral PCB antenna

Table 7-1. Signal Descriptions – SIPA Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
JTAG_TCKC	26	I/O	Digital	JTAG_TCKC
JTAG_TMSC	25	I/O	Digital	JTAG_TMSC, high-drive capability
NC	17	—	—	No Connect
RESET_N	4	I	Digital	Reset, active low. Internal pullup resistor to VDDS_PU
RF	14	—	RF	50 ohm RF port
VDDS	37	I/O	Digital	1.8-V to 3.8-V main SIP supply
VDSS_PU	38	—	Power	Power to reset internal pullup resistor
X32K_Q1	10	—	—	32-kHz crystal oscillator pin 1
X32K_Q2	9	—	—	32-kHz crystal oscillator pin 2

(1) PORT_ID = 0x00 is not supported. See the SimpleLink™ CC13x1x3, CC26x1x3 Wireless MCU Technical Reference Manual for further details.

7.3 Connections for Unused Pins and Modules

Table 7-2. Connections for Unused Pins – SIPA Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO	DIO_n	1-3 7-8 19-24 27-36 39 41-50	NC or GND	NC
32.768-kHz crystal	X32K_Q2	9	NC	NC
	X32K_Q1	10		
No Connects	NC	17	NC	NC

(1) NC = No connect

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

			MIN	MAX	UNIT
VDDS(3)	Supply voltage		–0.3	4.1	V
	Voltage on any digital pin(4) (5)		–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins, X32K_Q1, X32K_Q2		–0.3	VDDR + 0.3, max 2.25	V
V_{in}	Voltage on ADC input	Voltage scaling enabled	–0.3	VDDS	V
		Voltage scaling disabled, internal reference	–0.3	1.49	
		Voltage scaling disabled, VDDS as reference	–0.3	VDDS / 2.9	
	Input level, RF pin			5	dBm
T_{stg}	Storage temperature		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) VDDS_DCDC, VDDS2 and VDDS3 must be at the same potential as VDDS.
(4) Including analog capable DIOs.
(5) Injection current is not supported on any GPIO pin

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature(1)	–40	105	°C
Operating supply voltage (VDDS)	1.8	3.8	V
Rising supply voltage slew rate	0	100	mV/µs
Falling supply voltage slew rate	0	20	mV/µs

(1) For thermal resistance characteristics refer to Section 8.24.

8.4 Power Supply and Modules

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
VDDS Power-on-Reset (POR) threshold			1.1 - 1.55		V
VDDS Brown-out Detector (BOD)	Rising threshold		1.77		V
VDDS Brown-out Detector (BOD), before initial boot (1)	Rising threshold		1.70		V
VDDS Brown-out Detector (BOD)	Falling threshold		1.75		V

(1) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET_N pin

8.5 Power Consumption - Power Modes

When measured on the CC2651RSIPA-EM reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
Core Current Consumption				
I_{core}	Reset and Shutdown	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	150	nA
		Shutdown. No clocks running, no retention	100	
	Standby without cache retention	RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF	0.8	µA
		RTC running, CPU, 32KB RAM and (partial) register retention XOSC_LF	0.9	µA
	Standby with cache retention	RTC running, CPU, 32KB RAM and (partial) register retention. RCOSC_LF	2.4	µA
		RTC running, CPU, 32KB RAM and (partial) register retention. XOSC_LF	2.6	µA
	Idle	Supply Systems and RAM powered RCOSC_HF	650	µA
	Active	MCU running CoreMark at 48 MHz RCOSC_HF	2.91	mA
Peripheral Current Consumption				
I_{peri}	Peripheral power domain	Delta current with domain enabled	56	µA
	Serial power domain	Delta current with domain enabled	5.0	
	RF Core	Delta current with power domain enabled, clock enabled, RF core idle	144	
	µDMA	Delta current with clock enabled, module is idle	68.6	
	Timers	Delta current with clock enabled, module is idle(3)	102	
	I2C	Delta current with clock enabled, module is idle	12.1	
	I2S	Delta current with clock enabled, module is idle	30.8	
	SSI	Delta current with clock enabled, module is idle	71.7	
	UART	Delta current with clock enabled, module is idle(1)	147	
	CRYPTO (AES)	Delta current with clock enabled, module is idle(2)	28.1	
	TRNG	Delta current with clock enabled, module is idle	27.1	

(1) Only one UART running
(2) Only one SSI running
(3) Only one GPTimer running

8.6 Power Consumption - Radio Modes

When measured on the CC2651RSIPA-EM reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.

PARAMETER		TEST CONDITIONS	TYP	UNIT
	Radio receive current	2440 MHz	6.7	mA
	Radio transmit current 2.4 GHz PA (Bluetooth Low Energy)	0 dBm output power setting 2440 MHz	7.7	mA
		+5 dBm output power setting 2440 MHz	10	mA

8.7 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			8		KB
Supported flash erase cycles before failure, full bank(1) (5)		30			k Cycles
Supported flash erase cycles before failure, single sector(2)		60			k Cycles
Maximum number of write operations per row before sector erase(3)				83	Write Operations
Flash retention	105 °C	11.4			Years
Flash sector erase current	Average delta current		10.7		mA
Flash sector erase time(4)	Zero cycles		10		ms
	30k cycles			4000	ms
Flash write current	Average delta current, 4 bytes at a time		6.2		mA
Flash write time(4)	4 bytes at a time		21.6		ms

(1) A full bank erase is counted as a single erase cycle on each sector
(2) Up to 4 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(4) This number is dependent on Flash aging and increases over time and erase cycles
(5) Aborting flash during erase or program modes is not a safe operation.

8.8 Thermal Resistance Characteristics

THERMAL METRIC(1)		PACKAGE MOU (SIP) 59 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.7	°C/W(2)
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	12.4	°C/W(2)
$R_{\theta JB}$	Junction-to-board thermal resistance	32.2	°C/W(2)
ψ_{JT}	Junction-to-top characterization parameter	0.40	°C/W(2)
ψ_{JB}	Junction-to-board characterization parameter	32.0	°C/W(2)

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) °C/W = degrees Celsius per watt.

8.9 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2500	MHz

8.10 Bluetooth Low Energy - Receive (RX)

When measured on the CC2651RSIPA-EM reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125 kbps (LE Coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–103		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		>5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–300 / 300)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–320 / 240)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–125 / 125)		ppm
Co-channel rejection(1)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–1.5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		8 / 4.5(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 39(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		46 / 44(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		44 / 46(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		48 / 44(2)		dB
Selectivity, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		51 / 45(2)		dB
Selectivity, Image frequency(1)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		39		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4.5 / 44 (2)		dB
500 kbps (LE Coded)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–99		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–300 / 300)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–450 / 450)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–175 / 175)		ppm
Co-channel rejection(1)	Wanted signal at –72 dBm, modulated interferer in channel, BER = 10^{-3}		–3.5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		8 / 4(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 37(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		46 / 42(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		45 / 43(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		46 / 45(2)		dB
Selectivity, ±7 MHz	Wanted signal at –72 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		49 / 45(2)		dB
Selectivity, Image frequency(1)	Wanted signal at –72 dBm, modulated interferer at image frequency, BER = 10^{-3}		37		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –72 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4 / 46(2)		dB

When measured on the CC2651RSIPA-EM reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 Mbps (LE 1M)					
Receiver sensitivity	Differential mode. BER = 10^{-3}		–96		dBm
Receiver saturation	Differential mode. BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–350 / 350)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–750 / 750)		ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 4(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz,BER = 10^{-3}		40 / 33(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		36 / 41(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		40 / 45(2)		dB
Selectivity, ±5 MHz or more(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = 10^{-3}		40		dB
Selectivity, image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		33		dB
Selectivity, image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4 / 41(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–10		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–18		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–2		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–42		dBm
Spurious emissions, 30 to 1000 MHz	Measurement in a 50-Ω single-ended load.		< –59		dBm
Spurious emissions, 1 to 12.75 GHz	Measurement in a 50-Ω single-ended load.		< –47		dBm
RSSI dynamic range			70		dB
RSSI accuracy			±4		dB
2 Mbps (LE 2M)					
Receiver sensitivity	Differential mode. Measured at SMA connector, BER = 10^{-3}		–91		dBm
Receiver saturation	Differential mode. Measured at SMA connector, BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–500 / 500)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–700 / 750)		ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel,BER = 10^{-3}		–7		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = 10^{-3}		8 / 4(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		36 / 36(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		37 / 36(2)		dB
Selectivity, image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		4		dB

When measured on the CC2651RSIPA-EM reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, image frequency ±2 MHz(1)	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = 10^{-3}		–7 / 36(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–16		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–21		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–15		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–12		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level		–38		dBm

(1) Numbers given as I/C dB
(2) X / Y, where X is +N MHz and Y is –N MHz
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification

8.11 Bluetooth Low Energy - Transmit (TX)

When measured on the CC2651RSIPA-EM reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power	Differential mode, delivered to a single-ended 50 Ω load through a balun			5		dBm
Output power programmable range	Differential mode, delivered to a single-ended 50 Ω load through a balun			26		dB
Spurious emissions and harmonics						
Spurious emissions	f < 1 GHz, outside restricted bands	+5 dBm setting		< –36		dBm
	f < 1 GHz, restricted bands ETSI			< –54		dBm
	f < 1 GHz, restricted bands FCC			< –55		dBm
	f > 1 GHz, including harmonics			< –42		dBm
Harmonics	Second harmonic			< –42		dBm
	Third harmonic			< –42		dBm

8.12 Zigbee - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX

When measured on the CC2651RSIPA-EM reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Receiver sensitivity	PER = 1%		–99		dBm
Receiver saturation	PER = 1%		> 5		dBm
Adjacent channel rejection	Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1%		36		dB
Alternate channel rejection	Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1%		57		dB
Channel rejection, ±15 MHz or more	Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		59		dB
Blocking and desensitization, 5 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		57		dB
Blocking and desensitization, 10 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, 20 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, 50 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		66		dB
Blocking and desensitization, –5 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		60		dB
Blocking and desensitization, –10 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		60		dB
Blocking and desensitization, –20 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –50 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Spurious emissions, 30 MHz to 1000 MHz	Measurement in a 50-Ω single-ended load		–66		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Measurement in a 50-Ω single-ended load		–53		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> 350		ppm
Symbol rate error tolerance	Difference between incoming symbol rate and the internally generated symbol rate		> 1000		ppm
RSSI dynamic range			95		dB
RSSI accuracy			±4		dB

8.13 Zigbee - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX

When measured on the CC2651RSIPA-EM reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
General Parameters						
Max output power	Differential mode, delivered to a single-ended 50-Ω load through a balun			5		dBm
Output power programmable range	Differential mode, delivered to a single-ended 50-Ω load through a balun			25		dB
Spurious emissions and harmonics						
Spurious emissions (1)	f < 1 GHz, outside restricted bands	+5 dBm setting		< -36		dBm
	f < 1 GHz, restricted bands ETSI			< -47		dBm
	f < 1 GHz, restricted bands FCC			< -55		dBm
	f > 1 GHz, including harmonics			< –42		dBm
Harmonics	Second harmonic			< -42		dBm
	Third harmonic			< -42		dBm
IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)						
Error vector magnitude	+5 dBm setting			2		%

(1) To meet the FCC 15.247 Part 15 (US) Band Edge requirement, Channel 26 is reduced by 3 dBm when using the integrated antenna. When using the external antenna option, Channel 26 output power is reduding by 4 dBm, with a max allowable antenna gain of 3.3 dBi.

8.14 Timing and Switching Characteristics

8.14.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

8.14.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0 V (unless otherwise noted). The times listed here do not include software overhead.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset to Active(1)			850 - 3000		µs
MCU, Shutdown to Active(1)			850 - 3000		µs
MCU, Standby to Active			160		µs
MCU, Active to Standby			36		µs
MCU, Idle to Active			14		µs

(1) The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.

8.14.3 Clock Specifications

8.14.3.1 48 MHz Crystal Oscillator (XOSC_HF)

Measured on a Texas Instruments reference design with integrated 48 MHz crystal including parameters based on external manufacturer's crystal specification at T_c = 25 °C, V_{DDS} = 3.0 V at initial time, unless otherwise noted.

PARAMETER	MIN	TYP	MAX	UNIT
Crystal frequency		48		MHz
Start-up time(1)		200		µs
Crystal frequency tolerance(2)	-16		18	ppm
Crystal aging(2)	-4		2	ppm/year

(1) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(2) External manufacturer's crystal specification

8.14.3.2 48 MHz RC Oscillator (RCOSC_HF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1		%
Calibrated frequency accuracy(1)		±0.25		%
Start-up time		5		µs

(1) Accuracy relative to the calibration source (XOSC_HF)

8.14.3.3 32.768 kHz Crystal Oscillator (XOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
	Crystal frequency		32.768		kHz
ESR	Equivalent series resistance		30	100	kΩ
C_L	Crystal load capacitance	6	7(1)	12	pF

(1) Default load capacitance using TI reference designs including parasitic capacitance. Crystals with different load capacitance may be used.

8.14.3.4 32 kHz RC Oscillator (RCOSC_LF)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
Frequency			32.8		kHz
Calibrated RTC variation(1)	Calibrated periodically against XOSC_HF(2)		±600(3)		ppm
Temperature coefficient.			50		ppm/°C

(1) When using RCOSC_LF as source for the low frequency system clock (SCLK_LF), the accuracy of the SCLK_LF-derived Real Time Clock (RTC) can be improved by measuring RCOSC_LF relative to XOSC_HF and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.
(2) TI driver software calibrates the RTC every time XOSC_HF is enabled.
(3) Some device's variation can exceed 1000 ppm. Further calibration will not improve variation.

8.14.4 Synchronous Serial Interface (SSI) Characteristics

8.14.4.1 Synchronous Serial Interface (SSI) Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER NO.	PARAMETER		MIN	TYP	MAX	UNIT
S1	t_{clk_per}	SSIClk cycle time	12		65024	System Clocks (2)
S2(1)	t_{clk_high}	SSIClk high time		0.5		t_{clk_per}
S3(1)	t_{clk_low}	SSIClk low time		0.5		t_{clk_per}

(1) Refer to SSI timing diagrams Figure 8-1, Figure 8-2, and Figure 8-3.
(2) When using the TI-provided Power driver, the SSI system clock is always 48 MHz.

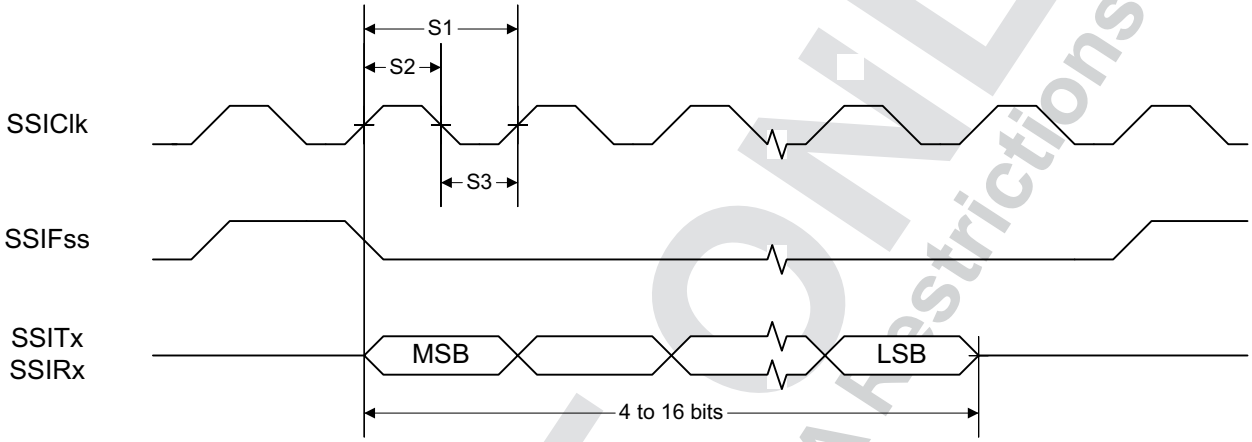


Figure 8-1. SSI Timing for TI Frame Format (FRF = 01), Single Transfer Timing Measurement

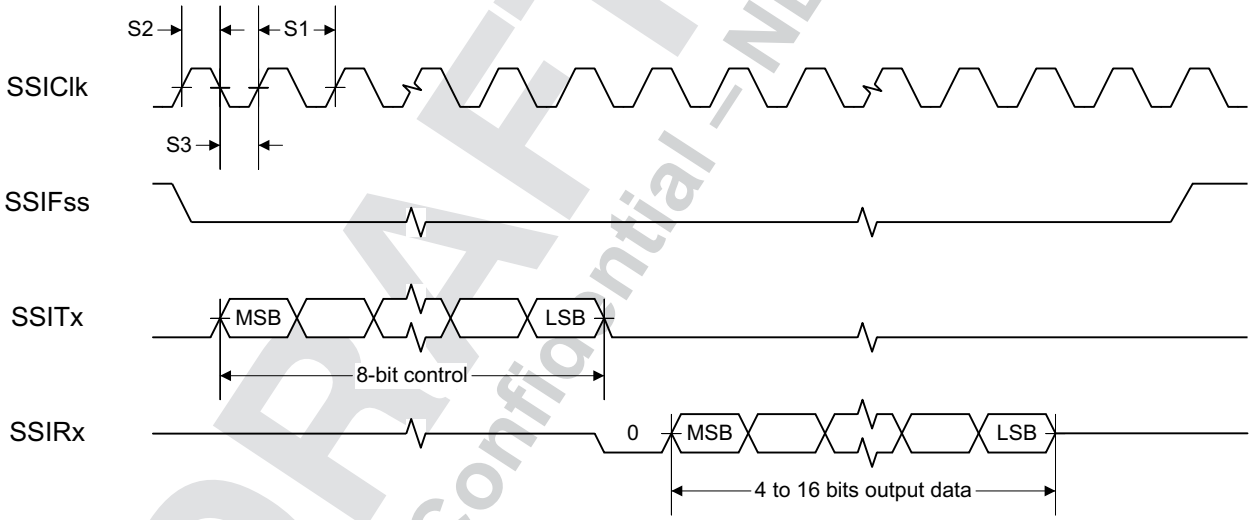


Figure 8-2. SSI Timing for MICROWIRE Frame Format (FRF = 10), Single Transfer

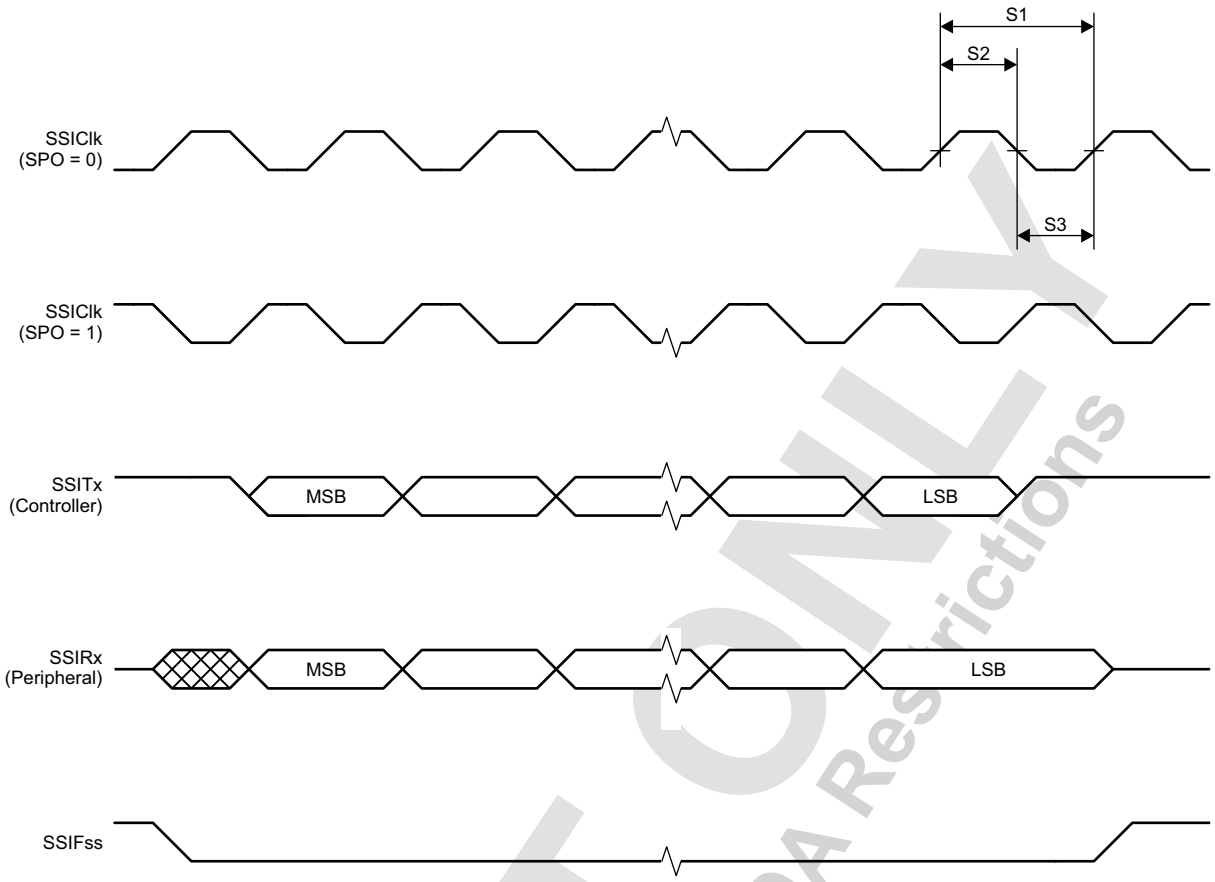


Figure 8-3. SSI Timing for SPI Frame Format (FRF = 00), With SPH = 1

8.14.5 UART

8.14.5.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

8.15 Peripheral Characteristics

8.15.1 ADC

Analog-to-Digital Converter (ADC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		VDDS	V
	Resolution			12		Bits
	Sample Rate				200	ksps
	Offset	Internal 4.3 V equivalent reference(2)		–0.24		LSB
	Gain error	Internal 4.3 V equivalent reference(2)		7.14		LSB
DNL(4)	Differential nonlinearity			>–1		LSB
INL	Integral nonlinearity			±4		LSB
ENOB	Effective number of bits	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		9.8		Bits
		Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone, DC/DC enabled		9.8		
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		10.1		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		11.1		
		Internal reference, voltage scaling disabled, 14-bit mode, 200 kSamples/s, 300 Hz input tone (5)		11.3		
		Internal reference, voltage scaling disabled, 15-bit mode, 200 kSamples/s, 300 Hz input tone (5)		11.6		
THD	Total harmonic distortion	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		–65		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		–70		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		–72		
SINAD, SNDR	Signal-to-noise and distortion ratio	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		60		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		63		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		68		
SFDR	Spurious-free dynamic range	Internal 4.3 V equivalent reference(2), 200 kSamples/s, 9.6 kHz input tone		70		dB
		VDDS as reference, 200 kSamples/s, 9.6 kHz input tone		73		
		Internal reference, voltage scaling disabled, 32 samples average, 200 kSamples/s, 300 Hz input tone		75		
	Conversion time	Serial conversion, time-to-output, 24 MHz clock		50		Clock Cycles
	Current consumption	Internal 4.3 V equivalent reference(2)		0.42		mA
	Current consumption	VDDS as reference		0.6		mA
	Reference voltage	Equivalent fixed internal reference (input voltage scaling enabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1		4.3(2) (3)		V
	Reference voltage	Fixed internal reference (input voltage scaling disabled). For best accuracy, the ADC conversion should be initiated through the TI-RTOS API in order to include the gain/offset compensation factors stored in FCFG1. This value is derived from the scaled value (4.3 V) as follows: V_{ref} = 4.3 V × 1408 / 4095		1.48		V
	Reference voltage	VDDS as reference, input voltage scaling enabled		VDDS		V
	Reference voltage	VDDS as reference, input voltage scaling disabled		VDDS / 2.82(3)		V

T_c = 25 °C, V_{DDS} = 3.0 V and voltage scaling enabled, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input impedance	200 kSamples/s, voltage scaling enabled. Capacitive input, Input impedance depends on sampling frequency and sampling time		>1		MΩ

(1) Using IEEE Std 1241-2010 for terminology and test methods
(2) Input signal scaled down internally before conversion, as if voltage range was 0 to 4.3 V
(3) Applied voltage must be within Absolute Maximum Ratings (see Section 8.1) at all times
(4) No missing codes
(5) ADC_output = Σ(4^n samples) >> n, n = desired extra bits

8.15.2 DAC

8.15.2.1 Digital-to-Analog Converter (DAC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters						
	Resolution			8		Bits
V_{DDS}	Supply voltage	Any load, any V_{REF}, pre-charge OFF, DAC charge-pump ON	1.8		3.8	V
		External Load(4), any V_{REF}, pre-charge OFF, DAC charge-pump OFF	2.0		3.8	
		Any load, V_{REF} = DCOUPL, pre-charge ON	2.6		3.8	
F_{DAC}	Clock frequency	Buffer ON (recommended for external load)	16		250	kHz
		Buffer OFF (internal load)	16		1000	
	Voltage output settling time	V_{REF} = VDDS, buffer OFF, internal load		13		1 / F_{DAC}
		V_{REF} = VDDS, buffer ON, external capacitive load = 20 pF(3)		13.8		
	External capacitive load			20	200	pF
	External resistive load		10			MΩ
	Short circuit current				400	µA
Z_{MAX}	Max output impedance Vref = VDDS, buffer ON, CLK 250 kHz	VDDS = 3.8 V, DAC charge-pump OFF		50.8		kΩ
		VDDS = 3.0 V, DAC charge-pump ON		51.7		
		VDDS = 3.0 V, DAC charge-pump OFF		53.2		
		VDDS = 2.0 V, DAC charge-pump ON		48.7		
		VDDS = 2.0 V, DAC charge-pump OFF		70.2		
		VDDS = 1.8 V, DAC charge-pump ON		46.3		
		VDDS = 1.8 V, DAC charge-pump OFF		88.9		
Internal Load - Continuous Time Comparator / Low Power Clocked Comparator						
DNL	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator F_{DAC} = 250 kHz		±1		LSB(1)
	Differential nonlinearity	V_{REF} = VDDS, load = Continuous Time Comparator or Low Power Clocked Comparator F_{DAC} = 16 kHz		±1.2		
	Offset error(2) Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V		±0.64		LSB(1)
		V_{REF} = VDDS= 3.0 V		±0.81		
		V_{REF} = VDDS = 1.8 V		±1.27		
		V_{REF} = DCOUPL, pre-charge ON		±3.43		
		V_{REF} = DCOUPL, pre-charge OFF		±2.88		
		V_{REF} = ADCREF		±2.37		
	Offset error(2) Load = Low Power Clocked Comparator	V_{REF} = VDDS= 3.8 V		±0.78		LSB(1)
		V_{REF} = VDDS = 3.0 V		±0.77		
		V_{REF} = VDDS= 1.8 V		±3.46		
		V_{REF} = DCOUPL, pre-charge ON		±3.44		
		V_{REF} = DCOUPL, pre-charge OFF		±4.70		
		V_{REF} = ADCREF		±4.11		
	Max code output voltage variation(2) Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V		±1.53		LSB(1)
		V_{REF} = VDDS = 3.0 V		±1.71		
		V_{REF} = VDDS= 1.8 V		±2.10		
		V_{REF} = DCOUPL, pre-charge ON		±6.00		
		V_{REF} = DCOUPL, pre-charge OFF		±3.85		
		V_{REF} = ADCREF		±5.84		

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Max code output voltage variation[2] Load = Low Power Clocked Comparator	V_{REF} = VDDS= 3.8 V		±2.92		LSB[1]
		V_{REF} =VDDS= 3.0 V		±3.06		
		V_{REF} = VDDS= 1.8 V		±3.91		
		V_{REF} = DCOUPL, pre-charge ON		±7.84		
		V_{REF} = DCOUPL, pre-charge OFF		±4.06		
		V_{REF} = ADCREF		±6.94		
	Output voltage range[2] Load = Continuous Time Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS = 3.8 V, code 255		3.62		
		V_{REF} = VDDS= 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.86		
		V_{REF} = VDDS= 1.8 V, code 1		0.01		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.01		
		V_{REF} = ADCREF, code 255		1.41		
	Output voltage range[2] Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS= 3.8 V, code 255		3.61		
		V_{REF} = VDDS= 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.85		
		V_{REF} = VDDS = 1.8 V, code 1		0.01		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.01		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.21		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.01		
		V_{REF} = ADCREF, code 255		1.41		
External Load						
INL	Integral nonlinearity	V_{REF} = VDDS, F_{DAC} = 250 kHz		±1		LSB[1]
		V_{REF} = DCOUPL, F_{DAC} = 250 kHz		±1		
		V_{REF} = ADCREF, F_{DAC} = 250 kHz		±1		
DNL	Differential nonlinearity	V_{REF} = VDDS, F_{DAC} = 250 kHz		±1		LSB[1]
	Offset error	V_{REF} = VDDS= 3.8 V		±0.20		LSB[1]
		V_{REF} = VDDS= 3.0 V		±0.25		
		V_{REF} = VDDS = 1.8 V		±0.45		
		V_{REF} = DCOUPL, pre-charge ON		±1.55		
		V_{REF} = DCOUPL, pre-charge OFF		±1.30		
		V_{REF} = ADCREF		±1.10		
	Max code output voltage variation	V_{REF} = VDDS= 3.8 V		±0.60		LSB[1]
		V_{REF} = VDDS= 3.0 V		±0.55		
		V_{REF} = VDDS= 1.8 V		±0.60		
		V_{REF} = DCOUPL, pre-charge ON		±3.45		
		V_{REF} = DCOUPL, pre-charge OFF		±2.10		
		V_{REF} = ADCREF		±1.90		

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Output voltage range Load = Low Power Clocked Comparator	V_{REF} = VDDS = 3.8 V, code 1		0.03		V
		V_{REF} = VDDS = 3.8 V, code 255		3.61		
		V_{REF} = VDDS = 3.0 V, code 1		0.02		
		V_{REF} = VDDS= 3.0 V, code 255		2.85		
		V_{REF} = VDDS= 1.8 V, code 1		0.02		
		V_{REF} = VDDS = 1.8 V, code 255		1.71		
		V_{REF} = DCOUPL, pre-charge OFF, code 1		0.02		
		V_{REF} = DCOUPL, pre-charge OFF, code 255		1.20		
		V_{REF} = DCOUPL, pre-charge ON, code 1		1.27		
		V_{REF} = DCOUPL, pre-charge ON, code 255		2.46		
		V_{REF} = ADCREF, code 1		0.02		
		V_{REF} = ADCREF, code 255		1.42		

(1) 1 LSB (V_{REF} 3.8 V/3.0 V/1.8 V/DCOUPL/ADCREF) = 14.10 mV/11.13 mV/6.68 mV/4.67 mV/5.48 mV
(2) Includes comparator offset
(3) A load > 20 pF will increases the settling time
(4) Keysight 34401A Multimeter

8.15.3 Temperature and Battery Monitor

8.15.3.1 Temperature Sensor

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			2		°C
Accuracy	-40 °C to 0 °C		±5.0		°C
Accuracy	0 °C to 105 °C		±2.5		°C
Supply voltage coefficient(1)			3.6		°C/V

(1) The temperature sensor is automatically compensated for VDDS variation when using the TI-provided driver.

8.15.3.2 Battery Monitor

Measured on a Texas Instruments reference design with T_c = 25 °C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution			25		mV
Range		1.8		3.8	V
Integral nonlinearity (max)			23		mV
Accuracy	VDDS = 3.0 V		22.5		mV
Offset error			-32		mV
Gain error			-1		%

8.15.4 Comparators

8.15.4.1 Continuous Time Comparator

T_c = 25°C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage range(1)		0		V_{DDS}	V
Offset	Measured at V_{DDS} / 2		±5		mV
Decision time	Step from –10 mV to 10 mV		0.78		µs
Current consumption	Internal reference		8.6		µA

(1) The input voltages can be generated externally and connected throughout I/Os or an internal reference voltage can be generated using the DAC

8.15.5 Current Source

8.15.5.1 Programmable Current Source

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current source programmable output range (logarithmic range)			0.25 - 20		µA
Resolution			0.25		µA

8.15.6 GPIO

8.15.6.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 1.8 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		1.56		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.24		V
GPIO VOH at 4 mA load	IOCURR = 1		1.59		V
GPIO VOL at 4 mA load	IOCURR = 1		0.21		V
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		73		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		19		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.73		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.35		V
T_A = 25 °C, V_{DDS} = 3.0 V					
GPIO VOH at 8 mA load	IOCURR = 2, high-drive GPIOs only		2.59		V
GPIO VOL at 8 mA load	IOCURR = 2, high-drive GPIOs only		0.42		V
GPIO VOH at 4 mA load	IOCURR = 1		2.63		V
GPIO VOL at 4 mA load	IOCURR = 1		0.40		V
T_A = 25 °C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		282		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		110		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.55		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.42		V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	0.8*V_{DDS}			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			0.2*V_{DDS}	V

8.16 Typical Characteristics

All measurements in this section are done with T_c = 25 °C and V_{DDS} = 3.0 V, unless otherwise noted. See *Recommended Operating Conditions*, Section 8.3, for device limits. Values exceeding these limits are for reference only.

8.16.1 MCU Current

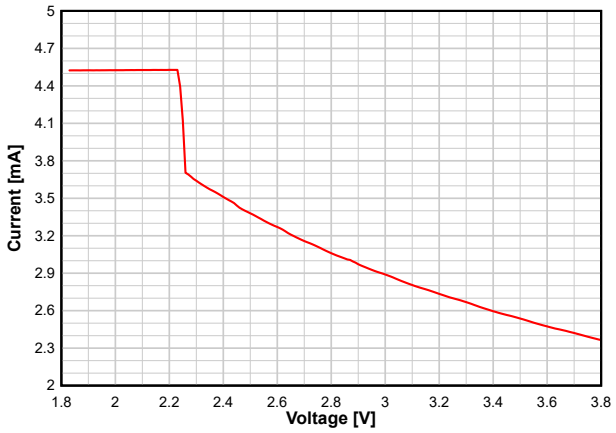


Figure 8-4. Active Mode (MCU) Current vs. Supply Voltage (VDDS)

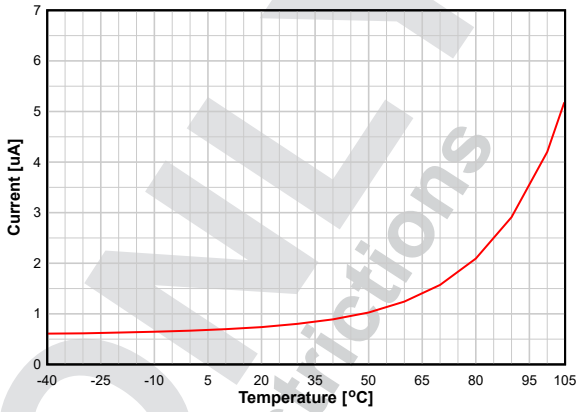


Figure 8-5. Standby Mode (MCU) Current vs. Temperature

8.16.2 RX Current

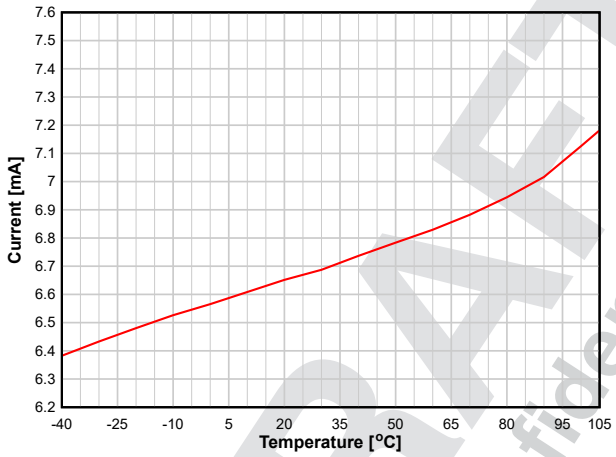


Figure 8-6. RX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz)

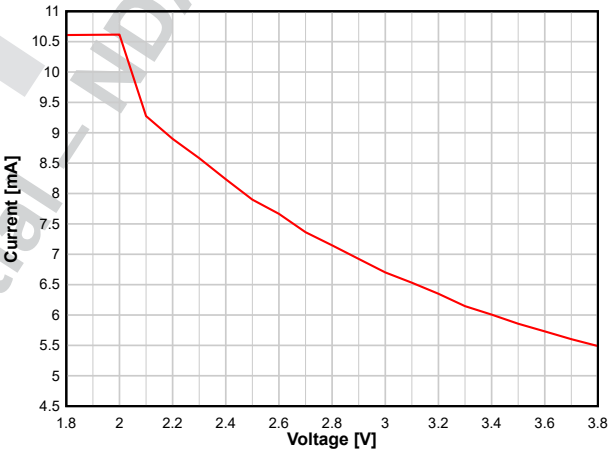


Figure 8-7. RX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

8.16.3 TX Current

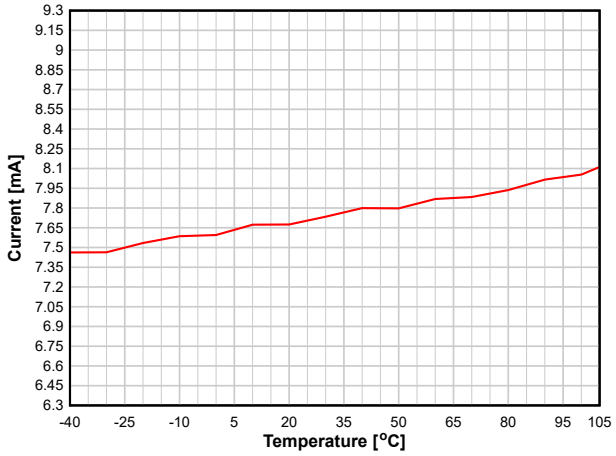


Figure 8-8. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, 0 dBm)

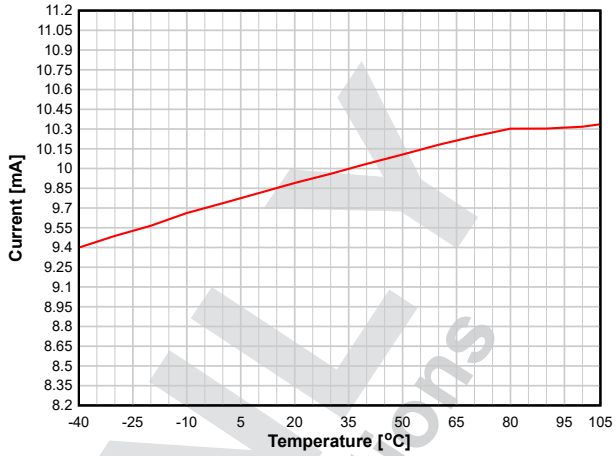


Figure 8-9. TX Current vs. Temperature (BLE 1 Mbps, 2.44 GHz, +5 dBm)

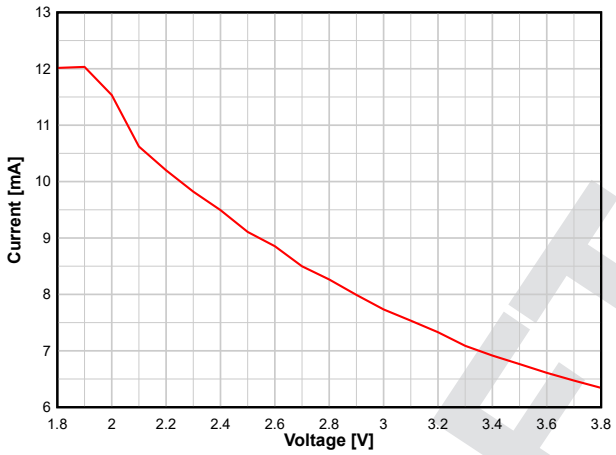


Figure 8-10. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, 0 dBm)

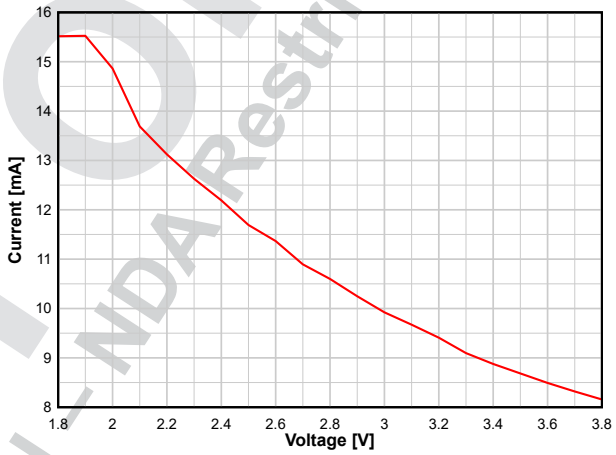


Figure 8-11. TX Current vs. Supply Voltage (VDDS) (BLE 1 Mpbs, 2.44 GHz, +5 dBm)

Table 8-1 shows the typical TX current and output power for different output power settings.

Table 8-1. Typical TX Current and Output Power

CC2652R at 2.4 GHz, VDDS = 3.0 V (Measured on CC2651RSIPA-EM)			
txPower	**TX Power Setting (SmartRF Studio)**	**Typical Output Power [dBm]**	**Typical Current Consumption [mA]**
0xA42E	5	4.4	9.9
0x601E	4	3.3	9.2
0x246A	3	2.5	8.8
0x2E64	2	1.7	8.4
0x20A5	1	0.7	8.0
0x20A2	0	0.1	7.7
0x08DC	-5	-4.6	6.4
0x00D2	-10	-9.0	5.6
0x00CD	-15	-12.7	5.2
0x00C8	-20	-18.2	4.8

8.16.4 RX Performance

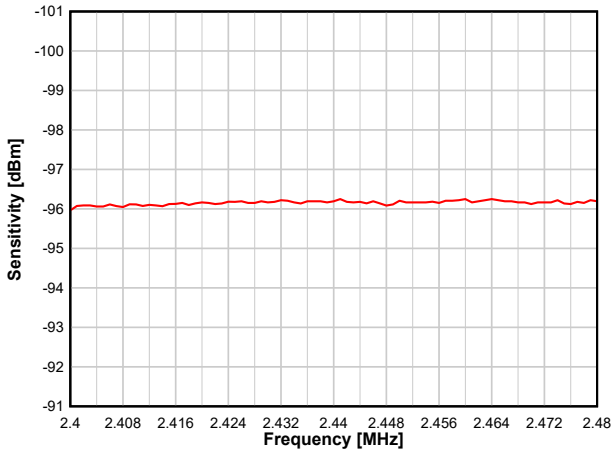


Figure 8-12. Sensitivity vs. Frequency (BLE 1 Mbps, 2.44 GHz)

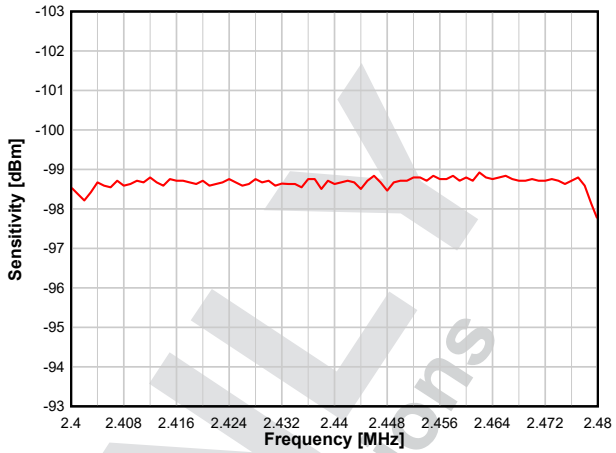


Figure 8-13. Sensitivity vs. Frequency (250 kbps, 2.44 GHz)

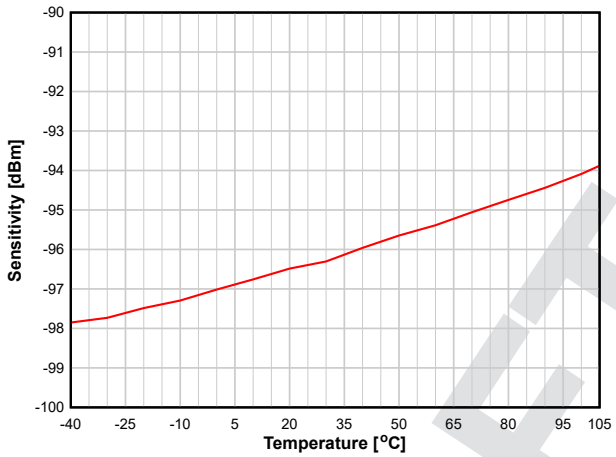


Figure 8-14. Sensitivity vs. Temperature (BLE 1 Mbps, 2.44 GHz)

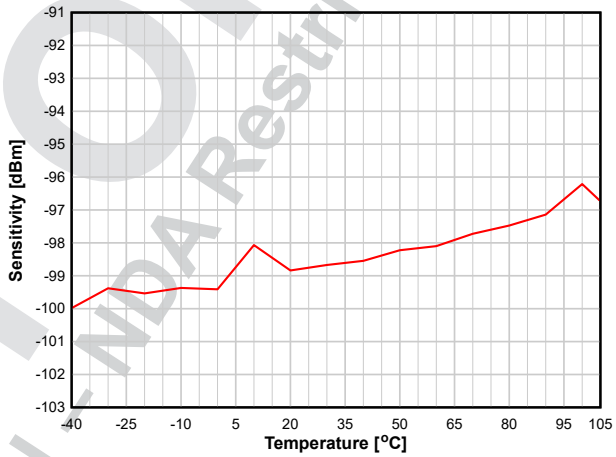


Figure 8-15. Sensitivity vs. Temperature (250 kbps, 2.44 GHz)

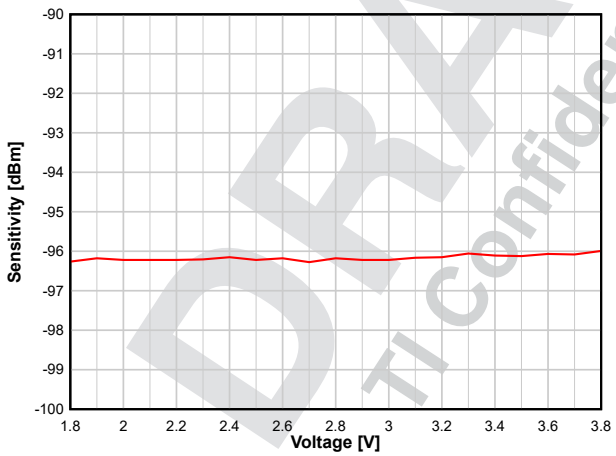


Figure 8-16. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz)

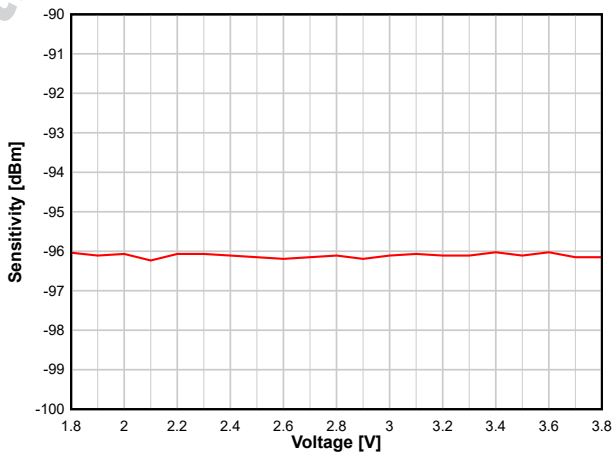


Figure 8-17. Sensitivity vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, DCDC Off)

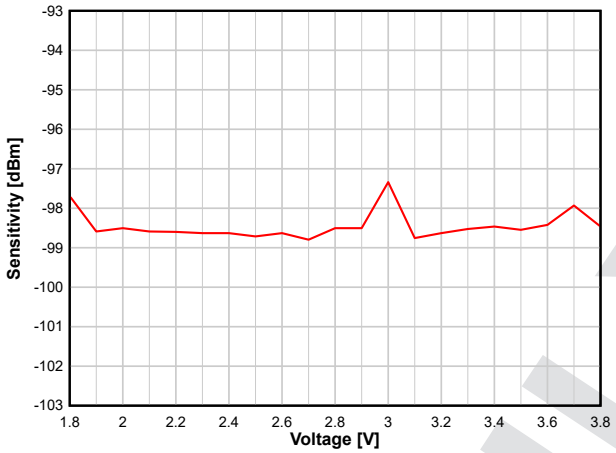


Figure 8-18. Sensitivity vs. Supply Voltage (VDDS) (250 kbps, 2.44 GHz)

8.16.5 TX Performance

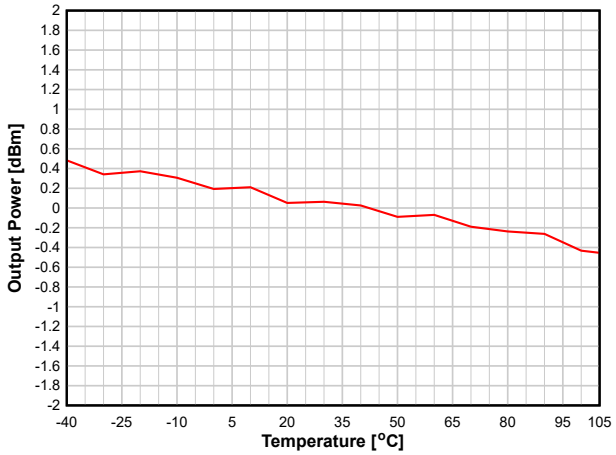


Figure 8-19. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, 0 dBm)

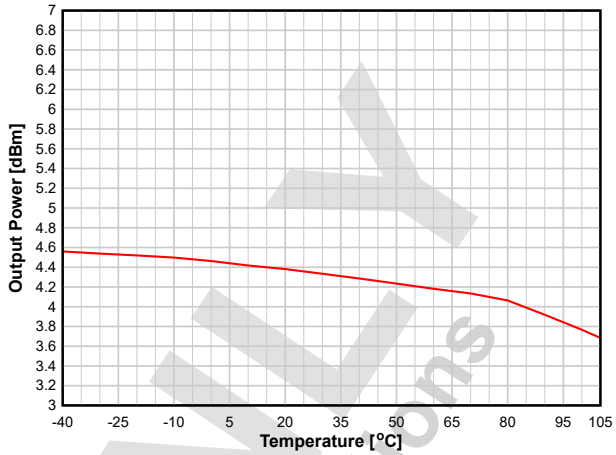


Figure 8-20. Output Power vs. Temperature (BLE 1 Mbps, 2.44 GHz, +5 dBm)

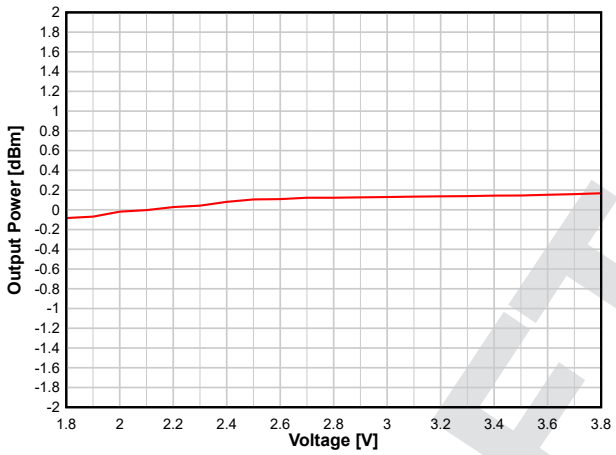


Figure 8-21. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, 0 dBm)

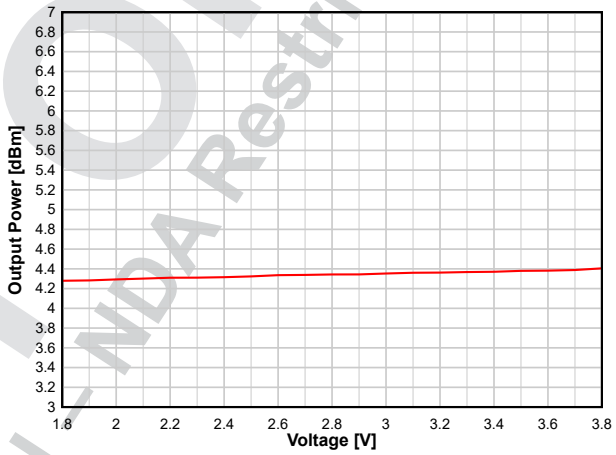


Figure 8-22. Output Power vs. Supply Voltage (VDDS) (BLE 1 Mbps, 2.44 GHz, +5 dBm)

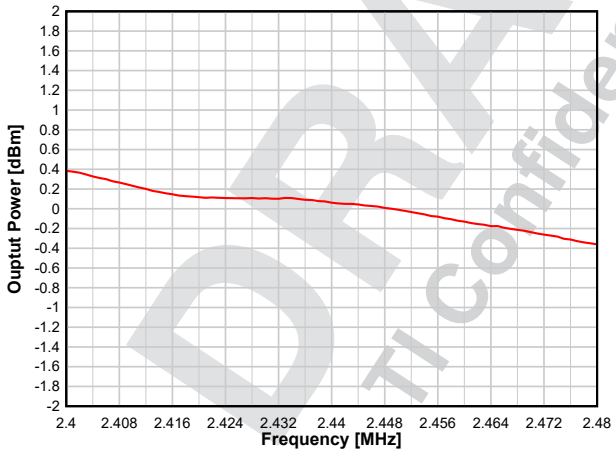


Figure 8-23. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, 0 dBm)

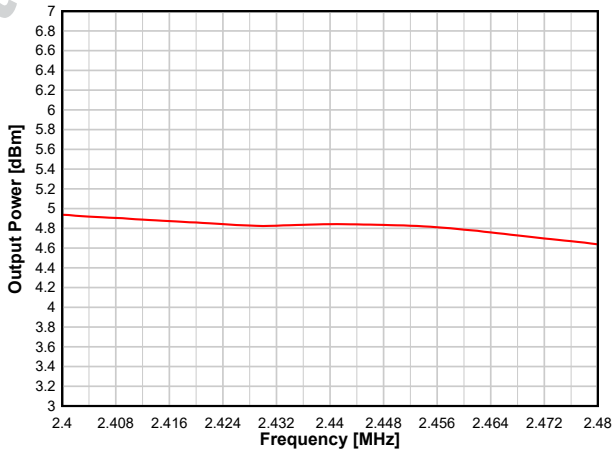


Figure 8-24. Output Power vs. Frequency (BLE 1 Mbps, 2.44 GHz, +5 dBm)

8.16.6 ADC Performance

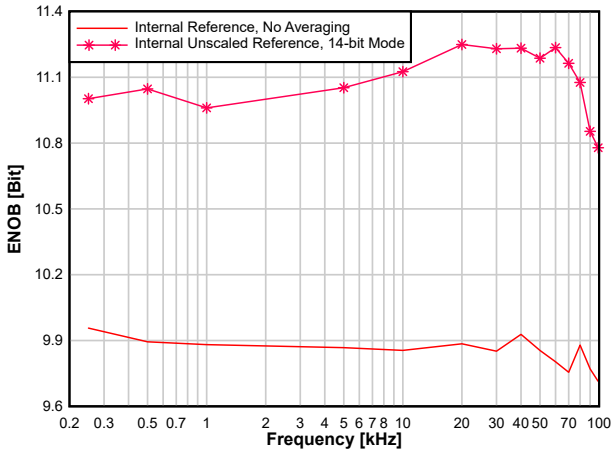


Figure 8-25. ENOB vs. Input Frequency

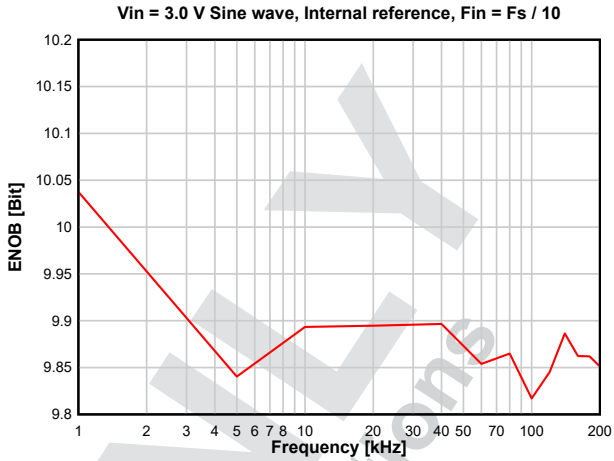


Figure 8-26. ENOB vs. Sampling Frequency

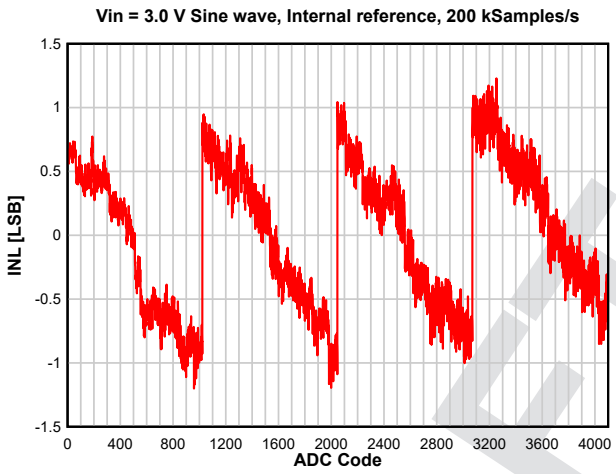


Figure 8-27. INL vs. ADC Code

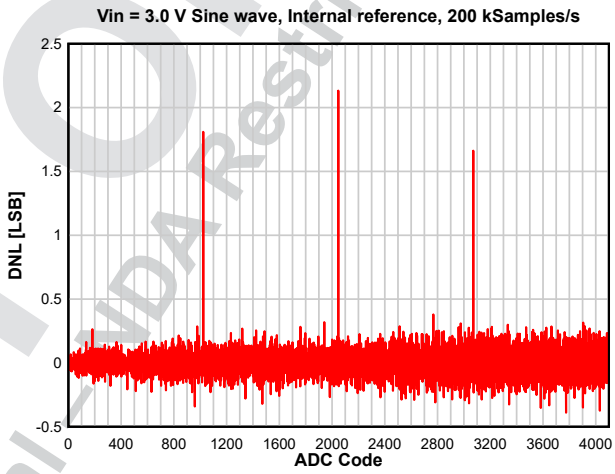


Figure 8-28. DNL vs. ADC Code

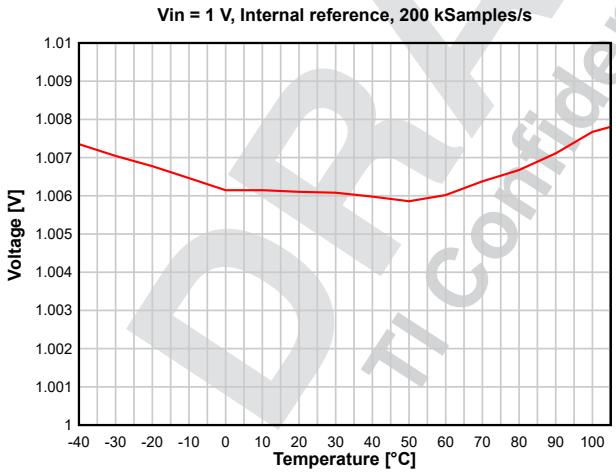


Figure 8-29. ADC Accuracy vs. Temperature

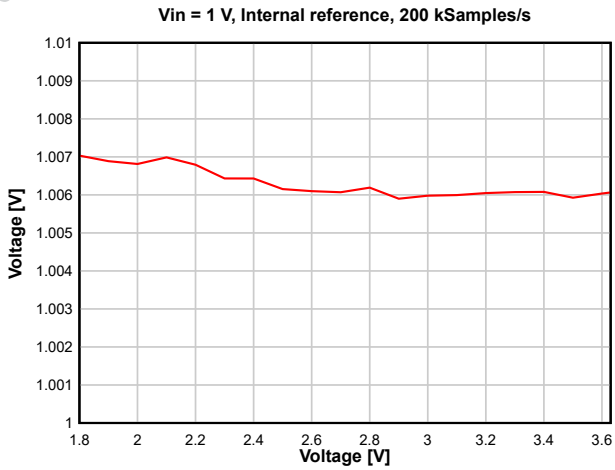


Figure 8-30. ADC Accuracy vs. Supply Voltage (VDDS)

9 Detailed Description

9.1 Overview

Section 4 shows the core modules of the CC2651R3SIPA device.

9.2 System CPU

The CC2651R3SIPA SimpleLink™ Wireless MCU contains an Arm® Cortex®-M4 system CPU, which runs the application and the higher layers of radio protocol stacks.

The system CPU is the foundation of a high-performance, low-cost platform that meets the system requirements of minimal memory implementation, and low-power consumption, while delivering outstanding computational performance and exceptional system response to interrupts.

Its features include the following:

- ARMv7-M architecture optimized for small-footprint embedded applications
- Arm Thumb®-2 mixed 16- and 32-bit instruction set delivers the high performance expected of a 32-bit Arm core in a compact memory size
- Fast code execution permits increased sleep mode time
- Deterministic, high-performance interrupt handling for time-critical applications
- Single-cycle multiply instruction and hardware divide
- Hardware division and fast digital-signal-processing oriented multiply accumulate
- Saturating arithmetic for signal processing
- Full debug with data matching for watchpoint generation
  - Data Watchpoint and Trace Unit (DWT)
  - JTAG Debug Access Port (DAP)
  - Flash Patch and Breakpoint Unit (FPB)
- Trace support reduces the number of pins required for debugging and tracing
  - Instrumentation Trace Macrocell Unit (ITM)
  - Trace Port Interface Unit (TPIU) with asynchronous serial wire output (SWO)
- Optimized for single-cycle flash memory access
- Tightly connected to 8-KB 4-way random replacement cache for minimal active power consumption and wait states
- Ultra-low-power consumption with integrated sleep modes
- 48 MHz operation
- 1.25 DMIPS per MHz

9.3 Radio (RF Core)

The RF Core is a highly flexible and future proof radio module which contains an Arm Cortex-M0 processor that interfaces the analog RF and base-band circuitry, handles data to and from the system CPU side, and assembles the information bits in a given packet structure. The RF core offers a high level, command-based API to the main CPU that configurations and data are passed through. The Arm Cortex-M0 processor is not programmable by customers and is interfaced through the TI-provided RF driver that is included with the SimpleLink Software Development Kit (SDK).

The RF core can autonomously handle the time-critical aspects of the radio protocols, thus offloading the main CPU, which reduces power and leaves more resources for the user application. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The various physical layer radio formats are partly built as a software defined radio where the radio behavior is either defined by radio ROM contents or by non-ROM radio formats delivered in form of firmware patches with the SimpleLink SDKs. This allows the radio platform to be updated for support of future versions of standards even with over-the-air (OTA) updates while still using the same silicon.

9.3.1 Bluetooth 5.2 Low Energy

The RF Core offers full support for Bluetooth 5.2 Low Energy, including the high-sped 2-Mbps physical layer and the 500-kbps and 125-kbps long range PHYs (Coded PHY) through the TI provided Bluetooth 5.2 stack or through a high-level Bluetooth API. The Bluetooth 5.2 PHY and part of the controller are in radio and system ROM, providing significant savings in memory usage and more space available for applications.

The new high-speed mode allows data transfers up to 2 Mbps, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.2 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mbps, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.2 enables fast, reliable firmware updates.

9.3.2 802.15.4 (Zigbee)

Through a dedicated IEEE radio API, the RF Core supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in the Zigbee protocol. The 802.15.4 PHY and MAC are in radio and system ROM. TI also provides royalty-free protocol stacks for Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

9.4 Memory

The up to 352-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. The last flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static RAM (SRAM) is a single 32-KB block and can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers.

To improve code execution speed and lower power when executing code from nonvolatile memory, a 4-way nonassociative 8-KB cache is enabled by default to cache and prefetch instructions read by the system CPU. The cache can be used as a general-purpose RAM by enabling this feature in the Customer Configuration Area (CCFG).

The ROM contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

9.5 Cryptography

The CC2651R3SIPA device comes with a wide set of cryptography-related hardware accelerators, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread. The hardware accelerator modules are:

- **True Random Number Generator (TRNG)** module provides a true, nondeterministic noise source for the purpose of generating keys, initialization vectors (IVs), and other random number requirements. The TRNG is built on 24 ring oscillators that create unpredictable output to feed a complex nonlinear-combinatorial circuit.
- **Advanced Encryption Standard (AES)** with 128 bit key lengths

Together with the hardware accelerator module, a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform. The TI provided cryptography drivers are:

- **Key Agreement Schemes**
  - Elliptic curve Diffie–Hellman with static or ephemeral keys (ECDH and ECDHE)
  - Elliptic curve Password Authenticated Key Exchange by Juggling (ECJ-PAKE)
- **Signature Generation**
  - Elliptic curve Diffie-Hellman Digital Signature Algorithm (ECDSA)
- **Curve Support**
  - Short Weierstrass form (full hardware support), such as:
    - NIST-P224, NIST-P256, NIST-P384, NIST-P521
    - Brainpool-256R1, Brainpool-384R1, Brainpool-512R1
    - secp256r1
  - Montgomery form (hardware support for multiplication), such as:
    - Curve25519
- **SHA2 based MACs**
  - HMAC with SHA224, SHA256, SHA384, or SHA512
- Block cipher mode of operation
  - AESCCM
  - AESGCM
  - AESECB
  - AESCBC
  - AESCBC-MAC
- **True random number generation**

Other capabilities, such as RSA encryption and signatures as well as Edwards type of elliptic curves such as Curve1174 or Ed25519, are a provided part of the TI SimpleLink SDK for the CC2651R3SIPA device.

9.6 Timers

A large selection of timers are available as part of the CC2651R3SIPA device. These timers are:

- **Real-Time Clock (RTC)**

  A 70-bit 3-channel timer running on the 32 kHz low frequency system clock (SCLK_LF)
  This timer is available in all power modes except Shutdown. The timer can be calibrated to compensate for frequency drift when using the LF RCOSC as the low frequency system clock. If an external LF clock with frequency different from 32.768 kHz is used, the RTC tick speed can be adjusted to compensate for this. When using TI-RTOS, the RTC is used as the base timer in the operating system and should thus only be accessed through the kernel APIs such as the Clock module. By default, the RTC halts when a debugger halts the device.
- **General Purpose Timers (GPTIMER)**

  The four flexible GPTIMERs can be used as either 4× 32 bit timers or 8× 16 bit timers, all running on up to 48 MHz. Each of the 16- or 32-bit timers support a wide range of features such as one-shot or periodic counting, pulse width modulation (PWM), time counting between edges and edge counting. The inputs and outputs of the timer are connected to the device event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. The GPTIMERs are available in Active and Idle power modes.
- **Radio Timer**

  A multichannel 32-bit timer running at 4 MHz is available as part of the device radio. The radio timer is typically used as the timing base in wireless network communication using the 32-bit timing word as the network time. The radio timer is synchronized with the RTC by using a dedicated radio API when the device radio is turned on or off. This ensures that for a network stack, the radio timer seems to always be running when the radio is enabled. The radio timer is in most cases used indirectly through the trigger time fields in the radio APIs and should only be used when running the accurate 48 MHz high frequency crystal is the source of SCLK_HF.
- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. It is typically used to generate an interrupt to and reset of the device for the case where periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 1.5 MHz clock rate and cannot be stopped once enabled. The watchdog timer pauses to run in Standby power mode and when a debugger halts the device.

9.7 Serial Peripherals and I/O

The SSI is a synchronous serial interfaces that are compatible with SPI, MICROWIRE, and TI's synchronous serial interfaces. The SSIs support both SPI controller and peripheral up to 4 MHz. The SSI modules support configurable phase and polarity.

The UARTs implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps.

The I^2S interface is used to handle digital audio and can also be used to interface pulse-density modulation microphones (PDM).

The I^2C interface is also used to communicate with devices compatible with the I^2C standard. The I^2C interface can handle 100 kHz and 400 kHz operation, and can serve as both controller and peripheral.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a flexible manner. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull or open-drain. Five GPIOs have high-drive capabilities, which are marked in **bold** in Section 7. All digital peripherals can be connected to any digital pin on the device.

For more information, see the CC13x1x2, CC26x1x2 SimpleLink™ Wireless MCU Technical Reference Manual.

9.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2651R3SIPA device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

9.9 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Highly flexible and configurable channel operation of up to 32 channels
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

9.10 Debug

The on-chip debug support is done through a dedicated cJTAG (IEEE 1149.7) or JTAG (IEEE 1149.1) interface. The device boots by default into cJTAG mode and must be reconfigured to use 4-pin JTAG.

9.11 Power Management

To minimize power consumption, the CC2651R3SIPA supports a number of power modes and power management features (see Table 9-1).

Table 9-1. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
Register and CPU retention	Full	Full	Partial	No	No
SRAM retention	Full	Full	Full	No	No
48 MHz high-speed clock (SCLK_HF)	XOSC_HF or RCOSC_HF	XOSC_HF or RCOSC_HF	Off	Off	Off
32 kHz low-speed clock (SCLK_LF)	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	XOSC_LF or RCOSC_LF	Off	Off
Peripherals	Available	Available	Off	Off	Off
Wake-up on RTC	Available	Available	Available	Off	Off
Wake-up on pin edge	Available	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	Duty Cycled	Off	Off
Power-on reset (POR)	On	On	On	Off	Off
Watchdog timer (WDT)	Available	Available	Paused	Off	Off

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 9-1).

In **Idle** mode, all active peripherals can be clocked, but the Application CPU core and memory are not clocked and no code is executed. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event or RTC event is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset by reading the reset status register. The only state retained in this mode is the latched I/O state and the flash memory contents.

Note

The power, RF and clock management for the CC2651R3SIPA device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2651R3SIPA software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

9.12 Clock Systems

The CC2651R3SIPA device has several internal system clocks.

The 48 MHz SCLK_HF is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (RCOSC_HF) or in-package 48 MHz crystal (XOSC_HF). Note that the radio operation runs off the included, in-package 48 MHz crystal within the module.

SCLK_LF is the 32.768 kHz internal low-frequency system clock. It can be used for the RTC and to synchronize the radio timer before or after Standby power mode. SCLK_LF can be driven by the internal 32.8 kHz RC Oscillator (RCOSC_LF), a 32.768 kHz watch-type crystal, or a clock input on any digitial IO.

When using a crystal or the internal RC oscillator, the device can output the 32 kHz SCLK_LF signal to other devices, thereby reducing the overall system cost.

9.13 Network Processor

Depending on the product configuration, the CC2651R3SIPA device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC) with the application and protocol stack running on the system CPU inside the device.

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

9.14 Device Certification and Qualification

The CC2651R3SIPA module from TI is certified for FCC, IC/ISED, and ETSI/CE as lised in Table 9-2. Moreover, the module is a Bluetooth Qualified Design by the Bluetooth Special Interest Group (Bluetooth SIG). TI Customers that build products based on the TI CC2651R3SIPA module can save in testing cost and time per product family.

Note

The FCC and IC IDs, as well as the UK and CE markings, must be located in both the user manual and on the packaging. Due to the small size of the module (7 mm x 7 mm), placing the IDs and markings in a type size large enough to be legible without the aid of magnification is impractical.

Table 9-2. CC2651R3SIPA List of Certifications

Regulatory Body	Specification	ID (IF APPLICABLE)
FCC (USA)	Part 15C + MPE FCC RF Exposure (Bluetooth)	ZAT-CC2651R3SIPA
	Part 15C + MPE FCC RF Exposure (802.15.4)	
IC/ISED (Canada)	RSS-102 (MPE) and RSS-247 (Bluetooth)	451H-2651R3SIPA
	RSS-102 (MPE) and RSS-247 (802.15.4)	
ETSI/CE (Europe)	EN 300328 v2.2.2 (2019-07) (Bluetooth)	—
	EN 300328 v2.2.2 (2019-07) (802.15.4)	—
	EN 62311:2019 (MPE)	—
	EN 301 489-1 v2.2.3 (2019-11)	—
	EN 301489-17 v3.2.4 (2020-09)	—
	EN 55024:2010 + A1:2015	—
	EN 55032:2015 + AC:2016-07	—
	EN 62368-1: 2020	—

9.14.1 FCC Certification and Statement

CAUTION

FCC RF Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure limits. This transmitter must not be co-located or operating with any other antenna or transmitter.

The CC2651R3SIPA module from TI is certified for the FCC as a single-modular transmitter. The module is an FCC-certified radio module that carries a modular grant.

You are cautioned that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device is planned to comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation of the device.

9.14.2 IC/ISED Certification and Statement

CAUTION

IC RF Radiation Exposure Statement:

To comply with IC RF exposure requirements, this device and its antenna must not be co-located or operating in conjunction with any other antenna or transmitter.

Pour se conformer aux exigences de conformité RF canadienne l'exposition, cet appareil et son antenne ne doivent pas étre co-localisés ou fonctionnant en conjonction avec une autre antenne ou transmetteur.

The CC2651R3SIPA module from TI is certified for IC as a single-modular transmitter. The CC2651R3SIPA module from TI meets IC modular approval and labeling requirements. The IC follows the same testing and rules as the FCC regarding certified modules in authorized equipment.

This device complies with Industry Canada licence-exempt RSS standards.

Operation is subject to the following two conditions:

- This device may not cause interference.
- This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence.

L'exploitation est autorisée aux deux conditions suivantes:

- L'appareil ne doit pas produire de brouillage
- L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

9.14.3 ETSI/CE Certification

The CC2651R3SIPA module from TI is CE certified with certifications to the appropriate EU radio and EMC directives summarized in the Declaration of Conformity and evidenced by the CE mark. The module is tested and certified against the Radio Equipment Directive (RED).

See the full text of the for the EU Declaration of Conformity for the CC2651R3SIPAT0MOU device.

9.14.4 UK Certification

The CC2651R3SIPA module from TI is UK certified with certifications to the appropriate UK radio and EMC directives summarized in the Declaration of Conformity and evidenced by the UK mark. The module is tested and certified against the Radio Equipment Regulations 2017.

See the full text of the for the UK Declaration of Conformity for the CC2651R3SIPAT0MOU device.

9.15 Module Markings

Figure 9-1 shows the top-side marking for the CC2651R3SIPA module.

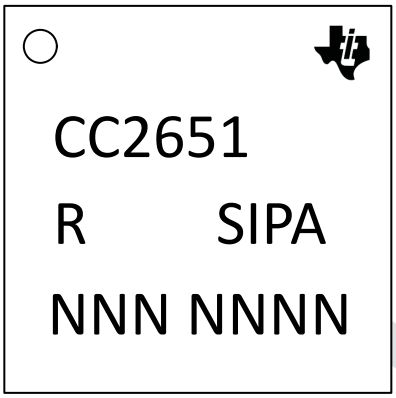


Figure 9-1. Top-Side Marking

Table 9-3 lists the CC2651R3SIPA module markings.

Table 9-3. Module Descriptions

MARKING	DESCRIPTION
CC2651	Generic Part Number
R	Model
SIPA	SIPA = Module type, X = pre-release
NNN NNNN	LTC (Lot Trace Code)

9.16 End Product Labeling

The CC2651R3SIPA module complies with the FCC single modular FCC grant, FCC ID: **ZAT-2651R3SIPA**. The host system using this module must display a visible label indicating the following text:

Contains FCC ID: **ZAT-2651R3SIPA**

The CC2651R3SIPA module complies with the IC single modular IC grant, IC: **451H-2651R3SIPA**. The host system using this module must display a visible label indicating the following text:

Contains IC: **451H-2651R3SIPA**

For more information on end product labeling and a sample label, please see section 4 of the OEM Integrators Guide

9.17 Manual Information to the End User

The OEM integrator must be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module.

The end user manual must include all required regulatory information and warnings as shown in this manual.

10 Application, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Typical Application Circuit

Figure 10-1 shows the typical application schematic using the the CC2651R3SIPA module. Note that C15 should be assembled when using the integrated antenna option within the module. C14 should be assembled if the module is to be used with an external antenna. In addition if using the external antenna option, Pin 16 of the module can be left unconnected. For the full reference schematic, download the LP-CC2651R3SIPA Design Files.

Note

The following guidelines are recommended for implementation of the RF design when using an external anenna on the RF path, pin 14:

- Ensure an RF path is designed with an impedance of 50 Ω.
- Tuning of the antenna impedance π matching network is recommended after manufacturing of the PCB to account for PCB parasitics.
- π or L matching and tuning may be required between RF out path, pin 14, and the external antenna.

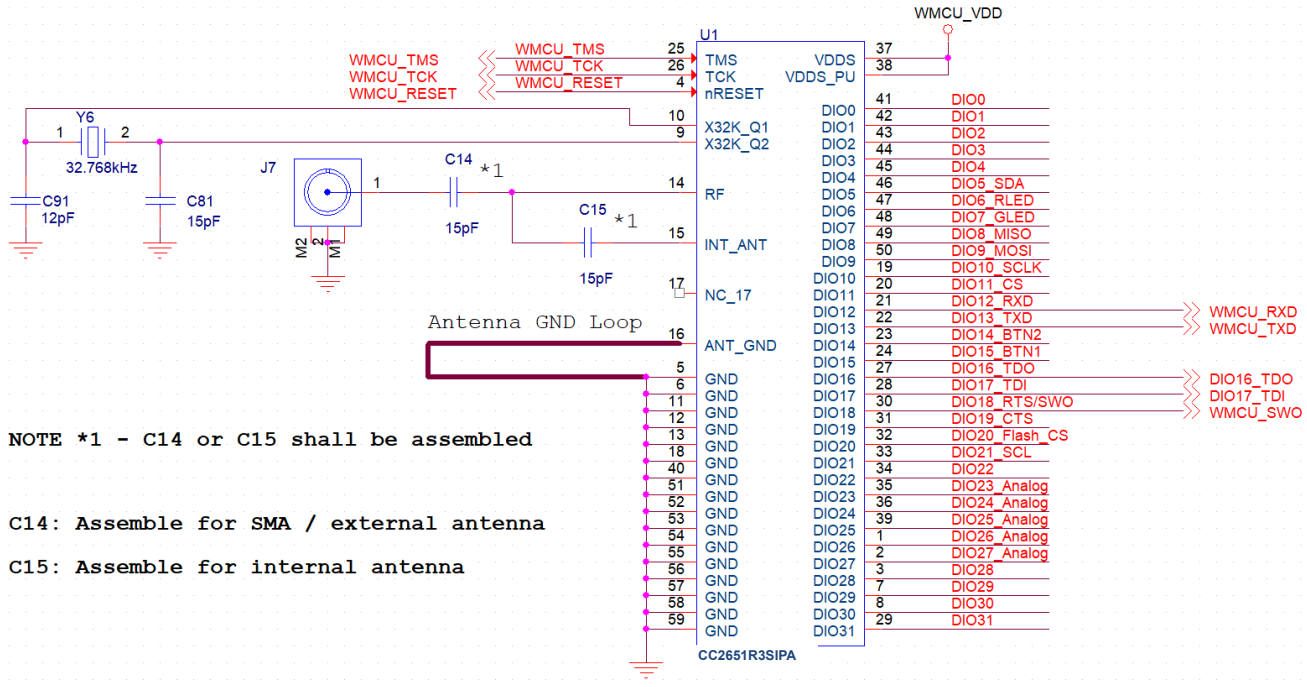


Figure 10-1. CC2651R3SIPA Typical Application Schematic

Table 10-1 provides the bill of materials for a typical application using the CC2651R3SIPA module in Figure 10-1.

For full operation reference design, see the LP-CC2651R3SIPA Design Files.

Table 10-1. Bill of Materials

PART REFERENCE	VALUE	MANUFACTURER	PART NUMBER	DESCRIPTION
C14, C15, C81, C91(1)	15 pF	Murata	GRM0335C1E150JA01D	Capacitor, ceramic, 15 pF, 50 V, ±5%, C0G/NP0, 0201
J7	U.FL	Hirose	U.FL-R-SMT-1(01)	U.FL (UMCC) connector receptacle, male pin 50 Ω, surface mount solder
U49	CC2651R3SIPA	Texas Instruments	CC2651R3SIPAT0MOUR	SimpleLink™ multiprotocol 2.4-GHz wireless MCU with integrated power amplifier and Antenna
Y6	32.768kHz	TAI-SAW	TZ1166C	Crystal, resonator, 32.768kHz, -40ºC / +125ºC, SMD

(1) C15 is placed when using the integrated antenna. C14 is placed when using an external antenna

10.2 Device Connections

10.2.1 Reset

In order to meet the module power-on-reset requirements, VDDS (Pin 37) and VDDS_PU (Pin 38) should be connected together. If the reset signal is not based upon a power-on-reset and is derived from an external MCU, then VDDS_PU (Pin 38) should be No Connect (NC). Please refer to Figure 10-1 for the recommended circuit implementation.

10.2.2 Unused Pins

All unused pins can be left unconnected without the concern of having leakage current.

10.3 PCB Layout Guidelines

This section details the PCB guidelines to speed up the PCB design using the CC2651R3SIPA module. The integrator of the CC2651R3SIPA modules must comply with the PCB layout recommendations described in the following subsections to minimize the risk with regulatory certifications for the FCC, IC/ISED, ETSI/CE. Moreover, TI recommends customers to follow the guidelines described in this section to achieve similar performance to that obtained with the TI reference design.

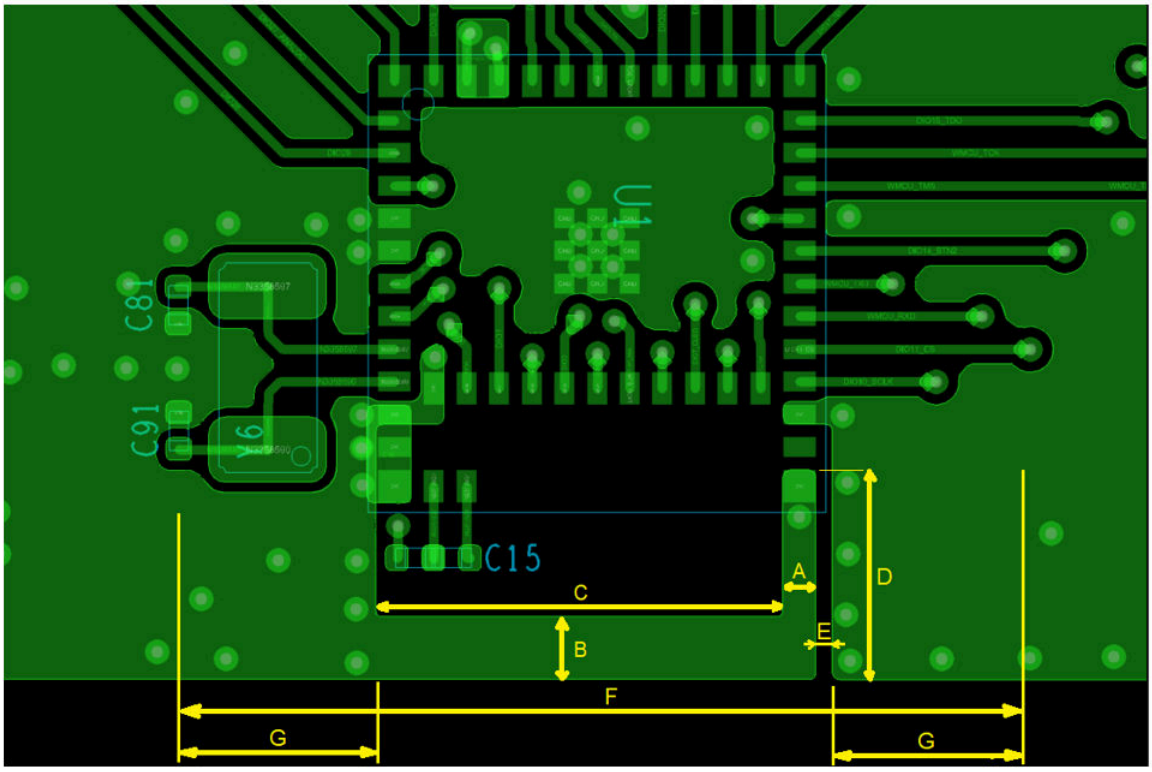
10.3.1 General Layout Recommendations

Ensure that the following general layout recommendations are followed:

- Have a solid ground plane and ground vias under the module for stable system and thermal dissipation.
- Do not run signal traces underneath the module on a layer where the module is mounted.

10.3.2 RF Layout Recommendations with Integrated Antenna

It is critical that the RF section be laid out correctly to ensure optimal module performance. A poor layout can cause low-output power and sensitivity degradation. Figure 10-2 shows the RF placement and routing of the CC2651R3SIPA module with the 2.4-GHz integrated antenna.



A: 0.5 mm
B: 1.00mm
C: 6.23 mm
D: 3.2mm
E: 0.25 mm
F: 26.98 mm
G: 10.0 mm

Figure 10-2. Module Layout Guidelines

Follow these RF layout recommendations for the CC2651R3SIPA module when using the integrated Antenna:

- Dimensions A thru G in Figure 10-2 must be strickly adhered to for optimal RF performance
- The module must have a minimum 10-mm ground plane on either side of the module on all layers as shown with dimension G in Figure 10-2
- There must be at least on ground-reference plane under the module on the main PCB

For the CC2651R3SIPA it is recommended to use 4-layer PCB board with the dimensions A thru G copied on all 4 layers. This will provided for the best antenna bandwidth in the 2.4GHz band. In addition, it s recommended that the L1 to L2 layer be 0.175 mm, with a dielectric constant of 4.0, and have an overall 4-layer board thickness of 1.6 mm as per our reference design, for optimal antenna RF performance. Deviation from this will cause a potential detuning of the integrated antenna.

10.4 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2651R3SIPA device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

CC2651RSIPA-EM Design Files	The CC2651RSIP-EM reference design provides schematic, layout and production files for the characterization board used for deriving the performance number found in this document.
LP-CC2651R3SIPA Design Files	The CC2651R3SIPA LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2651R3SIPA device.
Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag	The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including: • PCB antennas • Helical antennas • Chip antennas • Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

10.5 Junction Temperature Calculation

This section shows the different techniques for calculating the junction temperature under various operating conditions. For more details, see Semiconductor and IC Package Thermal Metrics.

There are three recommended ways to derive the junction temperature from other measured temperatures:

1. From package temperature:

$$T_J = \psi_{\mathrm{JT}} \times P + T_{\mathrm{case}} \quad (1)$$

2. From board temperature:

$$T_J = \psi_{\mathrm{JB}} \times P + T_{\mathrm{board}} \quad (2)$$

3. From ambient temperature:

$$T_J = R_{\theta\mathrm{JA}} \times P + T_A \quad (3)$$

P is the power dissipated from the device and can be calculated by multiplying current consumption with supply voltage. Thermal resistance coefficients are found in Section 8.8.

Example:

Using Equation 3, the temperature difference between ambient temperature and junction temperature is calculated. In this example, we assume a simple use case where the radio is transmitting continuously at 0 dBm output power. Let us assume the ambient temperature is 85 °C and the supply voltage is 3 V. To calculate P, we need to look up the current consumption for Tx at 85 °C in. From the plot, we see that the current consumption is 7.8 mA. This means that P is 7.95 mA × 3 V = 23.85 mW.

The junction temperature is then calculated as:

$$T_J = 48.7^{\circ C}/_{W} \times 23.85 mW + T_A = 1.2^{\circ}C + T_A$$

As can be seen from the example, the junction temperature is 1.2°C higher than the ambient temperature when running continuous Tx at 85 °C and, thus, well within the recommended operating conditions.

For various application use cases current consumption for other modules may have to be added to calculate the appropriate power dissipation. For example, the MCU may be running simultaneously as the radio, peripheral modules may be enabled, etc. Typically, the easiest way to find the peak current consumption, and thus the peak power dissipation in the device, is to measure as described in Measuring CC13xx and CC26xx current consumption.

11 Environmental Requirements and SMT Specifications

11.1 PCB Bending

The PCB follows IPC-A-600J for PCB twist and warpage < 0.75% or 7.5 mil per inch.

11.2 Handling Environment

11.2.1 Terminals

The product is mounted with motherboard through land-grid array (LGA). To prevent poor soldering, do not make skin contact with the LGA portion.

11.2.2 Falling

The mounted components will be damaged if the product falls or is dropped. Such damage may cause the product to malfunction.

11.3 Storage Condition

11.3.1 Moisture Barrier Bag Before Opened

A moisture barrier bag must be stored in a temperature of less than 30°C with humidity under 85% RH. The calculated shelf life for the dry-packed product will be 24 months from the date the bag is sealed.

11.3.2 Moisture Barrier Bag Open

Humidity indicator cards must be blue, < 30%.

11.4 PCB Assembly Guide

The wireless MCU modules are packaged in a substrate base Leadless Quad Flatpack (QFM) package. The modules are designed with pull back leads for easy PCB layout and board mounting.

11.4.1 PCB Land Pattern & Thermal Vias

We recommended a solder mask defined land pattern to provide a consistent soldering pad dimension in order to obtain better solder balancing and solder joint reliability. PCB land pattern are 1:1 to module soldering pad dimension. Thermal vias on PCB connected to other metal plane are for thermal dissipation purpose. It is critical to have sufficient thermal vias to avoid device thermal shutdown. Recommended vias size are 0.2mm and position not directly under solder paste to avoid solder dripping into the vias.

11.4.2 SMT Assembly Recommendations

The module surface mount assembly operations include:

- Screen printing the solder paste on the PCB
- Monitor the solder paste volume (uniformity)
- Package placement using standard SMT placement equipment
- X-ray pre-reflow check - paste bridging
- Reflow
- X-ray post-reflow check - solder bridging and voids

11.4.3 PCB Surface Finish Requirements

A uniform PCB plating thickness is key for high assembly yield. For an electroless nickel immersion gold finish, the gold thickness should range from 0.05 µm to 0.20 µm to avoid solder joint embrittlement. Using a PCB with Organic Solderability Preservative (OSP) coating finish is also recommended as an alternative to Ni-Au.

11.4.4 Solder Stencil

Solder paste deposition using a stencil-printing process involves the transfer of the solder paste through pre-defined apertures with the application of pressure. Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of package is highly recommended to improve board assembly yields.

11.4.5 Package Placement

Packages can be placed using standard pick and place equipment with an accuracy of ±0.05 mm. Component pick and place systems are composed of a vision system that recognizes and positions the component and a mechanical system that physically performs the pick and place operation. Two commonly used types of vision systems are:

- A vision system that locates a package silhouette
- A vision system that locates individual pads on the interconnect pattern

The second type renders more accurate placements but tends to be more expensive and time consuming. Both methods are acceptable since the parts align due to a self-centering features of the solder joint during solder reflow. It is recommended to avoid solder bridging to 2 mils into the solder paste or with minimum force to avoid causing any possible damage to the thinner packages.

11.4.6 Solder Joint Inspection

After surface mount assembly, transmission X-ray should be used for sample monitoring of the solder attachment process. This identifies defects such as solder bridging, shorts, opens, and voids. It is also recommended to use side view inspection in addition to X-rays to determine if there are "Hour Glass" shaped solder and package tilting existing. The "Hour Glass" solder shape is not a reliable joint. 90° mirror projection can be used for side view inspection.

11.4.7 Rework and Replacement

TI recommends removal of modules by rework station applying a profile similar to the mounting process. Using a heat gun can sometimes cause damage to the module by overheating.

11.4.8 Solder Joint Voiding

TI recommends to control solder joint voiding to be less than 30% (per IPC-7093). Solder joint voids could be reduced by baking of components and PCB, minimized solder paste exposure duration, and reflow profile optimization.

11.5 Baking Conditions

Products require baking before mounting if:

- Humidity indicator cards read > 30%
- Temp < 30°C, humidity < 70% RH, over 96 hours

Baking condition: 90°C, 12 to 24 hours

Baking times: 1 time

11.6 Soldering and Reflow Condition

- Heating method: Conventional convection or IR convection
- Temperature measurement: Thermocouple d = 0.1 mm to 0.2 mm CA (K) or CC (T) at soldering portion or equivalent method
- Solder paste composition: SAC305
- Allowable reflow soldering times: 2 times based on the reflow soldering profile (see Figure 11-1)
- Temperature profile: Reflow soldering will be done according to the temperature profile (see Figure 11-1)
- Peak temperature: 260°C

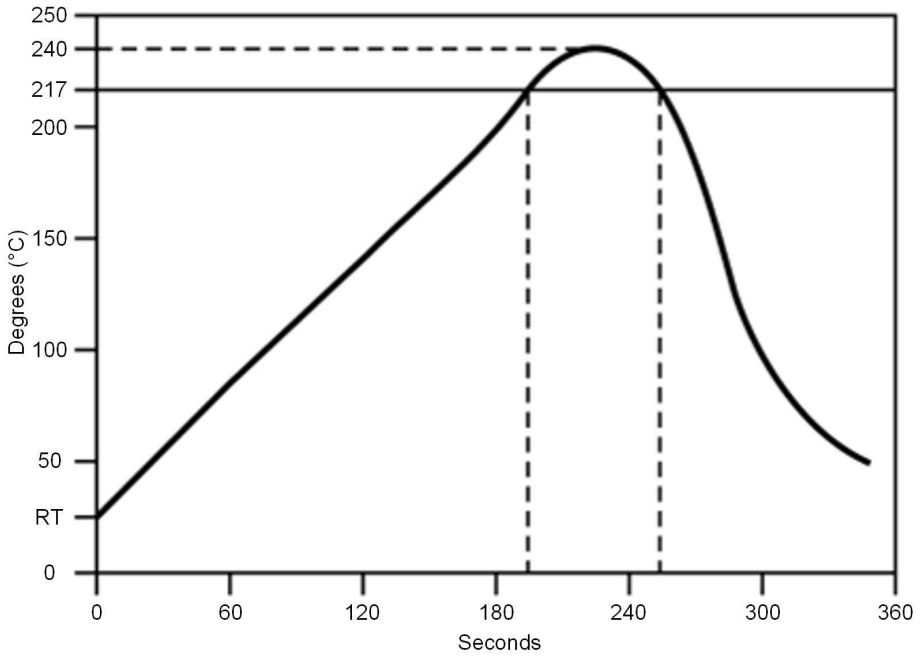


Figure 11-1. Temperature Profile for Evaluation of Solder Heat Resistance of a Component (at Solder Joint)

Table 11-1. Temperature Profile

Profile Elements	Convection or IR[1]
Peak temperature range	235 to 240°C typical (260°C maximum)
Pre-heat / soaking (150 to 200°C)	60 to 120 seconds
Time above melting point	60 to 90 seconds
Time with 5°C to peak	30 seconds maximum
Ramp up	< 3°C / second
Ramp down	< -6°C / second

(1) For details, refer to the solder paste manufacturer's recommendation.

Note

TI does not recommend the use of conformal coating or similar material on the SimpleLink™ module. This coating can lead to localized stress on the solder connections inside the module and impact the module reliability. Use caution during the module assembly process to the final PCB to avoid the presence of foreign material inside the module.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

12.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to all part numbers and/or date-code. Each device has one of three prefixes/identifications: X, P, or null (no prefix) (for example, XCC2651R3SIPA is in preview; therefore, an X prefix/identification is assigned).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *RGZ*).

For orderable part numbers of *CC2651R3SIPA* devices in the RGZ (7-mm x 7-mm) package type, see the *Package Option Addendum* of this document, the Device Information in Section 3, the TI website (www.ti.com), or contact your TI sales representative.

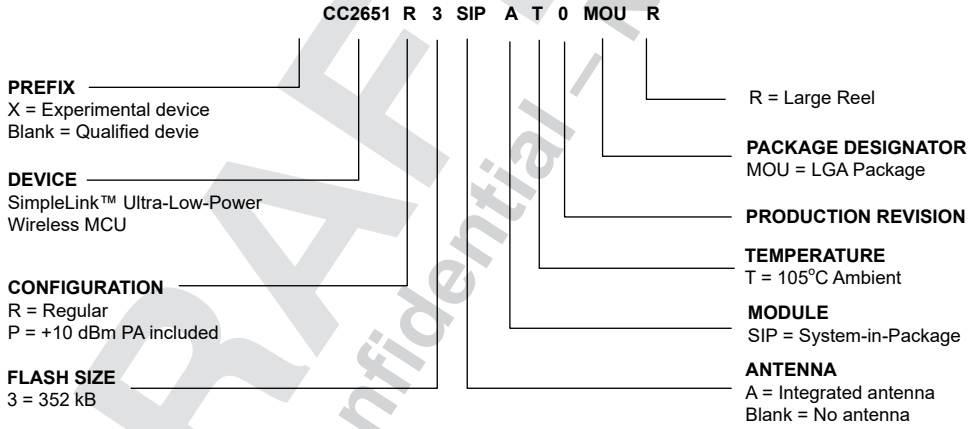


Figure 12-1. Device Nomenclature

12.2 Tools and Software

The CC2651R3SIPA device is supported by a variety of software and hardware development tools.

Development Kit

CC2651R3SIPA LaunchPad™ Development Kit

The CC2651R3SIPA LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2651R3SIPA SimpleLink Wireless system-in-Package, which allows you to quickly evaluate and prototype 2.4-GHz wireless applications such as Bluetooth 5

Low Energy and Zigbee, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more.

Software

SimpleLink™ CC13XX-CC26XX SDK

The SimpleLink CC13xx and CC26xx Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC13XX / CC26XX family of devices. The SDK includes a comprehensive software package for the CC2651R3SIPA module, including the following protocol stacks:

- Bluetooth Low Energy 4 and 5.2
- Thread (based on OpenThread)
- Zigbee 3.0
- TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for Sub-1 GHz and 2.4 GHz

The SimpleLink CC13XX-CC26XX SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit http://www.ti.com/simplelink.

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK.

Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.

Code Composer Studio™ Cloud IDE

Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.

IAR Embedded Workbench® for Arm®

IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK.

A 30-day evaluation or a 32 KB size-limited version is available through iar.com.

SmartRF™ Studio

SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include:

- Link tests - send and receive packets between nodes
- Antenna and radiation tests - set the radio in continuous wave TX and RX states
- Export radio configuration code for use with the TI SimpleLink SDK RF driver
- Custom GPIO configuration for signaling and control of external switches

CCS UniFlash	CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

12.2.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

12.3 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder on ti.com/product/CC2651R3SIPA In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer	Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC2651R3SIPA Silicon Errata	The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC2651R3SIPA device are found on the device product folder at: ti.com/product/CC2651R3SIPA/technicaldocuments.

Technical Reference Manual (TRM)

CC13x1x3, CC26x1x3 SimpleLink™ Wireless MCU TRM	The TRM provides a detailed description of all modules and peripherals available in the device family.

12.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Note

The total height of the module is 1.51 mm.

The weight of the CC2651R3SIPA module is typically 0.182 g.

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