Description of Operation

The AM3352 is the central processor of the TG400 whole system, it has direct interface to on the board memory and all peripherals. The system has one 1Gbit NAND Flash, one 64Mx16bit DDR2 on the board.

The system also has some I/O port for the external multi-media applications. On network side, the system provide one 802.3 Ethernet RJ45 connection to LAN, Four SIMCARD and Four Antenna for GSM modules.

1 Interface

1.1 Interface between the AM3352 and NAND flash

The NAND flash in the system is mainly used for program and data storage, based on the application, the system need to support up to 128MB NAND flash, the system supports 8-bit and 16-bit NAND devices, supports NAND flash that requires chip select to stay low during tR read time.

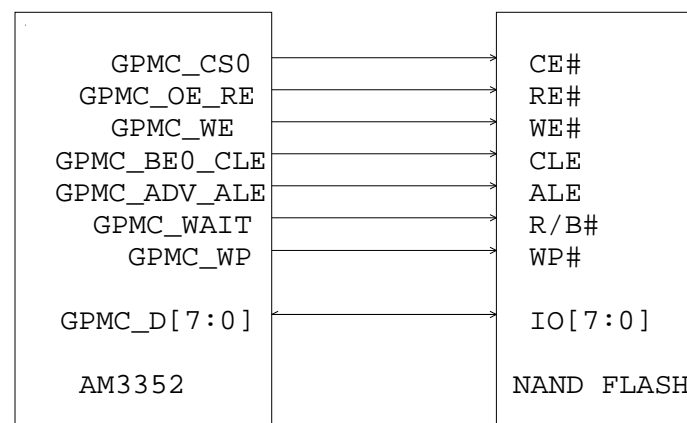Figure1.1 below shows the interface between processor and NAND flash:

```
GPMC_CS0        ────────────►  CE#
GPMC_OE_RE      ────────────►  RE#
GPMC_WE         ────────────►  WE#
GPMC_BE0_CLE    ────────────►  CLE
GPMC_ADV_ALE    ────────────►  ALE
GPMC_WAIT       ────────────►  R/B#
GPMC_WP         ────────────►  WP#

GPMC_D[7:0]     ────────────►  IO[7:0]

AM3352                         NAND FLASH
```

Figure1.1 Signal connection between AM3352 and NAND flash

1.2 Interface between the AM3352 and DDR2

The AM3352's SDRAM controller is a dedicated interface to DDR2 SDRAM, it can be programmed to interface to up to 1Gbytes of SDRAM. A set of programmable timing parameters is available to configure the SDRAM bank to support memory devices. The memory bank is 16 bits wide for minimum device count and lower

system cost.

Figure1.2 below shows the interface between processor and DDR2 SDRAM:

```
        DDR0_CKE   ───────────►   CKE
        DDR0_WE    ───────────►   WE
        DDR0_RAS   ───────────►   RAS
        DDR0_CAS   ───────────►   CAS
        DDR0_CS0   ───────────►   CS0

        DDR0_ODT   ───────────►   ODT

    DDR0_BA[2:0]   ───────────►   BA[2:0]
      DDR0_CLK0    ───────────►   CK
     DDR0_CLK0#    ───────────►   CK#
    DDR0_A[13:0]   ───────────►   A[13:0]
    DDR0_D[15:0]   ◄──────────►   DQ[15:0]
  DDR0_DQS[1:0]    ◄──────────►   DQS[1:0]

  DDR0_DQM[1:0]    ───────────►   DM[1:0]


        AM3352                    DDR2 SDRAM
```
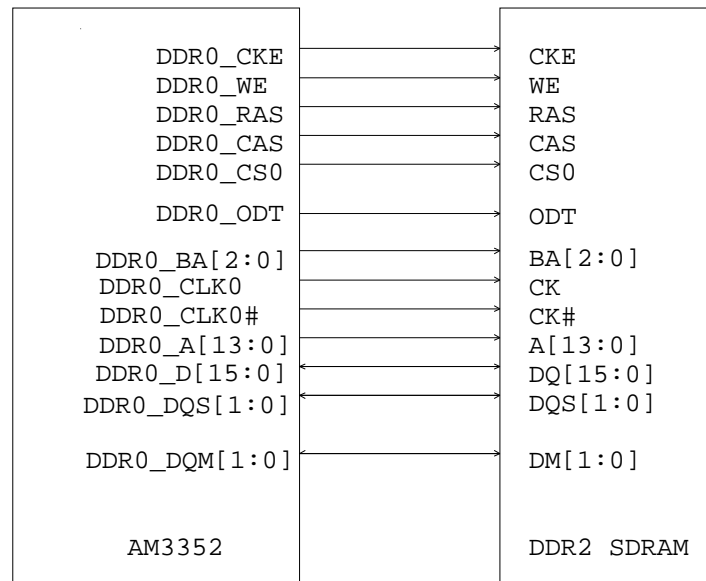
Figure1.2 Signal connection between AM3352 and DDR2 SDRAM

Main chip AM3352's MAX operating frequency is: 600MHz.