

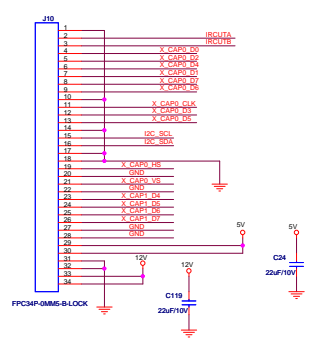
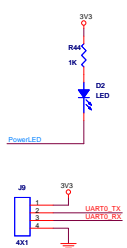
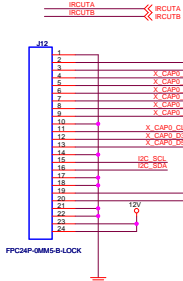
I2C_SCL I2C_SDA I2C_SCL I2C_SDA

X_CAP0_CLK X_CAP0_D0_7 X_CAP0_D0_7

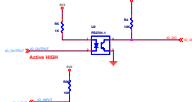
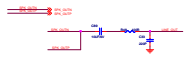
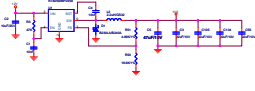
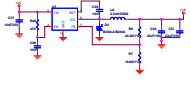
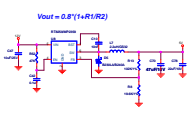
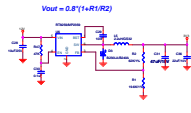
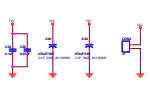
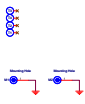
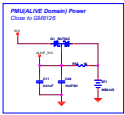
X_CAP1_D0_7 X_CAP1_D0_7 X_CAP0_HS X_CAP0_VS

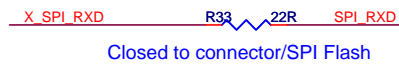
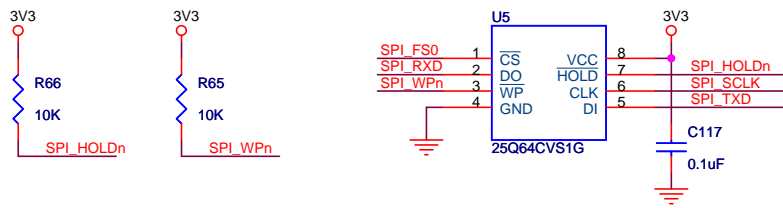
PowerLED Debut_Set

UART0_TX UART0_RX



	Bayer 12	Bayer 10	Bayer 8 +BT656	BT656 x2	BT601 +BT656	BT1120	BT601 16
CAPO_D7	D11	D9	D7	D0_7	D601_7	Y7	Y7
CAPO_D6	D10	D8	D6	D0_6	D601_6	Y6	Y6
CAPO_D5	D9	D7	D5	D0_5	D601_5	Y5	Y5
CAPO_D4	D8	D6	D4	D0_4	D601_4	Y4	Y4
CAPO_D3	D7	D5	D3	D0_3	D601_3	Y3	Y3
CAPO_D2	D6	D4	D2	D0_2	D601_2	Y2	Y2
CAPO_D1	D5	D3	D1	D0_1	D601_1	Y1	Y1
CAPO_D0	D4	D2	D0	D0_0	D601_0	Y0	Y0
CAPO_CLK	CLK	CLK	CLK	CLK0	601_CLK	CLK	CLK
CAPO_VS	VS	VS	VS		601_VS		VS
CAPO_HS	HS	HS	HS		601_HS		HS
CAP1_D7	D3	D1	D656_7	D1_7	D656_7	C7	C7
CAP1_D6	D2	D0	D656_6	D1_6	D656_6	C6	C6
CAP1_D5	D1		D656_5	D1_5	D656_5	C5	C5
CAP1_D4	D0		D656_4	D1_4	D656_4	C4	C4
CAP1_D3			D656_3	D1_3	D656_3	C3	C3
CAP1_D2			D656_2	D1_2	D656_2	C2	C2
CAP1_D1			D656_1	D1_1	D656_1	C1	C1
CAP1_D0			D656_0	D1_0	D656_0	C0	C0
CAP1_CLK			656_CLK	CLK1	656_CLK		





5

4

3

2

1

D

D

C

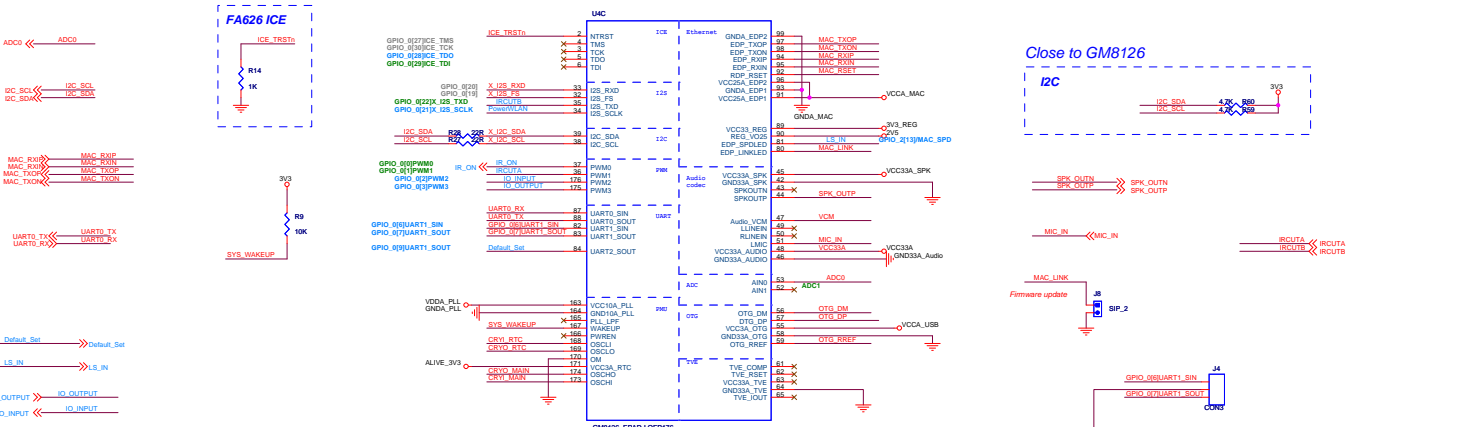
C

B

B

A

A



Pin1 setting:

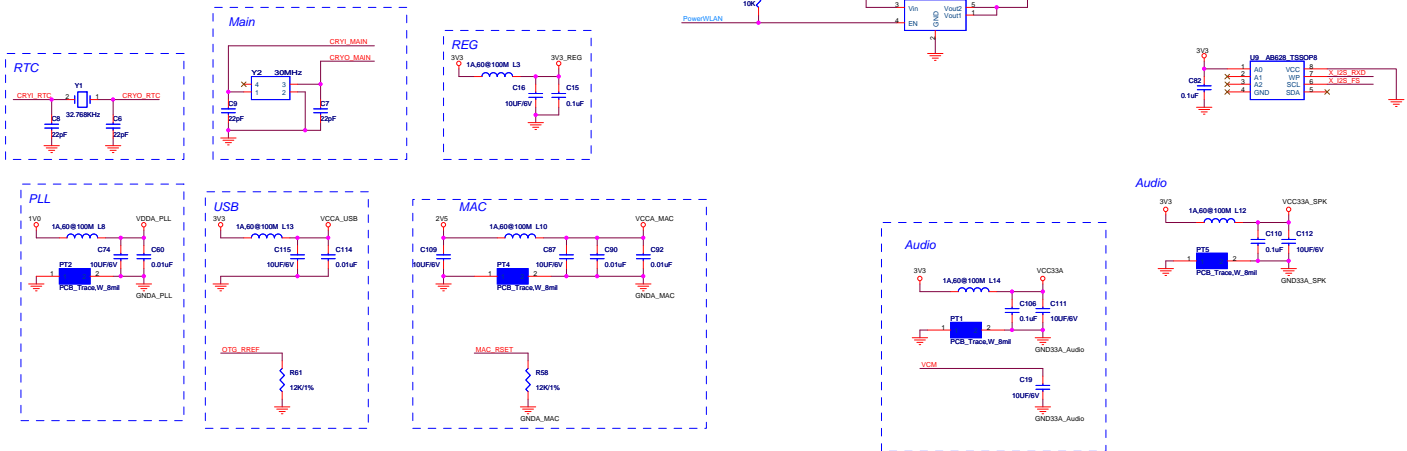
222	3-333	FD0000
1	0000	FD0000 (DEFAULT)

PIB32k dis

220	1M_210	X_SPL_F30
220	110_210	X_SPL_F31
220	110_210	X_SPL_F32

Firmware update:

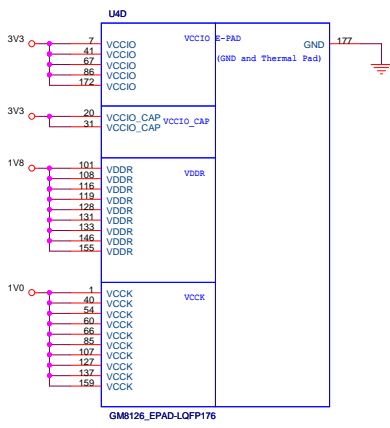
331	ESP_T00000	FD0000
1	0000	FD0000 (DEFAULT)



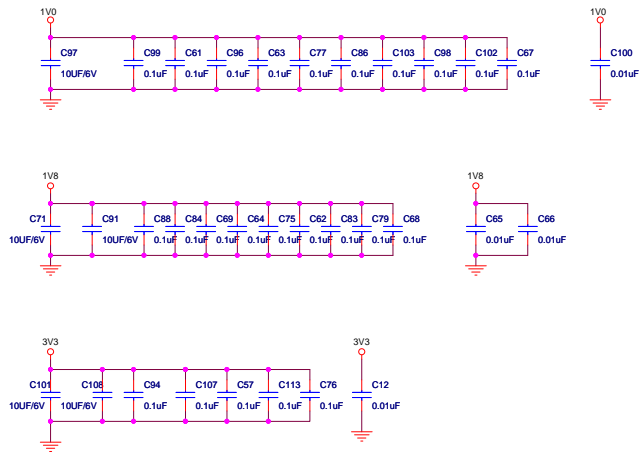
PIB1 setting:

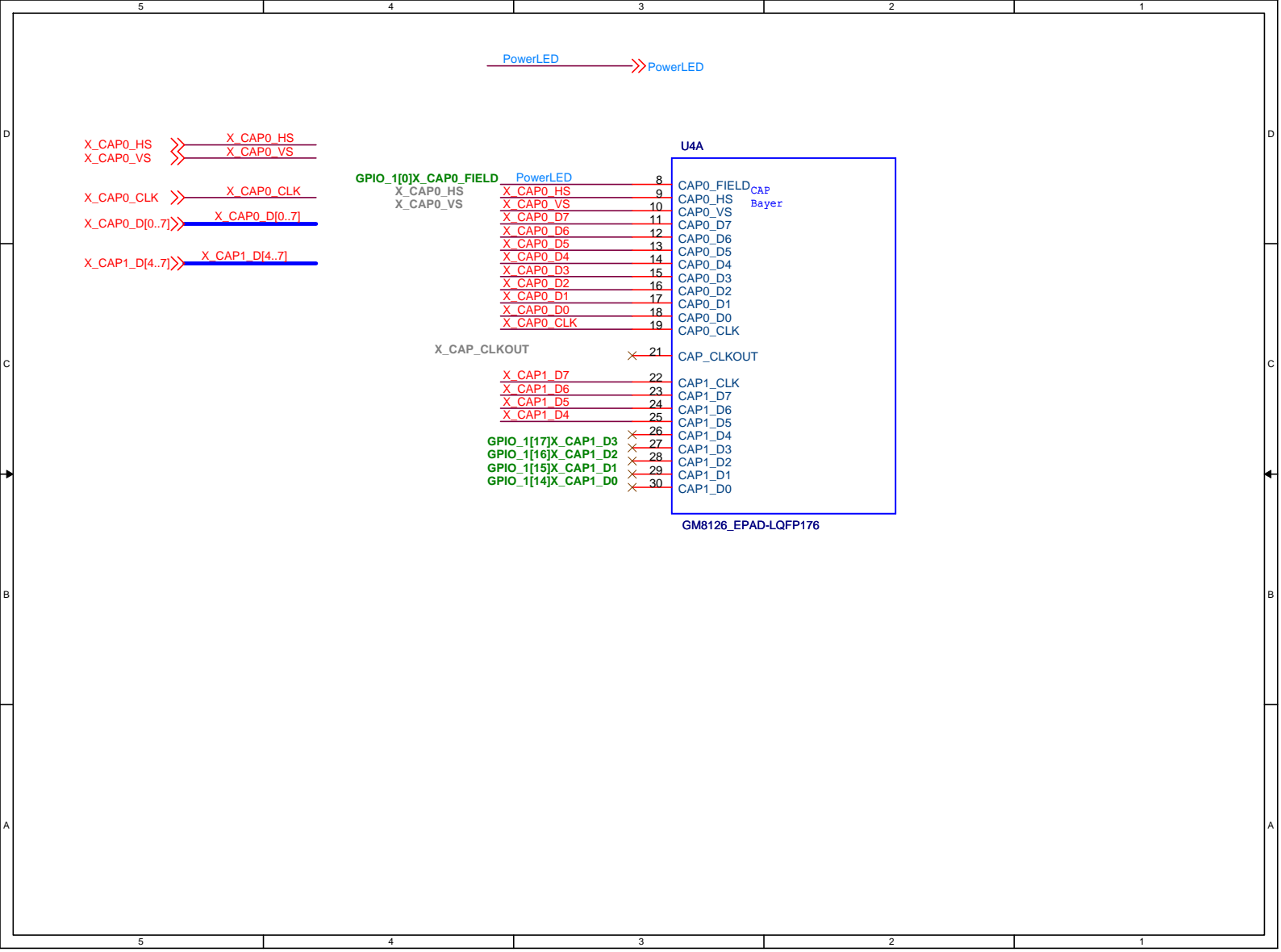
220	1M_210	X_SPL_F30
220	110_210	X_SPL_F31
220	110_210	X_SPL_F32



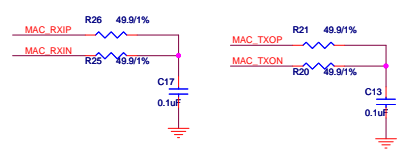
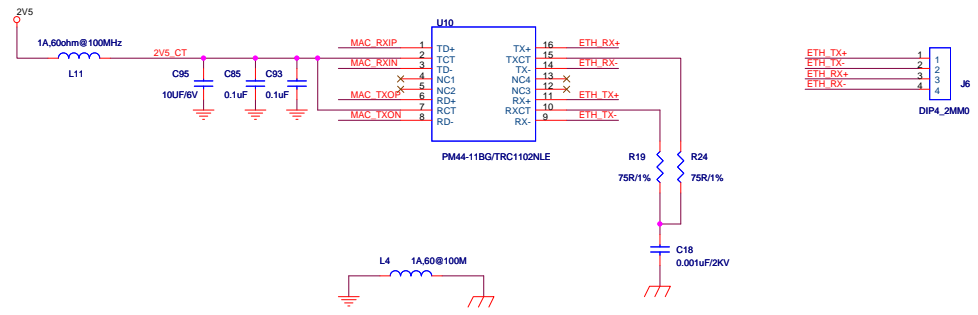
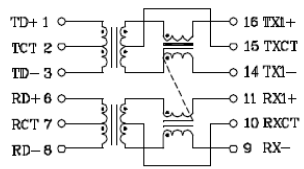


Close to GM8126





MAC_RXIP <-> MAC_RXIP
 MAC_RXIN <-> MAC_RXIN
 MAC_TXOP <-> MAC_TXOP
 MAC_TXON <-> MAC_TXON



5

4

3

2

1

D

D

C

C

B

B

A

A

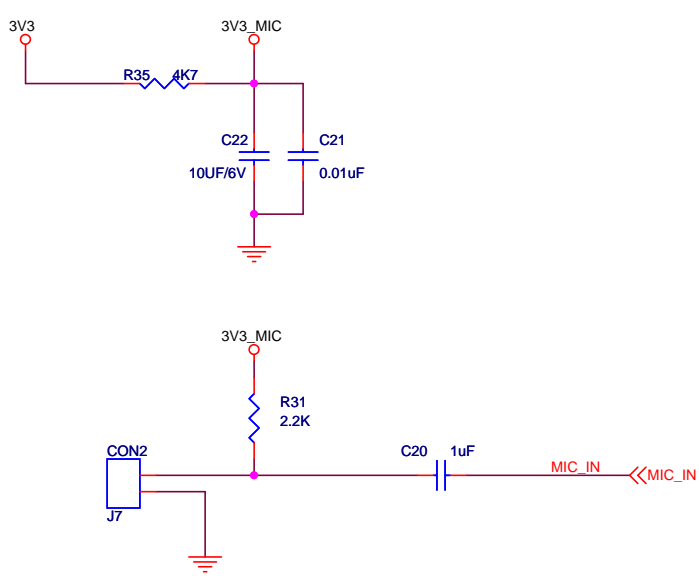
5

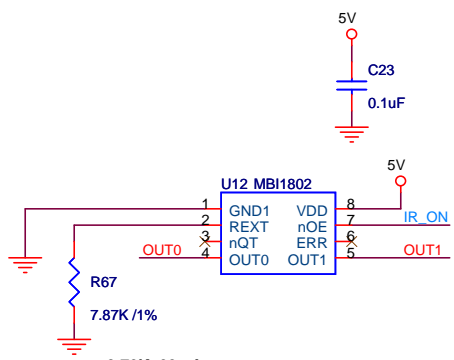
4

3

2

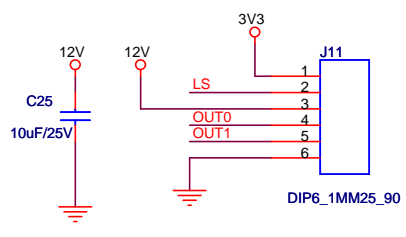
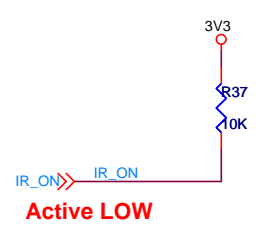
1





- 9.76K 60mA
- 9.53K 61mA
- 9.31K 63mA
- 9.1K 64mA
- 8.8K 66mA
- 7.87K 74.2mA

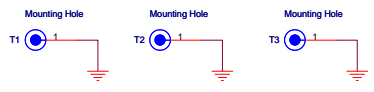
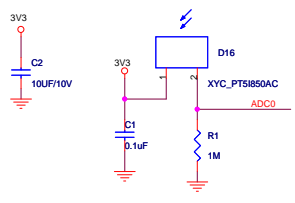
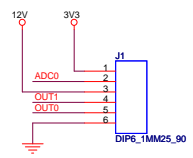
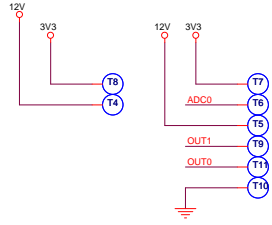
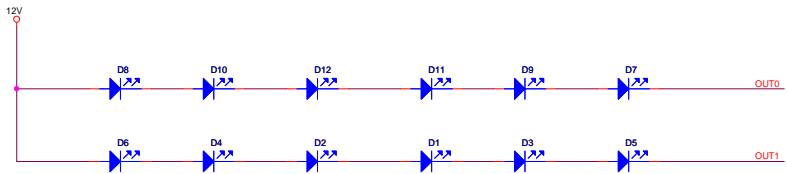
$I_{OUT} = (1.24V / R_{ext}) \times 471$ Within 6%



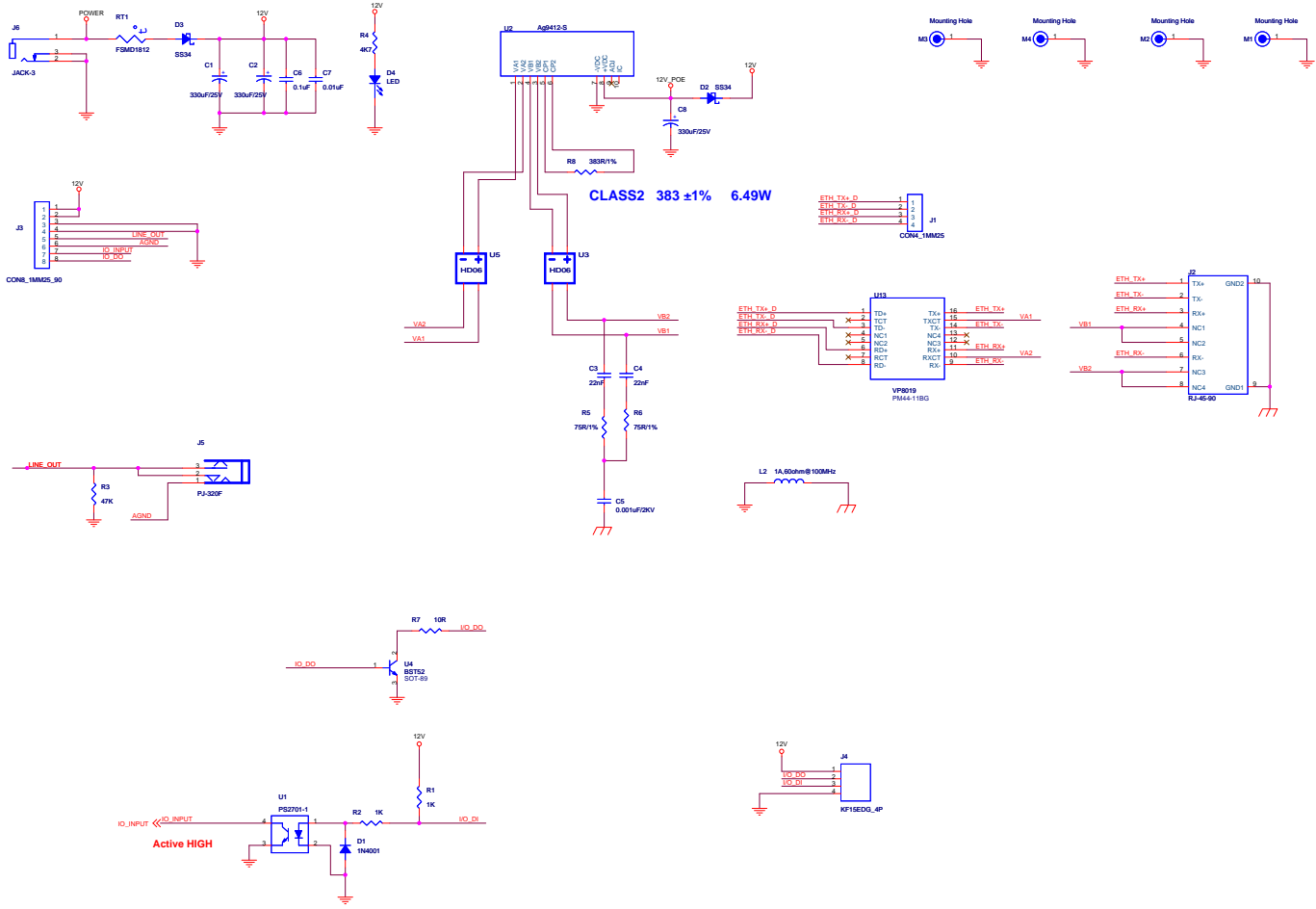
Data code/ Version	Modification

Change log:

Title		
Note		
Size	Document Number ABNC316IR1VA	Rev
Date:	Friday, March 02, 2012	Sheet 1 of 2



File	IRLED		
Size	Document Number	ABNC316R1VA	Rev
Date:	Friday, March 02, 2012	Sheet	2 of 2



CLASS2 383 ±1% 6.49W

J1
CONN_1MM25

U13
VP8019
PM44-118G

J2
RJ45-90

J4
KF15EDD_4P

Active HIGH

Data code/ Version	Modification
1.0	-First release

Change log:

D

D

C

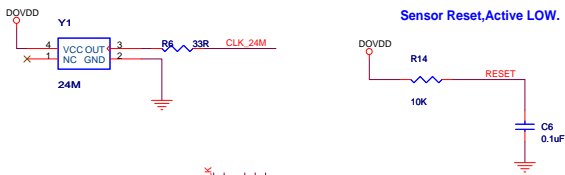
C

B

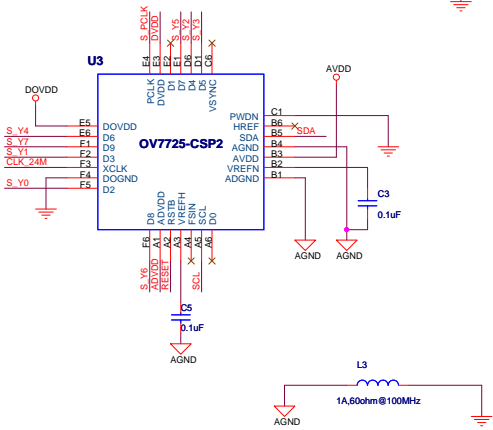
B

A

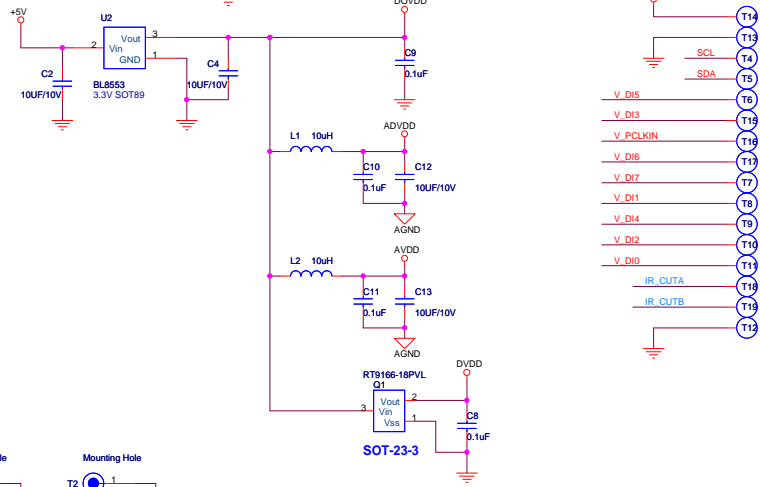
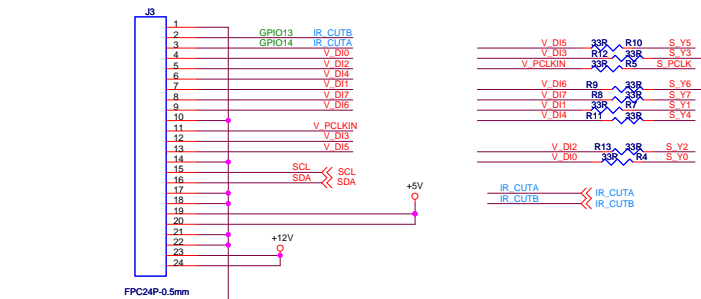
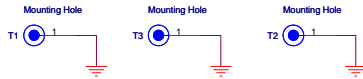
A



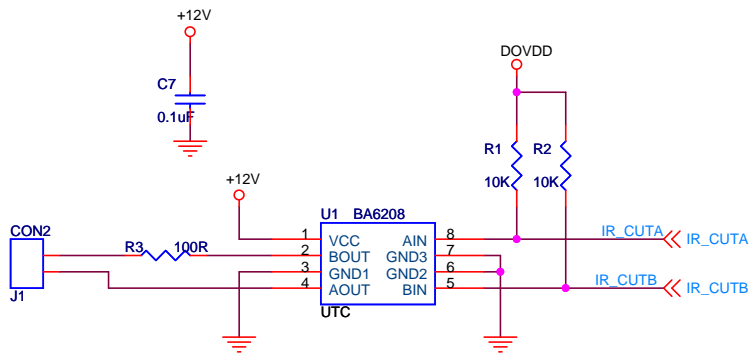
Sensor Reset,Active LOW.

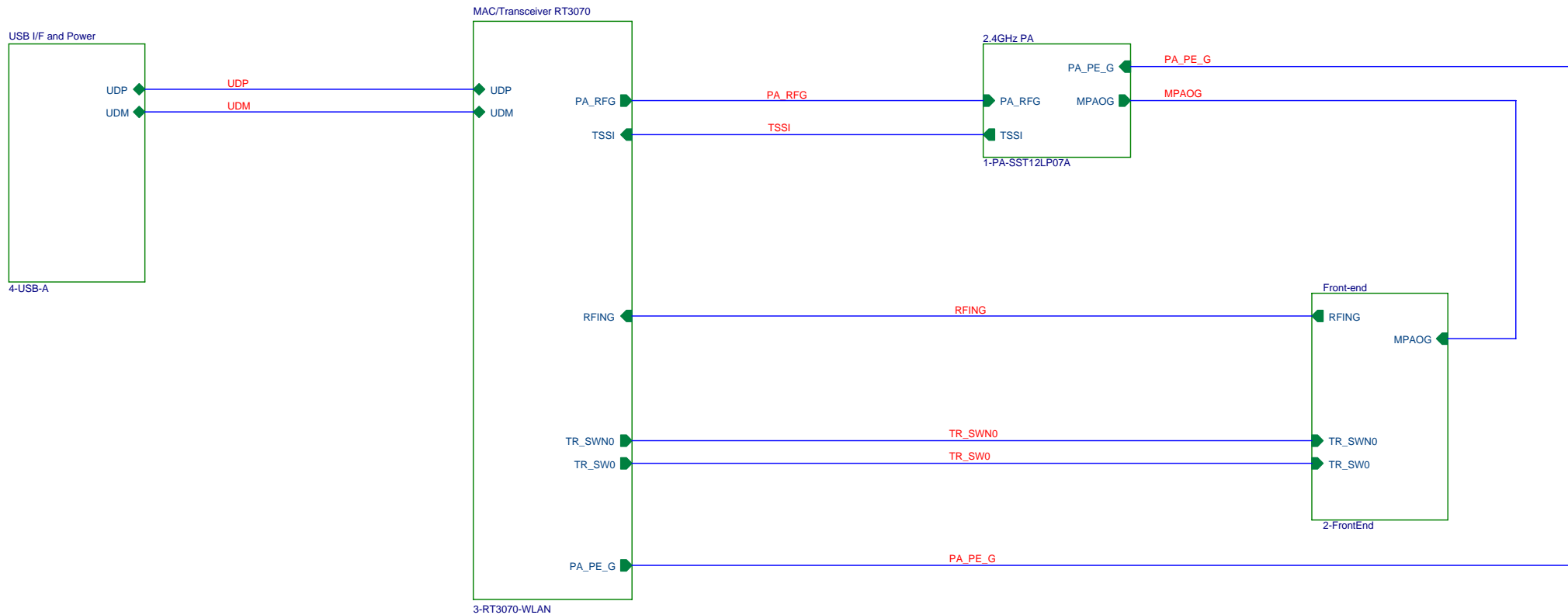


As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A6 oriented down on the PCB.




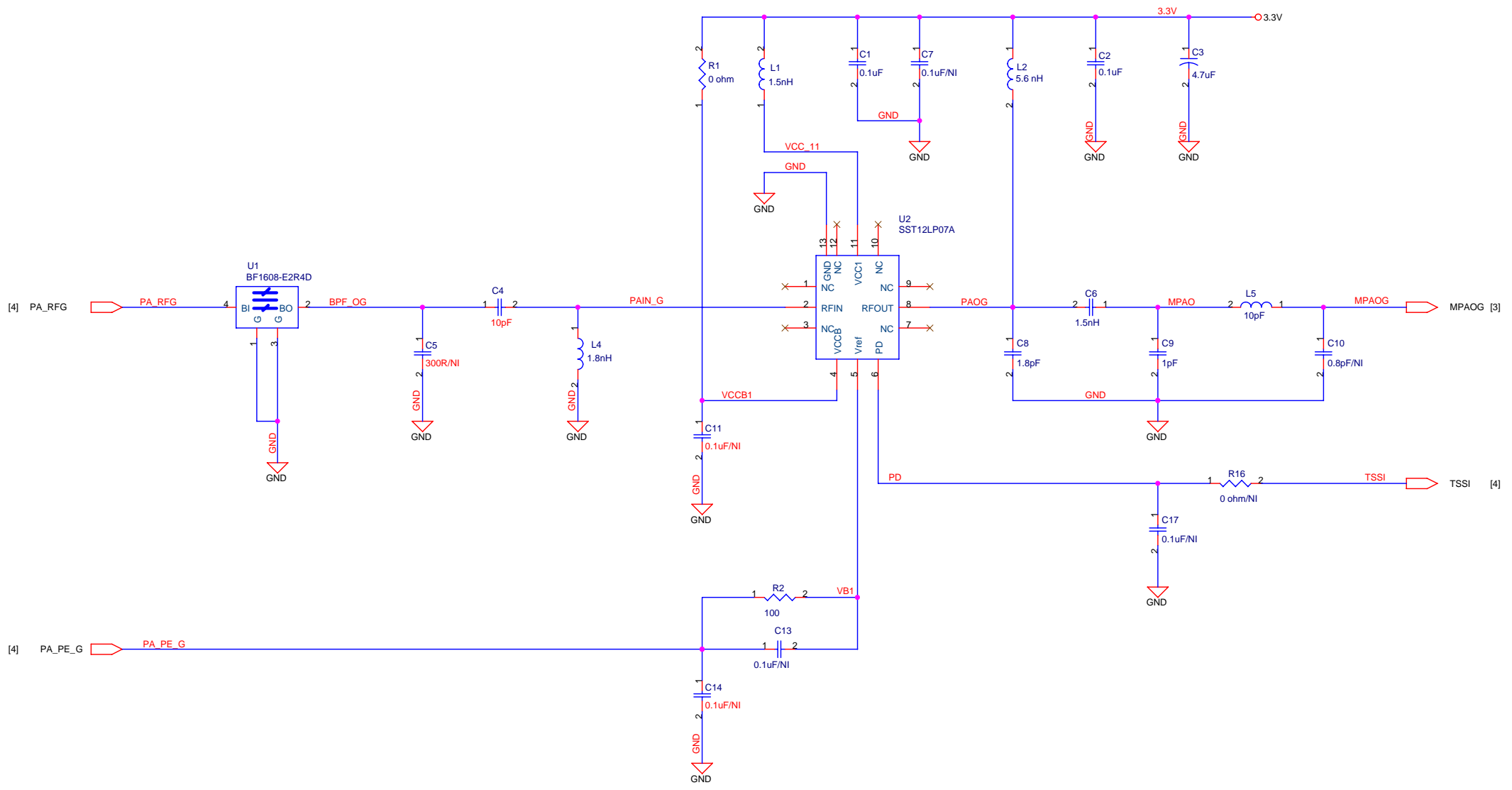
SOT-23-3




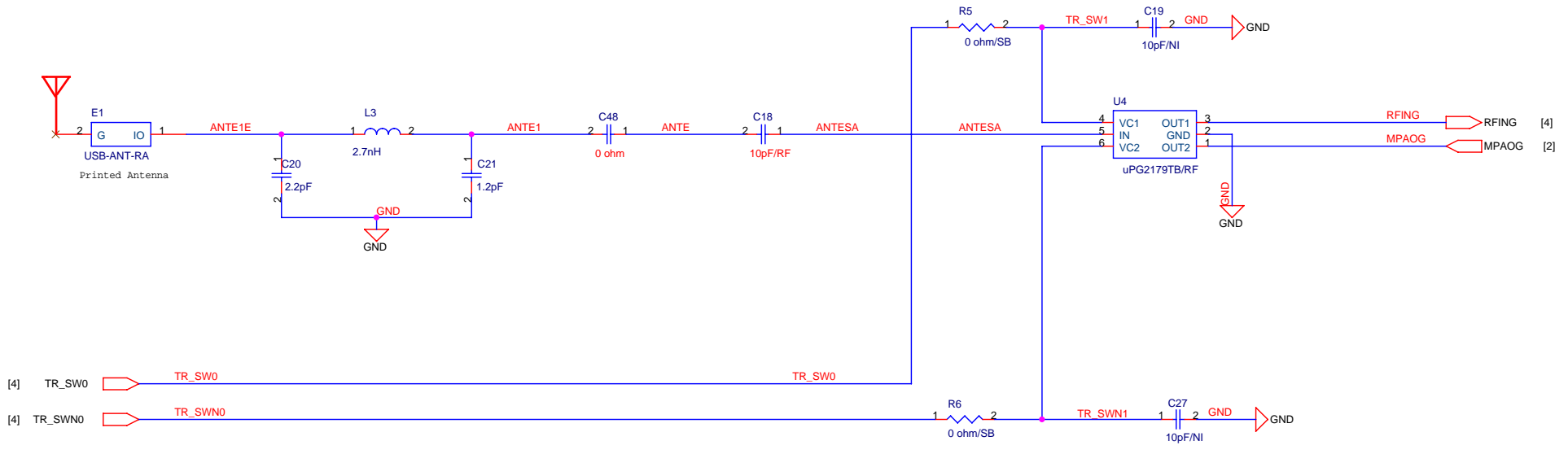



Filename:
PEN-RT3070-QFN-V33ST-A-081013.DSN

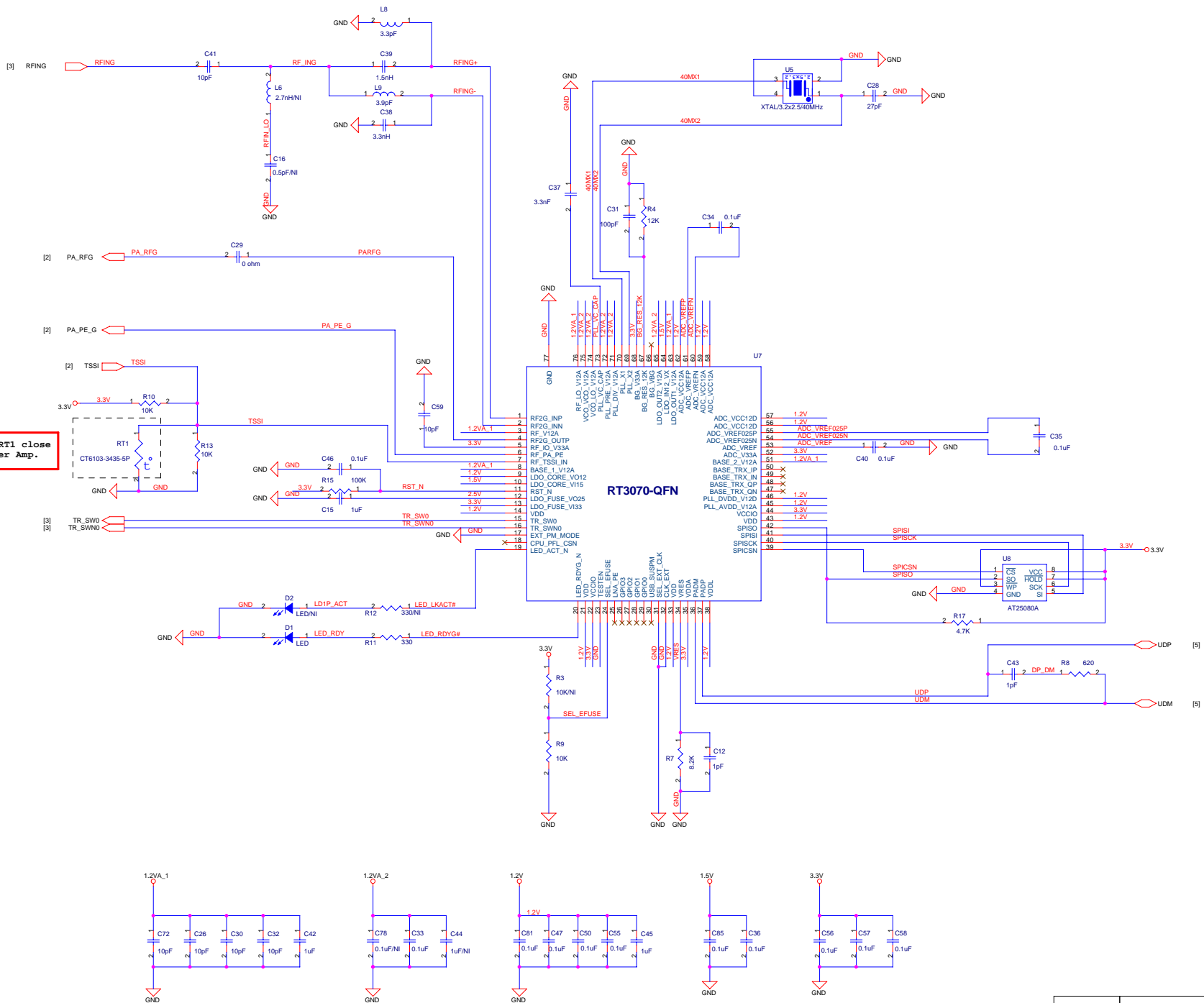
	RALINK TECHNOLOGY, CORP.	
	Title 2.4G USB Card - RT3070	
Size B	Document Number PEN-RT3070-V33ST-A.SCH	Rev 3.3
Date: Tuesday, November 25, 2008	Sheet 1 of 6	



		RALINK TECHNOLOGY, CORP.	
		Title 2.4GHz PA	
Size B	Document Number 1-PA-SST12LP07A.SCH		Rev 3.3
Date:	Wednesday, October 15, 2008		Sheet 2 of 6

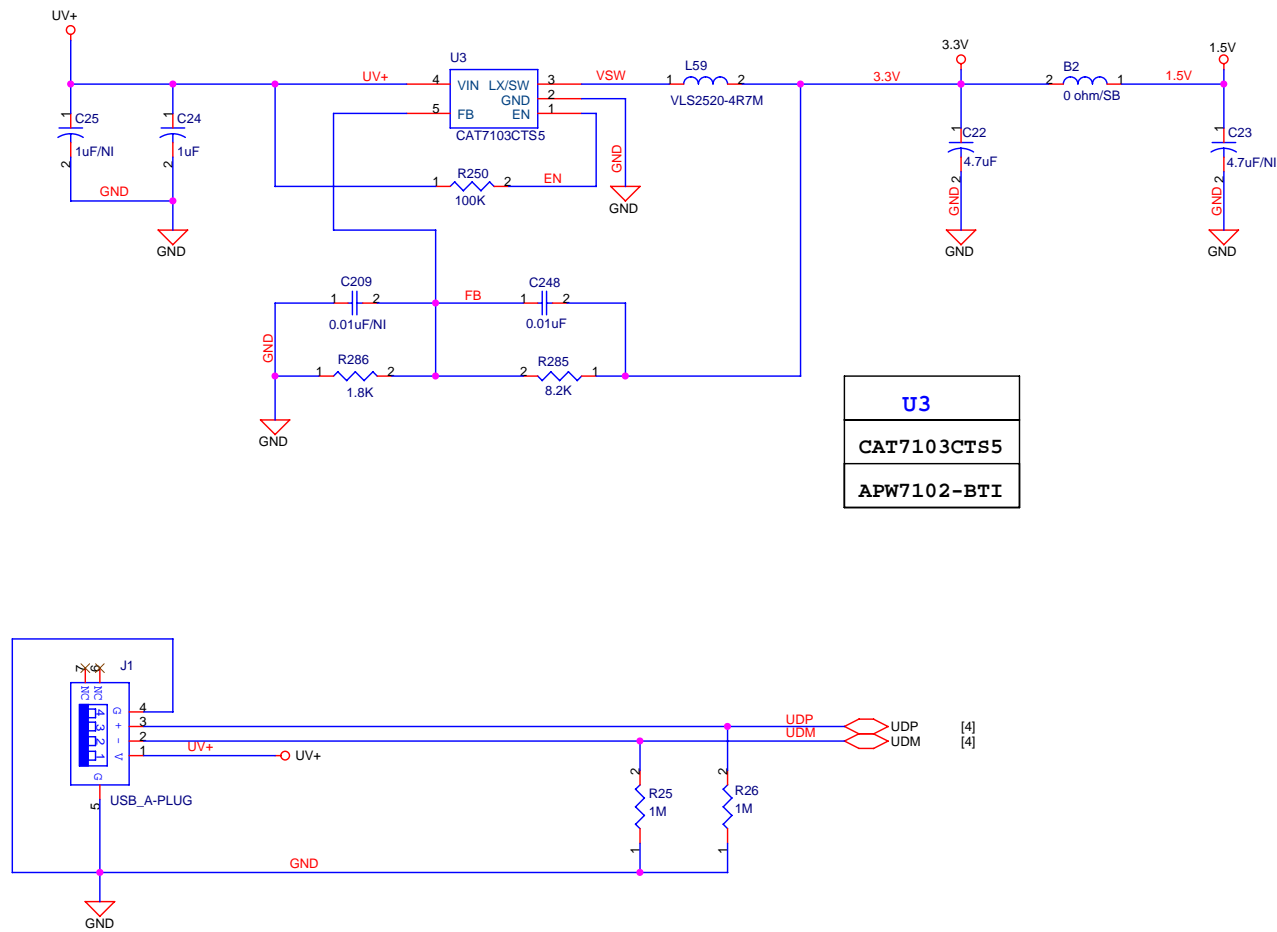


		RALINK TECHNOLOGY, CORP.	
		Title Front-End	
Size B	Document Number 2-FrontEnd.SCH		Rev 3.3
Date:	Wednesday, October 15, 2008	Sheet	3 of 6




Place RT1 close to Power Amp.

Ralink Technology, Corp.		
File	RT3070-WLAN	
Size	Document Number	Rev
C	3-RT3070-WLAN.SCH	3.3
Date	Wednesday, October 15, 2008	Sheet 4 of 6



U3
CAT7103CTS5
APW7102-BTI

		RALINK TECHNOLOGY, CORP.	
		Title PEN USB Interface and Power	
Size B	Document Number 4-USB-A.SCH	Rev 3.3	
Date: Tuesday, November 25, 2008	Sheet 5	of 6	

