Description of Operation

The TMS320DM365ZCE is the central controller of the GXV3500 whole system, it has direct interface to on the board memory and all peripherals , so no glue logic is needed in system design. The system has one 1Gbit NAND flash which can be expanded to 16Gbit NAND flash. One 64MX16Bit DDR2 is used on the board, but it also can be expanded to 256MByte.

The system also have some I/O port for the external multi-media applications, On network size, the system provide one 802.3 Ethernet RJ45 connection to LAN, The MICIN and LING OUT for user to connect to tone arm and audio AMP, a CVBS connector lets user to be able to use TV for a bigger display, The IO connector are for the alarm in, alarm out and also for the RS485 control.

1 Interface

1.1 Interface between the TMS320DM365ZCE and NAND flash

The NAND flash in the system is mainly used for program and data storage, based on the application, the system May need to support up to 1GB NAND flash, the system supports booting from 8-bit NAND devices (16-bit NAND devices are not supported),supports 4-bit ECC (1-bit ECC is not supported),supports NAND flash that requires chip select to stay low during the tR read time. Figure 6.1.1 below shows the interface between processor and NAND flash：

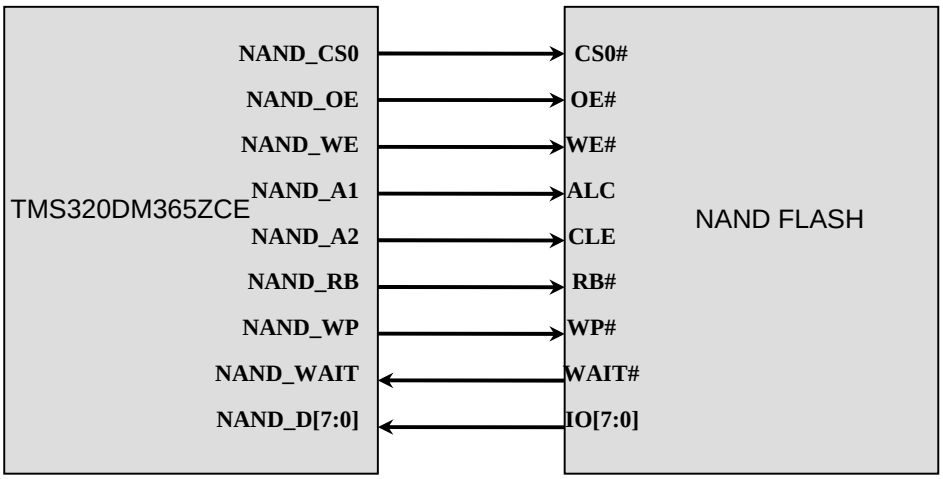

Figure 1.1 Signal connection between TMS320DM365ZCE and NAND flash

1.2 Interface between TMS320DM365ZCE and DDR2 SDRAM

The TMS320DM365ZCE DDR2 Memory Controller is a dedicated interface to DDR2 / mDDR SDRAM. It supports JESD79D-2A standard compliant DDR SDRAM devices and compliant Mobile DDR SDRAM devices . DDR2 SDRAM plays a key role in a DM365-based system. The DDR2 Memory Controller supports the following features:

- JESD79D-2A standard compliant DDR2 SDRAM

- Mobile DDR SDRAM
- 256 MByte memory space
- Data bus width 16 bits
- Burst length: 8
- Burst type: sequential
- 1 CS signal
- Page sizes: 256, 512, 1024, and 2048
- SDRAM autoinitialization
- Self-refresh mode
- Power down mode
- Prioritized refresh
- Programmable refresh rate and backlog counter

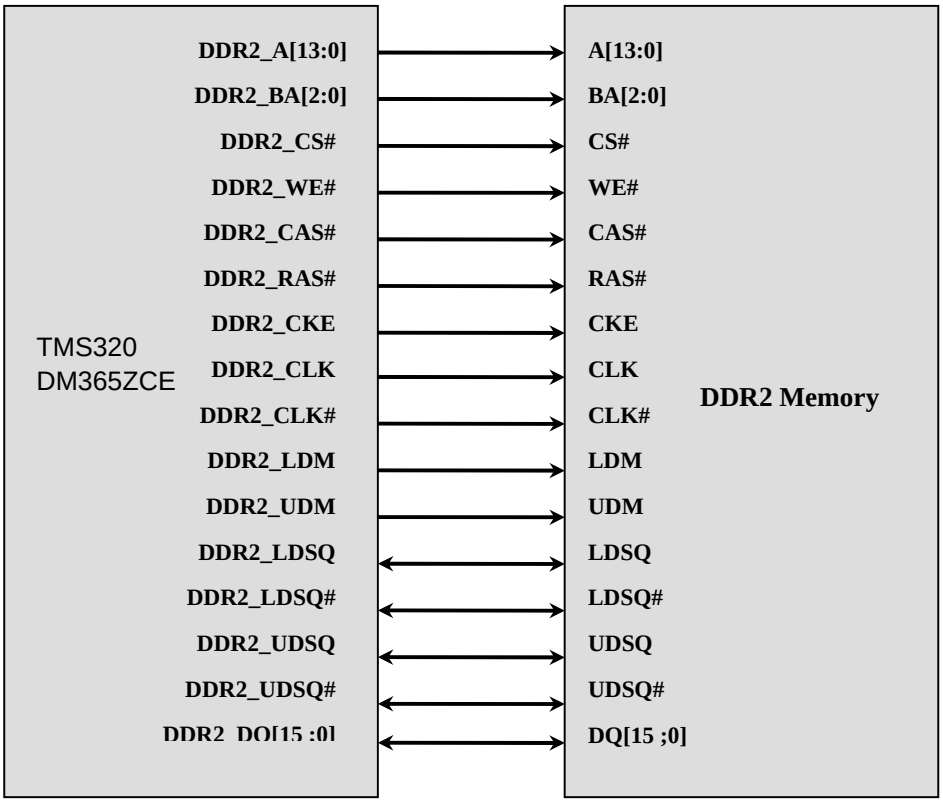

Figure 1.2 Signal connection between TMS320DM365ZCE and DDR2 memory

Main chip DM365 ‘s MAX operating frequency : 216MHz