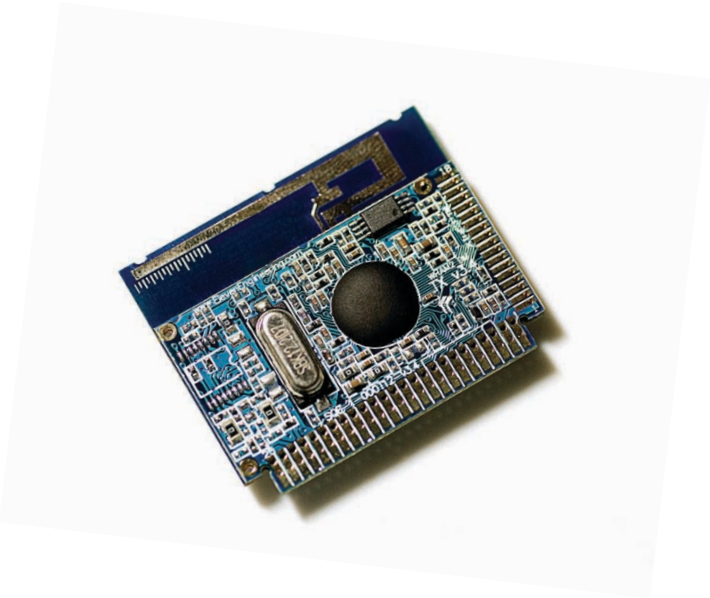
HT-201/202 Datasheet

Digital Wireless Audio Modules

HT



General Description

The HT-201/202 is a complete high-performance wireless home theatre audio solution, capable of transmitting a Left/Right surround audio channel pair for wireless rear speakers (HT-202), or a single Low Frequency Effects (LFE) channel to a wireless subwoofer (HT-201) across a robust 2.4 GHz radio frequency link.

The HT series of Wireless Hi-Fidelity Audio Modules (WHAM) are highly-integrated module packages utilizing the revolutionary XInC2 wireless processor. Eleven's proprietary adaptive frequency hopping protocol uses a narrow footprint in the 2.4 GHz band allowing seamless co-existence with other devices and offering unparalleled Quality of Service.

Each module typically requires two well filtered power supply rails for operation. A Digital power rail to supply the XInC2 processor and an RF power rail to supply the 2.4 GHz radio. HT audio modules accept, and output digital audio information in I2S format. Interfacing to the module is possible through standard two-wire I2C protocol, or through the built-in XInC Programming Debug (XPD) port using XInC2's Serial Peripheral Interface (SPI).

The HT audio module series comes pre-programmed with a standard software feature set that is built into the HT Standard Application Firmware, which includes bi-directional data control channels, low-power sleep modes, remote volume, mute control and automatic RF Mating.

Features

- Digital I2S Audio Input/Output
- 48 kHz, 16-bit digital, Stereo/Mono audio transmission
- Digital volume control, manual mute
- Auto mute (when signal lost)
- 2.4 GHz wireless at 1.536 Mbps
- High Quality of Service (QoS)
- Walking Frequency Diversity™ (WFD) – Eleven's proprietary adaptive frequency hopping protocol.
- Standard Application Firmware – Includes a complete set of built-in wireless audio software features and interface control functions.
- Optional HPX™ audio codec delivers CD-quality sound with ultra low THD+N across the entire audible band.
- 15m indoor range
- Up to 4 transmitters in specified range area
- Low latency; firmware selectable 20 – 64 ms
- Bi-Directional Data Channel
- Small form factor
- Compatible with FCC/ETSI regulations
- Two-wire Serial Data Interface

Ordering Information

Item	Description	Catalog #
HT-201: Audio Modules	TX	WH4946
	RX	WH4947
HT-202: Audio Modules	TX	WH4948
	RX	WH4949
HT-201: PB3 Evaluation Kit	TX	EV4946
	RX	EV4947
HT-202: PB3 Evaluation Kit	TX	EV4948
	RX	EV4949

TABLE OF CONTENTS

LIST OF TABLES

List of Figures

Contacting Technical Support

For all product questions and inquiries visit Eleven Engineering's online support page at **www.ElevenEngineering.com/support/** or contact an Eleven Sales Representative. To find one near you visit **www.ElevenEngineering.com/**

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1 CHARACTERISTICS AND SPECIFICATIONS

1.1 ABSOLUTE MAXIMUM RATINGS

All Min/Max characteristics and specifications are guaranteed over the specified operating conditions. Typical performance characteristics and specifications are derived from measurements taken at typical supply voltages. T_A=25°C. GND = 0 V, all voltages with respect to 0 V.

Transmitter

Parameter	Symbol	Value	Unit	Note
RFM Power	RFVCC	3.6	V	
Digital Power	VCC	3.63	V	
Digital Input Pin Absolute Maximum Input Voltage	GPIOx, ID_DATA, ID_CLCK, / RESET, MISO0, MOSI, CS0	3.63	V	IO Inputs are not 5 V Tolerant.
Operating Temperature	TA	50	C	
Storage Temperature	TS	90	C	

Table 1 – TX Absolute Maximum Ratings

Receiver

Parameter	Symbol	Value	Unit	Note
RFM Power	RFVCC	3.6	V	
Digital Power	VCC	3.63	V	
Digital Input Pin Absolute Maximum Input Voltage	GPIOx, ID_DATA, ID_CLCK, / RESET, MISO0, MOSI, CS0	3.63	V	IO Inputs are not 5 V Tolerant.
Operating Temperature	TA	50	C	
Storage Temperature	TS	90	C	

Table 2 – RX Absolute Maximum Ratings

1.2 TRANSMITTER OPERATING CONDITIONS

Parameter	Conditions	Min	Typical	Max	Unit
POWER CONSUMPTION					
Digital Power Supply		3.0	3.3	3.6	V
RF Power Supply		3.0	3.3	3.6	V
Digital Current	VCC = 3.3 V		53		mA
RF Current	VCC = 3.3 V		130		mA
RF Current Duty Cycle	Transmit Mode: Receive Mode:		92 8		% %
Audio Level Standby Current	Average Draw		50		mA
LOGIC THRESHOLDS					
Input Low Voltage Threshold	VCC = 3.3 V			0.8	V
Input High Voltage Threshold	VCC = 3.3 V	2.0			V
Output Low Voltage Threshold	VCC = 3.3 V			0.4	V
Output High Voltage Threshold	VCC = 3.3 V	2.4			V
Input Leakage Current	VCC = 3.3 V	-10	± 1	10	µA
TEMPERATURE					
Operating Temperature	All Power Ranges	0		60	C
Storage Temperature		-20		90	C
Standard Data Channel					
Tx I2C Interface Max Output Rate*	Tx to Rx		1		kbps
Tx Data Channel Latency**	Tx to Rx		11		ms
Extended Data Channel					
Tx I2C Interface Max Output Rate*	Tx to Rx		30		kbps
Tx Data Channel Latency**	Tx to Rx		6		ms

Table 3 – TX Operating Conditions

*Data rates averaged over 10 seconds
**Latency dependent on number of retransmissions

1.3 RECEIVER OPERATING CONDITIONS

Parameter	Conditions	Min	Typical	Max	Unit
POWER CONSUMPTION					
Digital Power Supply		3.0	3.3	3.6	V
RF Power Supply		3.0	3.3	3.6	V
Digital Current	VCC = 3.3 V		42		mA
RF Current	VCC = 3.3 V		65		mA
RF Current Duty Cycle	Transmit Mode: Receive Mode:		4 96		% %
Sleep Mode Current Consumption	Average Draw		30		mA
LOGIC THRESHOLDS					
Input Low Voltage Threshold	VCC = 3.3 V			0.8	V
Input High Voltage Threshold	VCC = 3.3 V	2.0			V
Output Low Voltage Threshold	VCC = 3.3 V			0.4	V
Output High Voltage Threshold	VCC = 3.3 V	2.4			V
Input Leakage Current	VCC = 3.3 V	-10	± 1	10	µA
TEMPERATURE					
Operating Temperature	All Power Ranges	0		60	C
Storage Temperature		-20		90	C
Standard Data Channel					
Rx I2C Interface Max Output Rate*	Rx to Rx		1		kbps
Rx Data Channel Latency**	Rx to Tx		6		ms
Extended Data Channel					
Rx I2C Interface Max Output Rate*	Rx to Tx		3.6		kbps
Rx Data Channel Latency**	Rx to Tx		7		ms

Table 4 – RX Operating Conditions

*Data rates averaged over 10 seconds
**Latency dependent on number of retransmissions

1.4 RF CHARACTERISTICS AND BEHAVIOR

The HT Series audio module RF characteristics are described below paying special attention to include information pertinent to FCC and ETSI regulations.

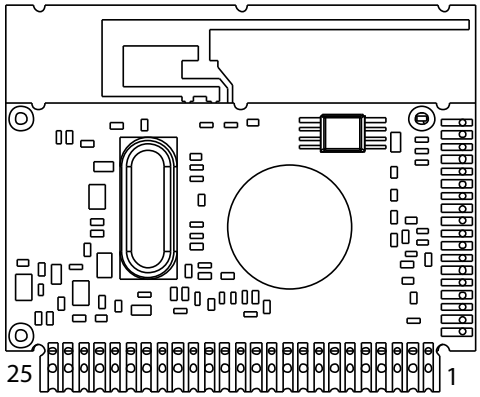
HT firmware operates by selecting a palette (or group) of random channels out of the total 38. Any channels with poor transmission rates are replaced with better channels from the remaining unused channels. The switching pattern from channel to channel is a random pattern. The table below describes some important aspects of the channel-hopping algorithm:

Parameter	Conditions	Min	Typical	Max	Unit
RF CHARACTERISTICS					
Transmission Method		ARQ with Adaptive FHSS			
Raw Data Rate				1.536	Mbps
Channel Width			<2		MHz
Total Channels				38	Ch
Hopping Channels			20		Ch
RF Coexistence	In Specified Radius			4	sets
TX Output Power		14	16	18	dBm
DETAILED BANDWIDTH CHARACTERISTICS					
Hopping Rate			187.5		Hz
Frequency Dwell Time			5.333		ms
Audio TX: RF Transmit Time	Tx Node		4.594		ms
Audio RX: RF Transmit Time	Per Each Rx Node		0.219		ms
Frequency Range (Total)	FCC Test Method	2.40197		2.48002	GHz
20 dB Channel BW			78.057		MHz
Distance to upper ISM band limit	FCC Test Method		1.94		MHz
Distance to lower ISM band limit			3.476		MHz
Distance to lower ISM band limit			1.967		MHz
Antenna Impedance	ZAnt		50		Ω
RF RANGE					
Indoor Range (Note 1)				15	m
Open Field Range (Note 2)				180	m

Table 5 – RF Characteristics

Notes:
1. Typical home/office environment (estimated)
2. Actual open field line of sight testing results.

1.5 PIN DESCRIPTION



Pin#	Tx Pin Function	Rx Pin Function	Description
1	RFVCC	RFVCC	RF Voltage Power Input
2	GND	GND	RF Ground
3	GND	GND	Digital Ground
4	VCC	VCC	Digital Power Input
5	/RESET	/RESET	Reset input (active low)
6	PB1	PB1	SPI0 Chip Select (CS0) PB1
7	MISO0	MISO0	SPI0 Master Data Input MISO0, or GPIO port PG0
8	MOSI0	MOSI0	SPI0 Master Data Output MOSI0, or GPIO port PG1
9	SCK0	SCK0	SPI0 Clock output SCK0, or GPIO port PG2
10	SDA	SDA	Two Wire Serial Data
11	SCL	SCL	Two Wire Serial Clock
12	Bond0 LED	Mute LED	Bond0 / Mute LED
13	Bond1 LED	Bond LED	Bond LED
14	RF-Mate	PC4	RF-Mate Push Button / GPIO PC4
15	Vol. Down	Mute	Volume Down / Mute Push Button
16	MCLK	MCLK	Master Clock Output
17	Vol. Up	Amp Disable	Volume Up Push Button/ Amp Disable Pin
18	Mute	Vol. Down	Volume Down/ Mute Push Button
19	LRCK	LRCK	Left-Right Clock (LRCK)
20	ADC Reset	Vol. Up Button	ADC Reset Pin / Volume Up Push Button
21	GND	GND	Ground
22	SDIO0	SDIO0	Serial DASI Data input/output SDIO0
23	BCLK	BCLK	Serial DASI Bit Clock output BCLK
24	GND	GND	Ground
25	(no connect)	(no connect)	n/a

Table 6 – Tx/Rx Pinout

1.6 AUDIO CHARACTERISTICS

Parameter	Symbol	Conditions	Min	Typical	Max	Unit
Signal to Noise Ratio: A-weighted Un-weighted	SNR	Left Channel, 997 Hz		 >95 >92		 dB FS dB FS
Signal to Noise Ratio: A-weighted Un-weighted	SNR	Right Channel, 997Hz		 >95 >92		 dB FS dB FS
Line THD+N, Left Channel	THD+N	997 Hz @ -1 dB FS			0.063	%
Line THD+N, Right Channel	THD+N	997 Hz @ -1 dB FS			0.063	%
Audio Bandwidth	BW	@-1 dB FS	10		20000	Hz
Pass Band Ripple		-1 dB FS 20 Hz – 20 kHz			±0.2	dB

Table 7 – Audio Characteristics

2 FUNCTIONAL DESCRIPTION

2.1 WIRELESS SYSTEM DESCRIPTION

Frequency Hopping Spread Spectrum (FHSS)

A frequency hopping spread spectrum (FHSS) system works by hopping from one frequency channel to another in a known sequence out of a select group of channels. The HT system frequency hops between 20 channels. The group of 20 channels is selected out of a total of 38 hopping channels in the ISM band. If it is determined that one of the 20 hopping channels is found to be noisy or poor due to other RF interference, then a new channel is selected from the 18 unused channels (i.e. 38 – 20 = 18) and the one noisy channel is released to the unused group. This repeats whenever a noisy or poor channel is detected.

The master dwells on a single hopping channel and transmits a data packet to the slave Rx. When the slave Rx receives a good data packet from a Tx, the Rx sends an acknowledgment back to the Tx. Once the slave Rx has responded to the master Tx, then both the Tx and Rx units each hop to the next frequency channel and the process is repeated.

However, when the Rx receives a corrupted data packet from a Tx, the Rx transmits a resend request back to the Tx. The Tx responds by re-transmitting the last packet of audio data. In this way the Rx can maintain a high quality of service (QoS) by replacing bad audio data with good audio data before the data is decoded and output to the speaker. This technique is known as data buffering.

A large data buffer size provides higher QoS than with a low buffer size, however a large data buffer size has higher system latency (i.e. up to 64 ms) compared to the latency of a small 20 ms buffer. If a Tx and Rx receive channel interference from another Tx-Rx system, or from other RF interference on the same hopping channel, then the Tx and Rx units have an opportunity to request for the data to be re-transmitted. This re-transmission scheme provides a time delay for the interfering Tx and Rx to change channels again before the re-transmission occurs. Thus a Tx-Rx audio data packet would have a higher probability to get successfully transmitted and received when a re-transmission occurs.

FHSS frequency hopping allows multiple systems and other RF devices to coexist in the same area, since each system selects a different pseudo random group of 20 hopping channels. Also, each system hops from channel to channel in a different 20 channel sequence from other systems. This allows multiple systems to coexist with minimal channel contention and interruption from nearby RF interference.

Indoor vs. Open Field Range

Open Field range is experimentally determined in an outdoor environment with no obstructions between the transmitter unit and the receiver unit, no other RF devices in the area and no multipath-creating objects aside from the earth itself. Indoor range can only be estimated because it is dependent on the type of physical obstructions such as building materials, building construction, obstacles, human body obstacles, and the presence of other RF devices in the same area, all of which vary from location to location.

2.2 AUDIO COMPRESSION CODEC

The HT wireless audio system is a digital audio system that operates at 1.536 Mbps of data transfer from the Tx unit to the Rx unit; therefore, the system must use data compression-decompression software to lower the amount of data to be transferred from the Tx unit to the Rx unit. The audio codec compresses the 16-bit digitally sampled data, sampled at 48 kSps (kilo-Samples-per-second) from the analog-to-digital converter, down to 5-bit digital data. This 5-bit data is then transmitted from the Tx unit to the Rx unit(s). When each Rx unit receives the 5-bit data, it decompresses the data from 5-bits back to 16-bits of digital-audio data. The Rx then uses the digital-to-audio converter (DAC) to translate the 16-bit digital audio back to an analog audio signal.

Disclosure Prevention/ Data Scrambling

The disclosure of the original audio data stream from the wireless audio system is prevented by data scrambling. Data scrambling is achieved using a proprietary multi-predictor compression algorithm that has been developed by Eleven Engineering. Each audio sample is compressed using the multi-predictor codec algorithm before the Tx transmits it over the wireless link. Once the data is received at the Rx unit, each audio sample is decompressed, again using Eleven's multi-predictor codec algorithm. If the data stream is read by another device its data content is undecipherable.

In addition, each customer is assigned a "License ID" number. Upon accepting the Software License Agreement, each customer agrees to incorporate their license ID number into their Tx and Rx firmware versions. Once the ID is imbedded in the firmware, then only Rx products with the customer's specific license ID can receive and decode the digitized audio.

2.3 MODES OF OPERATION

There are several modes of operation for the HT Standard Application Firmware. Each mode is described in further detail in the paragraphs below. For more information on how to configure the HT module into each mode, refer to Section 4.2. The modes of operation include:

- **Reset**
- **Module Standby**
- **Normal Bond Search**
- **Sleep**
- **Bonded**
- **Bonded & looking for additional receivers**
- **RF Mating**
- **Add-A-Node**

Reset:

All of the Digital Logic in the HT module can be held in a reset state by using the Reset pin on the Edge connector. In this state all of the Digital I/O on the HT module will be set to inputs.

The HT module can be placed into standby mode by setting the “standby” bit of the Command0 register accessed by the 2 wire serial interface. In standby mode the module is in a low power state. The RF module is turned off so no bond can be established with another device, but commands on the 2 wire serial interface are received. In this state, the audio clocks are disabled.

Normal Bond Search:

This is the normal mode that the module uses to acquire a link (bond) with another HT device. In this mode the Tx will send out poll requests looking for responses from an Rx. The Rx listens for Tx poll requests before it transmits a response.

Sleep:
On the Rx, this mode is entered after a configurable amount of time has passed with no bond to a Tx. In this mode, the Rx will still attempt to bond to a Tx, but will alternate between bond search and module standby to conserve power.

On the Tx this mode can be entered by using the audio level detection algorithm. (See the noise gate configuration in the 2 wire serial interface section). If the audio level is below a certain threshold for a configurable amount of time, then sleep mode can be entered. In this mode the normal bond search mode is entered only after the audio level goes above the configurable threshold

Bonded:
This is normal operation mode where the Tx and Rx are bonded and audio is transferred across the link.

RF Mating:
This mode is used to RF Mate a transmitter to a receiver. (Refer to Section 4.2)

Add-A-Node:
This mode is similar to RF Mating, however the existing Mating ID of the system will be retained and copied to the new node added to the system. (Refer to Section 3.3 for details).

2.4 FIRMWARE LOADING

The Standard Application Firmware package will allow the developer to take full advantage of many useful features that have already been built into the HT Application, and to ensure easier integration into the final product motherboards. The process below will describe how to download and update firmware to the HT audio module.

XPD Programming Module

Eleven strongly recommends for customers to include pins 3, 4, 5, 6, 7, 8 and 9 of the HT module edge connector in their design layout, and connect these pins to an 8x1x0.1" header.

This 8x1x0.1" connector is the XInC Programming Debug (XPD) port used to download firmware hex files to the modules. To do this, an XPD Programming Module, flat ribbon cable, programming cable, RS232 cable, and the XInC Development Environment (XDE) program are required. During firmware development, this XPD port is required to download firmware into the Tx and Rx modules. For mass production, customers can reduce part costs by not populating the 8x1x0.1" programming connector if it is not required.

Customers can purchase an XPD Programming Module and ribbon cables from Eleven Engineering, or build their own based on the Schematic, BOM, Assembly Drawing, and Gerber files, which are all available from Eleven without charge. The XDE download program is also available from Eleven's website without charge.

Downloading Firmware using the XinC2 Development Environment

Download the XInC Development Environment (XDE) program from Eleven's website. The XPD program is used to download hex files to the HT modules. Save and run the XDE.exe file. An XPD Programming module is required. Follow this firmware file download procedure:

(1) Connect the flat ribbon cable to the XPD Programmer Module on Port 3. The black line on the ribbon cable must be positioned at pin 1 of Port 3.
(2) Connect the ribbon cable to the XPD port on the Tx. The black line must be positioned at pin 1.
(3) Run the XDE program, select the "FILE" heading, and open the Master .hex file.
(4) Click "Download" in the menu. Select the correct computer serial COM port and click download. Click the reset button on the Tx unit (or turn the power to the Tx Off, then On again) and the program will begin to download.

(5) Wait 5 seconds after the download has been completed for the EEPROM to be fully programmed. This is so that the XInC2 processor has enough time to completely transfer the firmware into the EEPROM from the XPD module. (Note: This is an important step, don't skip it!)

(6) Repeat this procedure for the Rx, except using the Slave .hex file.

Downloading Firmware using the XinC Loader

The XInC Loader program is another utility used to download hex files and parameters to the HT modules. An XPD Programming module is required. Follow the file download procedure outlined below:

(1) Connect the flat ribbon cable to the XPD Programmer Module on Port 3. The black line on the ribbon cable must be positioned at pin 1 of Port 3.

(2) Connect the ribbon cable to the XPD port on the Tx module. The black line must be positioned at pin 1 which is the 3.3V pin.

(3) Open "XinCLoader.exe".

(4) Select the appropriate COM port from the drop down menu.

(5) Ensure the checkboxes "Unlock" and "Erase" are checked.

(6) Check the "Load Firmware" check box and Drag and Drop, or Browse for the Firmware hex file you wish to load.

(7) If loading Parameter pages, Check the "Load Squeak Parameter Page" or "Load Audio Parameter Page". Drag and Drop, or Browse to the appropriate Parameter Page hex files you with to Load

(8) Click "Start" and press the reset button on the unit (or turn the power off, then on). Then download will begin.

(9) Repeat this procedure for the Rx, using the Slave .hex file.

3 ADVANCED FEATURES

Standard functions in Application Firmware have been developed to accommodate a variety of different design options. A summary of some useful software features are outlined below:

3.1 RF MATING

Following power on, the Tx and Rx nodes search for each other and then establish a link (called a Bond). Mating occurs when a unique number is used to distinguish all of the Tx and Rx nodes in a system. Bonding requires that the Tx and Rx units have the same Mating ID (exact match). Mating is typically done only once in the whole life of the system. Usually, it is done in the plant before the final product goes into packaging. However, the HT Standard Application Firmware features an automatic Mating procedure called RF Mating that can be performed if necessary.

RF Mating is the procedure of matching the 16-bit ID of the transmit node (Tx) to 1 or more receive nodes (Rx) using a single button on the Tx. After an Rx node has been "RF mated" it will not connect to any other Tx until it sees a Tx node in RF mating mode. Currently, the RF system supports up to 4 Rx nodes. The Node topology of the system is configured at the same time as the RF Mating procedure.

When first power on, the Tx node will fetch it's 16 bit Mating ID from the EEPROM on the module and use this value until the RF Mating button has been pressed for more than 3 seconds or the RF Mating has been initiated using the 2 wire interface. When RF Mating has been initiated a 16 bit random number is generated and used for the new Mating ID.

This Mating ID is stored in the EEPROM only if a connection is established with an RX node. If the RF Mating procedure times out without Mating to any RX nodes it will terminate RF Mating mode and revert back to the previous Mating ID. The number of Rx nodes that RF Mate to the Tx will define the new topology after the RF Mating has timed out or completed.

The operating procedure is defined below:

1. Turn off Rx devices
2. Turn on Tx device. Tx will start to look for an RX device with the same Mating ID
3. Initiate RF Mating using one of two methods:
   - Press the RF Mating Button for greater then 3 seconds
   - Set the RF Mating Bit using the 2 wire interface. The Bond0 Led on the TX will begin to flash once RF Mating has begun
4. Power on Rx. The Rx device will begin a cycle of looking for a Tx with its current Mating ID for 3 seconds and then switch to looking for any Tx in RF Mating Mode for 3 seconds. The Rx device will continue this cycle indefinitely until it bonds with a Tx with the same Mating ID or it RF Mates to a new Tx.
5. The RF Mating procedure will terminate if no Rx node mates before the configured timeout. The Tx will use the original 16 bit Mating ID and will enter normal bond search mode.
6. When the RF Mating procedure times out after at least one Rx node has RF Mated, the number of Rx nodes bonded will define the Node topology until the RF Mating algorithm is repeated.

3.2 RF MATING: ADD-A-NODE

This RF mating mode is triggered by either a quick press of the RF mate button or by setting bit 4 in register 0x1E (Refer to Section 4.2 for more information). In this mode the mating ID will not be changed and a normal RF Mate operation will be triggered. After the slave bonds up the node topology will be incremented up to the Max Nodes (reg 0x02) setting and the connection will be reset. Using this mode any number of slaves may be added to a system, only the number of slaves specified by the node topology (reg 0x02) may be bonded at one time.

The operating procedure is defined below:
1. Press the RF mate button for less than 3 seconds
2. Cycle the power on the Rx

3.3 BI-DIRECTIONAL DATA CHANNELS

HT Series Audio Modules are able to transfer non-audio user data over two bi-directional data channels. **The Standard Data Channel** has a data transfer rate of 1 kbps maximum from the Tx to Rx and 1 kbps from the Rx to the Tx. The Standard Data Channel can be used to pass control information or digital data between the Tx and Rx units, such as commands for Play, Pause, Stop, Fast Forward, Rewind, Volume, Mute, disk and track information, remote power off, or any type of data the designer wishes to transfer between devices. In the event that a higher data rate is required, an **Extended Data Channel** is also available to transmit a larger amount of data from the Tx to one Rx at a rate of 30 kbps from Tx to Rx and 6 kbps from Rx to Tx.

3.4 VOLUME CONTROL MODES

HT audio modules are able to function in two different volume control modes depending on the nature of the product and the requirements of the designer. When set to **Global Volume Mode**, an absolute system wide volume on the master is stored. Upon bond up, the master sends the current system volume to a newly bonded slave. A change on the master is sent to all slaves and a change from a slave is sent to the master where it is distributed to all other slaves. When configured for **Local Volume Mode**, each slave stores it's own absolute volume level. The Master will not send changes across the link and each slave will ignore any incoming volume changes received from the system.

3.5 AUDIO LEVEL STANDBY

HT Series audio modules have sleep mode functionality built into Standard Application Firmware. Once in sleep mode, the modules will enter a low power mode when not active. On the Tx, this mode is known as audio level standby. In this mode, the Tx can be configured to enter a low powered sleep state after a configureable amount of time that the audio signal is below a specified threshold. Once in sleep mode, both the Tx and Rx will enter a low powered sleep state until the audio signal at the transmitter's audio inputs goes above this threshold.

The Rx also has a separate low power sleep mode that can be entered given a certain amount of time that has passed without bond to a Tx. In this mode, the Rx will wake up periodically to look for it's mated Tx. If none are found, it will return to the low power sleep state. Once a Tx is found, then the Rx will wake up fully and operate normally.

3.6 SUPPORTED AUDIO DEVICES

HT audio modules support a wide variety of industry standard audio devices for easy compatibility. System firmware can be configured to initiate the devices to a default state, eliminating the need for an external micro-controller. Eleven recommends choosing an external audio device from the list below to ensure maximum compatibility with the HT audio module.

Device Name	Type
PCM1803	ADC
PCM1808	ADC
CS5341	ADC
CS8421	SRC
CS4341	DAC
CS4L51	DAC/Class Amp
PCM1770	DAC/HP Amp
STA308	Audio Processor
TAS5010/TAS5012	Audio Processor
TAS5086	Audio Processor
TAS5504	Audio Processor

4 CONTROL PORT INTERFACE

HT wireless audio modules feature a built in 2 wire serial interface port. This interface serves three main purposes:

1. HT Parameter Configuration
2. Bi-Directional data link interface
3. Control of external devices such as ADC,DAC, and other devices.

The first is to provide a conveient method for external devices to configure HT system parameters. Parameter configuration using I2C is not a requirement for operation but provides benefits for developers. Examples of the parameters that can be configured are Mating ID, number of receiver nodes, audio mode for each slave (stereo, mono), latency, and volume. (Refer to Section 4.2 for a list of control registers)

The second purpose is for external devices to access the bi-directional data link that is provided by the HT RF Link protocol in addition to the audio link. (Refer to Section 4.3 for a description of the data channel registers)

The third purpose is to allow the HT System to configure external audio devices or other types of devices such as LCDs, etc. (Refer to Section 4.3)

In Slave Mode, the communication follows Standard I2C protocol. See the I2C-Bus Specification Version 2.1 for more information on the standard read and write protocol (also described below). The I2C slave address can be set to any 7-bit value. The address can only be changed using the XPD interface. The default 7-bit slave address of the HT system is **0x12**. This slave address is fully configurable to ensure that an address collision can be easily avoided in systems where the bus has many devices on it. The I2C address can be programmed using the same utilities that the customer would use to set up their default parameters.

4.1 I²C INTERFACE

HT control registers can be configured via the I2C Two-Wire serial interface, which consists of a control data line (SDA) and a serial control clock (SCL). The procedures outlined below describe the operation of writing to, or reading from the HT Control registers.

I2C Write

1) Initiate a START condition on the I2C bus.
2) Write the HT I2C Slave address byte (0x12 by default). The 8th bit of the address byte is the R/W bit, set low.
3) Wait for an acknowledge (ACK), then write the control register address to be written.
4) Wait for an acknowledge (ACK), then write the desired data to the specified register.
5) Repeat the previous step until all the desired registers are written.
6) Initiate a STOP condition to the bus.

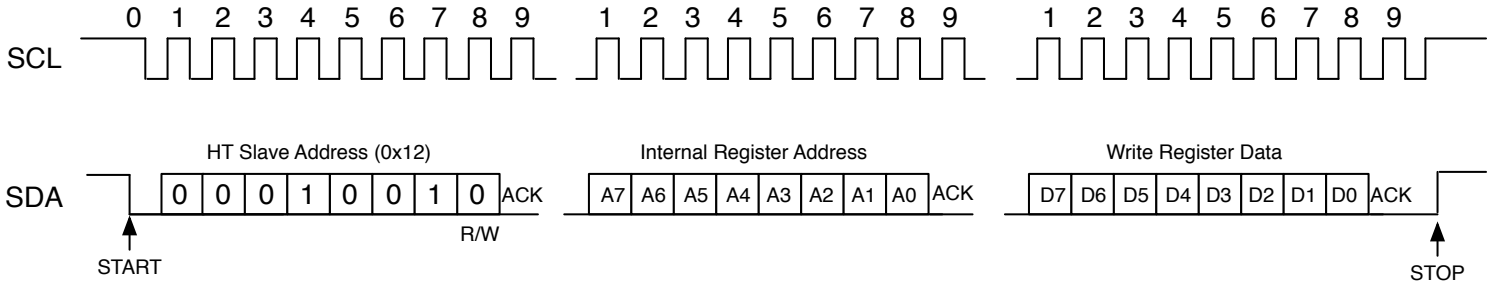


Figure 1 – I2C Write Procedure

I2C Read

1) Initiate a START condition to the I2C bus.
2) Write the HT I2C Slave address byte (0x12 by default). The 8th bit of the address byte is the R/W bit, set low.
3) Wait for an acknowledge (ACK), then write to the control register address to be read.
4) Initiate a Repeated START condition to the I2C bus.
5) Write the HT I2C Slave address byte. The 8th bit of the address byte is the R/W bit, set high (0x13).
6) Wait for an acknowledge (ACK), then read data from the specified register.
7) Repeat the previous step until all the desired registers are read.
8) Initiate a STOP condition to the bus.

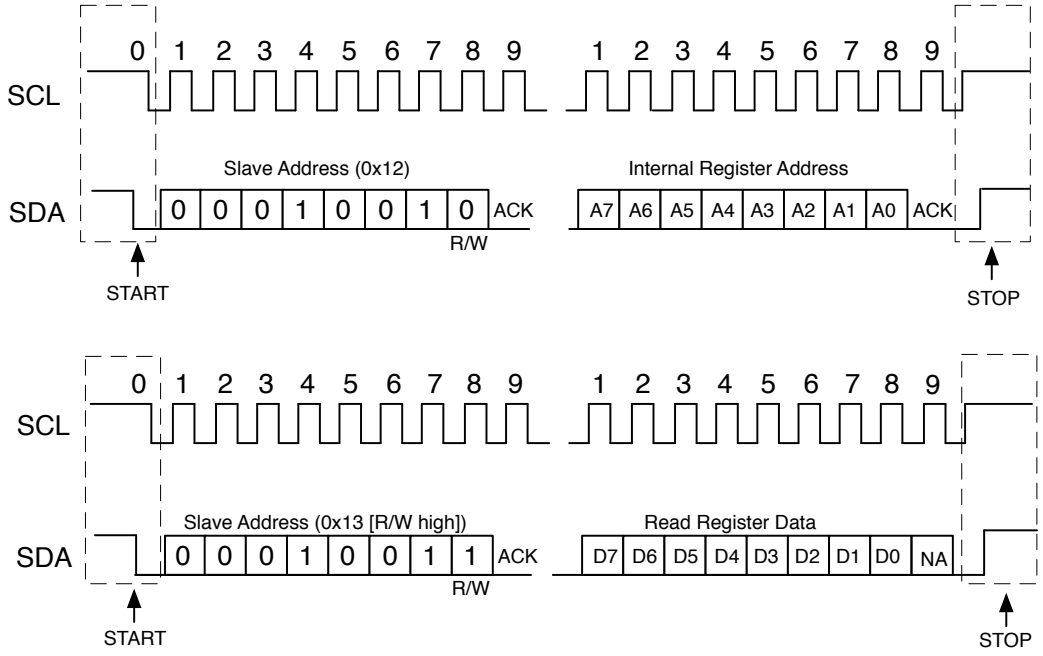
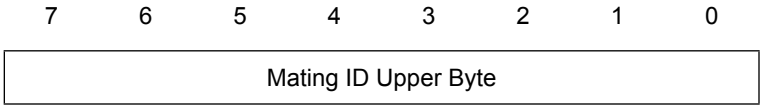


Figure 2 – I2C Read Procedure

4.2 REGISTER DESCRIPTION

A description of the HT control registers available for configuration are outlined below. All defaults are 0 unless otherwise specified.

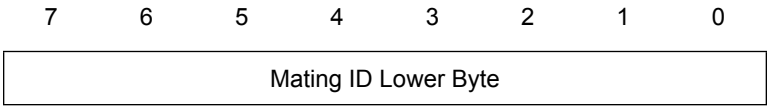
Mating ID Upper Byte (Address: 0x00)
Size: 8 bit
Access: R/W



Function:

Bit 7..0 – Mating ID – Upper Byte (Master/Slave)**:**
Manually Configure the Lower Byte of the Mating ID. In order for the Master and Slave modules to establish a connection, the Mating IDs on both must be identical.

Mating ID Lower Byte (Address: 0x01)
Size: 8 bit
Access: R/W



Function:

Bit 7..0 – Mating ID – Lower Byte (Master/Slave)**:**
Manually Configure the Lower Byte of the Mating ID. In order for the Master and Slave modules to establish a connection, the Mating IDs on both must be identical.

RF Configuration (Address: 0x02)
Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	Max RX Nodes		Mate Mode		Number of Slaves	

		Bit 5..4 – Max Nodes		Bit 3..2 – Mating Mode		Bit 1..0 - Number of Slaves	
7	6	5	4	3	2	1	0
-	-	1 Rx Node		RF Mating – Random ID		1 Rx Node	
		0	**0**	**0**	**0**	**0**	**0**
		2 Rx Nodes		RF Mating – Static ID		2 Rx Nodes	
		0	**1**	**1**	**0**	**0**	**1**
		3 Rx Nodes		Static ID		3 Rx Nodes	
		1	**0**	**x**	**1**	**1**	**0**
		4 Rx Nodes				4 Rx Nodes	
		1	**1**			**1**	**1**

Function:

Bit 1..0 – Number of Slaves (Master Only)**:**
The number of RX nodes the TX will search for upon power up. If the number of unbonded RX nodes in the area is higher than the value set in "Number of Slaves", the TX will bond to the first ones it sees until the number is reached, ignoring the remainder.

Bit 3..2 – Mating Mode (Master/Slave):
Specifies if the TX/RX will acquire it's Mating ID automatically through the RF Mating process, or by manually by configuring matching Static IDs in the "Mating ID" control registers. RF Mating can be configured to automatically generate a new Random 16-bit Mating ID when initiated (0,0), or acquire a new slave with the existing Mating ID currently programmed in the transmitter (1,0)

Bit 5..4 – Max Nodes (Master Only):
Max Nodes is used during RF Mating Mode. This setting is used by the TX node to determine the maximum number of RX devices to attempt to RF Mate with. Once RF Mating has been completed, the number of Slaves that the Master has successfully Mated with re-defines the new overall system topology and becomes the new value of "Number of Slaves" for normal operation.

Buffer Size (Address: 0x03)
Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	Buffer Size					

Function:

Buffer Size (Master Only)**:**
This register defins the size of the Audio Buffer. A larger audio buffer allows more time for packet retransmissions, but increases the latancy between the TX and RX nodes.

Latency = 6.248 ms + (1.33 ms * Buffer Size)
Valid range is 6 to 42 (0x2A). Default is 10 (0xA) = 20 ms

The 6.248 ms fixed latency is broken up as follows:

5.330 ms = Audio Compression + Audio Decompression
0.918 ms = Packetization + Framing

Bond Status (Address: 0x04)
Size: 8 bit
Access: R

7	6	5	4	3	2	1	0
S3 Bond		S2 Bond		S1 Bond		S0 Bond	
Bond	-						

Bit 5..4 – Slot3 Bond Stat		Bit 5..4 – Slot2 Bond Stat		Bit 3..2 – Slot1 Bond Stat		Bit 3..2 – Slot0 Bond Stat	
7	6	5	4	3	2	1	0
Nothing Bonded		Nothing Bonded		Nothing Bonded		Nothing Bonded	
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**
Left Channel Audio		Left Channel Audio		Left Channel Audio		Left Channel Audio	
0	**1**	**0**	**1**	**1**	**0**	**0**	**1**
Right Channel Audio		Right Channel Audio		Right Channel Audio		Right Channel Audio	
1	**0**	**1**	**0**	**x**	**1**	**1**	**0**
Stereo Audio		Stereo Audio		Stereo Audio		Stereo Audio	
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Function:

Bond Status (Master/Slave):
The Bond Status register can be read at any time to determine the current connection status of each node in the system. On the Master, 2 bits are allocated for each of the 4 possible Slave connection slots which can be read to determine whether or not there is a connection on a specific slot, and the properties of that connection (stereo, left,right). On the Slave side, the bond state is reported on bit 7 of the Bond Status control register.

Bit 7- Slave Bond Stat.

7	6	5	4	3	2	1	0
Bonded		-		-		-	
1	-						
Unbonded		-		-		-	
0	-						

General Config 0 (Address: 0x06)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	Stby Mute	Stby Disable	Sleep Disable	Mute Invert	Int	-

Function:

Bit 0 – Reserved
Bit 1 – Interrupt Enable (Master/Slave):
If this bit is set then squeak will generate a GPIO interrupt to indicate new data from the RF has been received. If this bit is clear then the IO pin is left unused. RF mating must be disabled to use this feature.
Bit 2 – Mute Invert (Slave Only):
If this bit is clear then the Mute/AmpDisable pin (Pin 17) will be an active low output. If this bit is set then the Mute/AmpDisable pin will be an active high output.
Bit 3 – Mute Invert (Slave Only):
On the Slave this feature that will de-assert the Mute/AmpDisable pin after a bond is lost (Reg 0x08) and then put the Slave to sleep (Reg 0x09).
Bit 4 – Audio Level Sleep Disable (Master Only):
If this bit is clear then sleep mode is enabled, if this bit is set then sleep mode is disabled. This feature will put the system to sleep when no audio is present for an amount of time set in the Audio Level Attack Time register (Reg 0x16 and 0x17). The threshold for detecting audio presence is set in the Audio Level Threshold 0 register (Reg 0x12 and 0x13).
Bit 5 – Audio Sleep Mute Only (Master Only):
If this bit is clear then the audio level sleep feature will sleep the system when the timeout is reached. If this bit is set then the system will remain bonded when the audio level sleep timeout is reached and the slave will be muted.
Bit 6 – Reserved
Bit 7 – Reserved

Mute/Amp Disable Time Config (Address: 0x08)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Mute Configuration							

Bit 7..0 – Mute/Amp Disable

Function:

Mute/Amp Disable (Slave Only)**:**

This is used to configure the delay after a bond is lost before the Mute/AmpDisable pin is asserted. Writing 0 will disable this feature. This value must be set lower than the Sleep time in Register 0x09 for proper operation.
Time = Mute Time * 1 second. Default = 0 (disabled).

Sleep Time Config (Address: 0x09)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Sleep Time Configuration							

Bit 7..0 – Sleep Time Config

Function:

Sleep Time Config (Slave Only)**:**

This is used to configure the time until the module enters sleep mode after no bond has been established. Writing 0 will disable this feature.
Time = Sleep Time * 1 second. Default = 0 (disabled).

RF Mating Timeout (Address: 0x0A)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
RF Mating Timeout							

Bit 7..0 – RF Mating Timeout

Function:

RF Mating Timeout (Master Only)**:**

This is used to configure the timeout for the RF Mating algorithm.
Time = RF Mating Timeout * 1 second. Default = 60. Note: 0 is invalid and will restore value to default.

Audio Config (Address: 0x0E)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	-	Move Buttons	Volume Mode		Audio Mode	

			Bit 4- Move Buttons	Bit 3..2 - Volume Mode		Bit 1..0 - Audio Mode	
7	6	5	4	3	2	1	0
-			Default	Global Mode		Stereo Audio	
			0	0	0	0	0
-			Modified	Local Mode		Left Channel Audio	
			1	1	0	0	1
						Right Channel Audio	
						1	0

Function:

Bit 1..0 – Audio Mode (Slave Only)**:**
Can be used to configure each slave to output two channel stereo, Left Channel only, or Right channel only. When set to Left/Right Channel only, both Left and Right channels will output the channel of audio specified in "Audio Mode"

Bit 3..2 – Volume Mode (Slave Only)**:**
Configures the Volume behavior used by each Slave.

Global Volume Mode - An absolute system wide volume is stored by the master. On bond up the master sends the current system volume to the newly bonded slave. A change on the master is sent to all slaves and a change from a slave is sent to the master where it is distributed to all other slaves.

Local Volume Mode - Each slave stores it's own absolute volume. It does not send changes across the link and ignores any incoming volume changes from the system.

Bit 3..2 – Move Volume Buttons (Slave Only)**:**
If this bit is clear then the volume buttons are in the default locations; Vol- = pin 18, Vol+ = pin 20. If this bit is set then the volume buttons replace the I2C Int and Mute Button; Vol- = PC4 (pin 14), Vol+ = PC5 (pin 15). This will allow volume control for the standard digital module. (currently this feature is not functional)

Left Channel Audio Volume (Address: 0x10)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Mute	DAC Attenuation						

Function:

Bit 6..0 – DAC Attenuation (Master/Slave)**:**
Attenuation setting written to the DAC. Valid range is 0 to 70. Max volume = 0 (0dB of attenuation); Min volume = 70 (70dB of attenuation). On the Slave the Volume Mode must be set to Global (0) in order for the volume register on the Master to operate.

Bit 6..0 – Mute (Master/Slave)**:**
Set this bit to mute the DAC.

Right Channel Audio Volume (Address: 0x11)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Mute	DAC Attenuation						

Function:

Bit 6..0 – DAC Attenuation (Master/Slave)**:**
Attenuation setting written to the DAC. Valid range is 0 to 70. Max volume = 0 (0dB of attenuation); Min volume = 70 (70dB of attenuation). On the Slave the Volume Mode must be set to Global (0) in order for the volume register on the Master to operate.

Bit 6..0 – Mute (Master/Slave)**:**
Set this bit to mute the DAC.

Audio Level Threshold 0 – Lower Byte (Address: 0x12)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Audio Level Thresh0 - Lower Byte							

Bit 7..0 - Audio Level Threshold 0 - Lower Byte

Audio Level Threshold 0 – Upper Byte (Address: 0x13)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Audio Level Thresh0 - Upper Byte							

Bit 7..0 – Audio Level Threshold 0 - Upper Byte

Function:

Audio Level Threshold (Master Only)**:**
This threshold is used for the audio level sleep feature When the Audio Level Standby is enabled, this is the threshold level that will trigger the TX to awake from sleep and begin behaving normally. and Default = 15 (0xF)

Audio Level Attack Time 0 – Lower Byte (Address: 0x16)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Audio Level Thresh0 - Upper Byte							

Bit 7..0 – Audio Level Threshold 0 - Upper Byte

Function:

Audio Level Threshold (Master Only)**:**

This threshold is used for the audio level sleep feature When the Audio Level Standby is enabled, this is the threshold level that will trigger the TX to awake from sleep and begin behaving normally. and Default = 15 (0xF)

Audio Level Attack Time 0 – Upper Byte (Address: 0x17)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Audio Level Thresh0 - Upper Byte							

Bit 7..0 – Audio Level Threshold 0 - Upper Byte

Function:

Audio Level Threshold (Master Only)**:**

This threshold is used for the audio level sleep feature When the Audio Level Standby is enabled, this is the threshold level that will trigger the TX to awake from sleep and begin behaving normally. and Default = 15 (0xF)

Command 0 (Address: 0x1E)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	Audio Standby	Add Node	RF Mate	Clear Data	StdBy	Reset

Function:

Bit 0 – Reset (Master/Slave):
Setting this bit will trigger a hard reset of the local device

Bit 1 – Standby (Master/Slave):
Set this bit to put the device into a standby state. Clear this bit to bring the device back out of standby. While in standby the I2C bus is active in standby mode. Any changes made to registers during standby mode will be implemented on exiting standby with the exception of the Command0 register, where Reset and Standby will be executed.

Bit 2 – Clear Data (Master/Slave):
Setting this bit will clear all stored register data and reset it to default values. Clearing data will be followed by a reset of the unit.

Bit 3 – RF Mate (Master Only):
Setting this bit will trigger a RFmate operation as described in section 0900. The number of slave connections desired should be set up in the RF Config register before initiating a RFmate operation. Clear this bit cancel the RFmate operation.

Bit 4 – Add Single Node (Master Only):
Setting this bit will trigger a RFmate add single node operation as described in section 0900

Bit 5 – Audio Sleep Mute Only (Master Only):
This is an indicator bit only. If this bit is set then the system has entered standby due to an absence of audio for the time indicated in Audio Level Threshold 0 (reg 0x12 and 0x13). Note that to save code space this bit is not refreshed if overwritten. Actions in this register will trigger an exit from the standby state.

Bit 6 – Reserved

Bit 7 – Reserved

4.3 STANDARD BI-DIRECTIONAL DATA LINK

The Bi-directional Data Link interface will allow for the transmission of non-audio user data across the wireless link from a Tx to an Rx, or from an Rx to a Tx. The procedure outlined below demonstrates the how to send information from a Tx module to an Rx module via the I2C interface.
Procedure:

On the Tx:
Connect to the I2C pins on the TX.

1. Write to Outgoing Data Channel Data Register (Address 0x8C)
-This is the data we want to send over the link (1 byte in this case, but can be as high as 46 bytes). We will write a value of 0xAA to this register that will sent to the other side

2. Write to Outgoing Data Channel Control0 Register (Address 0x8B)
-Write a value of 0x11. This will address our data to be sent to the slave bonded on Slot0. This will also set the New Data bit which will trigger the new data to be sent. When the transfer is complete, the ACK bit will be set in this register.

On the Rx:
Connect to the I2C pins on the Rx.

1. Read from Incoming Data Channel Data Register(Address 0x8E). Should get a value of 0xAA that was sent from the Tx.

TX Standard Outgoing Data Channel

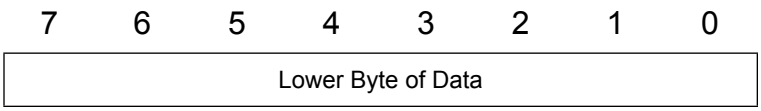
Standard Outgoing Data Control (Address: 0x8B)
Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
S3	S2	S1	S0	# of Resends		ACK	NEW

Function:

Bit 0 – New Data Bit
Set this bit to indicate that new data is ready to be sent. This bit is cleared to indicate a finished transfer
Bit 1 - ACK
This bit is set when the transfer is complete if an ACK was received from all addressed slaves. If this bit is clear when the transfer finished then one or more of the addressed slaves did not report an ACK.
Bit 2..3 – Number of resends
This indicates the number of times that squeak will try to resend the data
Bit 4 – S0
Set this bit to address the slave connected on slot 0
Bit 5 – S1
Set this bit to address the slave connected on slot 1
Bit 6 – S2
Set this bit to address the slave connected on slot 2
Bit 7 – S3
Set this bit to address the slave connected on slot 3

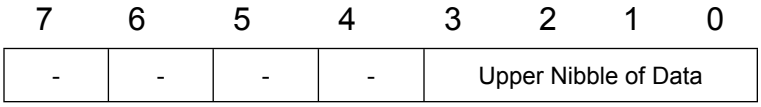
Standard Outgoing Data Lower Byte (Address: 0x8C)
Size: 8 bit
Access: R/W



Function:

Bit 0..7 – Lower byte of data
This is the lower byte, bits 0..7, of the data to be sent

Standard Outgoing Data Lower Byte (Address: 0x8D)
Size: 8 bit
Access: R/W

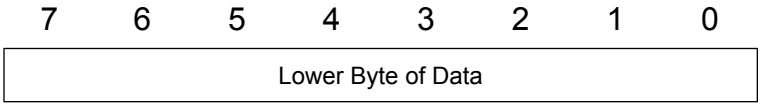


Function:

Bit 3..0 – Upper Nibble of data
This is the upper nibble, bits 8..11, of the data to be sent

TX Standard Incoming Data Channel

Slot0 Standard Incoming Data Lower Byte (Address: 0x8E)
Size: 8 bit
Access: R

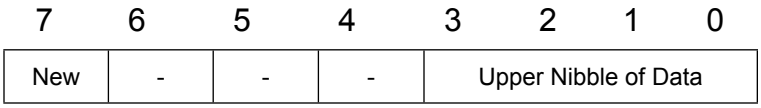


Function:

Bit 7..0 – Lower byte of data
This is the lower byte, bits 0..7, of the data to be sent

Slot0 Standard Incoming Data Upper Byte (Address: 0x8F)

Size: 8 bit
Access: R

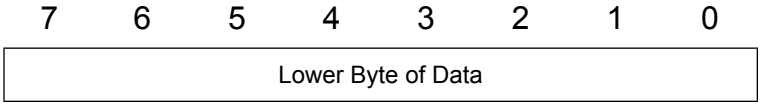


Function:

Bit 3..0 – Upper Nibble of data
This is the upper nibble, bits 8..11, of the data to be sent
Bit 7 – New Data Bit
This bit is set when new data is received from slot 0. This bit is cleared when read.

Slot1 Standard Incoming Data Lower Byte (Address: 0x90)

Size: 8 bit
Access: R

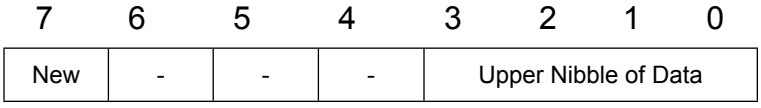


Function:

Bit 0..7 – Lower byte of data
This is the lower byte, bits 0..7, of the data to be sent

Slot1 Standard Incoming Data Upper Byte (Address: 0x91)

Size: 8 bit
Access: R



Function:

Bit 3..0 – Upper Nibble of data
This is the upper nibble, bits 8..11, of the data to be sent
Bit 7 – New Data Bit
This bit is set by when new data is received from slot 0. This bit is cleared when read.

Slot2 Standard Incoming Data Lower Byte (Address: 0x92)

Size: 8 bit
Access: R

7	6	5	4	3	2	1	0
Lower Byte of Data							

Function:

Bit 0..7 – Lower byte of data
This is the lower byte, bits 0..7, of the data to be sent

Slot2 Standard Incoming Data Upper Byte (Address: 0x93)

Size: 8 bit
Access: R

7	6	5	4	3	2	1	0
New	-	-	-	Upper Nibble of Data			

Function:

Bit 3..0 – Upper Nibble of data
This is the upper nibble, bits 8..11, of the data to be sent
Bit 7 – New Data Bit
This bit is set by when new data is received from slot 0. This bit is cleared when read

Slot3 Standard Incoming Data Lower Byte (Address: 0x94)

Size: 8 bit
Access: R

7	6	5	4	3	2	1	0
Lower Byte of Data							

Function:

Bit 0..7 – Lower byte of data
This is the lower byte, bits 0..7, of the data to be sent

Slot3 Standard Incoming Data Upper Byte (Address: 0x95)

Size: 8 bit
Access: R

7	6	5	4	3	2	1	0
New	-	-	-	Upper Nibble of Data			

Function:

Bit 3..0 – Upper Nibble of data
This is the upper nibble, bits 8..11, of the data to be sent
Bit 7 – New Data Bit
This bit is set by Squeak when new data is received from slot 0. This bit is cleared when read. In slave only mode Squeak will assert an IO pin when new data arrives.

RX Standard Outgoing Data Channel

Standard Outgoing Data Control (Address: 0x8B)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	-	-	# of Resends		ACK	NEW

Function:

Bit 0 – New Data Bit
Set this bit to indicate that new data is ready to be sent. This bit is cleared to indicate a finished transfer
Bit 1 - ACK
This bit is set when the transfer is complete if an ACK was received from all addressed slaves. If this bit is clear when the transfer finished then one or more of the addressed slaves did not report an ACK.
Bit 2..3 – Number of resends
This indicates the number of times the data will be resent in the event of an incomplete transmission.

Standard Outgoing Data Lower Byte (Address: 0x8C)

Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
Lower Byte of Data							

Function:

Bit 0..7 – Lower byte of data
This is the lower byte, bits 0..7, of the data to be sent

Standard Outgoing Data Upper Byte (Address: 0x8D)
Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	-	-	Upper Nibble of Data			

Function:

Bit 3..0 – Upper Nibble of data
This is the upper nibble, bits 8..11, of the data to be sent

RX Standard Incoming Data Channel

Standard Incoming Data Lower Byte (Address: 0x8E)
Size: 8 bit
Access: R

7	6	5	4	3	2	1	0
Lower Byte of Data							

Function:

Bit 0..7 – Lower byte of data
This is the lower byte, bits 0..7, of the data to be sent

Standard Incoming Data Upper Byte (Address: 0x8F)
Size: 8 bit
Access: R

7	6	5	4	3	2	1	0
New	-	-	-	Upper Nibble of Data			

Function:

Bit 3..0 – Upper Nibble of data
This is the upper nibble, bits 8..11, of the data to be sent
Bit 7 – New Data Bit
This bit is set when new data is received from slot 0. This bit is cleared when read.

4.4 EXTENDED BI-DIRECTIONAL DATA LINK

The Data link interface can operate in I2C slave mode to send and receive data from the external micro-controller. The link interface can also be configured to operate in I2C master mode to send data to the external micro-controller. There is a configurable interrupt pin that can be used to indicate that data has been received.

On the Tx:
Connect to the I2C pins on the TX.

1. Write to Outgoing Data Channel Control1 Register (Address 0x31)
-here we will set up the data size and message destination. writing a value of 0x01 will set a data size of 1 byte and pass the data through to be read over the I2C bus.

2. Write to Outgoing Data Channel Data Register (Address 0x32)
-This is the data we want to send over the link (1 byte in this case, but can be as high as 46 bytes). We will write a value of 0xAA to this register that will sent to the other side

3. Write to Outgoing Data Channel Control0 Register (Address 0x30)
-Write a value of 0x11. This will address our data to be sent to the slave bonded on Slot0. This will also set the New Data bit which will trigger the new data to be sent. When the transfer is complete, the ACK bit will be set in this register.

On the Rx:
Connect to the I2C pins on the Rx.

1. Read from Incoming Data Channel Data Register(Address 0x32). Should get a value of 0xAA that was sent from the Tx.

TX Extended Outgoing Data Channel

Outgoing Data Control 0 (Address: 0x30)
Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
S3	S2	S1	S0	# of Resends		ACK	NEW

Function:

Bit 0 – New Data Bit
Set this bit to indicate that new data is ready to be sent. This bit is cleared to indicate a finished transfer
Bit 1 - ACK
This bit is set when the transfer is complete if an ACK was received from all addressed slaves. If this bit is clear when the transfer finished then one or more of the addresseddressed slaves did not report an ACK.
Bit 2..3 – Number of resends
This indicates the number of times the data will be resent in the event of an incomplete transmission.
Bit 4 – S0
Set this bit to address the slave connected on slot 0
Bit 5 – S1
Set this bit to address the slave connected on slot 1
Bit 6 – S2
Set this bit to address the slave connected on slot 2
Bit 7 – S3
Set this bit to address the slave connected on slot 3

Outgoing Data Control 1 (Address: 0x31)
Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	MD	Data Size					

Function:

Bit 0..5 – Data Size
This indicates the size of the data to be sent across the link in bytes. Max = 46 bytes.

Bit 5 – MD (Message Destination)
This Bit determines the intended destination of the data sent across the link. If this bit is clear then the slave will pass the data though to the table to be read over the I2C bus. If this bit is set then the slave will route the received data to the attached audio device. The data in the buffer below will be sent as is to the audio device.

Outgoing Data Channel Data (Address: 0x32-0x5F)
Size: Up to 46 Bytes
Access: W

TX Extended Incoming Data Channel

Incoming Data Channel Control Slot0 (Address: 0x62)
Size: 8 bit
Access: W

7	6	5	4	3	2	1	0
-	-	Data Size					New

Function:

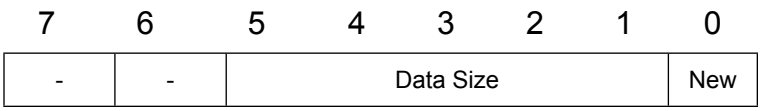
Bit 0 – New Data Bit
This bit is set when new data is received from the master. This bit is cleared when read.

Bit 5..1 – Data Size
Size of received data in Bytes

Incoming Data Channel Data Slot0 (Address: 0x64-6B)
Size: Up to 8 Bytes
Access: R

Incoming Data Channel Control Slot1 (Address: 0x6C)

Size: 8 bit
Access: R



Function:

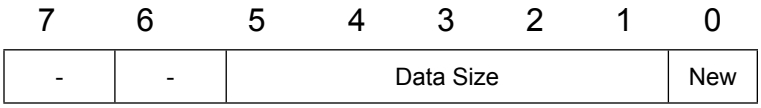
Bit 0 – New Data Bit
This bit is set when new data is received from the master. This bit is cleared when read.
Bit 5..1 – Data Size
Size of received data in Bytes

Incoming Data Channel Data Slot1 (Address: 0x6E-75)

Size: Up to 8 Bytes
Access: R

Incoming Data Channel Control Slot2 (Address: 0x76)

Size: 8 bit
Access: R



Function:

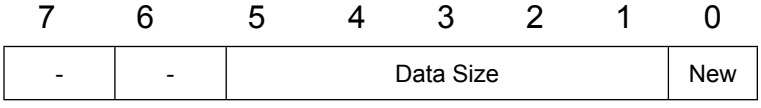
Bit 0 – New Data Bit
This bit is set when new data is received from the master. This bit is cleared when read.
Bit 5..1 – Data Size
Size of received data in Bytes

Incoming Data Channel Data Slot2 (Address: 0x78-7F)

Size: Up to 8 Bytes
Access: R

Incoming Data Channel Control Slot3 (Address: 0x80)

Size: 8 bit
Access: R



Function:

Bit 0 – New Data Bit
This bit is set when new data is received from the master. This bit is cleared when read.
Bit 5..1 – Data Size
Size of received data in Bytes

Incoming Data Channel Control Slot3 (Address: 0x82-0x89)
Size: 8 Bytes
Access: R

RX Extended Outgoing Data Channel

Outgoing Data Control 0 (Address: 0x62)
Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	-	-	# of Resends		ACK	New

Function:

Bit 0 – New Data Bit
Set this bit to indicate that new data is ready to be sent. This bit is cleared to indicate a finished transfer
Bit 1 - ACK
This bit is set when the transfer is complete if an ACK was received from all addressed slaves. If this bit is clear when the transfer finished then one or more of the addressed slaves did not report an ACK.
Bit 3..2 – Number of resends
This indicates the number of times to resend the data in event of an incomplete transmission.

Outgoing Data Control 1 (Address: 0x63)
Size: 8 bit
Access: R/W

7	6	5	4	3	2	1	0
-	-	-	-	-	Data Size		

Function:

Bit 0..2 – Data Size
This indicates the size of the data to be sent across the link in bytes.

Outgoing Data Channel Data (Address: 0x64-6B)
Size: Up to 8 Bytes
Access: W

RX Extended Incoming Data Channel

Incoming Data Channel Control (Address: 0x30)
Size: 8 bit
Access: R

7	6	5	4	3	2	1	0
-	Data Size						New

Function:

Bit 0 – New Data Bit
This bit is set when new data is received from the master. This bit is cleared when read.
Bit 6..1 – Data Size
Size of received data in Bytes

Incoming Data Channel Data (Address: 0x32-5F)
Size: Up to 46 Bytes
Access: R

5 PACKAGE DIMENSIONS

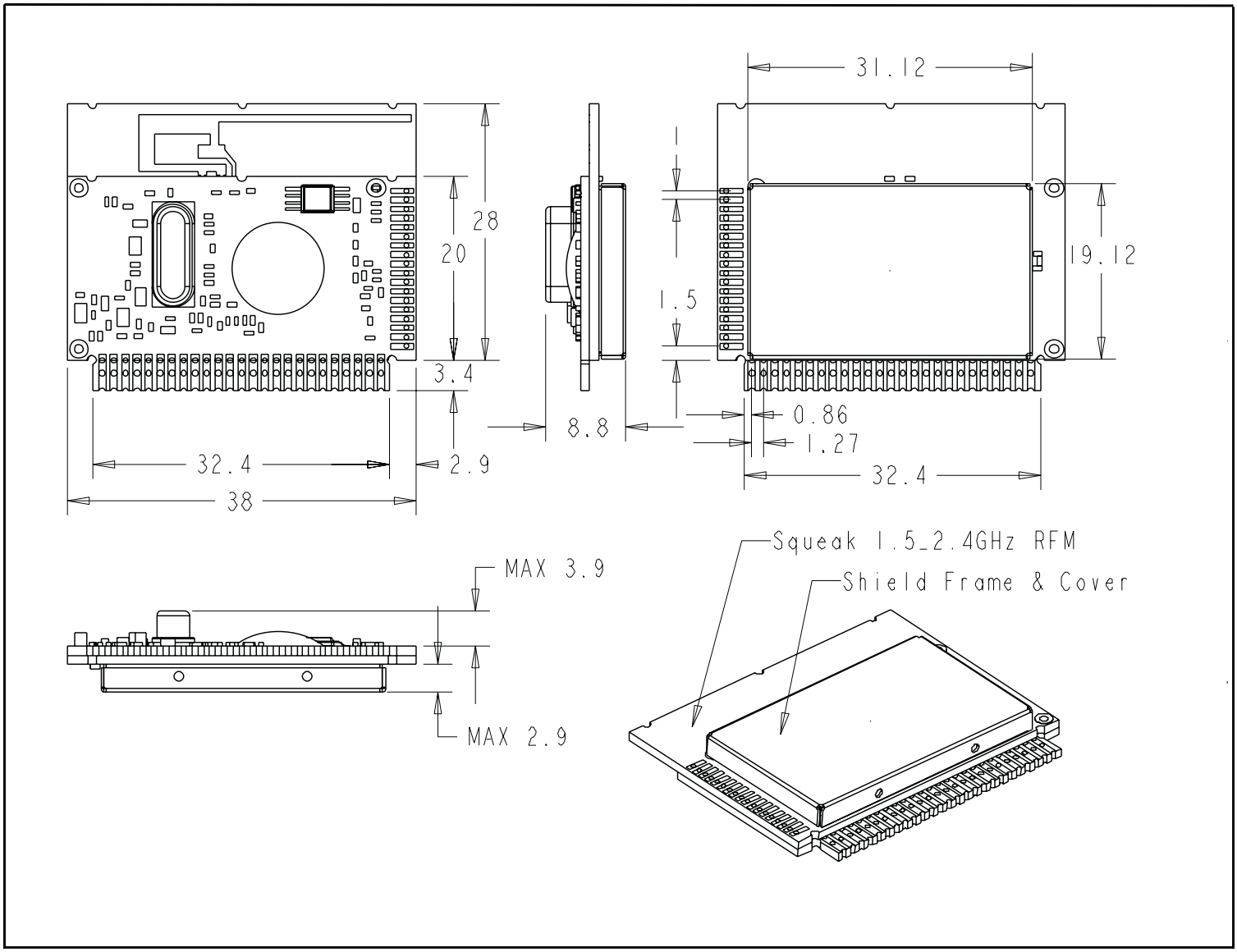


Figure 4 – Package Dimensions

6 MOUNTING METHODS

6.1 RIGHT ANGLE SLOT MOUNT

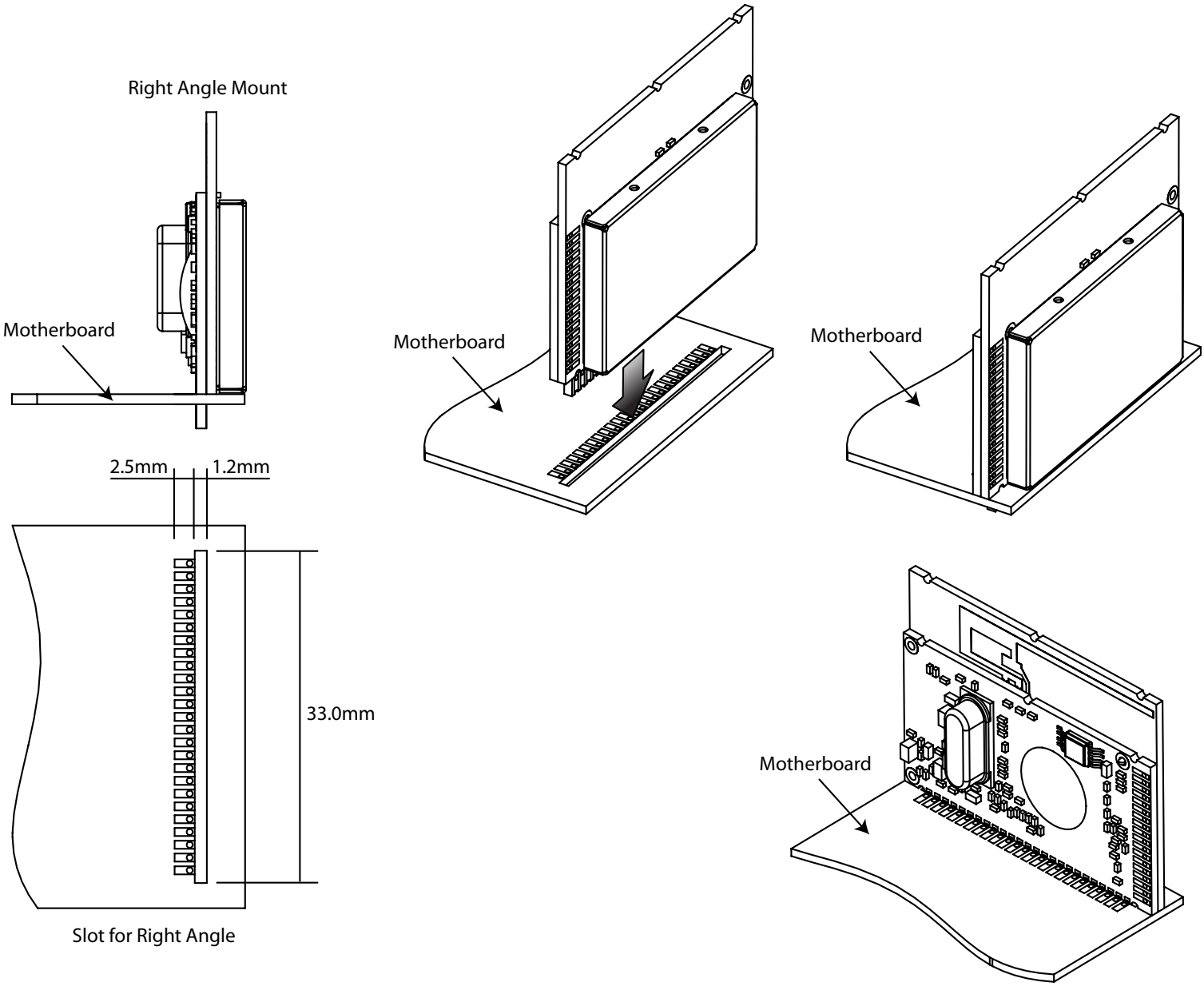


Figure 5 – Right Angle Slot Mount

6.2 EDGE MOUNT

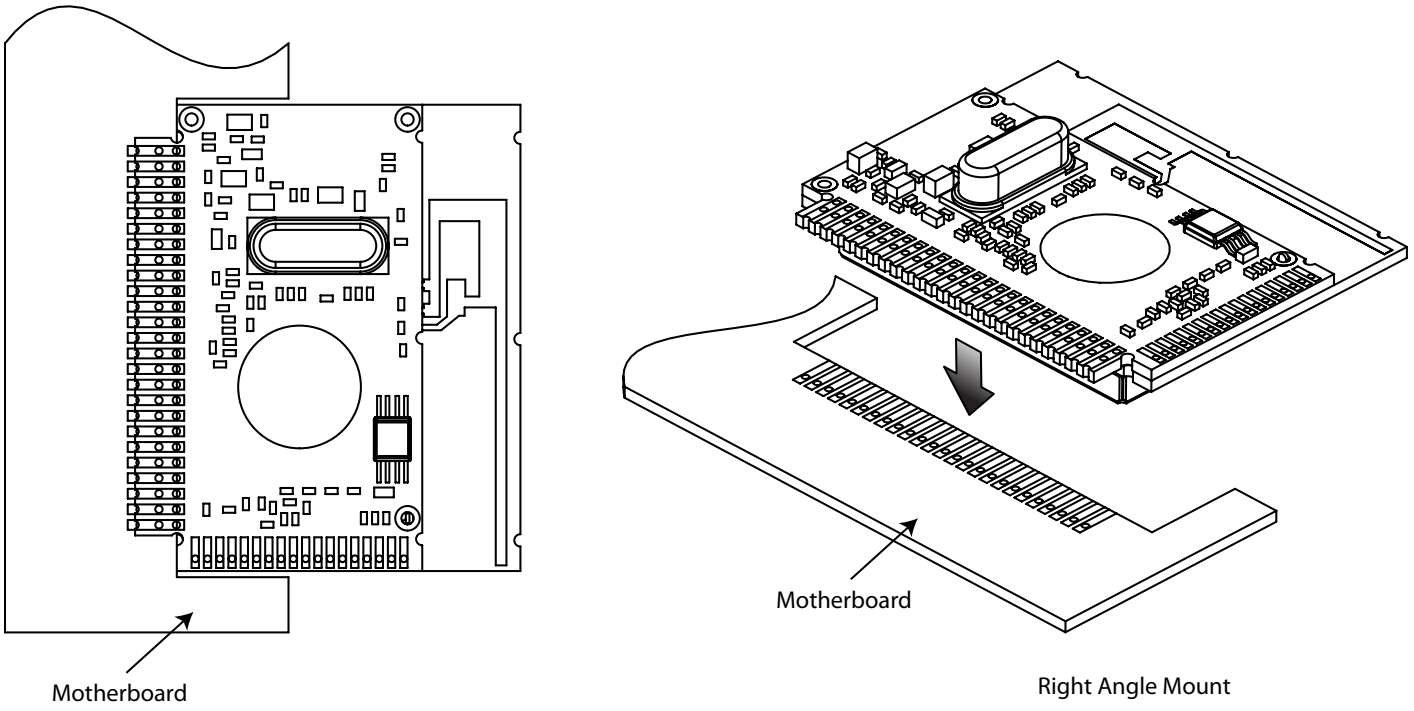


Figure 6 – Edge Mount

APPENDIX A: AUDIO CHARACTERISTIC CHARTS

The HT audio characteristics are shown in the following figures. All measurements were taken using WHAM2 Digital modules mounted on PB3 evaluation boards. Audio Precision SYS2722 with AES filter used in all cases unless otherwise stated.

Noise Floor

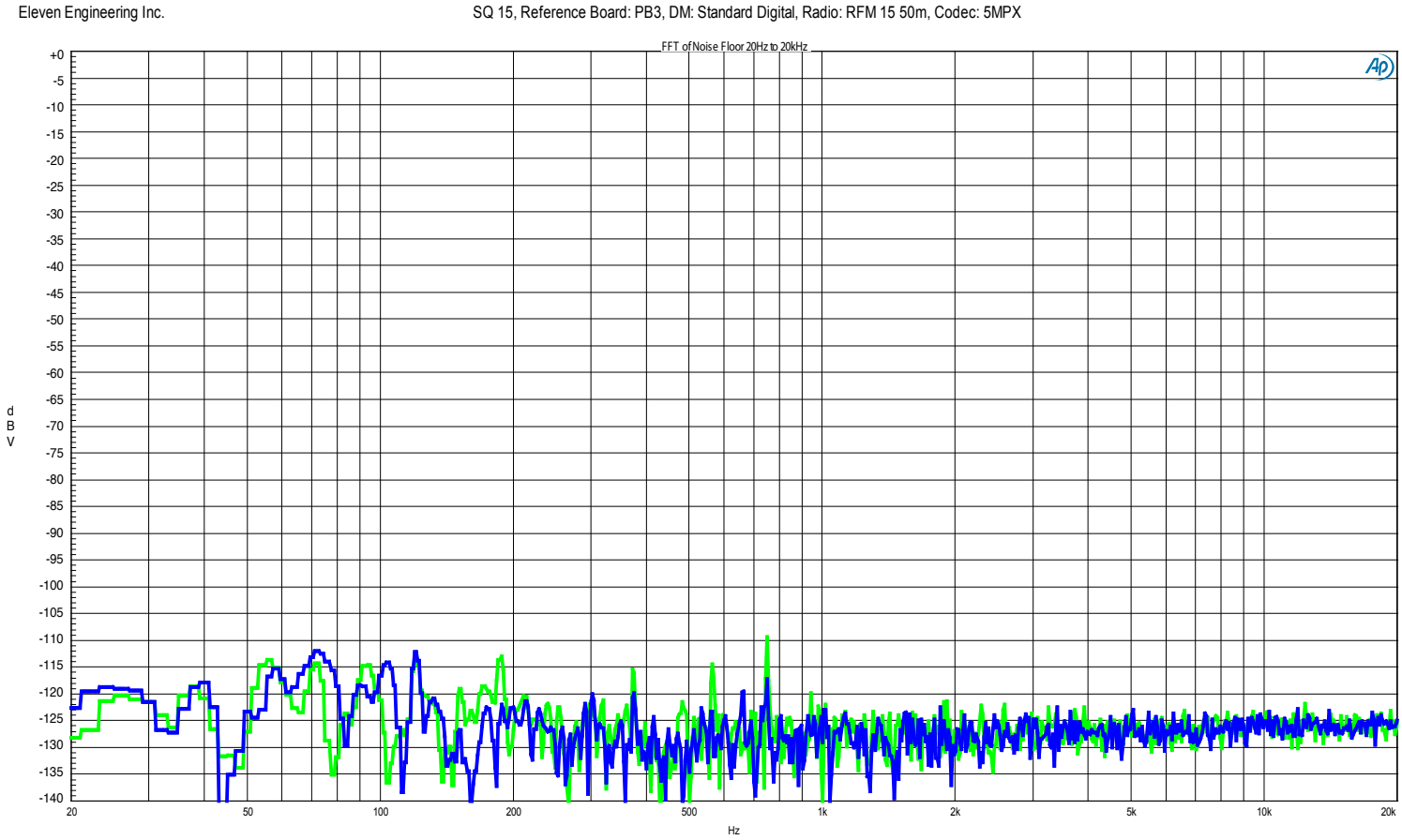


Figure 9 – FFT of Idle Tones (Noise Floor)

997 Hz Tone

Eleven Engineering Inc. SQ 15, Reference Board: PB3, DM: Standard Digital, Radio: RFM 15 50m, Codec: 5MPX

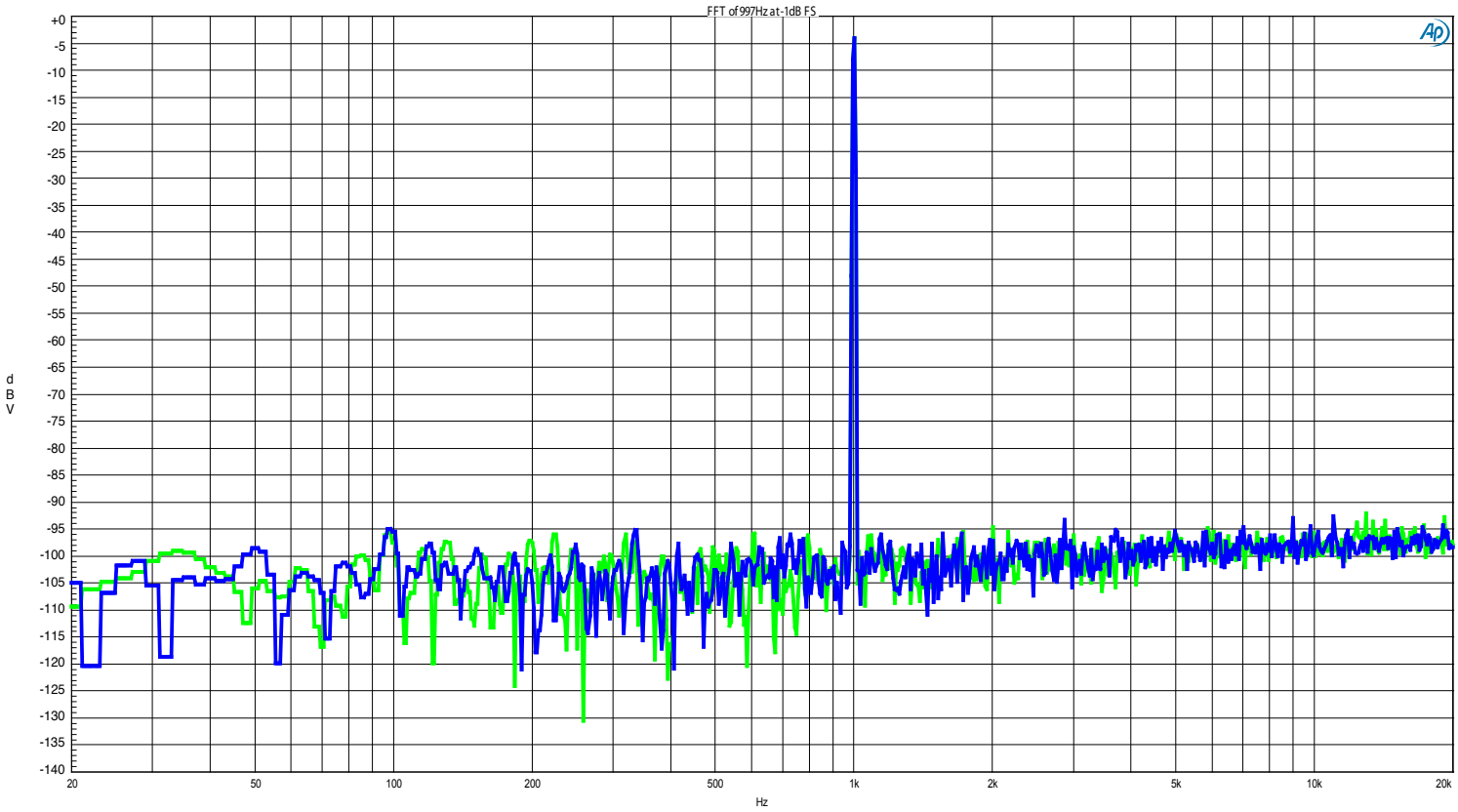


Figure 10 – FFT of 997 Hz at -1 dB FS

Frequency Response

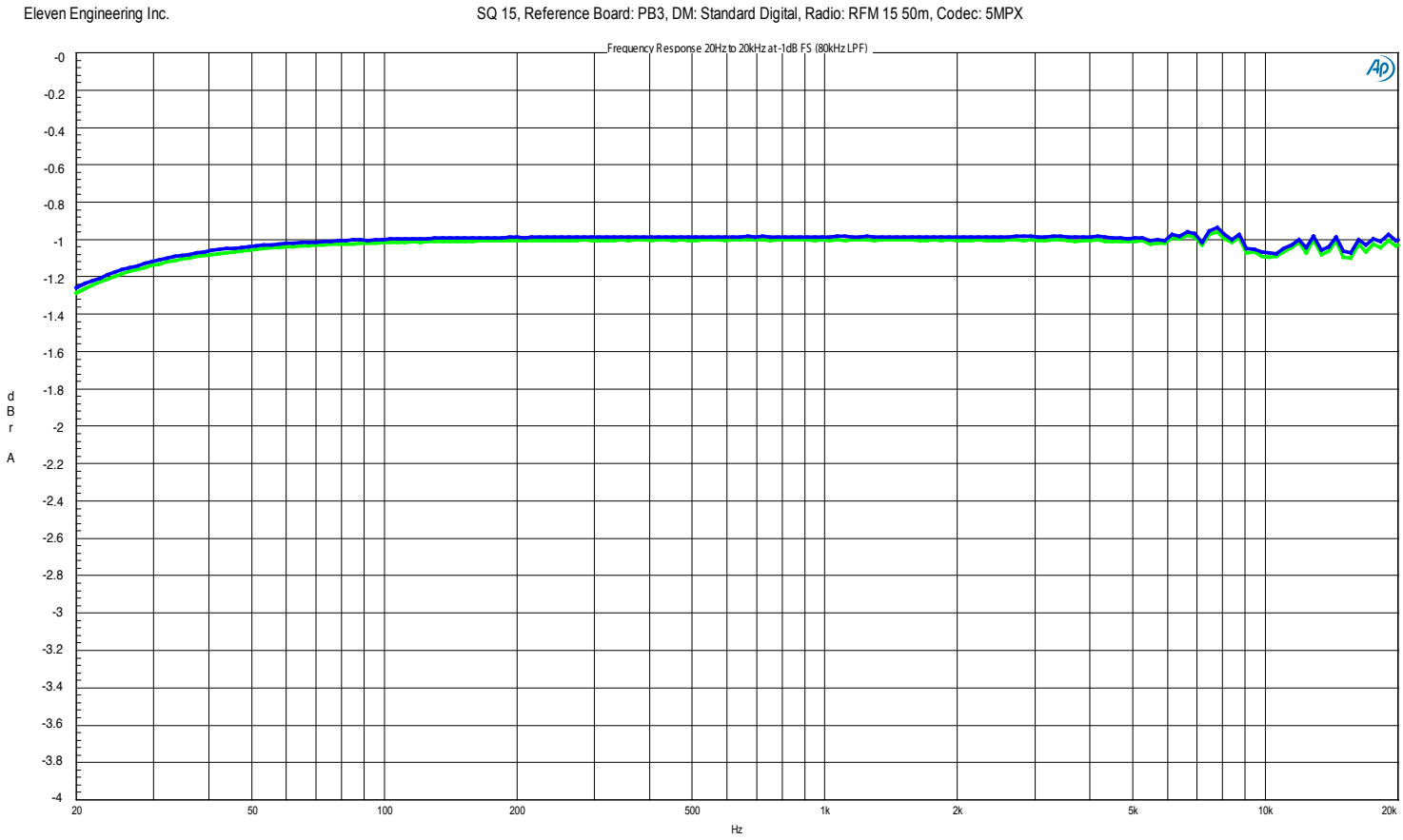


Figure 11 – Frequency Response at -1 dB FS

THD+N vs Frequency (HPX/ PB3)

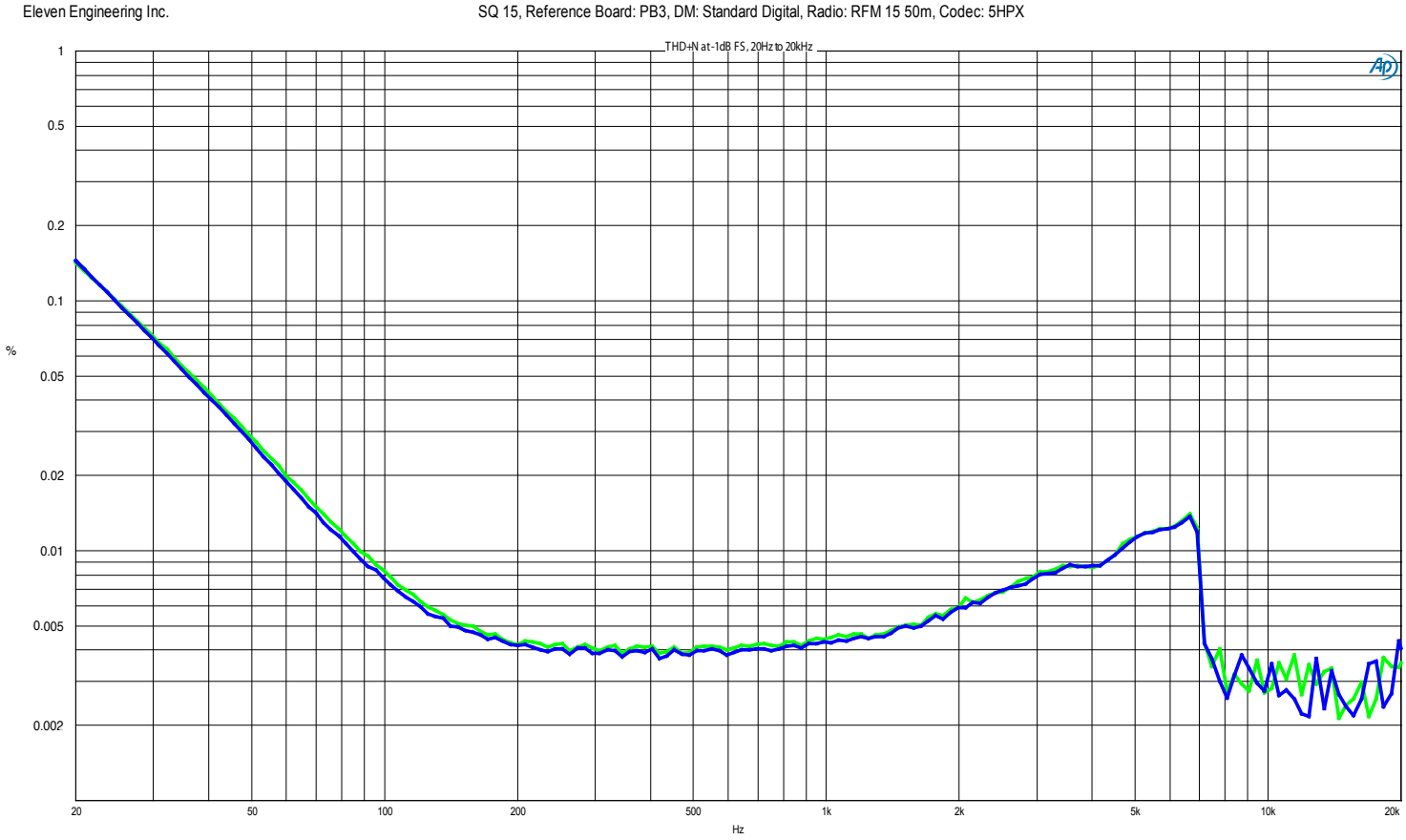


Figure 12 – THD+N vs. Frequency (HPX/PB3)*

***Notes:**
-Compressed signal tones over 10 KHz are stable when measured with an oscilloscope
-The THD+N curve shown above includes the contribution of the ADC and DAC used on the PB3 reference board along with the effects of the module itself.

Channel Isolation

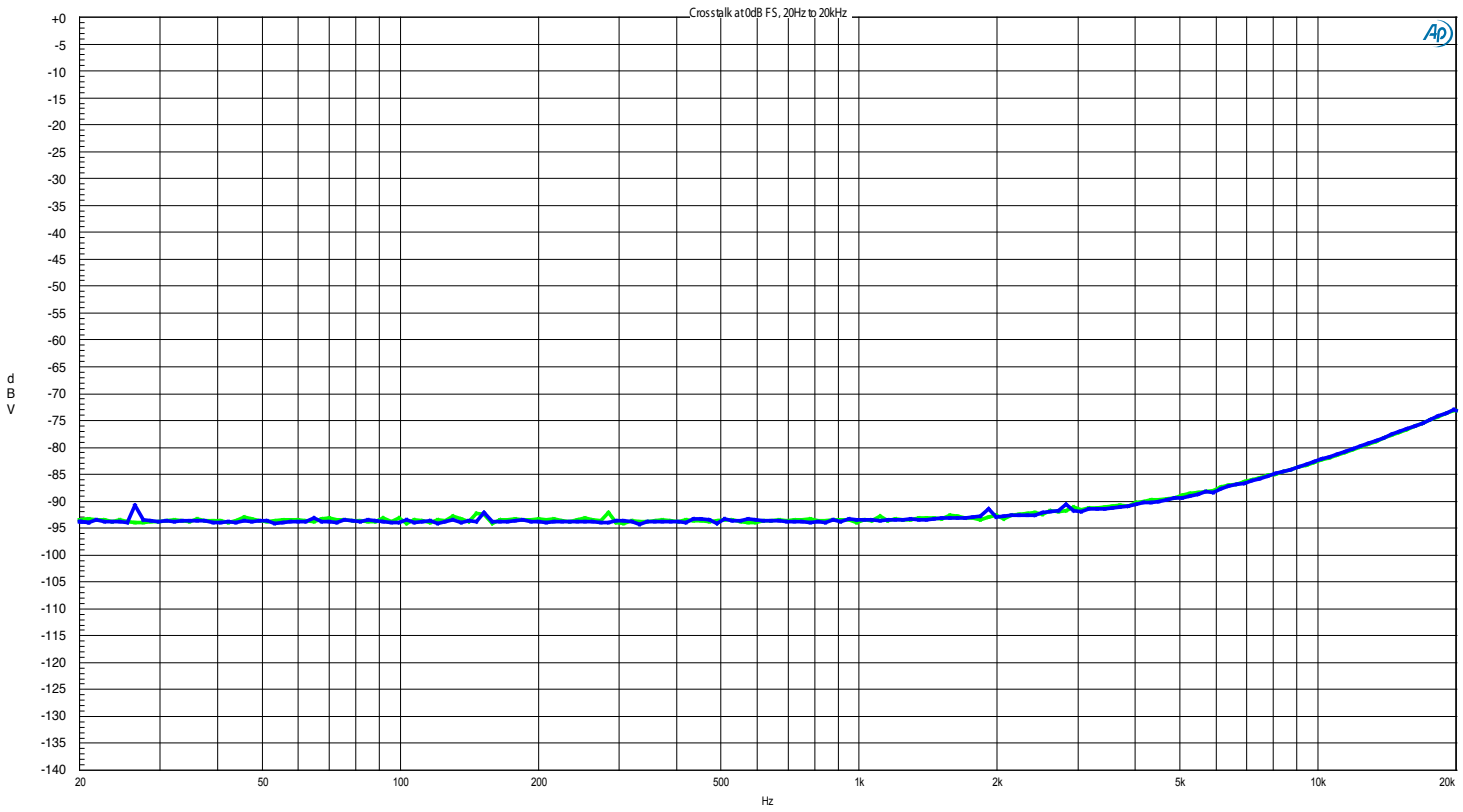


Figure 13 – Channel Isolation at 0 dB FS

APPENDIX B: CHANNEL TABLE

Channel #	Center Frequency (GHz)	Channel #	Center Frequency (GHz)
CENTER FREQUENCIES (CHANNEL TABLE)			
0	2.403328	19	2.442240
1	2.405376	20	2.444288
2	2.407424	21	2.446336
3	2.409472	22	2.448384
4	2.411520	23	2.450432
5	2.413568	24	2.452480
6	2.415616	25	2.454528
7	2.417664	26	2.456576
8	2.419712	27	2.458624
9	2.421760	28	2.460672
10	2.423808	29	2.462720
11	2.425856	30	2.464768
12	2.427904	31	2.466816
13	2.429952	32	2.468864
14	2.432000	33	2.470912
15	2.434048	34	2.472960
16	2.436096	35	2.475008
17	2.438144	36	2.477056
18	2.440192	37	2.479104

Table 8 – RF Center Frequencies

APPENDIX C: PB3 REFERENCE DESIGN SCHEMATICS

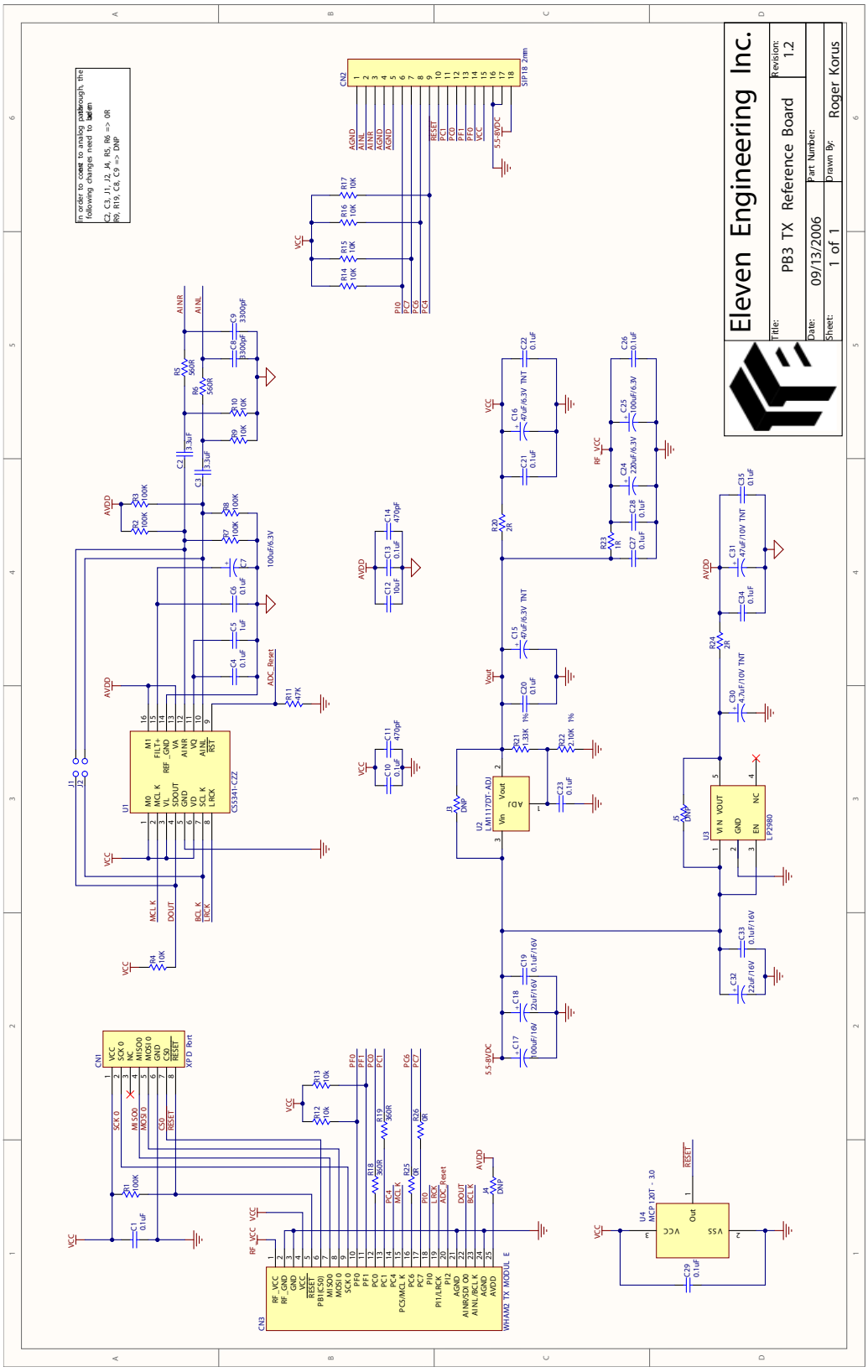


Figure 14 – PB3 Tx Reference Schematic

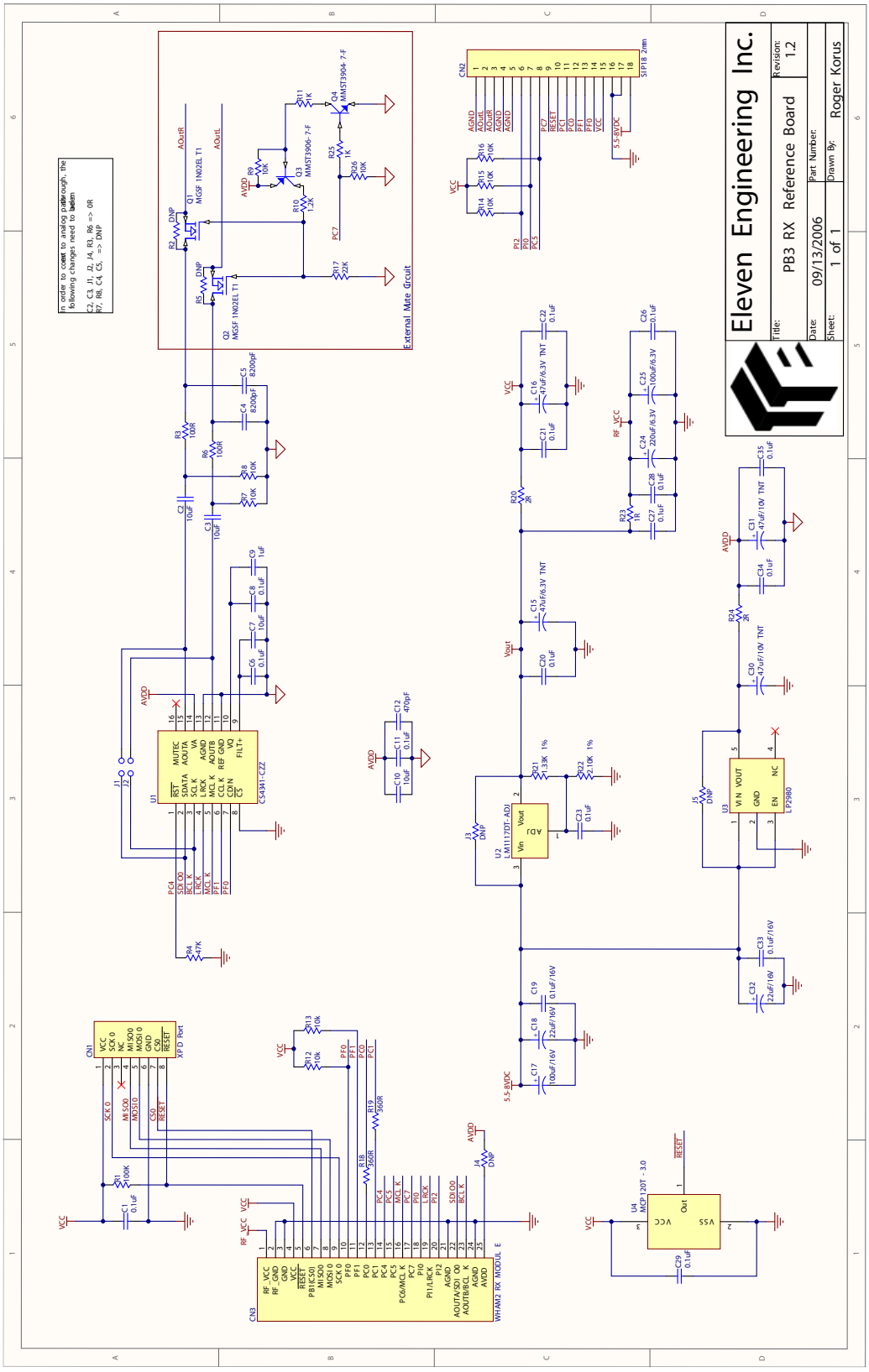


Figure 15 – PB3 Rx Reference Schematic