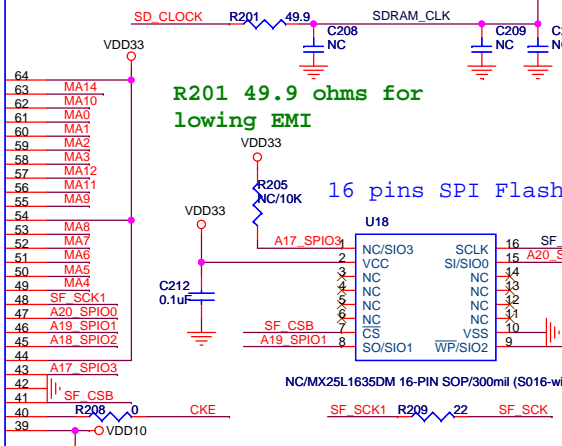
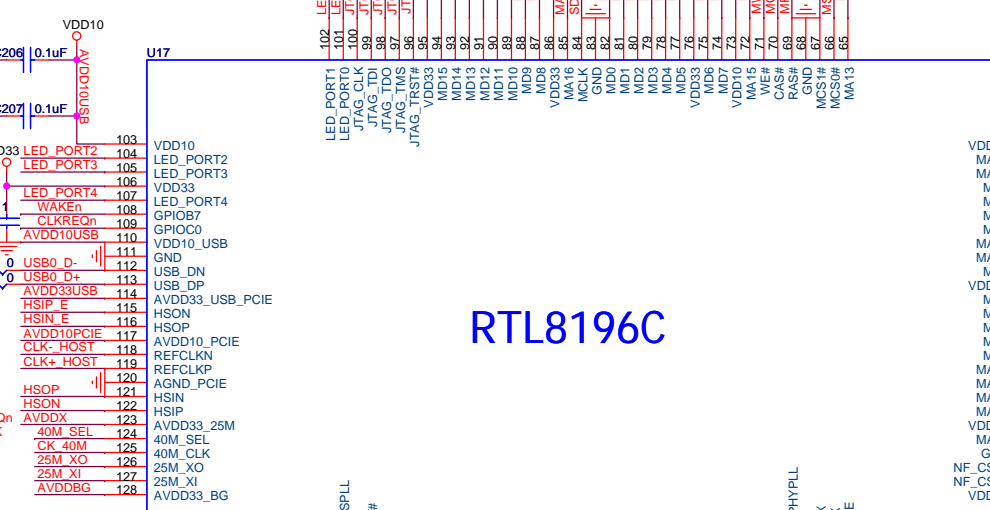
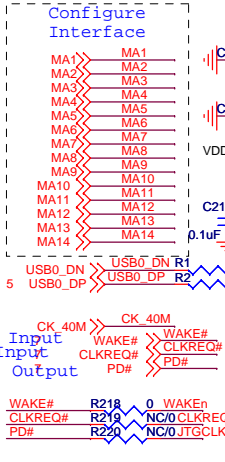
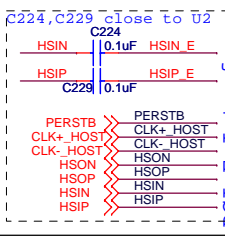
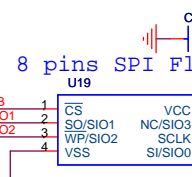
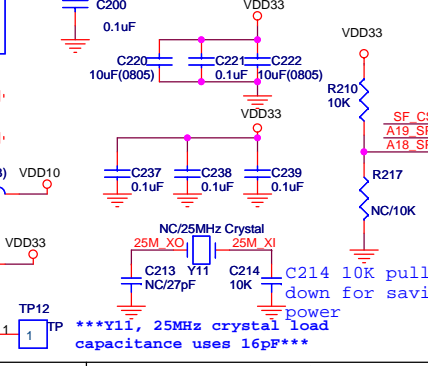
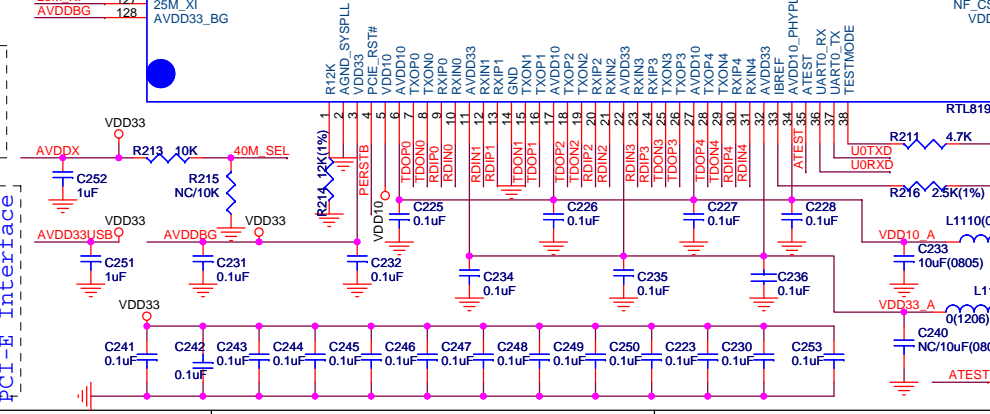
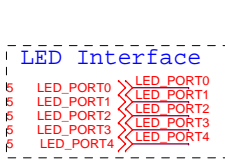


**Layout Guide:**  
Put termination near the RTL8196C Chip side

MWEB	R158	0	WEB
MCASB	R160	0	CASB
MRASB	R162	0	RASB
MSD_CSOB	R163	0	SD_CSOB
MD0	R164	0	D0
MD1	R165	0	D1
MD2	R166	0	D2
MD3	R167	0	D3
MD4	R168	0	D4
MD5	R171	0	D5
MD6	R176	0	D6
MD7	R177	0	D7
MD8	R178	0	D8
MD9	R179	0	D9
MD10	R180	0	D10
MD11	R181	0	D11
MD12	R182	0	D12
MD13	R183	0	D13
MD14	R184	0	D14
MD15	R185	0	D15
MA0	R186	0	A0
MA1	R188	0	A1
MA2	R189	0	A2
MA3	R190	0	A3
MA4	R191	0	A4
MA5	R193	0	A5
MA6	R195	0	A6
MA7	R194	0	A7
MA8	R195	0	A8
MA9	R196	0	A9
MA10	R197	0	A10
MA11	R198	0	A11
MA12	R199	0	A12
MA13	R200	0	A13
MA14	R202	0	A14
MA15	R203	0	A15
MA16	R204	0	A16



SPI Flash	Single I/O	Quad I/O
8 pins SPI	R210=10K	R212=NC
16 pins SPI	R205=10K	R205=NC
	R206=10K	R206=NC



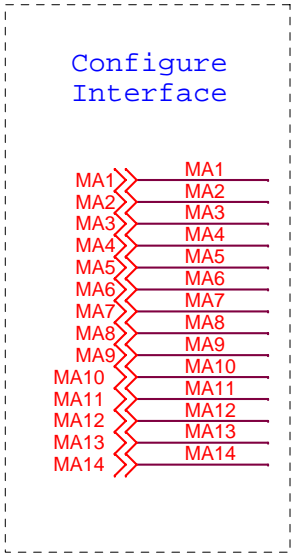
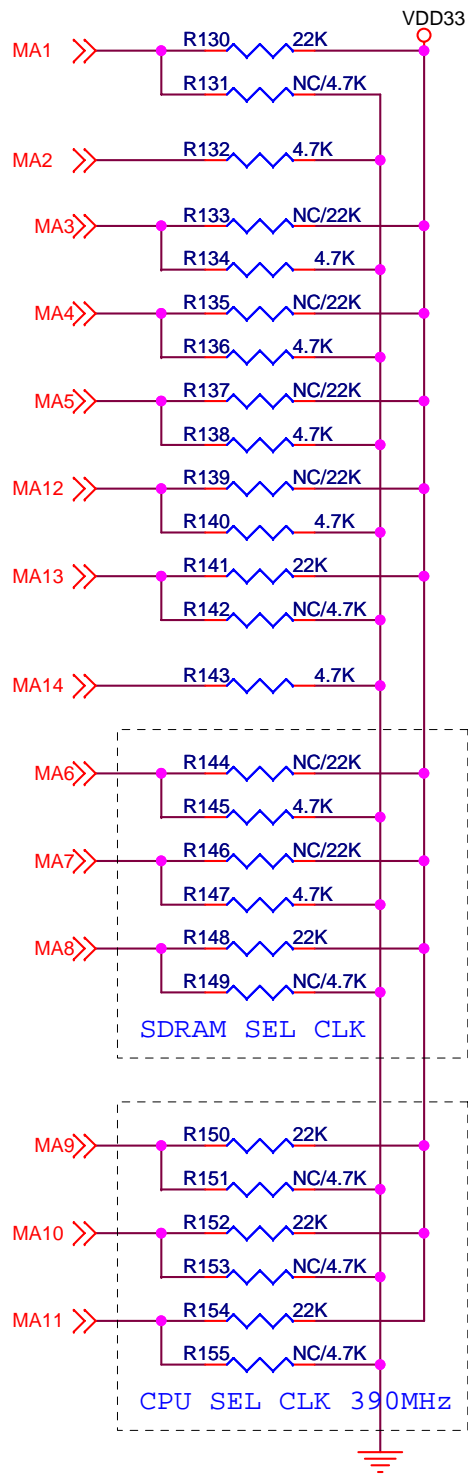
**ENCORE ELECTRONICS** Encore Electronics Inc.

Title: SOC/MEMORY Model: ENDB-XRL8196C

Size: Document Number: CustomSchematic of ENDB-ERL8192CE Drawn By: Rev: 0B

Date: Tuesday, December 14, 2010 Sheet: 3 of 7

\*\*\*Y11, 25MHz crystal load capacitance uses 16pF\*\*\*



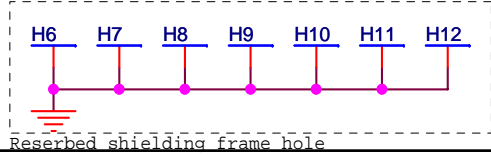
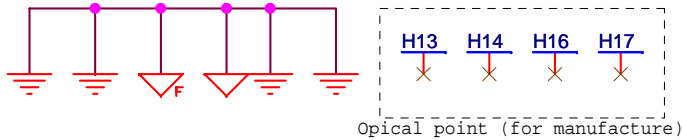
SDRAMClkSel[2:0]

000:	65.625 MHz
001:	78.125 MHz
010:	125 MHz
011:	150 MHz
100:	156.25 MHz (default)
101:	168.75 MHz
110:	193.75 MHz
111:	237.5 MHz

CPUClkSel[2:0]

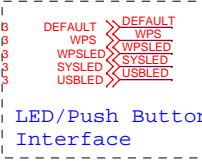
000:	250 MHz
001:	270 MHz
010:	290 MHz
011:	310 MHz
100:	330 MHz
101:	350 MHz
110:	370 MHz
111:	390 MHz

Signal	Function	Description
MA1	BOOTSEL	0: NOR Flash(default) 1: SPI Flash
MA3	Clklx_from_clkm	0: default 1: Clk_lx
MA4	Enable external reset	come from 0:clk_disable (default) 1: enable
MA5	SYNC_LX_OC	0: default 1: set SYNC_OC=SYNC_LX =SYNC_LX_OC for testing
MA[6:8]	(DRAM SEL CLK) clk_m2x_freq_sel[0:2]	H/W strap can set 3 bits[0:2]
MA[9:11]	(CPU SEL CLK) clk_cpu_freq_sel[1:3]	H/W strap can set 3 bits[1:3]
MA12	ck_cpu_div_sel	0: default 1: pll_cpu divide by AP mode
MA13	en_router_mode	0: 5 port router mode (default)

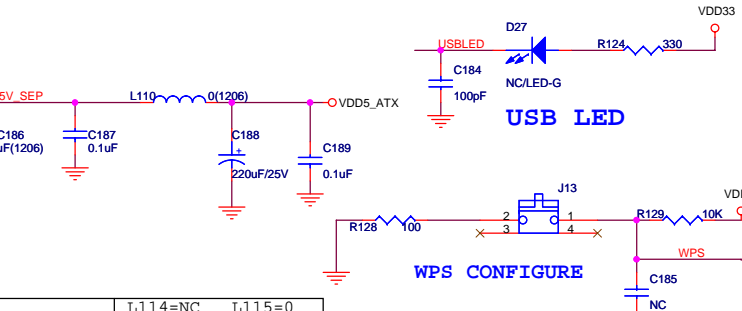
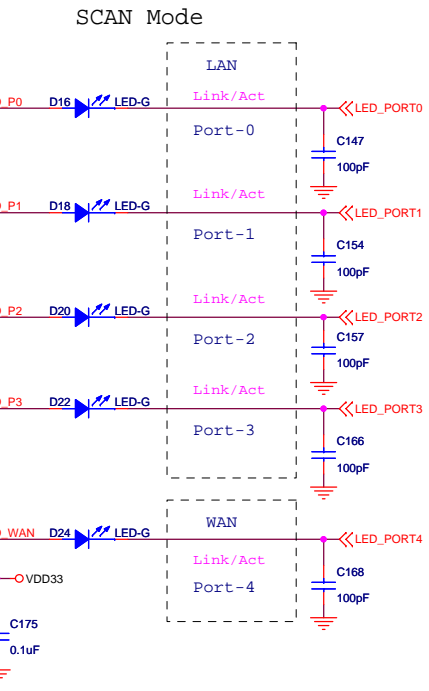
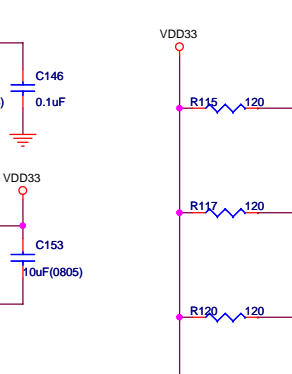
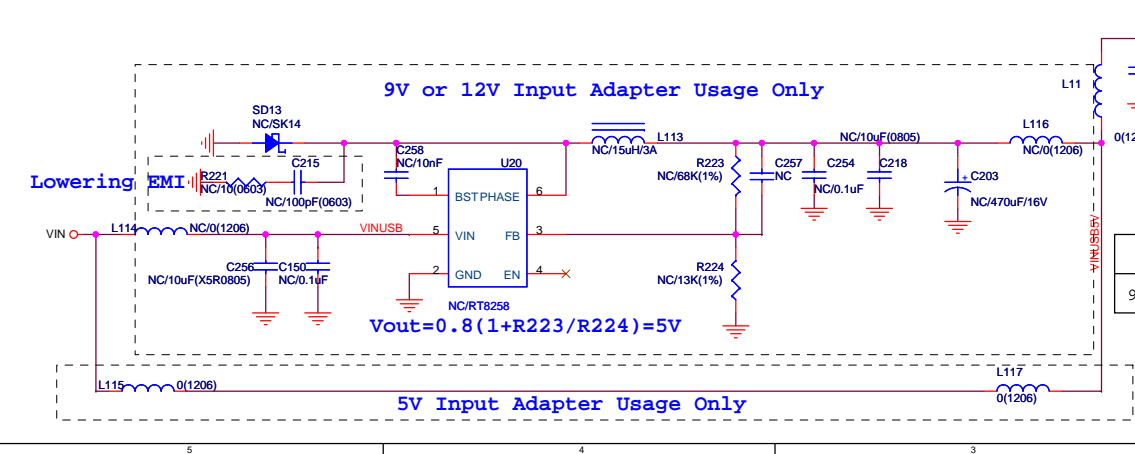
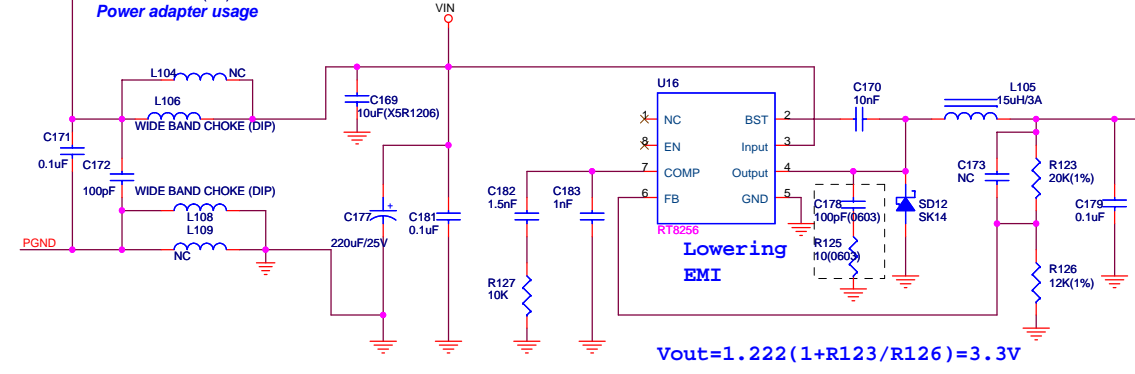
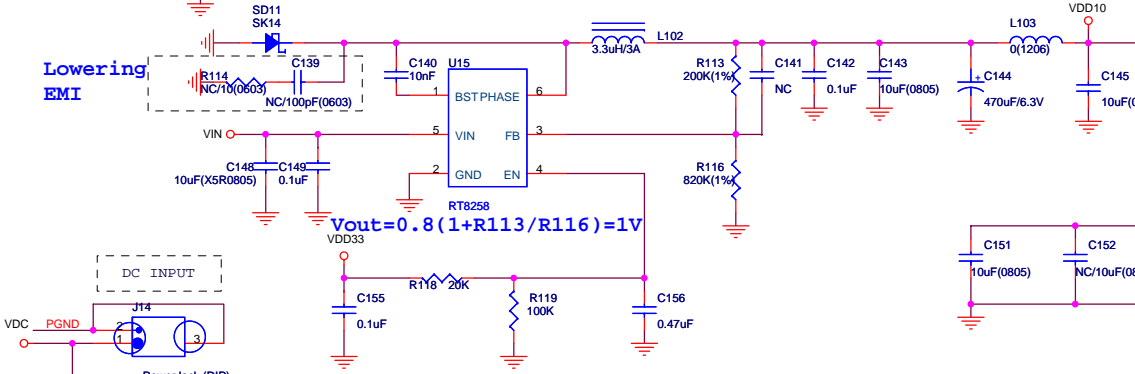
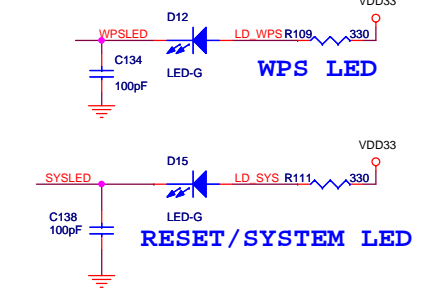
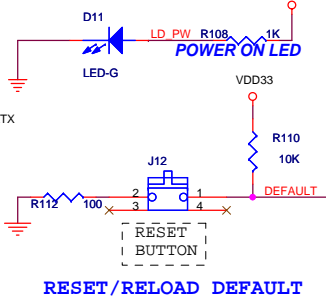
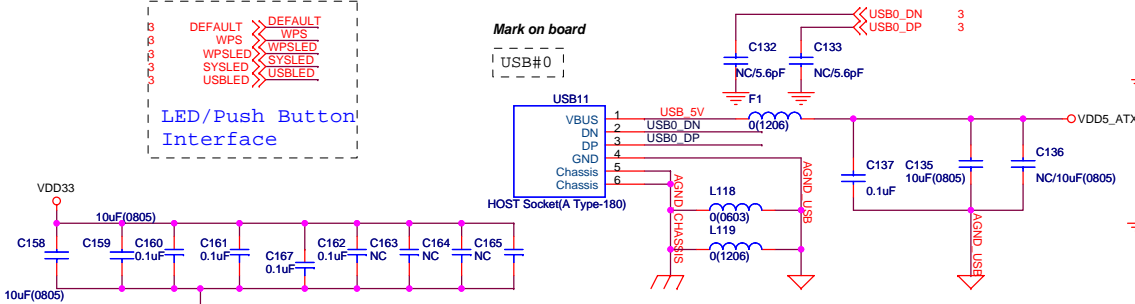


**ENCORE ELECTRONICS** Encore Electronics Inc.

Title CONFIGURE INTERFACE		Model ENDB-XRL8196C	
Size A	Document Number Schematic of ENDB-ERL8192CE	Drawn By	Rev 0B
Date:	Tuesday, December 14, 2010	Sheet	4 of 7



Mark on board  
USB#0



5V adapter	L114=NC L116=NC	L115=0 L117=0
9/12V adapter	L114=0 L116=0	L115=NC L117=NC

**ENCORE ELECTRONICS** Encore Electronics Inc.

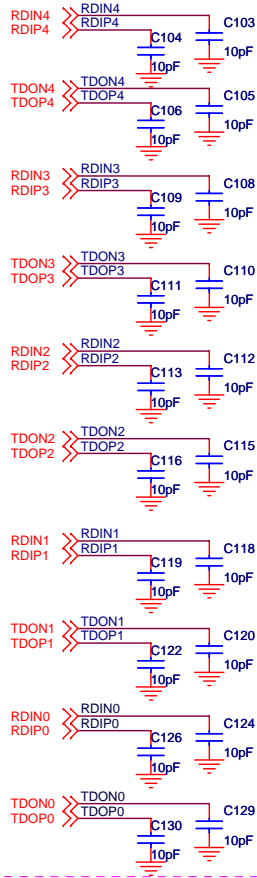
Title: POWER/LED/USB Model: ENDB-XRL8196C

Size Custom Document Number: Schematic of ENDB-ERL8192CE Drawn By: Rev 0B

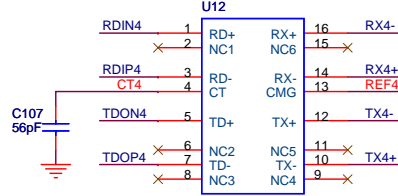
Date: Tuesday, December 14, 2010 Sheet 5 of 7

10pF for lowering EMI

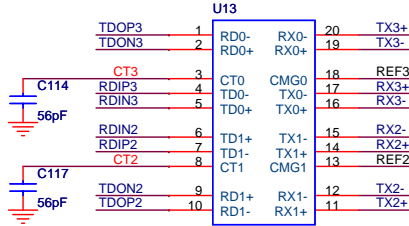
10/100M PHY Interface



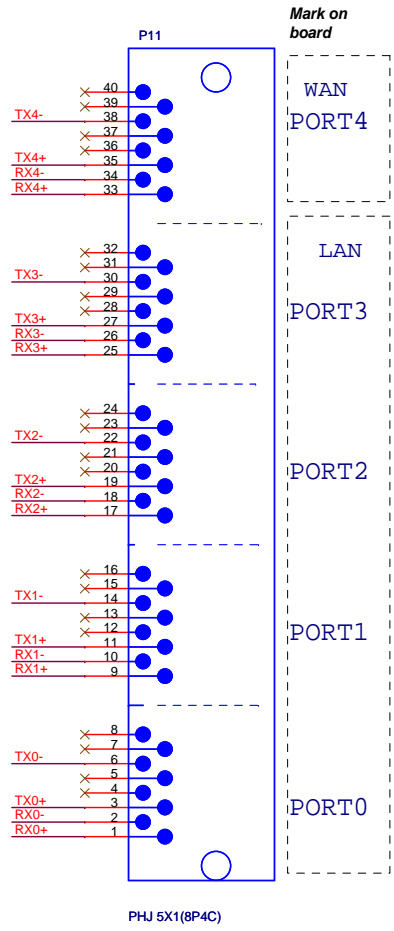
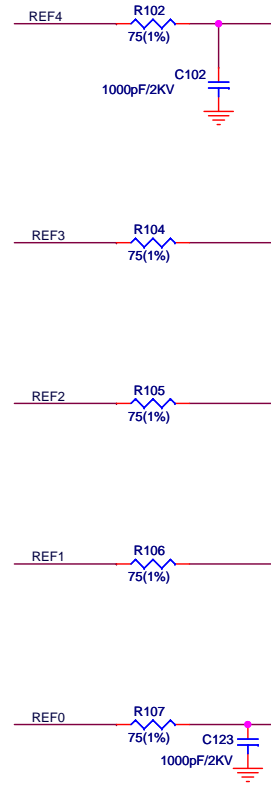
### Ethernet Transformer



U-TRON HTA-1616-R:  
Common mode chock  
near CPU side for  
lowering EMI



U-TRON HTA-2004-R:  
Common mode chock  
near CPU side for  
lowering EMI



**ENCORE ELECTRONICS** Encore Electronics Inc.

Title	MDI 10/100M	Model	ENDB-XRL8196C
Size	Document Number	Drawn By	Rev
B	Schematic of ENDB-ERL8192CE		0B
Date:	Tuesday, December 14, 2010	Sheet	6 of 7

RF 50 ohms trace

Power and Ground

1.5V Trace

1.2V Trace

ANT1 2412-2462MHz

RF PATH A

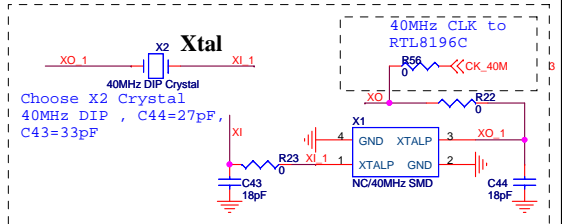
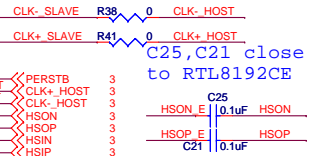
ANT2 2412-2462MHz

RF PATH B

These components inside of pink color line region are removed for 1T1R option

RTL8192CE

PCI-E Interface



ENCORE ELECTRONICS Encore Electronics Inc.

Title	WIFI	Model	ENDB-XRL8196C
Size	Document Number	Drawn By	Rev
Customer	Schematic of ENDB-ERL8192CE		0B
Date:	Tuesday, December 14, 2010	Sheet	7 of 7

