The Equipment under Test (EUT) is a Control unit for Batarang wireless controller model: 220050 operating at 2.4GHz band. It is powered by1x3.7V rechargeable battery and charged by PS3 USB port.

Channel List

Channel Number	Frequency (MHz)
1	2410.0000
2	2410.8109
3	2411.6218
4	2412.4327
5	2413.2436
6	2414.0545
7	2414.8654
8	2415.6763
9	2416.4872
10	2417.2981
11	2418.1090
12	2418.9199
13	2419.7308
14	2420.5417
15	2421.3526
16	2422.1635
17	2422.9744
18	2423.7853
19	2424.5962
20	2425.4071
21	2426.2180
22	2427.0289
23	2427.8398
24	2428.6507
25	2429.4616
26	2430.2725
27	2431.0834
28	2431.8943
29	2432.7052
30	2433.5161
31	2434.3270
32	2435.1379
33	2435.9488
34	2436.7597
35	2437.5706

36	*2438. 3815*
37	*2439. 1924*
38	*2440. 0033*
39	*2440. 8142*
40	*2441. 6251*
41	*2442. 4360*
42	*2443. 2469*
43	*2444. 0578*
44	*2444. 8687*
45	*2445. 6796*
46	*2446. 4905*
47	*2447. 3014*
48	*2448. 1123*
49	*2448. 9232*
50	*2449. 7341*
51	*2450. 5450*
52	*2451. 3559*
53	*2452. 1668*
54	*2452. 9777*
55	*2453. 7886*
56	*2454. 5995*
57	*2455. 4104*
58	*2456. 2213*
59	*2457. 0322*
60	*2457. 8431*
61	*2458. 6540*
62	*2459. 4649*
63	*2460. 2758*
64	*2461. 0867*
65	*2461. 8976*
66	*2462. 7085*
67	*2463. 5194*
68	*2464. 3303*
69	*2465. 1412*
70	*2465. 9521*
71	*2466. 7630*
72	*2467. 5739*
73	*2468. 3848*
74	*2469. 1957*
75	*2470. 0066*

Modulation Type: GFSK

Antenna Type: Integral antenna

The functions of main Components are mentioned as below.

Main Board

1) U1 acts as Standalone Linear Li-Ion Battery Charger.

2) U2 acts as power regulator.

3) U4&U7 act as a 3D-Sensor &G-Sensor chip, it will quantify the acceleration data of the X, Y and Z directions and converts the data to voltage value.

4) U6 acts as IO expansion.

5) U8 acts as 2- Wire Serial EEPROM.

6) Y1 acts as 12MHz oscillator for U5.

7) U5 acts as MCU, it processes the input data from the game player, and collects the game player data such as pressing the button, touching the panel, drawing, gesture and acceleration etc and sends this information to 2.4G RF module.

8) U3 acts as RF module.

RF Module

1) U1 acts 2.4 RF Chip.

2) X1 acts as 26MHz oscillator for U1.

RF Chip Worksheet

Chipcon SmartRF® CC2500

CC2500
Single Chip Low Cost Low Power RF-Transceiver

Applications

- *2400-2483.5MHz ISM/SRD band systems*
- *Consumer Electronics*
- *Wireless game controllers*
- *Wireless audio*
- *Wireless keyboard and mouse*

Product Description

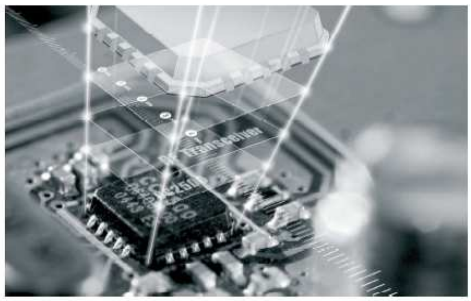
The **CC2500** is a low cost true single chip 2.4GHz transceiver designed for very low power wireless applications. The circuit is intended for the ISM (Industrial, Scientific and Medical) and SRD (Short Range Device) frequency band at 2400MHz-2483.5MHz.

The RF transceiver is integrated with a highly configurable baseband modem which has a configurable data rate up to 500kbps. Performance can be increased by enabling a Forward Error Correction option, which is integrated in the modem.

CC2500 provides extensive hardware support for packet handling, data buffering, burst transmissions, clear channel assessment, link quality indication and wake on radio.

The main operating parameters and the 64-byte transmit/receive FIFOs of **CC2500** can be controlled via an SPI interface. In a typical system, the **CC2500** will be used together with a microcontroller and a few extra passive components.

CC2500 is based on Chipcon's SmartRF®04 technology in 0.18µm CMOS.



Key Features

- Small size (QLP 4x4mm package, 20 pins)
- True single chip 2.4GHz RF transceiver
- Frequency range: *2400MHz-2483.5MHz*
- High sensitivity (–98dBm at 10kbps, 1% packet error rate)
- Programmable data rate up to 500kbps
- Low current consumption (15.6mA in RX)
- Programmable output power up to +1dBm
- Excellent receiver selectivity and blocking performance
- Very few external components: Totally on-chip frequency synthesizer, no external filters or RF switch needed
- Programmable baseband modem
- Ideal for multi-channel operation
- Configurable packet handling hardware
- Suitable for frequency hopping systems due to a fast settling frequency synthesizer
- Optional Forward Error Correction with interleaving
- Separate 64-byte RX and TX data FIFOs
- Efficient SPI interface: All registers can be programmed with one "burst" transfer
- Digital RSSI output
- Suited for systems compliant with EN 300 328 and EN 300 440 class 2 (Europe), CFR47 Part 15 (US), and ARIB STD-T66 (Japan)
- Wake-on-radio functionality for automatic low-power RX polling
- Many powerful digital features allow a high-performance RF system to be made using an inexpensive microcontroller
- Integrated analog temperature sensor
- Lead-free "green" package

Features (continued from front page)

- Flexible support for packet oriented systems: On chip support for sync word detection, address check, flexible packet length and automatic CRC handling.
- Programmable channel filter bandwidth
- OOK and flexible ASK shaping supported
- 2-FSK and MSK supported
- Automatic Frequency Compensation can be used to align the frequency synthesizer to received centre frequency
- Optional automatic whitening and de-whitening of data
- Support for asynchronous transparent receive/transmit mode for backwards compatibility with existing radio communication protocols
- Programmable Carrier Sense indicator
- Programmable Preamble Quality Indicator for detecting preambles and improved protection against sync word detection in random noise
- Support for automatic Clear Channel Assessment (CCA) before transmitting (for listen-before-talk systems)
- Support for per-package Link Quality Indication

1 Abbreviations

Abbreviations used in this data sheet are described below.

2-FSK	Binary Frequency Shift Keying
ADC	Analog to Digital Converter
AFC	Automatic Frequency Offset Compensation
AGC	Automatic Gain Control
AMR	Automatic Meter Reading
ASK	Amplitude Shift Keying
BER	Bit Error Rate
CCA	Clear Channel Assessment
CRC	Cyclic Redundancy Check
ESR	Equivalent Series Resistance
FEC	Forward Error Correction
FSK	Frequency Shift Keying
IF	Intermediate Frequency
LNA	Low Noise Amplifier
LQI	Link Quality Indicator
MCU	Microcontroller Unit
MSK	Minimum Shift Keying
PA	Power Amplifier
PD	Power Down
PER	Packet Error Rate
PLL	Phase Locked Loop
PQI	Preamble Quality Indicator
QPSK	Quadrature Phase Shift Keying
RCOSC	RC Oscillator
RF	Radio Frequency
RSSI	Received Signal Strength Indicator
RX	Receive, Receive Mode
SNR	Signal to Noise Ratio
SPI	Serial Peripheral Interface
TBD	To Be Defined
TX	Transmit, Transmit Mode
VCO	Voltage Controlled Oscillator
WOR	Wake on Radio, Low power polling
XOSC	Crystal Oscillator
XTAL	Crystal

2 Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 1 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Caution! *ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.*

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.6	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD+0.3, max 3.6	V	
Voltage on the pins RF_P, RF_N and DCOUPL	–0.3	2.0	V	
Input RF level		TBD	dBm	
Storage temperature range	–50	150	°C	
Solder reflow temperature		260	°C	T = 10 s
ESD		2	kV	All pads (excluding RF) have 2kV HBM ESD protection

Table 1: Absolute Maximum Ratings

3 Operating Conditions

The operating conditions for ***CC2500*** are listed Table 2 in below.

Parameter	Min	Max	Unit	Condition
Operating temperature	–40	85	°C	
Operating supply voltage	1.8	3.6	V	All supply pins must have the same voltage

Table 2: Operating Conditions

4 Electrical Specifications

Tc = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's ***CC2500*** EM reference design.

Parameter	Min	Typ	Max	Unit	Condition
Current consumption		8.7		µA	Automatic RX polling once each second, using low-power RC oscillator, with 460Hz filter bandwidth and 250kbps data rate, PLL calibration every 4th wakeup. Average current with signal in channel *below* carrier sense level.
		35		µA	Same as above, but with signal in channel *above* carrier sense level, 1.9ms RX timeout, and no preamble/sync word found.
		1.4		µA	Automatic RX polling every 15th second, using low-power RC oscillator, with 460kHz filter bandwidth and 250kbps data rate, PLL calibration every 4th wakeup. Average current with signal in channel below carrier sense level.
		16		µA	Same as above, but with signal in channel *above* carrier sense level, 14ms RX timeout, and no preamble/sync word found.
		1.8		mA	Only voltage regulator to digital part and crystal oscillator running (IDLE state)
		7.6		mA	Only the frequency synthesizer running (after going from IDLE until reaching RX or TX states, and frequency calibration states)
		15.6		mA	Receive mode, input near sensitivity limit (RX state)
		13.3		mA	Receive mode, input 30dB above sensitivity limit (RX state)
		11.5		mA	Transmit mode, –12dBm output power (TX state)
		15.4		mA	Transmit mode, -6dBm output power (TX state)
		21.6		mA	Transmit mode, 0dBm output power (TX state)
Current consumption in power down modes		180		µA	Voltage regulator to digital part on, all other modules in power down (XOFF state)
		100		µA	Voltage regulator to digital part off, register values retained, XOSC running (SLEEP state with `MCSM0.OSC_FORCE_ON` set)
		900		nA	Voltage regulator to digital part off, register values retained, low-power RC oscillator running (SLEEP state with WOR enabled)
		500		nA	Voltage regulator to digital part off, register values retained (SLEEP state)

Table 3: Electrical Specifications

5 General Characteristics

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency range	2400		2483.5	MHz	
Data rate	1.2		500	kbps	Modulation formats supported: (Shaped) MSK (differential offset QPSK, up to 500kbps) 2-FSK (up to 250kbps) OOK/ASK (up to 250kbps) Optional Manchester encoding (halves the data rate).

Table 4: General Characteristics

6 RF Receive Section

Tc = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's *CC2500* EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential input impedance		200		Ω	Optimised for matching to both 50Ω single-ended load and PCB antennas with higher impedance.
Receiver sensitivity		TBD		dBm	500kbps data rate (MSK), 1% packet error rate, 16 bytes packet length, 650kHz digital channel filter bandwidth.
		–88		dBm	250kbps data rate (2-FSK), 1% packet error rate, 16 bytes packet length, 460kHz digital channel filter bandwidth.
		–98		dBm	10kbps data rate (2-FSK), 1% packet error rate, 16 bytes packet length, 232kHz digital channel filter bandwidth.
Saturation		–15		dBm	
Digital channel filter bandwidth	58		650	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0MHz crystal).
Adjacent channel rejection		20-25 (TBD)		dB	Desired channel 3dB above the sensitivity limit. Depends on channel spacing and digital channel filter bandwidth.
Alternate channel rejection		25-35 (TBD)		dB	Desired channel 3dB above the sensitivity limit. Depends on channel spacing and digital channel filter bandwidth.
Image channel rejection		30 (TBD)		dB	Desired channel 3dB above the sensitivity limit. Depends on intermediate frequency (IF), channel spacing and digital channel filter bandwidth. Image channel rejection can be limited by adjacent channel rejection or alternate channel rejection when using low IF (<100kHz). Optimum IF depends on data rate and related chip configurations provided by SmartRF® Studio software.
Selectivity at 1MHz offset		–27		dB	Desired channel at –80dBm.
Selectivity at 2MHz offset		–27		dB	Desired channel at –80dBm.
Selectivity at 5MHz offset		–36		dB	Desired channel at –80dBm. Compliant to ETSI EN 300 440 class 2 receiver requirements.
Selectivity at 10MHz offset		–51		dB	Desired channel at –80dBm. Compliant to ETSI EN 300 440 class 2 receiver requirements.
Selectivity at 20MHz offset		–54		dB	Desired channel at –80dBm. Compliant to ETSI EN 300 440 class 2 receiver requirements.
Selectivity at 50MHz offset		–55		dB	Desired channel at –80dBm. Compliant to ETSI EN 300 440 class 2 receiver requirements.
Spurious emissions			–57 –47	dBm dBm	25MHz – 1GHz Above 1GHz

Table 5: RF Receive Section

7 RF Transmit Section

Tc = 25°C, VDD = 3.0V if nothing else stated. Measured on Chipcon's ***CC2500*** EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Differential load impedance		200		Ω	Optimised for matching to both 50Ω single-ended load and PCB antennas with higher impedance.
Output power, highest setting		1		dBm	Output power is programmable. Delivered to 50Ω single-ended load via Chipcon reference RF matching network.
Output power, lowest setting		–30		dBm	Output power is programmable. Delivered to 50Ω single-ended load via Chipcon reference RF matching network.
Adjacent channel power		–26		dBc	The given values are for 1MHz channel spacing (±1MHz from carrier) and 500kbps MSK.
Alternate channel power		–45		dBc	The given values are for 1MHz channel spacing (±2MHz from carrier) and 500kbps MSK.
Spurious emissions			–36	dBm	25MHz – 1GHz
			–54	dBm	47-74, 87.5-118, 174-230,470-862MHz
			–47	dBm	1800MHz-1900MHz (restricted band in Europe)
			–41	dBm	At 2·RF and 3·RF (restricted bands in USA)
			–30	dBm	Otherwise above 1GHz

Table 6: RF Transmit Parameters

8 Crystal Oscillator

Tc = 25°C @ VDD = 3.0V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Crystal frequency	26	26	28	MHz	
Tolerance		±40		ppm	This is the total tolerance including a) initial tolerance, b) ageing and c) temperature dependence. The acceptable crystal tolerance depends on RF frequency and channel spacing / bandwidth.
ESR			100	Ω	
C_0			TBD	pF	
C_L	TBD		TBD	pF	
Start-up time		300		µs	Measured on Chipcon's ***CC2500*** EM reference design.

Table 7: Crystal Oscillator Parameters

9 Low Power RC Oscillator

Typical performance is for Tc = 25°C @ VDD = 3.0V if nothing else is stated.

The values in the table are simulated results and will be updated in later versions of the data sheet.

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency	34.6	34.7	37.3	kHz	Calibrated RC Oscillator frequency is XTAL frequency divided by 750
Frequency accuracy after calibration			±0.2	%	
Temperature coefficient		+0.4		% / °C	Frequency drift when temperature changes after calibration
Supply voltage coefficient		+3		% / V	Frequency drift when supply voltage changes after calibration
Initial calibration time		2		ms	When the RC Oscillator is enabled, calibration is continuously done in the background as long as the crystal oscillator is running.
Wake-up period	63e-6		64800	Seconds	Programmable, dependent on XTAL frequency

Table 8: RC Oscillator parameters

10 Frequency Synthesizer Characteristics

Tc = 25°C @ VDD = 3.0V if nothing else is stated. Measured on Chipcon's ***CC2500*** EM reference design.

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{18}$	427	Hz	26MHz-28MHz crystal.
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing.
RF carrier phase noise		–73		dBc/Hz	@ 50kHz offset from carrier
RF carrier phase noise		–73		dBc/Hz	@ 100kHz offset from carrier
RF carrier phase noise		–73		dBc/Hz	@ 200kHz offset from carrier
RF carrier phase noise		–96		dBc/Hz	@ 1MHz offset from carrier
RF carrier phase noise		–106		dBc/Hz	@ 2MHz offset from carrier
RF carrier phase noise		–112		dBc/Hz	@ 5MHz offset from carrier
RF carrier phase noise		–113		dBc/Hz	@ 10MHz offset from carrier
PLL turn-on / hop time			80	µs	Time from leaving the IDLE state until arriving in the RX, FSTXON or TX state, when not performing calibration. Crystal oscillator running.
PLL RX/TX and TX/RX settling time			10	µs	Settling time for the 1xIF frequency step from RX to TX, and vice versa.
PLL calibration time		18739		XOSC cycles	Calibration can be initiated manually, or automatically before entering or after leaving RX/TX.
	0.67	0.72	0.72	ms	Min/typ/max time is for 28/26/26MHz crystal frequency.

Table 9: Frequency Synthesizer Parameters

11 Analog temperature sensor

The characteristics of the analog temperature sensor are listed in Table 10 below. Note that it is necessary to write 0xBF to the PTEST register to use the analog temperature sensor in the IDLE state.

The values in the table are simulated results and will be updated in later versions of the data sheet. Minimum / maximum values are valid over entire supply voltage range. Typical values are for 3.0V supply voltage.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C	0.638	0.648	0.706	V	
Output voltage at 0°C	0.733	0.743	0.793	V	
Output voltage at +40°C	0.828	0.840	0.891	V	
Output voltage at +80°C	0.924	0.939	0.992	V	
Output voltage at +120°C	1.022	1.039	1.093	V	
Temperature coefficient	2.35	2.45	2.46	mV/°C	Fitted from –20°C to +80°C
Absolute error in calculated temperature	–14	–8	+14	°C	From –20°C to +80°C when assuming best fit for absolute accuracy: 0.763V at 0°C and 2.44mV / °C
Error in calculated temperature, calibrated	–2		+2	°C	From –20°C to +80°C when using 2.44mV / °C, after 1-point calibration at room temperature
Settling time after enabling		TBD		µs	
Current consumption increase when enabled		0.3		mA	

Table 10: Analog Temperature Sensor Parameters

12 DC Characteristics

The DC Characteristics of *CC2500* are listed in Table 11 below.

Tc = 25°C if nothing else stated.

Digital Inputs/Outputs	Min	Max	Unit	Condition
Logic "0" input voltage	0	0.7	V	
Logic "1" input voltage	VDD-0.7	VDD	V	
Logic "0" output voltage	0	0.5	V	For up to 4mA output current
Logic "1" output voltage	VDD-0.3	VDD	V	For up to 4mA output current
Logic "0" input current	N/A	–1	µA	Input equals 0V
Logic "1" input current	N/A	1	µA	Input equals VDD

Table 11: DC Characteristics

13 Power On Reset

When the power supply complies with the requirements in Table 12 below, proper Power-On-Reset functionality is guaranteed. Otherwise, the chip should be assumed to have unknown state until transmitting an SRES strobe over the SPI interface. It is recommended to transmit an SRES strobe after turning power on in any case. See section 28.1 on page 30 for a description of the recommended start up sequence after turning power on.

Parameter	Min	Typ	Max	Unit	Condition/Note
Power-up ramp-up time.			5	ms	From 0V until reaching 1.8V
Power off time	1			ms	Minimum time between power off and power-on.

Table 12: Power-on Reset Requirements

14 Pin Configuration

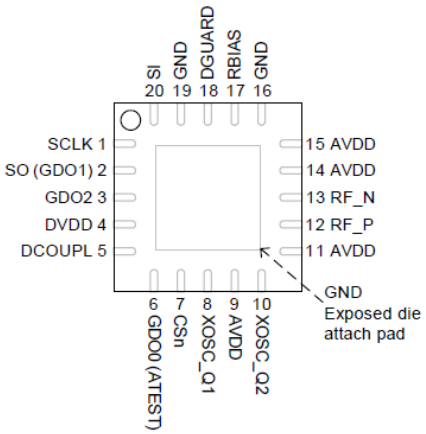


Figure 1: Pinout top view

Note: The exposed die attach pad **must** be connected to a solid ground plane as this is the main ground connection for the chip.

Pin #	Pin name	Pin type	Description
1	SCLK	Digital Input	Serial configuration interface, clock input
2	SO (GDO1)	Digital Output	Serial configuration interface, data output. Optional general output pin when CSn is high
3	GDO2	Digital Output	Digital output pin for general use: • Test signals • FIFO status signals • Clear Channel Indicator • Clock output, down-divided from XOSC • Serial output RX data
4	DVDD	Power (Digital)	1.8V-3.6V digital power supply for digital I/O's and for the digital core voltage regulator
5	DCOUPL	Power (Digital)	1.6V-2.0V digital power supply output for decoupling. NOTE: This pin is intended for use with the ***CC2500*** only. It cannot be used to provide supply voltage to other devices.
6	GDO0 (ATEST)	Digital I/O	Digital output pin for general use: • Test signals • FIFO status signals • Clear Channel Indicator • Clock output, down-divided from XOSC • Serial output RX data • Serial input TX data Also used as analog test I/O for prototype/production testing
7	CSn	Digital Input	Serial configuration interface, chip select
8	XOSC_Q1	Analog I/O	Crystal oscillator pin 1, or external clock input
9	AVDD	Power (Analog)	1.8V-3.6V analog power supply connection
10	XOSC_Q2	Analog I/O	Crystal oscillator pin 2
11	AVDD	Power (Analog)	1.8V-3.6V analog power supply connection
12	RF_P	RF I/O	Positive RF input signal to LNA in receive mode Positive RF output signal from PA in transmit mode
13	RF_N	RF I/O	Negative RF input signal to LNA in receive mode Negative RF output signal from PA in transmit mode
14	AVDD	Power (Analog)	1.8V-3.6V analog power supply connection
15	AVDD	Power (Analog)	1.8V-3.6V analog power supply connection
16	GND	Ground (Analog)	Analog ground connection
17	RBIAS	Analog I/O	External bias resistor for reference current
18	DGUARD	Power (Digital)	Power supply connection for digital noise isolation
19	GND	Ground (Digital)	Ground connection for digital noise isolation
20	SI	Digital Input	Serial configuration interface, data input

Table 13: Pinout overview

15 Circuit Description

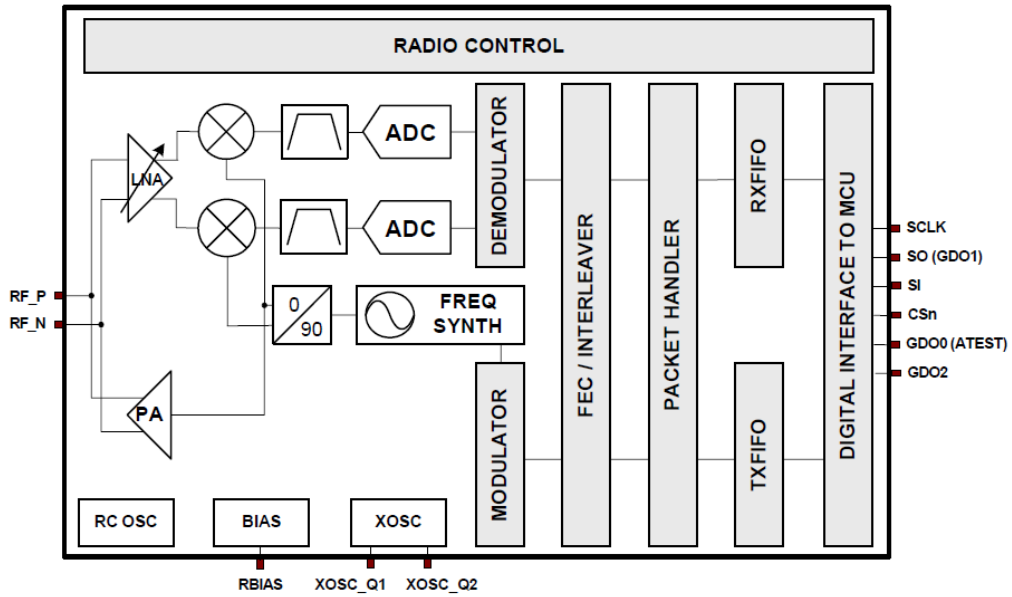


Figure 2: *CC2500* Simplified Block Diagram

A simplified block diagram of ***CC2500*** is shown in Figure 2.

CC2500 features a low-IF receiver. The received RF signal is amplified by the low-noise amplifier (LNA) and down-converted in quadrature (I and Q) to the intermediate frequency (IF). At IF, the I/Q signals are digitised by the ADCs. Automatic gain control (AGC), fine channel filtering, demodulation bit/packet synchronization is performed digitally.

The transmitter part of ***CC2500*** is based on direct synthesis of the RF frequency. The frequency synthesizer includes a completely on-chip LC VCO and a 90 degrees phase shifter for generating the I and Q LO signals to the down-conversion mixers in receive mode.

A crystal is to be connected to XOSC_Q1 and XOSC_Q2. The crystal oscillator generates the reference frequency for the synthesizer, as well as clocks for the ADC and the digital part.

A 4-wire SPI serial interface is used for configuration and data buffer access.

The digital baseband includes support for channel configuration, packet handling and data buffering.

16 Application Circuit

Only a few external components are required for using the ***CC2500***. The recommended application circuit is shown in Figure 3. The external components are described in Table 14, and typical values are given in Table 15. Note that the PCB antenna alternative indicated in Figure 3 is preliminary and subject to changes. Performance for the PCB antenna alternative will be included in future revisions of this data sheet.

Bias resistor

The bias resistor R171 is used to set an accurate bias current.

Balun and RF matching

C122, C132, L121 and L131 form a balun that converts the differential RF port on ***CC2500*** to a single-ended RF signal (C121 and C131 are also needed for DC blocking). Together with an appropriate LC network, the balun components also transform the impedance to match a 50Ω antenna (or cable). Component

values for the RF balun and LC network are easily found using the SmartRF® Studio software. Suggested values are listed in Table 15.

Crystal

The crystal oscillator uses an external crystal with two loading capacitors (C81 and C101). See section 34 on page 36 for details.

Power supply decoupling

The power supply must be properly decoupled close to the supply pins. Note that decoupling capacitors are not shown in the application circuit. The placement and the size of the decoupling capacitors are very important to achieve the optimum performance. Chipcon provides a reference design that should be followed closely.

Component	Description
C51	100nF decoupling capacitor for on-chip voltage regulator to digital part
C81/C101	Crystal loading capacitors, see section 34 on page 36 for details
C121/C131	RF balun DC blocking capacitors
C122/C132	RF balun/matching capacitors
C123/C124	RF LC filter/matching capacitors
L121/L131	RF balun/matching inductors (inexpensive multi-layer type)
L122	RF LC filter inductor (inexpensive multi-layer type)
R171	56kΩ resistor for internal bias current reference
XTAL	26MHz-28MHz crystal, see section 34 on page 36 for details

Table 14: Overview of external components (excluding supply decoupling capacitors)

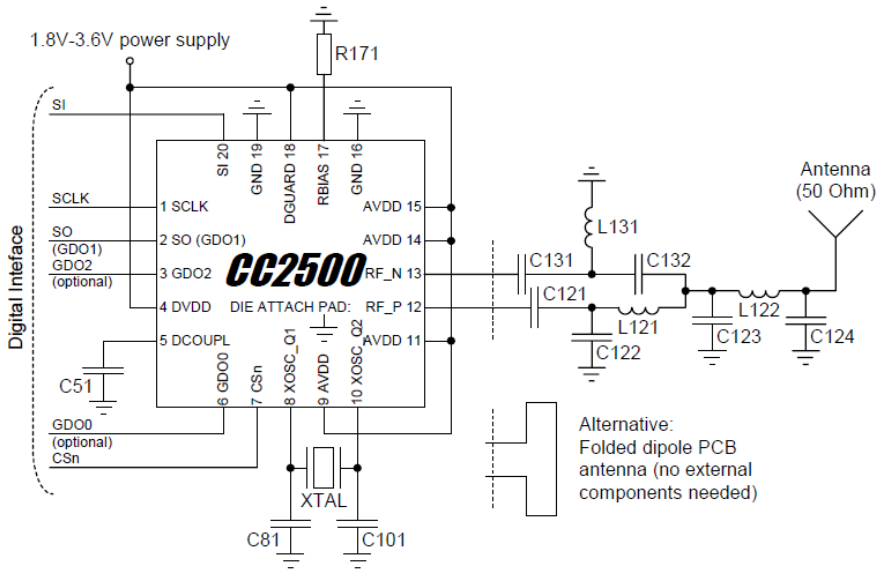


Figure 3: Typical application and evaluation circuit (power supply decoupling not shown)

Component	Value
C51	100nF±10%, 0402 X5R
C81	27pF±5%, 0402 NP0
C101	27pF±5%, 0402 NP0
C121	100pF±5%, 0402 NP0
C122	1.0pF±0.25pF, 0402 NP0
C123	1.8pF±0.25pF, 0402 NP0
C124	1.5pF±0.25pF, 0402 NP0
C131	100pF±5%, 0402 NP0
C132	1.0pF±0.25pF, 0402 NP0
L121	1.2nH±0.3nH, 0402 monolithic
L122	1.2nH±0.3nH, 0402 monolithic
L131	1.2nH±0.3nH, 0402 monolithic
R171	56kΩ±1%, 0402
XTAL	26.0MHz surface mount crystal

Table 15: Bill Of Materials for the application circuit (subject to changes)

17 Configuration Overview

CC2500 can be configured to achieve optimum performance for many different applications. Configuration is done using the SPI interface. The following key parameters can be programmed:

- Power-down / power up mode
- Crystal oscillator power-up / power – down
- Receive / transmit mode
- RF channel selection
- Data rate
- Modulation format
- RX channel filter bandwidth
- RF output power
- Data buffering with separate 64-byte receive and transmit FIFOs
- Packet radio hardware support
- Forward Error Correction with interleaving
- Data Whitening
- Wake On Radio (WOR)

Details of each configuration register can be found in section 38, starting on page 39.

Figure 4 shows a simplified state diagram that explains the main ***CC2500*** states, together with typical usage and current consumption. For detailed information on controlling the ***CC2500*** state machine, and a complete state diagram, see section 28, starting on page 29.

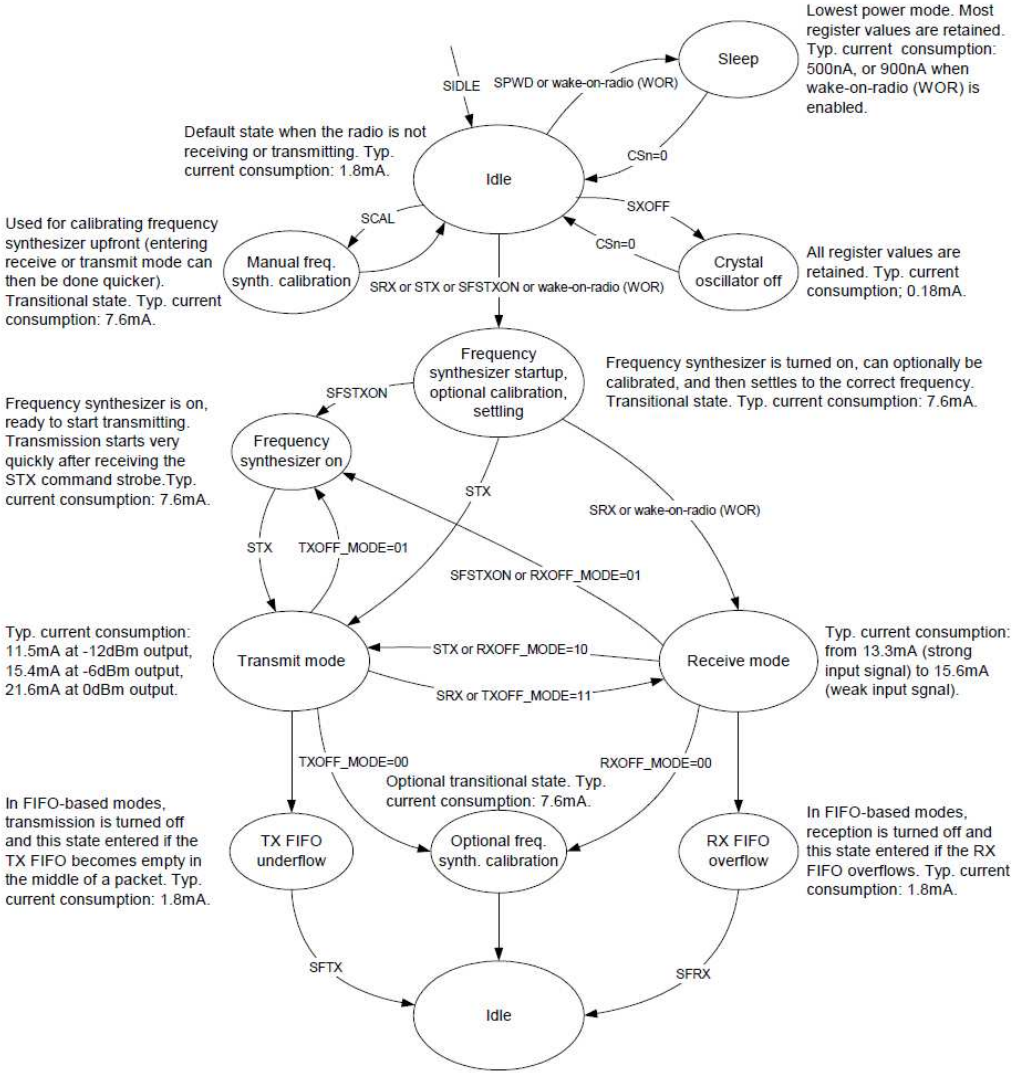


Figure 4: Simplified state diagram, with typical usage and current consumption

18 Configuration Software

CC2500 can be configured using the SmartRF® Studio software, available for download from http://www.chipcon.com. The SmartRF® Studio software is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality. A screenshot of the SmartRF® Studio user interface for ***CC2500*** is shown in Figure 5.