DATA SHEET

RX101_RX101B

LOW Cost 2.4GHZ Radio Transceiver

RUIXING Use Only

Preliminary

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Version 1.3

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Low Cost 2.4GHz Radio Transceiver

FEATURES

Complete 2.4 GHz radio transceiver includes fully integrated RF PLL and channel filtering

Supports Frequency-Hopping Spread Spectrum

Supports SPI and I²C bus interface

Built-in smart auto-acknowledge Tx/Rx protocol simplifies usage

Packet data rate 1 Mbps over-the-air

FIFO flag signal permits continuous streaming data at 1 Mbps over-the-air

Power management for minimizing current consumption

Digital readout of RSSI and temperature

Lead-free 4x4mm QFN Package & SOP16 for best RF performance

Application

Remote controls

Wireless keyboards and mice

Proprietary Wireless Networks

Home automation

Commercial and industrial short-range wireless

Wireless voice, VoIP, Cordless headsets

Robotics and machine connectivity

GENERAL DESCRIPTION

The RX101 is a low-cost, fully integrated CMOS RF transceiver, GFSK data modem, and packet framer, optimized for use in the 2.4 GHz ISM band. It contains transmit, receive, RF synthesizer, and digital modem functions, with few external components. The transmitter supports digital power control. The receiver utilizes extensive digital processing for excellent overall performance, even in the presence of interference and transmitter impairments.

The RX101 transmits GFSK data at approximately 1 dBm output power. The low-IF receiver architecture produces good selectivity, with sensitivity down to approx. -87 dBm. Digital RSSI values are available to monitor channel quality.

On-chip transmit and receive FIFO registers are available to buffer the data transfer with MCU. Over-the-air data rate is always 1 Mbps even when connected to a slow, low-cost MCU. Built-in CRC, FEC, data whitening, and automatic retry/acknowledge are all available to simplify and optimize performance for individual applications.

The digital baseband interface can be either 4-wire SPI or 2-wire I2C-bus. Three additional pins are available for optional reset and buffer control.

For extended battery life, power consumption is minimized all key areas. A sleep mode is available to reduce standby current consumption to just 1 uA typ. while preserving register settings.

This product is available in RoHS compliant 24-lead 4x4 mm JEDEC standard QFN package, featuring an exposed pad on the bottom for best RF characteristics. Also available in bare die form.

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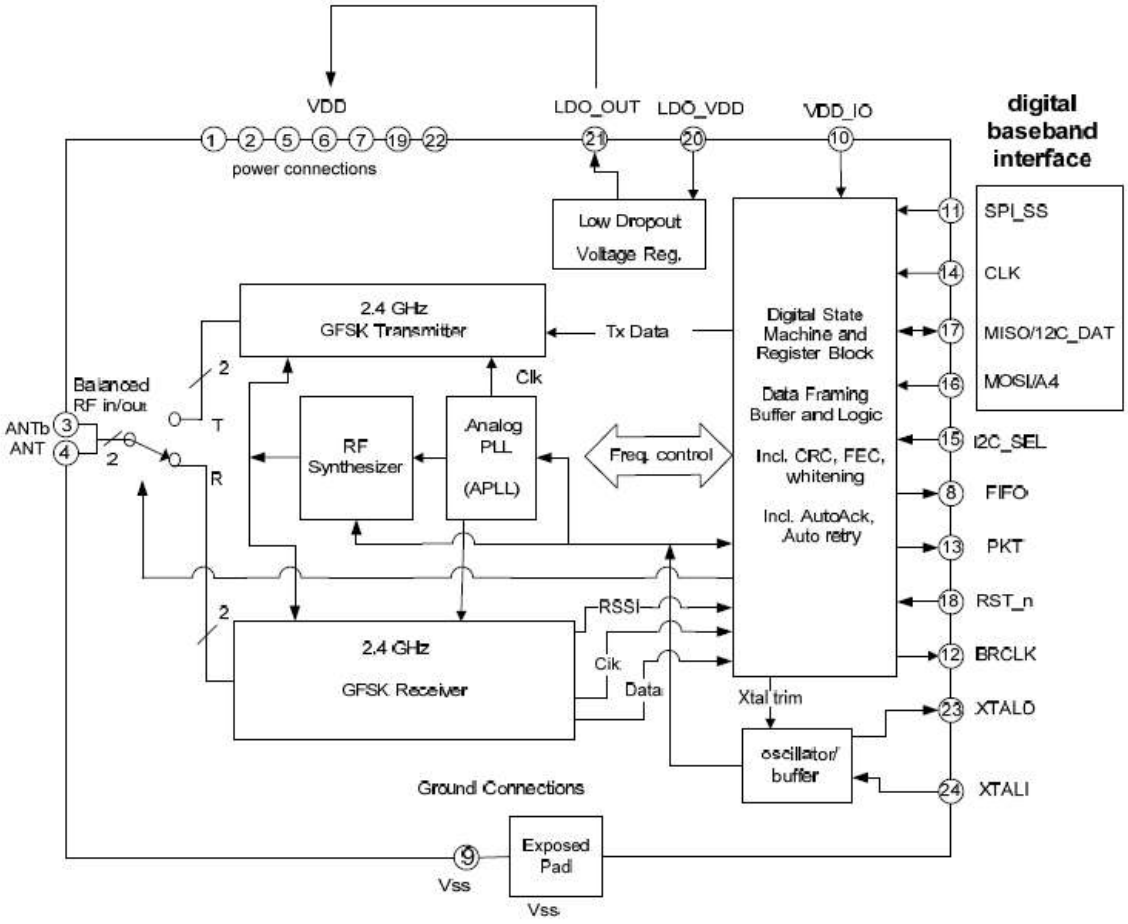
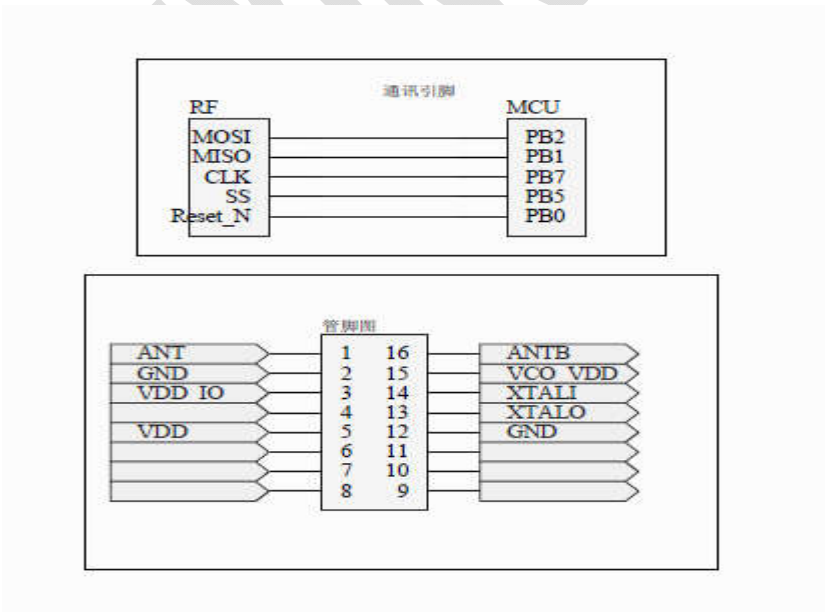
1. Block Diagram





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2. Absolute Maximum Ratings

Table 1. Absolute Maximum Rating

Parameter	Symbol	MIN	TYP	MAX	Unit
Operating Temp.	T_{OP}	-40		+85	°C
Storage Temp.	$T_{STORAGE}$	-55		+125	°C
LDO_VDD, VDD_IO Voltage	V_{IN_MAX}			+3.7	VDC
VDD pins	VDD_MAX			+2.5	
Applied Voltages to Other Pins	V_{OTHER}	-0.3		+3.7	VDC
Input RF Level	P_{IN}			+10	dBm
Output Load mismatch (Z0=50Ω)	VSWROUT			10:1	VSWR

Notes:

1. Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics section below.

2. These devices are electro-static sensitive. Devices should be transported and stored in anti-static containers. Equipment and personnel contacting the devices need to be properly grounded. Cover workbenches with grounded conductive mats.

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3. Electrical Characteristics

Table 2. Electrical Characteristics

The following specifications are guaranteed for TA = 25 C, LDO_VDD= VDD_IO = 3.3 VDC, unless otherwise noted.

Parameter	Symbol	MIN	TYP	MAX	Units	Test Condition and Notes
Supply Voltage						
DC power supply voltage range		1.9		3.6	VDC'	Input to VDD_IO and LDO_VDD pins.
Current Consumption						
Current Consumption - TX	IDD_TXH		18		mA	POUT = high power setting
	IDD_TXL		12		mA	POUT = low power setting
Current Consumption - RX	IDD_RX		17		mA	
Current Consumption –IDLE	IDD_IDLE1		1.4		mA	Configured for BRCLK output running.
	IDD_IDLE2		1.1		mA	Configured for BRCLK output OFF.
Current Consumption - SLEEP	IDD_SLP		1		uA	
Digital Inputs						
Logic input high	VIH	0.8 VDD_IN		1.2 VDD_IN	V	
Logic input low	VIL	0		0.8	V	
Input Capacitance	C_IN			10	pF	
Input Leakage Current	I_LEAK_IN			10	uA	
Digital Outputs						
Logic output high	VOH	0.8 VDD_IN		VDD_IN	V	
Logic output low	VOL			0.4	V	
Output Capacitance	C_OUT			10	pF	
Output Leakage Current	I_LEAK_OUT			10	uA	
Rise/Fall Time (SPI)	T_RISE_OUT			5	nS	
Clock Signals						
CLK rise, fall time (SPI)	Tr_spi			25	nS	Requirement for error-free register reading, writing.
CLK frequency range (SPI)	FSPI	0	12		MHz	
Overall Transceiver						
Operating Frequency Range	F_OP	2400		2482	MHz	
Antenna port mismatch	VSWR_I		<2:1		VSWR	Receive mode.
(Z0=50Ω)	VSWR_O		<2:1		VSWR	Transmit mode.

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Parameter	Symbol	MIN	TYP	MAX	Unis	Test Condition and Notes	
Receive Section						Measured using 50 Ohm balun. For BER ≤ 0.1%:	
Receiver sensitivity			-87		dBm	FEC off.	
Maximum useable signal		-20	1		dBm		
Data (Symbol) rate	Ts		1		us		
Min. Carrier/Interference ratio						For BER ≤ 0.1%	
Co-Channel Interference	CI_cochannel		+9		dB	-60 dBm desired signal.	
Adjacent Ch. Interference, 1MHz offset	CI_1		+6		dB	-60 dBm desired signal.	
Adjacent Ch. Interference, 2MHz offset	CI_2		-12		dB	-60 dBm desired signal.	
Adjacent Ch. Interference, 3MHz offset	CI_3		-24		dB	-67 dBm desired signal.	
Out-of-Band Blocking For additional test conditions, see footnote1.	OBB_1	-10			dBm	30 MHz to 2000 MHz	Meas. with ACX BF2520 ceramic filter 2 on ant. pin . Desired sig. -67 dBm, BER ≤ 0.1%.
	OBB_2	-27			dBm	2000 MHz to 2400 MHz	
	OBB_3	-27			dBm	2500 MHz to 3000 MHz	
	OBB_4	-10			dBm	3000 MHz to 12.75 GHz	
Transmit Section						Measured using 50 Ohm balun3:	
RF Output Power	PAV			6	dBm	POUT= maximum output power Reg09=0x4000	
			2			POUT = nominal output power, Reg09=0x1840	
		-17				POUT=minimum output power,Reg09=1FC0	
Second harmonic			-50		dBm	Conducted to ANT pin.	
Third harmonic			-50		dBm	Conducted to ANT pin.	
Modulation Characteristics							
Peak FM Deviation 00001111 pattern	Δf1avg		280		kHz		
Peak FM Deviation 01010101 pattern	Δf2max		225		kHz		
In-Band Spurious Emission							
2MHz offset	IBS_2			-40	dBm		
>3MHz offset	IBS_3			-60	dBm		
Out-of-Band Spurious Emission, Operation	OBS_O_1		< -60	-36	dBm	30 MHz ~ 1 GHz	
	OBS_O_2		-45	-30	dBm	1 GHz ~ 12.75 GHz, excludes desired signal and harmonics.	
	OBS_O_3		< -60	-47	dBm	1.8 GHz ~ 1.9 GHz	
	OBS_O_4		< -65	-47	dBm	5.15 GHz ~ 5.3 GHz	

Note:

1. ***The test is run at one midband frequency, typically 2460 MHz. With blocking frequency swept in 1 MHz steps, up to 24 exception frequencies are allowed. Of these, no more than 5 shall persist with blocking signal reduced to -50dBm. For blocking frequencies below desired receive frequency, in-band harmonics of the out-of-band blocking signal are the most frequent cause of failure, so be sure blocking signal has adequate harmonic filtering.***
2. ***In some applications, this filter may be incorporated into the antenna, or be approximated by the effective antenna bandwidth.***
3. ***Transmit power measurement is corrected for insertion loss of Balun, in order to indicate the transmit power at the IC pins.***

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Parameter	Symbol	MIN	TYP	MAX	Unit	Test Condition and Notes	
RF VCO and PLL Section							
Typical PLL lock range	FLOCK	2366		2516	MHz		
Tx, Rx Frequency Tolerance			--		ppm	Same as XTAL pins frequency tolerance	
Channel (Step) Size			1		MHz		
SSB Phase Noise			≤ -95		dBc/Hz	550kHz offset	
			≤ -115		dBc/Hz	2MHz offset	
Crystal oscillator freq. range (Reference Frequency)			12.000		MHz	Designed for 12 MHz crystal reference freq.	
Crystal oscillator digital trim range, typ.			±20		ppm	See Register 27 description. Amount of pull depends on crystal spec. and operating point.	
RF PLL Settling Time	THOP		75	150	uS	Settle to within 30 kHz of final value.	
Spurious Emissions	OBS_1		< -75	-57	dBm	30 MHz ~ 1 GHz	IDLE state, Synthesizer and VCO ON.
	OBS_2		-68	-47	dBm	1 GHz ~ 12.75 GHz	
LDO Voltage Regulator Section							
Dropout Voltage	Vdo		0.17	0.5	V	Measured during Receive state	

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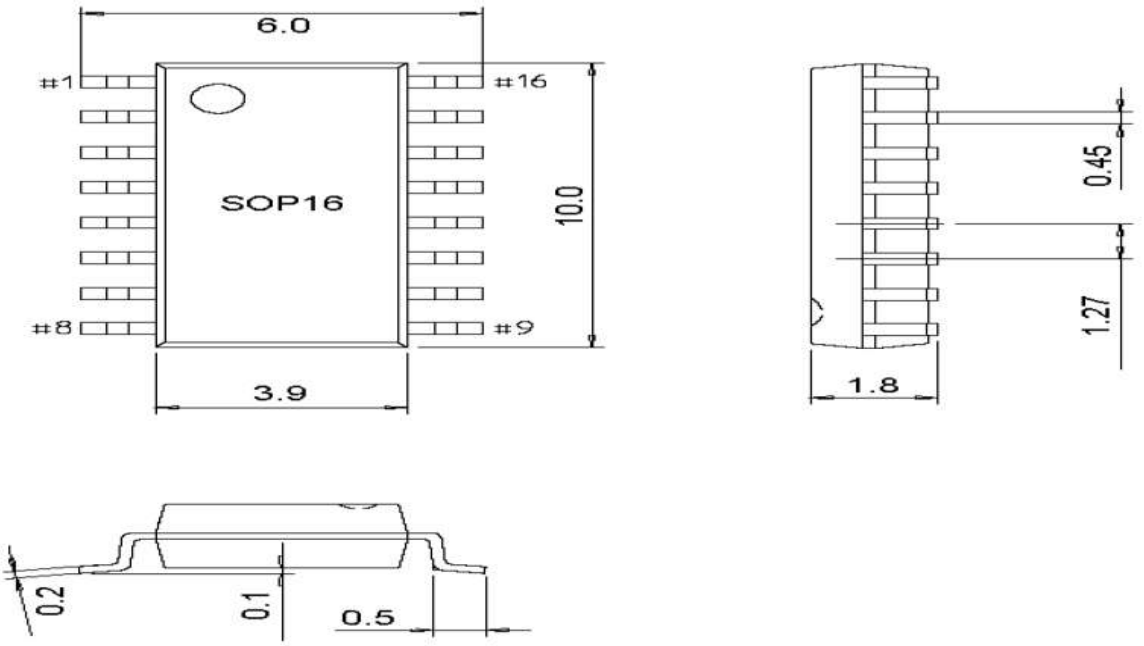

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