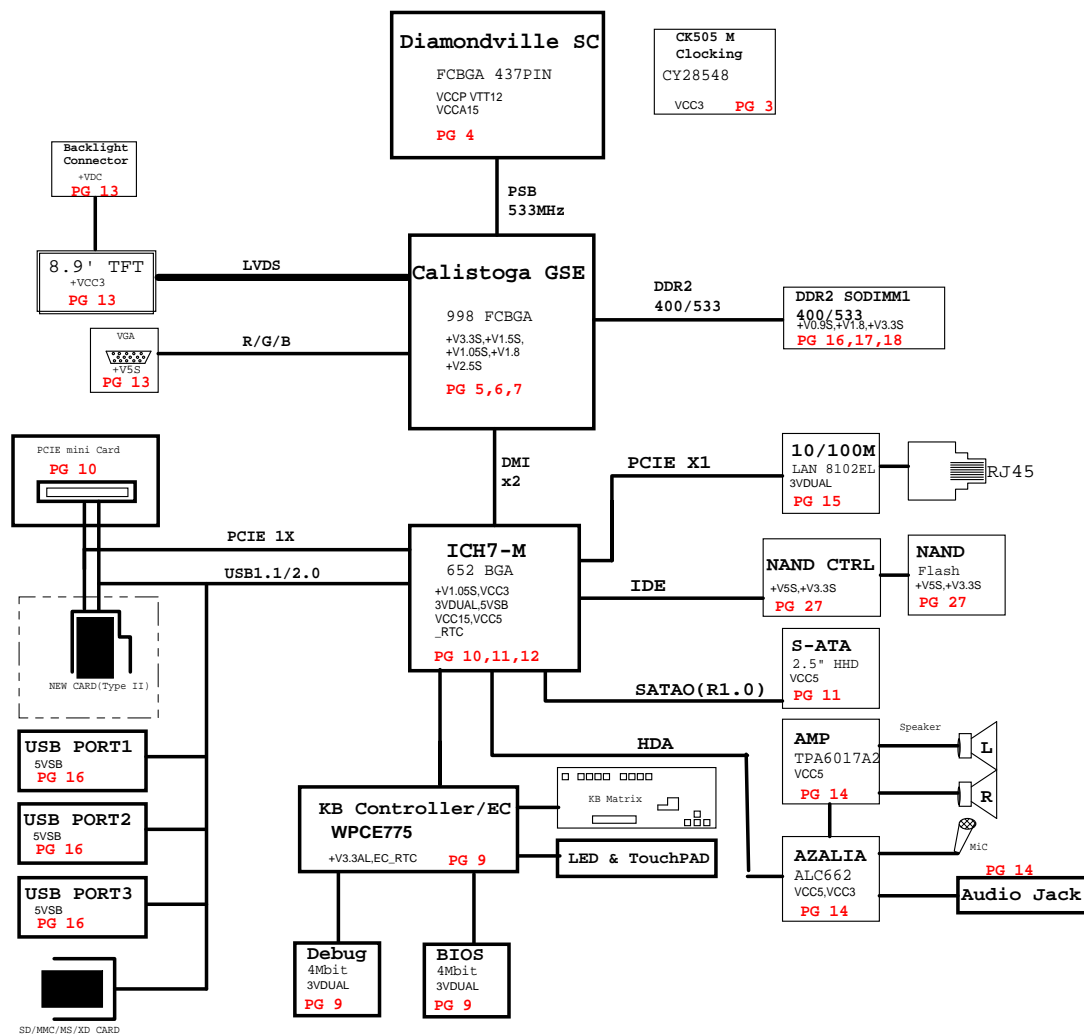
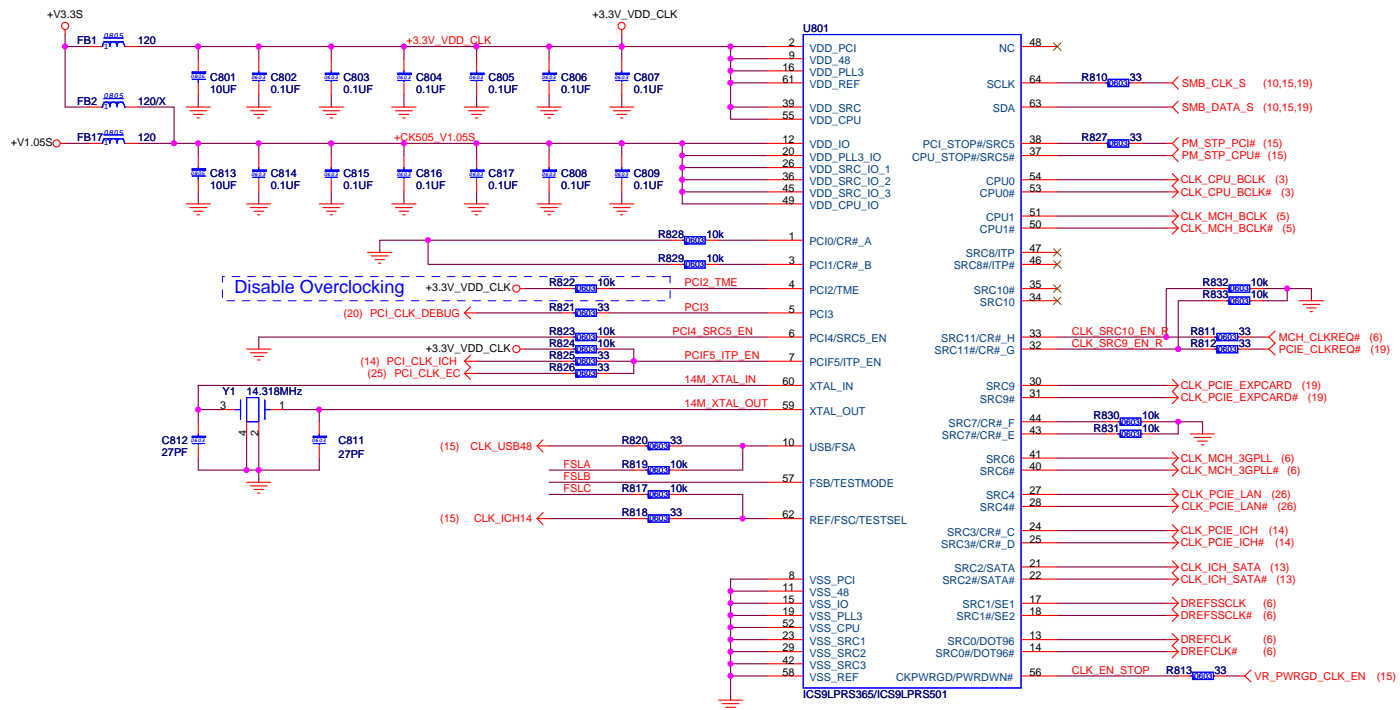


Phitowin KT945 sch V1.0

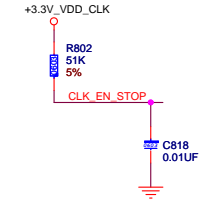
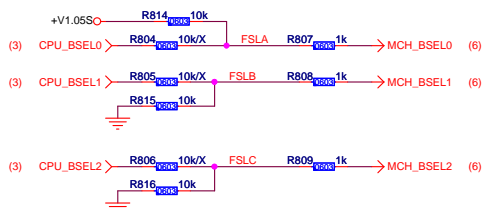


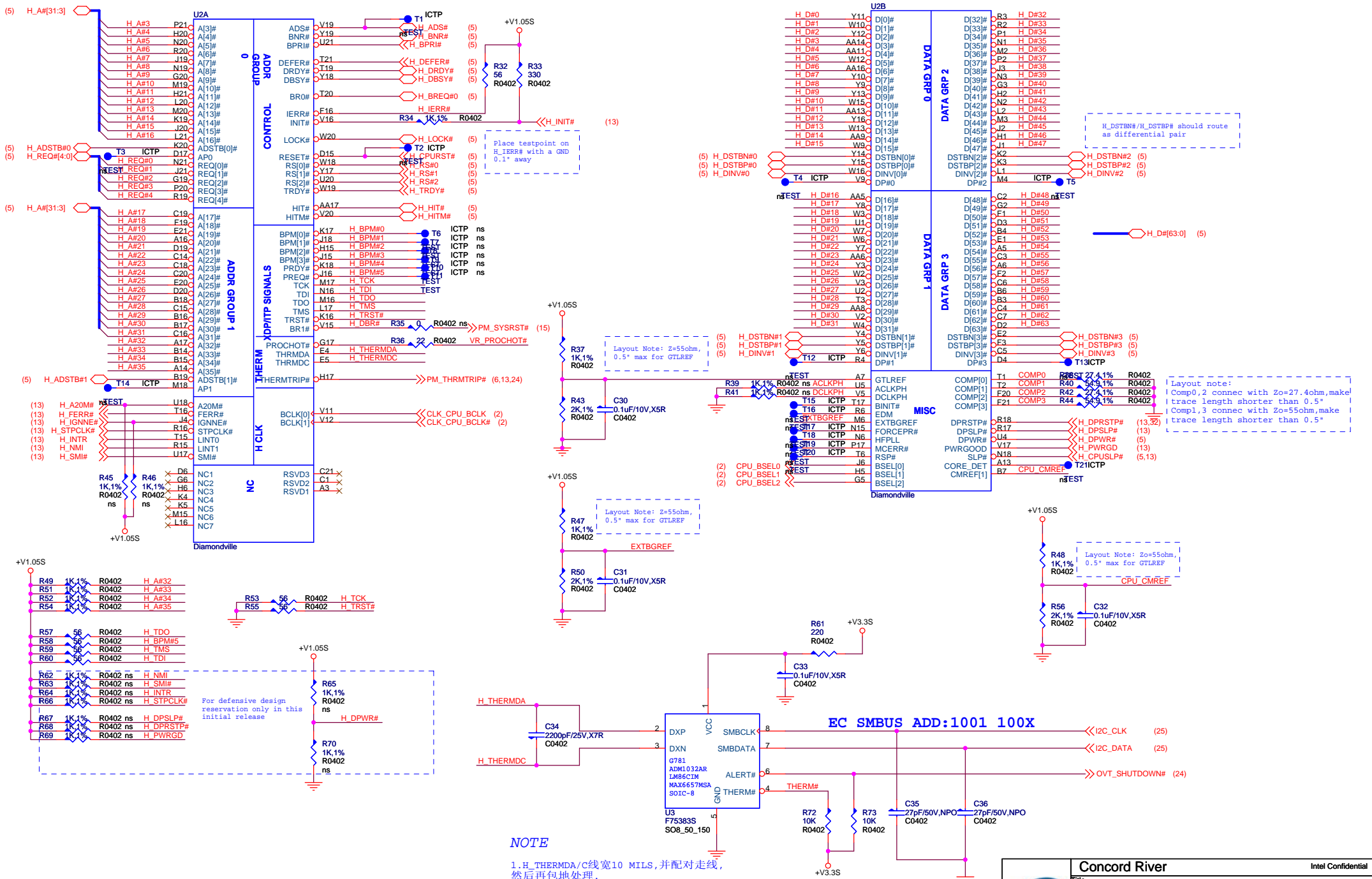


Disable Overclocking

CPU, MCH and XDP BCLK FREQUENCY SELECTION TABLE

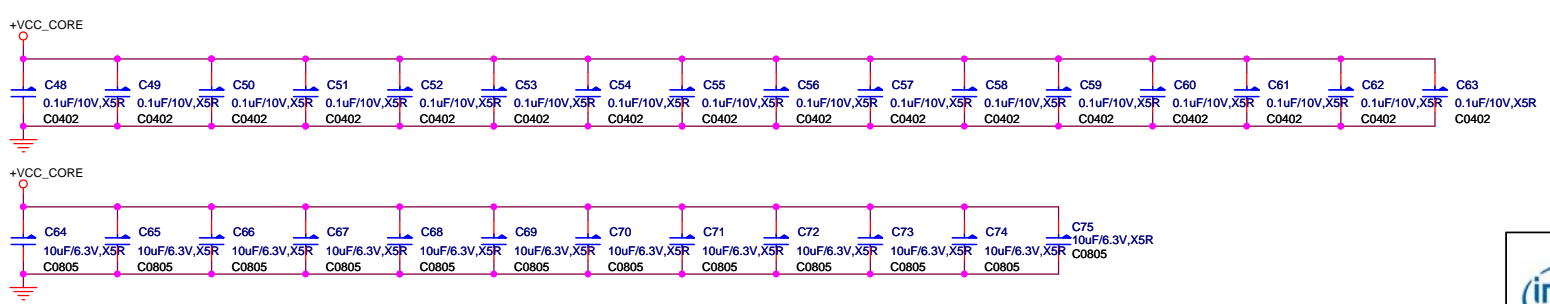
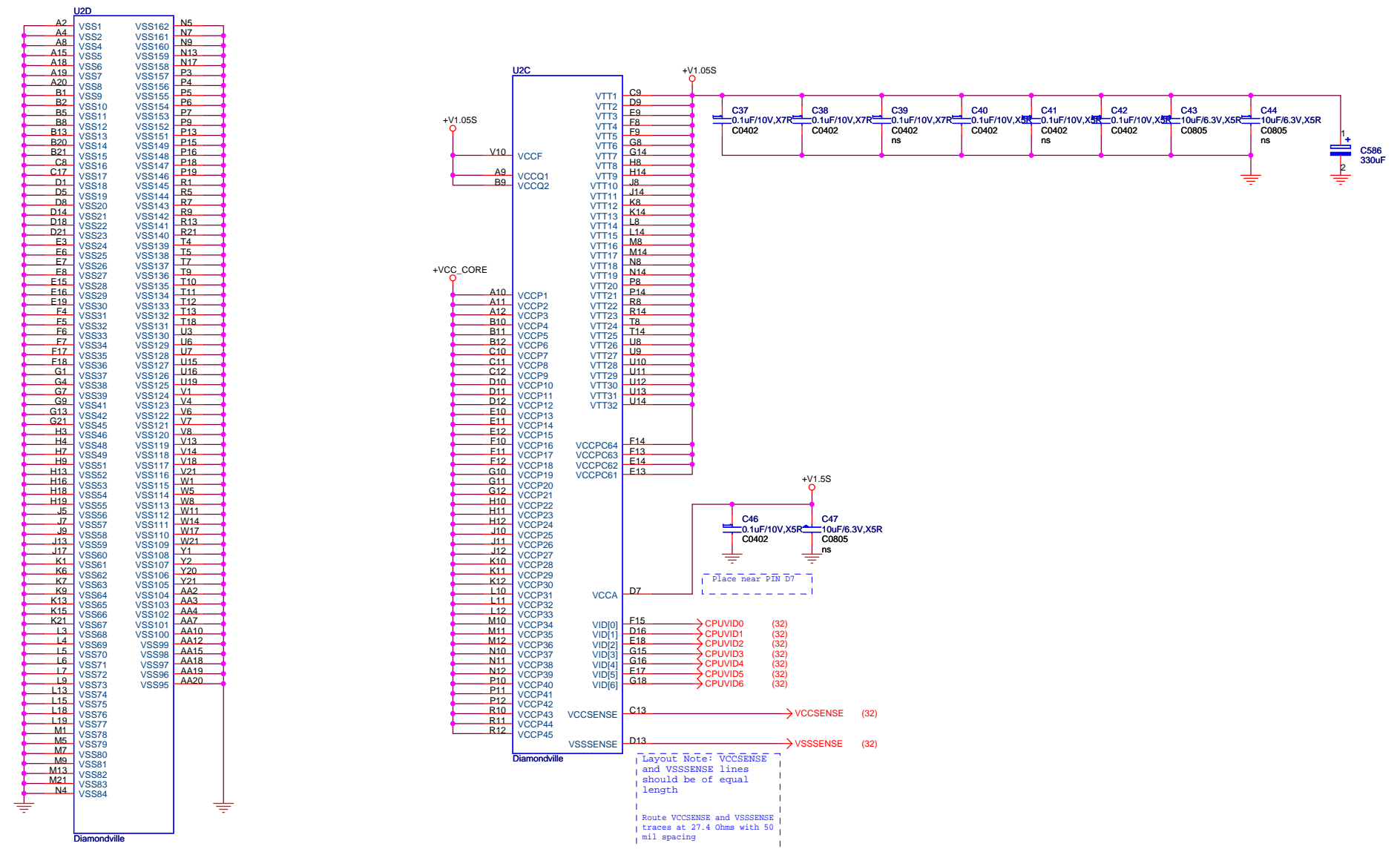
FSC BSEL2	FSB BSEL1	FSA BSEL0	Host Clock frequency MHz
1	0	1	100
0	0	1	133
0	1	1	166
0	1	0	200
0	0	0	266
1	0	0	333
1	1	0	400
1	1	1	Reserved

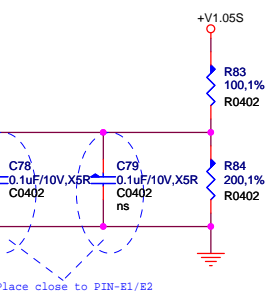
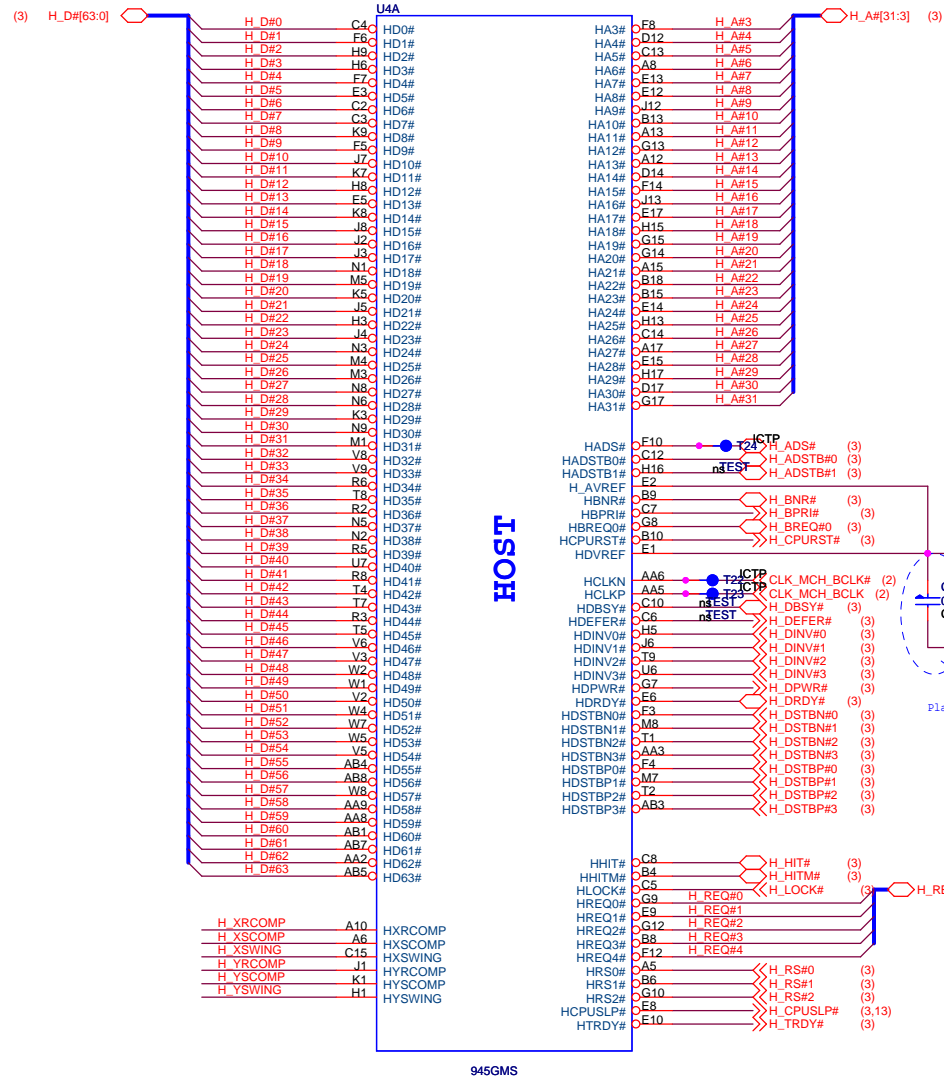
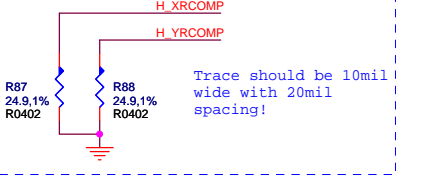
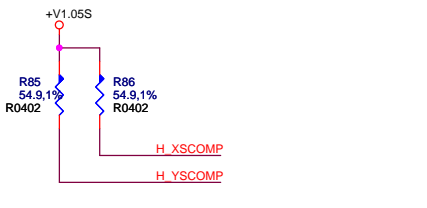
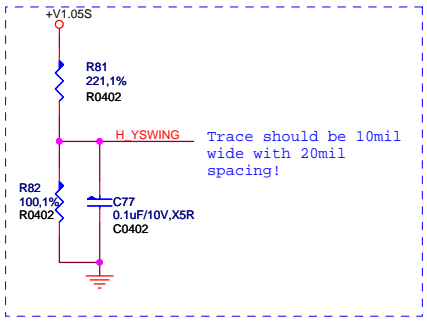
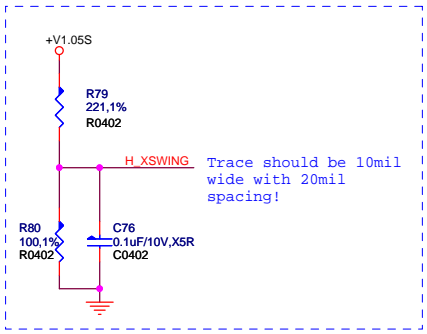


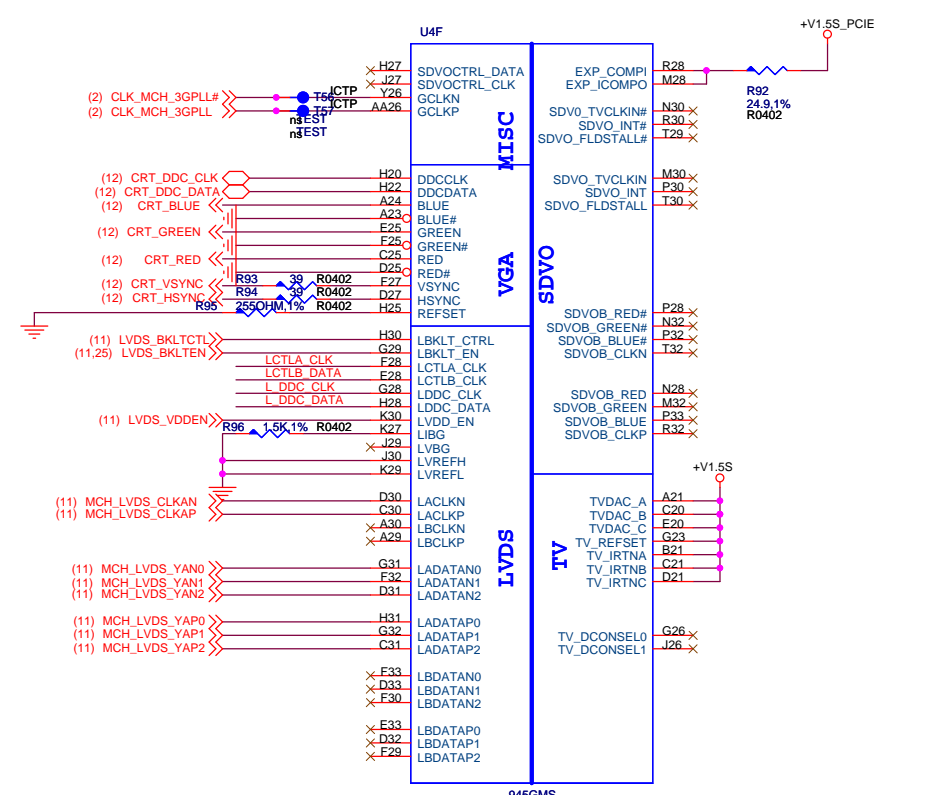
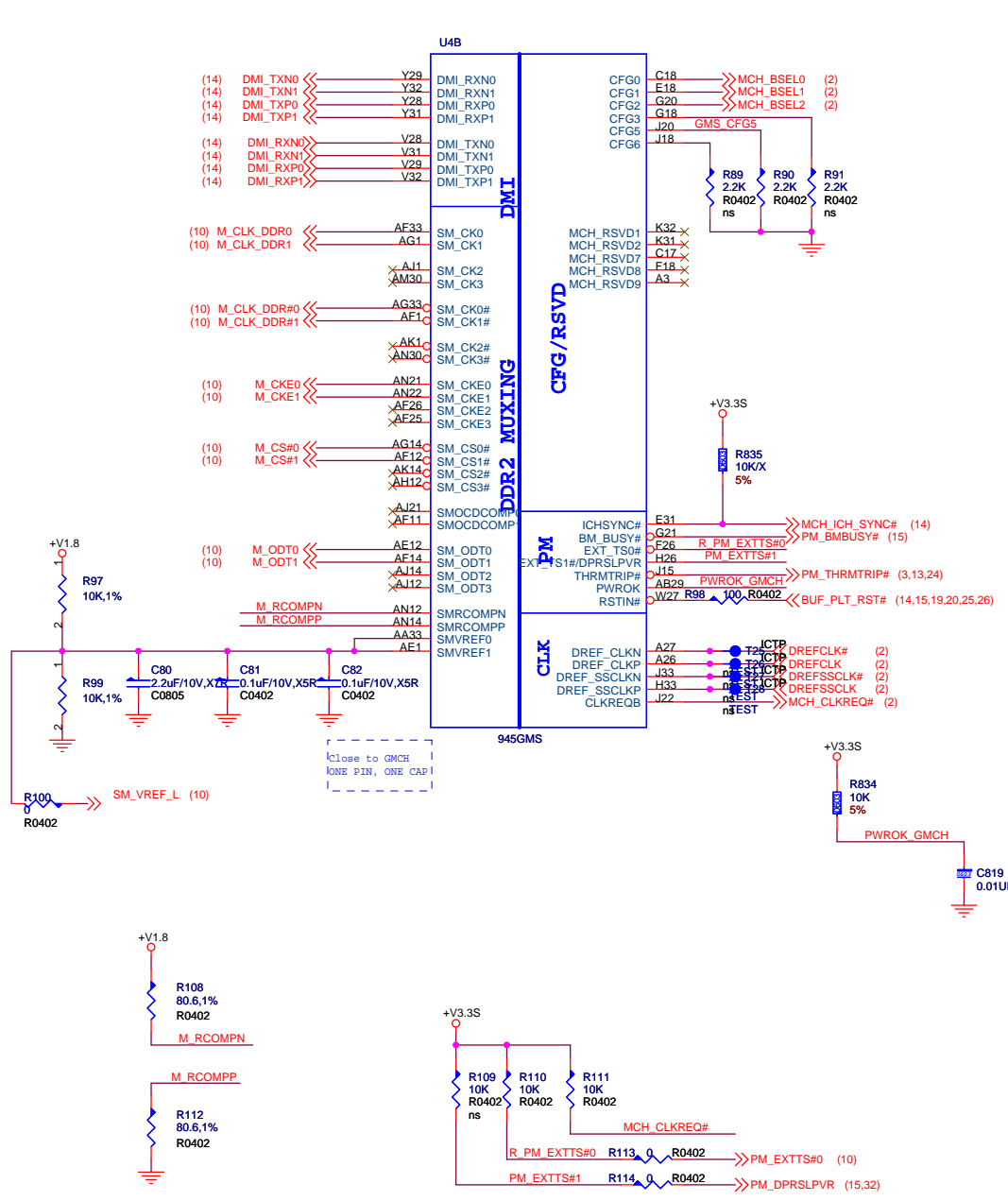


NOTE

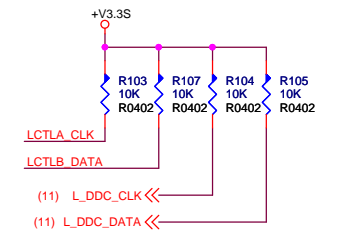
- H_THERMDA/C线宽10 MILS,并配对走线,然后再包地处理.
- H_THERMDA/C走线远离19V及VGA或高速线走线

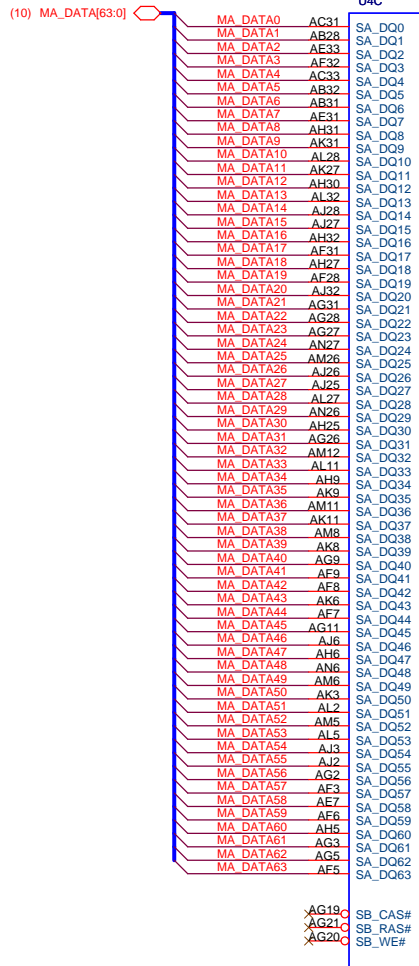






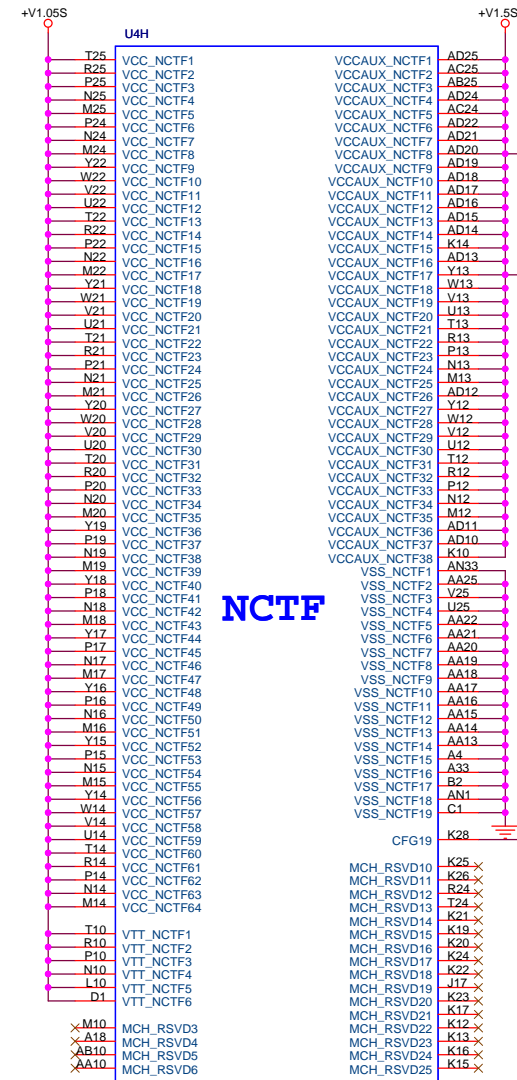
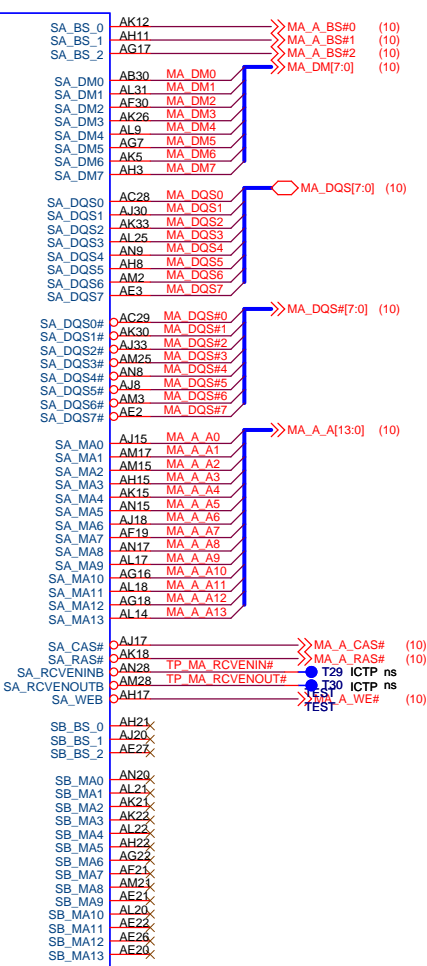
R101 150.1% R0402 CRT_BLUE
 R102 150.1% R0402 CRT_GREEN
 R106 150.1% R0402 CRT_RED
150ohm电阻到GMCH
走线阻抗37.5ohm
150ohm电阻到VGA口
走线阻抗50ohm
PLACE 150 OHM
RESISTORS CLOSE TO
GMCH





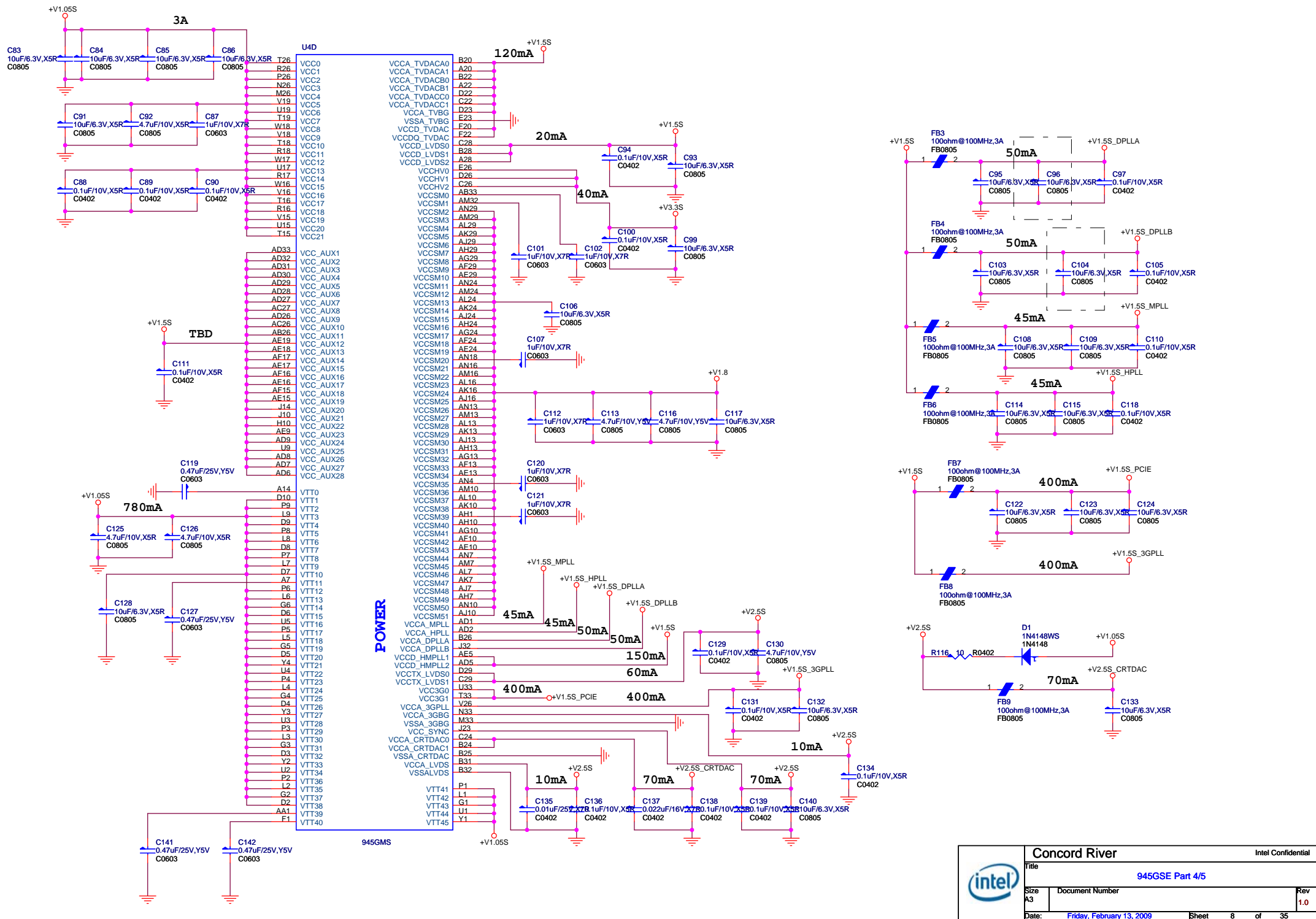
DDR2 SYSTEM MEMORY

945GMS



NCTF

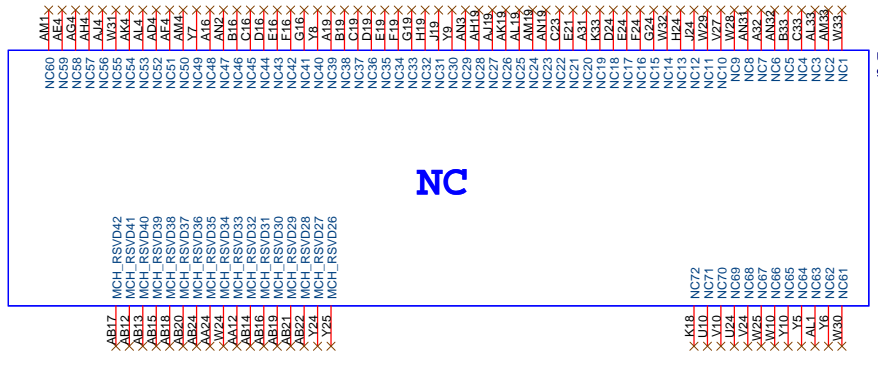
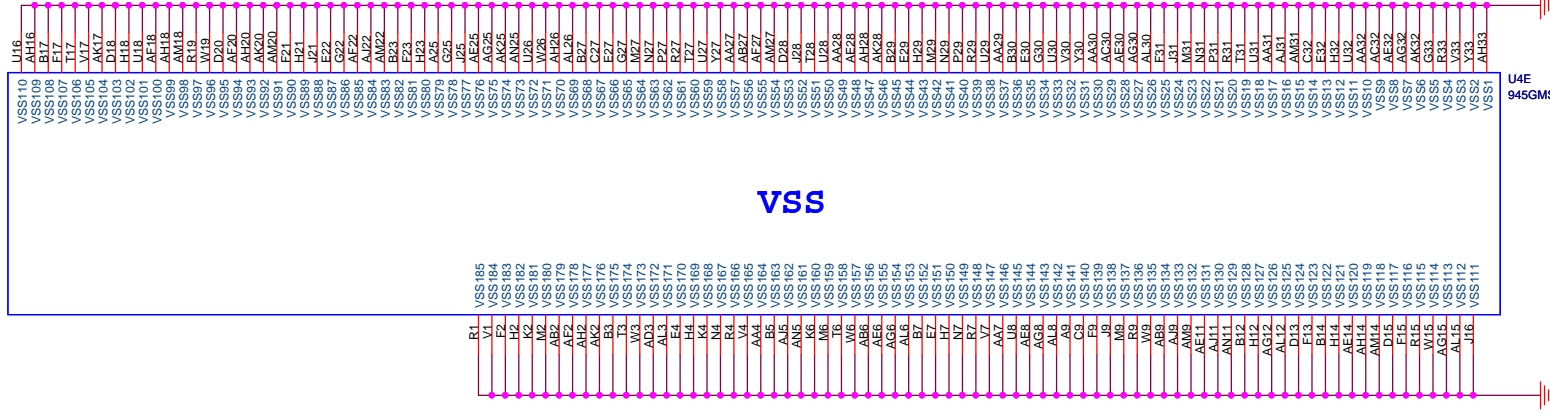
LOW=Normal
High=LANES
REVERSED(945GMS no support.)



POWER

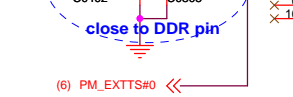
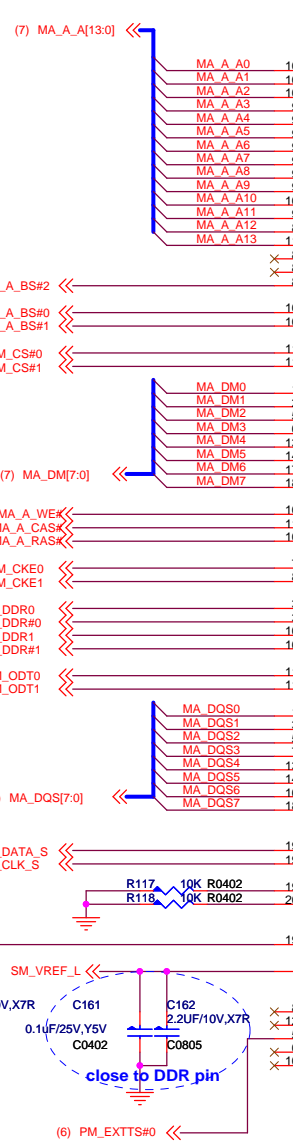
945GMS

		Concord River		Intel Confidential
		Title: 945GSE Part 4/5		
Size: A3	Document Number:			Rev:
Date: Friday, February 13, 2009		Sheet: 8	of 35	

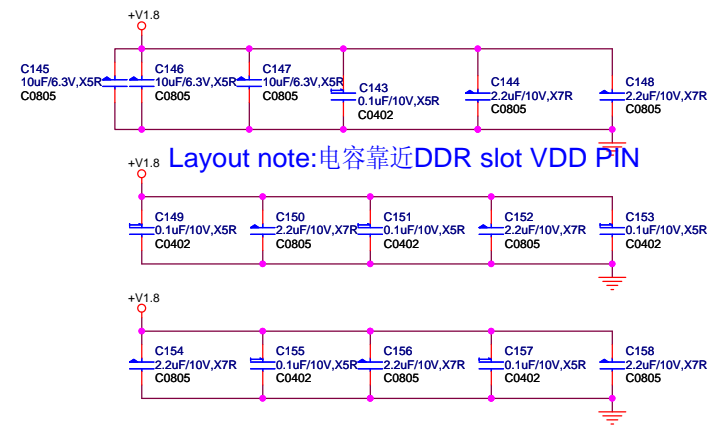




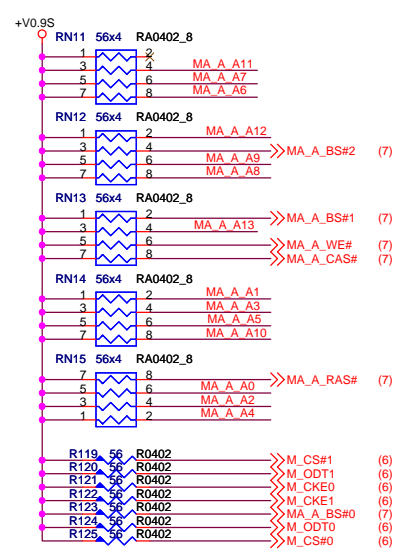
DDR I I

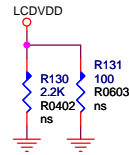
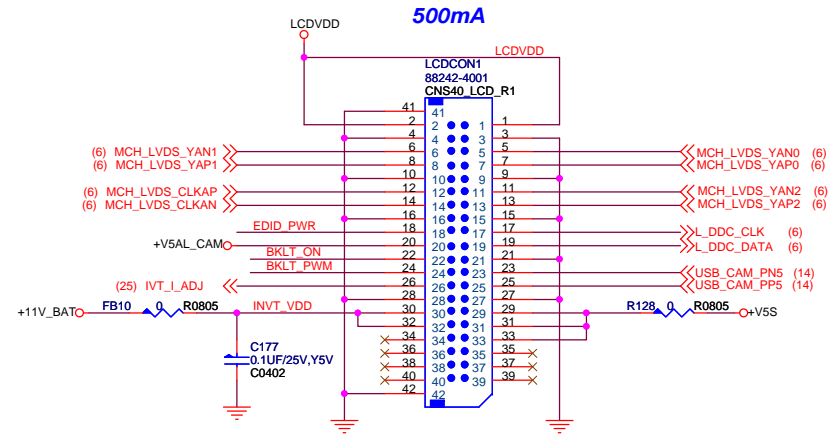
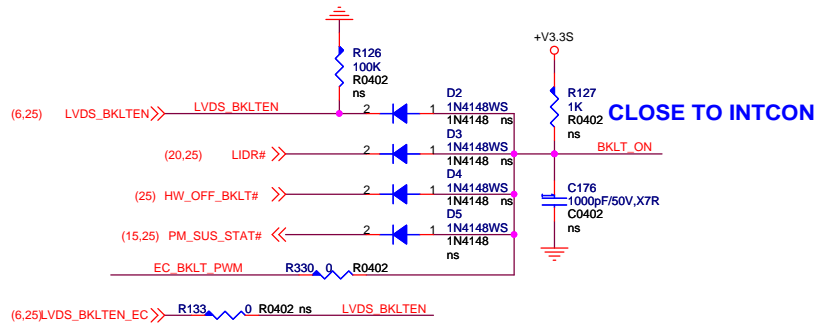


每4个电阻两个0.1UF电容

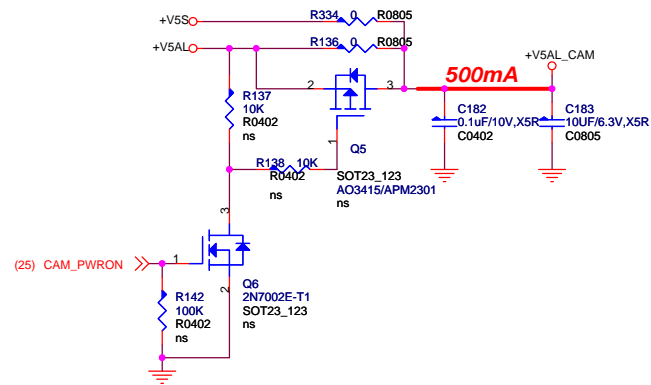
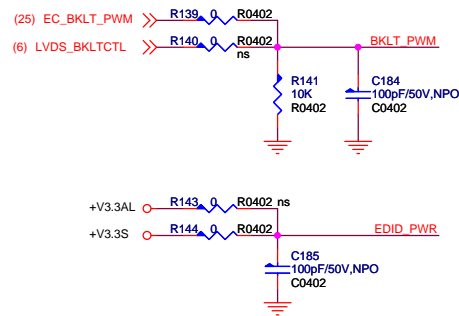


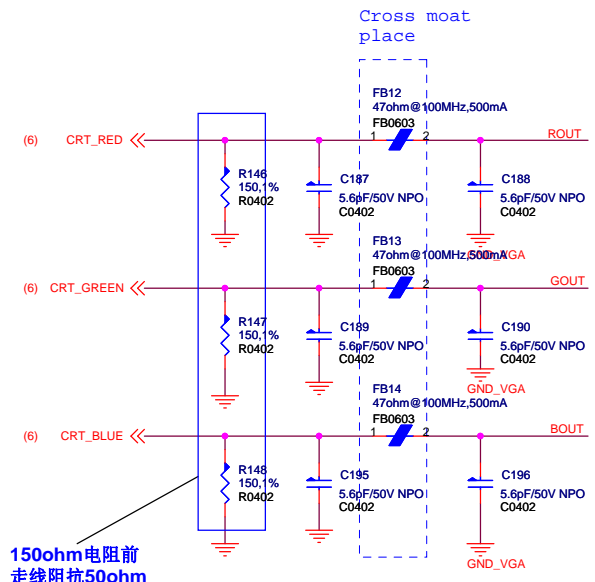
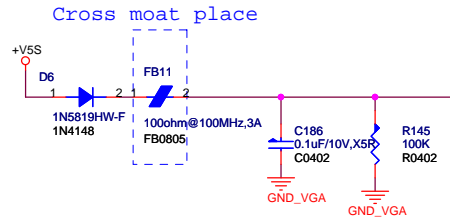
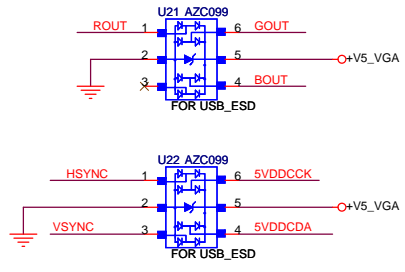
Layout note: 电容靠近DDR slot VDD PIN



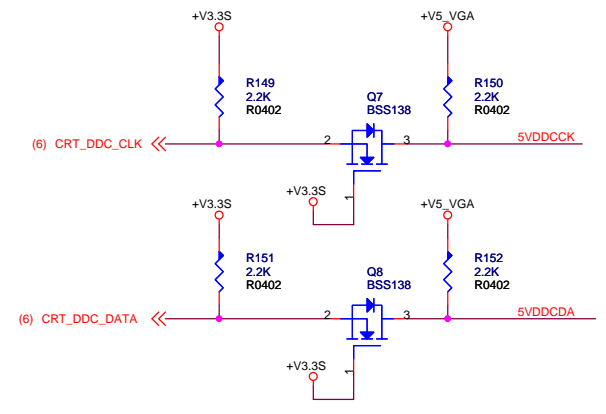
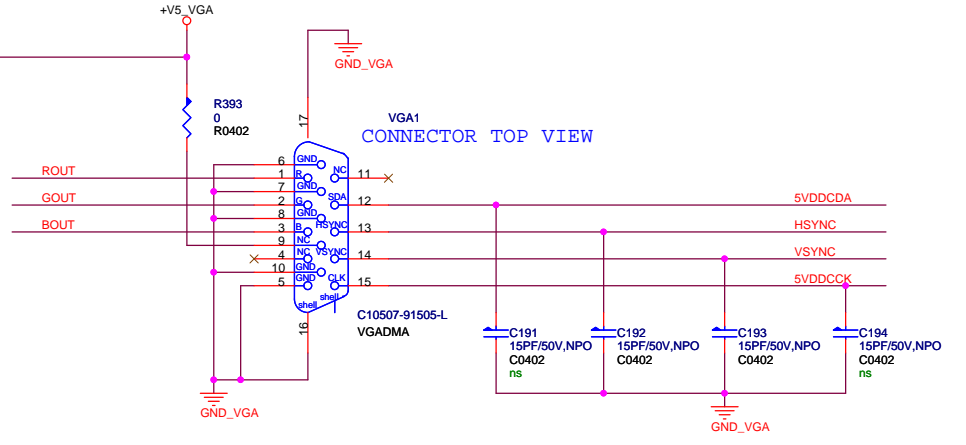
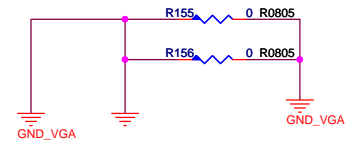


SPWG Require LCDVDD rising time is 0.5-10ms, 1-10ms is better

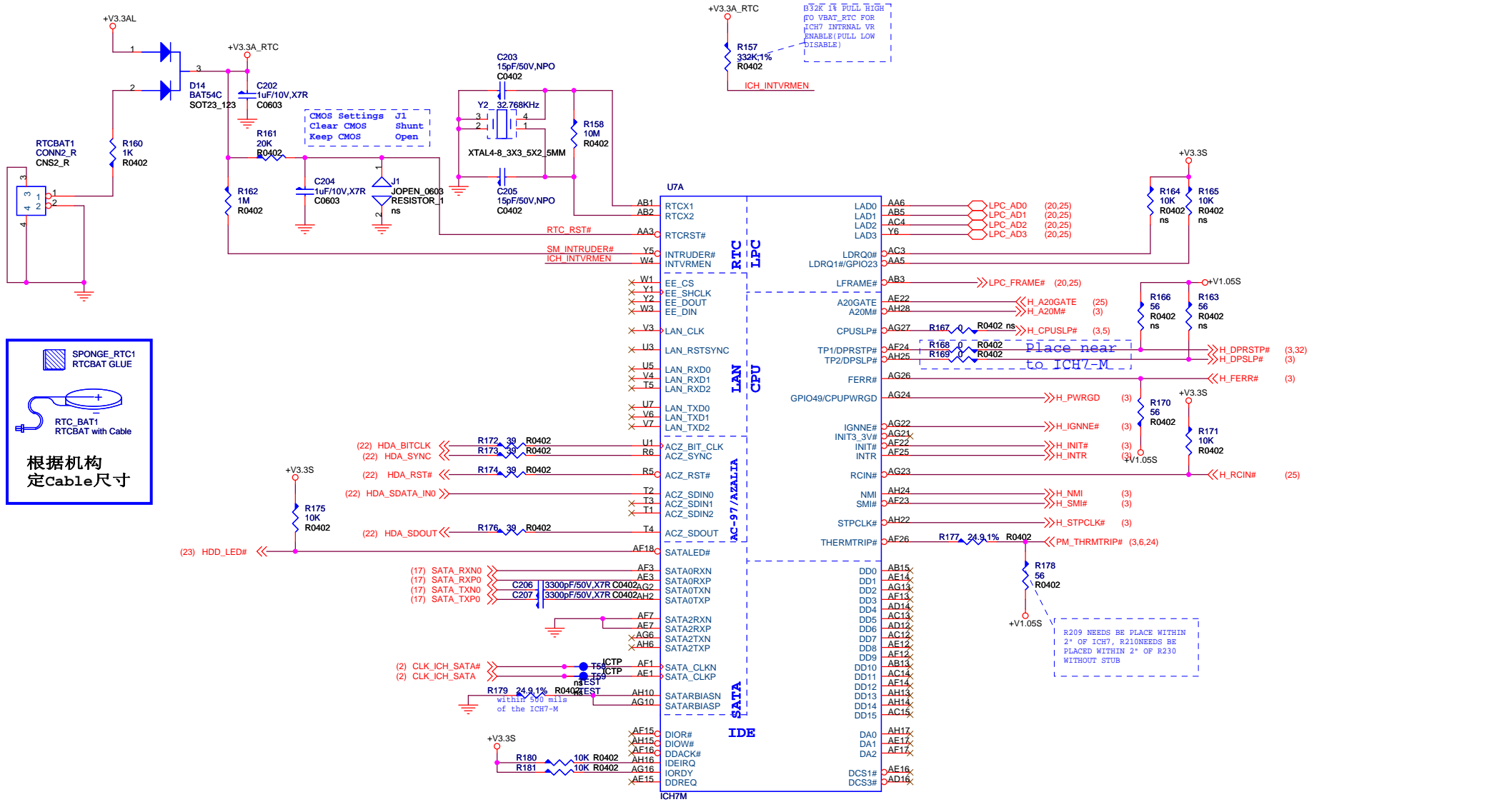




150ohm电阻前走线阻抗50ohm



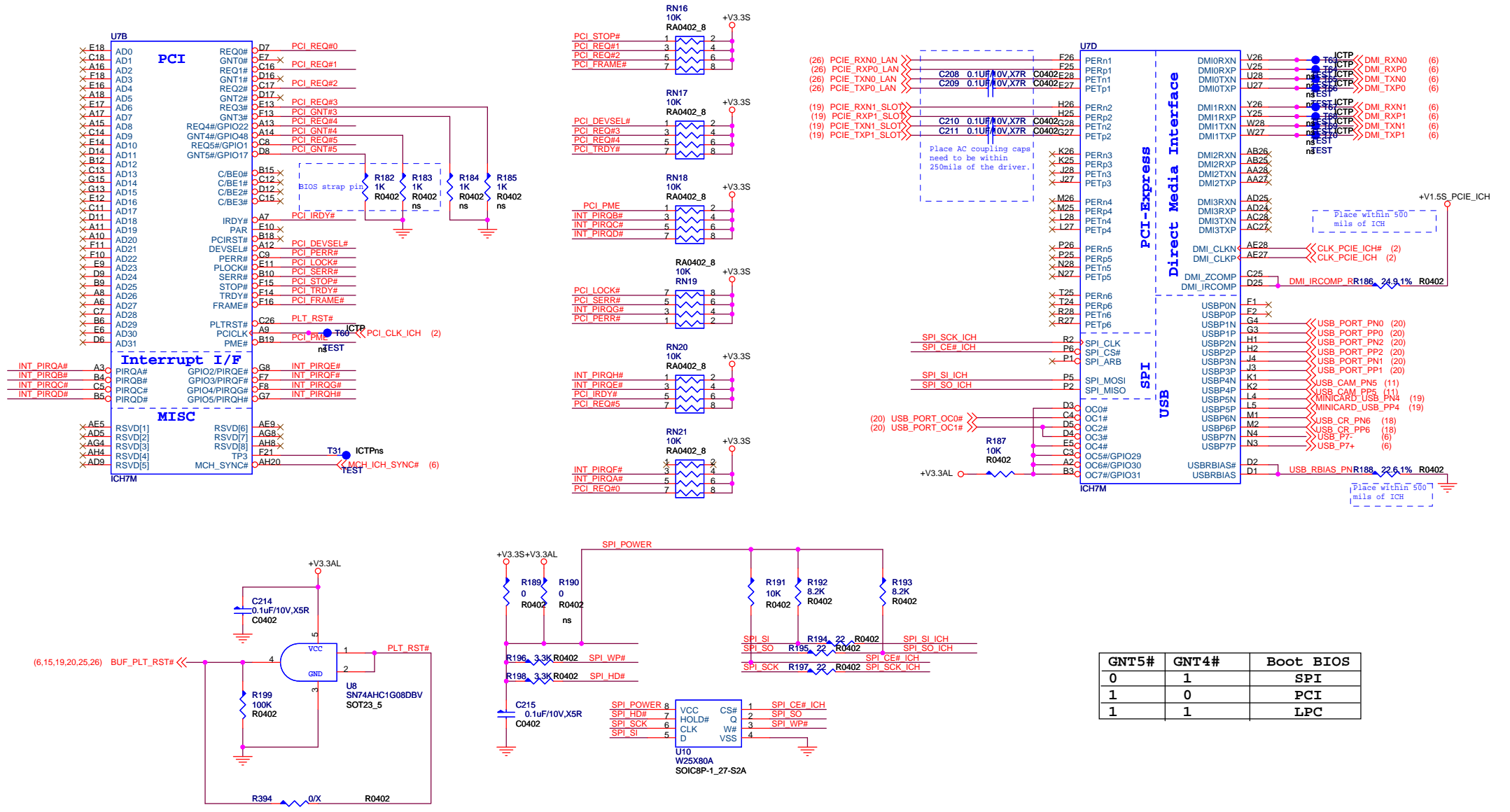
Concord River		Intel Confidential
Title		
VGA Conn.		
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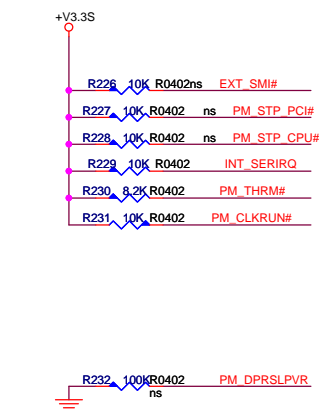
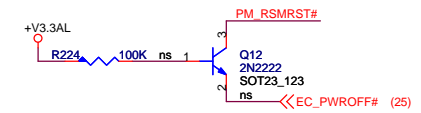
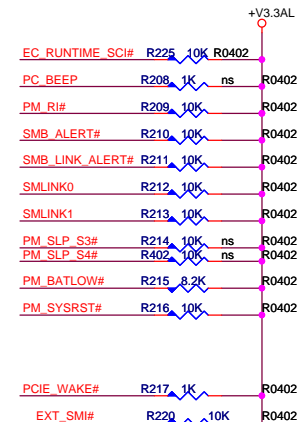
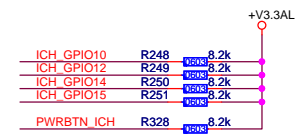
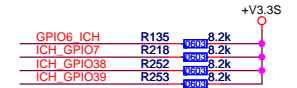
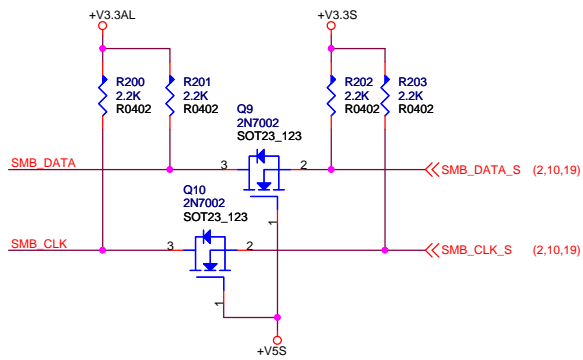
SPONGE_RTC1
RTCBAT GLUE

RTC BAT1
RTCBAT with Cable

**根据机构
定Cable尺寸**



GNT5#	GNT4#	Boot BIOS
0	1	SPI
1	0	PCI
1	1	LPC

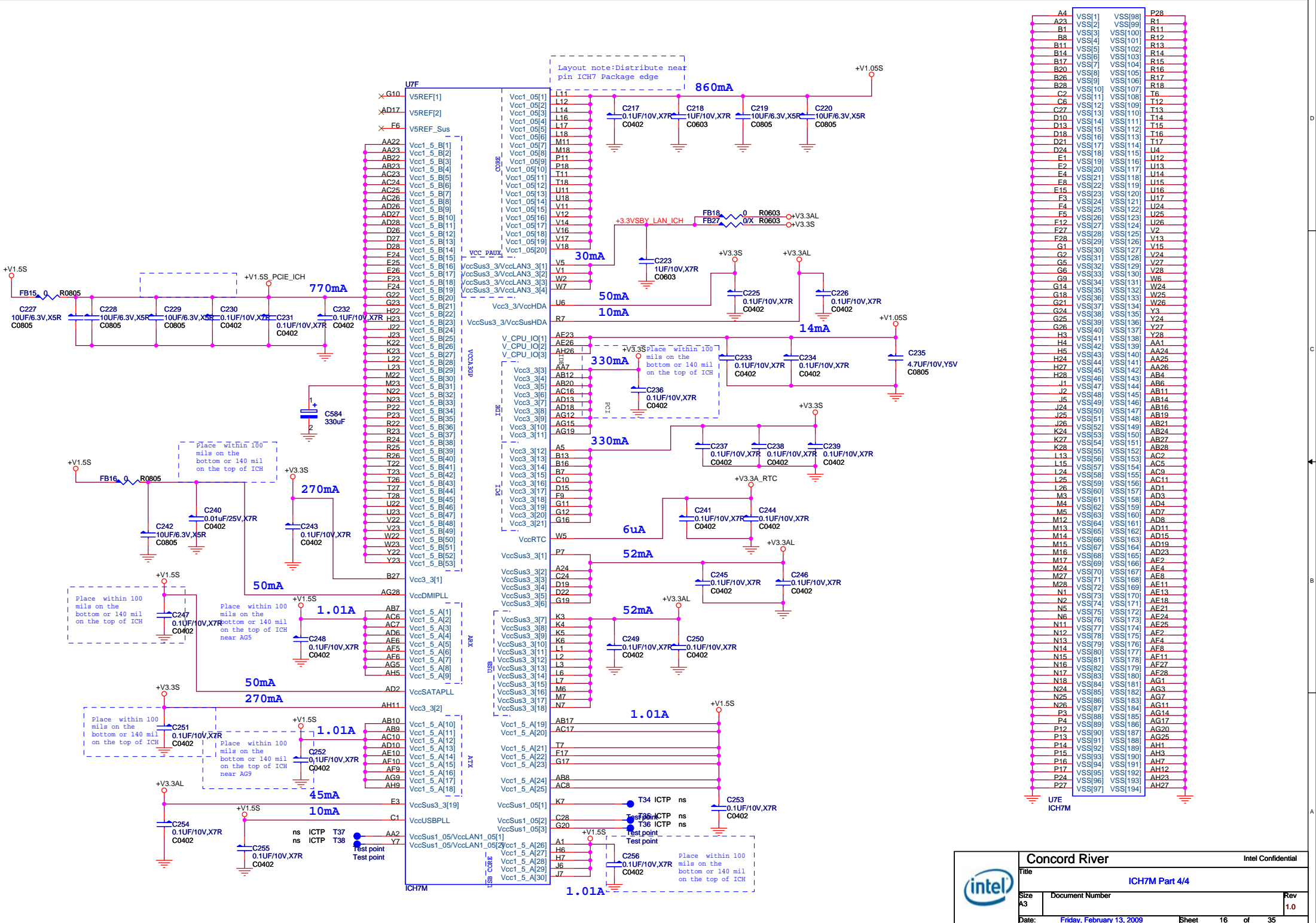


- SMB_CLK C22 SMBCLK
- SMB_DATA B22 SMBDATA
- SMB_LINK_ALERT# A26 LINKALERT#
- SMLINK0 B25 SMLINK0
- SMLINK1 A25 SMLINK1
- PM_RI# A28 RI#
- PC_BEEP A19 SPKR
- PM_SUS_STAT# A27 SUS_STAT#
- PM_SYSRST# A22 SYS_RST#
- PM_BMBUSY# AB18 GPIO0/BM_BUSY#
- SMB_ALERT# B23 GPIO11/SMBALERT#
- PM_STP_PCI# AC20 GPIO18/STPPCI#
- PM_STP_CPU# AE21 GPIO20/STPCPU#
- GPIO26 A21
- GPIO27 B21
- GPIO28 E23
- PM_CLKRUN# AG18 GPIO32/CLKRUN#
- GPIO33/AZ_DOCK_EN# AC19
- GPIO34/AZ_DOCK_RST# U2
- PCIE_WAKE# F20
- INT_SERIRQ (25) AH21
- PM_THRM# AF20 WAKE#
- VR_PWRGD_CLK_EN AD22 VRMPWRGD
- GPIO6 ICH GPIO7 AC21
- ICH_GPIO7 AC18
- EXT_SMI# E21
- GPIO8 ICH7M

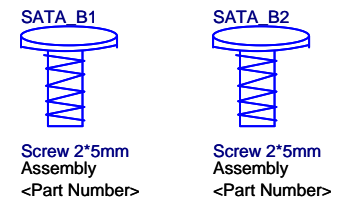
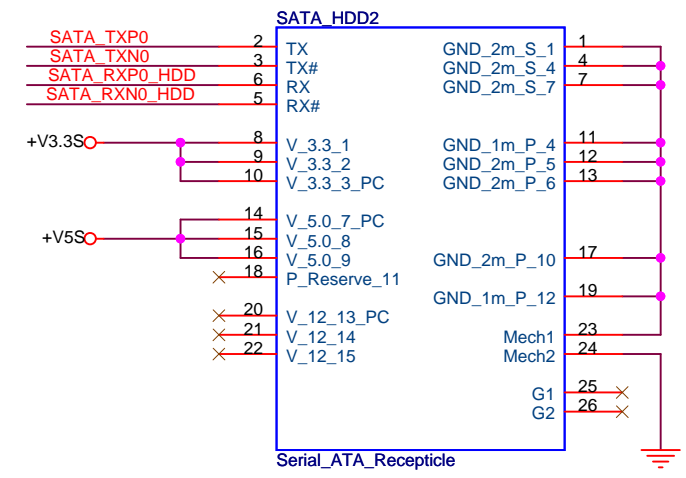
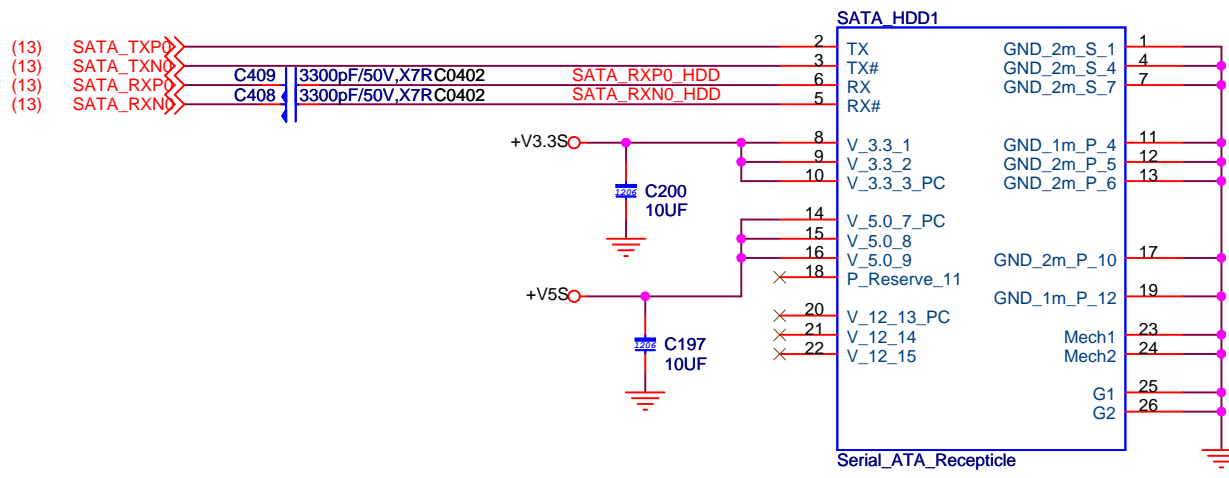
- GPIO21/SATA0GP AF19
- GPIO19/SATA1GP AH18
- GPIO36/SATA2GP AH19
- GPIO37/SATA3GP AE19
- CLK14 AC1
- CLK48 B2
- SUSCLK C20
- SLP_S3# B24
- SLP_S4# D23
- SLP_S5# F22
- PWROK AA4
- GPIO16/DPRSLPVR AC22
- TP0/BATLOW# C21
- PWRBTN# C23
- LAN_RST# C19
- RSMRST# Y4
- GPIO9 E20
- GPIO10 A20
- GPIO12 F19
- GPIO13 R4
- GPIO14 E22
- GPIO15 E22
- GPIO24 R3
- GPIO25 D20
- GPIO35 AD24
- GPIO38 AD20
- GPIO39 AE20

GPIO[0:7,19,21:23,36:39] default is input, if not USE,require PULL-up to VCC3_3.
 GPIO[8:15,29:31] default is input, if not USE,require PULL-up to VccSUS3_3.



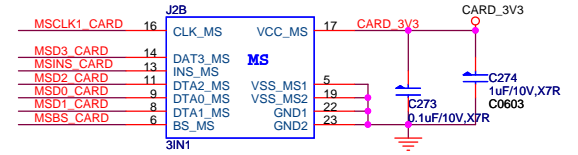
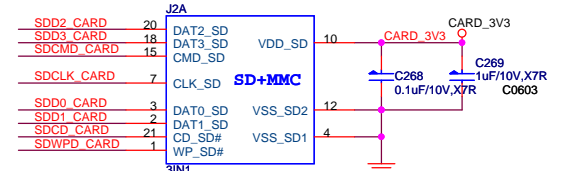
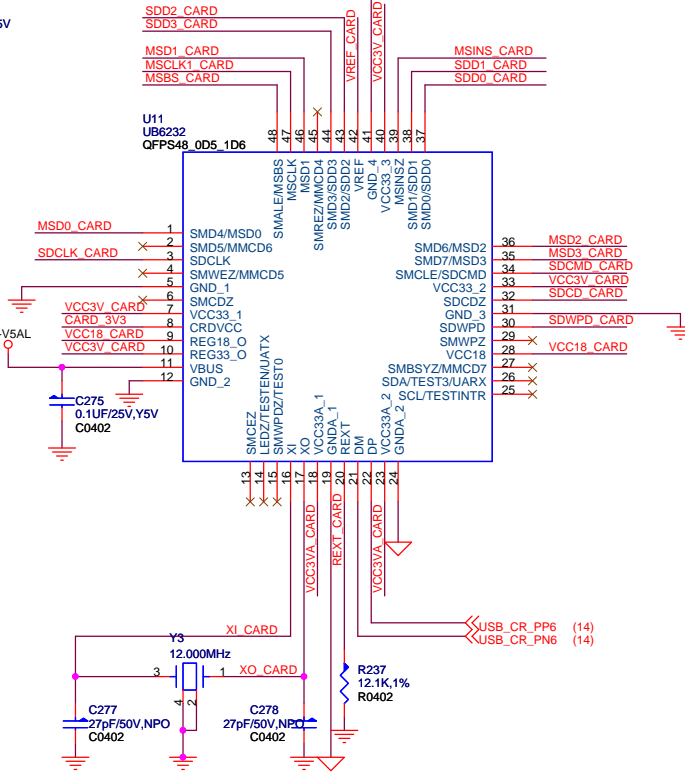
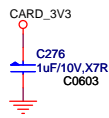
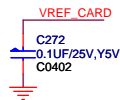
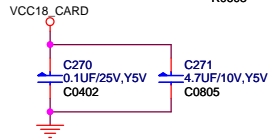
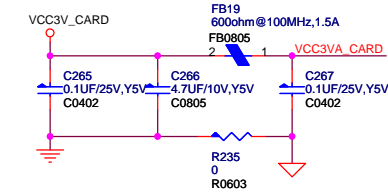


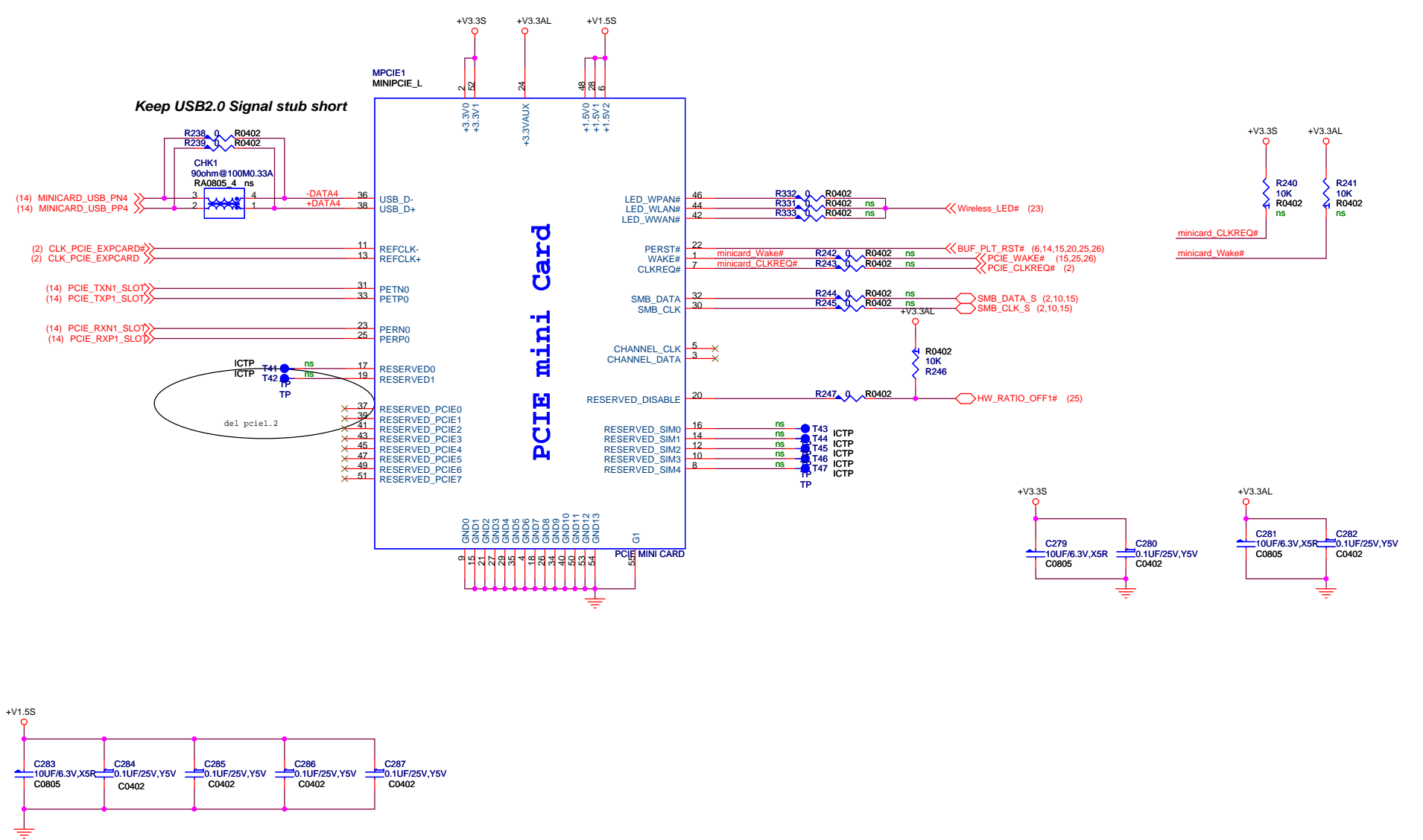
A4	VSS[1]	VSS[98]	P28
A23	VSS[2]	VSS[99]	R1
B1	VSS[3]	VSS[100]	R11
B8	VSS[4]	VSS[101]	R12
B11	VSS[5]	VSS[102]	R13
B14	VSS[6]	VSS[103]	R14
B17	VSS[7]	VSS[104]	R15
B20	VSS[8]	VSS[105]	R16
B26	VSS[9]	VSS[106]	R17
B28	VSS[10]	VSS[107]	R18
C2	VSS[11]	VSS[108]	T6
C6	VSS[12]	VSS[109]	T12
C27	VSS[13]	VSS[110]	T13
D10	VSS[14]	VSS[111]	T14
D13	VSS[15]	VSS[112]	T16
D18	VSS[16]	VSS[113]	T17
D21	VSS[17]	VSS[114]	U4
D24	VSS[18]	VSS[115]	U12
E1	VSS[19]	VSS[116]	U13
E2	VSS[20]	VSS[117]	U14
E4	VSS[21]	VSS[118]	U15
E6	VSS[22]	VSS[119]	U16
F3	VSS[23]	VSS[120]	U17
F4	VSS[24]	VSS[121]	U24
F5	VSS[25]	VSS[122]	U25
F6	VSS[26]	VSS[123]	U26
F12	VSS[27]	VSS[124]	V2
F27	VSS[28]	VSS[125]	V13
F31	VSS[29]	VSS[126]	V15
G1	VSS[30]	VSS[127]	V24
G2	VSS[31]	VSS[128]	V27
G5	VSS[32]	VSS[129]	V28
G6	VSS[33]	VSS[130]	V30
G9	VSS[34]	VSS[131]	W6
G14	VSS[35]	VSS[132]	W24
G18	VSS[36]	VSS[133]	W25
G21	VSS[37]	VSS[134]	W26
G24	VSS[38]	VSS[135]	Y3
G25	VSS[39]	VSS[136]	Y24
G26	VSS[40]	VSS[137]	Y27
H3	VSS[41]	VSS[138]	Y28
H4	VSS[42]	VSS[139]	Y29
H5	VSS[43]	VSS[140]	AA1
H24	VSS[44]	VSS[141]	AA25
H27	VSS[45]	VSS[142]	AA26
H28	VSS[46]	VSS[143]	AB4
J1	VSS[47]	VSS[144]	AB6
J2	VSS[48]	VSS[145]	AB14
J5	VSS[49]	VSS[146]	AB16
J24	VSS[50]	VSS[147]	AB19
J25	VSS[51]	VSS[148]	AB21
J26	VSS[52]	VSS[149]	AB22
K24	VSS[53]	VSS[150]	AB27
K27	VSS[54]	VSS[151]	AB28
K28	VSS[55]	VSS[152]	AC2
L13	VSS[56]	VSS[153]	AC5
L15	VSS[57]	VSS[154]	AC9
L24	VSS[58]	VSS[155]	AC11
L25	VSS[59]	VSS[156]	AD1
L26	VSS[60]	VSS[157]	AD3
M3	VSS[61]	VSS[158]	AD4
M4	VSS[62]	VSS[159]	AD7
M5	VSS[63]	VSS[160]	AD8
M12	VSS[64]	VSS[161]	AD15
M13	VSS[65]	VSS[162]	AD11
M14	VSS[66]	VSS[163]	AD19
M15	VSS[67]	VSS[164]	AD23
M16	VSS[68]	VSS[165]	AE2
M17	VSS[69]	VSS[166]	AE4
M24	VSS[70]	VSS[167]	AE8
M27	VSS[71]	VSS[168]	AE11
M28	VSS[72]	VSS[169]	AE13
N1	VSS[73]	VSS[170]	AE18
N2	VSS[74]	VSS[171]	AE21
N5	VSS[75]	VSS[172]	AF14
N6	VSS[76]	VSS[173]	AF25
N11	VSS[77]	VSS[174]	AF2
N12	VSS[78]	VSS[175]	AF27
N13	VSS[79]	VSS[176]	AF4
N14	VSS[80]	VSS[177]	AF8
N15	VSS[81]	VSS[178]	AF11
N16	VSS[82]	VSS[179]	AF22
N17	VSS[83]	VSS[180]	AF28
N18	VSS[84]	VSS[181]	AG1
N24	VSS[85]	VSS[182]	AG3
N25	VSS[86]	VSS[183]	AG7
N26	VSS[87]	VSS[184]	AG11
P3	VSS[88]	VSS[185]	AG14
P4	VSS[89]	VSS[186]	AG17
P12	VSS[90]	VSS[187]	AG20
P13	VSS[91]	VSS[188]	AG25
P14	VSS[92]	VSS[189]	AH1
P15	VSS[93]	VSS[190]	AH3
P16	VSS[94]	VSS[191]	AH7
P17	VSS[95]	VSS[192]	AH12
P24	VSS[96]	VSS[193]	AH23
P27	VSS[97]	VSS[194]	AH27



SATA HDD

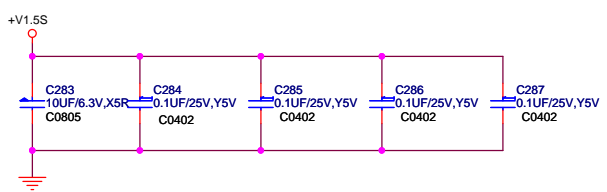
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	Date: Friday, February 13, 2009	Sheet 17 of 35		

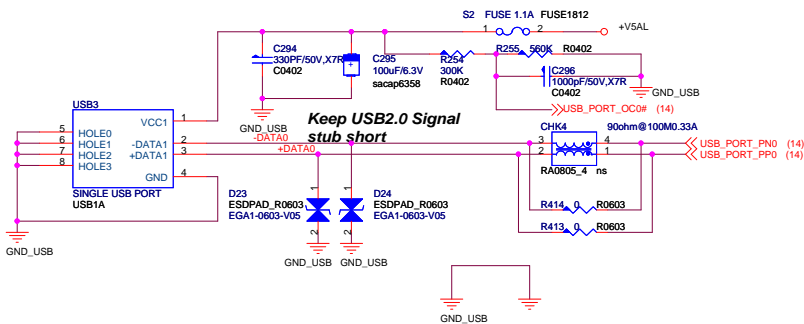
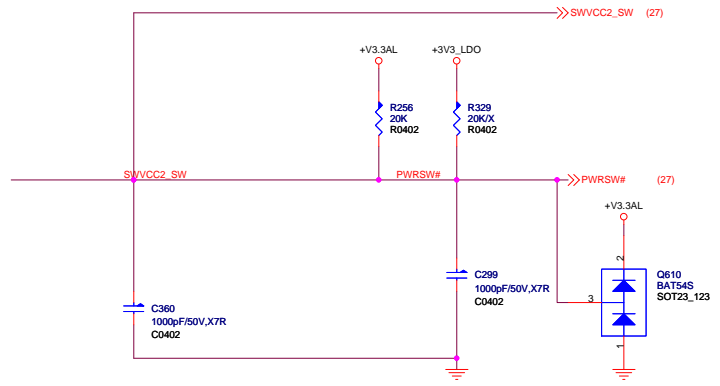
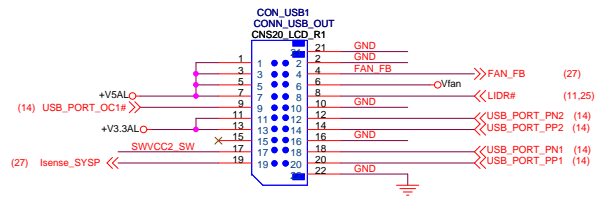
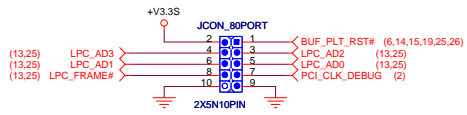


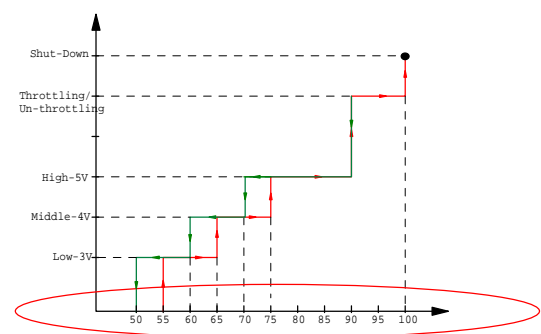
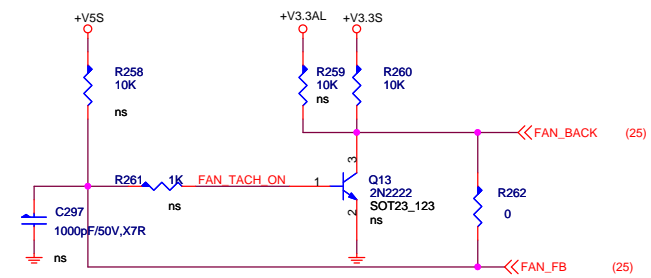
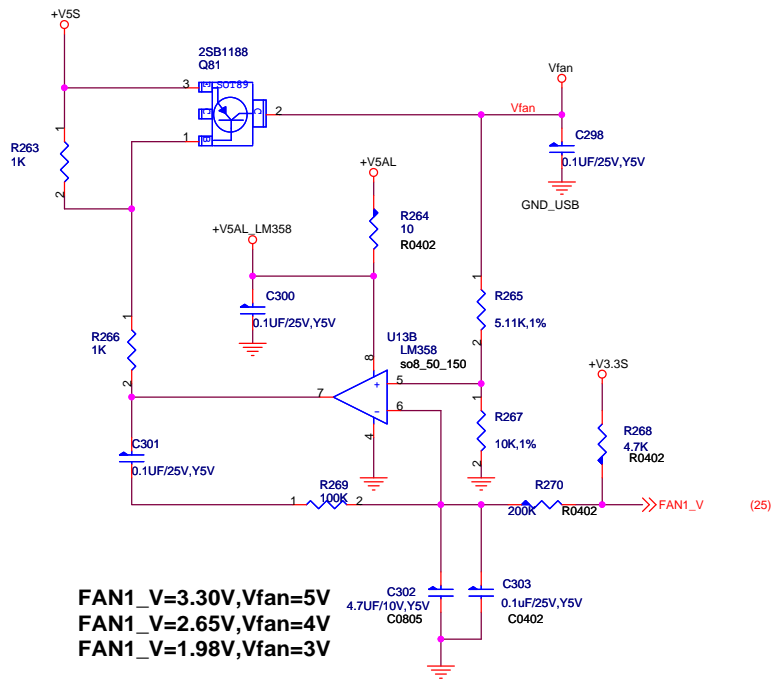


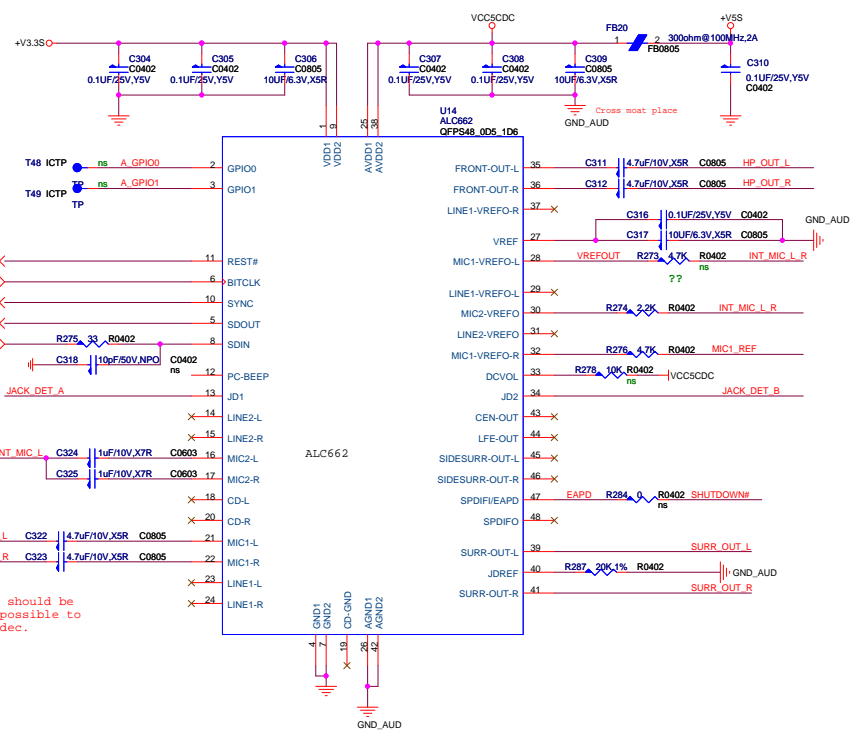
Keep USB2.0 Signal stub short

PCIE mini Card







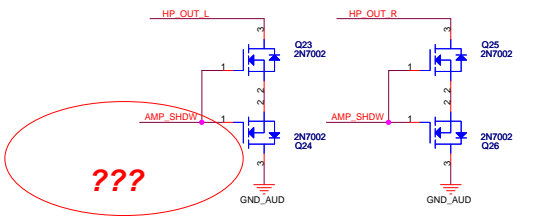
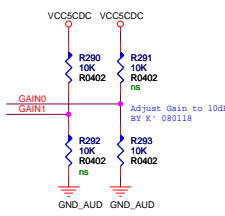


- (13) HDA_RST#
- (13) HDA_BITCLK
- (13) HDA_SYNC
- (13) HDA_SDOUT
- (13) HDA_SDATA_IN0

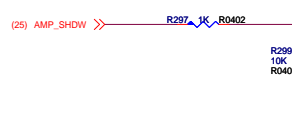
update internal MIC circuit
 Layout Note:
 All of JD resistors should be placed as close as possible to the sense pin of codec.

GAIN0	GAIN1	Av(inv)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

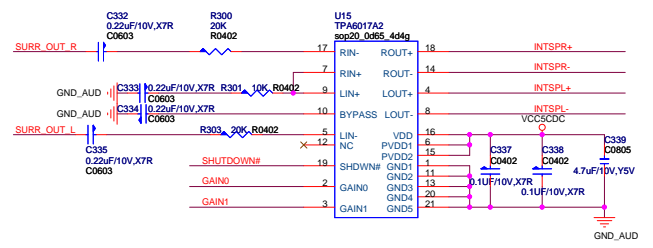
REMOVE SHUTDOWN#



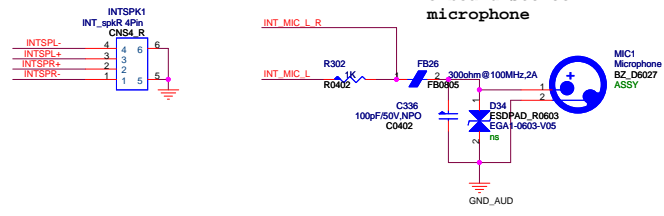
De-pop Solution



Onboard Amp

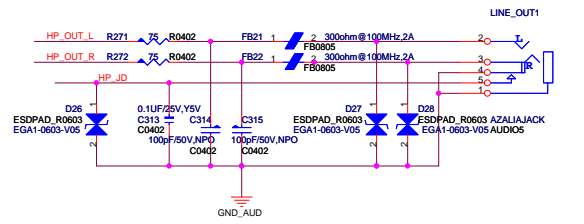


onboard stereo microphone



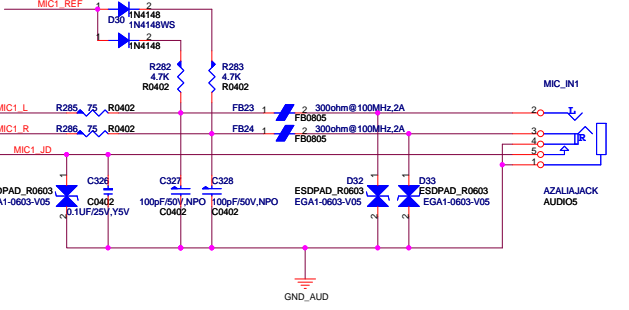
Headphone Jack

INPUT: HEADPHONE/LINE-OUT
 OUTPUT: FRONT L/R

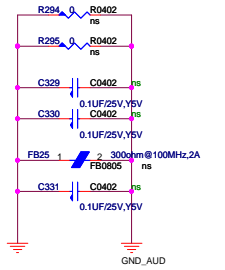


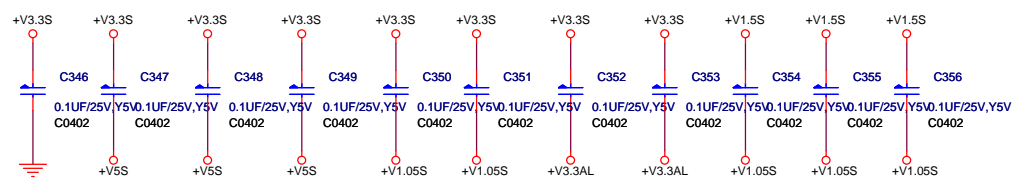
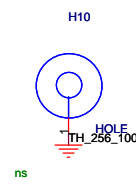
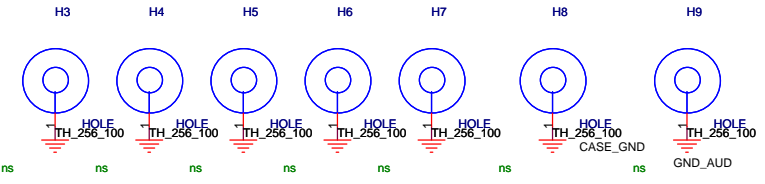
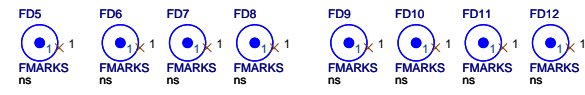
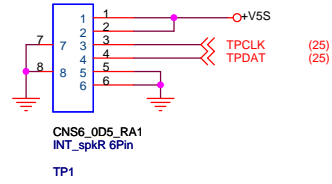
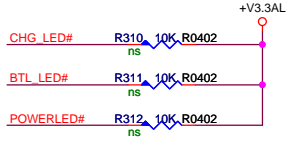
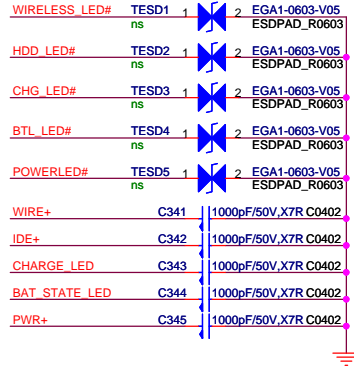
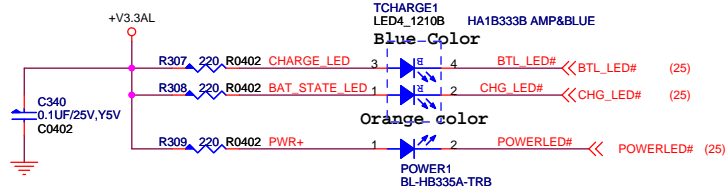
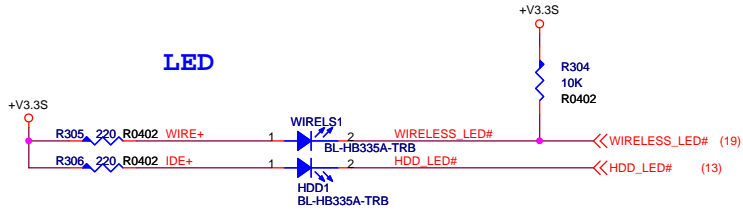
Stereo Microphone Jack

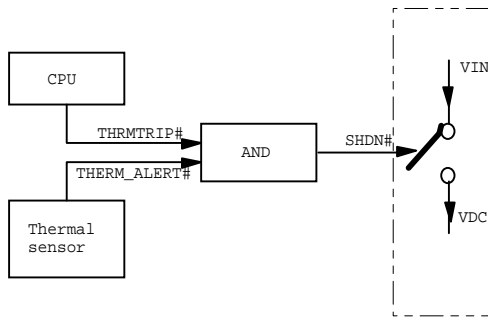
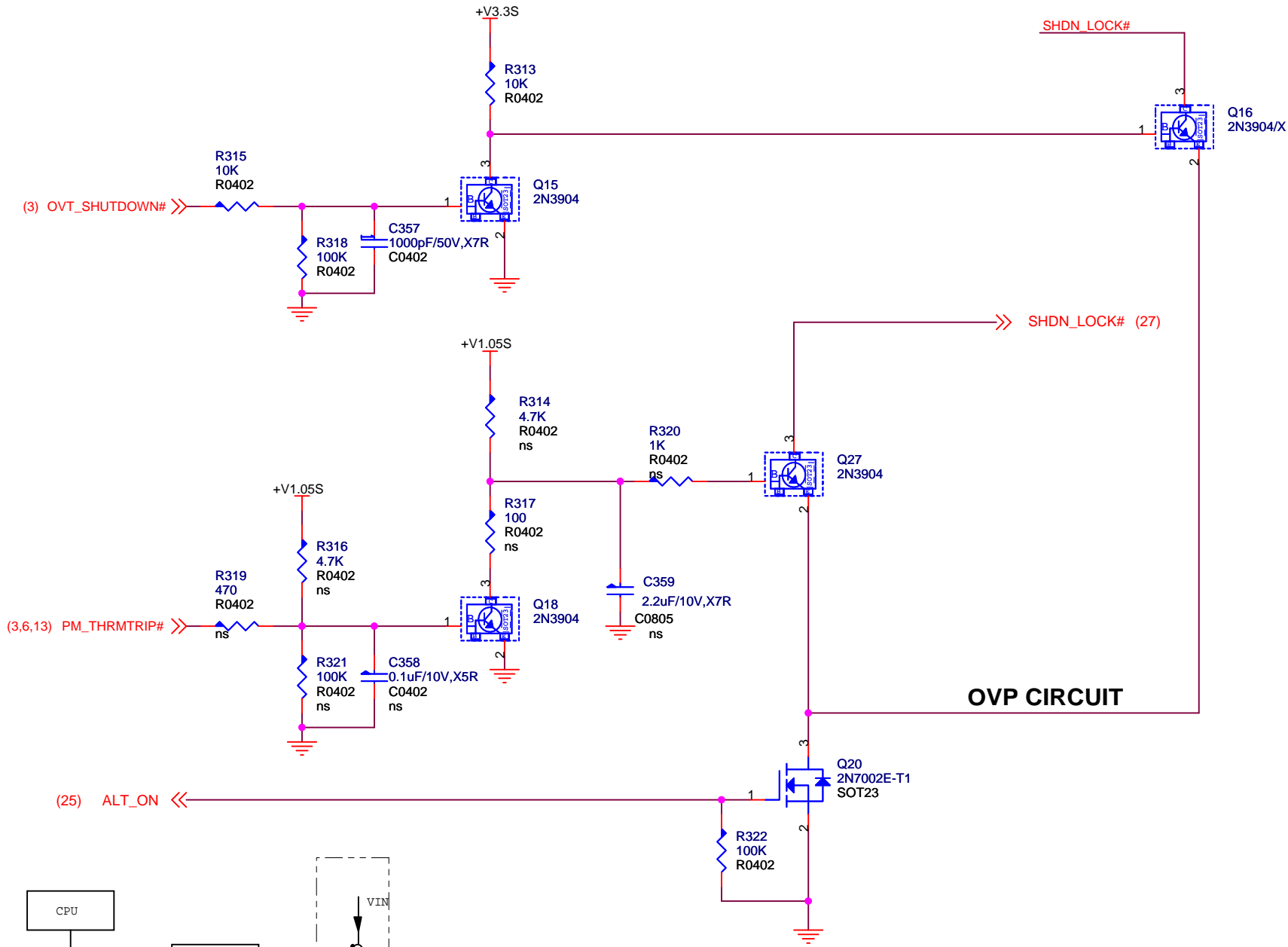
INPUT: STEREO MIC-IN
 OUTPUT: CENT/LFE



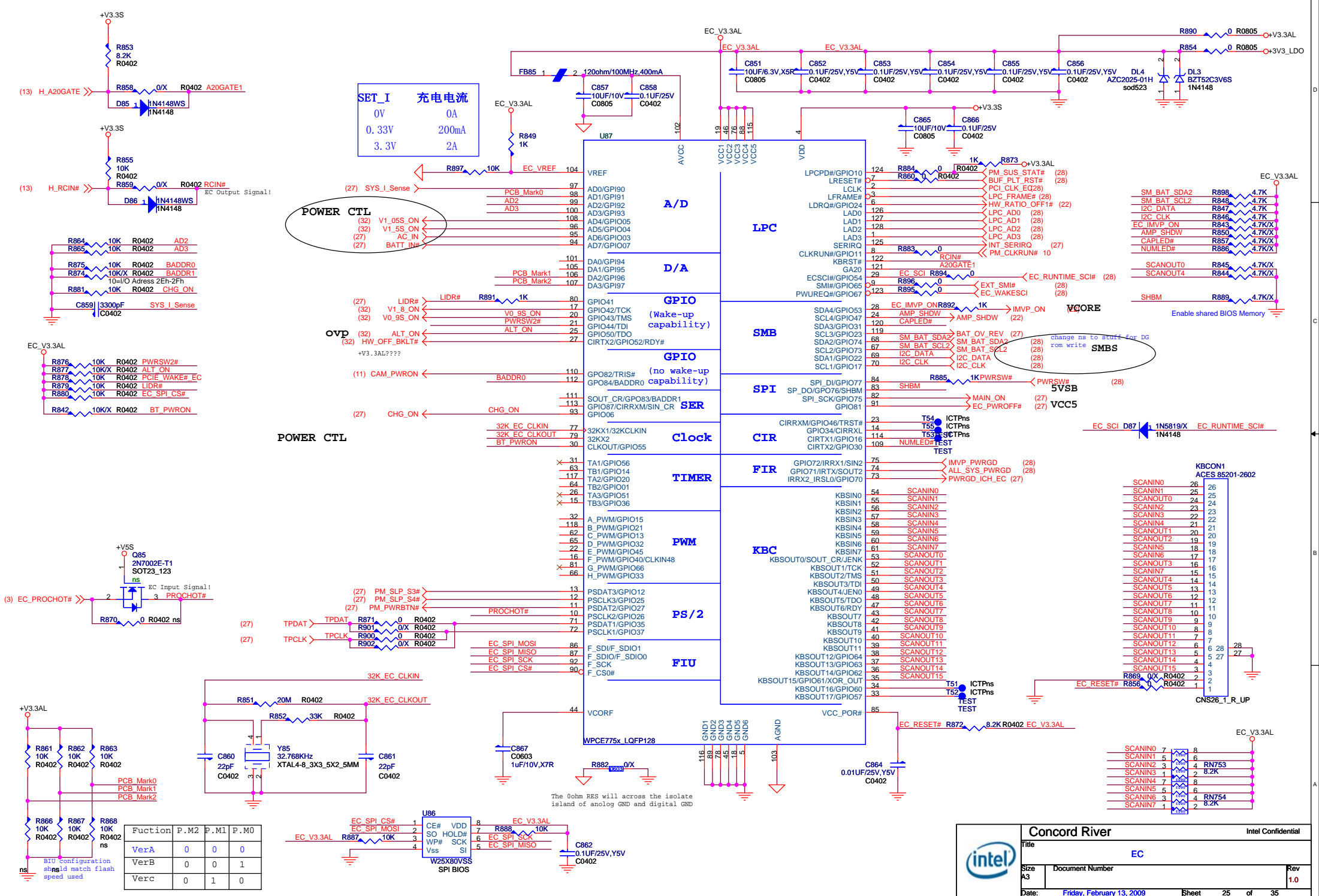
Layout Note:
 Tied at three points under the codec and near the codec







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		Title: OVP Protection.		
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SET_I 充电电流

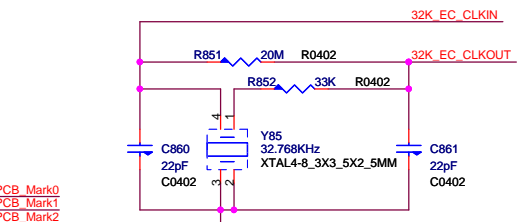
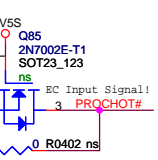
0V	0A
0.33V	200mA
3.3V	2A

POWER CTL

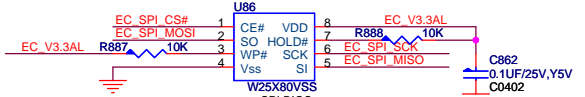
V1_05S_ON (32)
V1_5S_ON (32)
AC_IN (27)
BATT_IN# (27)

POWER CTL

LIDR# (27)
V1_8_ON (32)
V1_9S_ON (32)
PWRSW# (27)
ALT_ON (32)
HW_OFF_BKLT# (32)
+V3.3AL????



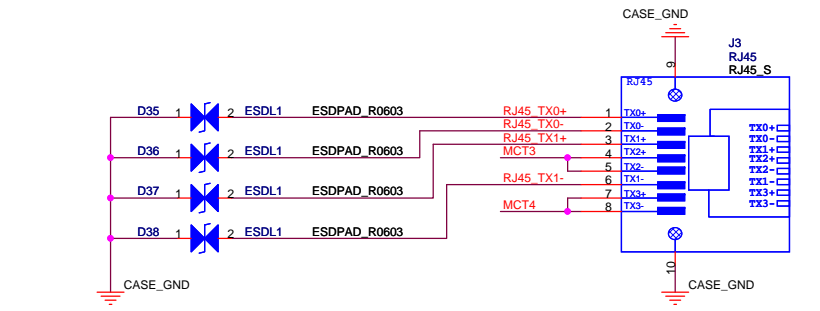
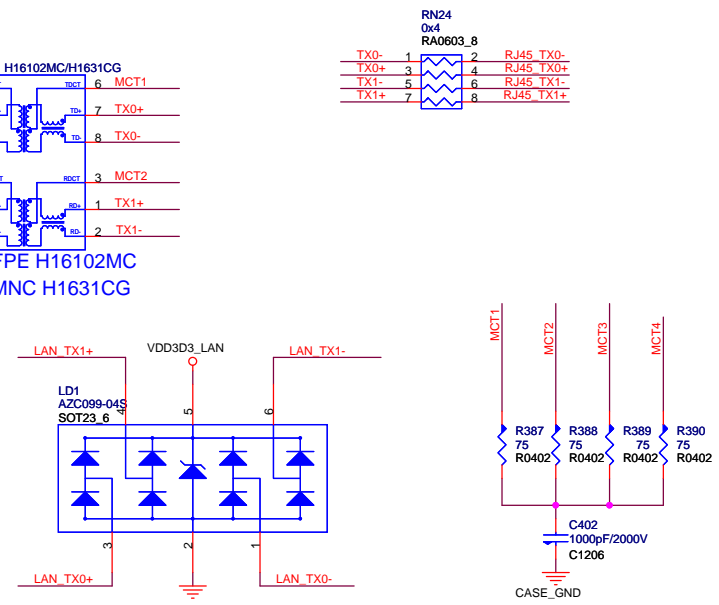
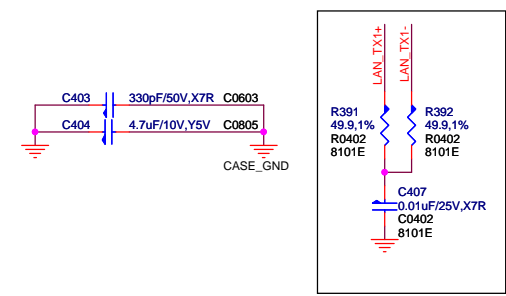
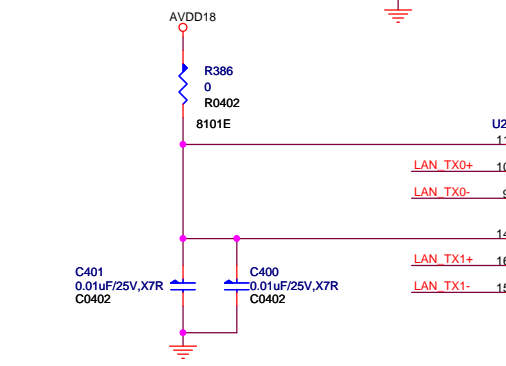
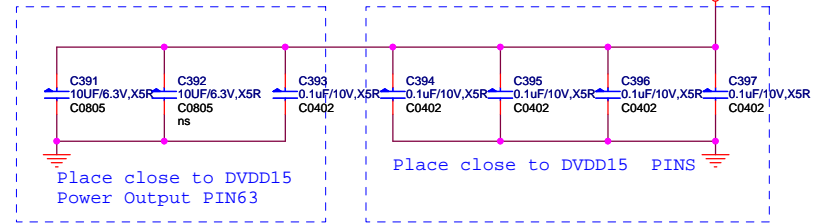
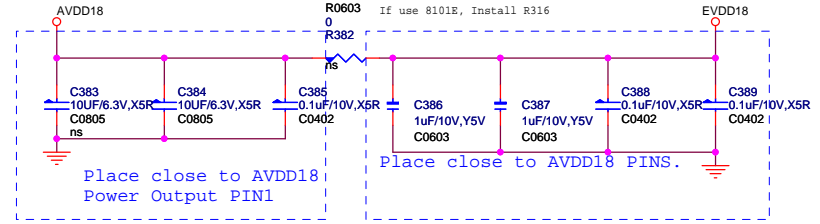
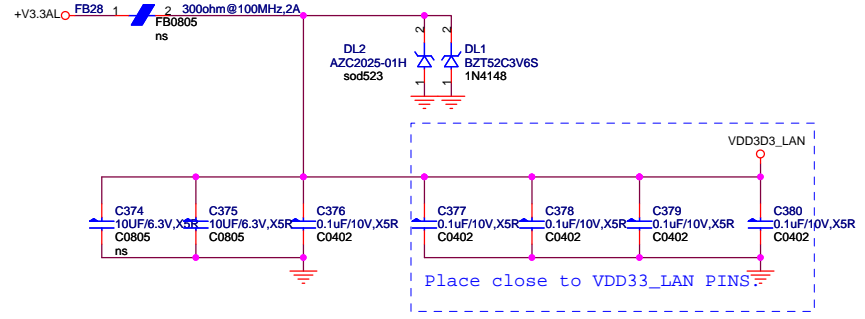
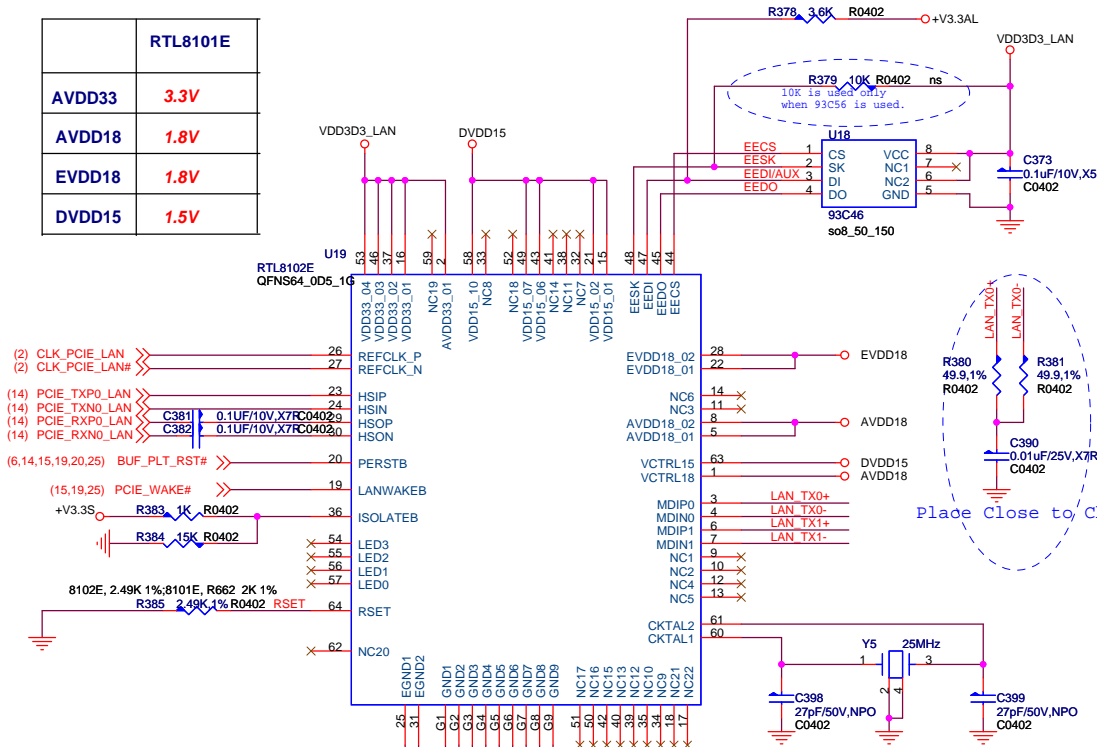
Fuction	P.M2	P.M1	P.M0
VerA	0	0	0
VerB	0	0	1
VerC	0	1	0

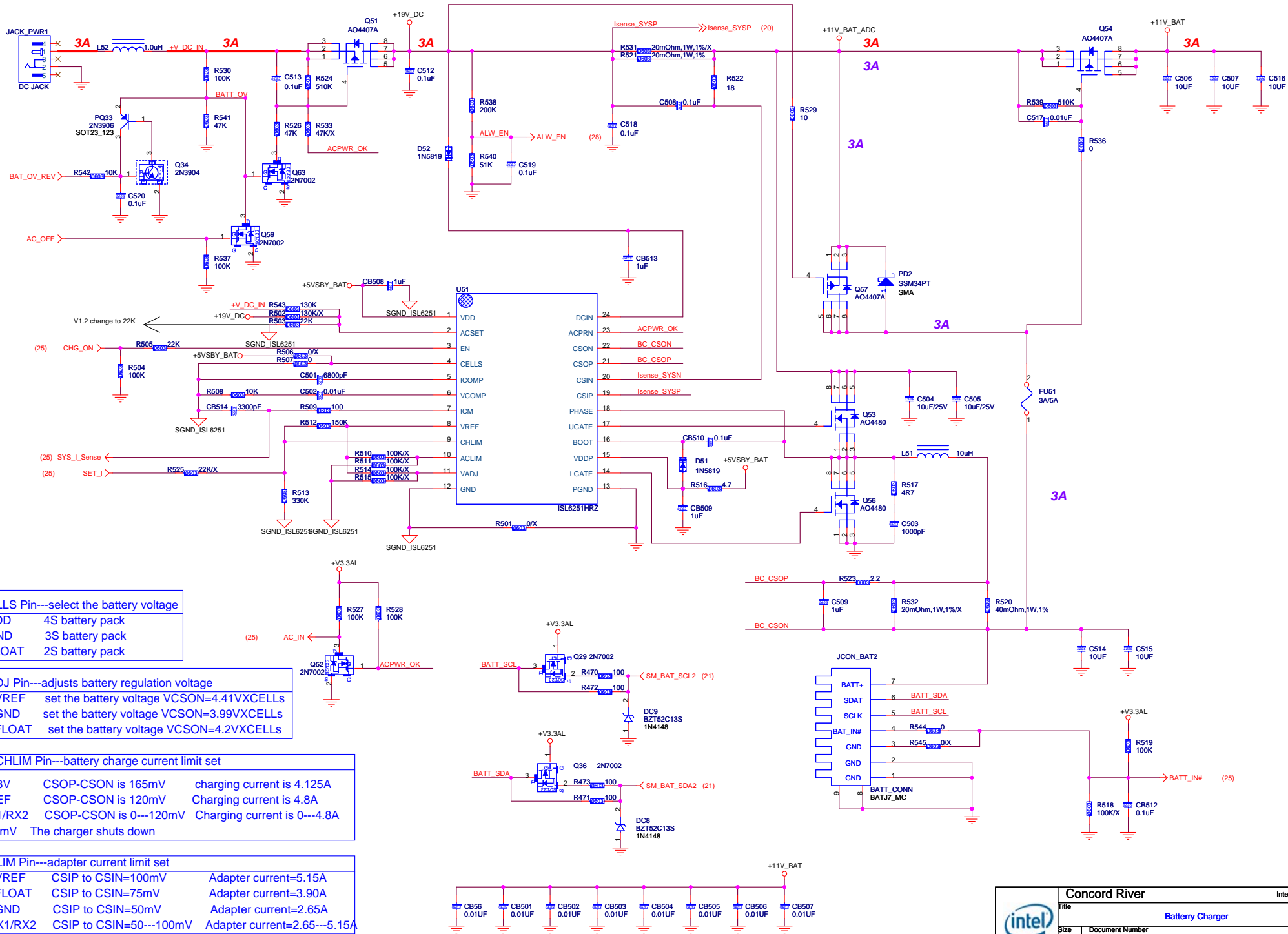


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		EC		
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Power domain chart

	RTL8101E
AVDD33	3.3V
AVDD18	1.8V
EVDD18	1.8V
DVDD15	1.5V





CELLS Pin---select the battery voltage
 =VDD 4S battery pack
 =GND 3S battery pack
 =FLOAT 2S battery pack

VADJ Pin---adjusts battery regulation voltage
 =VREF set the battery voltage VCSON=4.41VXCCELLS
 =GND set the battery voltage VCSON=3.99VXCCELLS
 =FLOAT set the battery voltage VCSON=4.2VXCCELLS

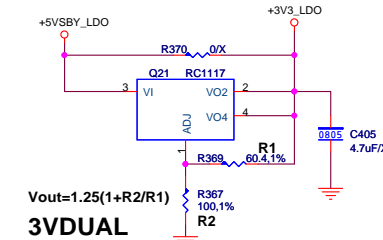
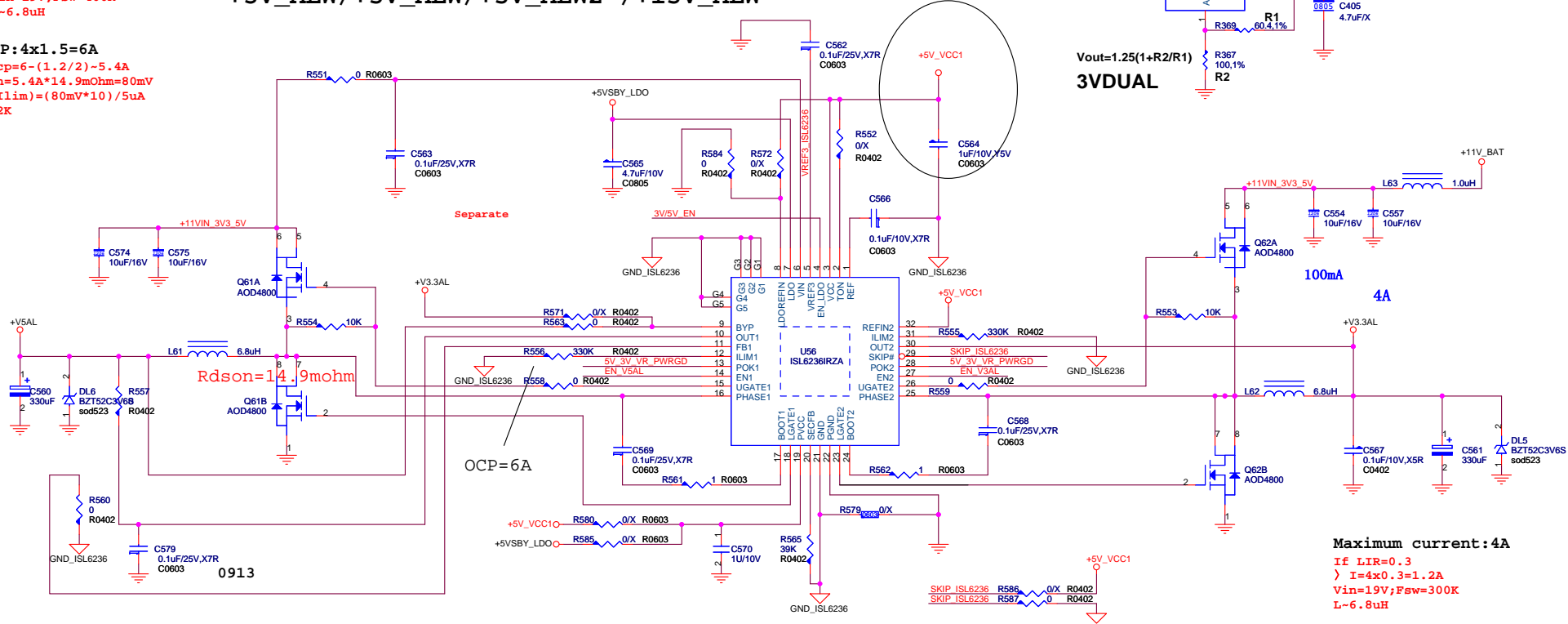
CHLIM Pin---battery charge current limit set
 =3.3V CSOP-CSON is 165mV charging current is 4.125A
 VREF CSOP-CSON is 120mV Charging current is 4.8A
 RX1/RX2 CSOP-CSON is 0---120mV Charging current is 0---4.8A
 <88mV The charger shuts down

ACLIM Pin---adapter current limit set
 =VREF CSIP to CSIN=100mV Adapter current=5.15A
 =FLOAT CSIP to CSIN=75mV Adapter current=3.90A
 =GND CSIP to CSIN=50mV Adapter current=2.65A
 RX1/RX2 CSIP to CSIN=50---100mV Adapter current=2.65---5.15A

Maximum current:4A
 If LIR=0.3
 > I=4x0.3=1.2A
 Vin=19V;Fsw=400K
 L=6.8uH

OCP:4x1.5=6A
 Iocp=6-(1.2/2)-5.4A
 Vth=5.4A*14.9mOhm=80mV
 R(Ilim)=(80mV*10)/5uA
 162K

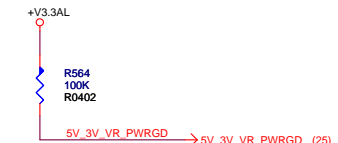
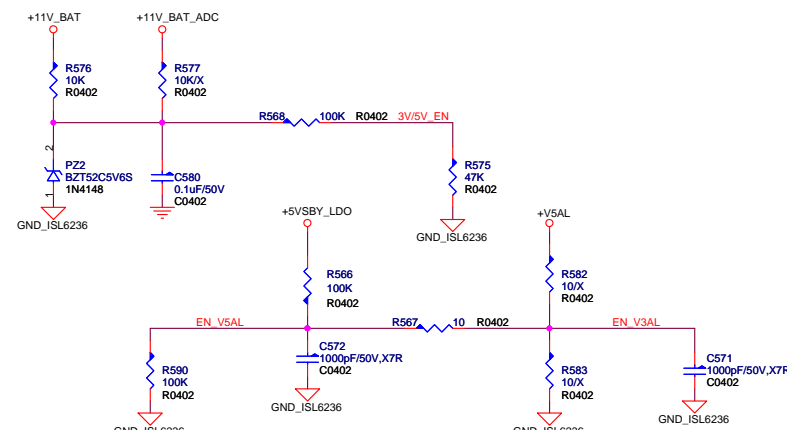
+3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

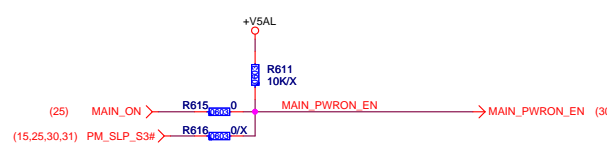
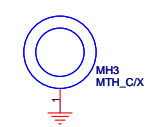
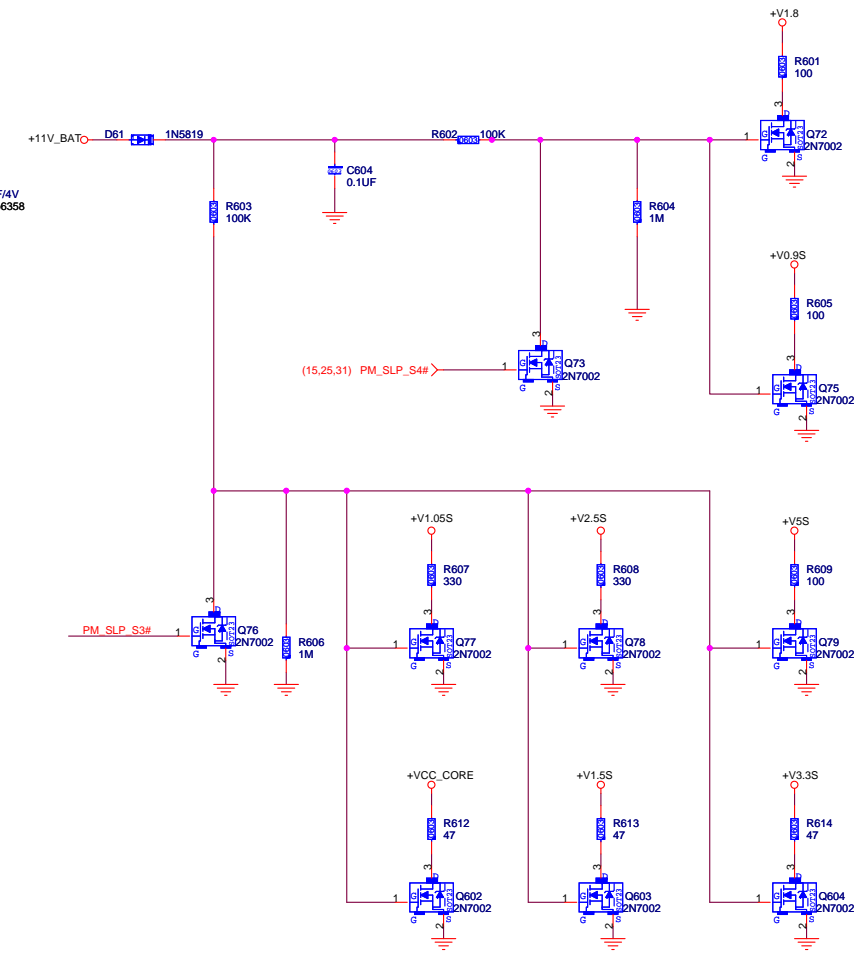
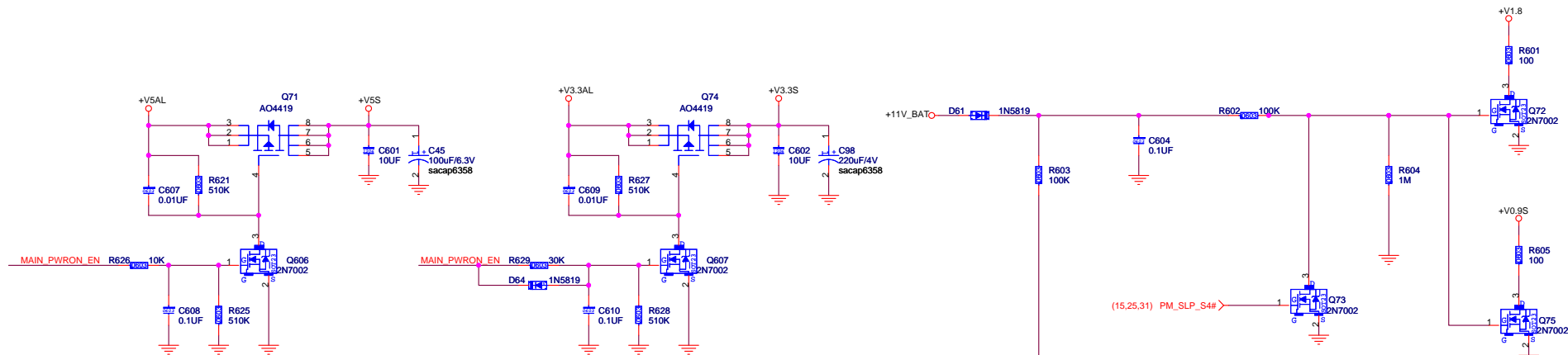


Vout=1.25(1+R2/R1)
3VDUAL

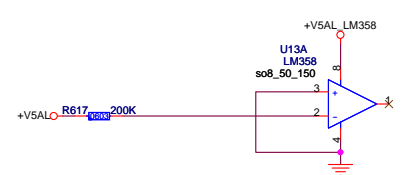
REF: 2V/1%/50uA
 Ton
 GND: 400K/500K
 REF: 400K/300K---Open
 VCC: 200K/300K
 VREF3: 3.3V/1.5%/5mA
 LDOPHASE1/GND---LDO/5V
 LDOPHASE1/VCC---LDO/3.3V
 LDOPHASE1/GND---BYP--->5V
 LDOPHASE1/VCC---BYP--->3.3V
 FB1/GND---Vout1/5V
 FB1/VCC---Vout1/1.5V
 VFBI/0.7V---Res. divider
 V(GND-PHASE)=VILIM/10
 Isource=5uA;0.3%/C
 SECFB: 2V
 REFIN2/VCC---Vout2/3.3V
 REFIN2/VREF3---Vout2/1.05V
 REFIN2<0.5V---Vout2/0V

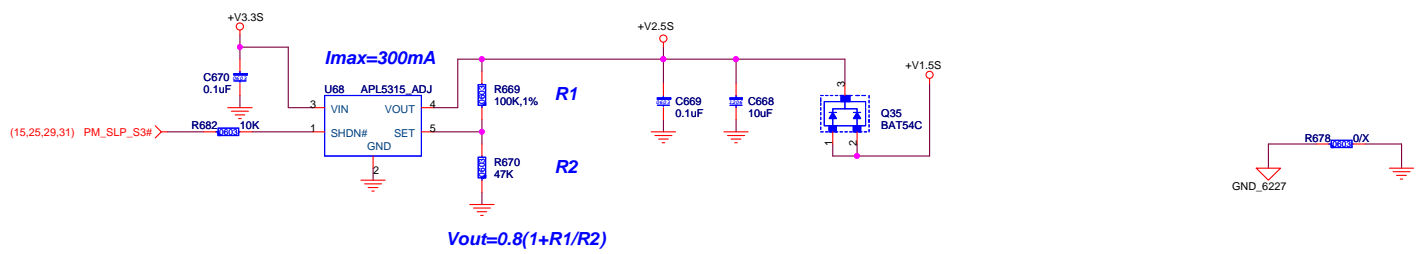
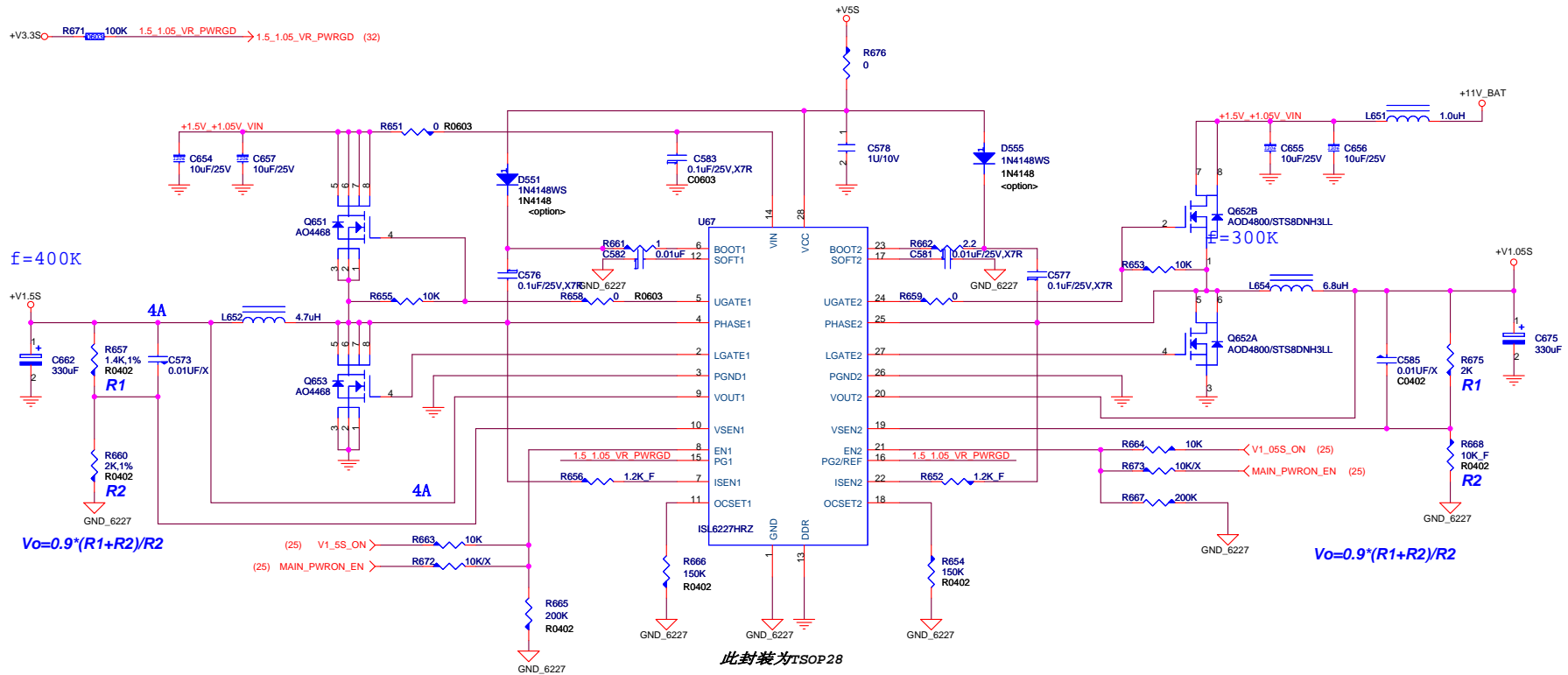
Maximum current:4A
 If LIR=0.3
 > I=4x0.3=1.2A
 Vin=19V;Fsw=300K
 L=6.8uH
 OCP:4x1.5=6A
 Iocp=6-(1.2/2)-5.4A
 Vth=5.4A*14.9mOhm=80mV
 R(Ilim)=(80mV*10)/5uA
 162K

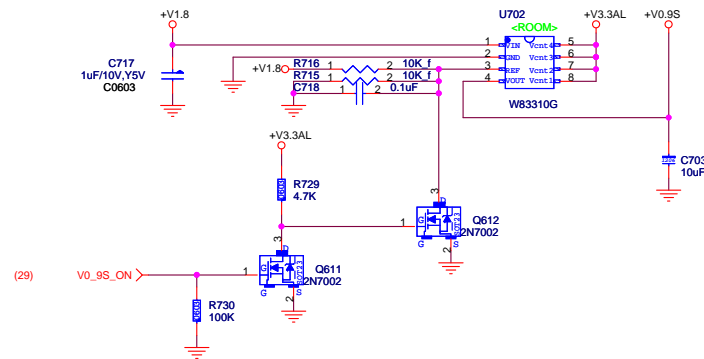
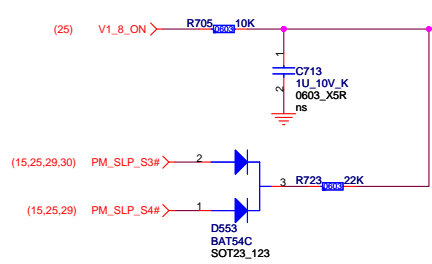
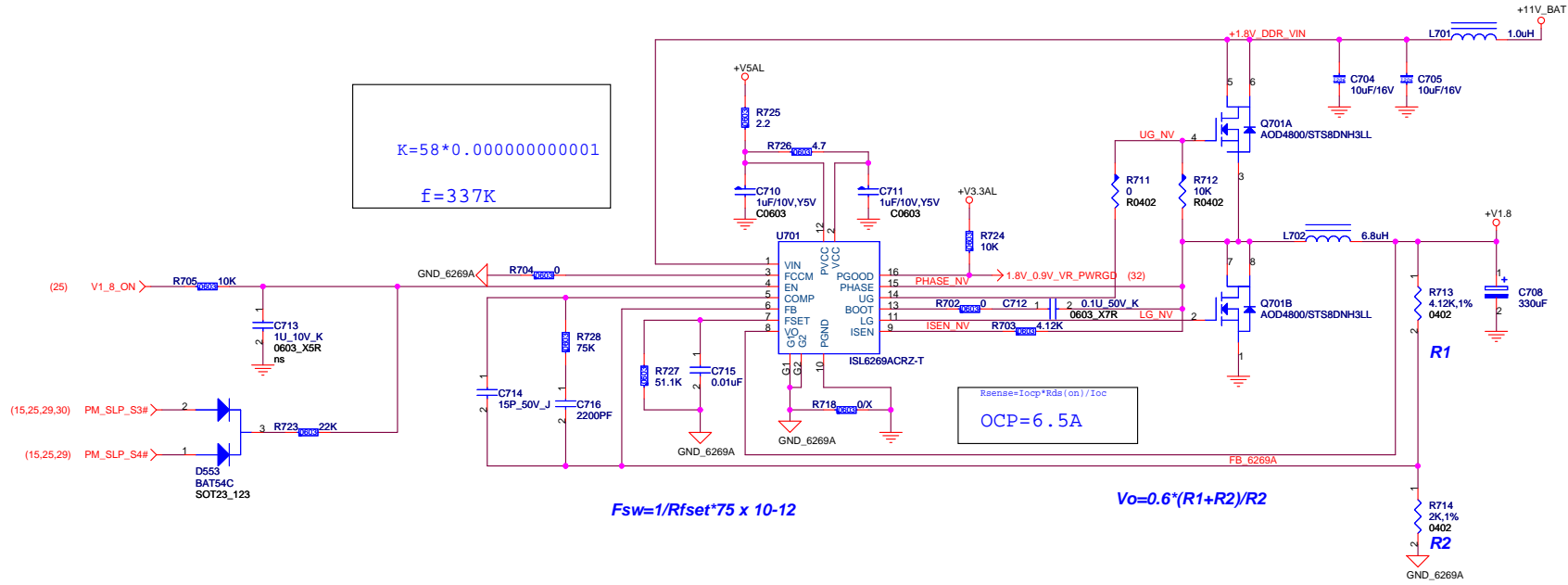


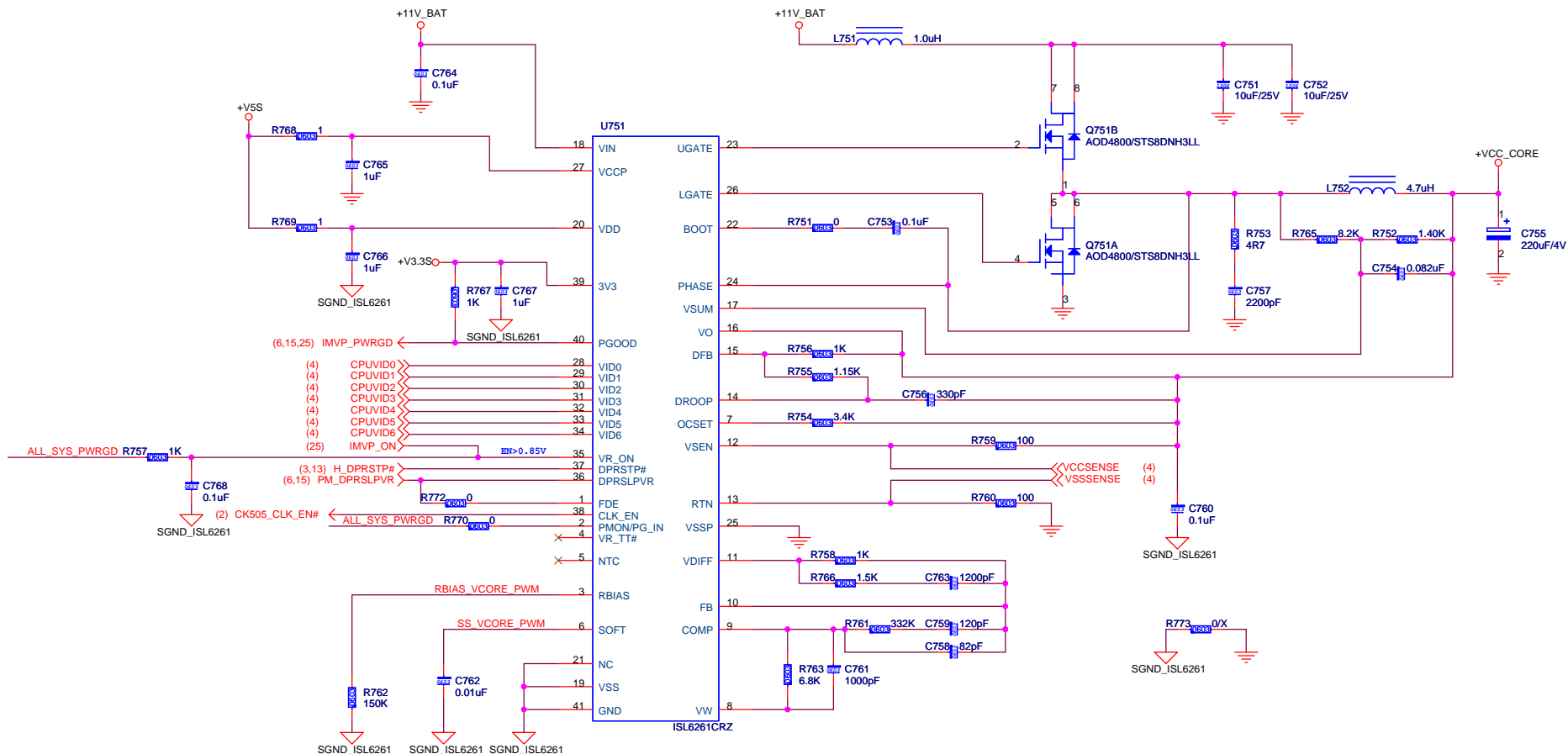


1, For first plug DC Jack,
 3.3VSBY,5VSBY power
 ON,S3 go High, if Don't Push
 Pwer ON Button, can't
 Output 3.3V/5V.

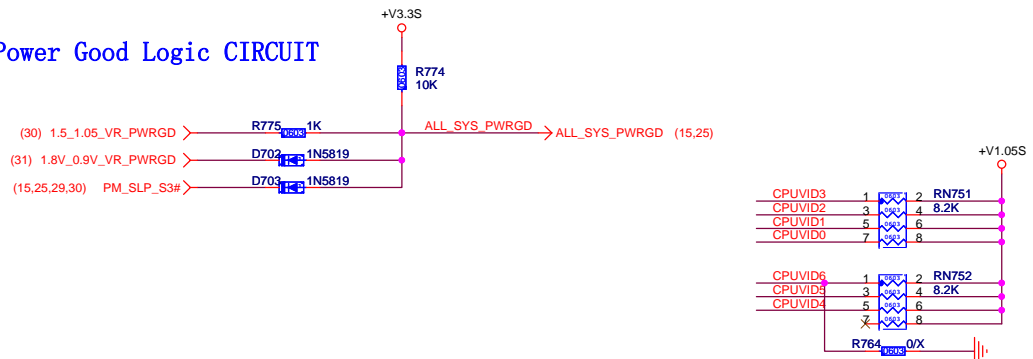








Power Good Logic CIRCUIT




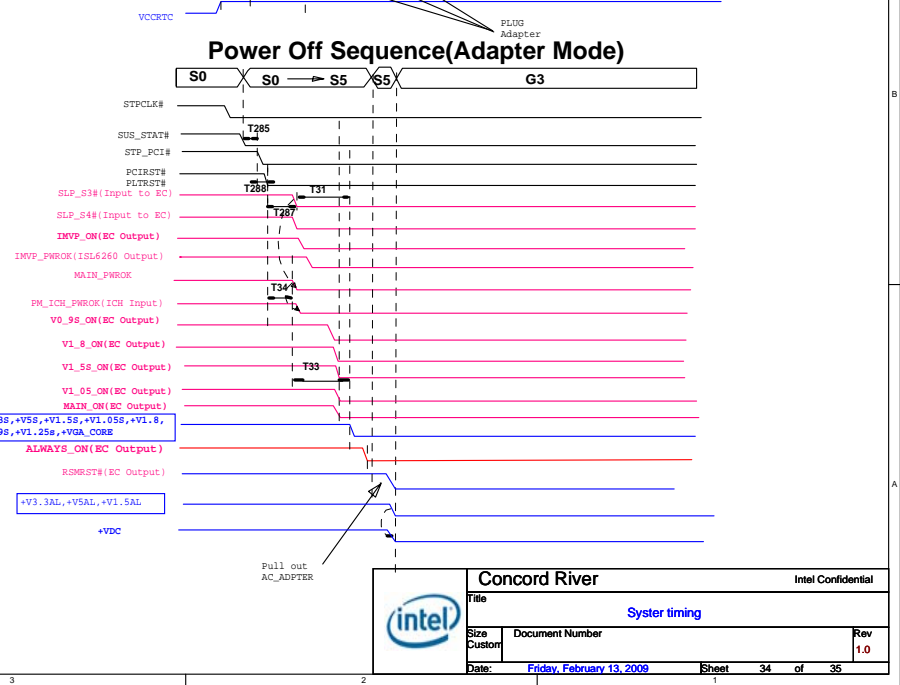
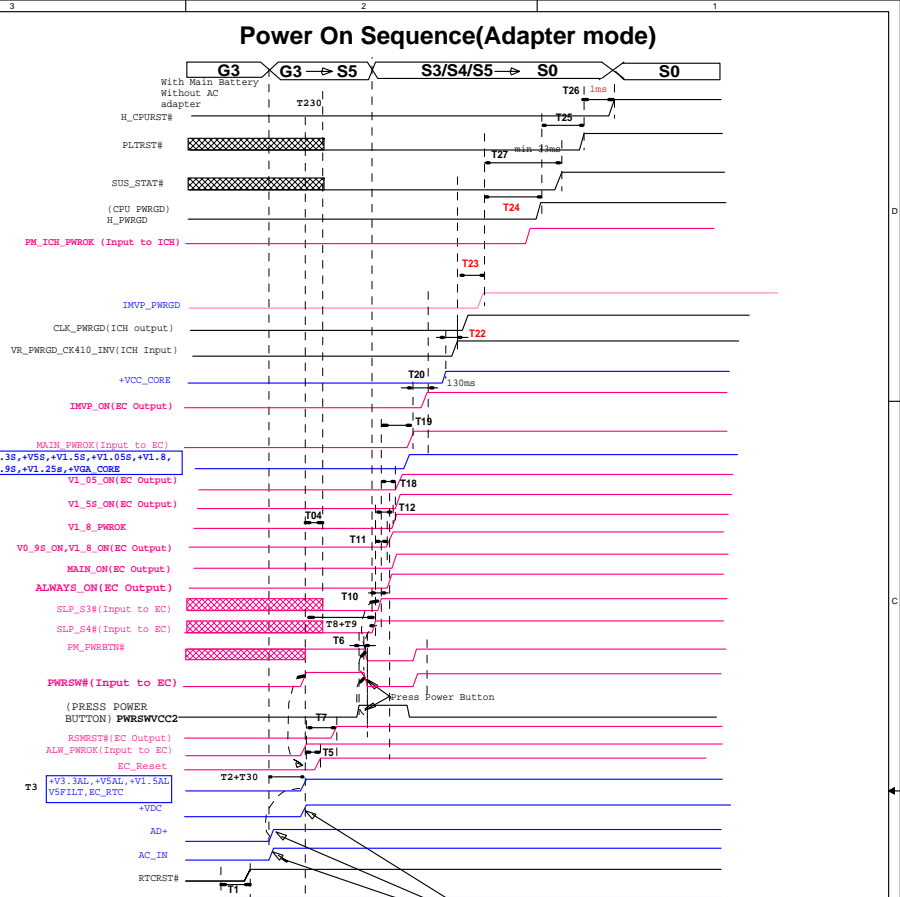
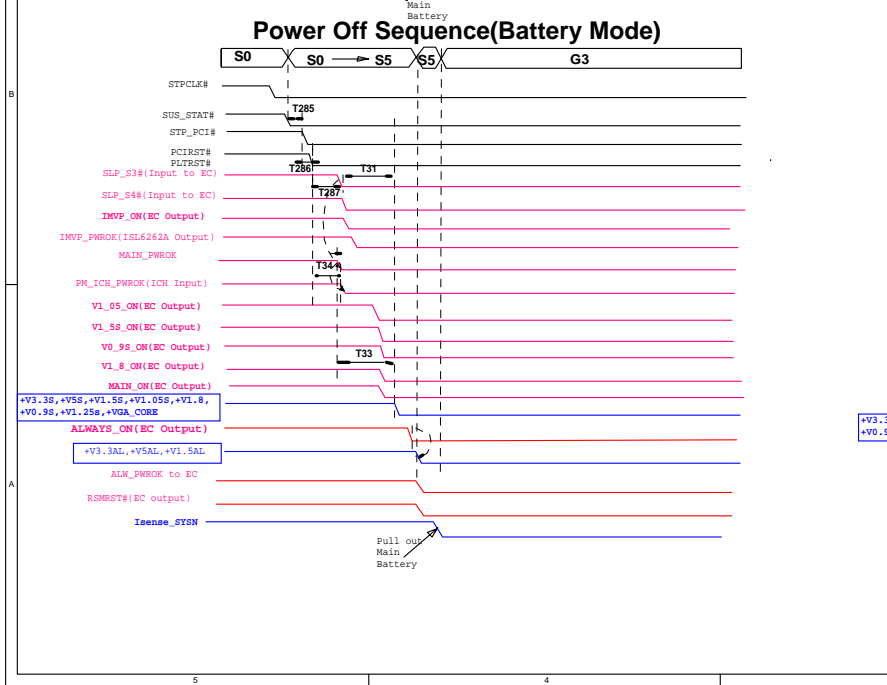
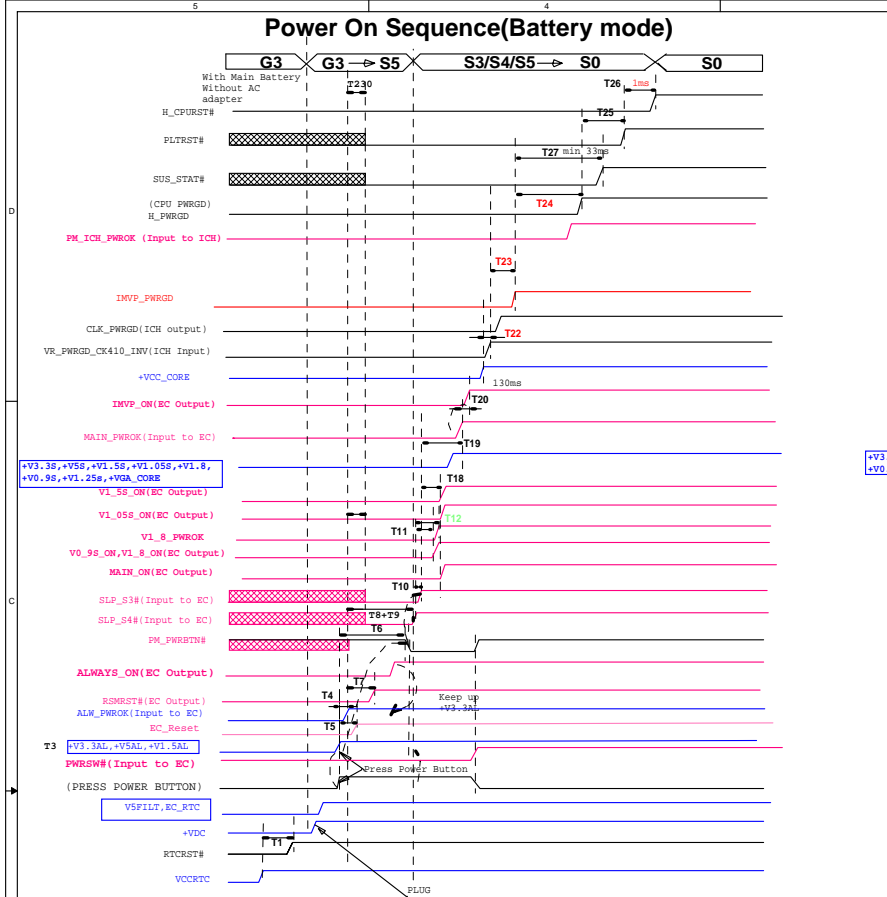
OPERATIONAL MODES

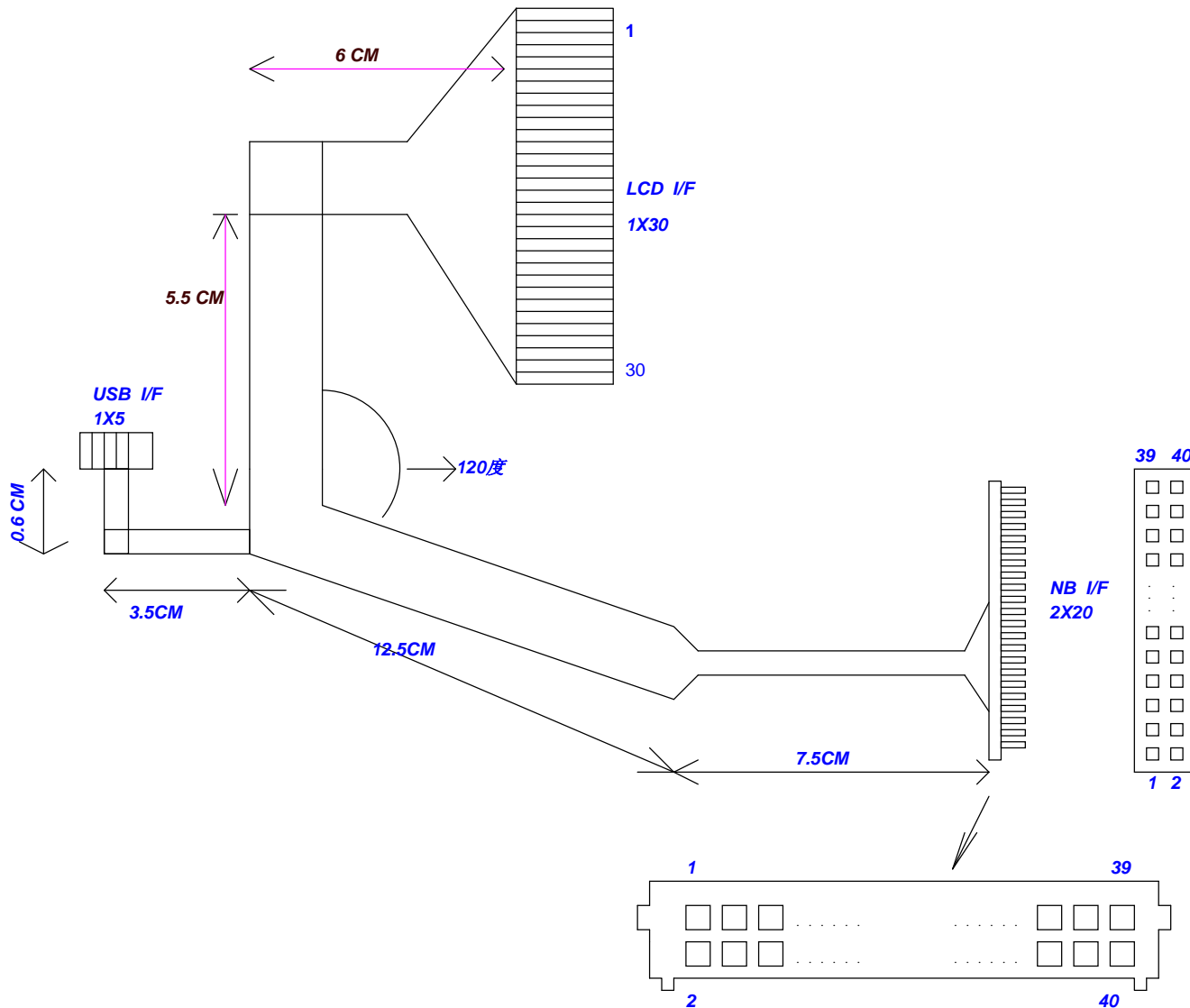
DPRSTP#	FDE	DPRSLPVR	OPERATIONAL MODE	VW-COMP WINDOW VOLTAGE INCREASE
0	0	0	Forced CCM(heavy load)	0%
0	0	1	Diode Emulation Mode(light load)	0%
0	1	X	Enhanced Diode Emulation Mode	33%
1	X	X	Forced CCM	0%

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LCD I/F Pin NB I/F Pin

1	3
2	1
3	2
4	17
5	21
6	18
7	20
8	6
9	8
10	9
11	5
12	7
13	10
14	12
15	14
16	16
17	13
18	11
19	15
20	X
21	X
22	22
23	4
24	30
25	32
26	34
27	X
28	X
29	X
30	X

USB I/F

1	19
2	24
3	26
4	27
5	28
X	23
X	25
X	29
X	31
X	33
X	35
X	36
X	37
X	38
X	39
X	40


V1.0 Change List

- 1, Change CLOCK IC
- 2, Add Adapte Shut down Circuit.
- 3, Change 3.3VSBY/5VSBY to 3.3V/5V control.
- 12, Add R334.
- 12, Add R335,C360.
- 12, Change R534,R566 net.
- 12, Delete R581,D552,R578.
- 12, Delete D62,R619,Q608,R618,C606,R633,Q30,R630,R631,C603.
- 12, Delete D554.

- 1, Change J1 Footprint
- 2, Add U12 for Debug
- 3, Add USB Port7 for test
- 4, Add ICH7 GPIO PULLUP Res.
- 5, Change VREF5V_SBY Net.
- 6, correct SATA RX Net.
- 7, Delete R401(Card Reader 3.3V Power)
- 8, Add USB Port7 Conn.
- 9, Change Jcon_80Port
- 10, Change 3VSBY/5VSBY Net.
- 11, Change R757 net for debug.
- 12, Change NB PWRGD Net.
- 13, Change Q802 to 2N7002
- 14, Change R801 to 22K
- 15, Change R538 to 200K, R540 to 51K.
- 16, Add D17,D54
- 17, Change SB net.

2008.11.12 V1.1---->V1.2 Change List

- 1, Change 3IN1 Card Reader net.
- 2, Change EC_RUNTIME_SCI from GPIO7 to GPIO9.
- 3, EC的KB加上拉电阻RN753, RN754。
- 4, Change KB net.
- 5, Change PD3 to P-MOS Q65.
- 6, Change R584 net.
- 7, SWAP LCD 1,2 PIN net.
- 8, Change BATT Pin.
- 9, Add BATT PWRBTN circuit.
- 9, Add R557,C579, Delete R588,R589.
- 10, Change C45,C98 to 5V,3.3V,Change C298 footprint.
- 11, Change C775 ,L651 footprint.
- 12, Change R575 to 100K.

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	Title		
	History		
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