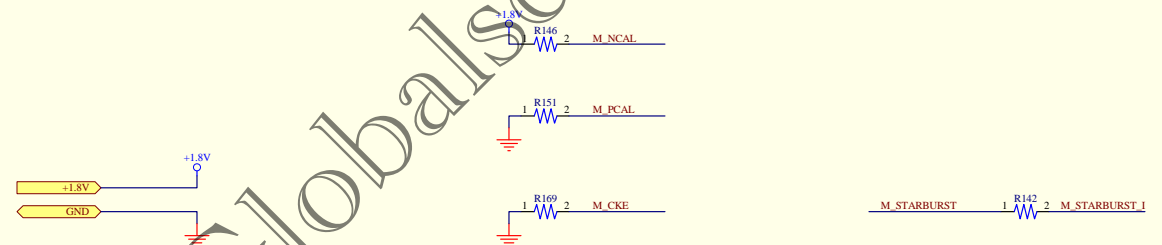
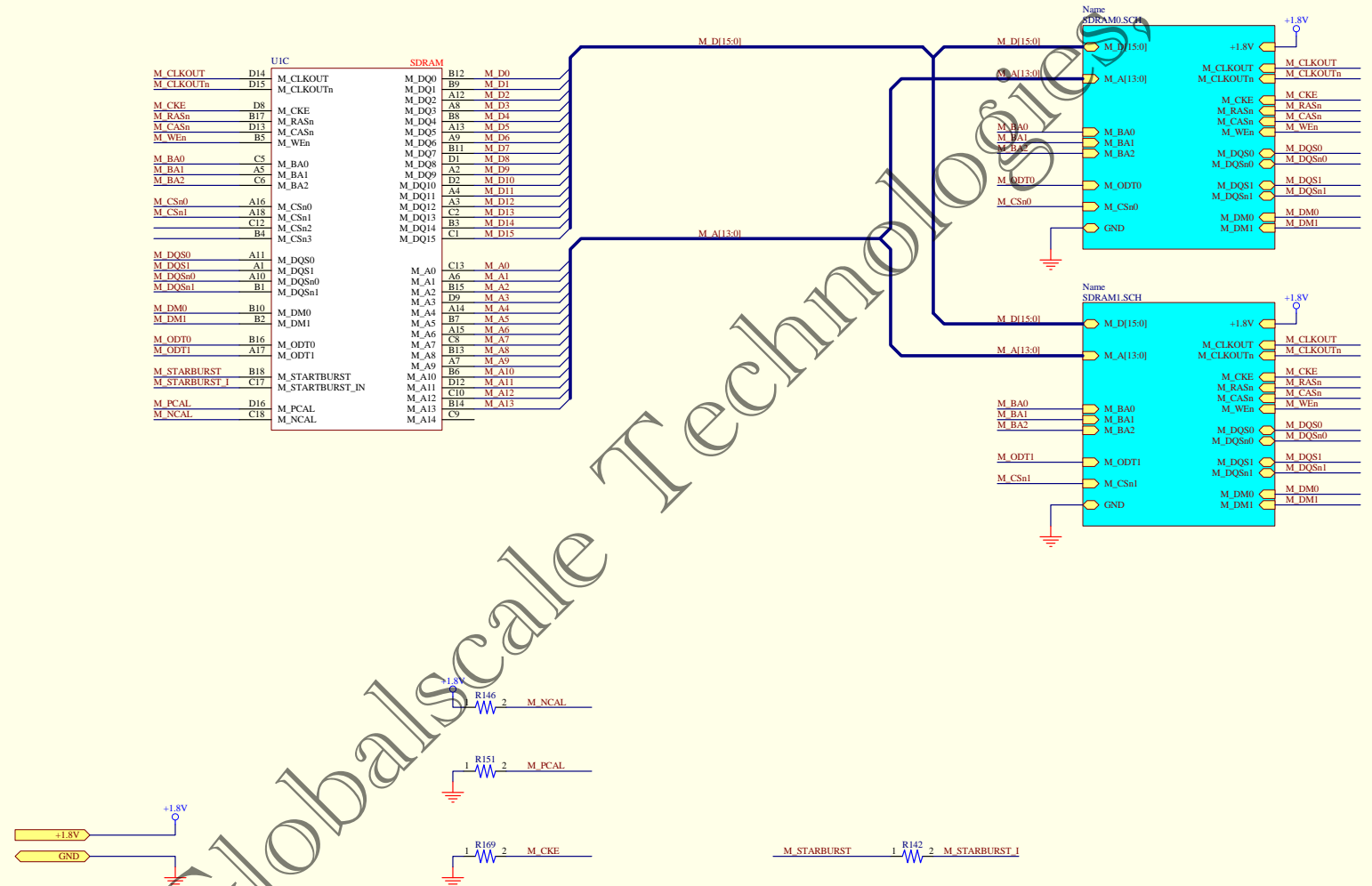
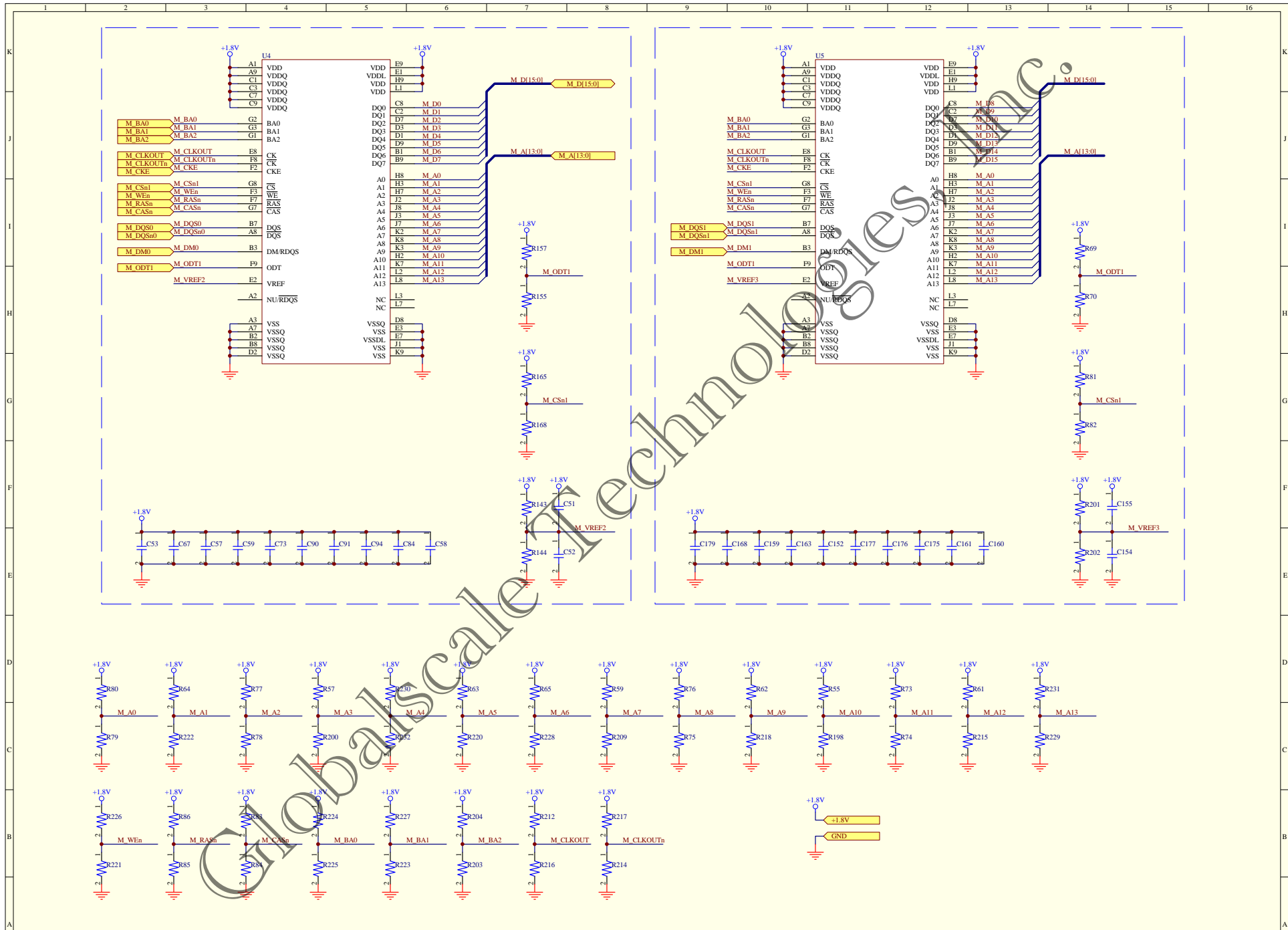


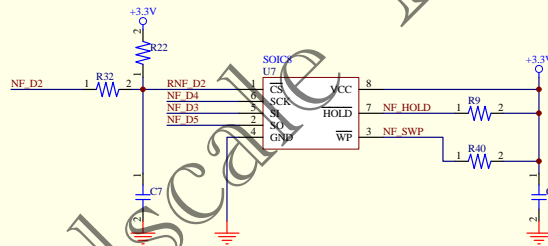
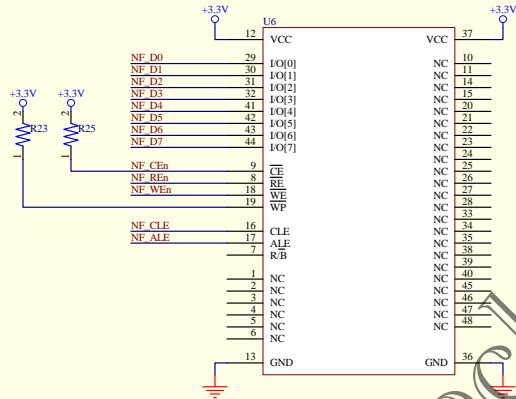
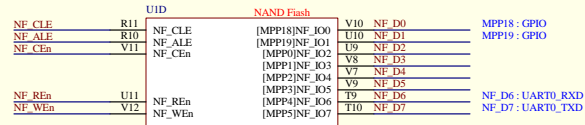
PD[1:4] 接2樓板銅柱孔

SheevaPlug2L_V2_R00

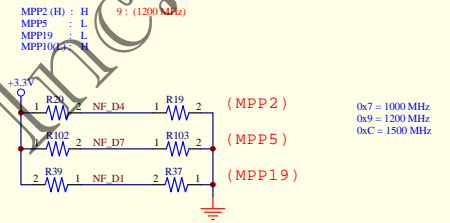
UIC		SDRAM	
M_CLKOUT	D14	M_CLKOUT	M_DQ0
M_CLKOUTn	D15	M_CLKOUTn	M_DQ1
M_CKE	D8	M_CKE	M_DQ2
M_RASn	B17	M_RASn	M_DQ3
M_CASn	D13	M_CASn	M_DQ4
M_We	B5	M_We	M_DQ5
M_BA0	C5	M_BA0	M_DQ6
M_BA1	A5	M_BA1	M_DQ7
M_BA2	C6	M_BA2	M_DQ8
M_CSn0	A16	M_CSn0	M_DQ9
M_CSn1	A18	M_CSn1	M_DQ10
	C12	M_CSn2	M_DQ11
	B4	M_CSn3	M_DQ12
			M_DQ13
			M_DQ14
			M_DQ15
M_DQS0	A11	M_DQS0	M_A0
M_DQS1	A1	M_DQS1	M_A1
M_DQS0n	A10	M_DQS0n	M_A2
M_DQS1n	B1	M_DQS1n	M_A3
M_DM0	B10	M_DM0	M_A4
M_DM1	B2	M_DM1	M_A5
M_ODT0	B16	M_ODT0	M_A6
M_ODT1	A17	M_ODT1	M_A7
M_STARBURST	B18	M_STARBURST	M_A8
M_STARBURST_1	C17	M_STARBURST_IN	M_A9
M_PCAL	D16	M_PCAL	M_A10
M_NCAL	C18	M_NCAL	M_A11
			M_A12
			M_A13
			M_A14
			M_A15



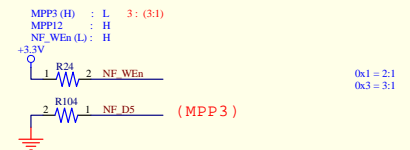




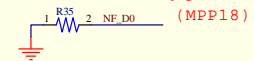
CPU_CLK Frequency Select



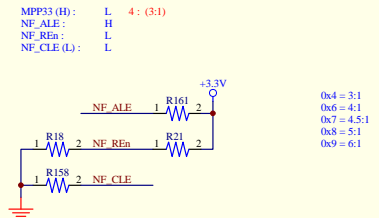
CPU Clk to L2 Clk Ratio



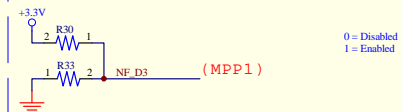
MUST be externally pulled down to 0x0 during reset



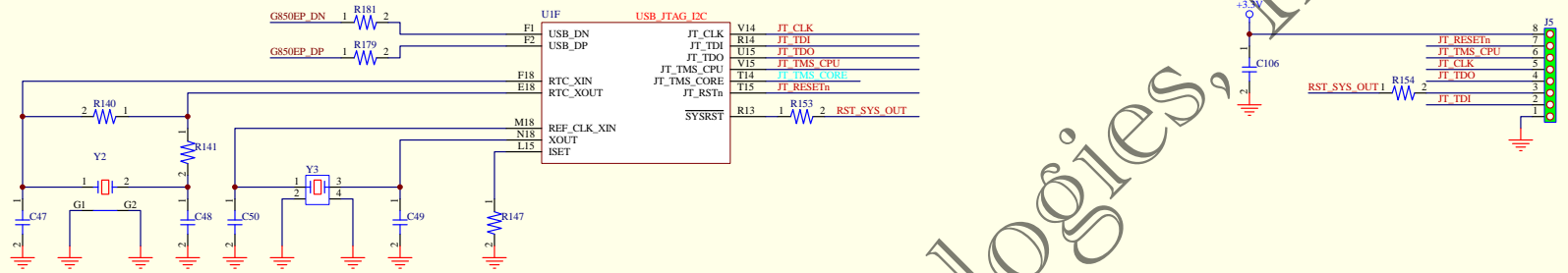
CPU Clk to DDR Clk Ratio



TWSI Serial ROM Initialization Disble

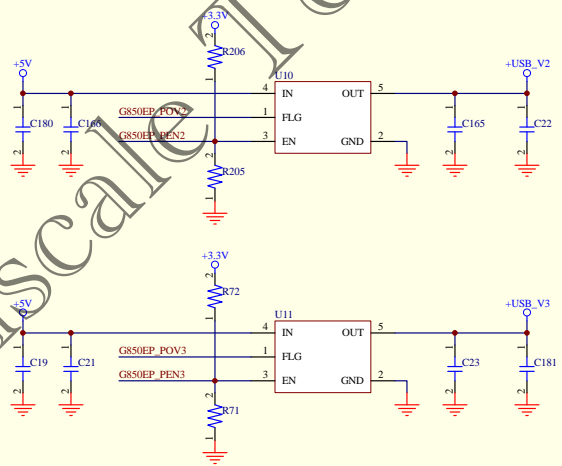
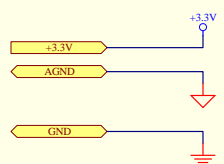


MPP18 : GPIO
MPP19 : GPIO
NF_D6 : UART0_RXD
NF_D7 : UART0_TXD

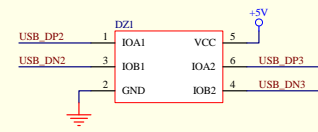
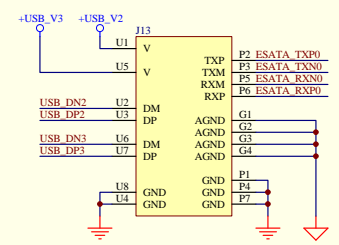


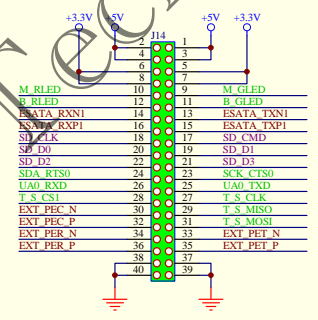
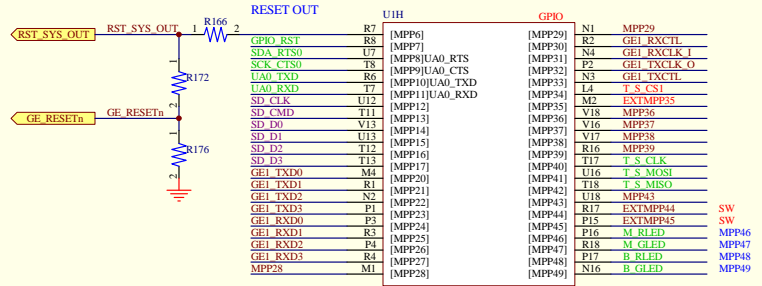
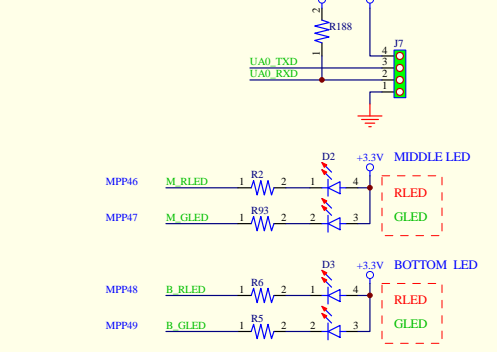
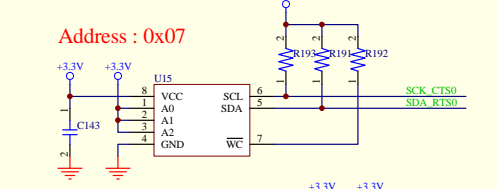
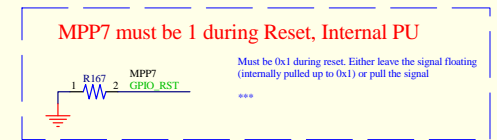
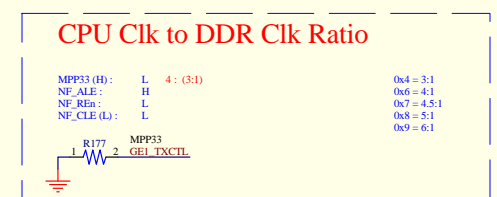
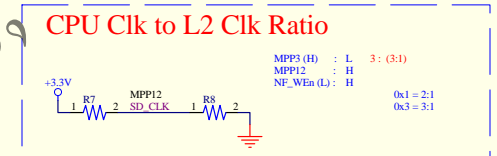
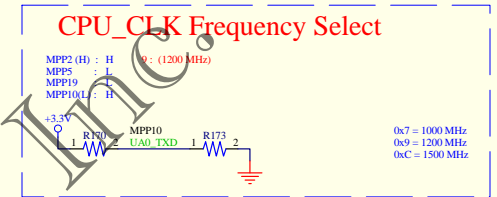
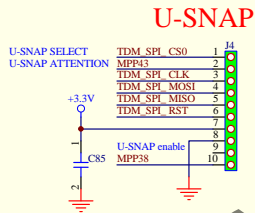
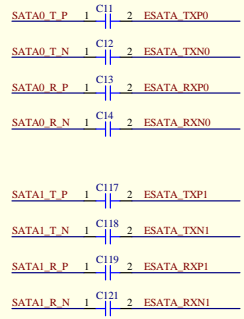
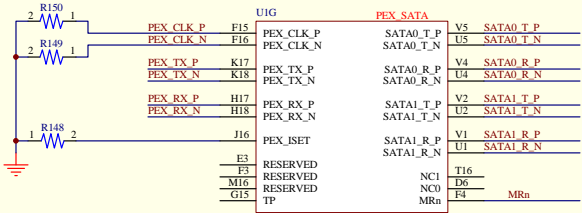
- G850EP_DP G850EP_DP
- G850EP_DN G850EP_DN
- G850EP_DN2 G850EP_DN2
- G850EP_DP2 G850EP_DP2
- G850EP_POV2 G850EP_POV2
- G850EP_PEN2 G850EP_PEN2
- G850EP_DN3 G850EP_DN3
- G850EP_DP3 G850EP_DP3
- G850EP_POV3 G850EP_POV3
- G850EP_PEN3 G850EP_PEN3

- ESATA_TXP0 ESATA_TXP0
- ESATA_TXN0 ESATA_TXN0
- ESATA_RXP0 ESATA_RXP0
- ESATA_RXN0 ESATA_RXN0

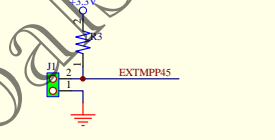


- G850EP_DN2 BIT2 USB_DN2
- G850EP_DP2 BIT1 USB_DP2
- G850EP_DN3 BIT3 USB_DN3
- G850EP_DP3 BIT4 USB_DP3

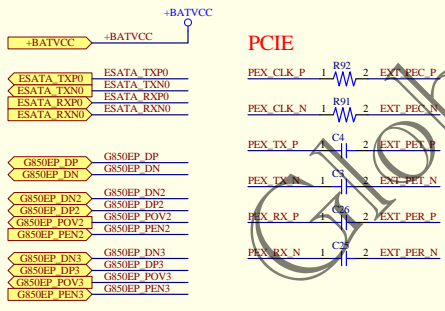
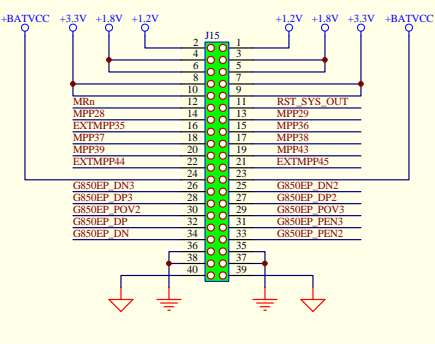
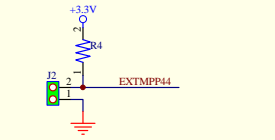


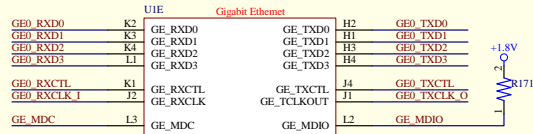


UART Monitor On/Off



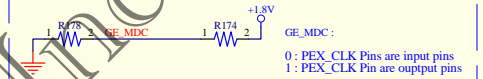
BootLoader & Format SD card





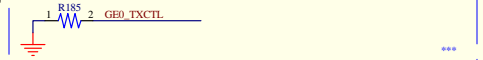
PCI Express Clock

0x0 = The device use external source for PCI Express clock. Pins PEX_CLK_P/PEX_CLK_N are
 0x1 = The device use internal generated clock for PCI Express clock. Pins
 PEX_CLK_P/PEX_CLK_N pins are outputs, driving out the PCI Express differential clock.



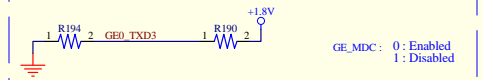
Used for internal testing

GE0_TXCTL
 Must be 0x0 during reset. Either leave the signal floating
 (internally pulled down to 0x0) or pull the signal to



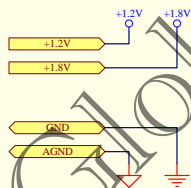
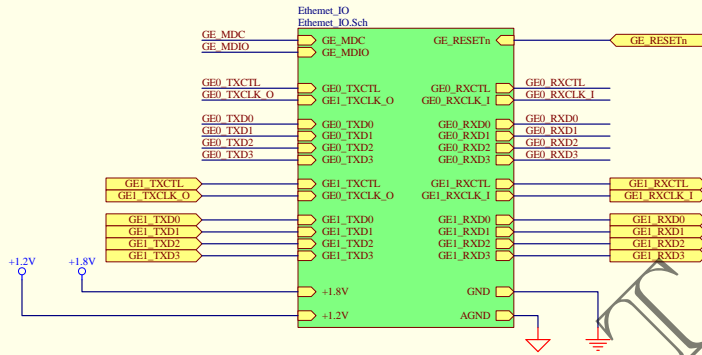
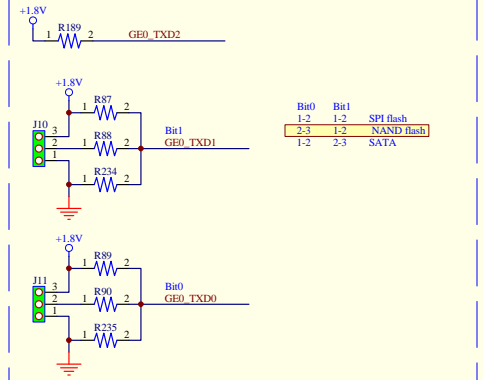
SSCG

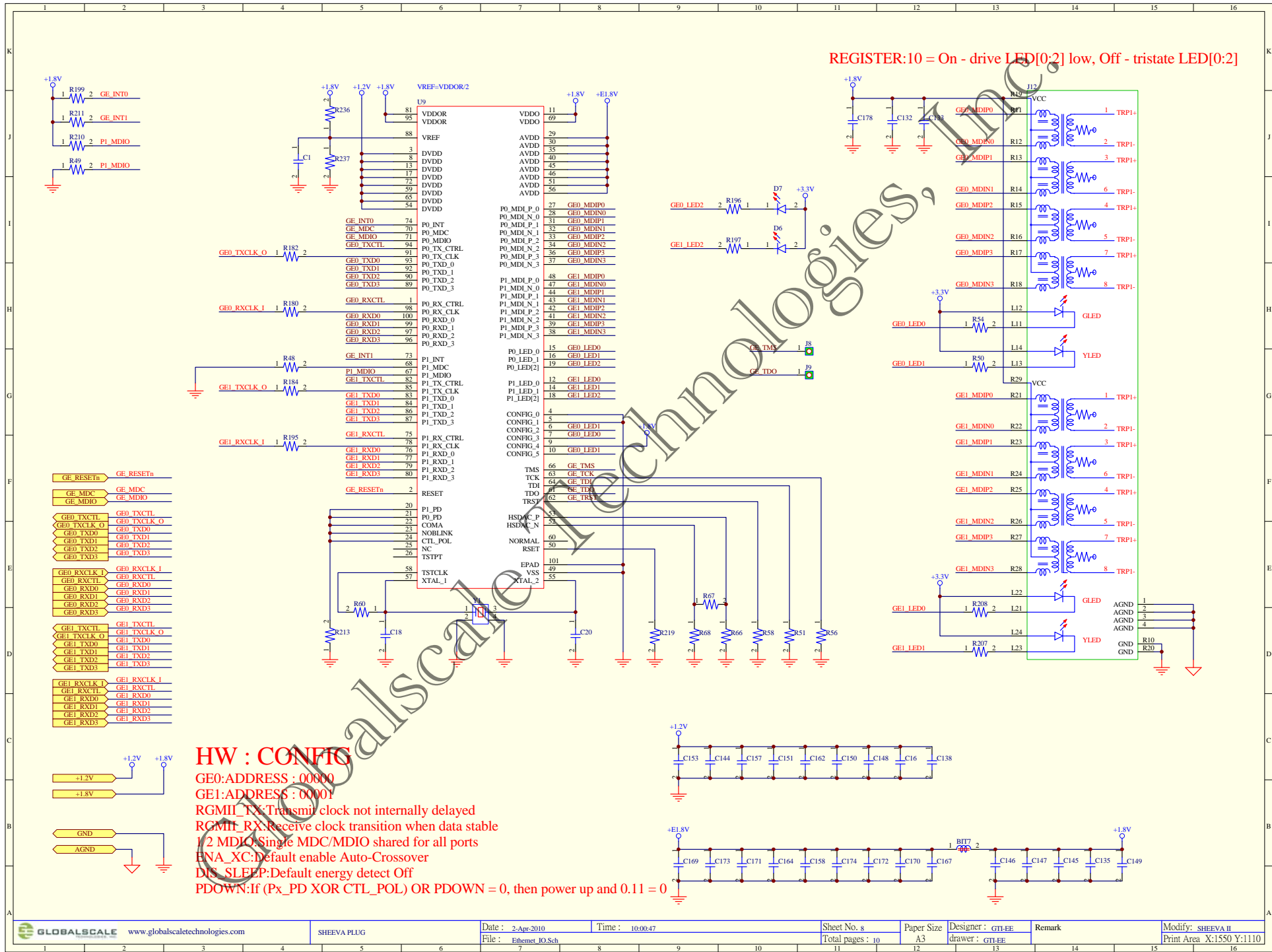
Spread Spectrum Clock Generator



Reset Configuration(Boot from NAND flash)

GE0_TXD3(H) : H 4 : Boot from SPI flash (SPI_CSn on MPP(0))
 GE0_TXD1 : L 5 : Boot from NAND flash
 GE0_TXD0(L) : L 6 : Boot from SATA

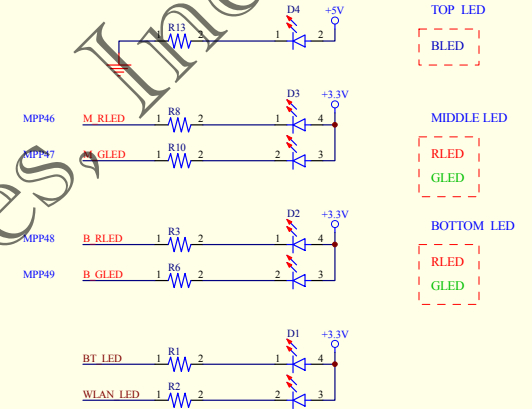
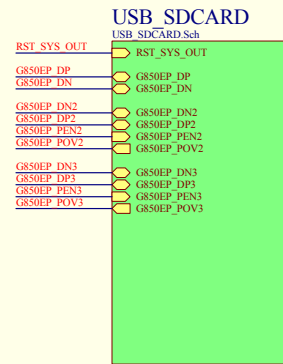
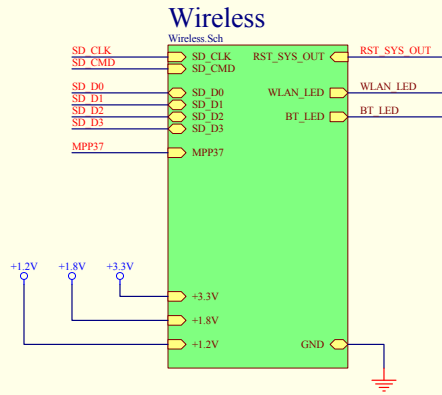




HW : CONFIG
 GE0:ADDRESS : 00000
 GE1:ADDRESS : 00001
 RGMII_TX:Transmi clock not internally delayed
 RGMII_RX:Receive clock transition when data stable
 MDIO:Single MDC/MDIO shared for all ports
 ANA_XC:default enable Auto-Crossover
 DIS_SLEEP:Default energy detect Off
 PDOWN:If (Px_PD XOR CTL_POL) OR PDOWN = 0, then power up and 0.11 = 0

REGISTER:10 = On - drive LED[0:2] low, Off - tristate LED[0:2]

- GE_RESETn GE_RESETn
- GE_MDC GE_MDC
- GE_MDIO GE_MDIO
- GE0_TXCTL GE0_TXCTL
- GE0_TXCLK_O GE0_TXCLK_O
- GE0_TXD0 GE0_TXD0
- GE0_TXD1 GE0_TXD1
- GE0_TXD2 GE0_TXD2
- GE0_TXD3 GE0_TXD3
- GE0_RXCLK_I GE0_RXCLK_I
- GE0_RXCTL GE0_RXCTL
- GE0_RXD0 GE0_RXD0
- GE0_RXD1 GE0_RXD1
- GE0_RXD2 GE0_RXD2
- GE0_RXD3 GE0_RXD3
- GE1_TXCTL GE1_TXCTL
- GE1_TXCLK_O GE1_TXCLK_O
- GE1_TXD0 GE1_TXD0
- GE1_TXD1 GE1_TXD1
- GE1_TXD2 GE1_TXD2
- GE1_TXD3 GE1_TXD3
- GE1_RXCLK_I GE1_RXCLK_I
- GE1_RXCTL GE1_RXCTL
- GE1_RXD0 GE1_RXD0
- GE1_RXD1 GE1_RXD1
- GE1_RXD2 GE1_RXD2
- GE1_RXD3 GE1_RXD3



SheevaPlug2_F2_V02_R02

