Description of Hardware block diagram – GTI- 2010.04.03

Power supply

1. There is a AC-DC power module inside this product to take 100V~240V AC input and transfer it to 5VDC output with 3A maximum current load.
2. 5VDC is then fed into U8, U12 and U14 on the MB (Mother Board or 1st floor board) to create all the necessary power rails for system use , including 1.0VDC, 1.1VDC, 1.2VDC, 1.8VDC and 3.3VDC

SDRAM – 1F-U2, U3, U4, U5

1. DDR2 SDRAM is used for this application with 400MHz clock rate and 800MHz data rate.
2. 4 units of 1Gb DDR2 with the structure of 8Mbit x 16 I/Os x 8 banks each, totally there will be 512M x 8 bit of memory size in two banks (256MB+ 256MB)

NAND FLASH- 1F-U6

1. 512M x 8 bit NAND Flash is used as the storage memory for the Operating system .
2. During power on boot up, the contents will be read out from NAND Flash and stored to SDRAM for fast operating.

Gb Ethernet- 1F-U9

1. There are two 1000Mb/s Ether net MACs built inside the CPU, 1F-U9 works as a dual Ethernet PHY (Physical Layers) to bring the signals to two RJ45 ports
2. These two ports are running at speed of 10/100/1000 Mb/s

SATA/eSATA- 1F-J13

1. Two SATA interfaces have been built inside this CPU, all you have to do is to connect them to the SATA or eSATA connectors.
2. Here we use only one of the ports and connected it to the external eSATA interface.
3. 1F-J13 is the connector which combined 1xeSATA and 2x USB ports together.

Description of Hardware block diagram (continued)

USB- 2F-U4, 1F-J13

1. This CPU supports one USB 2.0 high speed host port.
2. 2F-U14 is the 1-to-4 USB HUB controller which expands 1 USB port to 4 ports.
3. Here we bring to the edge of the PCB only two USB connectors for use.
4. Another USB port will be converted as uSD interfaces described as below.

uSD- USB- 2F-U2, 2F-J3, 2F-J4

1. 2F-U2 is the USB to SD converter which takes signals input from one of 2F-U4 USB ports and has two SD output interfaces.
2. These two SD interfaces were connected to 2F-J3 and 2F-J4 uSD slots, one is inside the enclosure another one is on the edge of the enclosure with opening for user to insert the uSD card from outdide.

WiFi -802.11b/g- 2F-U1, 2F-J1, 2F-ANT1

1. One WiFi chip with 820.11/b/g compliance is incorporated for wireless LAN application.
2. The broadcast frequency band for this 802.11 b/g is 2.4GHz.
3. 2F-J1 is the connector for extern instrument connection and 2F-ANT1 is the Antenna

U-SNAP- 1F-J4

1. U-SNAP is the new interface standard for communication.
2. It uses the SPI signal interface and protocol so you may take it as the SPI port.
3. 1F-J4 is the connecting header.

Description of Hardware block diagram (continued)

UART0, JTAG

1. JTAG interface has been built-in the CPU for software development and system debug. An external debug board is used for this application.
2. These UART0 and JTAG signals are connected through 2 cables to the debug board and signals are converted to USB standard.
3. One mini-USB socket is implemented on the JTAG board to let the software programmer connect it to PC for development.

== End Of File ==