Circuit Description

Note: The description related to the LCD is applicable to PD78X only.

1. RF Section

1.1 TX Circuit

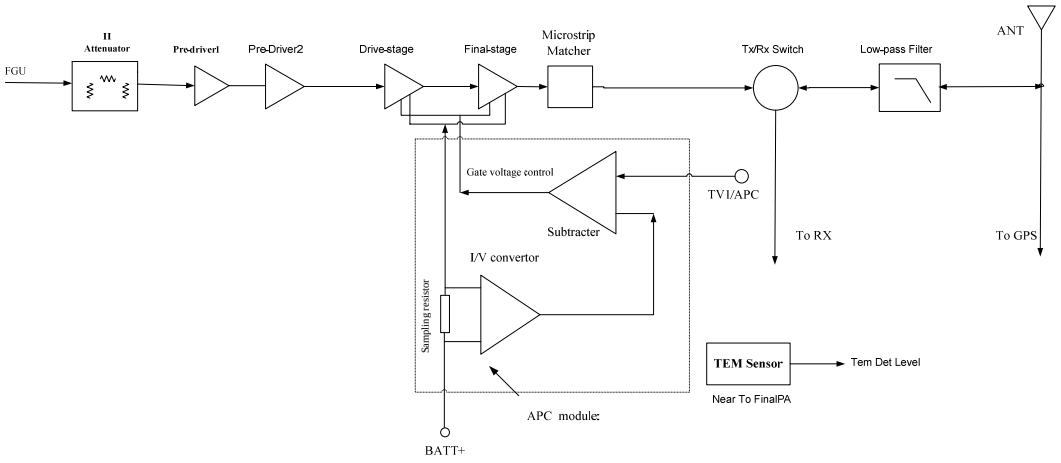

Figure 1 Diagram of TX Circuit

The TX circuit is mainly composed of:

① RF power amplifier circuit

② Low-pass filter circuit (for suppressing harmonics)

③ Auto power control circuit (APC) (including temperature detection circuit)

The carrier signal generated by TX VCO is modulated and amplified, and then feeds to the TX circuit. In this circuit, the signal passes through a II-type attenuator first, allowing certain isolation between the RF power amplifier circuit and TX VCO. Then it goes to a pre-driver amplifier (2SC3356) for pre-amplification, also generating certain isolation. After that, the signal goes to another pre-driver amplifier (2SC4988) and a driver amplifier (RD01) for further power amplification, to provide appropriate signal to the final-stage amplifier (RD07) for final power amplification. After processed by multiple amplifiers, the signal is processed by a microstrip matcher to complete output impedance matching, so as to reduce output power loss due to impedance mismatch. Then the signal passes through the TX/RX switch and goes to the low-pass filter.

The low-pass filter is a high-order Chebyshev filter composed of lumped parameter

inductors and capacitors. Via this filter, the spurious signal within the stop band can be attenuated as much as possible, provided that in-band ripple are within the required range.

In the auto power control and temperature detection circuit, the drain current from the driver amplifier and final-stage amplifier is converted to voltage via the sampling resistor and subtraction circuit (composed of the first operational amplifier). This voltage is compared with the APC control voltage (output by DAC) at the second operational amplifier. Then the error voltage, which is output by the second operational amplifier, controls TX power by controlling the bias voltage at the gates of the amplifiers (including driver amplifier and final-stage amplifier). The temperature sensor detects the temperature on the surface of the final-stage amplifier, and converts it to DC voltage. Then it is compared with the voltage corresponding to the protection temperature (generally 90% of the extreme temperature) of the amplifier. If the surface temperature is too high, the bias voltage of the amplifier will be reduced, so as to reduce output power. The bias voltage will not be increased until the surface temperature restores to normal level. This process will be repeated when the radio operates.

1.2. RX Circuit

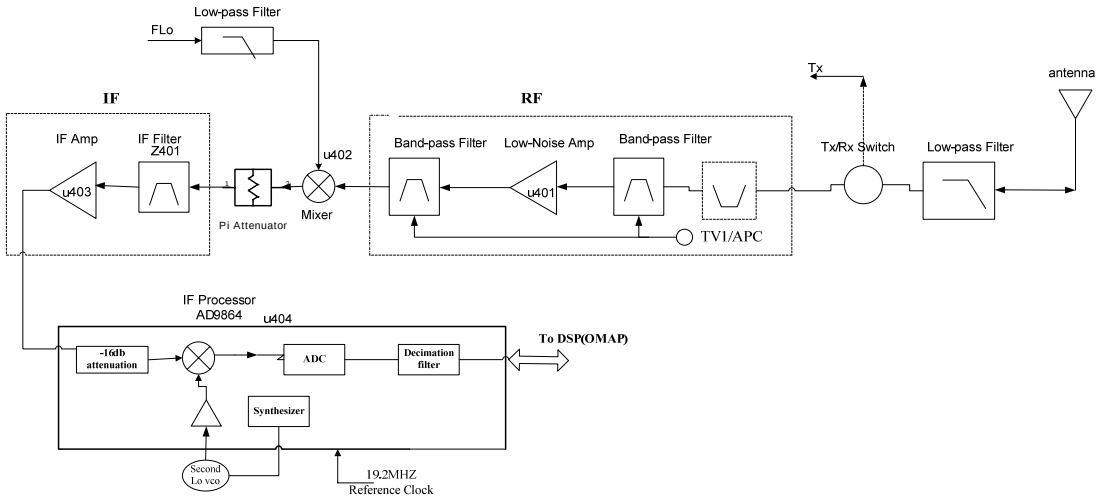

Figure 2 Diagram of RX Circuit

The RX circuit mainly comprises: RF band-pass filter, low-noise amplifier, mixer, IF filter,

IF amplifier and IF processor.

1) Front-end Circuit

The HF signal from the low-pass filter passes through the electrically tunable band-pass filter controlled via APC/TV1 level, to remove out-of-band interference and to send wanted band-pass signal to the low-noise amplifier (Q9001). The amplified signal goes to a band-pass filter controlled via APC/TV1 level, to remove out-of-band interference resulted from amplification, and to send wanted HF signal to the mixer.

The wanted signal passes through the RF band-pass filter and low-noise amplifier and goes to the mixer (D9017). Meanwhile, the first local oscillator (LO) signal generated by VCO passes through the low-pass filter and also goes to the mixer (D9017). In the mixer, the wanted signal and the first LO signal are mixed to generate the first IF signal (44.85MHz). Then the signal passes through a II-type attenuator (2dB) and the LC, to suppress carrier other than the first IF signal, and to increase the isolation between the mixer and the IF filter. After that, the first IF signal is processed by the crystal filter (Z9001), and is sent to the two-stage IF amplifier circuit (composed of PBR941) for amplification. Then the amplified signal goes to the IF processor AD9864(U401) for processing.

2) Rear-end Circuit

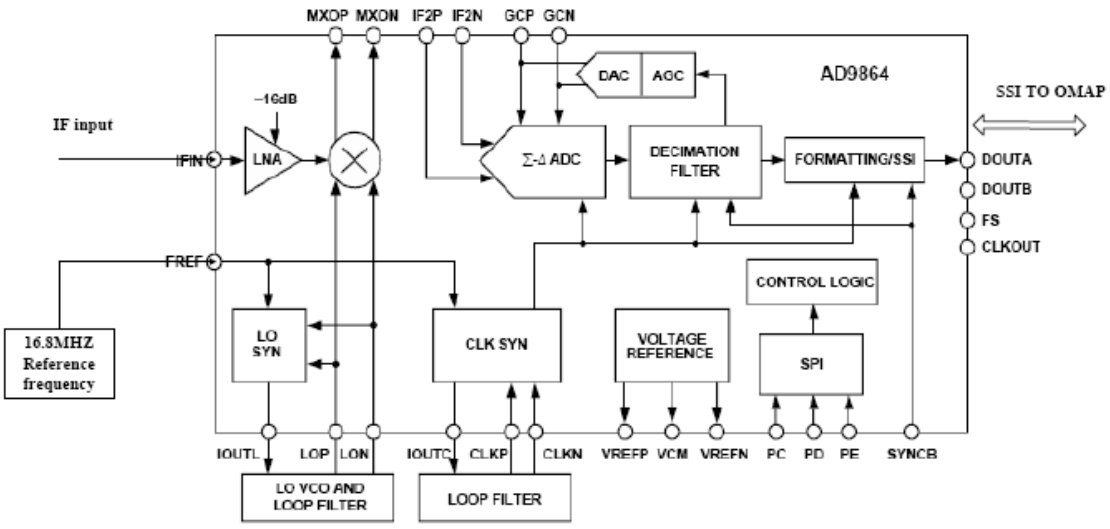

Figure 3 Diagram of IF Processor

The first IF signal (44.85MHz) output by the IF amplifier goes into AD9864 (U401) via Pin 47, where the signal is converted to the second IF signal (2.25MHz). Then the signal is converted to digital signal via ADC sampling, and output via the SSI interface. Finally, the digital signal is sent to DSP (OMAP5912) for demodulation.

AD9864 employs reference frequency of 19.2MHz and shares the crystal with OMAP. The second LO VCO comprises oscillator, varactor and some other components, to generate the 42.6/47.1MHZ LO signal. The 18MHz clock frequency is generated by the LC resonance loop.

1.3 Frequency Synthesizer Circuit

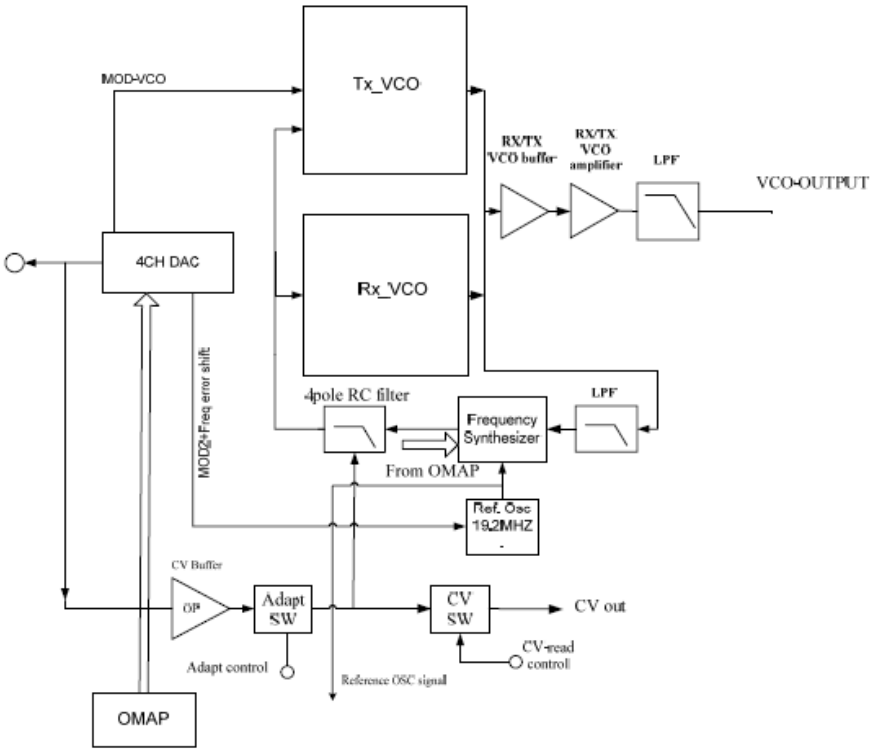

Figure 4 Diagram of Frequency Synthesizer Circuit

The frequency synthesizer circuit is composed of VCO and PLL. It is the core module of the whole TX-RX system. This circuit provides accurate carrier frequency during transmission, and stable LO signal during reception. It has a direct influence on the performance of the system.

1) Working Principle of PLL

The 19.2MHz frequency generated by the reference crystal oscillator is divided into reference frequency (i.e. step frequency f1) by the frequency divider in PLL. In addition, the frequency generated by VCO is divided into frequency f2 by the frequency divider in PLL. Then frequencies f1 and f2 are compared in the phase detector (PD), to generate continuous pulse current. The current goes to the loop filter for RC integration, and is then converted to DC CV

voltage. The CV voltage is sent to the varactor of VCO. It adjusts the output frequency of VCO directly until the CV voltage becomes constant. Then PLL is locked, and the stable frequency output by VCO goes to the TX-RX path after passing through two buffer amplifiers.

2) Working Principle of VCO

VCO employs Colpitts oscillator circuit (the RX oscillator circuit is composed of D102, D103, D106, D107 and L112; the TX oscillator circuit is composed of D108, D109, D110, D101 and L117). It obtains different output frequencies by changing the varactor's control voltage (i.e. CV change).

There are two types of VCO: TX VCO and RX VCO. Both types control EMD22 to switch operating status via OMAP. RX VCO is composed of the oscillator loop and Q104, to provide LO signal. TX VCO is composed of the oscillator loop and Q108, to provide carrier for TX signal.

1.4 GPS Circuit

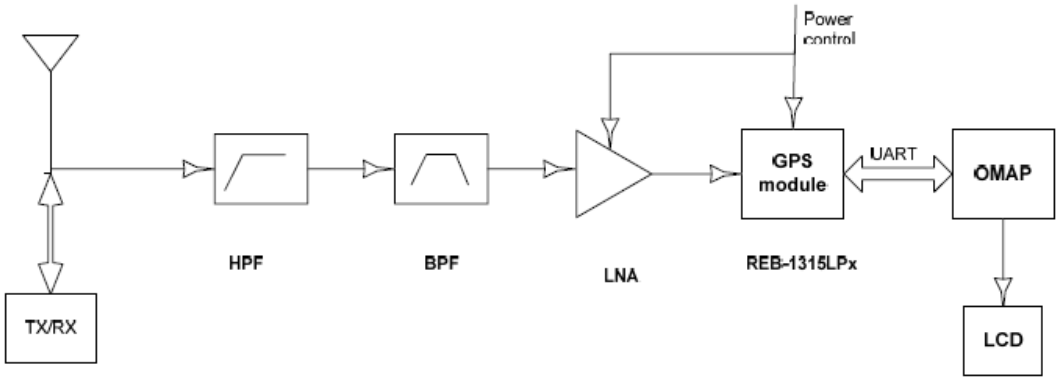

Figure 5 Diagram of GPS Circuit

The GPS function is realized via REB-1315LPx. The GPS circuit integrates a baseband processor, a LNA and a SAW.

The 1575.42MHz GPS signal is received by the antenna, and then goes to HPF to remove the 136MHz-174MHz signals used for transmission and reception. After that, the signal goes to BPF to further remove 136MHz-174MHz signals and interference caused by harmonic and spurious signals. Then the weak GPS signal goes to a low-noise amplifier (LNA) for amplification. After amplified, the signal goes to the GPS module for further

amplification and filtering, and is then sent to the BB section for calculation. Then the calculated GPS positioning information is sent to OMAP via the UART interface. Meanwhile, OMPA can send appropriate command information to the GPS module via the UART interface. Finally, OMAP sends the processed data information to LCD.

（Note: The GPS feature will be realized in future. ）

2. BB Section

2.1 OMAP5912 Dual-core Processor

PD70X/78X uses the dual-core processor OMAP5912, which is mainly composed of ARM926EJ-S and TMS320C55xx. ARM926EJ-S is the main controller, while TMS320C55xx is used for modulation/demodulation and voice encoding/decoding.

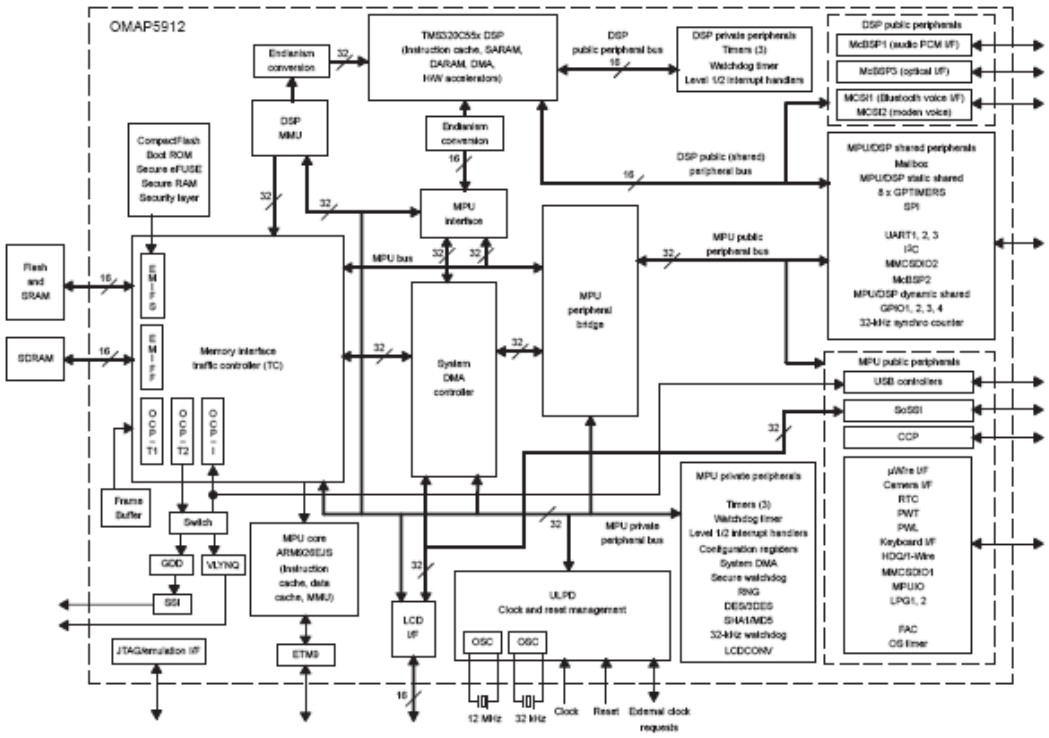

Figure 6 Diagram of OMAP5912

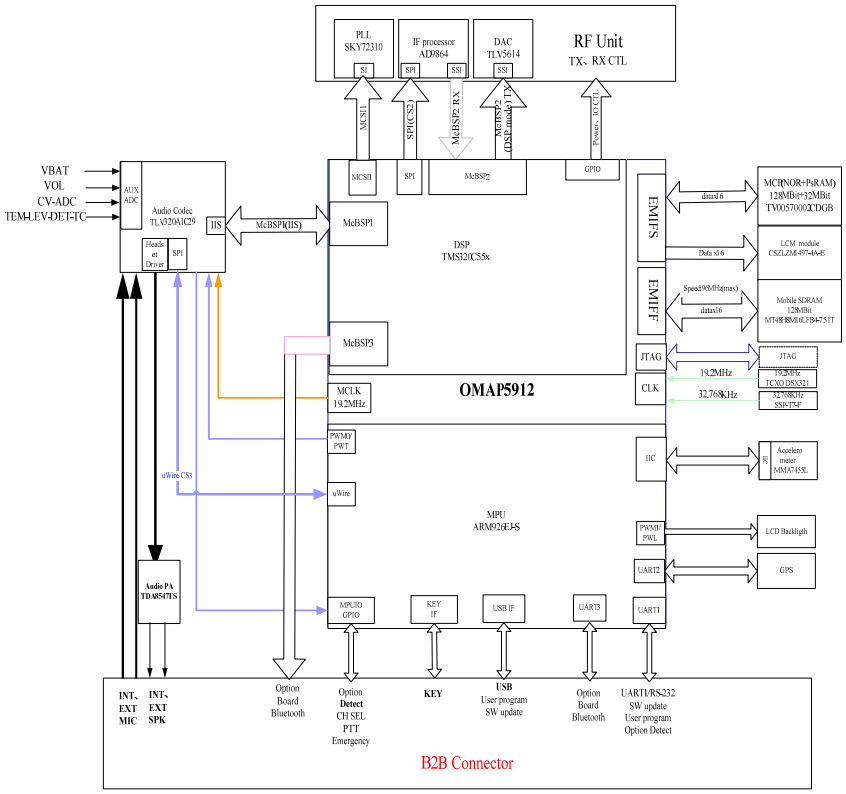

Figure 7 Diagram of Overall Scheme

2.2 External Memory

OMAP5912 provides two types of external memory interfaces: external memory interface slow (EMIFS) and external memory interface fast (EMIFF).

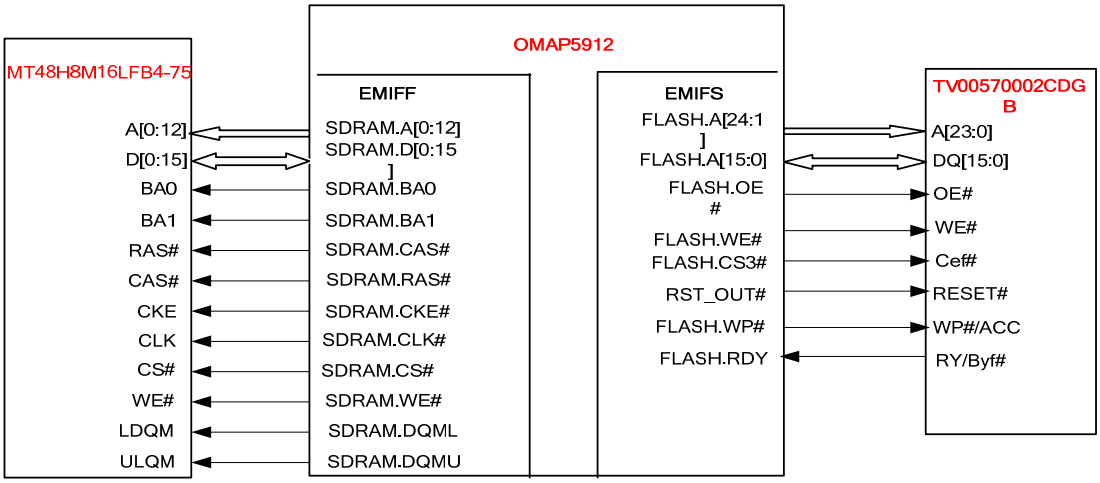

Figure 8 Diagram of External Memory

1) EMIFS

EMIFS is a 16-bit interface, and provides chip-selects CS0~CS3 (CS1 and CS2 can be divided into two 32MB chip-selects), each of which is 64MB. This interface supports

memories such as NAND Flash, NOR Flash, SRAM, andasynchronous and synchronous memories with AD mux or NON mux interface. EMIFS supports synchronous burst read, asynchronous read, asynchronous page read and asynchronous write.

2) EMIFF

EMIFF is a 16-bit interface, and supports SDRAM (up to 128MB), mobile SDRAM and mobile DDR. The maximum clock signal of the interface is 96MHz. The system can boot from CS0 (internal ROM), or from CS3 (external memory).

2.3 Clock

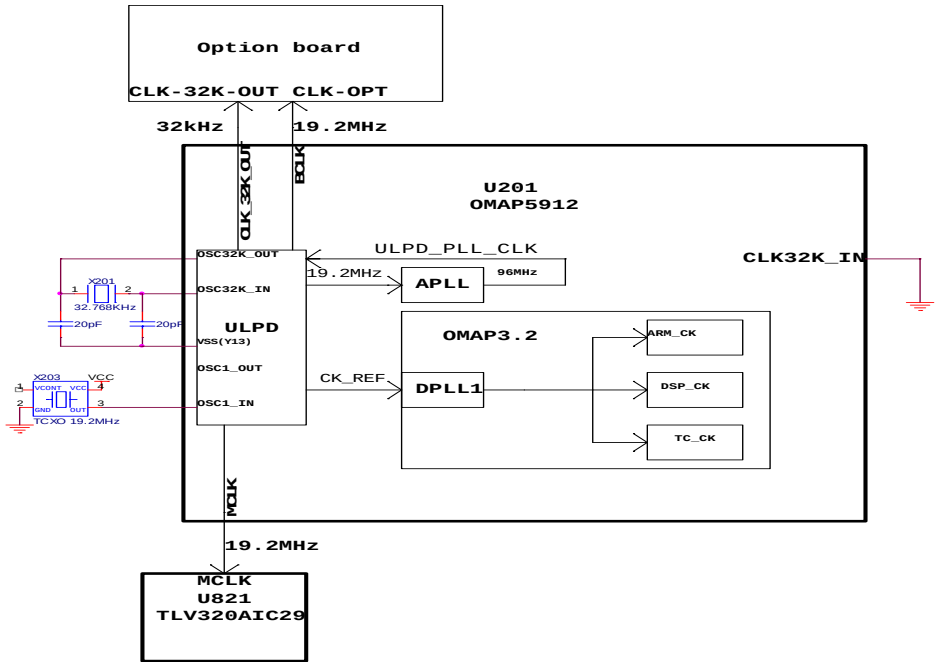

Figure 9 Diagram of Baseband Clock

Input Clock:

(A) 32K clock (also called “sleep clock”) is mainly used for timing and sleeping of the system.

(B) 19.2MHz clock is mainly used to provide input clock for APLL and DPLL.

Output Clock:

Three output clocks are provided: MCLK, BCLK and CLK32K_OUT. MCLK provides 19.2MHz clock to the audio codec; BCLK provides 19.2MHz clock to the optional board; and CLK32K_OUT provides 32KHz clock to the optional board.

2.4 Reset Signal

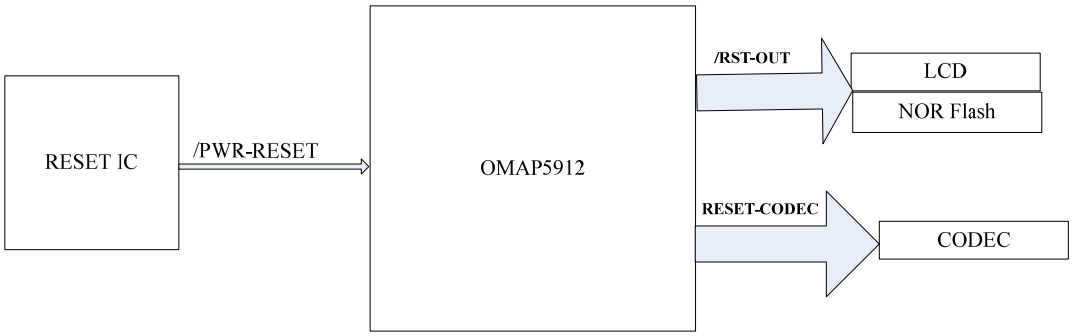

Figure 10 Diagram of Reset Circuit

2.5 SPI

OMAP5912 has a SPI, which has four chip-selects for connecting four external SPI components. The SPI signals available are SPI.DOUT, SPI.DIN, SPI.CLK and SPI.CS. The system uses SPIF.CS2 to select the IF processor AD9864, to configure register of AD9864. The connection of SPI is shown below.

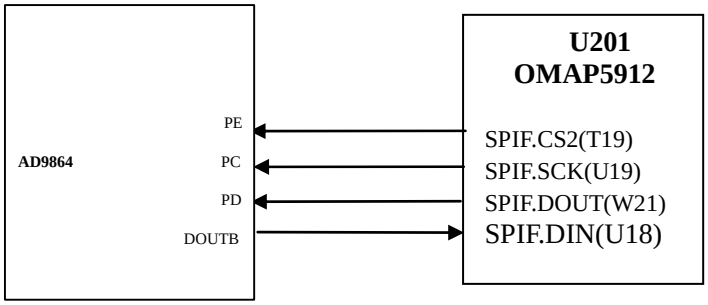

Figure 11 Diagram of SPI Connection

2.6 McBSP

OMAP5912 provides 3 McBSP interfaces: McBSP1, McBSP2 and McBSP3. McBSP1 is connected with the I2S interface of the audio codec, to realize two-way transmission of digital voice and data. McBSP2 uses independent clock and frame synchronization for transmission and reception. AD9864 SSI is connected to the RX end of OMAP5912 McBSP2. AD9864 works in master mode, while DSP works in slave mode. DAC is connected with TX end of McBSP2, and DSP works in master mode. McBSP3 is connected to the optional board. The connection of McBSP is shown below.

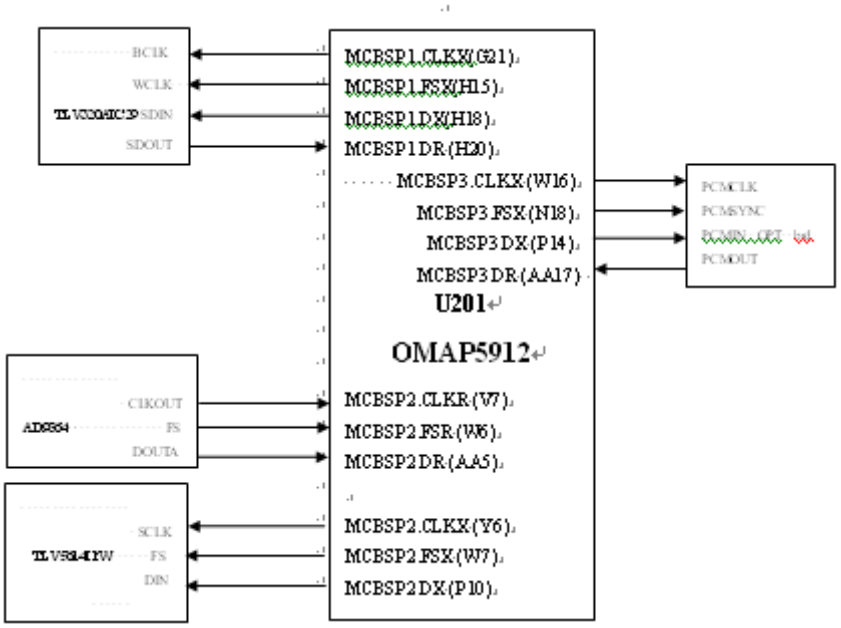

Figure 12 Diagram of McBSP Connection

2.7 USB

OMAP5912 provides 3 USB interfaces, one of which integrates USB transceiver. In this way, the design of USB interface is simplified. The integrated USB transceiver is connected to the accessory jack, and is used for program downloading and data applying.

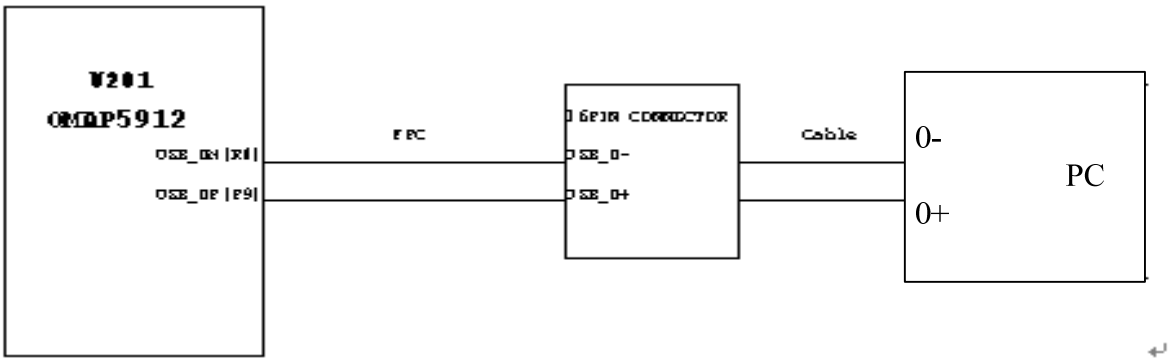

Figure 13 Diagram of USB Interface

2.8 UART

OMAP5912 has three UART interfaces (UART1, UART2 and UART3), and supports hardware flow control. The maximum communication rate is 1.5Mbps. The connection of UART is shown below. UART1 is connected with the accessory jack, and is used for updating and programming. UART2 is for GPS, and UART3 is for the optional board.

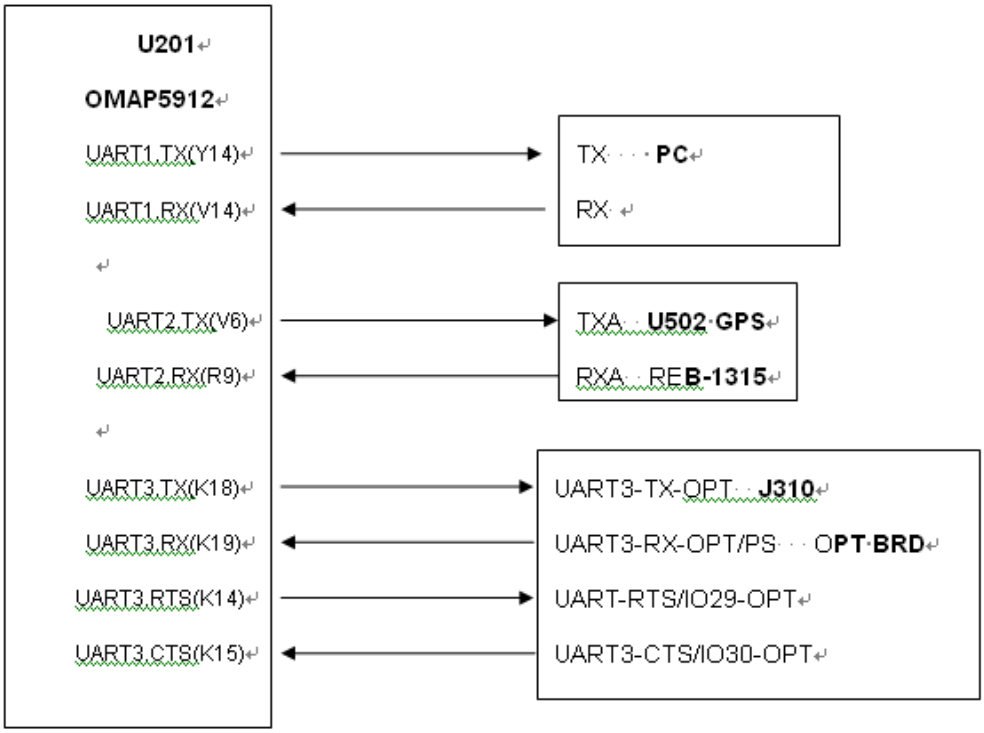

Figure 14 Diagram of UART Interface

2.9 I2C

OMAP5912 provides one I2C interface, and supports communication rate of up to 400Kbps. The I2C interface is connected with the acceleration sensor, and works in slave mode. The connection of I2C is shown below.

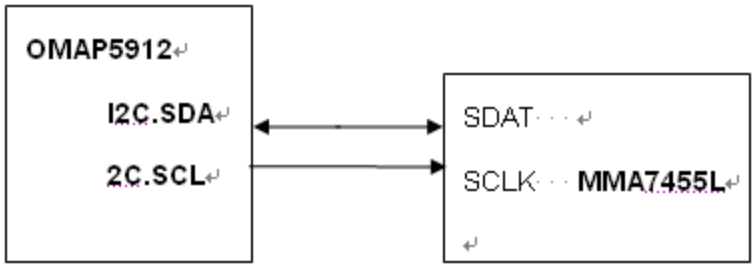

Figure 15 Diagram of I2C Connection

2.10 MICROWIRE

OMAP5912 provides a MICROWIRE. The four chip select signals can drive four external components. MICROWIRE is used to configure the audio codec and read the value of its register. It uses the chip select signal 3. The connection is shown below.

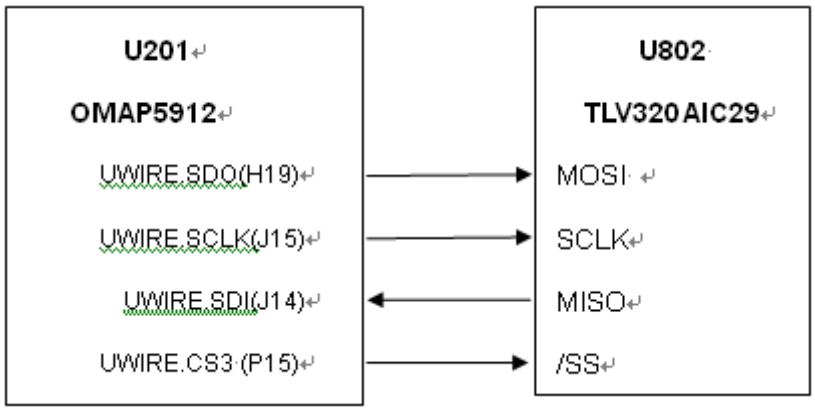

Figure 16 Diagram of MICROWIRE Connection

2.11 MCSI1

OMAP5912 has two MCSI interfaces. MCSI1 is used for PLL configuration and data transmission. The connection of MCSI1 is shown below.

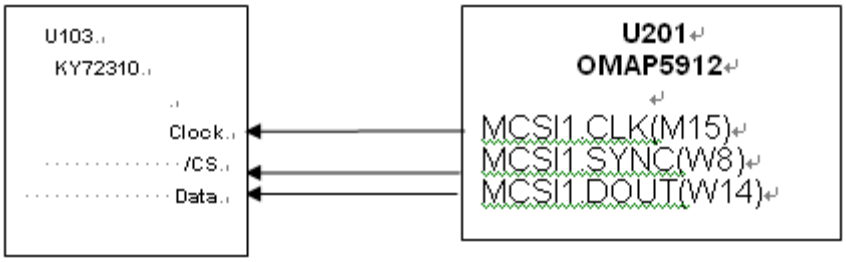

Figure 17 Diagram of SPI Connection

3 Power Supply Section

3.1 Power Control Diagram

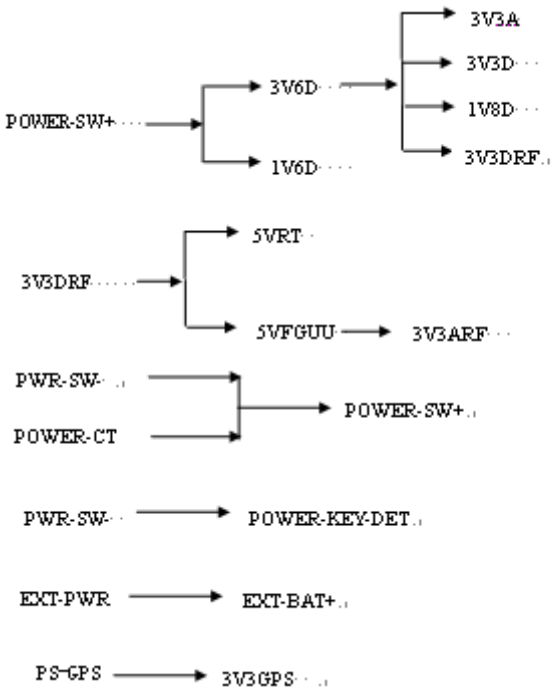

Figure 18 Diagram of Power Control

3.2 Radio On/Off

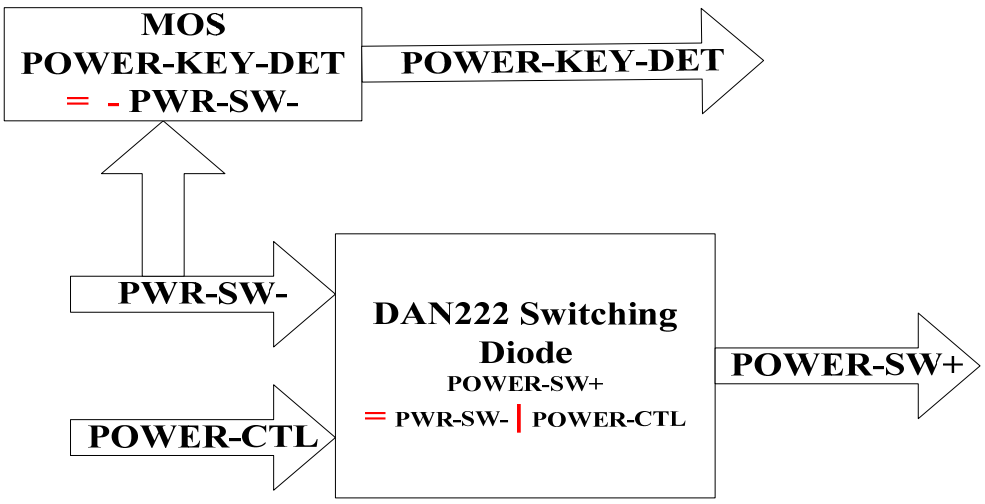

Figure 19 Diagram of Radio On/Off Control

The radio-on signal (POWER-SW+) satisfies the equation: POWER-SW+= PWR-SW- | POWER-CTL. When the Volume Switch is on, PWR-SW- and POWER-SW+ are at high level, and the radio powers up. After power-on, POWER-CTL goes to high level, and POWER-KEY-DET goes to low level. During power-off, POWER-SW+ is at low level, while POWER-KEY-DET is at high level. The system detects power-off procedure via POWER-KEY-DET and implements the power-off procedure. Then POWER-KEY-DET

and POWER-SW+ goes to low level, and the power is cut off.

3.3 Power Protection

Power protection includes over-current, reverse-voltage and ESD protection.

3.4 Power Consumption Control

OMAP can control and configure the power supply and working mode of the peripheral modules (RF section and BB section) via I/O port and serial bus, so as to reduce power consumption.

4 Audio Section

4.1 Audio Diagram

The audio module is mainly for audio input and output. TLV320AIC29 is used as the audio codec to convert and process audio signal and digital signal. The audio amplifier TDA8547TS is used to amplify the analog audio signal. DSP processes digital signal (audio signal encoding/decoding, digital I/Q signal decoding, digital audio signal processing). AD9864 converts and processes the RF IF signal, and sends the unmodulated serial digital I/Q signal to the DSP for processing. Then DAC5614 converts the digital signal output by DSP to analog signal.

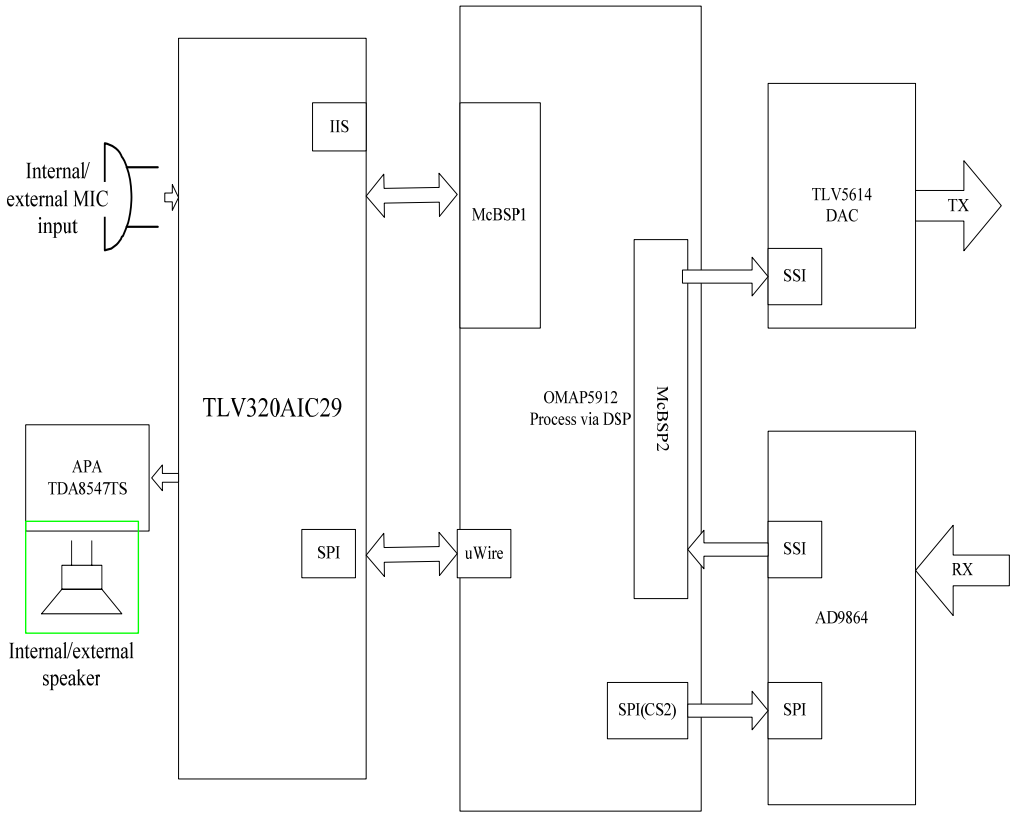

Figure 20 Diagram of Audio Section

4.2 Signal Flow Chart

The audio TX channel is shown as the red line in the figure below. The microphone converts the audio signal into electrical signal, which is amplified by PGA of the codec and then sent to ADC of the codec for sampling. After digital audio processing, the signal is output to DSP for processing. Then the signal is sent to DAC (TLV5614), which converts the signal to modulation signal. After modulated and amplified in the RF module, the signal is sent out from the antenna.

The audio RX channel is shown as the green line in the figure below. The RF signal received by the RF module is converted to digital signal by ADC (AD9864), and is then sent to DSP for modulating and processing. Then the digital signal is sent to the digital audio processor of the codec for digital audio processing, and is then converted into analog audio signal by DAC of the codec. Finally the signal is amplified by the external audio amplifier (TDA8547TS) to drive the speaker.

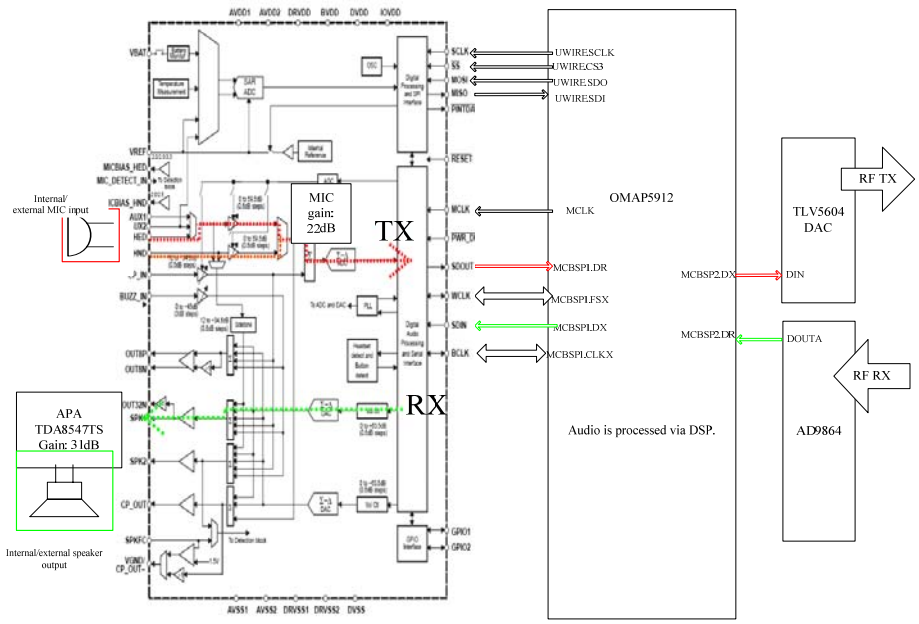

Figure 21 Diagram of Audio Signal Flow

4.3 Audio Amplifier

Main parameters of TDA8547TS are listed in the table below:

Rated Power (P_o)	0.5W	R_L =16Ω
Maximum Power (P_{max})	1.3W	R_L =16Ω
Rated Audio Distortion	3%	R_L =16Ω， P_o=0.9W

The operation status of the audio amplifier is controlled via GPIO of OMAP. See the table below.

Mode-Amp	SEL-SPK	MODE	SELECT	OUT
1	1	0	0	OUT2
1	0	0	1	OUT1
0	1	1	1	Standby