JUL 1, 2014 V1.6

SC14SPNODE SF
DECT Module with integrated Antenna and FLASH

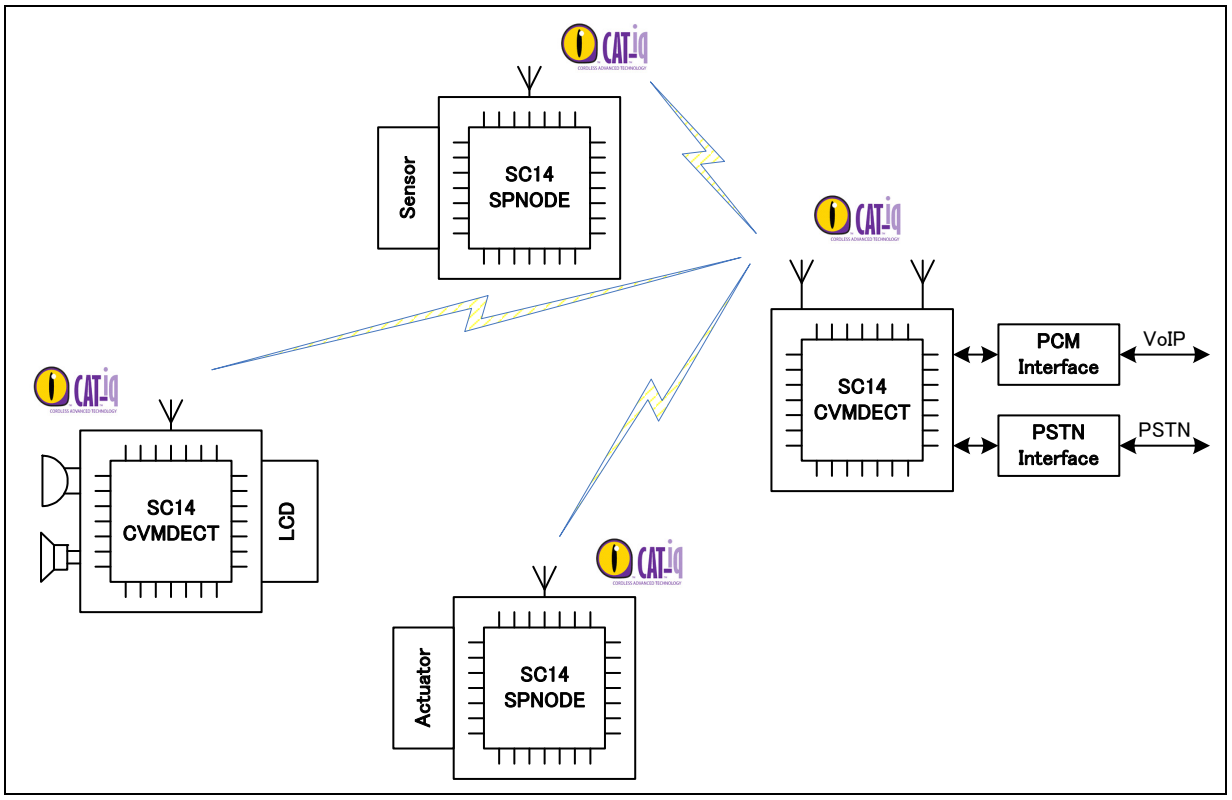
General description

The SC14SPNODE SF is a member of the Cordless Module family with an integrated radio transceiver and baseband processor in a single package. It is designed for voice and data applications in the DECT frequency band.

Features

- Ultra Low Power, sleep current < 3 µA
- ETSI (EU-DECT) and FCC (DECT 6.0) certified
- J-DECT pre-certified
- RF range: 1870 MHz to 1930 MHz
- Receiver sensitivity < -93 dBm
- Transmit power
  - EU: 24 dBm: 1881MHz - 1897MHz
  - USA: 20 dBm: 1921MH - 1928MHz
  - JP: 23 dBm: 1895MHz - 1903MHz
- Power supply voltage: 2.1 V to 3.45 V
- Supports NiMH and Li-Ion batteries
- Small form factor (19.6 mm x 18.0 mm x 2.7 mm)
- Program memory available for custom software.
- 16 Mbit Flash embedded
- Operating temperature range: -40 °C to +85 °C

System diagram



SC14SPNODE SF
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1.0 Connection diagram

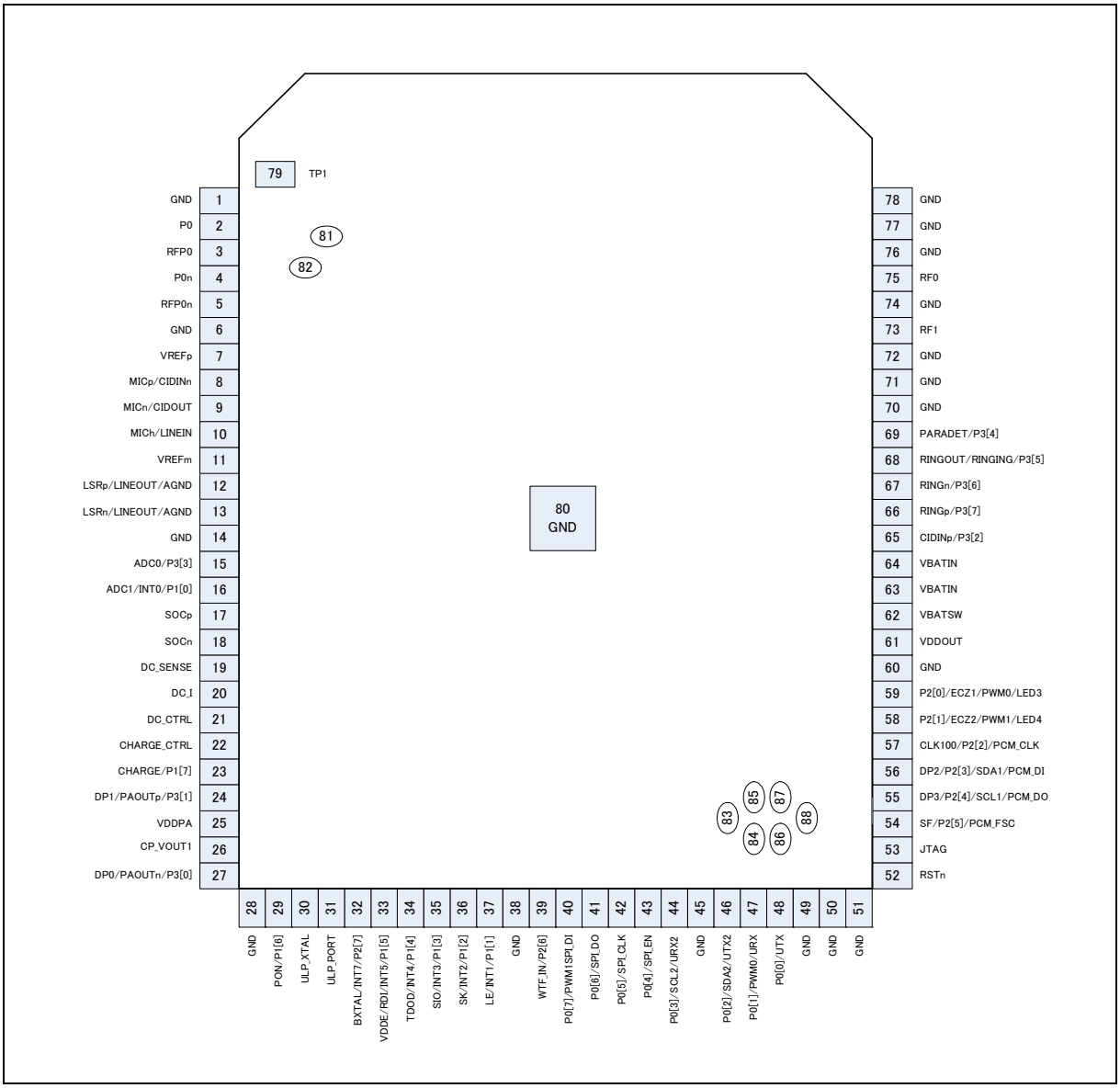


Figure 1 Connection diagram (top view, leads face down)

Order numbers:
SC14SPNODE SF01T (tray, MPQ = 600 pcs)

1.1 PIN DESCRIPTION

Table 1: Pin description

Pin	Module Pin name (Note 1)	In/ Out	Iout Drive (mA)	Reset State (Note 2)	Description
1	GND	-	-	-	Ground
2	P0	O	8	Hi-Z	Control port for FAD. See 2.6
3	RFP0	O	8	Hi-Z	Control port for FAD. See 2.6
4	P0n	O	8	Hi-Z	Control port for FAD. See 2.6
5	RFP0n	O	8	Hi-Z	Control port for FAD. See 2.6
6	GND	-	-	-	Ground
7	VREFp	O	-	I	Positive microphone supply voltage
8	CIDINn MICp	I	-	I	INPUT. Caller-id opamp negative input with switchable input protection enabled from start-up. INPUT. Positive microphone input.
9	CIDOUT/ MICn	IO	-	I	OUTPUT. Caller-id opamp output to ADC. INPUT. Negative microphone input.
10	MICh/ LINEIN	I	-	I	INPUT. Headset microphone input with fixed input protection INPUT. Line interface input with fixed input protection
11	VREFm	-	-	-	Negative microphone reference. This pin must also be connected to GND ground, but make sure that the microphone ground is directly routed to VREFm (VREFm is the star point).
12	LSRp/ LINEOUT/ AGND	O	-	O	OUTPUT. Positive loudspeaker output OUTPUT. To Line interface. OUTPUT. Buffered analog ground (0.9 V) if LSRP_MODE = 00.
13	LSRn/ LINEOUT/ AGND	O	-	O	OUTPUT. Negative loudspeaker output. OUTPUT. To Line interface. OUTPUT. Buffered analog ground (0.9 V) if LSRN_MODE = 00.
14	GND	-	-	-	Ground
15	P3[3]/ ADC0	IO	8	I	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. ADC0 input to ADC with programmable input protection enabled from reset. **(Note 4)**
16	P1[0]/ INT0/ ADC1	IO	2	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. Keyboard input interrupt. INPUT. ADC1 input to ADC with programmable input protection enabled from reset. **(Note 4)**
17	SOCp	I	-	I	Battery State Of Charge positive input. Connect to GND if not used.
18	SOCn	I	-	I	Battery State Of Charge negative input. Star point connected to the SOC resistor. Connect to GND if not used.
19	DC_SENCE	I		I	INPUT. Voltage sense input. Connected via a resistor divider to the output of the DC/C converter. Maximum 1.27 V Connect to GND if not used.
20	DC_I	I		I	Current sense input of DC/DC converter. Connect to GND if not used
21	DC_CTRL	O	2	O-PD (fixed 100k pull-down)	OUTPUT. Switching clock for the DC/DC converter, this pad is supplied with VBAT. Leave unconnected if not used.

Table 1: Pin description (Continued)

Pin	Module Pin name (Note 1)	In/ Out	Iout Drive (mA)	Reset State (Note 2)	Description
22	CHARGE_CTRL	O	1	O-0	ANALOG OUTPUT. Charge control pin. Supplied by internal VBAT if device is off else from AVD. Leave unconnected if not used.
23	CHARGE / P1[7]	I	-	I-PD (270k fixed pull-down)	INPUT. Charger connected indication and supply voltage for power management. Switches on the device if voltage > Vih_a3pad. Must be connected to charger via resistor R>(Vcharger_max-3 V)/10 mA (round to next largest value in range). An internal 10 ms hold circuit keeps device on if the charger voltage ripple momentarily drop below Vil_charge. This eliminates the use of expensive ripple filter. If used as port pin, the maximum input switching speed of this pin is 100 kHz. Leave unconnected if not used.
24	PAOUTp P3[1] DP1	IO	500	O-0 (5k fixed pull-down)	OUTPUT. CLASSD positive output to loudspeaker. OUTPUT. General purpose output. OUTPUT. DIP port DP1
25	VDDPA	I	-	-	CLASSD Audio Amplifier supply voltage up to 3.45 V. GND or leave unconnected if PAOUT/P3[1:0] ports are not used.
26	CP_VOUT1	O	-	I	Charge Pump Output 1. A capacitor of 1 µF to GND is internally connected to this pin.
27	PAOUTn P3[0] DP0	IO	500	O-0 (5k fixed pull-down)	OUTPUT. CLASSD negative output to loudspeaker. OUTPUT. General purpose output. OUTPUT. DIP port DP0
28	GND	-	-	-	Ground
29	PON/ P1[6]	I	-	I (270k fixed pull-down)	INPUT. Power on, Switches on the device if Voltage > Vih_a3pad. May be directly connected to VBAT. If used as port pin, the maximum input switching speed of this pin is 100 kHz.
30	ULP_XTAL	I	-	I	32.768 kHz XTAL clock input. Connect to GND if not used. **(Note 7)**
31	ULP_PORT	I	-	I	Ultra Low Power Port Pin. Connect to GND if not used. **(Note 7)**
32	P2[7]/ INT7 BXTAL	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. Keyboard Interrupt.connected to P1[2] or P2[7]. OUTPUT. Digital buffered Xtal oscillator. This pin is not optimized as reference clock for external RF devices.
33	P1[5]/ INT5/ RDI/ VDDE	IO	8	O-1	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. Keyboard input interrupt. INPUT. BMC Receive data (for monitoring/external radio). OUTPUT. P1[5] Used for supply of external EEPROM
34	P1[4]/ INT4/ TDOD	IO	1/2	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. 1 mA or 2 mA mode used to bias external NPN transistor without external resistor. INPUT. Keyboard input interrupt. OUTPUT. BMC transmit digital data.
35	P1[3]/ INT3/ SIO	IO	1/2	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. 1 mA or 2 mA mode used to bias external NPN transistor without external resistor. INPUT. Keyboard input interrupt. INPUT/OUTPUT. MicroWire data (for monitoring/external radio).
36	P1[2]/ INT2/ SK	IO	2	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. Keyboard input interrupt. OUTPUT. MicroWire clock (for monitoring/external radio).

Table 1: Pin description (Continued)

Pin	Module Pin name (Note 1)	In/ Out	Iout Drive (mA)	Reset State (Note 2)	Description
37	P1[1]/ INT1/ LE	IO	2	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. Keyboard input interrupt. INPUT. MicroWire latch enable. (for monitoring/external radio).
38	GND	-	-	-	Ground
39	P2[6]/ WTF_IN	IO	2	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. OUTPUT. Gen2DSP enable signal used to monitor DSP load
40	P0[7]/ SPI_DI/ PWM1	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. SPI data input. OUTPUT. Timer 0 PWM 1 output.
41	P0[6]/ SPI_DO	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. OUTPUT. SPI data output.
42	P0[5]/ SPI_CLK	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT/OUTPUT. SPI clock.
43	P0[4]/ SPI_EN	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT/OUTPUT. SPI clock enable. Active low.
44	P0[3]/ SCL2/ URX2	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT/OUTPUT. ACCESS bus 2 clock with programmable Push-pull or open drain. In open drain mode, SCL2 is monitored to support bit stretching by a slave. INPUT. UART2 receive data
45	GND	-	-	-	Ground
46	P0[2]/ SDA2/ UTX2	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT/OUTPUT. ACCESS bus 2 data with programmable. Push-pull or open drain. OUTPUT. UART2 transmit data
47	P0[1]/ URX/ PWM0	IO	8	I-PD (10k)	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. UART receive data. OUTPUT. Timer 0 PWM0
48	P0[0]/ UTX	O	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. OUTPUT. UART transmit data.
49	GND	-	-	-	Ground
50	GND	-	-	-	Ground
51	GND	-	-	-	Ground
52	RSTn	I	1	I-PU (200k pull-up)	Active low Reset input with Schmitt-trigger input, open-drain output and pull up resistor to internal VDD. Input may not exceed 2.0 V. An internal capacitor of 47 nF is mounted on this pin.
53	JTAG	IO	8	I-PU	JTAG-SDI+; one wire Debug interface with open-drain. Requires external 1 kΩ Pull-up to VDD.
54	P2[5]/ PCM_FSC/ SF	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT/OUTPUT. PCM Frame Sync. OUTPUT. S-field Sync found signal indicating the 00 or 11 preamble to unique word transition with 96 ns resolution. Used for debugging purposes.
55	P2[4]/ SCL1/ PCM_DO/ DP3	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT / OUTPUT. ACCESS bus 1 clock with programmable Push-pull or open drain. In open drain mode, SCL1 is monitored to support bit stretching by a slave. OUTPUT. PCM data output. OUTPUT. DIP port DP3.

Table 1: Pin description (Continued)

Pin	Module Pin name (Note 1)	In/ Out	Iout Drive (mA)	Reset State (Note 2)	Description
56	P2[3]/ SDA1/ PCM_DI/ DP2	IO	8	I-PU	INPUT/OUTPUT with selectable pull up/down resistor. INPUT / OUTPUT. ACCESS bus 1 data with programmable Push-pull or open drain. INPUT. PCM data input. OUTPUT. DIP port DP2.
57	P2[2]/ PCM_CLK/ CLK100	I/O	8	I-PD	INPUT/OUTPUT with selectable pull up/down resistor. INPUT/OUTPUT. PCM clock. OUTPUT. DIP 100 Hz output.
58	P2[1]/ ECZ2/ PWM1/ LED4	IO	8	I	INPUT/OUTPUT with selectable pull up/down resistor. OUTPUT. Gen2DSP output port. OUTPUT. Timer 0 PWM 1 output. LED4: 2.5 mA/5 mA LED current sink.
59	P2[0]/ ECZ1/ PWM0/ LED3	IO	8	I	INPUT/OUTPUT with selectable pull up/down resistor. OUTPUT. Gen2DSP output port. OUTPUT. Timer 0 PWM 0 output. LED3: 2.5 mA/5 mA LED current sink.
60	GND	-	-	-	Ground
61	VDDOUT	-	-	-	Test purpose only. Must be left unconnected. See 2.5
62	VBATSW				Test purpose only. Must be left unconnected. See 2.5
63	VBATIN	I	-	-	Main supply voltage < 3.45 V. See 2.5
64	VBATIN	I	-	-	Main supply voltage < 3.45 V. See 2.5
65	P3[2]/ CIDINp/	IO	8	I	INPUT/OUTPUT with selectable pull up/down resistor. INPUT. Caller-id opamp positive input with switchable input protection enabled from start-up.
66	P3[7]/ RINGp	IO	4	I	INPUT/OUTPUT with selectable pull up/down resistor. ANALOG INPUT. Positive ringing signal opamp input with switchable input protection.
67	P3[6] / RINGn	IO	4	I	INPUT/OUTPUT with selectable pull up/down resistor. ANALOG INPUT. Negative ringing signal opamp input with switchable input protection.
68	P3[5]/ RINGOUT/ RINGING	IO	4	I	INPUT/OUTPUT with selectable pull up/down resistor. OUTPUT. Ringing opamp output to ADC. INPUT. Ringer signal detection input to capture timers and ADC.
69	P3[4]/ PARADET	IO	8	I	INPUT/OUTPUT with selectable pull up/down resistor. ANALOG INPUT. Parallel set detection input to ADC with switchable input protection.
70	GND	-	-	-	Ground
71	GND	-	-	-	Ground
72	GND	-	-	-	Ground
73	RF1	-	-	-	RF signal for external antenna. See 2.6
74	GND	-	-	-	Ground
75	RF0	-	-	-	RF signal for external antenna. See 2.6
76	GND	-	-	-	Ground
77	GND	-	-	-	Ground
78	GND	-	-	-	Ground
79	TP1	-	-	-	Tuning point for internal antenna. Follow instructions of section 4.3.
80	GND	-	-	-	Ground

Table 1: Pin description (Continued)

Pin	Module Pin name (Note 1)	In/ Out	Iout Drive (mA)	Reset State (Note 2)	Description
81-88	TP2 to TP9	NC			Must be left unconnected. See section 4.1 and Figure 15.

Note 1: "NC" means: leave unconnected.
"GND" means internally connected to the module ground plane. Every GND pin should be connected to the main PCB.ground plane.

Note 2: All digital inputs have Schmitt trigger inputs. After reset all I/Os are set to input and all pull-up or pull-down resistors are enabled unless otherwise specified.
PU = Pull-up resistor enabled, PD = Pull-down resistor enabled, I = input,
O = output, Hi-Z = high impedance, 1 = logic HIGH level, 0 = logic LOW level
Refer also to Px_DIR_REGs for INPUT/OUTPUT and Pull-up/Pull-down configurations

Note 3: Back drive protected pins allow always interfacing with devices up to a supply voltage of 3.45 V.
If PAD_CTRL_REG[xxx_OD] bit is set then
1) the internal Pull-up resistors are always disabled to prevent currents from 1.8 V < Vin < 3.45 V to VDD.
2) If port is set to output, the output is always configured as open drain to allow the output level to reach Vin >1.8 V. The external pull-up resistor value determines the rise time of the signal.

Note 4: For base station applications with high line input voltages, an input protection on all ADC inputs can be enabled with AD_CTRL_REG[ADCx_PR_DIS] ='0'. To limit the input current as specified in chapter "specifications", an external resistor must placed in series with the ADC inputs. With the input protection enabled, the ADC is linear from 0 to 0.9 V. With ADCx_PR_DIS='1' the ADC0 and ADC1 are linear from 0 V to 1.8 V.

Note 5: In digital mode extra static VDDPA current will flow (See Supply currents (indicative value) (table 9, page 14)). So the digital mode is not recommended in portable applications.The reason for this output overvoltage protection is that a speaker is an inductor (which can store energy). In case the battery is removed from the handset while handsfree speaker is active, the battery voltage could become too high when the inductor releases its energy to the battery (which is not present anymore as a buffer). To prevent this electrical overstress situation, the overvoltage protection is added.

Note 6: This pin description describes all function that is supported by hardware. Supported pin function depends on installed software.

Note 7: All ULP pins use snap-back devices as ESD protection, which (when triggered) have a holding voltage below the typical battery voltage. This means that the snap-back device of a ULP pin may remain conductive, when triggered while the pin is directly connected to the battery voltage. If any of the ULP pins are directly or indirectly electrically accessible on the outside of the application, system level ESD precautions must be taken to ensure that the snap-back device is not triggered while in active mode, to prevent the chip from being damaged.

2.0 Introduction

2.1 SCOPE

The SC14SPNODE SF is a programmable DECT module for voice and data services, Ultra Low Energy (ULE) sensor applications and actuator applications.

This module includes a fully integrated DECT RF and baseband processor, 16 Mbit QSPI FLASH, one internal antenna, two antenna switches and a 20.736 MHz crystal. Customer end products can be designed by adding just a few components to this module.

Customer and Dialog software are stored in the internal 16 Mbit QSPI FLASH.

Dialog standard software for the SC14SPNODE supports:

- EU-DECT (CAT-iq V2.0, V3.0), DECT6.0 for North American and Japan DECT.
- ETSI certified
- ETSI 300 444 (DECT GAP) compliant
- FCC approved, Japan DECT pre-certified

The end product must undergo certification testing again if other software than Dialog standard software stack is used.

Dialog will provide the following standard software stacks:

- Wireless sensor application with ULE
- Wireless actuator application with ULE
- Cordless Voice module application

2.2 REFERENCES

1. AN-D-207, External Antenna design guidelines for the SC14 Module, Dialog Semiconductor, Application note
2. AN-D-174, SC14480 Battery Management; using the State of Charge function, Dialog Semiconductor, Application Note
3. MX25U1635E, Macronix, Data sheet
4. Dialog Semiconductor web page to get software release information: http://www.dialog-semiconductor.com/products/short-range-wireless-technology/software-stacks
5. AN-D-204, RF settings in Natalie, Dialog Semiconductor, Application note

2.3 GLOSSARY AND DEFINITIONS

AFE	Analog Front End
CAT-iq	Cordless Advanced Technology, Internet and Quality
Codec	Coder and Decoder converts analog signals to digital signals and vice versa
CVM	Cordless Voice Module
DECT	Digital Enhanced Cordless Telephone
EMC	Equipment Manufacturer's Code
ESD	ElectroStatic Discharge
FAD	Fast Antenna Diversity
FP	Fixed Part
GAP	General Access Profile (DECT)
IPEI	International Portable Equipment Identity (ETSI EN 300 175-6)
IWU	Inter Working Unit (ETSI EN 300 175-1)
MCU	Micro Controller Unit
MMI	Man Machine Interface (keypad, LCD, buzzer, microphone, earpiece, speaker, headset)
NSMD	Non Solder Mask Defined (pad)
NTP	Normal Transmitted Power
OTP	One Time Programmable
PCB	Printed Circuit Board without components
PP	Portable Part
PSTN	Public Switched Telephone Network
RF	Radio Frequency
RFPI	Radio Fixed Part Identity (ETSI EN 300 175-6)
RLR	Receive Loudness Rating
RSSI	Radio Signal Strength Indication (ETSI EN 300 175-1)
Sidetone	Feedback of microphone signal to earpiece
SLR	Sending Loudness Rating
SPI	Serial Peripheral Interface Bus
TDD	Time Division Duplex
UART	Universal Asynchronous Receiver and Transmitter
ULE	Ultra Low Energy
VES	Virtual EEPROM Storage

2.4 BLOCK DIAGRAM

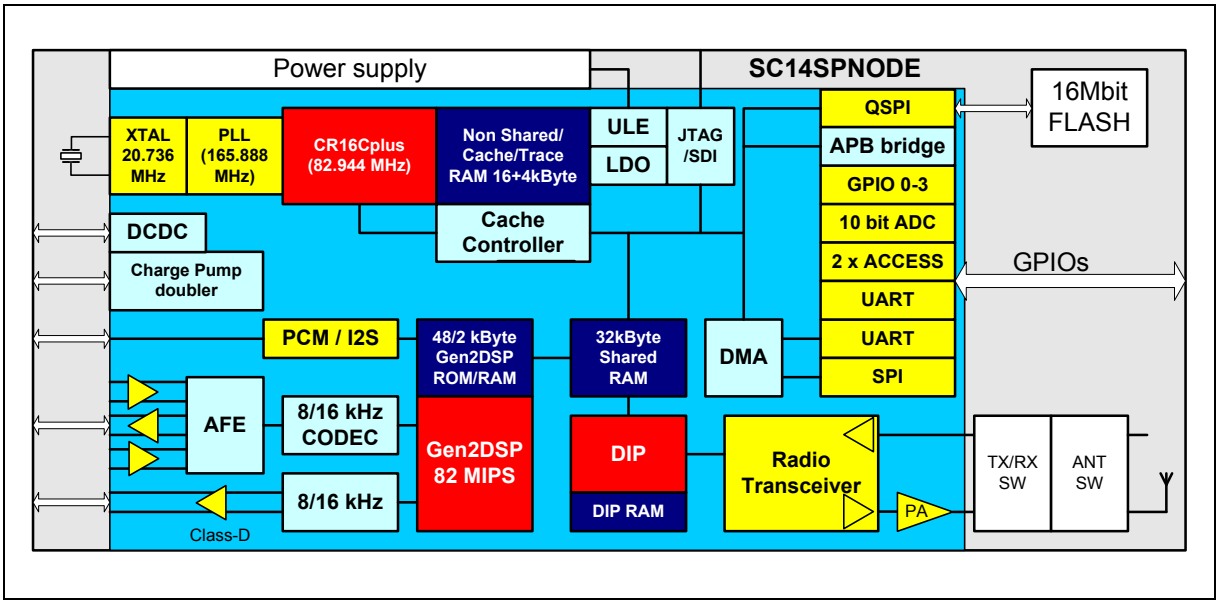


Figure 2 SC14SPNODE hardware block diagram

2.5 POWER SUPPLY

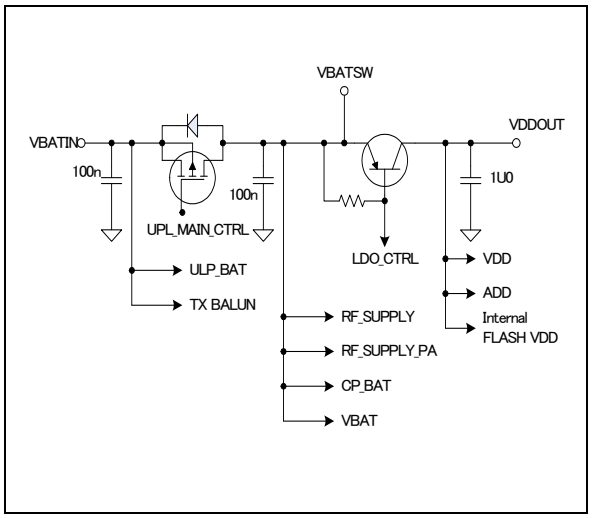


Figure 3 Internal circuit of the power supply

Figure 3 shows the internal power supply circuit of the SC14SPNODE SF.

2.6 ANTENNA OPERATION

Figure 4 shows the internal antenna circuit of the SC14SPNODE SF. Pin RF0 is used for two external antennas and can also be used for RF test purposes, so it is recommended to add a 10 pF capacitor as reserve pattern even when the two external antennas are not used.

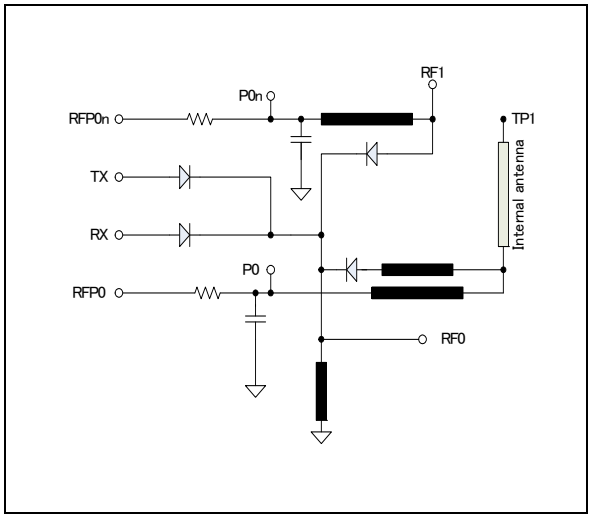


Figure 4 Internal circuit of the antenna part

Re-certification of the SC14SPNODE SF is required if at least one external antenna is added. On request, Dialog Semiconductor can provide a pre-certified PCB layout for an external antenna circuit.

RF1 is also recommended to use and can be connected to the RF cable to be able to do the JPN DECT type approval test.

2.6.1 Internal antenna only

The FAD function is not enabled if only the internal antenna is used. In this case RFP0, RFP0n, P0 and P0n must be left unconnected.

2.6.2 Internal and external antenna with FAD

Figure 5 shows one external antenna that is connected to RF1 of the SC14SPNODE SF. This configuration supports the FAD function. In this case pins RFP0, RFP0n, P0 and P0n must be left unconnected. The software patch code is not needed if the SC14SPNODE SF is operated as FP.

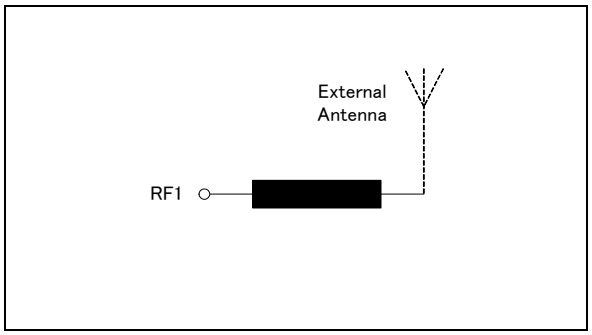


Figure 5 One external antenna

2.7 BATTERY MANAGEMENT

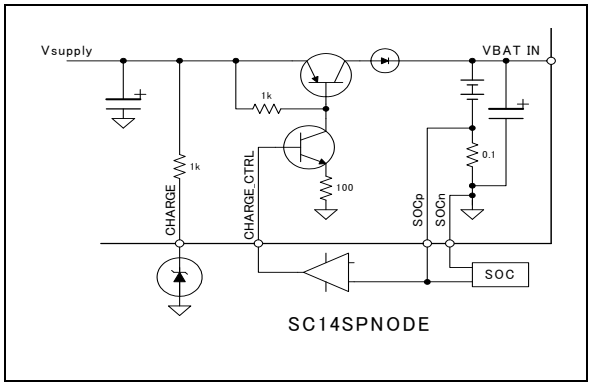


Figure 6 Handset (PP) application with 2x NiMH

Figure 6 shows a handset application with NiMH. SOC (State Of Charge) is used to measure the amount of charge in the rechargeable batteries.

Figure 7 shows an FP application. The FP uses an external LDO, so the SOC pins are not used and can be connected to GND.

The SOC circuit is used to very accurately determine the amount of charge in rechargeable batteries as well as the discharge state of Alkaline batteries. This information is essential for the battery charging algorithm and necessary for battery status indication to the user. Detailed information can be found in AN-D-174 (see Reference [2]).

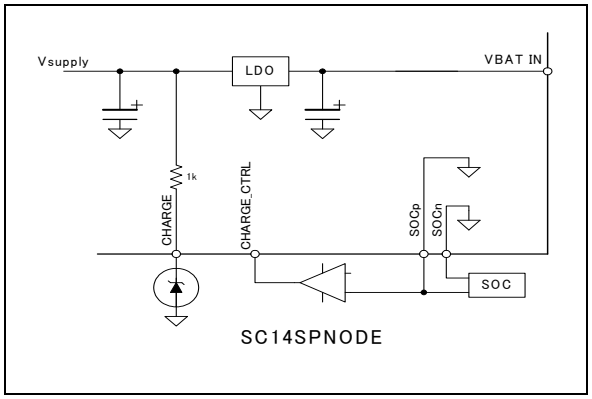


Figure 7 Base station (FP) application

Pin CHARGE_CTRL is driven high when either “sensed voltage on the VBAT pin” is lower than the voltage setting (defined by the module hardware) or “sensed current via SOCp” is lower than the current setting (defined by the module hardware). Pin CHARGE_CTRL can drive up to 500 µA as source current (see Table 19).

2.8 EMBEDDED QSPI FLASH

The SC14SPNODE SF has a QSPI FLASH with type number MX25U1635E as embedded FLASH. Please refer to Reference [3] for detailed specifications.

The MX25U1635E has an OTP area, a part of which has already been factory programmed by Dialog for tuning purposes.

Table 2 shows the production parameters and the relation between the SC14SPNODE SF register address and the OTP address.

The OTP addresses from 0x020 to 0x1FF are available for write access before locking the OTP.

Table 2: SC14SPNODE production parameters

Register name	SC14SPNODE address	OTP address	Alignment Spec.
RF_BURST_MODE_CTRL_REG[MODINDEX]	0xFF7053[5:0]	0x05	340 kHz to 370 kHz
CLK_FREQ_TRIM_REG (lsb)	0xFF400A	0x06	20.736 MHz +/- 1 ppm
CLK_FREQ_TRIM_REG (msb)	0xFF400B	0x07	
BANDGAP_REG	0xFF4810	0x08	1.8 V +/- 1%

3.0 Specifications

All MIN/MAX specification limits are guaranteed by design, or production test, or statistical methods unless note 8 is added to the parameter description. Typical values are informative.

Note 8: This parameter will not be tested in production. The MIN/MAX values are guaranteed by design and verified by characterization.

3.1 GENERAL

Table 3: SC14SPNODE SF module

ITEM	CONDITIONS	VALUE	UNIT
Dimensions	l x w x h	**18.0 x 19.6 x 2.7**	**mm**
Weight		**1.5**	**g**
Temperature range		**-40 to +85**	**°C**
Frequency range	According to DECT standard	**1870 to 1930**	**MHz**
Antenna range	According to DECT standard; **(Note 9)**		
	- typical outdoor	**350**	**m**
	- typical indoor	**75**	**m**
Standards compliancy	ETS 300 444 (DECT GAP), former TBR2214 FCC part 15		
Power supply	2 cell NiCd/NiMH Note: for 1 Li-Ion battery an external LDO is required.	**2.10 to 3.45**	**V**
Maximum PCB warpage	For entire reflow range	**0.1**	**mm**

Note 9: The resulting range is very dependent of the mechanical design. Dialog Semiconductor is not responsible for this design and as such Dialog Semiconductor is not responsible for the resulting performance range of the final product.

3.2 ABSOLUTE MAXIMUM RATINGS

Table 4: Absolute Maximum Ratings (Note 10)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	MAX	UNIT
Vbat_max	Max voltage on pin VBATIN, VDDPA			**3.45**	**V**
Vpon_max	Max voltage on pin PON			**5.5**	**V**
Vled_max	Max voltage on pin LED4, LED3			**3.6**	**V**
Vdig_bp_max	Max voltage on digital pins with back drive protection; ports P0 and P2 (except P2.6)			**3.6**	**V**
Vdig_max	Max voltage on other digital pins			**2.0**	**V**
Vana_max	Max voltage on analog pins			**2.2**	**V**
Vesd_hbm	ESD voltage according to human body model; all pins			**2000**	**V**
Vesd_mm	ESD voltage according to machine model; all pins			**150**	**V**

Note 10: Absolute maximum ratings are those values that may be applied for maximum 50 hours. Beyond these values, damage to the device may occur.

3.3 OPERATING CONDITIONS

Table 5: Operating Conditions (Note 11)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vbat	Supply voltage on pin VBATIN		**2.1**		**3.45**	**V**
Vdd_pa	CLASSD supply voltage on pin VDDPA		**2.1**		**3.45**	**V**
Vpon	Voltage on pin PON				**5.5**	**V**
Vdig_bp	Voltage on digital pins with back drive protection; ports P0 and P2 (except P2.6)				**3.45**	**V**
Vdig	Voltage on other digital pins	VDD = 1.8 V			**1.98**	**V**
Vana	Voltage on analog pins	AVD = 1.8 V			**2.1**	**V**
Icharge	Current through pin CHARGE	Rseries > (Vcharge-3 V)/ 10 mA			**10**	**mA**
Ipa	Current through pin PAOUTp, PAOUTn	**(Note 12)**			**500**	**mA**
Iout_vrefp	Output current through pin VREFp				**1**	**mA**
TA	Ambient temperature	**(Note 13)**	**-40**		**+85**	**°C**

Note 11: Within the specified limits, a life time of 10 years is guaranteed.
Note 12: A life time of 10 years of the CLASS-D amplifier is guaranteed if switched on for 10% of the time.
Note 13: Within this temperature range full operation is guaranteed.

3.4 DIGITAL INPUT/OUTPUT PINS

Table 6: Digital input levels

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vil_dig	Logic 0 input level; all digital input pins except PON, CHARGE and RSTn	VDD = 1.8 V			**0.3*VDD**	**V**
Vil_pon	Logic 0 input level; pin PON				**0.9**	**V**
Vil_charge	Logic 0 input level; pin CHARGE				**0.9**	**V**
Vil_rst	Logic 0 input level; pin RSTn	VDD = 1.8 V			**0.2*VDD**	**V**
Vih_dig	Logic 1 input level; all digital input pins except PON, CHARGE and RSTn	VDD = 1.8 V	**0.7*VDD**			**V**
Vih_pon	Logic 1 input level; pin PON		**1.5**			**V**
Vih_charge	Logic 1 input level; pin CHARGE		**1.5**			**V**
Vih_rst	Logic 1 input level; pin RSTn	VDD = 1.8 V	**0.8*VDD**			**V**

Table 7: Digital output levels

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vol_dig	Logic 0 output level	VDD = 1.8 V; Iout = 2, 4, 8 mA **(Note 14)**			**0.2*VDD**	**V**
Voh_dig	Logic 1 output level	VDD = 1.8 V; Iout = 2, 4, 8 mA **(Note 14)**	**0.8*VDD**			**V**

Note 14: For output drive capability, see section "Pin Description" on page 4.

3.5 ULTRA LOW ENERGY (ULE) I/O PIN

Table 8: ULP_PORT specifications

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Vil_ulp	Logic 0 input level; pin ULP_PORT	Vbat = 2.1 V to 3.45 V			**0.2*Vbat**	**V**
Vih_ulp	Logic 1 input level; pin ULP_PORT	Vbat = 2.1 V to 3.45 V	**0.8*Vbat**			**V**
Vol_ulp	Logic 0 output level; pin ULP_PORT	Iout = 1 mA, Vbat = 2.4 V			**0.2*Vbat**	**V**
Voh_ulp	Logic 1 output level; pin ULP_PORT	Iout = 1 mA, Vbat = 2.4 V	**0.8*Vbat**			**V**
Ipull_up_ulp	Input current with pull up enabled; pin ULP_PORT	Vin = GND		**2.5**		**µA**
Ipull_down_ulp	Input current with pull down enabled; pin ULP_PORT	Vin = Vbat; Vbat = 2.1 V to 3.45 V		**2.5**		**µA**

3.6 SUPPLY CURRENTS

Table 9: Supply currents (indicative value)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	Unit
Iavd_pa	CLASSD normal mode supply current at AVD	CLASSD_PD=0		**3.5**		**mA**
Iavd_paport	CLASSD digital port mode supply current at AVD	(P3_0_MODE = 00 or P3_1_MODE = 00) and CLASSD_PD=1. **(Note 15)**		**5**		**µA**

Note 15: PAOUTp and PAOUTn have internal fixed resistors connected to VSSPA. The values are 5 kΩ if CLASSD[CLASSD_VOUT] = 01, else 6 kΩ. So in digital mode with a '1' on output a small static current will flow.

3.7 ANALOG FRONT END

Table 10: Microphone amplifier

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vmic_0dB_unt	Untrimmed differential RMS input voltage between MICp and MICn (0 dBm0 reference level) **(Note 8)**	0 dBm0 on COUT **(Note 17)** MIC_GAIN[3:0] = 0, @ 1020 Hz; Tolerance: • 13% when untrimmed (BANDGAP_REG=8) **(Note 16)** • 6% when trimmed **(Note 18)**	**114**	**131**	**149**	**mV**
Rin_mic	Resistance of activated microphone amplifier inputs (MICp, MICn and MICh) to internal GND **(Note 8)**		**75**	**150**		**kΩ**
Vmic_offset	Input referred DC-offset **(Note 8)**	MIC_GAIN[3..0] = 1111 3 sigma deviation limits	**-2.6**		**+2.6**	**mV**

Note 16: BANDGAP_REG will be tuned at the factory.

Note 17: 0 dBm0 on COUT = -3.14 dB of max PCM value. COUT is CODEC output in test mode

Note 18: Trimming possibility is foreseen. At system production the bandgap reference voltage can be controlled within 2% accuracy and data can be stored in Flash. Either AVD or VREF can be trimmed within 2% accuracy. If AVD is trimmed VREF will be within 2% accuracy related to either AVD. Or vice versa VREF can be trimmed. For Vref trimming measure Δ (VREFp, VREFm) and update BANDGAP_REG[3..0].

Table 11: Microphone amplifier (Operating Condition)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vmic_cm_level	MICp and MICn common mode voltage	MICp and MICn are set to GND with internal resistors (Rin_mic). If DC coupled the input voltage must be equal to this voltage.		**(0.9 V/1.5)* VREFp**		**V**

Table 12: Microphone supply voltages

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vref_unt	VREFp-VREFm untrimmed **(Note 19)**	I_{LOAD} = 0 mA BANDGAP_REG = 8 **(Note 18)**	**1.41**	**1.5**	**1.59**	**V**
Rout_vrefp	VREFp output resistance	Figure 8		**1**		**Ω**
Nvrefp_idle	Peak noise on VREFp-VREFm **(Note 8)**	CCITT weighted			**-120**	**dBV**
PSRRvrefp	Power supply rejection Vref output **(Note 8)**	See Figure 8, AVD to VREFp/m, f = 100 Hz to 4 kHz BANDGAP_REG[5:4] = 3	**40**			**dB**

Note 19: Vrefm is a clean ground input and is the 0 V reference.

Table 13: VREFp load circuit

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Cload_vrefp	VREFp (parasitic) load capacitance				**20**	**pF**
Iout_vrefp	VREFp output current				**1**	**mA**

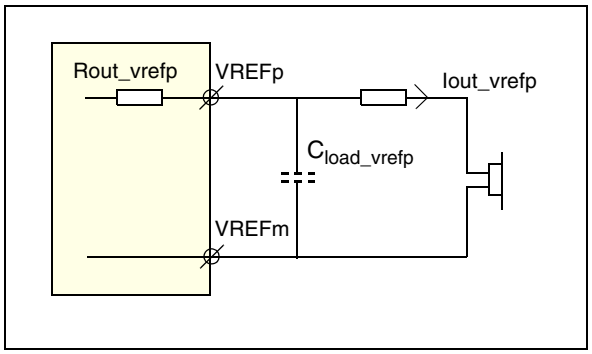


Figure 8 VREFp load circuit

Table 14: LSRp/LSRn outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vlsr_0dB_unt	Untrimmed differential RMS output voltage between LSRp and LSRn in audio mode (0 dBm0 reference level)	0 dBm0 on CIN **(Note 20)**, LSRATT[2:0] = 001, @ 1020 Hz Load circuit A (see Figure 9, Table 15) with RL1= ∞ Ω, Cp1 or load circuit B (see Figure 10) with RL2, Cp2 and Cs2 Tolerance: • 13% when untrimmed (BANDGAP_REG=8) • 6% when trimmed **(Note 18)**	**621**	**714**	**807**	**mV**
Rout_lsr	Resistance of activated loudspeaker amplifier outputs LSRp and LSRn			**1**		**Ω**
Vlsr_dc	DC offset between LSRp and LSRn **(Note 8)**	LSRATT[2:0] = 3 R_{L1} = 28 Ω 3 sigma deviation limits	**-20**		**20**	**mV**

Note 20: 0 dBm0 on CIN = -3.14 dB of max PCM value.

Table 15: LSRp/LSRn load circuits

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Cp1_Rl1_inf	Load capacitance	see Figure 9, $R_{L1} = \infty$			**30**	**pF**
Cp1_Rl1_1k	Load capacitance	see Figure 9, $R_{L1} \leq 1\ k\Omega$			**100**	**pF**
Rl1	Load resistance		**28**			**Ω**
Cp2	Parallel load capacitance	see Figure 10			**30**	**pF**
Cs2	Serial load capacitance				**30**	**µF**
Rl2	Load resistance		**600**			**Ω**

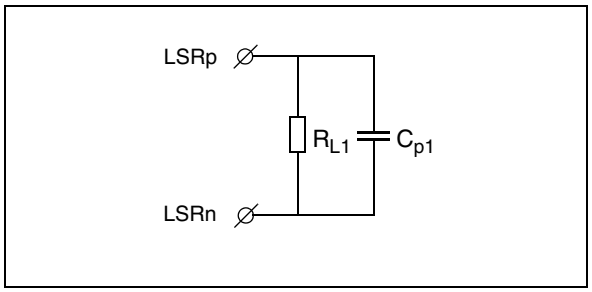


Figure 9 Load circuit A: Dynamic loudspeaker

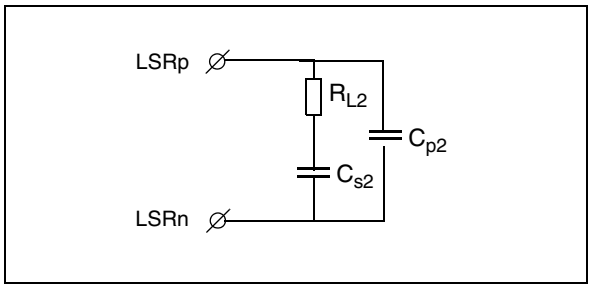


Figure 10 Load circuit B: Piezo loudspeaker

Table 16: PAOUTp, PAOUTn outputs

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vpa_4v	Differential rms output voltage between PAOUTp and PAOUTn	Trimmed bandgap input = 0 dBm0, 1 kHz **(Note 17)** Output low-pass filtered CLASSD_VOUT = 0		**0.985**		**Vrms**
Vpa_6v		As above CLASSD_VOUT = 1		**1.478**		**Vrms**
Zload_pa_4v	Speaker impedance, connected between PAOUTp and PAOUTn	With these values, the peak currents stays within the operating range.	**4**			**Ω**
Zload_pa_6v			**6**			**Ω**

Table 17: PAOUTp, PAOUTn outputs (Note 21)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Rout_pa	Differential output resistance between PAOUTp and PAOUTn	See **(Note 21)**		**1**		**Ω**

Note 21: Clipping of the outputs occurs when the VDDPA drops and the following conditions becomes true. If CLASSD_CTRL_REG[CLASSD_CLIP] is not equal to zero then upon a programmable number of clipping occurrences a CLASSD_INT is generated:
The software can stop clipping by reducing the gain via the GENDSP:

Clipping occurs if $\frac{peak(LowPassFiltered(PAOUTp - PAOUTm))}{VDDPA - VSSPA} > \frac{Zload}{Zload + Rout\_pa}$

Table 18: PAOUTp, PAOUTn external components

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
C_VDDPA	Decoupling capacitor on VDDPA	Required when Class-D is used and guaranteed life time. (see Figure 11)		1		µF
Cs_PAOUT	Snubber capacitor (to reduce ringing at PAOUTp/n)	Required when Class-D is used to prevent EMI and guaranteed life time. (see Figure 11)		1		nF
Rs_PAOUT	Snubber resistor (to reduce ringing at PAOUTp/n)	Required when Class-D is used to prevent EMI and guaranteed life time. (see Figure 11)		1		Ω

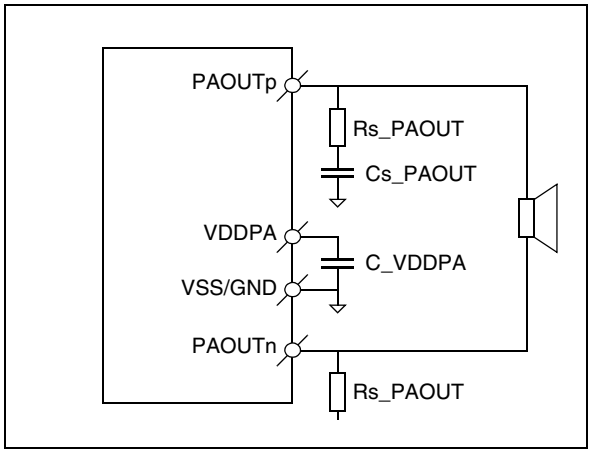


Figure 11 Class-D external components

Efficiency 75% at 300 mW@2 V, 500 mW@2.5 V into a 4 Ω transducer.

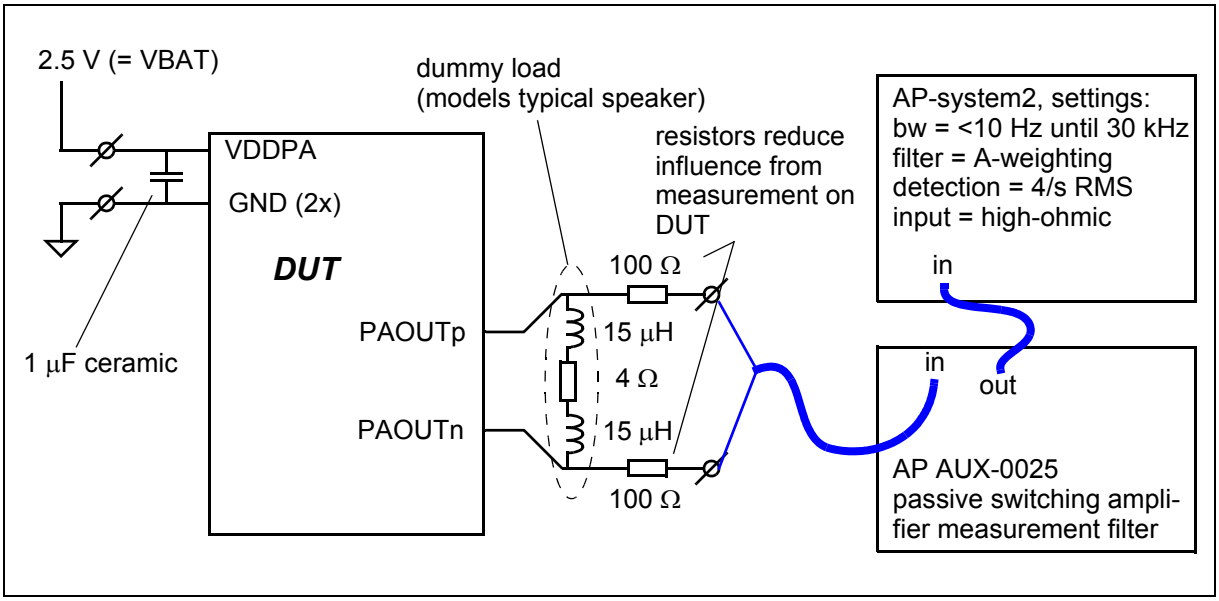


Figure 12 CLASS-D amplifier measurement setup

3.8 BATTERY MANAGEMENT

Table 19: CHARGE_CTRL pin

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Voh_charge_ctrl	Drive capability of pin CHARGE_CTRL	sourcing 500 µA	**1.6**			**V**
Vol_charge_ctrl		sinking 100 µA			**0.2**	**V**

Table 20: State of charge circuit (SoC) (Operating condition)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Vsocp_socn	Input voltage between SOCp and SOCn	With the prescribed 0.1 Ω sense resistor this results in the usable current range	**-100**		**+100**	**mV**

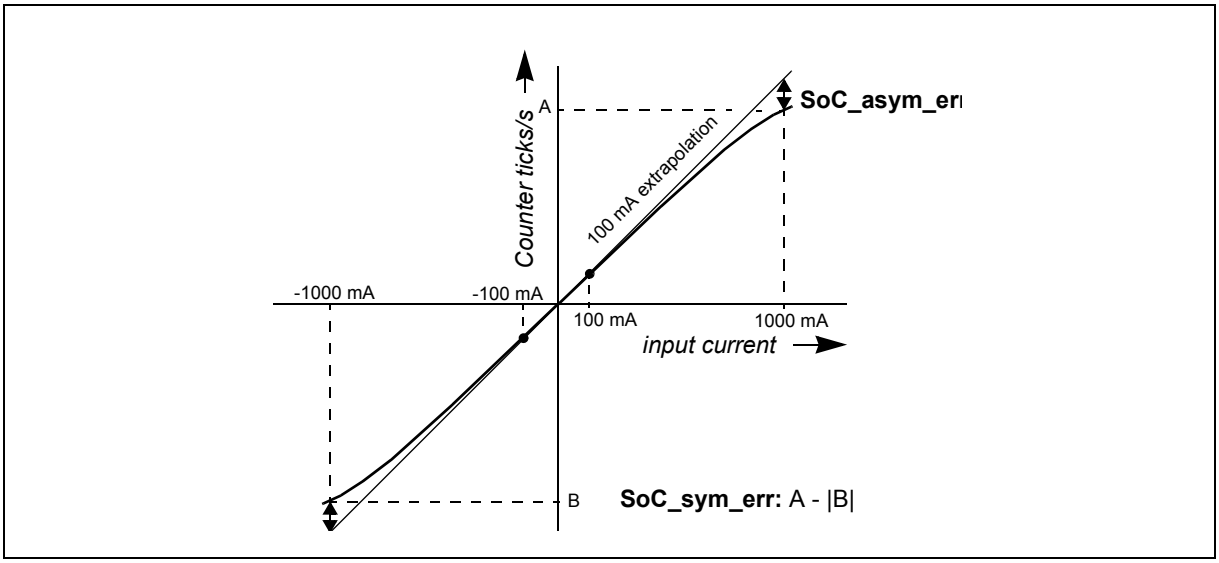


Figure 13 State of charge (SOC) counter accuracy

3.9 BASEBAND PART

Table 21: Baseband specifications

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
Fbit_uart	Serial interface bit rate	UART; Interface for external microprocessor or PC			**115.2**	**kbit/s**
Fbit_flash	Flash download bit rate	Via UART			**115.2**	**kbit/s**
Ibat_stdby_fp	Standby supply current	FP application (3.3 V)		**55**	**60**	**mA**
Ibat_act_fp	Active supply current	FP application (3.3 V)		**65**	**70**	**mA**
Ibat_stdby_pp	Standby supply current	PP application (3.3 V)		**4.5**	**6**	**mA**
Ibat_act_pp	Active supply current	PP application (3.3 V)		**30**	**40**	**mA**

3.10 RADIO (RF) PART

Standards compliancy: ETS 301 406 (former TBR6).

Table 22: Radio specifications

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
P_Rx	Receiver sensitivity	BER = 0.001; TA = 25 °C	**-93**	**-92**	**-89**	**dBm**
P_Rx_T	Receiver sensitivity, full temperature range	BER = 0.001; -40 °C ≤ TA ≤ +85 °C	**-94**		**-87**	**dBm**
IPL	Intermodulation performance level (EN 301 406 section 4.5.7.6)	TA = 25 °C; Pw = -80 dBm; Δf = 2 channels	**-35**			**dBm**
NTP	Normal transmitted power	DECT: 250 mW		**24**	**26**	**dBm**
		J-DECT: 10 mW average per frame for each slot		**23**	**24.5**	**dBm**
		DECT6.0: 100 mW (max peak)			**20.0**	**dBm**
dPrfpa_T	RFPA power variation, full temperature range	-40 °C ≤ TA ≤ +85 °C		**2.5**	**4**	**dB**
Fbit	Bit rate	GFSK modulation		**1.152**		**Mbit/s**
BW_Tx	Transmitter bandwidth	DECT GFSK; NTP = 20 dB			**1.728**	**MHz**

Table 23: RFPA preferred settings for various power modes (PP application)

Address (VES)	Register / Parameter	HPM/U (USA)	HPM (Europe)	HPM/J (Japan)
0x3D	RF_BBADC_CTRL_REG	0x0380	0x03A0	0x0398
0x39	RF_PA_CTRL1_REG	0x09A0	0x0CF0	0x2CE0
0x3B	RF_TEST_MODE2_REG	0x0056	0x0062	0x0068
0x05	RF_PLL_CTRL2_REG[MODINDEX]	0x25	0x25	0x23
0x23	Upper RSSI threshold	0x2C	N/A	0x28
0x24	Lower RSSI threshold	0x22	N/A	0x1E

3.11 RF POWER SUPPLY

Table 24: Requirements for linear supply regulator

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
VBAT IN	Voltage at VBAT SW	Unloaded V_B Loaded V_B-V_1-V_2-V_3	**2.1**	**3**	**3.45**	**V**
V_1	Settling time	I = 50 mA			**20**	**mV**
V_2	Receive period	I = 130 mA			**100**	**mV**
V_2	Transmit period	I = 550 mA			**200**	**mV**
V_3	Drop during transmit				**25**	**mV**

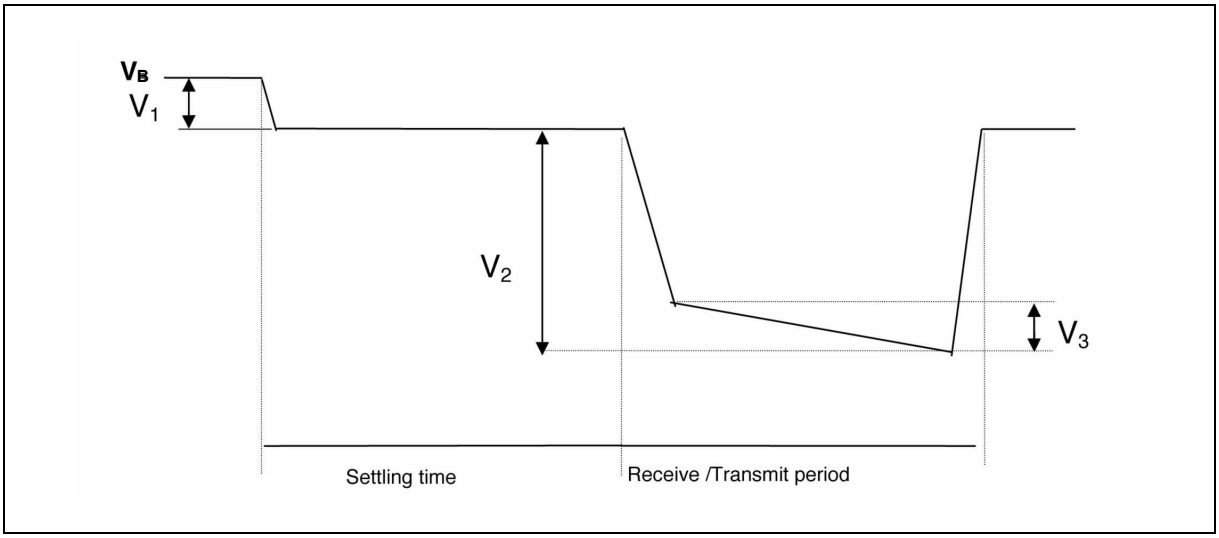


Figure 14 RF power supply

3.12 RF CHANNEL FREQUENCIES

Table 25: RF frequencies and channel numbers

Frequency (MHz)	DECT CH	J-DECT CH	DECT6.0 CH
1881.792	9		
1883.520	8		
1885.248	7		
1886.976	6		
1888.704	5		
1890.432	4		
1892.160	3		
1893.888	2		
1895.616	1	1	
1897.344	0	0	
1899.072		10	
1900.800		11	
1902.528		12	
1921.536			4
1923.264			3
1924.992			2
1926.720			1
1928.448			0

RF setting values must be followed according to AN-D-204 when DECT country mode was changed.

4.0 Design guidelines

4.1 PCB DESIGN GUIDELINES

- Because of the presence of the digital radio frequency burst with 100 Hz time division periods (TDD noise), supply ripple and RF radiation, special attention is needed for the power supply and ground PCB layout.
- Power supply considerations
  Both high and low frequency bypassing of the supply line connections should be provided and placed as close as possible to the SC14SPNODE. In order to get the best overall performance for both FP and PP applications, a number of considerations for the PCB has to be taken into account.
  - Make angle breaks on long supply lines to avoid resonances at DECT frequencies. Maximum 80 mm before an angle break is recommended.
  - Supply lines should be placed as far as possible away from sensitive audio circuits. If it is necessary to cross supply lines and audio lines, it should be done with right angles between supply and audio lines/circuits (microphone, ear-speaker, speakerphone, etc.)
  - Ground plane considerations
    In order to achieve the best audio performance and to avoid the influence of power supply noise, RF radiation, TDD noise and other noise sources, it is important that the audio circuits on both FP and PP applications boards are connected to the VREFM pin on the SC14SPNODE with separate nets in the layout.
    It is advised to provide the following audio circuits with separate ground nets connected to the VREFM pin:
    - Microphone(s)
    - Headset microphone and speaker
    - Speakerphone (signal grounds)

Depending on the layout it may also be necessary to bypass a number of the audio signals listed above to avoid humming, noise from RF radiation and TDD noise. It is also important to choose a microphone of appropriate quality with a high RF immunity (with built-in capacitor).

- ESD performance
  Besides TDD noise, the ESD performance is important for the end-application. In order to achieve a high ESD performance supply lines should be placed with a large distance from charging terminals, display, headset connector and other electrical terminals with direct contact to the ESD source.
  On a two-layer PCB application it is important to keep a simulated one layer ground. With a stable ground ESD and TDD noise performance will always improve.
- Clearance around test patterns
  Pin number 81 to 88 are used for production test purposes. In order to avoid any interference or disturbance the area around these signal pins must be kept clear of any signal and/or GND. The recommended clearance is at least 1 mm as shown in Figure 15.

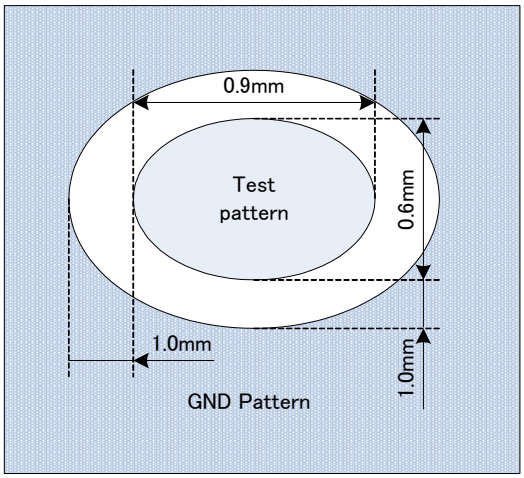


Figure 15 Clearance around test patterns

4.2 MODULE PLACEMENT ON THE MAIN BOARD

In order to ensure FCC compliance, proper coverage and to avoid detuning of the antennas, it is required to place the module on the main board free from other surrounding materials.

Keep a distance of at least 10 mm from the antenna elements to conducting objects and at least 5 mm to non-conducting objects.

Keep in mind that electrical shielding objects, even partly surrounding the antennas, will normally cause a significant degradation of the coverage.

Place the module at the edge of the main-board as shown in Figure 16.

If the module has to be placed away from the edge of the main-board, then avoid conducting areas in front of the antennas and make a cut-out in the main board underneath the antennas as shown in the figure.

See Figure 18 and Figure 21 for the detailed package outline.

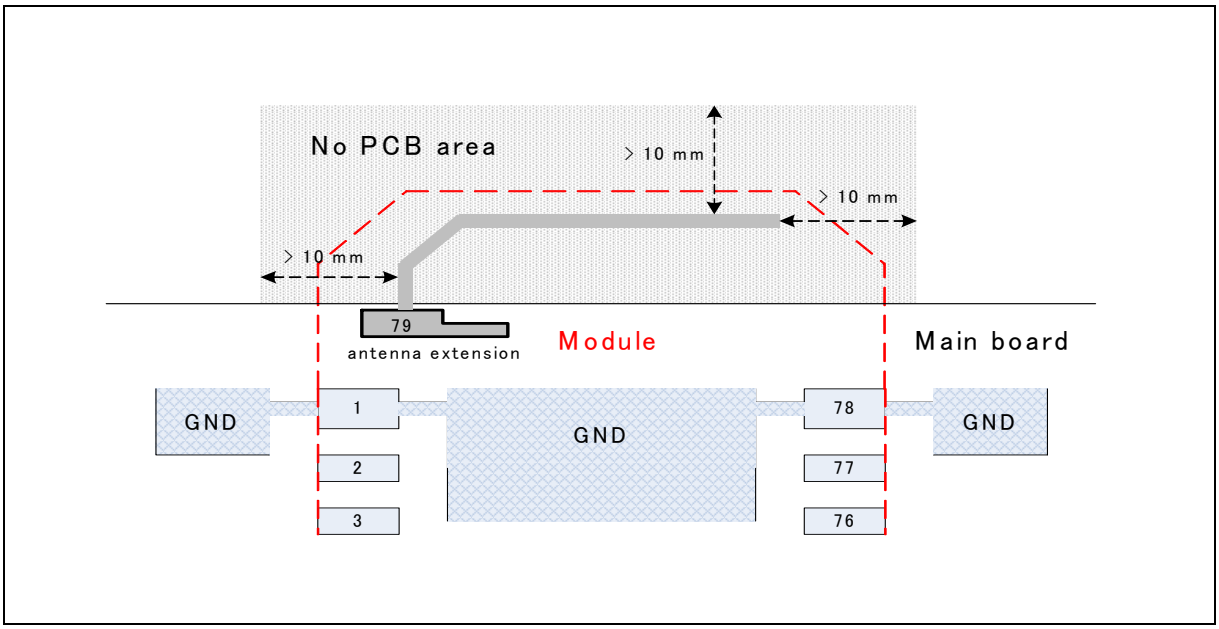


Figure 16 Module placement on the main board (top view)

4.3 PATTERN FOR PIN 79 ON THE MAIN BOARD

The copper pattern for pin 79 on the main board is very important because it is part of the internal antenna of the module. It is used to extend the internal antenna for optimum RF performance.

The PCB pattern shown in Figure 19 under “pads C” for pin 79 on the main board was used during module certification.

4.4 PRECAUTIONS REGARDING UNINTENDED COUPLING

The SC14SPNODE includes an internal antenna, so by integration on the main board precautions shall be taken in order to avoid any kind of coupling from the main board to the RF part of the module.

If there is any doubt about this, a brief radio test should be performed.

5.0 Notices to OEM

The end product has to be certified again if it has been programmed with other software than Dialog standard software stack for portable part and/or uses one or two external antenna(s).

5.1 FCC REQUIREMENTS REGARDING THE END PRODUCT AND THE END USER

The end product that the module is integrated into must be marked as follows:

"Contains Transmitter Module FCC ID: Y82-SC14S / IC: 9576A-SC14S"

The literature provided to the end user must include the following wording:

FCC compliance statement

This device complies with Part 15 of the FCC Rules.] for **only portable part**.

Operation is subject to the following two conditions:
(1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation of the device.

Module transmetteur ID IC: 9576A-SC14S.

Son fonctionnement est soumis aux deux conditions suivantes: (1) cet appareil ne doit pas causer d'interférences nuisibles et (2) appareil doit accepter toute interférence reçue, y compris les interférences qui peuvent perturber le fonctionnement.

Changes or modifications to the equipment not expressly approved by the Party responsible for compliance could void the user's authority to operate the equipment.

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generate, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation.

If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Privacy of communications may not be ensured when using this phone.

5.2 INDUSRY CANADA REQUIREMENTS REGARDING THE END PRODUCT AND THE END USER

The host device shall be properly labelled to identify the modules within the host device. The Industry Canada certification label of a module shall be clearly visible at all times when installed in the host device, otherwise the host device must be labelled to display the Industry Canada certification number of the module, preceded by the words "Contains transmitter module", or the word "Contains", or similar wording expressing the same meaning, as follows:

Contains transmitter module IC: 9576A-SC14S

L'appareil hôte doit être étiqueté comme il faut pour permettre l'identification des modules qui s'y trouvent. L'étiquette de certification d'Industrie Canada d'un module donné doit être posée sur l'appareil hôte à un endroit bien en vue en tout temps. En l'absence d'étiquette, l'appareil hôte doit porter une etiquette donnant le numéro de certification du module d'Industrie Canada, précédé des mots " Contient un module d'émission ", du mot " Contient " ou d'une formulation similaire exprimant le même sens, comme suit :

Contient le module d'émission IC: 9576A-SC14S

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

CAN ICES-3 (B)/NMB-3(B)

5.3 PRECAUTIONS REGARDING UNINTENDED COUPLING

Integration on the main board precautions shall be taken in order to avoid any kind of coupling from the main board to the RF part of the module. If there is any doubt about this, a radio short test should be performed.

5.4 END APPLICATION APPROVAL

The module is intended to be used in an end application. Type approval concerning the end product, except for the module, should off cause be done. Please contact a test-house in order to clarify what is needed.

5.5 SAFETY REQUIREMENTS

This section provides of an overview of the safety requirements you must adhere to when working with the SC14SPNODE.

- The specific external power supply for the SC14SPNODE has to fulfil the requirements according to clause 2.5 (Limited power source) of this standard EN 60950-1:2006.
- Interconnection circuits shall be selected to provide continued conformance to the requirements of clause 2.2 for SELV (Safety Extra Low Voltage) circuits according to EN 60950-1:2006 after making connections.
- Interface type not subjected to over voltages (i.e. does not leave the building).
- Requirements additional to those specified in this standard may be necessary for:
  - Equipment intended for operation in special environments (for example, extremes of temperature, excessive dust, moisture or vibration, flammable gases and corrosive or explosive atmospheres).
  - Equipment intended to be used in vehicles, on Board ships or aircraft, in tropical countries or at altitudes greater than 2000 m.
  - Equipment intended for use where ingress of water is possible.
- Installation by qualified personnel only!
- The product is a component intended for installation and use in complete equipment. The final acceptance of the component is dependent upon its installation and use in complete equipment.

6.0 Package information

6.1 SOLDERING PROFILE

The SC14SPNODE should be soldered using a standard reflow soldering profile and lead free solder paste as shown below. Adjustments to the profile may be necessary depending on process requirements.

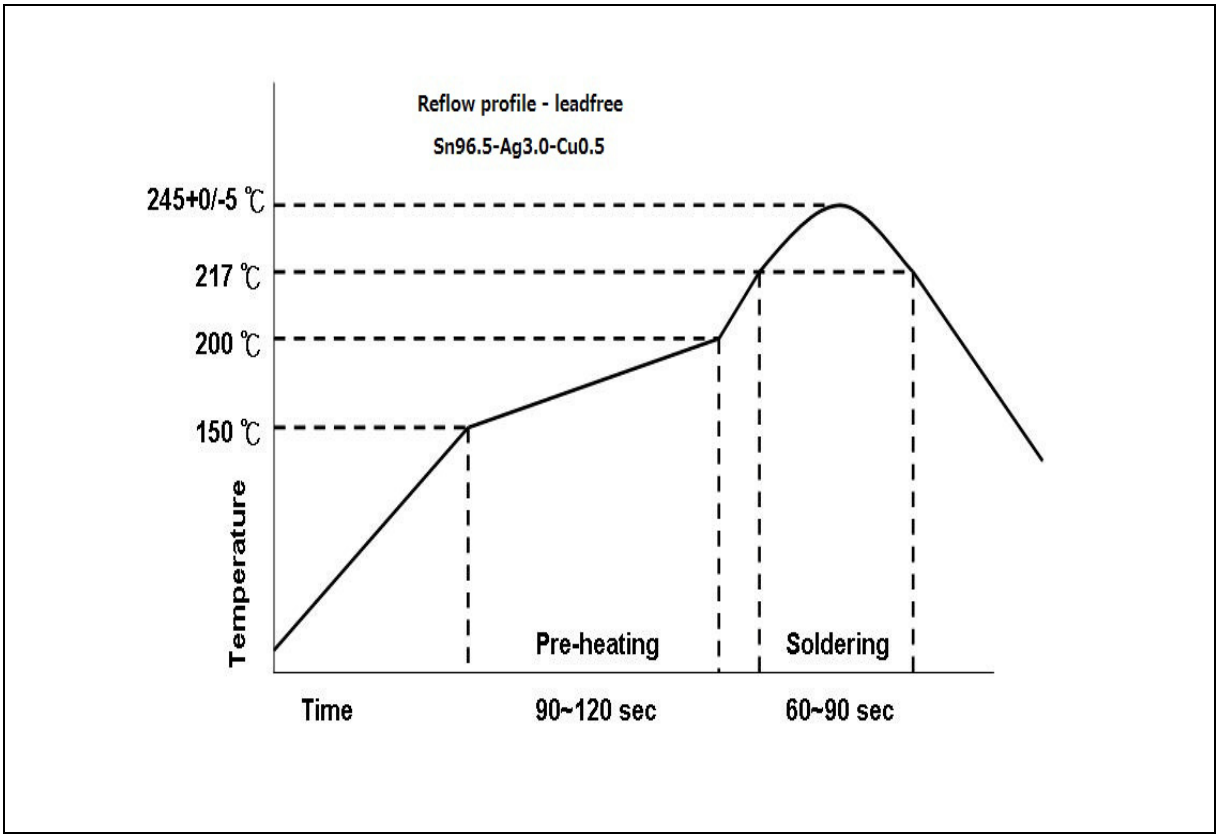


Figure 17 Reflow profile

6.2 MOISTURE SENSITIVITY LEVEL (MSL)

The MSL is an indicator for the maximum allowable time period (floor life time) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a maximum temperature of 30°C and a maximum relative humidity of 60% RH. before the solder reflow process.

The SC14SPNODE is qualified to MSL 3.

MSL Level	Floor Life Time
MSL 4	72 hours
MSL 3	168 hours
MSL 2A	4 weeks
MSL 2	1 year
MSL 1	Unlimited at 30°C/85%RH

6.3 COPPER PAD, SOLDER OPENING AND STENCIL

For the stencil a thickness of 0.122 mm is recommended. Recommended copper pad, solder mask opening and stencil are shown below.

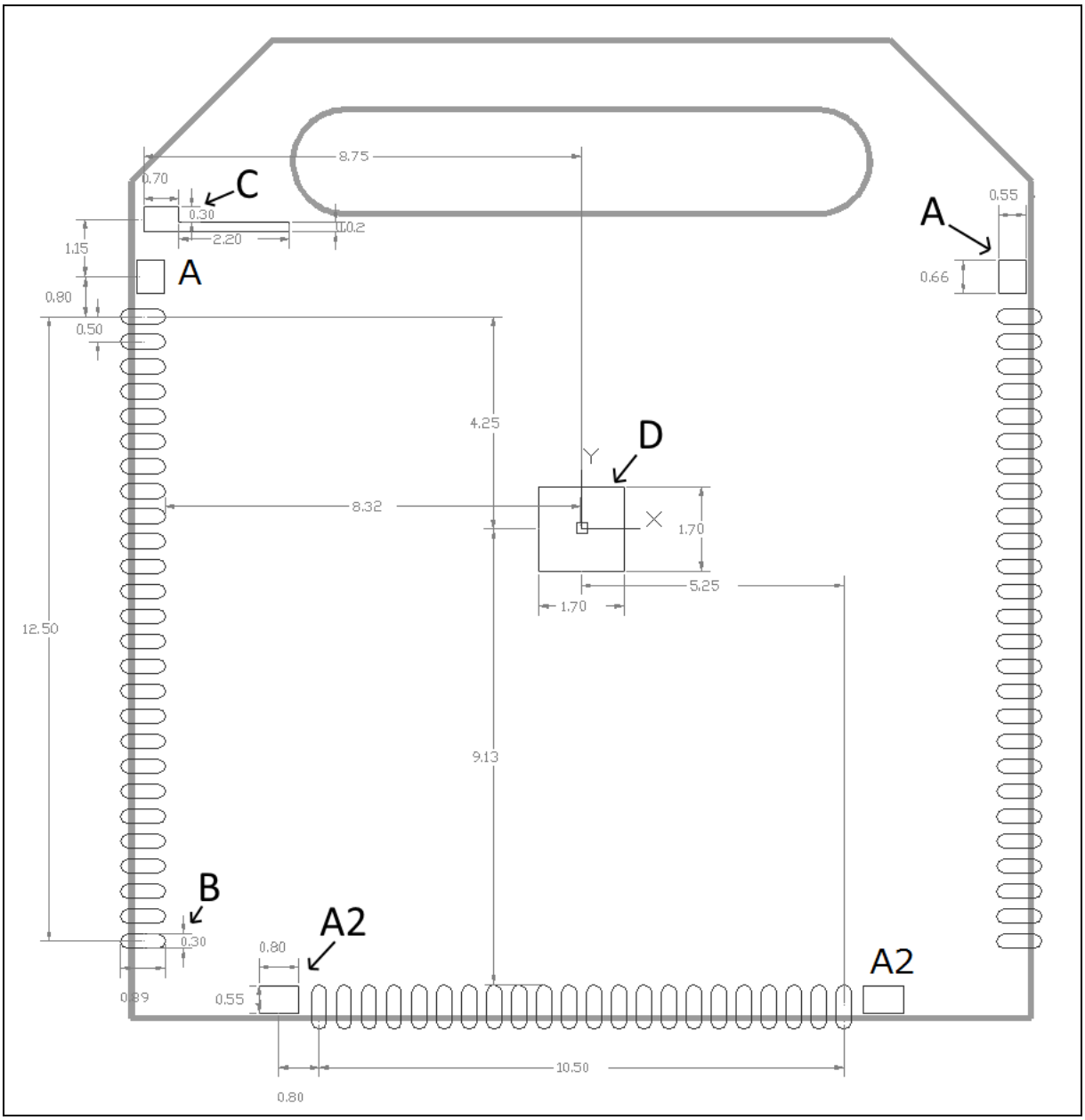


Figure 18 Pad dimensions

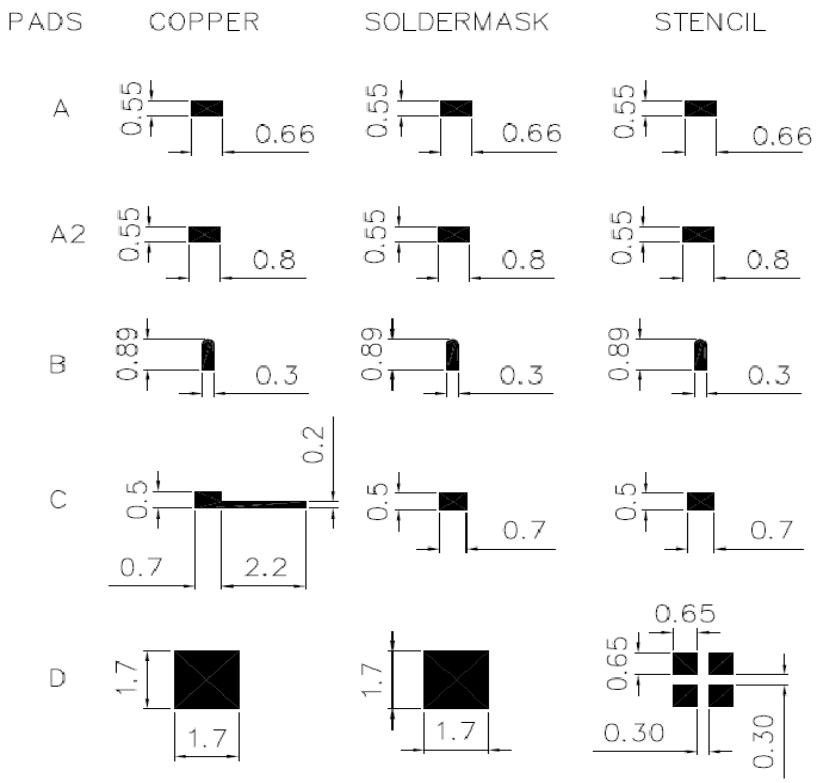


Figure 19 Copper pad, Solder mask opening and Stencil

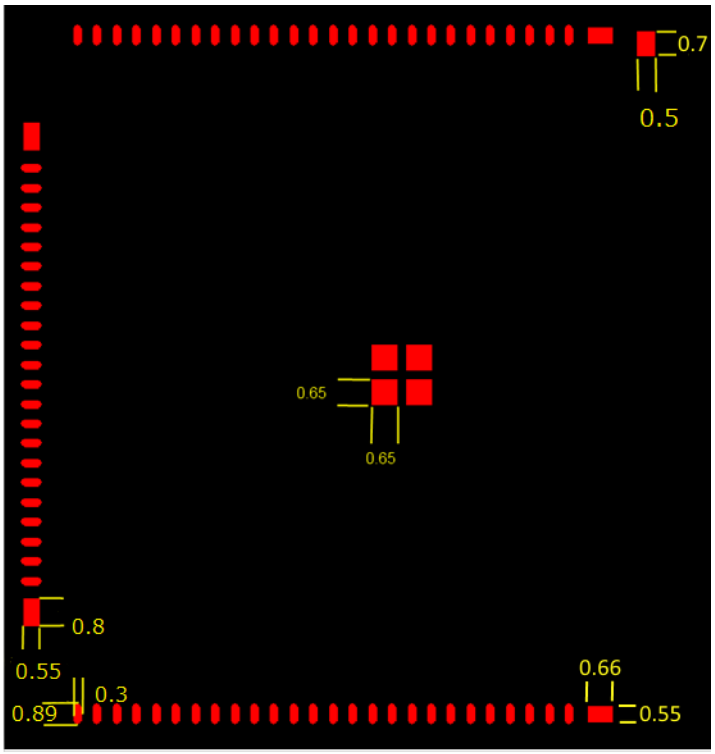
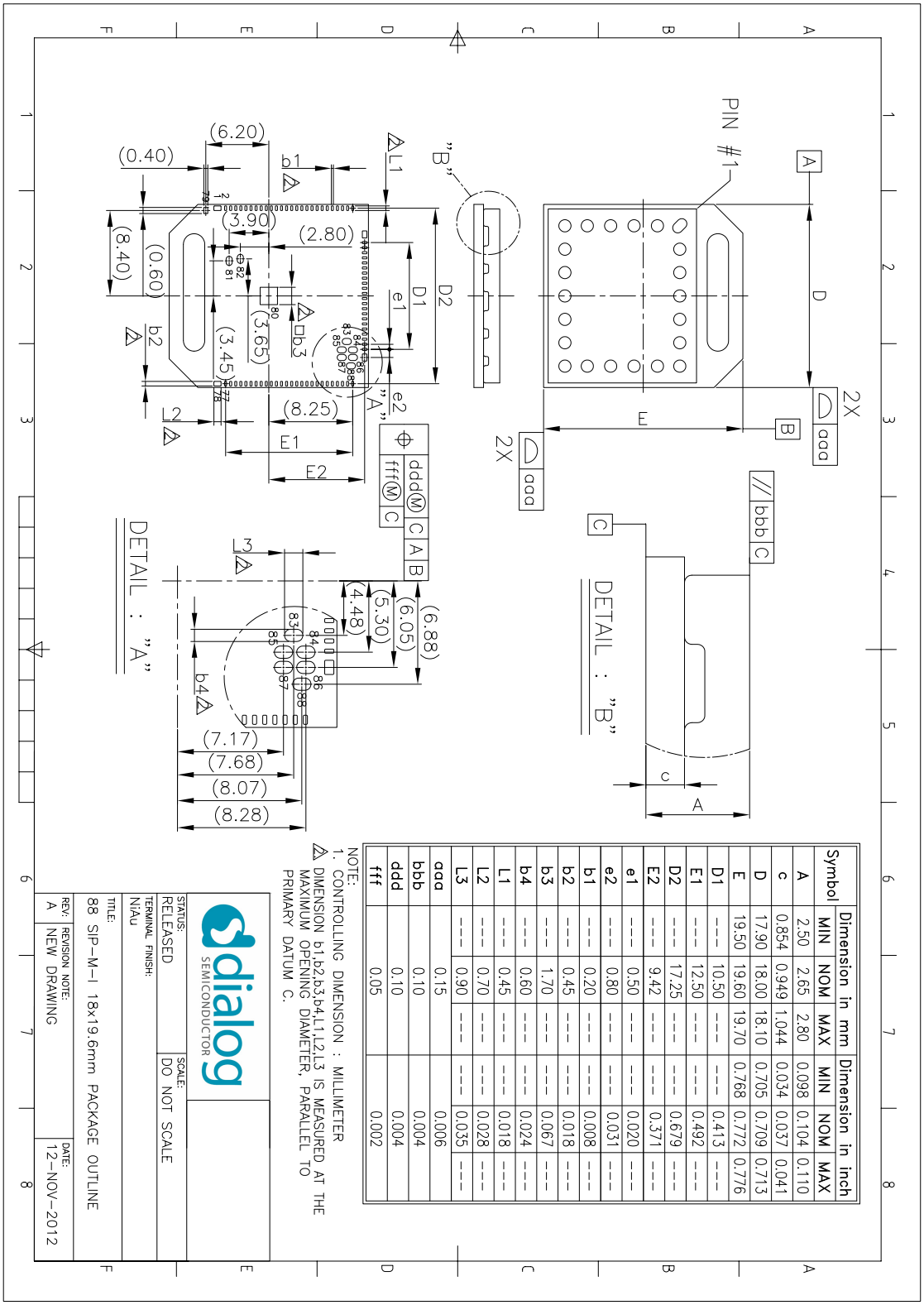


Figure 20 Solder stencil

6.4 MECHANICAL DIMENSIONS



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.50	2.65	2.80	0.098	0.104	0.110
c	0.854	0.949	1.044	0.034	0.037	0.041
D	17.90	18.00	18.10	0.705	0.709	0.713
E	19.50	19.60	19.70	0.768	0.772	0.776
D1	---	10.50	---	---	0.413	---
E1	---	12.50	---	---	0.492	---
D2	---	17.25	---	---	0.679	---
E2	---	9.42	---	---	0.371	---
e1	---	0.50	---	---	0.020	---
e2	---	0.80	---	---	0.031	---
b1	---	0.20	---	---	0.008	---
b2	---	0.45	---	---	0.018	---
b3	---	1.70	---	---	0.067	---
b4	---	0.60	---	---	0.024	---
L1	---	0.45	---	---	0.018	---
L2	---	0.70	---	---	0.028	---
L3	---	0.90	---	---	0.035	---
aaa		0.15			0.006	
bbb		0.10			0.004	
ddd		0.10			0.004	
fff		0.05			0.002	

Figure 21 Package outline drawing

7.0 Revision history

Jul1, 2014 v1.6:

- Changed maximum RF output power for DECT 6.0

Apr 16, 2014 v1.5:

- Added an explanation for RF1 on 2.6

Feb 11, 2014 v1.4:

- Correct 6.3Copper pad, solder openinG and STENCIL28

Feb 4, 2014 v1.3:

- Modified 6.3Copper pad, solder openinG and STENCIL28

Nov 8, 2013 v1.2:

- Added section “5.2 INDUSTRY CANADA REQUIREMENTS REGARDING THE END PRODUCT AND THE END USER”

Sept 12, 2013 v1.1:

- Ordering code for tray version corrected.
- Ordering code for tape-on-reel version removed.

July 10, 2013 v1.0: Initial version

Product Status Definitions

Datasheet Status	Product Status	Definition
Advance Information	Formative or in Design	This data sheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This data sheet contains preliminary data. Supplementary data will be published at a later date. Dialog Semiconductor reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
No Identification Noted	Full production	This data sheet contains final specifications. Dialog Semiconductor reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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