

Title: VP2 Refresh Flatpanel(FP) system pictures

Project:	VP2 Refresh Flatpanel		
Maturity:	<u>draft</u> / ready/ reviewed	Version:	A01

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Purpose:
This document describes the VP2 Refresh FP system pictures

History of Content Changes				
Version	Status	Date dd-Mmm-YYYY	Document Owner, Department	Changes (e.g. CR-number)
A01	released	08-Jul-2016	F. Born I IC RD SP EE D2	First version

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2 Target pictures

The following pictures show the VP2 Refresh FP radio system disassembled down to the PCB's.



Figure3: VP2 Refresh FP top view with label example



Figure4: VP2 Refresh FP backside view with label example

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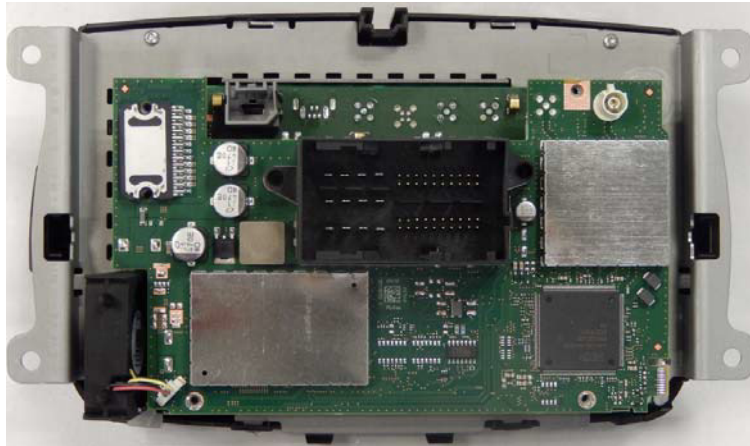


Figure5: VP2 Refresh FP backside view with open housing



Figure6: VP2 Refresh FP backside view without fan and connector housing



Figure7: VP2 Refresh FP backside view without power radio board

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Figure8: VP2 Refresh FP backside view with Mainboard

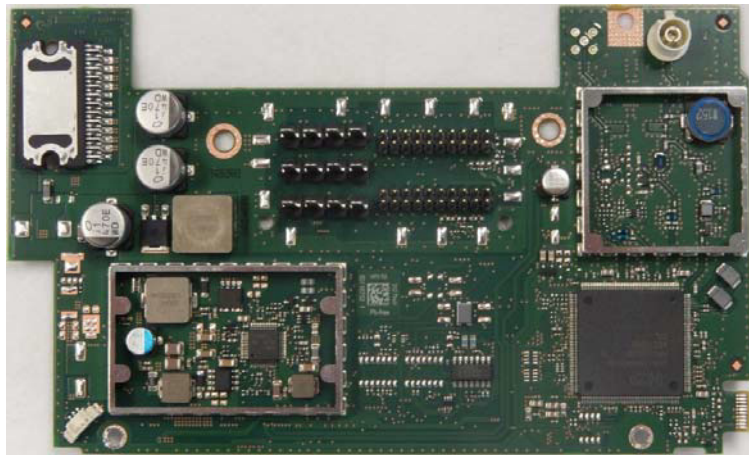


Figure9: VP2 Refresh FP PowerRadio board PCB Top

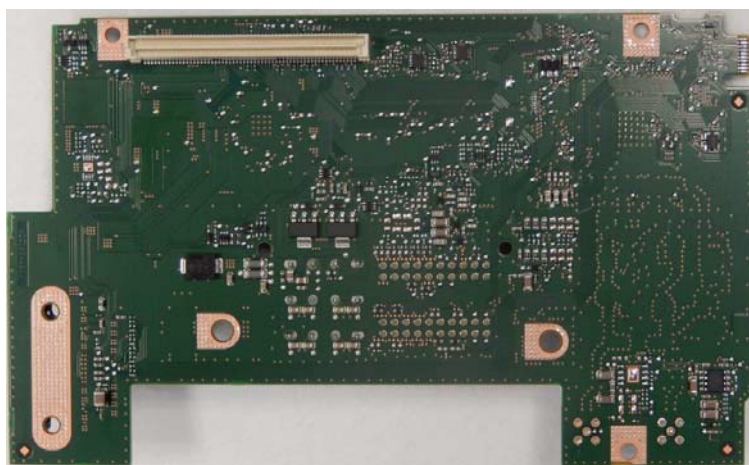
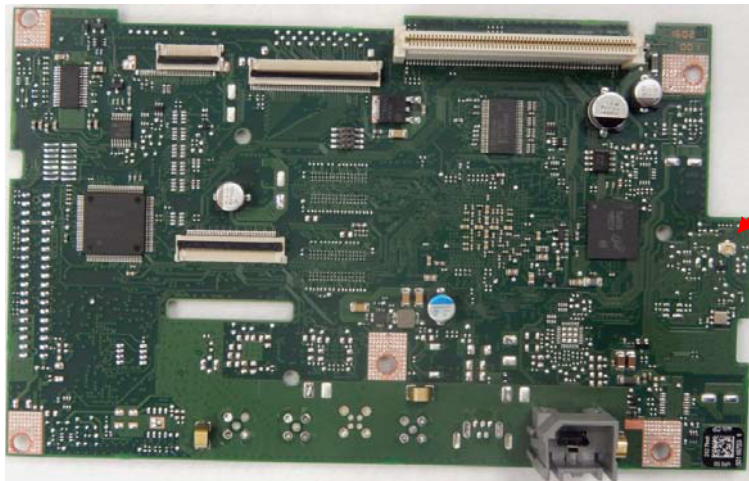


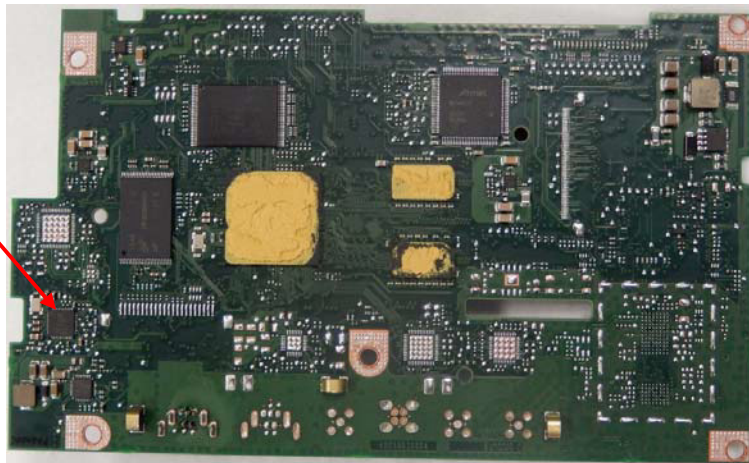
Figure10: VP2 Refresh FP PowerRadio board PCB Bottom

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BT RF connector

Figure11: VP2 Refresh FP Mainboard PCB Top side



BT chip

Figure12: VP2 Refresh FP Mainboard PCB Bottom side with BT chip

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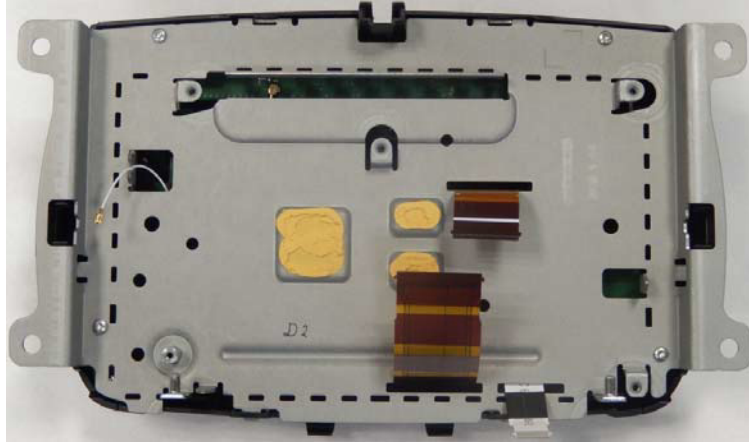


Figure13: VP2 Refresh FP Front backside view



Figure14: VP2 Refresh FP Front backside view without metal plate

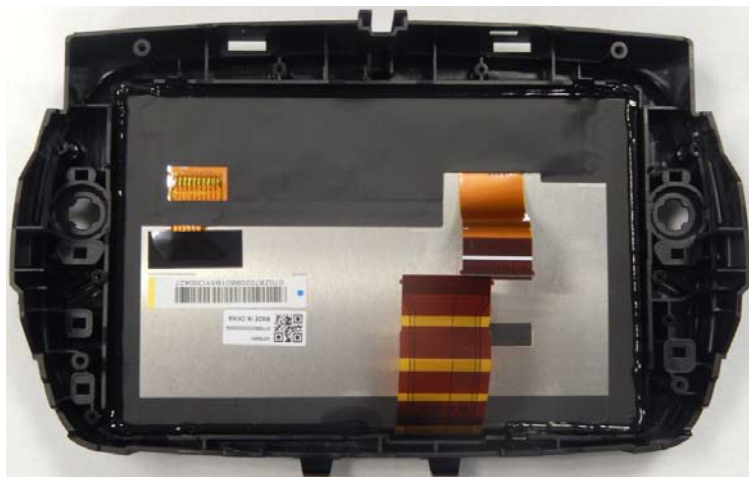


Figure15: VP2 Refresh FP Front display backside view

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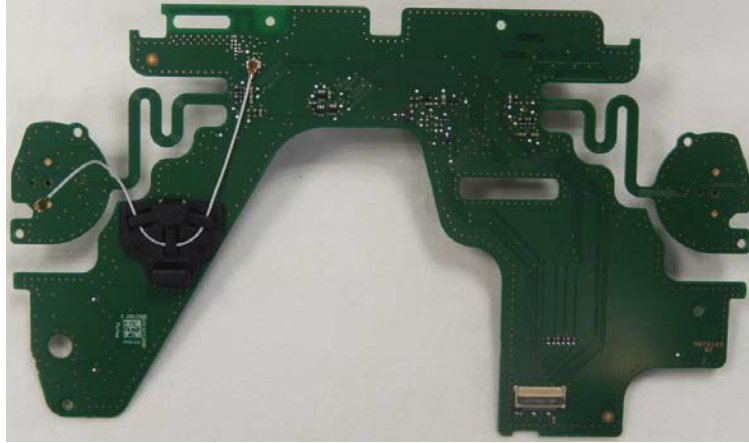


Figure16: VP2 Refresh FP Front PCB Bottom side

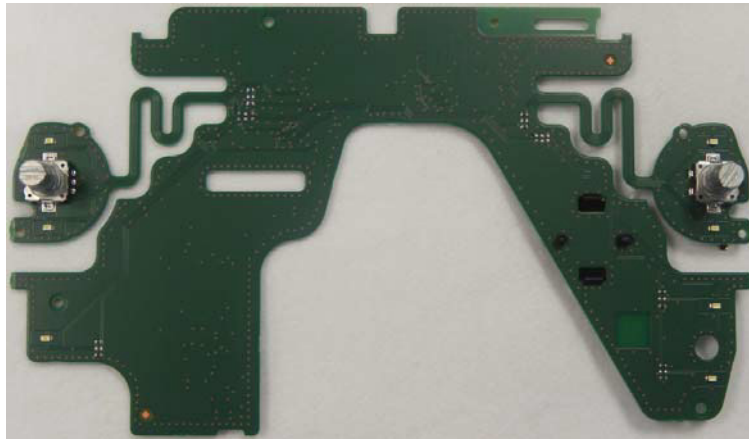


Figure17: VP2 Refresh FP Front PCB Top side

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