Theory of Operation

The **SCRN800** radio is a dual diversity receiver and single carrier WCDMA transmitter implemented with two commercially available transceiver ICs. The transceivers are located on a single small PCB with the digital baseband circuit on a separate access point PCB assembly. Page 3 of the radio schematic contains details of the transmitter and receiver frequencies. The A channel has an additional receive front-end that the B channel does not that is used to monitor the cellular down-link band.

The transceiver:

The receiver is based on direct conversion architecture. This architecture includes highly integrated wideband CDMA (WCDMA) receivers, reducing the bill of materials by fully integrating all interstage filtering. Inside the IC the front end includes three high performance, single-ended low noise amplifiers (LNAs), allowing the device to support tri-band receive (downlink monitoring).

The integrated receive baseband filters offer selectable bandwidth, enabling the device to receive both WCDMA and GSM-EDGE radio signals. The selectable bandwidth filter, coupled with the multiband LNA input structure, allows GSM-EDGE signals to be monitored as part of a UMTS small base station.

The transmitter uses a direct conversion modulator that achieves high modulation accuracy with low noise, eliminating the need for external transmit SAW filters. **The power limiting and control function is done by creating a calibration table in the manufacturing process and using the programmable output power features of the transceiver.**

The fully integrated phase lock loops (PLLs) provide high performance and low power fractional-N frequency synthesis for both receive and transmitter sections. Precautions were taken in the IC to provide the isolation demanded by frequency division duplex (FDD) systems. All VCO and loop filter components are fully integrated.

The transceiver contains a low noise variable gain direct conversion transmitter architecture that removes the need for external transmit SAW filters however the duplexer utilized provides a bandpass transfer function response. The direct conversion architecture significantly reduces the risk of transmit harmonics across all bands due to the simplified nature of the frequency plan. Each of the 2 receivers digital interface is connected to its own A/D.

I/Q Modulator

The I/Q modulator converts the transmit baseband input signals to RF. Calibration techniques are used to maintain accurate IQ balance and phase across frequency and environmental conditions, thus ensuring that 3GPP carrier leakage and EVM and ACLR requirements are met under all conditions, thus providing the **modulation limiting function**. The on-chip calibrations are carried out during the transmit PLL lock time and are self-contained inside the transceiver IC.

PLL (frequency stabilization circuitry)

All necessary components are fully integrated for both transmit and receive synthesizers, including loop filters, VCOs, and tank components. The VCOs run at 2× the high band frequency and 4× the low band frequency. The dividers are external to the synthesizer loop. This minimizes VCO leakage power at the desired frequency and tuning range requirements of the VCO. The VCOs use a multiband structure to cover the wide frequency range required.

The IC design incorporates both frequency and amplitude calibration to ensure that the oscillator is always operating with its optimum performance. The charge pump and loop filter are internally trimmed in the transceiver IC's manufacture to remove variations associated with manufacture and frequency.

The transceiver requires a 26 MHz reference frequency input. A voltage controlled temperature compensated crystal oscillator (VCTCXO) is used to provide the 100ppb reference. The 26 MHz reference is buffered inside the IC and distributed to the respective blocks, such as the synthesizer PFD inputs.

The transceiver provides two buffered outputs: a buffered version of the 26 MHz reference on Pin REFCLK and a 19.2 MHz WCDMA chip clock on Pin CHIPCLK. The 19.2 MHz chip clock is a multiple of the 3.84 MHz chip rate used in WCDMA. The chip clock is generated by an integrated PLL and contains no IC external settings.

Transmitter Output Circuit

The transceiver IC transmit output is followed by a driver and power amplifier, a directional coupler, an isolator, a duplexer, and an RF switch. The isolator is used to provide an optimum termination for the power amplifier. Each component was selected for linearity. The duplexer has a bandpass response in both paths.

PLL reference

FREQUENCY CHARACTERISTICS

Line	*Parameter*	*Test Condition*		*Max.*	*Units*
2.1	**frequency**	26.000		MHz	
2.2	**Initial frequency tolerance**	Frequency offset at 25°C, sixty minutes after reflow over a 10% range of supply voltage	±2		ppm
2.3	**Temperature rate of change**	Maximum rate of change of temperature condition for guaranteed stability specifications	1		°C/min
2.4	**In-service short term frequency stability (Note 1)**	Over any 24 hours 50°C ~ 70°C at fixed supply voltage and load 0°C ~ 70°C ±100ppB 0°C ~ 85°C ±250ppB	±80		ppb
2.6	**Frequency variation with supply voltage**	±2% variation in supply voltage at 25°C	±10		ppb
2.7	**Frequency variation with load**	±2% variation in magnitude from 10pF	±5		ppb

Duplexer

A duplexer is installed after the antenna switch and has 2 outputs. The outputs of the duplexer connect to the transmitter output and the primary receiver input LNA. Each path through the duplexer has a bandpass transfer function. The bandpass action attenuates undesired out of band signals providing **suppression of spurious radiation.**

Isolator

The transmit path contains an isolator to improve the load seen by the final amplifier stage improving the amplifiers linearity. The isolator and final amplifier are band specific.

Antenna

Frequency Range:	824-894 MHz, 880-960 MHz, 1575 MHz, 1710-1880 MHz, 1850-1995 MHz, 1920-2170 MHz, 2400-2500 MHz
Gain	1 - 3 dBi
VSWR	<2.5:1
Polarization	Linear
Azimuth (3dB beamwidth)	Omni-directional
Impedance	50 Ω
Temperature Range	-5° C to +50° C
Power	10 W

Grounds

On the radio PCB ground ids principally provided by the 2nd layer of the PCB and by shields on the top layer of the PCB. Additional grounding and shielding are provided by RF cable shields, and the circuit enclosure -- a sturdy aluminum assembly.

Digital Baseband Board

The digital board of an SCRN (Smart Cloud Radio Node) consists of a Network processor and a Baseband DSP sub-system and additional circuits for programmable logic, clock and power distribution.

The Baseband DSP sub-system performs the digital baseband modulation and demodulation, filtering, signal processing, diversity (MRC) and other functions of a UMTS radio. It communicates to the Network Processor via an MII interface and to the Radio via a Full-Duplex parallel interface that carries I, Q data to and from the UMTS Radio.

The Network processor sub-system provides a secure 10/100 Ethernet interface back to the SpiderCloud Controller (SCSN, Smart Cloud Services Node) and provides various control functions for the SCRN-800. The SCRN-800 is booted over this Network connection and the Network Processor is also responsible for maintaining network Synchronization over 1588 (Precision Time Protocol) to an oven controlled clock source that resides on the SCSN.

An additional RS232 console interface is provided for factory diagnostics and maintenance support.

The SCRN-800 is powered up over PoE+ (802.3at). The Power-Over-Ethernet circuit resides on the digital board and provides up to 25.5W of power to the SCRN-800. In addition there are a number of switching regulator circuits that provide power to the various rails on the digital board. A 100ppb 26MHZ VCTCXO circuit that is synchronized with the SCSN over 1588 also resides on the digital board. All additional clocks are derived from this clock source using PLL's except for an xtal used on a UART interface to the Baseband DSP sub-system.

Additional circuits on the digital board include Flash, DDR2, 10/100 PHY with 1588 support, RS232 transceivers, CPLD, FPGA's, buffers and discrete logic. In addition there is a USB-Parallel interface that is used during development.