1.1 Features

This section provides a simplified block diagram and highlights MC1322x features.

1.1.1 Block Diagram

Figure 1-2 shows a simplified block diagram of the MC1322x.

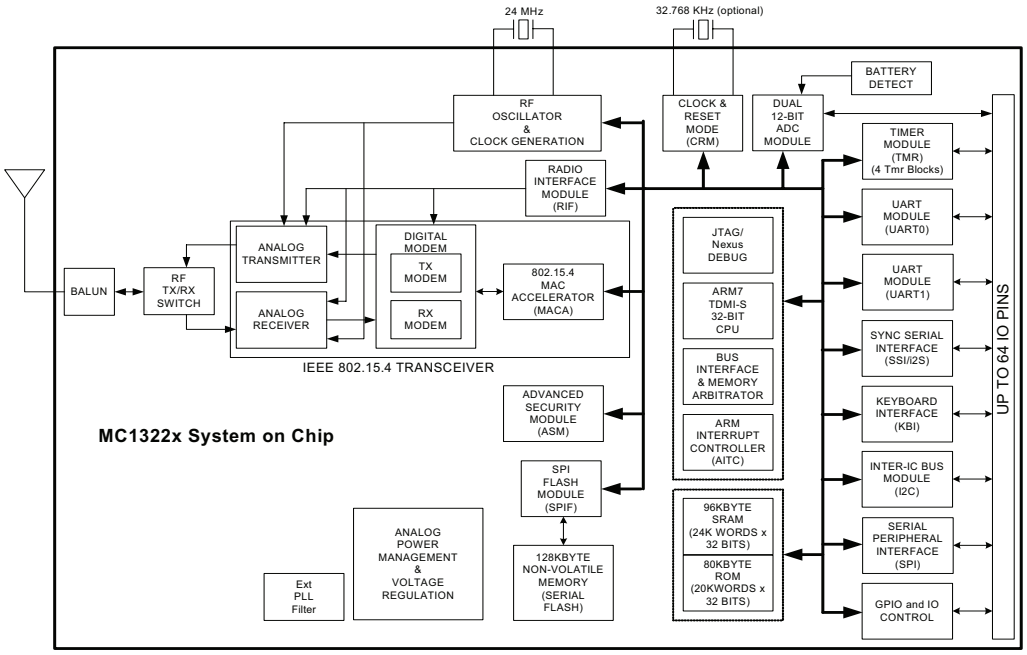

Figure 1-2. MC1322x Simplified Block Diagram

1.1.2 Features Summary

- IEEE 802.15.4 standard compliant on-chip transceiver/modem
  - 2.4GHz
  - 16 selectable channels
  - Programmable transmitter output power (-30 dBm to +4 dBm typical)
  - World-class receiver sensitivity
    - < -96 dBm typical receiver sensitivity using DCD mode (<1% PER, 20-byte packets)
    - < -100 dBm typical receiver sensitivity using NCD mode (<1% PER, 20-byte packets)
- Hardware acceleration for IEEE 802.15.4 applications
  - MAC accelerator (sequencer and DMA interface)
  - Advanced encryption/decryption hardware engine (AES 128-bit)
- Supports standard IEEE 802.15.4 signalling with 250 kbps data rate
- 32-bit ARM7TDMI-S CPU core with programmable performance up to 26 MHz (24 MHz typical)
- Extensive on-board memory resources