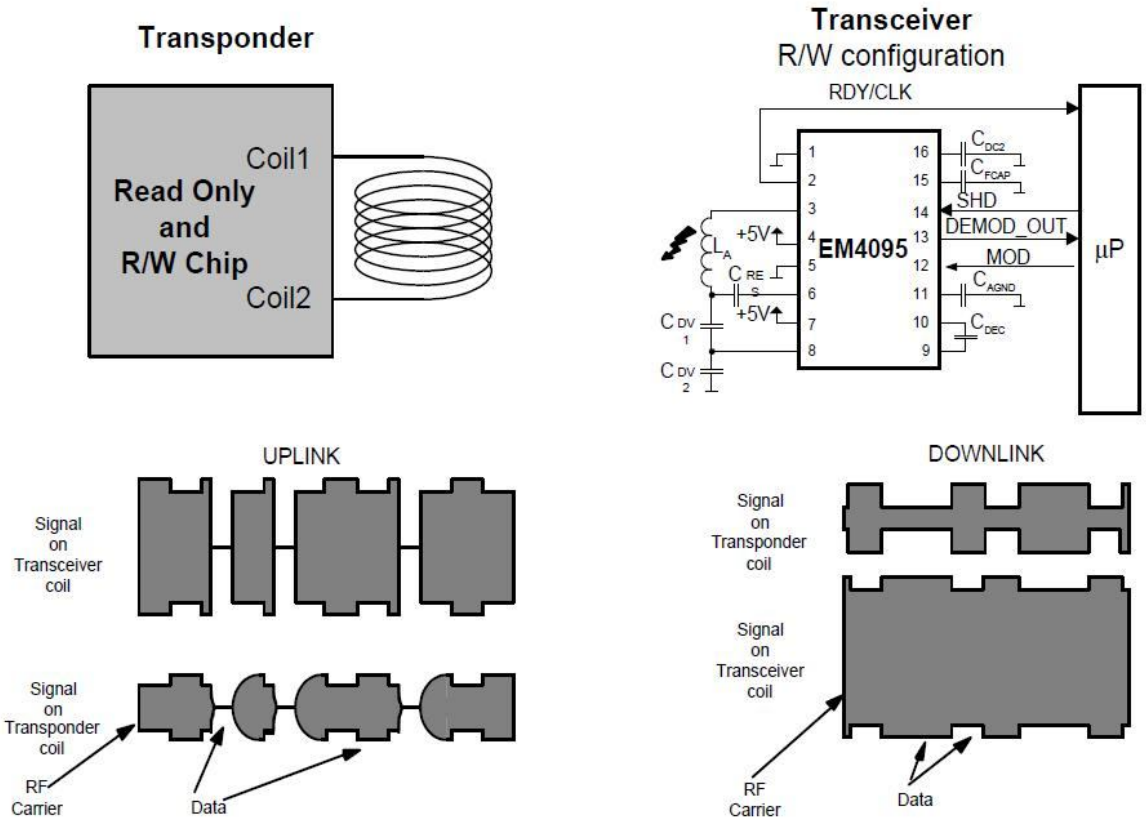
Applicant: UNION COMMUNITY Co.,Ltd.
Model Name: VS-R20D RF

1. Operation Description



1) General Description

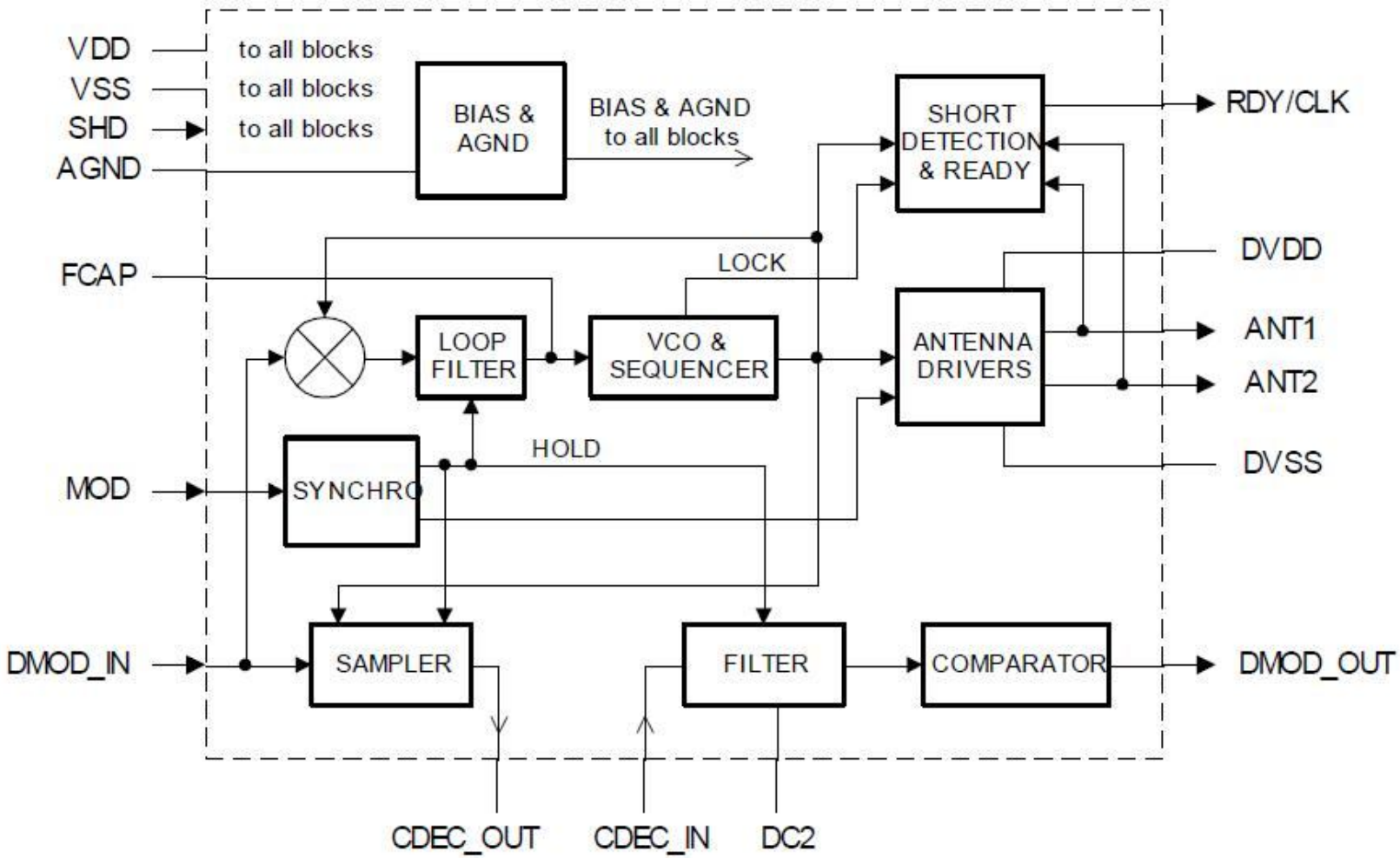
The EM4095 is intended to be used with an attached antenna circuit and a microcontroller. Few external components are needed to achieve DC and RF filtering, current sensing and power supply decoupling.

A stabilised power supply has to be provided. Please refer to EM4095 Application Notes for advice.

Device operation is controlled by logic inputs SHD and MOD. When SHD is high EM4095 is in sleep mode, current consumption is minimised. At power up the input SHD has to be high to enable correct initialisation. When SHD is low the circuit is enabled to emit RF field, it starts to demodulate any amplitude modulation (AM) signal seen on the antenna. This digital signal coming from the AM demodulation block is provided through DEMOD_OUT pin to the microcontroller for decoding and processing.

High level on MOD pin forces in tri-state the main antenna drivers synchronously with the RF carrier. While MOD is high the VCO and AM demodulation chain are kept in state before the MOD went high. This ensures fast recovery after MOD is released. The switching ON of VCO and AM demodulation is delayed by 41 RF clocks after falling edge on MOD. In this way the VCO and AM demodulation operating points are not perturbed by start-up of antenna resonant circuit.

2) Transmitter & Receiver Architecture



Transmission

Referring to the block diagram, transmission is achieved by a Phase Locked Loop (PLL) and the antenna drivers.

Drivers

The antenna drivers supply the reader basestation antenna with the appropriate energy. They deliver current at the resonant frequency which is typically 125 kHz. Current delivered by drivers depends on Q of external resonant circuit. It is strongly recommended that design of antenna circuit is done in a way that maximum peak current of 250 mA is never exceeded (see Typical Operating Configuration for antenna current calculation). Another limiting factor for antenna current is Thermal Convection of package. Maximum peak current should be designed in a way that internal junction temperature does not exceed maximum junction temperature at maximum application ambient temperature. 100% modulation (field stop) is done by switching OFF the drivers. The ANT drivers are protected against antenna DC short circuit to the power supplies. When a short circuit has been detected the RDY/CLK pin is pulled low while the main driver is forced in tri-state. The circuit can be restarted by activating the SHD pin.

Phase locked loop

The PLL is composed of the loop filter, the Voltage Controlled Oscillator (VCO), and the phase comparator blocks. By using an external capacitive divider, pin DEMOD_IN gets information about the actual high voltage signal on antenna. Phase of this signal is compared with the signal driving antenna drivers. Therefore the PLL is able to lock the carrier frequency to the resonant frequency of the antenna. Depending on the antenna type the resonant frequency of the system can be anywhere in the range from 100 kHz to 150 kHz. Wherever the resonant frequency is in this range it will be maintained by the Phase Lock Loop.

Reception

The demodulation input signal for the reception block is the voltage sensed on the antenna. DEMOD_IN pin is also used as input to Reception chain. The signal level on the DEMOD_IN input must be lower than VDD-0.5V and higher than VSS+0.5V. The input level is adjusted by the use of an external capacitive divider. Additional capacitance of

divider must be compensated by accordingly smaller resonant capacitor. The AM demodulation scheme is based on the "AM Synchronous Demodulation" technique.

The reception chain is composed of sample and hold, DC offset cancellation, bandpass filter and comparator. DC voltage of signal on DEMOD_IN is set to AGND by internal resistor. The AM signal is sampled, the sampling is synchronised by a clock from VCO. Any DC component is removed from this signal by the CDEC capacitor. Further filtering to remove the remaining carrier signal, high and low frequency noise is made by second order highpass filter and CDC2. The amplified and filtered receive signal is fed to asynchronous comparator. Comparator output is buffered on output pin DEMOD_OUT.