Spectrum 2.4Ghz, RX RF Daughter Board Module Operational Description

Version 1.0

Revision History

Date	Version	Description	Author
10/1/2010	1.0	Original.	Chris S. Russell

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1. Features

- Spectrum 2.4Ghz, RX RF Daughter Board Module is a 2.4GHz Direct Sequence Spread Spectrum (DSSS) radio which includes the Cypress radio integrated circuit Wireless USB™ CYRF6936/7936 and an integrated PA.
- Operation in intended in the unlicensed Worldwide Industrial, Scientific and Medical (ISM band (2.400GHz – 2.483GHz)
- Less than 100mA operating current (Transmit @ 22 dBm)
- Transmit power up to -29.27dBm
- Sleep current < 10uA
- Outdoor LOS range up to 1500ft.
- DSSS rates up to 250Kbps
- Serial Peripheral Interface (SPI)
- Operating voltage 3.3 volts
- Operating temperature 0^{o} to 70^{o} C

2. Functional Description

The Spectrum 2.4Ghz, RX RF Daughter Board Module is a complete radio module solution for integration into existing or new 2.4GHz products.

The Spectrum 2.4Ghz, RX RF Daughter Board Module is tested for functional operation and is certified:

FCC ID: XVE-SA09218.

The Spectrum 2.4Ghz, RX RF Daughter Board Module is a small PCB design with 1 10 pin 2mm header, and 1 2 pin 2mm header that is pluggable.

2.1 Operating Frequencies

This unit operates only on two channels during transmit:

For the Bind Sequence – 2444MHz

For the Link sequence – 2435MHz

2.2 Output Power

The output power level for this unit is 1.1×10^{-6} Watts.

3. Application

The application for this product is the hobby industry as a remote control device.

4. Functional Overview

The Spectrum 2.4Ghz, RX RF Daughter Board Module provides a complete SPI to RF antenna wireless MODEM. The module is designed to implement wireless device links in the 2.4GHz ISM frequency band. It is intended for applications covered by Europe ETSI EN 301 489-1, ETSI EN 301 489-7& ETSI EN 300 328-2, and USA FCC Part 15.

The module contains a 2.4GHz GFSK radio transceiver, packet data buffering, packet framer, DSSS baseband controller, Received Signal Strength Indication (RSSI), and SPI interface for data transfer and device configuration.

The radio supports 98 discrete 1MHz channels (regulations may limit the use of some of these channels in certain jurisdictions). In DSSS modes the baseband performs DSSS spreading/de-spreading, while in GFSK Mode (1 Mb/s – GFSK) the baseband performs Start of Frame (SOF), End of Frame (EOF), detection and CRC16 generation and checking.

4.1 Link Layer Modes

The Spectrum 2.4Ghz, RX RF Daughter Board Module supports the following data packet features:

SOP – Packets begin with a 2-symbol Start of Packet (SOP) marker. This is required in GFSK and 8DR modes, but is optional in DDR mode and is not supported in SDR mode; if framing is disabled then an SOP event is inferred whenever two successive correlations are detected. The SOP_CODE_ADR code used for the SOP is different from that used for the "body" of the packet and if desired may be different length

EOP - There are two options for detecting the end of a packet. If SOP is enabled, then a packet length field may be enabled. GFSK and 8DR must enable the length field. This is the first 8-bits after the SOP symbol, and is transmitted at the payload data length field, plus two bytes for the CRC16 (if enabled). The alternative to using the length field is to infer an EOP condition from a configurable number of successive non-correlations; this option is not available in GFSK mode and is only recommended to enable when using SDR mode.

CRC16 – The device may be configured to append a 16-bit CRC16 to each packet. The CRC16 uses the USB CRC polynomial with the added programmability of the seed. If enabled, the receiver will verify the calculated CRC16 for the payload data against the received value in the CRC16 field. The starting value for the CRC16 calculation is configurable, and the CRC16 transmitted may be calculated using either the loaded seed value or a zero seed; the received data CRC16 will be checked against both the configured and zero CRC16 seeds.

CRC16 detects the following errors:

- Any one bit error
- Any two bits in error
- Any odd number of bits in error
- An error burst as wide as the checksum itself

4.2 Packet Buffers

All data transmission and reception utilizes the 16-byte packet buffers—one for transmission and one for reception. The transmit buffer allows a complete packet of up to 16-bytes of payload data to be loaded in one burst SPI transaction, and then transmitted with no further micro controller intervention. Similarly, the receive buffer allows an entire packet of payload data up to 16 bytes to be received with no firmware intervention required until packet reception is complete.
The Spectrum 2.4Ghz, RX RF Daughter Board Module supports packet length of up to 40 bytes; interrupts are provided to allow a micro controller to use transmit and receive buffers as FIFOs. When transmitting a packet longer than 16 bytes, the micro controller can load 16-bytes initially, and add further bytes to the transmit buffer as transmission of data creates space in the buffer. Similarly, when receiving packets longer than 16 bytes, the micro controller must fetch received data from the FIFO periodically during packet reception to prevent it from overflowing.

4.3 Data Rates

By combining the DATA_CODE_ADR code lengths and data transmission modes described above, the Spectrum 2.4Ghz, RX RF Daughter Board Module supports the following modes and data rates.

RF Transmission Mode	Raw Data Rate kbps
GFSK	1000.00
32-Chip 8DR	250.00
64-Chip 8DR[2]	125.00
32-Chip DDR[3]	62.50
64-Chip DDR[3]	31.25
64-Chip SDR[2,3]	15.63

Table 1: Data Rates

5. SPI Communication

The Spectrum 2.4Ghz, RX RF Daughter Board Module has an SPI interface supporting communications between an application MCU and one or more slave devices. The SPI interface supports single-byte and multi-byte serial transfers using either 4-pin or 3-pin interfacing. The SPI communications interface consists of Slave Select ( ), Serial Clock (SCK), and Master Out- Slave In
(MOSI), Master In-Slave Out (MISO), or Serial Data (SDAT). The SPI communications is as follows:

- Command Direction (bit 7) = “1” enables SPI write transaction. A “0” enables SPI read transactions.
- Command Increment (bit 6) = “1” enables SPI auto address increment. When set, the address field automatically increments at the end of each data byte in a burst access, otherwise the same address is accessed.
- Six bits of address.
- Eight bits of data.

The device receives SCK from an application MCU on the SCK pin. Data from the application MCU is shifted in on the MOSI pin. Data to the application MCU is shifted out on the MISO pin. The active-low Slave Select ( ) pin must be asserted to initiate an SPI transfer.

The application MCU can initiate SPI data transfers via a multi byte transaction. The first byte is the Command/Address byte, and the following bytes are the data, where the first byte can be followed by as many data bytes as desired. A burst transaction is terminated by de-asserting the slave select (= 1).

The SPI communications interface single read and burst read sequences are shown in Figure 3 and Figure 4, respectively.

The SPI communications interface single write and burst write sequences are shown in Figure 5 and Figure 6, respectively.

This interface may optionally be operated in a 3-pin mode with the MISO and MOSI functions combined in a single bidirectional data pin (SDAT). When using 3-pin mode, user firmware should ensure that the MOSI pin on the MCU is in a high impedance state except when MOSI is actively transmitting data.

The device registers may be written to or read from 1 byte at a time, or several sequential register locations may be written/read in a single SPI transaction using incrementing burst mode. In addition to single byte configuration registers, the device includes register files; register files are FIFOs written to and read from using non-incrementing burst SPI transactions.

The IRQ pin function may optionally be multiplexed onto the MOSI pin; when this option is enabled the IRQ function is not available while the pin is low. When using this configuration, user firmware should ensure that the MOSI pin on the Spectrum 2.4Ghz, RX RF Daughter Board Module is in a high impedance state whenever the pin is high.

The SPI interface is not dependent on the internal 12-MHz clock, and registers may therefore be read from or written to while the device is in sleep mode, and the 12-MHz oscillator disabled.

	Byte 1			Byte 1+N
Bit#	7	6	[5:0]	[7:0]
Bit Name	Dir	Inc	Address	Data

Table 2: SPI Transaction Format

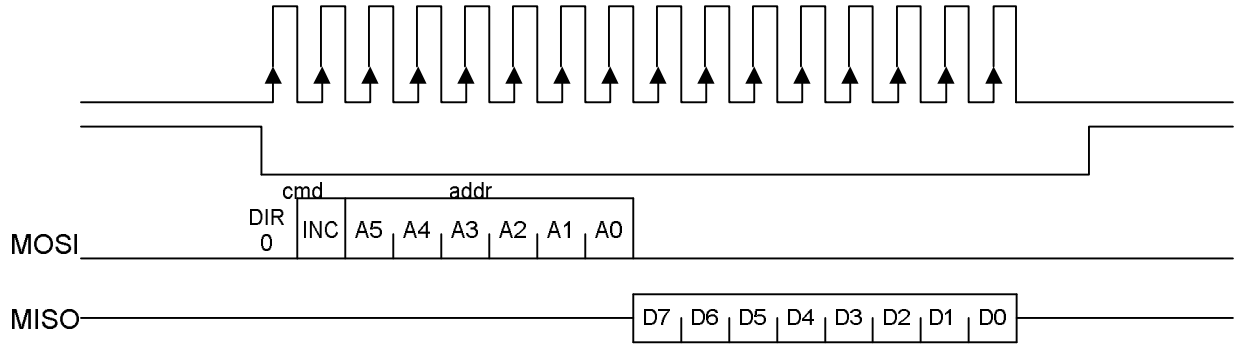

Table 2: SPI Single Read Sequence

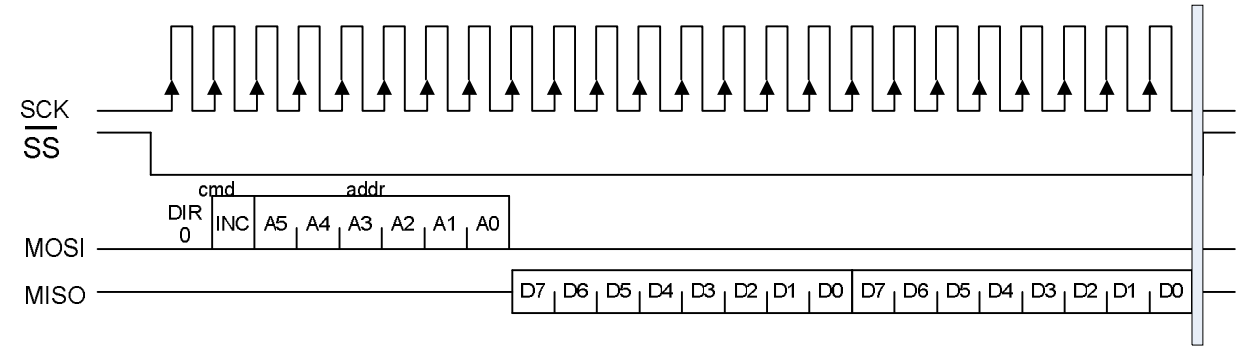

Table 3: SPI Incrementing Burst Read Sequence

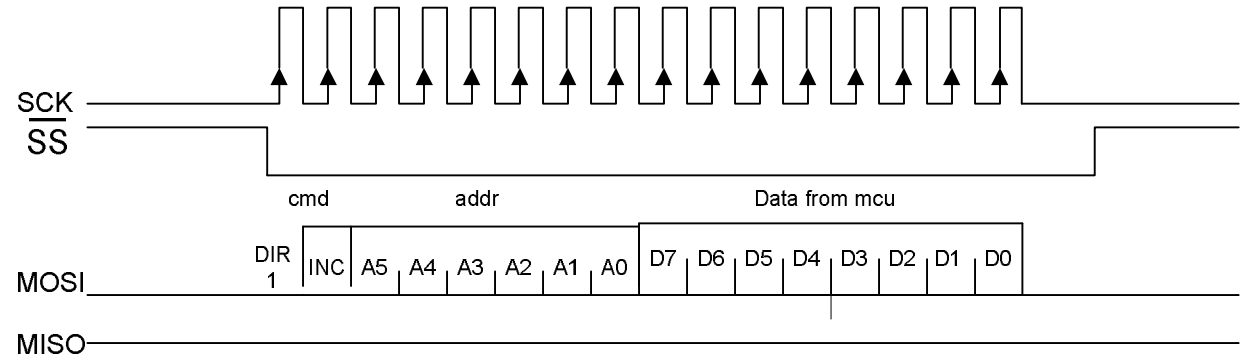

Table 4: SPI Single Write Sequence

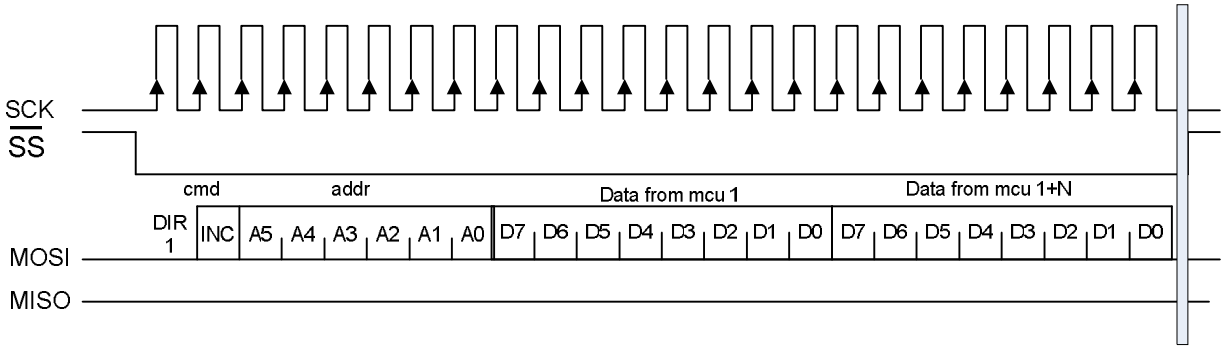

Table 5: SPI Incrementing Burst Write Sequence

Operating RF Frequencies
2405Mhz – 2452Mhz
(Controlled by firmware)

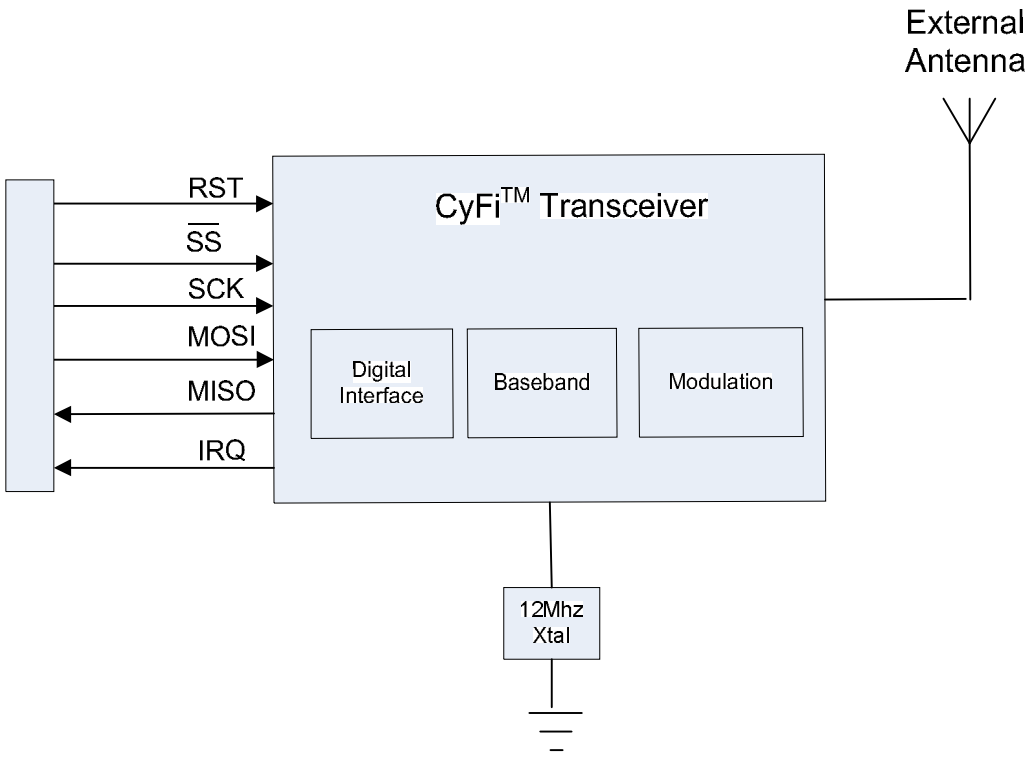

Table 6: Module Block Diagram

6. Power Management

The operating voltage of the module is 3.3V DC, which is applied to the V_{cc} pin 6 of the connector. The device can be shutdown to a fully static sleep mode by writing FRC_END = 1 and END State =000 bits of the XACT_CFG_ADR register over the SPI. The CYRF6936/7936 chip will enter the sleep mode 35us after the last SCK positive edge at the end of the SPI transaction. Alternatively, the CYRF6936/7936 may be configured to automatically enter the sleep mode after completing packet transmission or reception. When in sleep mode, the on-chip oscillator is stopped, but the SPI remains functional . The CYRF6936/7936 chip will wake from the sleep mode automatically when the module is commanded to enter transmit or receive mode. When resuming from the sleep mode, there is a short delay while the oscillator restarts and locks. The CYRF6936/7936 chip may be configured to assert the IRQ pin when the oscillator has stabilized.

承 認 書

SPECIFICATION FOR APPROVAL

公司名稱：設新企業有限公司

客戶名稱：智晟股份有限公司

客戶料號：E44053

概　　述：2.4GHz RX antenna

日　期：97 年 11 月 10 日

簽核及意見欄

全 部 承 認 FULLY APPROVED	部 份 承 認 PARTILLY APPROVED	修 訂 承 認 REVISE APPROVED

承認書 List:

P2(產品圖面&尺寸)　　P3 (測試報告)

P4~P21 (SGS 測報)

承辦人員：劉杰璋 陳維欣

TEL：(02) 8512-3409

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設新企業股份有限公司
NEW PREMIER ENTERPRISE CO., LTD.

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Item

Modification History:

REV.	Date	Content
01	2008/7/31	

REV	CONTENTS	DATE

NEW PREMIER
設新企業股份有限公司

DRAWED	HAO			DWG NO:	E44053		
CHKD	HAO						
APPD	JORDAN			CUSTOMER	--		
MATERIAL	--	SCALE	10:1	SIZE	A4	REV	001
FINISH	--	UNITS	mm	DATE	2008/10/28		

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Electrical Properties

Type	RX Antenna
Frequency Range	2.4~2.5GHz
Impedance	50 Ohm
VSWR	≦2.0

Mechanical Properties

Material	
Connector	
Cable Type	1.13
dimension	270mm* § 1.13


2008/12/03 Wed 15:56:17
CH1 S11 LOG MAG REF 8.000 dB 5.000 dB/
CH2 S11 SWR REF 1.000 1.000 /
-25.617 dB
1.107
Cor
Cor
CENTER 2.45GHz
[10.00 dBm]
SPAN 300MHz
CH1 MARKER LIST
1: 2.400 416GHz -19.551 dB
2: 2.450 000GHz -25.617 dB
3: 2.500 000GHz -22.850 dB
CH2 MARKER LIST
1: 2.400 416GHz 1.235
2: 2.450 000GHz 1.107
3: 2.500 000GHz 1.155
DISPLAY
DISPLAY DATA
DISPLAY MEMORY
DISPLAY DATA&MEM
Return

設新企業股份有限公司

NEW PREMIER ENTERPRISE CO., LTD.

線材規格

CABLE SPECIFICATION

SPECIFICATION: 1.13mm CABLE

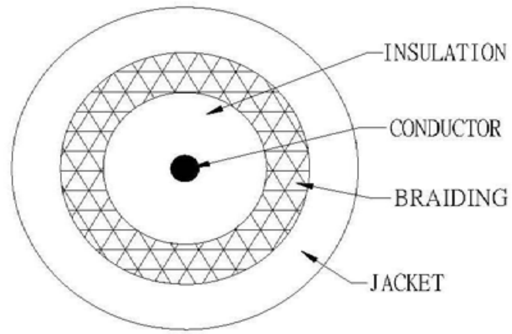
ITEM		SPECIFICATION
CONDUCTOR	AWG	30AWG
	MATERIAL	Silver-plated copper wire stranded conductor
	COND.SIZE	7/0.08 ㎜
INSULATION	MATERIAL	Teflon FEP
	O . D	0.68±0.03 ㎜
	N O.	1C
	COLOR	Natural color
BRAID	MATERIAL	Silver-plated copper wire
COPPER	SIZE	4/16/0.05 Min.90% ↑
JACKET	MATERIAL	Teflon FEP
	COLOR	White,Black,Brown,Gray
	O . D	1.13+0.08/-0.05 ㎜

Character of electrical

Item		Unit	Detail of spec.
1.Capacitance(Nom.)	AT 1KHz	pF/M	95
2.Impedance	-------	0	50±2
3.Attenuation(Max.)	1.0GHZ	dB/M	2.0
	2.0GHZ	dB/M	2.9
	2.4GHZ	dB/M	3.2
	3.0GHZ	dB/M	3.7
	4.0GHZ	dB/M	4.3
	5.0GHZ	dB/M	4.8
	6.0GHZ	dB/M	5.3

PHYSICAL PROPERTIES OF JACKET

CONSRUCTION D.W.G



COLOUR CODE:

1. 30AWG*1C

MARKING

REMARK

Master Wave Technology Co., Ltd.

PART NO.			
APPROVED		CUSTOMER	
CHECKED		REV	A
DRAWING	*Dyan*	DATE	2007/10/8