LEXI-R422

Ultra-small LTE-M / NB-IoT / EGPRS module

System integration manual

Abstract

This document describes the features and the integration of the ultra-small LEXI-R422 cellular modules. These modules are a complete, cost efficient, performance optimized, multi-mode and multi-band LTE-M / NB-IoT / EGPRS solution in the compact LEXI form factor.

UBX-23007449 - R02
C1-Public

Document information

Title	**LEXI-R422**
Subtitle	Ultra-small LTE-M / NB-IoT / EGPRS module
Document type	System integration manual
Document number	UBX-23007449
Revision and date	R02 06-Oct-2023
Disclosure restriction	C1-Public

Product status	**Corresponding content status**	
Functional sample	Draft	For functional testing. Revised and supplementary data will be published later.
In development / Prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	**Type number**	**Firmware version**	**Notification reference**	**Product status**
LEXI-R422	LEXI-R422-01B-00	Modem: 01.25 Application: A01.06	UBXDOC-686885345-1805	Engineering sample

Contents

Document information **2**
Contents **3**
1 System description **6**
1.1 Overview 6
1.2 Architecture 8
1.3 Pin-out 9
1.4 Operating modes 12
1.5 Supply interfaces 15
1.5.1 Module supply input (VCC) 15
1.5.2 Generic digital interfaces supply output (V_INT) 21
1.6 System function interfaces 22
1.6.1 Module power-on 22
1.6.2 Module power-off 23
1.6.3 Module reset 25
1.7 Antenna interfaces 26
1.7.1 Cellular antenna RF interface (ANT) 26
1.7.2 Antenna detection interface (ANT_DET) 27
1.8 SIM interface 27
1.8.1 SIM interface 27
1.8.2 SIM detection interface 27
1.9 Data communication interfaces 27
1.9.1 UART interfaces 28
1.9.2 USB interface 29
1.9.3 I2C interface 29
1.10 General purpose input / output 30
1.11 Cellular antenna dynamic tuner interface 30
1.12 Reserved pins (RSVD) 31
2 Design-in **32**
2.1 Overview 32
2.2 Supply interfaces 33
2.2.1 Module supply (VCC) 33
2.2.2 Generic digital interfaces supply output (V_INT) 47
2.3 System functions interfaces 48
2.3.1 Module PWR_CTRL input 48
2.4 Antenna interfaces 49
2.4.1 Cellular antenna RF interface (ANT) 49
2.4.2 Cellular and GNSS RF coexistence 59
2.4.3 Antenna detection interface (ANT_DET) 61
2.4.4 Cellular antenna dynamic tuner interface 63
2.5 SIM interface 65

2.5.1 Guidelines for SIM circuit design ... 65
2.5.2 Guidelines for SIM layout design ... 69
2.6 Data communication interfaces ... 70
2.6.1 UART interfaces ... 70
2.6.2 USB interface ... 75
2.6.3 I2C interface ... 78
2.7 General purpose input / output ... 80
2.7.1 Guidelines for GPIO circuit design ... 80
2.7.2 Guidelines for general purpose input/output layout design ... 80
2.8 Reserved pins (RSVD) ... 81
2.9 Module placement ... 81
2.10 Module footprint and paste mask ... 82
2.11 Thermal guidelines ... 83
2.12 Schematic for LEXI-R422 modules integration ... 84
2.13 Design-in checklist ... 85
2.13.1 Schematic checklist ... 85
2.13.2 Layout checklist ... 85
2.13.3 Antenna checklist ... 86
3 Handling and soldering ... 87
3.1 Packaging, shipping, storage and moisture preconditioning ... 87
3.2 Handling ... 87
3.3 Soldering ... 88
3.3.1 Soldering paste ... 88
3.3.2 Reflow soldering ... 88
3.3.3 Optical inspection ... 89
3.3.4 Cleaning ... 89
3.3.5 Repeated reflow soldering ... 90
3.3.6 Wave soldering ... 90
3.3.7 Hand soldering ... 90
3.3.8 Rework ... 90
3.3.9 Conformal coating ... 90
3.3.10 Casting ... 90
3.3.11 Grounding metal covers ... 91
3.3.12 Use of ultrasonic processes ... 91
4 Approvals ... 92
4.1 Product certification approval overview ... 92
4.2 US Federal Communications Commission notice ... 93
4.2.1 Integration instructions for host product manufacturers ... 93
4.3 Innovation, Science, Economic Development Canada notice ... 95
4.3.1 Declaration of Conformity ... 95
4.3.2 Modifications ... 96
4.4 European Conformance CE mark ... 97

4.5 UK Conformity Assessed (UKCA) 98
5 Product testing 99
5.1 Validation testing and qualification 99
5.2 Production testing 100
5.2.1 u-blox in-line production tests 100
5.2.2 Production test parameters for OEM manufacturers 100
Appendix 102
A Migration from SARA-R42 series modules 102
B Glossary 104
Related documentation 107
Revision history 107
Contact 108

1 System description

1.1 Overview

The LEXI-R422 modules are a multi-band LTE-M / NB-IoT / EGPRS multi-mode solution in the ultra-small LEXI LGA form factor (16.0 x 16.0 mm, 133-pin), allowing an easy integration into compact designs.

LEXI-R422 modules provide software-based multi-band configurability enabling international multi-regional coverage in LTE-M / NB-IoT and EGPRS radio access technologies.

LEXI-R422 modules offer data communications over an extended operating temperature range of -40 °C to +85 °C, with low power consumption, and with coverage enhancement for deeper range into buildings and basements (and underground with NB-IoT).

Measuring just 16x16 mm, LEXI-R422 modules are ideal for size-constrained devices like people and animal wearables, small asset trackers, portable healthcare systems and other small IoT applications.

With many interface options and an integrated IP stack, LEXI-R422 modules are the optimal choice for LPWA applications with low to medium data throughput rates, as well as devices that require long battery lifetimes, such as used in smart metering, smart lighting, telematics, asset tracking, remote monitoring, alarm panels, and connected healthcare.

Furthermore, the LEXI-R422 modules support a comprehensive set of 3GPP Release 14 features for LTE Cat M1 and Cat NB2 that are relevant for IoT applications.

Customers can future-proof their solutions by means of Over-The-Air firmware updates, thanks to the uFOTA client/server solution that utilizes LWM2M, a light and compact protocol ideal for IoT.

Model	Region	RAT			Positioning			u-blox services			Interfaces						Features														Grade		
		LTE category	LTE FDD bands	(E)GPRS 4-band	Integrated GNSS receiver	Dedicated GNSS antenna interface	External GNSS control via modem	MQTT Anywhere, MQTT Flex	AssistNow	CellLocate®	UARTs	USB (for FW update and diagnostics)	I2C	SIM	GPIOs	Digital audio (I2S)	Secure boot, updates, and production	Antenna dynamic tuning	Ultra-low consumption in PSM / eDRX	Embedded TCP/UDP stack	Embedded HTTPS, FTPS	Embedded TLS, DTLS	FW update via serial (FOAT)	u-blox FW update Over the Air (uFOTA)	LwM2M with dynamically loaded objects	Embedded MQTT, MQTT-SN	Embedded CoAP	Last gasp	Jamming detection	Antenna and SIM detection	Standard	Professional	Automotive
LEXI-R422	Multi Region	M1 NB2	*	•			•	•	•	•	•	•	•	•	•		•	•	•	•	•	•	•	•	•	•	•	•	•	•		•	

* = LTE bands 1, 2, 3, 4, 5, 8, 12, 13, 18, 19, 20, 25, 26, 28, 66, 85

Table 1: LEXI-R422 main features summary

Table 2 summarizes cellular radio access technologies characteristics and features of the modules.

Item	LEXI-R422
Protocol stack	3GPP Release 14
RAT	LTE Cat M1 Half-Duplex LTE Cat NB2 Half-Duplex 2G GPRS / EGPRS TDMA
LTE FDD bands	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (750 MHz) Band 18 (850 MHz) Band 19 (850 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) Band 26 (850 MHz) Band 28 (700 MHz) Band 66 (1700 MHz) Band 85 (700 MHz)
2G bands	GSM 850 MHz E-GSM 900 MHz DCS 1800 MHz PCS 1900 MHz
Power class	LTE category M1 / NB2: Class 3 (23 dBm) 2G GMSK: Class 4 (33 dBm) in 850/900 MHz Class 1 (30 dBm) in 1800/1900 MHz 2G 8-PSK: Class E2 (27 dBm) in 850/900 MHz Class E2 (26 dBm) in 1800/1900 MHz
Data rate	LTE category M1: up to 1119 kbit/s UL up to 588 kbit/s DL LTE category NB2: up to 158.5 kbit/s UL up to 127 kbit/s DL GPRS multi-slot class 33[1]: up to 85.6 kb/s UL up to 107 kb/s DL EGPRS multi-slot class 33[1]: up to 236.8 kb/s UL up to 296 kb/s DL

Table 2: LEXI-R422 modules cellular characteristics summary

[1] GPRS/EGPRS multi-slot cass 33 implies a maximum of 5 slots in Down-Link and 4 slots in Up-Link with 6 slots in total.

1.2 Architecture

Figure 1 summarizes the internal architecture of LEXI-R422 modules.

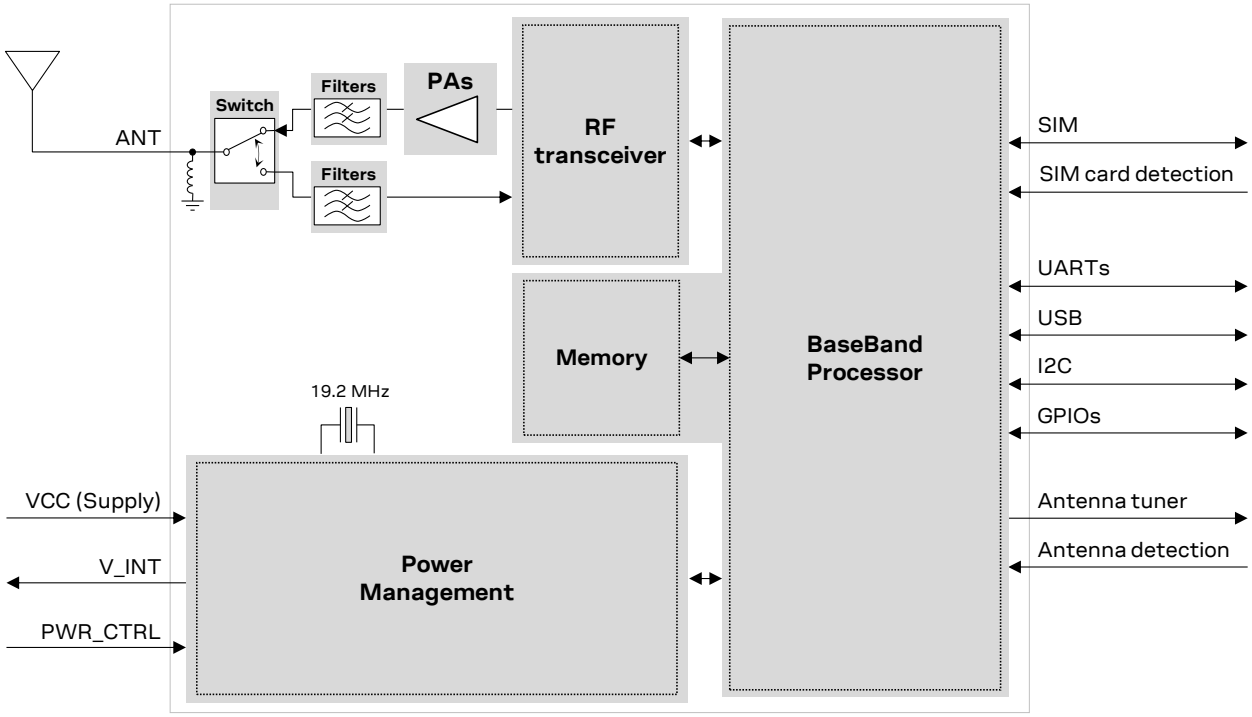

Figure 1: LEXI-R422 modules' simplified block diagram

Below is a detailed description of LEXI-R422 modules sections shown in figure above.

Cellular RF section

The cellular RF section is composed of the following main elements:

- RF switch connecting the antenna port (**ANT**) to the suitable RF Tx / Rx paths
- Power Amplifiers (PA) amplifying the Tx signal modulated and pre-amplified by the RF transceiver
- RF filters along the Tx and Rx signal paths providing RF filtering
- RF transceiver, performing modulation, up-conversion and pre-amplification of baseband signals for transmission, and performing down-conversion and demodulation of RF signals for reception
- 19.2 MHz crystal oscillator generating the reference clock signal for the RF transceiver and the baseband system, when the related system is in active mode or connected mode

Baseband and power management section

The baseband and power management section, is composed of the following main elements:

- On-chip modem processor, vector signal processor, with dedicated hardware assistance for signal processing and system timing
- On-chip modem processor, with interfaces control functions
- On-chip voltage regulators to derive all the internal or external (**V_SIM**, **V_INT**) supply voltages from the module supply input **VCC**
- Dedicated flash memory IC
- Calibrated low frequency RC oscillator to provide the clock reference in the low power idle mode, which can be enabled using the +UPSV AT command, and in the PSM / eDRX deep-sleep mode, which can be enabled using the +CPSMS / +CEDRXS / +UPSMVER AT commands

1.3 Pin-out

Table 3 lists the pin-out of the LEXI-R422 modules, with pins grouped by function.

Function	Name	No	ID	I/O	Description	Remarks
Power	VCC	40-42	A12-14	I	Module supply input	VCC supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for functional description / requirements. See section 2.2.1 for external circuit design-in.
	GND	1,3,50,52, 53,56-61, 64-70, 73-79, 82-88, 91-97, 100-106, 109-115, 116-124, 125-133	B1,D1,A4,A2, C3,C7-11,C13, E6-11,E13, F6-11,F13, G6-11,G13, H6-11,H13, J6-11,J13, K6-11,K13, L3,L5-11,L13, N3,N5-11,N13	N/A	Ground	GND pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.
	V_INT	43	A11	O	Generic digital interfaces supply output	V_INT = 1.8 V (typical) generated by internal regulator when the module is switched on, outside the low power PSM / eDRX deep-sleep mode. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in. Provide test point for diagnostic purposes.
System	PWR_CTRL	27	P15	I	Power-on / power-off / reset input	Internal pull-up resistor. See section 1.6.1, 1.6.2 and 1.6.3 for functional description. See section 2.3.1 for external circuit design-in. Provide test point for diagnostic purposes.
Antenna	ANT	51	A3	I/O	Cellular antenna	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and application device compliance with required certification schemes. See section 1.7.1 for functional description and requirements. See section 2.4 for external circuit design-in.
	ANT_DET	49	A5	I	Antenna detection	ADC for antenna presence detection function. See section 1.7.2 for functional description. See section 2.4.3 for external circuit design-in.
SIM	VSIM	33	H15	O	SIM supply output	Supply output for external SIM / UICC. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	32	J15	I/O	SIM data	Data input/output for external SIM / UICC. Internal pull-up to VSIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	31	K15	O	SIM clock	Clock output for external SIM / UICC See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	30	L15	O	SIM reset	Reset output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.

Function	Name	No	ID	I/O	Description	Remarks
UART	RXD	4	E1	O	UART data output	Primary UART circuit 104 (RxD) in ITU-T V.24, for AT commands, data, Mux, FOAT. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	TXD	5	F1	I	UART data input	Primary UART circuit 103 (TxD) in ITU-T V.24, for AT commands, data, Mux, FOAT. Internal active pull-up to V_INT. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	CTS	6	G1	O	UART clear to send output	Primary UART circuit 106 (CTS) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	7	H1	I	UART request to send input	Primary UART circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to V_INT. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	11	M1	O / I	UART data set ready output / AUX UART request to send input	Primary UART circuit 107 (DSR) in ITU-T V.24, configurable as auxiliary UART RTS input. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RI	10	L1	O / O	UART ring indicator output / AUX UART clear to send output	Primary UART circuit 125 (RI) in ITU-T V.24, configurable as auxiliary UART CTS output. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	9	K1	I / I	UART data terminal ready input / AUX UART data input	Primary UART circuit 108/2 (DTR) in ITU-T V.24, configurable as auxiliary UART TxD input. Internal active pull-up to V_INT. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DCD	8	J1	O / O	UART data carrier detect output / AUX UART data output	Primary UART circuit 109 (DCD) in ITU-T V.24, configurable as auxiliary UART RxD output. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
USB	USB_5V0	22	R10	I	USB detect input	VBUS sense input pin to enable the USB interface. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for FW update and diagnostic.
	USB_3V3	19	R7	I	USB supply input	VBUS supply input pin to supply the USB interface. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for FW update and diagnostic.
	USB_D-	20	R8	I/O	USB Data Line D-	USB available only for FW update and diagnostic. 90 Ω nominal differential impedance. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for FW update and diagnostic.
	USB_D+	21	R9	I/O	USB Data Line D+	USB available only for FW update and diagnostic. 90 Ω nominal differential impedance. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for FW update and diagnostic.

Function	Name	No	ID	I/O	Description	Remarks
I2C	SCL	12	N1	O	I2C bus clock line	Fixed open drain, to communicate with I2C devices. Internal pull-up to V_INT: no need external pull-up. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	SDA	13	P1	I/O	I2C bus data line	Fixed open drain, to communicate with I2C devices. Internal pull-up to V_INT: no need external pull-up. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
GPIO	GPIO1	14	R2	I/O	GPIO	Pin with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO2	15	R3	I/O	GPIO	Pin with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO3	16	R4	I/O	GPIO	Pin with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO4	17	R5	I/O	GPIO	Pin with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO5	18	R6	I/O	GPIO	Pin with alternatively configurable functions. See section 1.10 for functional description. See section 2.7 for external circuit design-in.
	GPIO6	29	M15	I/O	GPIO	Pin with alternatively configurable functions. See sections 1.8.2 / 1.10 for functional description. See sections 2.5 / 2.7 for external circuit design-in.
Antenna tuning	RFCTRL1	45	A9	O	RF GPIO for antenna tuner	Optional output for antenna dynamic tuning. See section 1.10 / 1.11 for functional description. See section 2.4.4 for external circuit design-in.
	RFCTRL2	44	A10	O	RF GPIO for antenna tuner	Optional output for antenna dynamic tuning. See section 1.10 / 1.11 for functional description. See section 2.4.4 for external circuit design-in.
Reserved	RSVD	2,23-26, 28,34,35, 36-38, 39,46,47, 48,54,55, 62,63,71, 72,80,81, 89,90,98, 107,108	C1,R11-14, N15,G15,F15, E15,D15,C15, B15,A8,A7, A6,C5,C6, E3,E5,F3, F5,G3,G5, H3,H5,J3, K3,K5	N/A	Reserved pin	Leave unconnected. See sections 1.12 and 2.8.
	RSVD	99	J5	N/A	Reserved pin	Provide test point for diagnostic purposes. See sections 1.12 and 2.8.

Table 3: LEXI-R422 modules pin definition, grouped by function

1.4 Operating modes

LEXI-R422 modules have several operating modes. The operating modes are defined in Table 4 and described in detail in Table 5, providing general guidelines for operation.

General status	Operating mode	Definition
Power-down	**Not-powered mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-off mode	**VCC** supply within operating range and module is switched off.
Normal Operation	**Deep-sleep mode**	Only the RTC runs. The processor and other parts of the module are switched off.
	Idle mode	Module processor runs at the minimum frequency to save power consumption.
	Active mode	Module processor runs at normal operating frequency to enable related functions.
	Connected mode	RF Tx/Rx enabled with processor running at related operating frequency.

Table 4: LEXI-R422 modules operating modes definition

Mode	Description	Transition between operating modes
Not-powered	Module is switched off. Application interfaces are not accessible.	When VCC supply is removed, the modules enter not-powered mode. When in not-powered mode, the module can enter power-off mode applying VCC supply (see 1.6.1).
Power-off	Module is switched off: normal shutdown by an appropriate power-off event (see 1.6.2). Application interfaces are not accessible.	The modules enter power-off mode from active mode when the host processor implements a clean switch-off procedure, by sending the +CPWROFF AT command or by using the PWR_CTRL pin (see 1.6.2). When in power-off mode, the modules can be switched on by the host processor using the PWR_CTRL input pin (see 1.6.1). When in power-off mode, the modules enter not-powered mode by removing VCC supply.
Deep-sleep	Module is in RTC-only mode: only the internal Real Time Clock is active. The RF section and the application interfaces are temporarily disabled and switched off: the module is temporarily not ready to communicate with an external device by means of the application interfaces as configured to reduce the current consumption to the minimum possible (see section 1.5.1.4).	The modules automatically switch from the active mode to the ultra-low power deep-sleep mode whenever possible, upon expiration of the T3324 active timer set by the network (entering the Power Saving Mode defined in 3GPP Rel.13, depending on the configuration set by +CPSMS AT command), upon expiration of the 6 s AT inactivity timer (depending on the configuration set by the +UPSV AT command), in-between eDRX cycles when not listening to paging (depending on the configuration set by the +UPSMVER AT command), if no other concurrent activities are executed. When the module is in the ultra-low power deep-sleep mode, it automatically switches on to the active mode upon expiration of the T3412 periodic TAU timer set by the network according to the Power Saving Mode defined in 3GPP Rel.13, it automatically switches on in-between eDRX cycles when listening to paging according to the timing set by the network, or it can be switched on to the active mode by the host processor using the PWR_CTRL input pin (see 1.6.1). For further details, see the application development guide [3] and the AT commands manual [2].

Mode	Description	Transition between operating modes
Idle	Module is switched on with application interfaces temporarily disabled: the module is temporarily not ready to communicate with an external device by means of the application interfaces as configured to reduce the current consumption (see section 1.5.1.5).	The modules automatically switch from the active mode to low power idle mode whenever possible, depending on concurrent activities executed by the module, upon expiration of the 6 seconds AT inactivity timer (with AT+UPSV=4 setting), or upon DTR set to OFF (with AT+UPSV=3 setting), if low power configuration is enabled (see the AT commands manual [2], +UPSV AT command). When in low power idle mode, the module switches to the active mode upon data reception over UART serial interface (with AT+UPSV=4 setting, and in this case the first character received in low power idle mode wakes up the system, it is not recognized as valid communication character, and the recognition of the subsequent characters occurs only after the complete system wake-up), or upon DTR set to ON (with AT+UPSV=3 setting).
Active	Module is switched on with application interfaces enabled or not suspended: the module is ready to communicate with an external device by means of the application interfaces, with related necessary current consumption (see section 1.5.1.6).	The modules enter active mode from power-off mode when the host processor implements a clean switch-on procedure by using the PWR_CTRL pin (see 1.6.1). The modules enter active mode from the ultra-low power deep-sleep mode upon expiration of the T3412 periodic TAU timer set by the network, to receive the paging in-between eDRX cycles according to the timing set by the network, or if the host processor wakes up the module using the PWR_CTRL input pin (see 1.6.1). The modules enter power-off mode from active mode when the host processor implements a switch-off procedure (see 1.6.2). The modules automatically switch from active to ultra-low power deep-sleep mode whenever possible, upon expiration of the T3324 active timer set by the network (depending on +CPSMS AT command setting), upon expiration of the 6 s AT inactivity timer (depending on the +UPSV AT command setting), in-between eDRX cycles when not listening to paging (depending on the +UPSMVER AT command setting), if no other concurrent activities are executed. The module switches from active to connected mode when a RF Tx/Rx data connection is initiated or when RF Tx/Rx activity is required due to a connection previously initiated. The module switches from connected to active mode when a RF Tx/Rx data connection is terminated or suspended.
Connected	RF Tx/Rx data connection is in progress, with related necessary current consumption (see sections 1.5.1.2 and 1.5.1.3). The module is prepared to accept data signals from an external device.	When a data connection is initiated, the module enters connected mode from active mode. Connected mode is suspended if Tx/Rx data is not in progress. In such cases the module automatically switches from connected to active mode and then, depending on the +UPSV, +CPSMS and +UPSMVER AT commands settings, the module automatically switches to the low power idle mode and/or to the ultra-low power deep-sleep mode whenever possible. Vice-versa, the module wakes up from low power idle mode or from ultra-low power deep-sleep mode to active mode and then connected mode if RF Tx/Rx activity is necessary. When a data connection is terminated, the module returns to the active mode.

Table 5: LEXI-R422 modules operating modes description

The initial operating mode of LEXI-R422 modules is the one with **VCC** supply not present or below the operating range: the modules are switched off in not-powered mode.

Once a valid **VCC** supply is applied to the LEXI-R422 modules, they remain switched off in the power-off mode. Then the proper toggling of the **PWR_CTRL** input line is necessary to trigger the switch-on routine of the modules that subsequently enter the active mode.

LEXI-R422 modules are ready to operate when in active mode: the available communication interfaces are completely functional and the module can accept and respond to AT commands, entering connected mode upon cellular RF signal reception / transmission.

The external GNSS can be concurrently enabled by the dedicated +UGPS AT command.

LEXI-R422 modules switch from active mode to the low power idle mode whenever possible, if the low power configuration is enabled by the dedicated +UPSV AT command. The low power idle mode can last for different time periods according to the specific +UPSV AT command setting, according to the DRX / eDRX setting, and according to the concurrent activities executed by the module.

LEXI-R422 modules enter the User Equipment (UE) power saving mode (PSM) defined in 3GPP Rel.13 whenever possible, if PSM is enabled by the +CPSMS / +UCPSMS AT commands, and according to the +UMNOPROF AT command settings. The PSM can last for different time periods according to the T3412 periodic TAU timer set by the network. Then, the modules enter the ultra-low power deep-sleep mode whenever possible, if no other concurrent activities are executed by the module.

Modules may automatically enter the ultra-low power deep-sleep mode in-between eDRX cycles, whenever possible, if the functionality is enabled using the +UPSMVER AT command.

Once the modules enter the ultra-low power deep-sleep mode, the available communication interfaces are not functional: a wake-up event, consisting in proper toggling of the **PWR_CTRL** input input line or the expiration of the timer set by the network, is necessary to trigger the wake-up routine of the modules that subsequently enter back into the active mode.

LEXI-R422 modules can be gracefully switched off by the dedicated +CPWROFF AT command, or by proper toggling of the **PWR_CTRL** input.

Figure 2 describes the transition between the different operating modes.

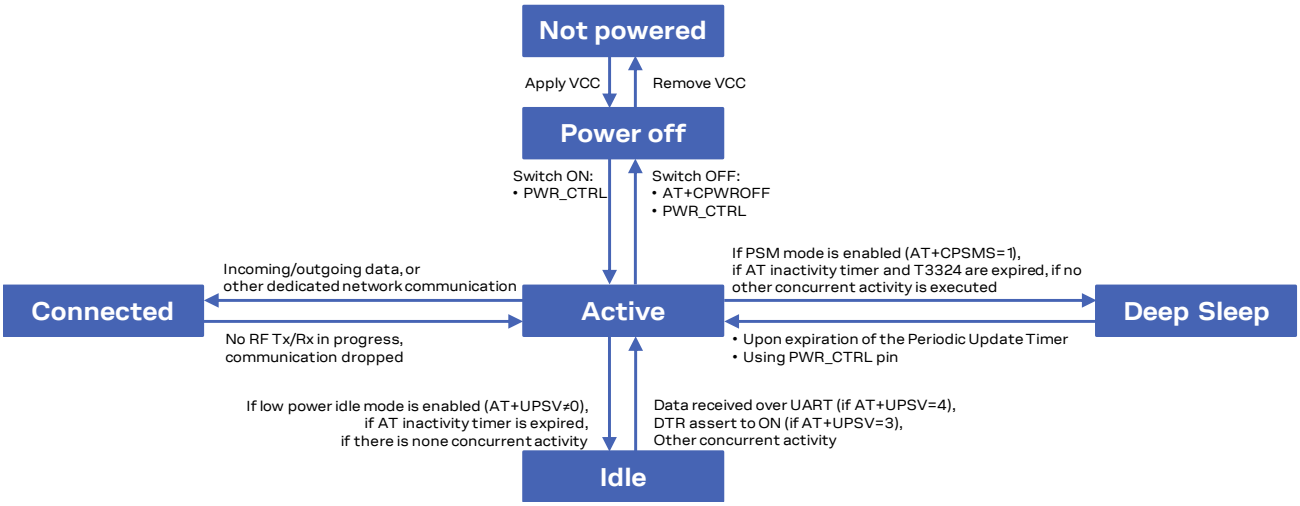

Figure 2: LEXI-R422 modules operating modes transitions

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

Voltage must be stable, because during operation, the current drawn by the LEXI-R422 modules through the **VCC** pins can vary by several orders of magnitude, depending on the operating mode and state (as described in sections 1.5.1.2, 1.5.1.3, 1.5.1.4 and 1.5.1.6).

It is important that the supply source is able to withstand both the maximum pulse current occurring during a transmit burst at maximum power level and the average current consumption occurring during Tx / Rx call at maximum RF power level (see the LEXI-R422 data sheet [1]).

LEXI-R422 modules, supporting 2G radio access technology, provide separate supply inputs over the three **VCC** pins:

- **VCC** pins A13 and A14 represent the supply input for the internal RF power amplifier, demanding most of the total current drawn of the module when RF transmission is enabled during a call
- **VCC** pin A12 represents the supply input for the internal baseband power management unit, demanding minor part of the total current drawn of the module when RF transmission is enabled during a call

Figure 3 provides a simplified block diagram of LEXI-R422 modules internal VCC supply routing.

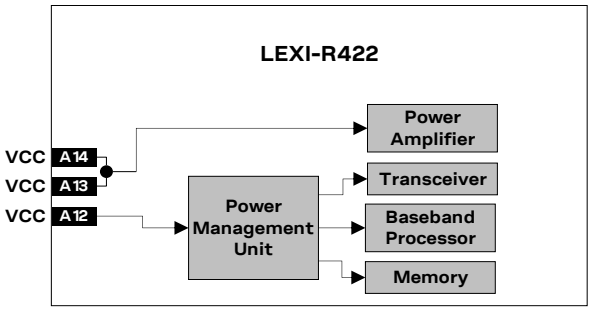

Figure 3: Block diagram of LEXI-R422 modules internal VCC supply routing

1.5.1.1 VCC supply requirements

Table 6 summarizes the requirements for the VCC modules supply. See section 2.2.1 for suggestions to correctly design a **VCC** supply circuit compliant with the requirements listed in Table 6.

⚠ The supply circuit affects the RF compliance of the device integrating LEXI-R422 modules with applicable required certification schemes as well as antenna circuit design. RF performance is optimized by fulfilling the requirements summarized in the Table 6.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.2 V / 4.5 V	Operating within 3GPP / ETSI specifications: RF performance is optimized when **VCC** PA voltage is inside the normal operating range limits.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.0 V / 4.5 V	Operating with possible slight deviation in RF performance outside normal operating range. **VCC** voltage must be above the extended operating range minimum limit to switch-on the module and to avoid possible switch-off of the module. Operation above **VCC** extended operating range is not recommended and may affect device reliability.
VCC average current	Support with adequate margin the highest averaged **VCC** current consumption value in connected mode conditions specified in the LEXI-R422 data sheet [1]	The maximum average current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. Section 1.5.1.2 describes current consumption profiles in connected mode.
VCC peak current	Support with adequate margin the highest peak **VCC** current consumption value in Tx connected mode conditions specified in the LEXI-R422 data sheet [1]	The maximum peak Tx current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. Sections 1.5.1.2 and 1.5.1.3 describe current consumption profiles in connected mode.
VCC voltage drop during Tx slots	Lower than 400 mV	**VCC** voltage drop directly affects the RF compliance with applicable certification schemes. Figure 6 describes **VCC** voltage drop during 2G Tx slots.
VCC voltage ripple during Tx	Noise in the supply pins must be minimized	High supply voltage ripple values during RF transmissions in connected mode directly affect the RF compliance with the applicable certification schemes.
VCC under/over-shoot at start/end of Tx slots	Absent or at least minimized	**VCC** under/over-shoot directly affects the RF compliance with applicable certification schemes. Figure 6 describes **VCC** voltage under/over-shoot.

Table 6: VCC modules supply requirements

1.5.1.2 VCC current consumption in LTE connected mode

During an LTE connection, the LEXI-R422 modules transmit and receive in half duplex mode.

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 0.5 ms (time length of one Resource Block), thus the rate of power change can reach a maximum rate of 2 kHz.

Figure 4 shows an example of LEXI-R422 modules current consumption profile versus time in connected mode: transmission is enabled for one sub-frame (1 ms) according to LTE Category M1 half-duplex connected mode.

Detailed current consumption values can be found in the LEXI-R422 data sheet [1].

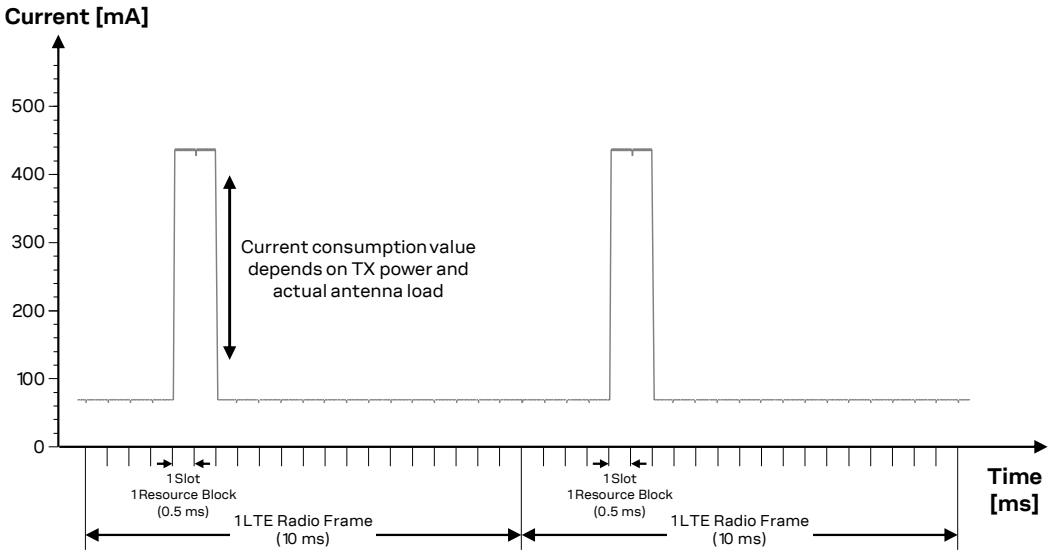

Figure 4: VCC current consumption profile versus time during LTE Cat M1 half-duplex connection

1.5.1.3 VCC current consumption in 2G connected mode

When a 2G call is established, the **VCC** consumption is determined by the current consumption profile typical of the 2G transmitting and receiving bursts.

The current consumption peak during a transmission slot is strictly dependent on the transmitted power, which is regulated by the network. The transmitted power in the transmit slot is also the more relevant factor for determining the average current consumption.

If the module is transmitting in 2G single-slot mode in the 850 or 900 MHz bands at the maximum RF power control level (approximately 2 W or 33 dBm in the Tx slot/burst), then the current consumption can reach a high peak / pulse (see the LEXI-R422 data sheet [1]) for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), that is, with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access).

If the module is transmitting in 2G single-slot mode in the 1800 or 1900 MHz bands, the current consumption figures are much lower than during transmission in the low bands, due to the 3GPP transmitter output power specifications.

During a 2G call, current consumption is not significantly high while receiving or in monitor bursts, and it is low in the bursts unused to transmit / receive.

Figure 5 shows an example of the module current consumption profile versus time in 2G single-slot.

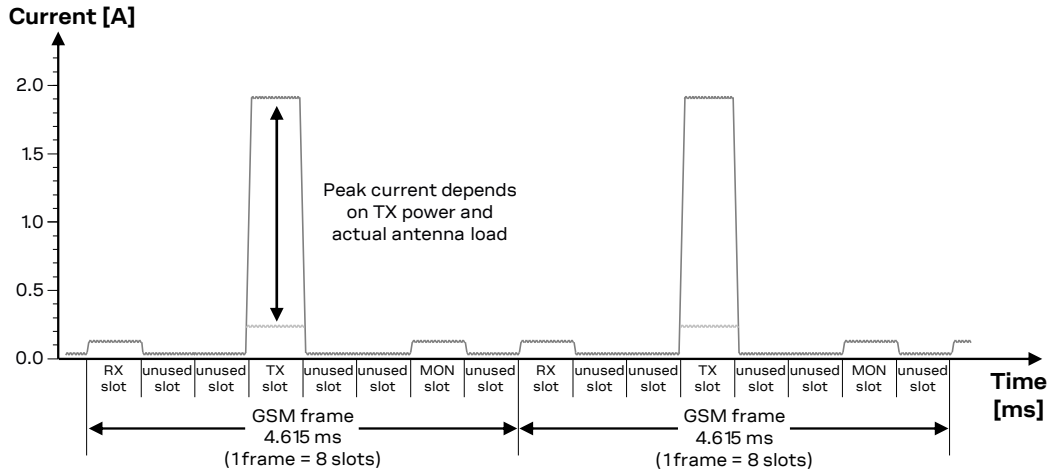

Figure 5: VCC current consumption profile versus time during a GSM call (1 TX slot, 1 RX slot)

Figure 6 illustrates the **VCC** voltage profile versus time during a 2G single-slot call, according to the related **VCC** current consumption profile described in Figure 5.

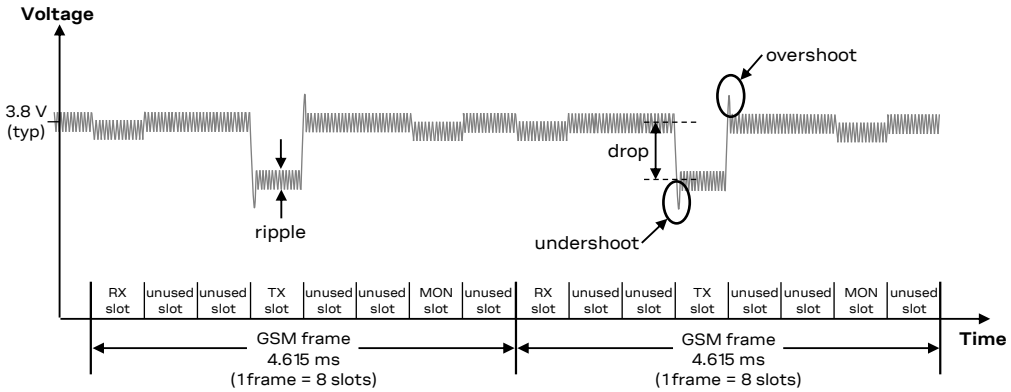

Figure 6: VCC voltage profile versus time during a 2G single-slot call (1 TX slot, 1 RX slot)

When a GPRS connection is established, more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on network conditions, which set the peak current consumption. But according to GPRS specifications, the maximum transmitted RF power is reduced if more than one slot is used to transmit, so the maximum peak of current is not as high as it can be in the case of a GSM call.

If the module transmits in GPRS multi-slot class 12, in 850 or 900 MHz bands, at maximum RF power level, the consumption can reach a quite a high peak but lower than the one achievable in 2G single-slot mode. This happens for 2.308 ms (width of the 4 Tx slots/bursts) in the case of multi-slot class 12, with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/2 duty cycle, according to GSM TDMA.

If the module is in GPRS connected mode in the 1800 or 1900 MHz bands, consumption figures are lower than in the 850 or 900 MHz band because of the 3GPP Tx power specifications.

Figure 7 illustrates the current consumption profiles in GPRS connected mode, in 850 or 900 MHz bands, with 4 slots used to transmit and 1 slot used to receive, as for the GPRS multi-slot class 12.

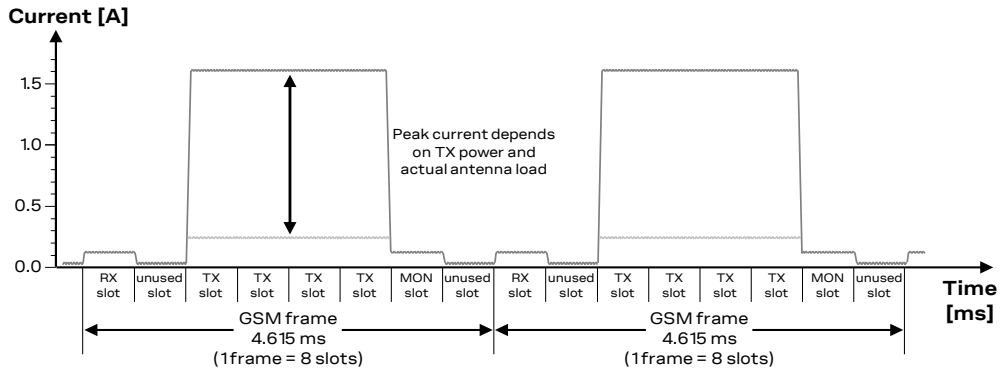

Figure 7: VCC current consumption profile versus time during a GPRS multi-slot class 12 connection (4 TX slots, 1 RX slot)

In case of EGPRS (i.e. EDGE) connections, the VCC current consumption profile is similar to that during GPRS connections: the current consumption profile in GPRS multi-slot class 12 connected mode illustrated in Figure 7 is representative for the EDGE multi-slot class 12 connected mode.

1.5.1.4 VCC current consumption in ultra-low power deep-sleep mode

The UE power saving mode (PSM) defined in 3GPP Rel.13 is by default disabled, but can be enabled by AT+CPSMS command (see the AT commands manual [2] and the application development guide [3]). When PSM is enabled, the module automatically enters the PSM and the ultra-low power deep-sleep mode whenever possible.

LEXI-R422 modules may automatically enter the ultra-low power deep-sleep mode in-between eDRX cycles, whenever possible, if the functionality is enabled by the +UPSMVER AT command, see the AT commands manual [2] and the application development guide [3].

In ultra-low power deep-sleep mode, the current consumption is reduced down to a steady value in the µA range: only the RTC runs with internal reference clock frequency.

See detailed current consumption values in the LEXI-R422 data sheet [1].

☞ Due to RTC running during PSM mode, the Cal-RC turns on the crystal every ~10 s to calibrate the RC oscillator, as a consequence, a very low spike in current consumption will be observed.

Figure 8 shows VCC current consumption profile in ultra-low power deep-sleep mode, with PSM enabled (AT+CPSMS ≠ 0). The module is registered to the network and is in ultra-low power deep-sleep mode, with no concurrent activities on. It does not periodically wake up for paging block reception, but wakes up upon the expiration of the periodic update timer set by the network, or due to proper toggling of the **PWR_CTRL** input line.

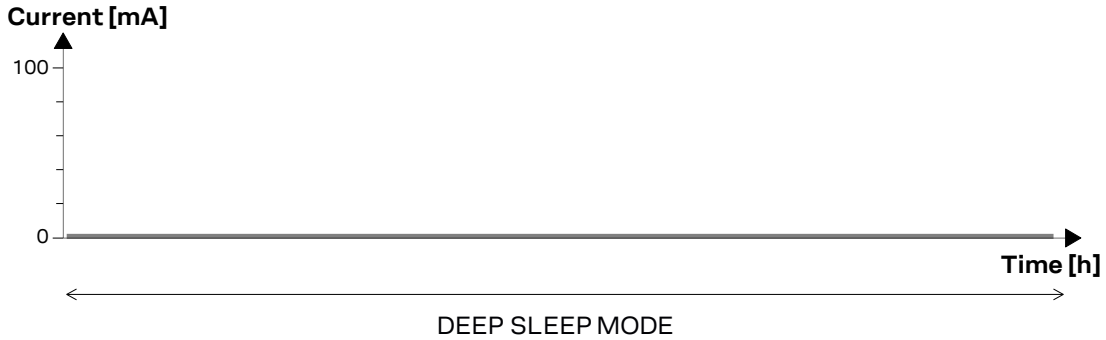

Figure 8: Example of VCC current consumption profile in ultra-low power deep-sleep mode with PSM (AT+CPSMS≠0)

1.5.1.5 VCC current consumption in low power idle mode

The low power idle mode configuration is by default disabled, but it can be enabled using the +UPSV AT command (see the AT commands manual [2]).

When low power idle mode is enabled, the module automatically enters the low power mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to the 2G / LTE system requirements, even if connected mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active mode to enable the reception of the paging block. In between, the module switches to low power mode. This is known as discontinuous reception (DRX) or extended discontinuous reception (eDRX).

Figure 9 illustrates an example of the module current consumption profile when low power mode configuration is enabled. The module is registered to the network. It automatically enters the low power idle mode, and periodically wakes up to active mode to monitor the paging channel for the paging block reception in discontinuous reception (DRX) mode.

See detailed current consumption values in the LEXI-R422 data sheet [1].

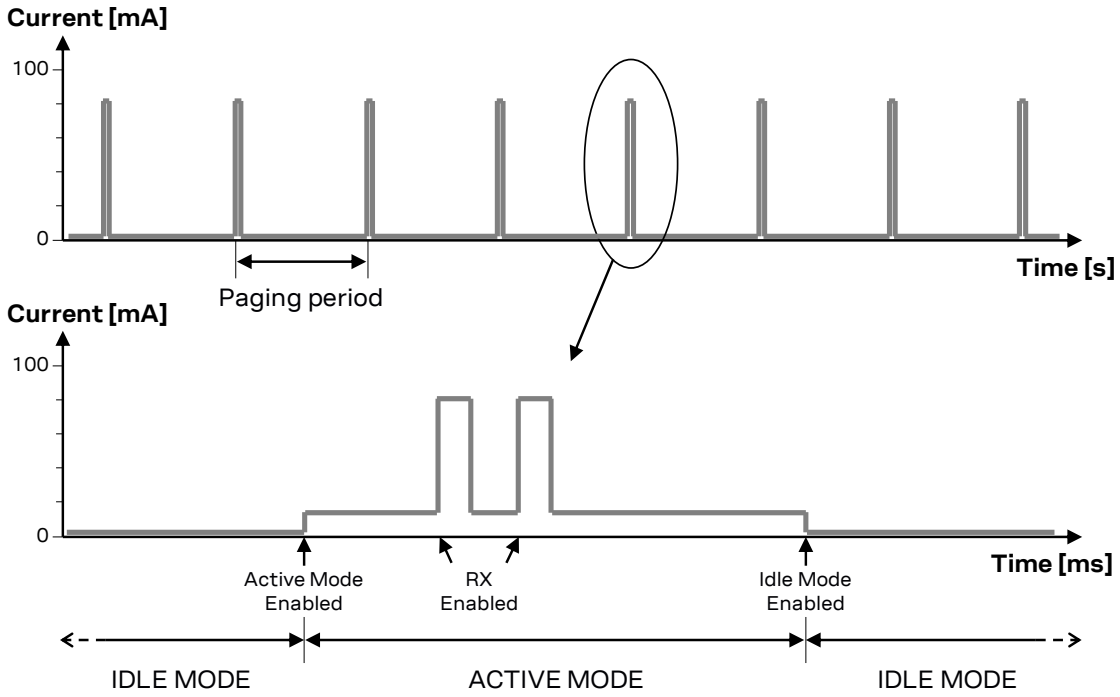

Figure 9: Example of VCC current consumption profile with low power mode enabled (AT+UPSV≠0)

1.5.1.6 VCC current consumption in active mode (PSM / low power disabled)

The active mode is the state where the module is switched on and ready to communicate with an external device by means of the application interfaces (as the USB or the UART serial interface). The module processor core is active, and the 19.2 MHz reference clock frequency is used.

If power saving mode and/or low power mode configurations are disabled, as it is by default (see the AT commands manual [2], +CPSMS, +UCPSMS, +UPSMVER, +UPSV AT commands for details), the module remains in active mode. Otherwise, if PSM mode and/or low power mode configurations are enabled, the module enters PSM mode and/or low power mode whenever possible.

Figure 10 illustrates a typical example of the module current consumption profile when the module is in active mode. The module is registered to the network. When active mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception.

Detailed current consumption values can be found in the LEXI-R422 data sheet [1].

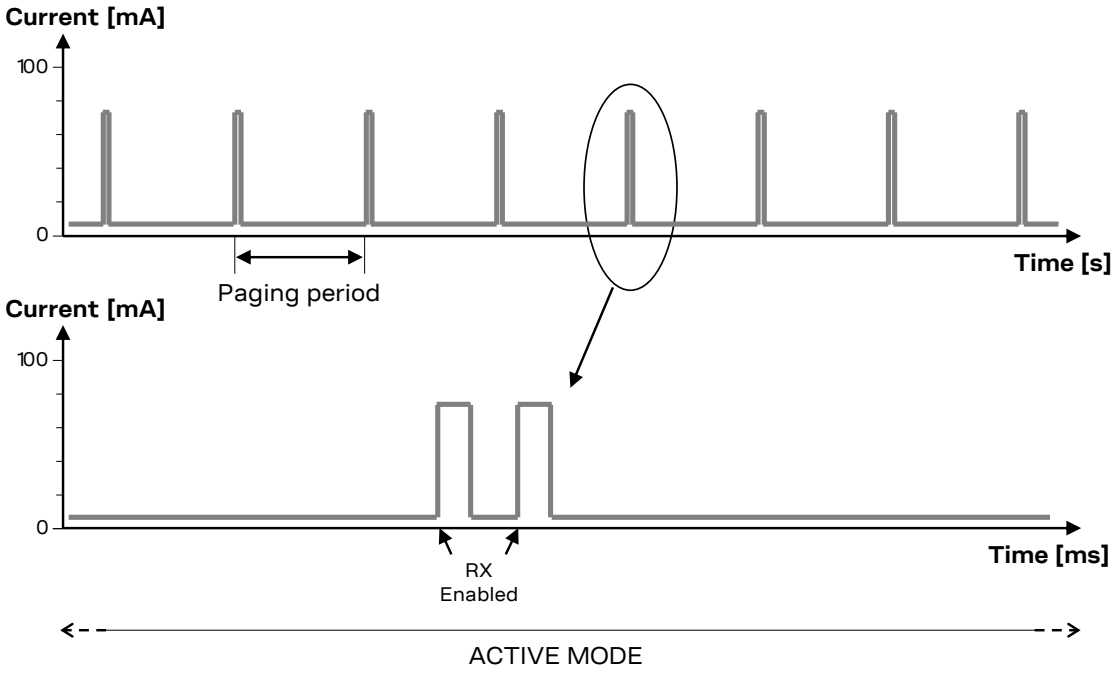

Figure 10: Example of VCC current consumption profile with low power mode disabled (AT+UPSV=0))

1.5.2 Generic digital interfaces supply output (V_INT)

The **V_INT** output pin of LEXI-R422 modules is generated by the module internal power management circuitry when the module is switched on and it is not in the deep-sleep power saving mode.

The typical operating voltage is 1.8 V, whereas the current capability is specified in the LEXI-R422 data sheet [1]. The **V_INT** voltage domain can be used in place of an external discrete regulator as a reference voltage rail for external components.

1.6 System function interfaces

1.6.1 Module power-on

When the LEXI-R422 modules are in the not-powered mode (i.e. the **VCC** module supply is not applied), they can be switched on as follows:

- Rising edge on the **VCC** input pins to a valid voltage level, and then a low logic level needs to be set at the **PWR_CTRL** input pin for a valid time

When the LEXI-R422 modules are in the power-off mode (i.e. switched off) or in the Power Saving Mode (PSM), with a valid **VCC** supply applied, they can be switched on as follows:

- Low pulse on the **PWR_CTRL** pin for a valid time period

The **PWR_CTRL** input pin is equipped with an internal active pull-up resistor. Detailed characteristics with voltages and timings are described in the LEXI-R422 data sheet [1].

Figure 11 shows the module switch-on sequence from the not-powered mode, with following phases:

- The external power supply is applied to the **VCC** module pins.
- The **PWR_CTRL** pin is held low for a valid time.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The internal reset signal is held low: the baseband core and all digital pins are held in reset state.
- When the internal reset signal is released, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- The module is ready to operate after all interfaces are configured.

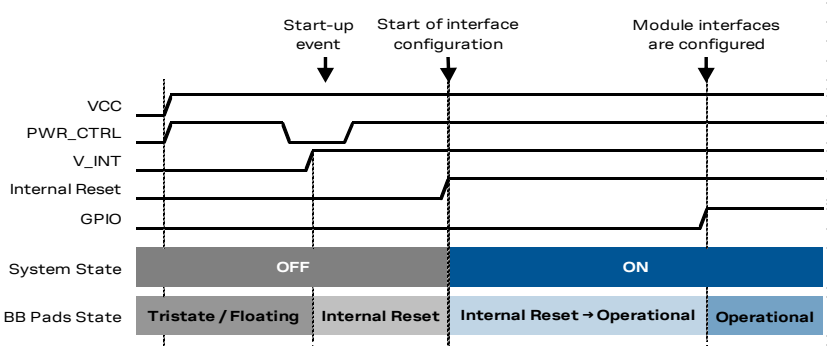

Figure 11: LEXI-R422 switch-on sequence description

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor:
- the **V_INT** pin, to sense the start of the LEXI-R422 module switch-on sequence
- the **GPIO** pin configured to provide the module operating status indication (see AT commands manual [2], +UGPIOC AT command), to sense when the module is ready to operate

☞ Before the switch-on of the generic digital interface supply (**V_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the module.

☞ Before the LEXI-R422 module is ready to operate, the host application processor should not send any AT command over AT communication interfaces of the module.

☞ The duration of the LEXI-R422 modules switch-on routine can largely vary depending on the application / network settings and the concurrent module activities.

⚠ An abrupt removal of the **VCC** supply, or forcing an abrupt emergency reset by asserting the **PWR_CTRL** input, once the boot of LEXI-R422 modules has been triggered may lead to an unrecoverable faulty state!

1.6.2 Module power-off

The graceful power-off procedure, with storage of current parameter settings in module's non-volatile memory and performing a clean network detach, can be triggered by:

- AT+CPWROFF command (see AT commands manual [2])
- Low pulse on the **PWR_CTRL** pin for a valid time period (for detailed characteristics, see LEXI-R422 data sheet [1])

☞ The graceful shutdown must be started as indicated above, and then a proper **VCC** supply must be held at least until the end of the modules' internal switch-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

A faster emergency power-off procedure of LEXI-R422, with storage of current parameter settings in the non-volatile memory of the module, but without proper network detach, can be triggered by:

- AT+CFUN=10 command (see AT commands manual [2])
- Forcing a rising edge at the GPIO input pin configured with the faster power-off function (see section 1.10, faster power-off)

The fastest memory-safe emergency power-off procedure of LEXI-R422, inhibiting further operations in the module's non-volatile flash memory, without executing the storage of the current parameter settings, and without executing a clean network detach, can be triggered by:

- AT+CFUN=11 command (see AT commands manual [2])
- Forcing a rising edge at the GPIO input pin configured with the memory-safe power-off function (see section 1.10, memory-safe power-off)

☞ The graceful shutdown procedure must be preferred to any emergency power-off procedures, which shall be used for emergency only.

An abrupt under-voltage shutdown occurs on LEXI-R422 when the **VCC** voltage supply is removed, dropping below the under-voltage shutdown threshold. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform the clean network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during LEXI-R422 modules normal operations.

☞ If an abrupt power removal is unavoidable, it is recommended to apply a rising edge to the GPIO pin configured with the memory-safe power-off function as soon as the power failure in the supply source is detected, placing a low-ESR 470 mF capacitor at the **VCC** supply input to let the module complete the memory-safe emergency power-off.

⚠ An abrupt removal of the **VCC** supply during LEXI-R422 modules normal operations may lead to an unrecoverable faulty state!

LEXI-R422 modules automatically switch off, with storage of the current parameter settings in the module's internal non-volatile memory and a clean network detach, after having sent the last gasp, once the feature is enabled and triggered (see the AT commands manual [2], +ULGASP AT command).

Figure 12 and Figure 13 show the LEXI-R422 modules switch-off sequence started by means of the AT+CPWROFF command and by the **PWR_CTRL** input pin respectively, allowing storage of current parameter settings in the module's non-volatile memory and a clean network detach, with the following phases:

- When the +CPWROFF AT command is sent, or when a low pulse is applied at the **PWR_CTRL** input pin with appropriate time duration (see the LEXI-R422 data sheet [1]), the module starts the switch-off routine.
- Then, if the +CPWROFF AT command has been sent, the module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in switch-off mode as long as a switch on event does not occur (e.g. applying a low level to **PWR_CTRL** input pin), and it enters not-powered mode if the **VCC** supply is removed.

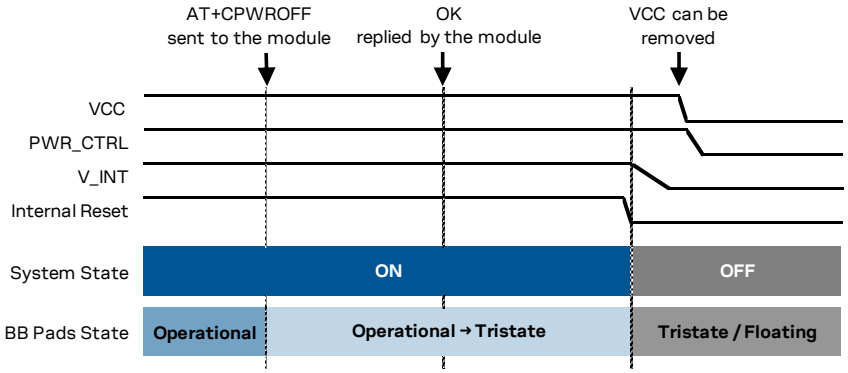

Figure 12: LEXI-R422 modules switch-off sequence by means of AT+CPWROFF command

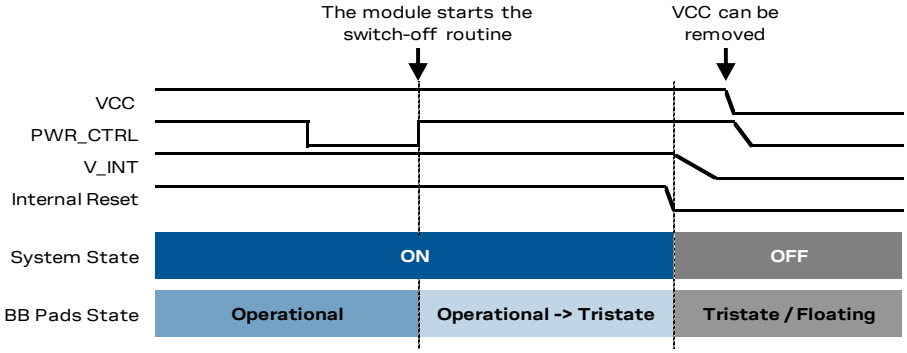

Figure 13: LEXI-R422 modules switch-off sequence by means of PWR_CTRL pin

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor the **V_INT** pin to sense the end of the switch-off sequence.

⚠ **VCC** supply can be removed only after **V_INT** goes low: an abrupt removal of the **VCC** supply during LEXI-R422 modules normal operations may lead to an unrecoverable faulty state!

☞ The duration of each phase in the LEXI-R422 modules switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

LEXI-R422 modules can be cleanly reset (rebooted) by:

- AT+CFUN=16 command (see the AT commands manual [2])

In the case above an “internal” or “software” reset of the module is executed: the current parameter settings are saved in the module’s non-volatile memory and a clean network detach is performed.

An abrupt hardware reset (reboot) occurs on the LEXI-R422 modules when a low level is applied on **PWR_CTRL** input pin for a long time period (see the LEXI-R422 data sheet [1]). In this case, the current parameter settings are not saved in the module’s non-volatile memory and a clean network detach is not performed.

☞ It is highly recommended to avoid an abrupt hardware reset (reboot) of the module by forcing a low level for a long time period on the **PWR_CTRL** input pin during modules normal operation: the abrupt hardware reset (reboot) should be performed only if reset or shutdown via AT commands fails or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the AT commands manual [2].

⚠ Forcing an abrupt hardware reset (reboot) during LEXI-R422 modules normal operations may lead to an unrecoverable faulty state!

The **PWR_CTRL** input pin is directly connected to the power management unit IC, with an integrated pull-up to an internal supply domain, in order to perform an abrupt hardware reset when asserted for a specific time period. Detailed electrical characteristics with voltages and timings are described in the LEXI-R422 data sheet [1].

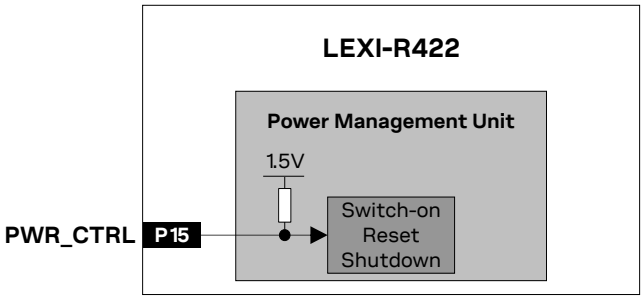

Figure 14: PWR_CTRL input pin description

1.7 Antenna interfaces

1.7.1 Cellular antenna RF interface (ANT)

LEXI-R422 modules provide an RF interface for connecting the external cellular antenna. The **ANT** pin represents the primary RF input/output for transmission and reception of cellular RF signals.

The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the cellular Tx / Rx antenna system through a 50 Ω transmission line to allow clear RF transmission and reception.

1.7.1.1 Cellular antenna RF interface requirements

Table 7 summarizes the requirements for the antenna RF interface. See section 2.4.1.4 for suggestions to correctly design antennas circuits compliant with these requirements.

⚠ The antenna circuits affect the RF compliance of the device integrating LEXI-R422 modules with applicable required certification schemes (for more details see section 4). RF performance is optimized by fulfilling the cellular antenna RF interface requirements summarized in Table 7.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** port.
Frequency range	See the LEXI-R422 data sheet [1]	The required frequency range of the antenna connected to **ANT** port depends on the operating bands of the used cellular module and the used mobile network.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT** port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits. For additional info see section 4.
Input power	> 33 dBm (> 2.0 W)	The antenna connected to the **ANT** port must support with adequate margin the maximum power transmitted by the modules.

Table 7: Tx/Rx antenna RF interface requirements

1.7.2 Antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an Analog to Digital Converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the AT commands manual [2] for more details on this feature.

The **ANT_DET** pin generates a DC current (for detailed characteristics see the LEXI-R422 data sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.3 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM interface

LEXI-R422 modules provide a SIM interface on the **VSIM**, **SIM_IO**, **SIM_CLK**, **SIM_RST** pins to connect an external SIM card or UICC chip.

LEXI-R422 modules support only the 1.8 V type of SIM / UICC.

1.8.2 SIM detection interface

The **GPIO6** pin is configured as an external interrupt to detect the SIM card mechanical / physical presence. The pin is configured as input with an internal active pull-down enabled, and it can sense SIM card presence only if cleanly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **GPIO6** input pin is recognized as SIM card not present
- High logic level at **GPIO6** input pin is recognized as SIM card present

For more details, see the AT commands manual [2], +UGPIOC, +CIND and +CMER AT commands.

1.9 Data communication interfaces

LEXI-R422 modules provide the following serial communication interfaces:

- UART interfaces: asynchronous serial interface supporting AT commands, data communication, GNSS tunneling, FW update by means of FOAT. See section 1.9.1.
- USB interface: High-Speed USB 2.0 compliant serial interface supporting FW update by means of the u-blox EasyFlash tool and diagnostic trace logging. See section 1.9.2.
- I2C interface: I2C bus compatible interface supporting communication with external u-blox GNSS positioning chips or modules and with external I2C devices. See section 1.9.3.

1.9.1 UART interfaces

1.9.1.1 UART features

LEXI-R422 modules include a primary UART interface (UART) for communication with an application host processor, supporting AT commands, data communication, multiplexer protocol functionality (see 1.9.1.3), and FW update by means of FOAT, with settings configurable by dedicated AT commands (for more details, see the AT commands manual [2]):

- 8-wire serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [5], with CMOS compatible signal levels (0 V for low data bit / ON state, 1.8 V for high data bit / OFF state)
  - Data lines (**RXD** as data output, **TXD** as data input)
  - HW flow control lines (**CTS** as flow control output, **RTS** as flow control input)
  - Modem status and control lines (**DTR** input, **DSR** output, **DCD** output, **RI** output)[2]

☞ UART signal names of LEXI-R422 modules conform to the ITU-T V.24 [5]: e.g. **TXD** line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

LEXI-R422 modules include an auxiliary UART interface (UART AUX) for communication with an host processor, supporting AT commands, data, GNSS tunneling, FW update by means of FOAT, with settings configurable by dedicated AT commands (for details, see the AT commands manual [2]):

- 4-wire serial port with RS-232 functionality conforming to ITU-T V.24 recommendation [5], with CMOS compatible signal levels (0 V for low data bit / ON state, 1.8 V for high data bit / OFF state)
  - Data lines (**DCD** as data output, **DTR** as data input)
  - HW flow control lines (**RI** as flow control output, **DSR** as flow control input)

LEXI-R422 modules UART interface is by default configured in AT command mode: the module waits for AT command instructions and interprets all the characters received as commands to execute. The functionalities supported by the modules can be in general set and configured by AT commands:

- AT commands according to 3GPP TS 27.007 [6], 3GPP TS 27.005 [7], 3GPP TS 27.010 [8]
- u-blox AT commands (see the AT commands manual [2])

The default baud rate is 115200 b/s. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit: see Figure 15). Baud rates can be configured by AT command (see the AT commands manual [2]).

☞ Automatic baud rate detection and automatic frame format recognition are not supported.

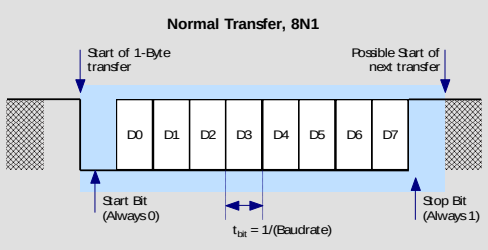

Figure 15: UART 8N1 frame format (8 data bits, no parity, 1 stop bit)

1.9.1.2 UART signals behavior

At the end of the module boot sequence (see Figure 11), the module is by default in active mode, and the UART interface is initialized and enabled as AT commands interface.

[2] **DTR**, **DSR**, **DCD** and **RI** pins can be alternatively configured, in mutually exclusive way, as auxiliary UART interface (UART AUX).

The configuration and behavior of the UART signals after the boot sequence are described below:

- The module data output line (**RXD**) is set by default to the OFF state (high level) at UART initialization. The module holds **RXD** in the OFF state until the module transmits some data.
- The module data input line (**TXD**) is assumed to be controlled by the external host once UART is initialized. The **TXD** data input line has an internal active pull-up enabled.

1.9.1.3 UART multiplexer protocol

LEXI-R422 modules include multiplexer functionality as per 3GPP TS 27.010 [8], on the primary UART physical link. This is a data link protocol which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the primary UART physical link. The following virtual channels are defined:

- Channel 0: for multiplexer control.
- Channel 1: for all AT commands, and non-Dial Up Network (non-DUN) data connections. UDP, TCP data socket / data call connections via relevant AT commands.
- Channel 2: for Dial Up Network (DUN) data connection. It requires the host to have and use its own TCP/IP stack. The DUN can be initiated on modem side or terminal/host side.
- Channel 3: for u-blox GNSS data tunneling.

1.9.2 USB interface

1.9.2.1 USB features

LEXI-R422 modules include a high-speed USB 2.0 interface [4], available for FW upgrade by means of the u-blox EasyFlash tool and for diagnostic purposes. The module itself acts as a USB device, and it can be connected to a USB host such as a Personal Computer equipped with compatible drivers.

LEXI-R422 modules provide the following USB lines:

- the **USB_D+** / **USB_D-** lines, carrying the USB data and signaling
- the **USB_5V0** input pin to enable the USB interface by applying an external 5.0 V typical voltage
- the **USB_3V3** input pin to supply the USB interface by applying an external 3.3 V typical voltage

☞ If the USB interface is enabled, the module does not enter the low power deep-sleep mode.

☞ It is highly recommended to provide accessible test points directly connected to the **V_INT**, **PWR_CTRL**, **USB_5V0**, **USB_3V3**, **USB_D+**, **USB_D-**, **RSVD #99** pins for FW upgrade and/or for diagnostic purpose.

1.9.3 I2C interface

LEXI-R422 modules include an I2C-bus compatible interface (**SDA**, **SCL** lines) to communicate with an external u-blox GNSS receiver and with external I2C devices: the LEXI-R422 module acts as an I2C host which can communicate with I2C devices in accordance with the I2C bus specifications [9].

The **SDA** and **SCL** pins have internal pull-up to **V_INT**, so there is no need of additional pull-up resistors on the external application board.

1.10 General purpose input / output

LEXI-R422 modules include pins which can be configured as general purpose input/output or to provide custom functions via u-blox AT commands (for details, see the AT commands manual [2], +UGPIOC, +UGPIOR, +UGPIOW AT commands), as summarized in Table 8.

Function	Description	Default GPIO	Configurable GPIOs
General purpose output	Output to set the high or the low digital level	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, RFCTRL1, RFCTRL2
General purpose input	Input to sense high or low digital level	RFCTRL1, RFCTRL2	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, RFCTRL1, RFCTRL2
Network status indication	Network status: registered / data transmission, no service	--	GPIO1
External GNSS supply enable	Enable/disable the supply of a u-blox GNSS receiver connected to the cellular module by the I2C	--	GPIO2
External GNSS data ready	Sense when a u-blox GNSS receiver connected to the module is ready for sending data by the I2C	--	GPIO3
SIM card detection	SIM card physical presence detection	--	GPIO6
Module status indication	Module switched off or in PSM low power deep-sleep mode, versus active or connected mode	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Last gasp	Input to trigger last gasp notification	--	GPIO3, GPIO4, GPIO5
Faster power-off	Input with internal pull-down to trigger a faster emergency shutdown (as AT+CFUN=10) by applying a rising edge	--	GPIO3, GPIO4
Memory-safe power-off	Input with internal pull-down to trigger the fastest memory-safe emergency shutdown (as AT+CFUN=11) by applying a rising edge	--	GPIO3, GPIO4
LwM2M pulse	Output to notify a settable LwM2M event with a configurable pulse	--	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Antenna dynamic tuning	Output changing the status according to the RF band in use, to control in real time an external antenna tuning IC	--	RFCTRL1, RFCTRL2
Pin disabled	Tri-state with an internal active pull-down enabled	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6

Table 8: LEXI-R422 modules GPIO custom functions configuration

1.11 Cellular antenna dynamic tuner interface

LEXI-R422 modules include two output pins (named **RFCTRL1** and **RFCTRL2**) that can be configured, as optional feature, to control in real time an external antenna tuning IC, changing their output value dynamically according to the specific actual cellular band in use by the module. Table 9 illustrates the default factory-programmed configuration that can be changed by dedicated AT command.

RFCTRL1	RFCTRL2	LTE frequency band in use	2G frequency band in use
0	0	-	-
0	1	B12, B13, B28, B85 (700..800 MHz)	-
1	0	B5, B8, B18, B19, B20, B26 (800..900 MHz)	GSM 850, E-GSM 900 (800..900 MHz)
1	1	B1, B2, B3, B4, B25, B66 (> 1000 MHz)	DCS 1800, PCS 1900 (> 1000 MHz)

Table 9: LEXI-R422 modules antenna dynamic tuning truth table (default factory-programmed configuration)

1.12 Reserved pins (RSVD)

LEXI-R422 modules have pins reserved for future use, marked as **RSVD**, which can all be left unconnected on the application board, except for the **RSVD #99** (J5) pin which is recommended to be externally accessible by connecting it to a dedicated Test-Point.

☞ It is highly recommended to provide an accessible test point directly connected to the **RSVD #99** (J5) pin for diagnostic purposes. It is also highly recommended to provide access to the **V_INT**, **PWR_CTRL**, **USB_5V0**, **USB_3V3**, **USB_D+**, **USB_D-** pins for FW update and/or for diagnostic purposes using accessible dedicated Test-Points that are directly connected to each of these pins, or using a dedicated connector / circuit.

2 Design-in

2.1 Overview

For an optimal integration of the LEXI-R422 modules in the final application board, follow the design guidelines stated in this section.

Every application circuit must be suitably designed to ensure the correct functionality of the relative interface, but a number of points require greater attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT** and **ANT_DET** pins.
   Cellular antenna circuit directly affects the RF compliance of the device integrating a LEXI-R422 module with applicable certification schemes. Follow the suggestions provided in the relative section 2.4 for the schematic and layout design.

2. Module supply: **VCC** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a LEXI-R422 module with the applicable required certification schemes as well as the antenna circuit design. Very carefully follow the suggestions provided in the relative section 2.2.1 for the schematic and layout design.

3. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins.
   Accurate design is required to ensure SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in relative section 2.5 for schematic and layout design.

4. System functions: **PWR_CTRL** pin.
   Accurate design is required to ensure that the voltage level is well defined during operation. Carefully follow the suggestions provided in relative section 2.3 for schematic and layout design.

5. Other digital interfaces: UART, USB, I2C, GPIOs, and reserved pins.
   Accurate design is required to ensure correct functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6.1, 2.6.2, 2.6.3, 2.7 and 2.8 for the schematic and layout design.

6. Other supplies: **V_INT** generic digital interfaces supply.
   Accurate design is required to ensure correct functionality. Follow the suggestions provided in the corresponding section 2.2.2 for the schematic and layout design.

☞ It is recommended to follow the specific design guidelines provided by each manufacturer of any external part selected for the application board integrating the u-blox cellular modules.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins have to be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

LEXI-R422 modules must be sourced through the **VCC** pins with a suitable DC power supply that should meet the following prerequisites to comply with the modules **VCC** requirements summarized in Table 6.

The appropriate DC power supply can be selected according to the application requirements (see Figure 16) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

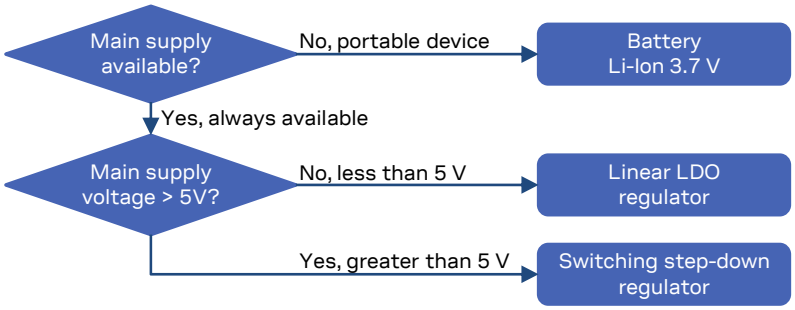

Figure 16: VCC supply concept selection

The switching step-down regulator is the typical choice when primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the operating supply voltage of LEXI-R422. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See section 2.2.1.2 for design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 5 V). In this case, the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See section 2.2.1.3 for design-in.

If LEXI-R422 modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.5, 2.2.1.6 and 2.2.1.7 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit, which is not included in the modules. The charger circuit needs to be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements. A DC/DC switching charger is the typical choice when the charging source has a high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a suitable charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.6 and 2.2.1.7 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected considering the maximum current specified in the LEXI-R422 data sheet [1] during connected mode, considering that primary cells might have weak power capability. See section 2.2.1.5 for specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The selected regulator or battery must be able to support with adequate margin the highest averaged current consumption value specified in the LEXI-R422 data sheet [1].

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 6.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail source to the **VCC** value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during transmissions at the maximum power, as specified in the LEXI-R422 data sheet [1].
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications it is recommended to select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** profile and therefore negatively impact modulation spectrum performance.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce noise on **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the active mode to connected mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 17 and the components listed in Table 10 show an example of a high reliability power supply circuit for the LEXI-R422 modules, where the module VCC input is supplied by a step-down switching regulator capable of delivering the highest peak / pulse current specified for the 2G use-case, with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

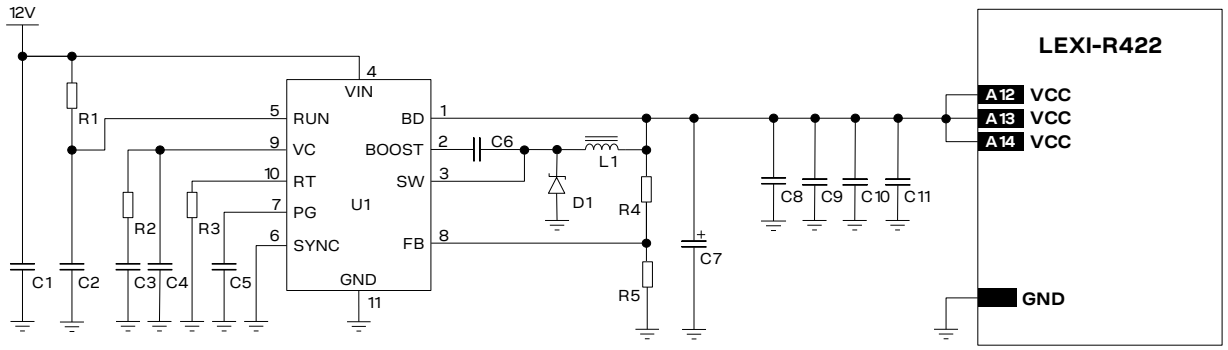

Figure 17: Example of high reliability VCC supply circuit for LEXI-R422 modules, using a step-down regulator

Reference	Description	Part number - Manufacturer
C1	10 µF capacitor ceramic X7R 5750 15% 50 V	Generic manufacturer
C2	10 nF capacitor ceramic X7R 0402 10% 16 V	Generic manufacturer
C3	680 pF capacitor ceramic X7R 0402 10% 16 V	Generic manufacturer
C4	22 pF capacitor ceramic C0G 0402 5% 25 V	Generic manufacturer
C5	10 nF capacitor ceramic X7R 0402 10% 16 V	Generic manufacturer
C6	470 nF capacitor ceramic X7R 0603 10% 25 V	Generic manufacturer
C7	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C8	100 nF capacitor ceramic X7R 16 V	GRM155R71C104KA01 - Murata
C9	10 nF capacitor ceramic X7R 16 V	GRM155R71C103KA01 - Murata
C10	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E680JA01 - Murata
C11	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E150JA01 - Murata
D1	Schottky diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	15 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	22 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R4	390 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
R5	100 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1	Step-down regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 10: Components for high reliability VCC supply circuit for LEXI-R422 modules, using a step-down regulator

☞ See the section 2.2.1.10, and in particular Figure 26 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

Figure 18 and the components listed in Table 11 show an example of a low cost power supply circuit suitable for the LEXI-R422 modules, where the module **VCC** is supplied by a step-down switching regulator capable of delivering the highest peak / pulse current specified for the 2G use-case, transforming a 12 V supply input.

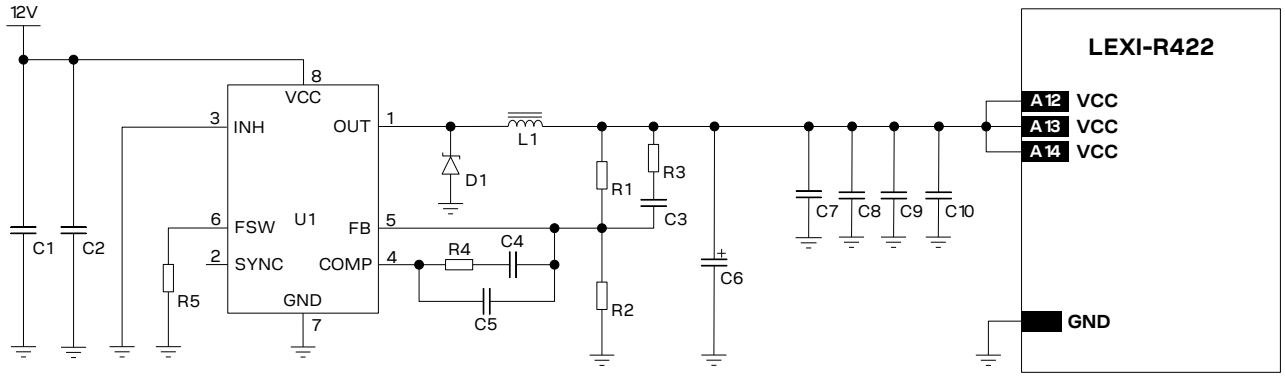

Figure 18: Example of low cost VCC supply circuit for LEXI-R422 modules, using a step-down regulator

Reference	Description	Part number - Manufacturer
C1	22 µF capacitor ceramic X5R 1210 10% 25 V	Generic manufacturer
C2	220 nF capacitor ceramic X7R 0603 10% 25 V	Generic manufacturer
C3	5.6 nF capacitor ceramic X7R 0402 10% 50 V	Generic manufacturer
C4	6.8 nF capacitor ceramic X7R 0402 10% 50 V	Generic manufacturer
C5	56 pF capacitor ceramic C0G 0402 5% 50 V	Generic manufacturer
C6	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C7	100 nF capacitor ceramic X7R 16 V	GRM155R71C104KA01 - Murata
C8	10 nF capacitor ceramic X7R 16 V	GRM155R71C103KA01 - Murata
C9	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E680JA01 - Murata
C10	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E150JA01 - Murata
D1	Schottky diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 µH inductor 30% 5.28A 22 mΩ	MSS1038-522NL – Coilcraft
R1	4.7 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
R2	910 Ω resistor 0402 1% 0.063 W	Generic manufacturer
R3	82 Ω resistor 0402 5% 0.063 W	Generic manufacturer
R4	8.2 kΩ resistor 0402 5% 0.063 W	Generic manufacturer
R5	39 kΩ resistor 0402 5% 0.063 W	Generic manufacturer
U1	Step-down regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 11: Suggested components for low cost VCC circuit for LEXI-R422 modules, using a step-down regulator

☞ See the section 2.2.1.10, and in particular Figure 26 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.3 Guidelines for VCC supply circuit design using LDO linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail source and the **VCC** value is low. The linear regulators provide high efficiency when transforming a 5 V DC supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during a transmission at the maximum Tx power, as specified in the LEXI-R422 data sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the rated range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 19 and the components listed in Table 12 show an example of a high reliability power supply circuit for LEXI-R422 modules, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the highest peak / pulse current specified for the 2G use-case, with an appropriate power handling capability. The regulator described in this example supports a wide input voltage range, and it includes internal circuitry for reverse battery protection, current limiting, thermal limiting and reverse current protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

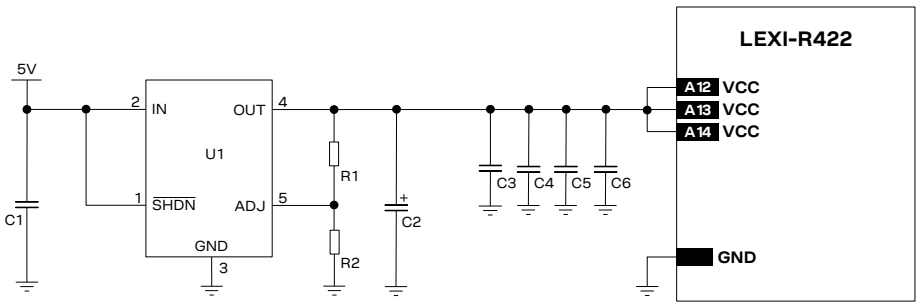

Figure 19: Example of high reliability VCC supply circuit for LEXI-R422 modules, using an LDO linear regulator

Reference	Description	Part number - Manufacturer
C1	10 µF capacitor ceramic X5R 0603 20% 6.3 V	Generic manufacturer
C2	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	100 nF capacitor ceramic X7R 16 V	GRM155R71C104KA01 - Murata
C4	10 nF capacitor ceramic X7R 16 V	GRM155R71C103KA01 - Murata
C5	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E680JA01 - Murata
C6	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E150JA01 - Murata
R1	9.1 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	3.9 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1	LDO linear regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 12: Suggested components for high reliability VCC circuit for LEXI-R422 modules, using an LDO regulator

☞ See the section 2.2.1.10, and in particular Figure 26 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

Figure 20 and the components listed in Table 13 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified highest peak / pulse current, with an appropriate power handling capability. The regulator described in this example supports a limited input voltage range and it includes internal circuitry for current and thermal protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module VCC normal operating range (e.g. ~4.1 V). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

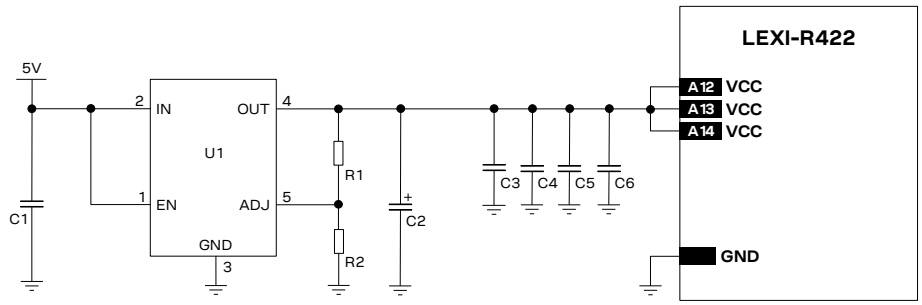

Figure 20: Example of low cost VCC supply circuit for LEXI-R422 modules, using an LDO linear regulator

Reference	Description	Part number - Manufacturer
C1	10 µF capacitor ceramic X5R 0603 20% 6.3 V	Generic manufacturer
C2	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	100 nF capacitor ceramic X7R 16 V	GRM155R71C104KA01 - Murata
C4	10 nF capacitor ceramic X7R 16 V	GRM155R71C103KA01 - Murata
C5	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E680JA01 - Murata
C6	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1E150JA01 - Murata
R1	27 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	4.7 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1	LDO linear regulator ADJ 3.0 A	LP38501ATJ-ADJ/NOPB - Texas Instrument

Table 13: Suggested components for low cost VCC supply circuit for LEXI-R422 modules, using an LDO linear regulator

☞ See the section 2.2.1.10, and in particular Figure 26 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current occurring during a transmission at maximum Tx power, as specified in the LEXI-R422 data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 6 during transmit bursts.

2.2.1.5 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current consumption occurring during a transmission at maximum Tx power, as specified in LEXI-R422 data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 6 during transmit bursts.

2.2.1.6 Guidelines for external battery charging circuit

LEXI-R422 modules do not have an on-board charging circuit. Figure 21 provides an example of a battery charger design, suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features the correct pulse and DC discharge current capabilities and the appropriate DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the battery charger IC, which from a USB power source (5.0 V typ.), linearly charges the battery in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage, the battery charger IC starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor or when the charging timer reaches the factory set value.

Using a battery pack with an internal NTC resistor, the battery charger IC can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The battery charger IC, as linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see section 2.2.1.7 for the specific design-in).

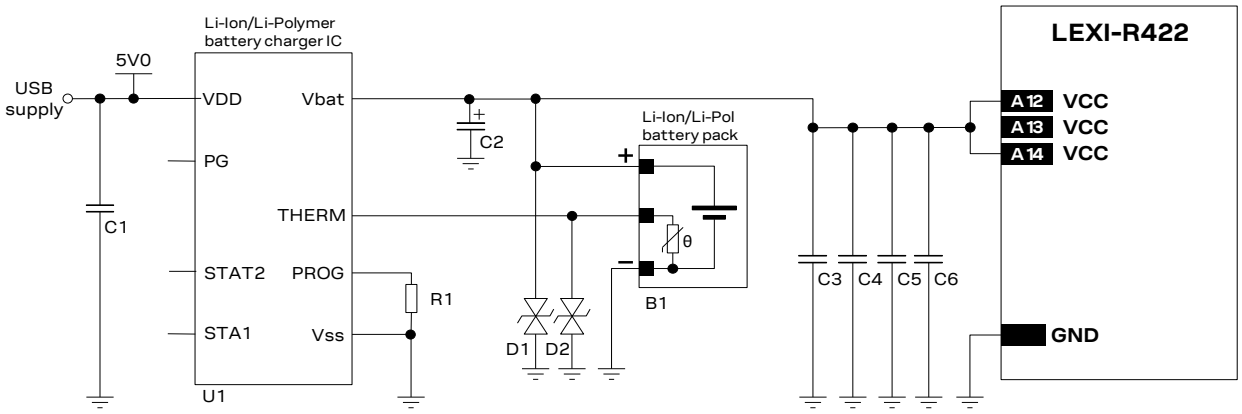

Figure 21: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Generic manufacturer
C1	1 µF capacitor ceramic X7R 16 V	Generic manufacturer
C2	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C4	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C5	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G - Bourns
R1	10 kΩ resistor 0.1 W	Generic manufacturer
U1	Single cell Li-Ion (or Li-Polymer) battery charger IC	MCP73833 - Microchip

Table 14: Suggested components for the Li-Ion (or Li-Polymer) battery charging application circuit

☞ See the section 2.2.1.10, and in particular Figure 26 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.7 Guidelines for external charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as a possible supply source, should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 22 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator, which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system. The power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- High efficiency internal step down converter, with characteristics as indicated in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

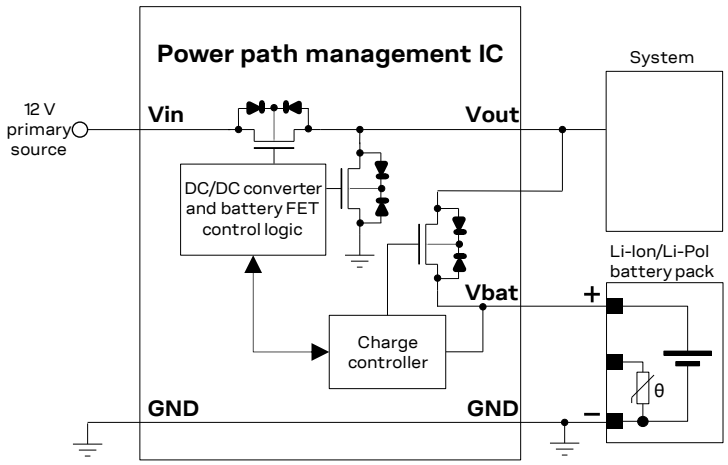

Figure 22: Charger / regulator with integrated power path management circuit block diagram

Figure 23 and the parts listed in Table 15 provide an application circuit example where the MPS MP2617H switching charger / regulator with integrated power path management function provides the supply to the cellular module. At the same time it also concurrently and autonomously charges a suitable Li-Ion (or Li-Polymer) battery with the correct pulse and DC discharge current capabilities and the appropriate DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617H IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617H IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor.

Using a battery pack with an internal NTC resistor, the MP2617H can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: suitable resistors or capacitors must be accordingly connected to the related pins of the IC.

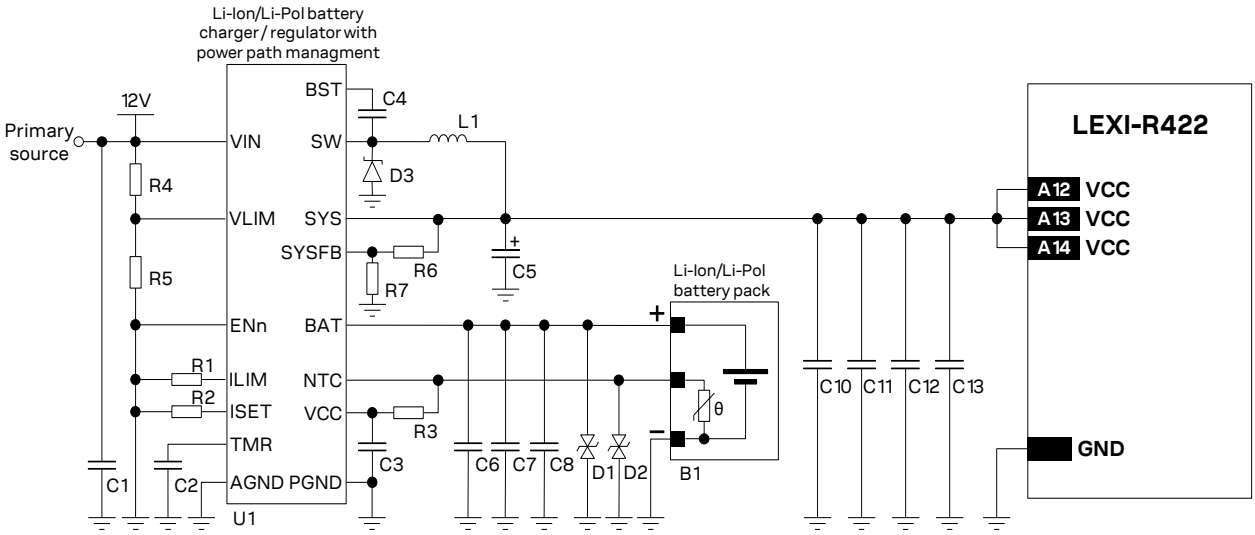

Figure 23: Li-Ion (or Li-Polymer) battery charging and power path management application circuit

Reference	Description	Part number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 10 kΩ NTC	Generic manufacturer
C1, C6	22 µF capacitor ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2, C4, C10	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	1 µF capacitor ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C5	330 µF capacitor tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7, C12	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C8, C13	15 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C11	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G - Bourns
D3	Schottky diode 40 V 3 A	MBRA340T3G - ON Semiconductor
R1, R3, R5, R7	10 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R2	1.05 kΩ resistor 0402 1% 0.1 W	Generic manufacturer
R4	22 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R6	26.5 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
L1	2.2 µH inductor 7.4 A 13 mΩ 20%	SRN8040-2R2Y - Bourns
U1	Li-Ion/Li-Polymer battery DC/DC charger / regulator with integrated power path management function	MP2617H - Monolithic Power Systems (MPS)

Table 15: Suggested components for battery charging and power path management application circuit

☞ See the section 2.2.1.10, and in particular Figure 26 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.8 Guidelines for particular VCC supply circuit design

LEXI-R422 modules, supporting 2G radio access technology, have separate supply inputs over the **VCC** pins (see Figure 3):

- **VCC** pins A13 and A14: supply input for the internal RF power amplifier, demanding most of the total current drawn of the module when RF transmission is enabled during a call.
- **VCC** pin A12: supply input for the internal power management unit, baseband and transceiver parts, demanding minor current.

Generally, all the **VCC** pins are intended to be connected to the same external power supply circuit, but separate supply sources can be implemented for very specific applications, as for example for applications using a battery with poor discharge current capability or with significative voltage drop at the battery output upon current drawn. The voltage at the VCC pins A13 and A14 can drop to a value lower than the one at the VCC pin A12, keeping the module still switched-on and functional. Figure 24 illustrates a possible application circuit.

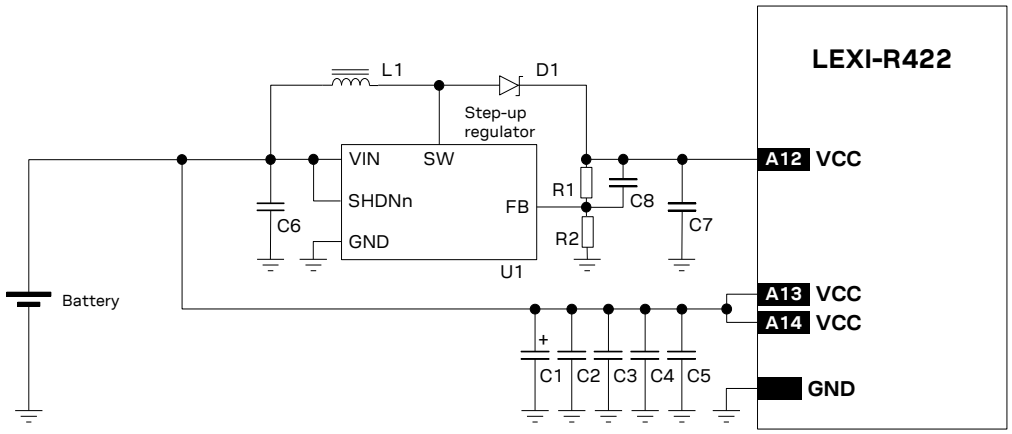

Figure 24: VCC circuit example with separate supply for LEXI-R422 modules

Reference	Description	Part number - Manufacturer
C1	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	56 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C5	15 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C6	10 µF capacitor ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C7	22 µF capacitor ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	10 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E100JA01 - Murata
D1	Schottky diode 40 V 1 A	SS14 - Vishay General Semiconductor
L1	10 µH inductor 20% 1 A 276 mΩ	SRN3015-100M - Bourns Inc.
R1	1 MΩ resistor 0402 5% 0.063 W	Generic manufacturer
R2	412 kΩ resistor 0402 5% 0.063 W	Generic manufacturer
U1	Step-up regulator 350 mA	AP3015 - Diodes Incorporated

Table 16: Examples of parts for the VCC circuit with separate supply for LEXI-R422 modules

☞ See the section 2.2.1.10, and in particular Figure 26 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.9 Guidelines for removing VCC supply

The current consumption of LEXI-R422 modules is extremely low when the modules are switched off or when the modules are in deep-sleep Power Saving Mode (see LEXI-R422 data sheet [1] for module current consumption figures), and therefore removing the **VCC** power is in general not strictly needed, but it may be useful to further minimize the current consumption when the LEXI-R422 modules are switched off.

The **VCC** supply source can be removed using an appropriate low-leakage load switch or p-channel MOSFET controlled by the application processor as shown in Figure 25, given that the external switch has provided:

- Ultra-low leakage current (for example, less than 1 µA), to minimize the current consumption
- Very low $R_{DS(ON)}$ series resistance (for example, less than 50 mΩ), to minimize voltage drops
- Adequate maximum drain current (see LEXI-R422 data sheet [1] for module current consumption figures)

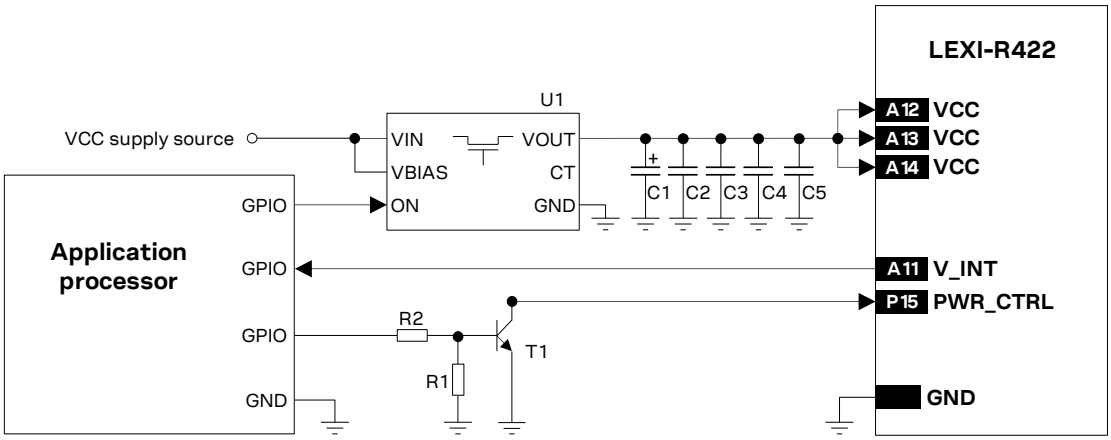

Figure 25: Example of application circuit for VCC supply removal

Reference	Description	Part number - Manufacturer
C1	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C2	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C4	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C5	15 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
R1, R3	47 kΩ resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	10 kΩ resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
T1	NPN BJT transistor	BC847 - Infineon
U1	Ultra-low resistance load switch	TPS22967 - Texas Instruments

Table 17: Components for VCC supply removal application circuit

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during LEXI-R422 normal operations: the **VCC** supply can be removed only after **V_INT** goes low, indicating that the module has entered deep-sleep Power Saving Mode or power-off mode.

☞ See the section 2.2.1.10, and in particular Figure 26 / Table 18, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.10 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the supply lines (connected to the modules **VCC** and **GND** pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize losses.

Three pins are allocated to **VCC** supply connection. Several pins are designated for **GND** connection. It is recommended to correctly connect all of them to supply the module minimizing series resistance.

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 68 pF capacitor with self-resonant frequency in the 800/900 MHz range (e.g. Murata GRM1555C1H680J), to filter EMI in the low cellular frequency bands
- 15 pF capacitor with self-resonant frequency in the 1800/1900 MHz range (as Murata GRM1555C1H150J), to filter EMI in the high cellular frequency bands
- 10 nF capacitor (e.g. Murata GRM155R71C103K), to filter digital logic noise from clocks and data
- 100 nF capacitor (e.g. Murata GRM155R61C104K), to filter digital logic noise from clocks and data

An additional capacitor is recommended to avoid undershoot and overshoot at the start and at the end of RF transmission:

- 100 µF low ESR capacitor (e.g Kemet T520B107M006ATE015)

An additional series ferrite bead is recommended for additional RF noise filtering, in particular if the application device integrates an internal antenna:

- Ferrite bead specifically designed for EMI suppression in GHz band (as Murata BLM18EG221SN1), placed as close as possible to the **VCC** pins of the module, implementing the circuit described in Figure 26, to filter out EMI in all the cellular bands

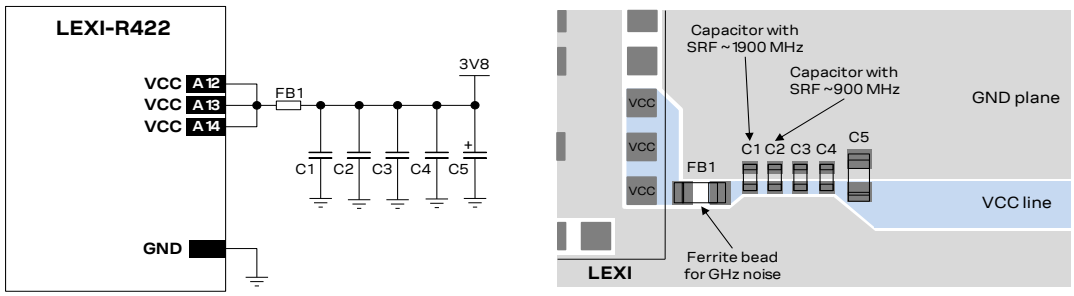

Figure 26: Suggested design to reduce ripple / noise on VCC, highly recommended when using an integrated antenna

Reference	Description	Part number - Manufacturer
C1	68 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C2	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C3	10 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C5	100 µF capacitor tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
FB1	Chip ferrite bead EMI filter for GHz band noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata

Table 18: Suggested components to reduce ripple / noise on VCC

☞ The necessity of each part depends on the specific design, but it is recommended to provide all the parts described in Figure 26 / Table 18 if the application device integrates an internal antenna.

☞ ESD sensitivity rating of the **VCC** supply pins is 1 kV (HBM according to JS-001-2017). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to the supply pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

2.2.1.11 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing.
- **VCC** connection must be routed as far as possible from the antenna, in particular if embedded in the application device: see Figure 27.
- Coupling between **VCC** and digital lines, especially USB, must be avoided.
- The tank bypass capacitor with low ESR for current spikes smoothing described in section 2.2.1.10 should be placed close to the **VCC** pins; if the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize **VCC** track length, otherwise consider using separate capacitors for DC-DC converter and module tank capacitor.
- The bypass capacitors in the pF range described in Figure 26 and Table 18 should be placed as close as possible to the **VCC** pins, where the **VCC** line narrows close to the module input pins, improving the RF noise rejection in the band centered on the self-resonant frequency of the pF capacitors: this is highly recommended if the application device integrates an internal antenna.
- Since **VCC** input provide the supply to RF power amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal; this is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the LEXI-R422 modules in the worst case.
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably closer to the DC source (otherwise protection function may be compromised).

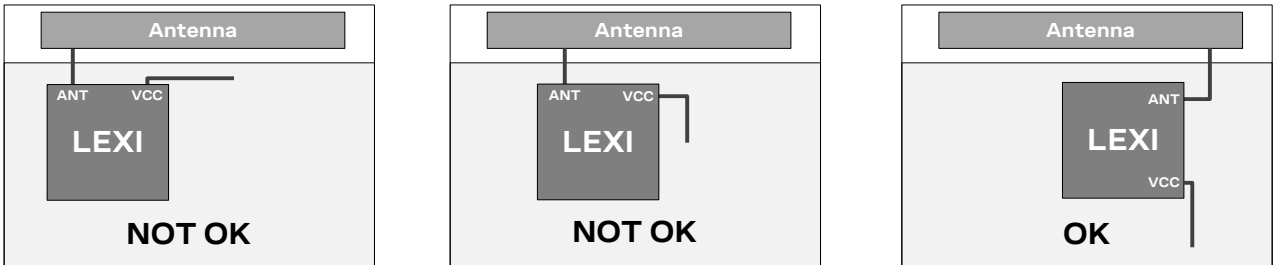

Figure 27: VCC line routing guideline for designs integrating an embedded antenna

2.2.1.12 Guidelines for grounding layout design

Good connection of the module **GND** pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer; it is strongly recommended that each **GND** pad surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- It is recommended to implement one layer of the application board as ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board; use as many vias as possible to connect the ground planes.
- Provide a dense line of vias at the edges of each ground area, in particular along RF and high speed lines.
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.
- Good grounding of **GND** pads also ensures thermal heat sink; this is critical during connection, when the real network commands the module to transmit at maximum power: correct grounding helps prevent module overheating.

2.2.2 Generic digital interfaces supply output (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

LEXI-R422 modules provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on and it is not in the deep-sleep power saving mode (as described in sections 1.6.1, 1.6.2)
- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply voltage translators to connect 1.8 V module generic digital interfaces to 3.0 V devices (e.g. see 2.6.1)
- Enable external voltage regulators providing supply for external devices

☞ Do not apply loads which might exceed the maximum available current from **V_INT** supply (see LEXI-R422 data sheet [1]) as this can cause malfunctions in internal circuitry.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (HBM according to JS-001-2017). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG) close to accessible point.

☞ It is recommended to monitor the **V_INT** pin to sense the end of the internal switch-off sequence of LEXI-R422 modules: **VCC** supply can be removed only after **V_INT** goes low.

☞ It is highly recommended to provide direct access to the **V_INT** pin on the application board by means of an accessible test point directly connected to the **V_INT** pin, for firmware upgrade and/or for diagnostic purposes.

2.3 System functions interfaces

2.3.1 Module PWR_CTRL input

2.3.1.1 Guidelines for PWR_CTRL circuit design

LEXI-R422 **PWR_CTRL** input is equipped with an internal active pull-up resistor; an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_CTRL** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 28 and Table 19.

ESD sensitivity rating of the **PWR_CTRL** pin is 1 kV (HBM according to JS-001-2017). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **PWR_CTRL** input from an application processor, as described in Figure 28.

PWR_CTRL input line should not be driven high, as it may cause start up issues.

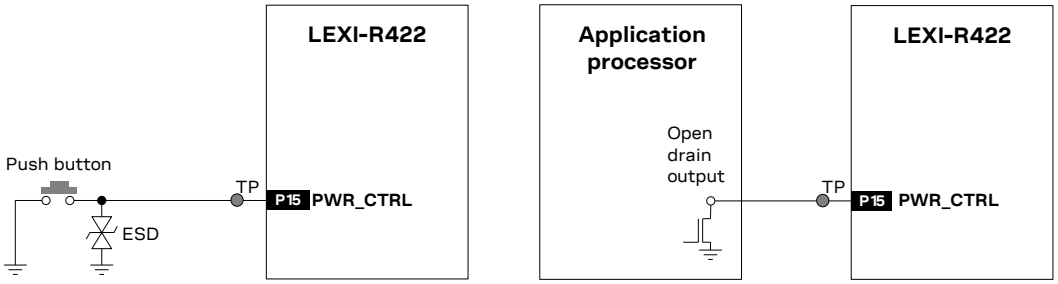

Figure 28: PWR_CTRL application circuits using a push button and an open drain output of an external processor

Reference	Description	Remarks
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 19: Example ESD protection component for the PWR_CTRL application circuit

It is highly recommended to provide direct access to the **PWR_CTRL** pin on the application board by means of an accessible test point directly connected to the **PWR_CTRL** pin, for firmware upgrade and/or for diagnostic purposes

2.3.1.2 Guidelines for PWR_CTRL layout design

The **PWR_CTRL** circuit requires careful layout since it is the sensitive input available to switch on and switch off the LEXI-R422 modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.4 Antenna interfaces

LEXI-R422 modules provide an RF interface for connecting the external antenna: the **ANT** pin represents the RF input/output for RF signals transmission and reception.

The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the related external antenna system through a 50 Ω transmission line to allow clean transmission / reception of RF signals.

2.4.1 Cellular antenna RF interface (ANT)

2.4.1.1 Guidelines for ANT pin RF connection design

A clean transition between the **ANT** pad and the application PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT** pad:

- On a multilayer PCB, the whole layer stack below the RF connections should be free of digital lines.
- Increase GND keep-out (i.e. clearance, a void area) at least up to 500 µm around the **ANT** pad on the top layer of the application PCB, to reduce parasitic capacitance to ground, as described in the left picture in Figure 29.
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** pad if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 29.

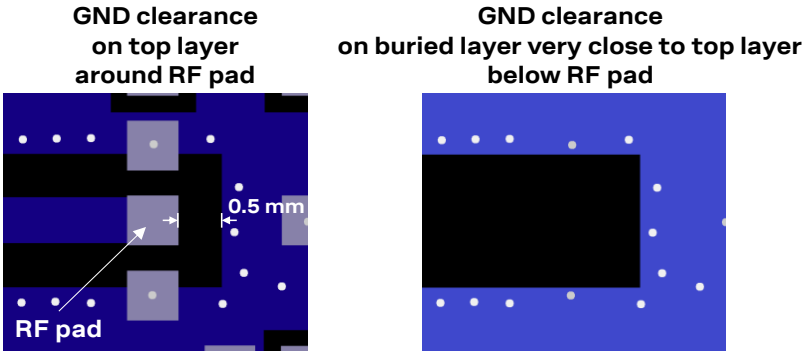

Figure 29: GND keep-out area on top layer around RF pad and on very close buried layer below RF pad (ANT)

☞ See section 2.4.1.6 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of LEXI-R422 surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.2 Guidelines for RF transmission lines design

Any RF transmission line, such as the ones from the **ANT** pad up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 30 and Figure 31 provide two examples of suitable 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

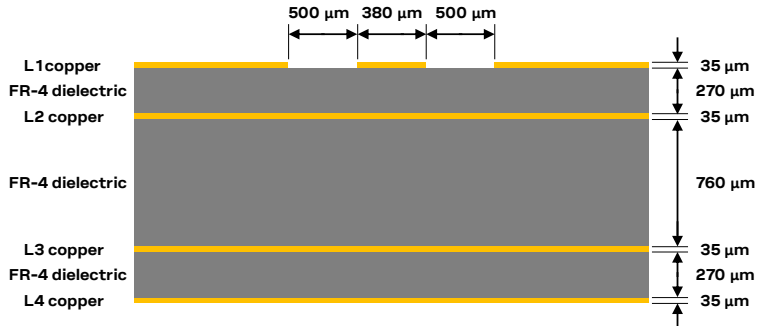

Figure 30: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

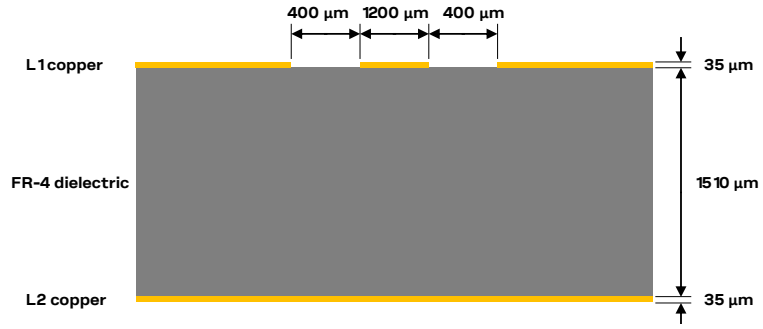

Figure 31: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB stack-up, then the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad) taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the transmission line width must be chosen due to:

- The thickness of the transmission line itself (e.g. 35 µm in the example of Figure 30 / Figure 31).
- The thickness of the dielectric material between the top layer (where the line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 30).
- The dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 30 and Figure 31).
- The gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 30 and 400 µm in Figure 31).

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the width of the line, use the “Coplanar Waveguide” model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission lines:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission lines, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground.
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND stitching vias around transmission lines, as described in Figure 32.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer, as described in Figure 32.
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB).

- Avoid stubs on the transmission lines.
- Avoid signal routing in parallel to transmission lines or crossing the transmission lines on buried metal layer.
- Do not route microstrip lines below discrete component or other mechanics placed on top layer.

Two examples of a suitable RF circuit design for **ANT** pin are illustrated in Figure 32, where the cellular antenna detection circuit is not implemented (if the cellular antenna detection function is required by the application, follow the guidelines for circuit and layout implementation detailed in section 2.4.3):

- In the first example shown on the left, the **ANT** pin is directly connected to an SMA connector by means of a suitable 50 Ω transmission line, designed with the appropriate layout.
- In the second example shown on the right, the **ANT** pin is connected to an SMA connector by means of a suitable 50 Ω transmission line, designed with the appropriate layout, with an additional high pass filter to improve the ESD immunity at the antenna port. The filter consists of a suitable series capacitor and shunt inductor, for example the Murata GRM1555C1H150JB01 15 pF capacitor and the Murata LQG15HN39NJ02 39 nH inductor with SRF ~1 GHz.

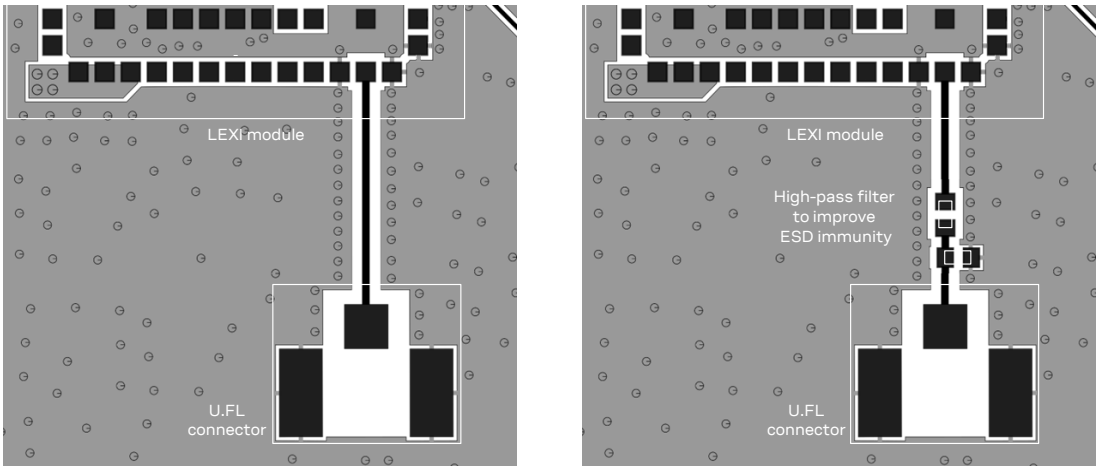

Figure 32: Example of circuit and layout for ANT RF circuits on the application board

☞ See section 2.4.1.6 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of LEXI-R422 surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.3 Guidelines for RF termination design

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination, to match the characteristic impedance of **ANT** port.

However, real antennas do not have a perfect 50 Ω load on all the supported frequency bands. So to reduce as much as possible any performance degradation due to antenna mismatching, the RF termination must provide optimal return loss (or VSWR) figures over all the operating frequencies, as summarized in Table 7.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable 50 Ω connector providing a clean PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require a GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to the annular pads of the four GND posts.
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads, as shown in Figure 32 and Figure 33.

- Cut out the GND layer under the RF connector and close to any buried vias, to remove stray capacitance and thus keep the RF line at 50 Ω, e.g. the active pad of U.FL connector needs to have a GND keep-out (i.e. clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

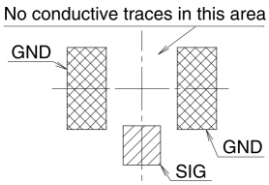

Figure 33: U.FL surface mounted connector mounting pattern layout

If an integrated antenna is used, the integrated antenna represents the RF termination. The following guidelines should be followed:

- Use an antenna designed by an antenna manufacturer providing the best possible return loss.
- Provide a ground plane large enough according to the relative integrated antenna requirements: the ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that needs to be radiated; as numerical example,
  Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including the PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes; it is recommended to consult the antenna manufacturer for antenna matching design-in guidelines relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place the antennas within a closed metal case.
- Do not place the cellular antenna in close vicinity to the end user since the emitted radiation in human tissue is restricted by regulatory requirements.
- Place the antennas as far as possible from VCC supply line and related parts (see also Figure 27), from high-speed digital lines (as USB) and from any possible noise source.
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce EMC or EMI issues.
- Be aware of interaction between co-located RF systems since the LTE transmitted power may interact or affect the performance of companion systems as a GNSS receiver (see section 2.4.2 for further details and design-in guidelines regarding cellular / GNSS RF coexistence).

☞ See section 2.4.1.6 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of LEXI-R422 surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.1.4 General guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antenna from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating the LEXI-R422 modules with all the applicable requirements depends on antenna radiating performance.

Cellular antennas are typically available as:

- External antennas (e.g. linear monopole):
  - External antennas basically do not imply physical restriction to the design of the PCB where the LEXI-R422 module is mounted.
  - The radiation performance mainly depends on the antennas: it is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses: additional insertion loss will be introduced by low quality or long cable; large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides a clean PCB-to-RF-cable transition: it is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antennas (e.g. PCB antennas such as patches or ceramic SMT elements):
  - Internal integrated antennas imply physical restriction to the design of the PCB: integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that needs to be radiated, given that the orientation of the ground plane relative to the antenna element must be considered. As numerical example, the PCB physical restriction can be considered as following:
    Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm
  - Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage: antennas should be selected with optimal radiating performance according to the mechanical specifications of the PCB and the whole product.
  - It is recommended to select a custom antenna designed by an antennas manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide); the antenna design process should begin at the start of the whole product design process.
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
  - Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes: it is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both cases, selecting external or internal antennas, these recommendations should be observed:

- Select an antenna providing optimal return loss / VSWR / efficiency figure over all the operating cellular frequencies.
- Select an antenna providing the worst possible return loss / VSWR / efficiency figure in the GNSS frequency band, to optimize the RF coexistence between the cellular and the GNSS systems (see section 2.4.2 for further details and guidelines regarding cellular / GNSS RF coexistence).
- Select an antenna providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in some countries, such as FCC United States (see section 4.2), ISED Canada (see section 4.3), CE Europe (see section 4.4), UKCA Great Britain (see section 4.5), etc.

2.4.1.5 Examples of cellular antennas

Table 20 lists some examples of possible internal on-board surface-mount antennas.

Manufacturer	Part number	Product name	Description
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.26.A	Havok	LTE SMD dielectric antenna 617..960 MHz, 1710..2690 MHz 54.6 x 13.0 x 3.0 mm
Taoglas	PCS.06.A	Reach	Low-profile 4G/3G/2G SMD antenna 698..960 MHz, 1710..2690 MHz 42.0 x 10.0 x 3.0 mm
Taoglas	PCS.86.A	Reach	Wideband cellular SMD antenna 791..6000 MHz 32.0 x 16.0 x 1.6 mm
Antenova	SR4L002	Lucida	GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm
KYOCERA AVX	1004795 / 1004796		Cellular SMD antenna 617..960 MHz, 1710..2200 MHz, 2490..2700 MHz 36.0 x 9.0 x 3.2 mm
KYOCERA AVX	P822601 / P822602		GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1710..2170 MHz, 2490..2700 MHz 50.0 x 8.0 x 3.2 mm
KYOCERA AVX	1002436		GSM / WCDMA / LTE vertical mount antenna 698..960 MHz, 1710..2700 MHz 50.6 x 19.6 x 1.6 mm
Ignion	NN03-310	TRIO mXTEND™	GSM / WCDMA / LTE SMD antenna 698..8000 MHz 30.0 x 3.0 x 1.0 mm
AMOTECH	AMMAL004, AMMAL008		GSM / WCDMA / LTE SMD antenna, AEC-Q200 699..960 MHz, 1710..2690 MHz 35.0 x 9.0 x 3.2 mm
AMOTECH	AMMAL021, AMMAL022		GSM / WCDMA / LTE SMD antenna, AEC-Q200 699..960 MHz, 1710..2690 MHz 39.0 x 9.0 x 3.2 mm
Pulse	W3796	Domino	GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1427..1661 MHz, 1695..2200 MHz, 2300..2700 MHz 42.0 x 10.0 x 3.0 mm
TE Connectivity	2118310-1		GSM / WCDMA / LTE vertical mount antenna 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 74.0 x 10.6 x 1.6 mm
Molex	1462000001		GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1700..2700 MHz 40.0 x 5.0 x 5.0 mm
Cirocomm	DSAN0001		Ceramic LTE SMD antenna 698..960 MHz, 1710..2170 MHz 40.0 x 6.0 x 5.0 mm

Table 20: Examples of internal surface-mount antennas

Table 21 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

Manufacturer	Part number	Product name	Description
PulseLarsen Antennas	W3929B0100		LTE FPC antenna with coax feed 617..960 MHz, 1710..2690 MHz, 3400..3900 MHz 115.8 x 30.4 mm
Taoglas	FXUB63		GSM / WCDMA / LTE PCB antenna with cable and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Taoglas	FXUB64	Cyclone	LTE wideband flex antenna 617..960 MHz, 1710..2690 MHz 130.0 x 30.0 mm
Taoglas	FXUB65 / FXUB68	Minima	Flexible wideband antenna 700..2700 MHz 67.0 x 58.0 x 0.2 mm
Laird Tech.	EFF692SA3S	Revie Flex	Flexible LTE antenna 689..875 MHz, 1710..2500 MHz 90.0 x 20.0 mm
Antenova	SRFL026	Mitis	GSM / WCDMA / LTE antenna on flexible PCB with cable and U.FL 689..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 110.0 x 20.0 mm
KYOCERA AVX	1002289		GSM / WCDMA / LTE antenna on flexible PCB with cable and U.FL 698..960 MHz, 1710..2700 MHz 140.0 x 75.0 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB antenna with cable and U.FL 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm
AMOTECH	AMMAL024		FPCB antenna with cable 617..5000 MHz 120.0 x 30.0 mm
AMOTECH	AMMAL030U200		GSM / LTE flexible PCB antenna with coaxial cable and connector 699..960 MHz, 1427..3800 MHz 43.0 x 43.0 mm

Table 21: Examples of internal antennas with cable and connector

Table 22 lists some examples of possible external antennas.

Manufacturer	Part number	Description
KYOCERA AVX	1003657	Cellular antenna with RG178 coax cable and MMCX connector 698..960 MHz, 1710..2700 MHz 104 x 22 x 4.2 mm
KYOCERA AVX	1004112-A001 / 1004112-B002 / 1004112-C003	Broadband External LTE / Cellular Antenna 698..960 MHz, 1710..2700 MHz 218.2 x 27.2 x 13.8 mm
KYOCERA AVX	X1005246-4GA1SA10A1	Adhesive-mount LTE external antenna 698..960 MHz, 1710..2170 MHz, 2300..2690 MHz, 105.1 x 30.1 x 6.7 mm
Taoglas	TG.35.8113	Wideband LTE dipole terminal antenna hinged SMA(M) 617..1200 MHz, 1710..2700 MHz, 4900..5900 MHz 224 x 58 x 13 mm

Manufacturer	Part number	Description
Taoglas	MA241.BI.001	GSM / WCDMA / LTE MIMO 2in1 adhesive-mount combination antenna waterproof IP67 rated with cable and SMA(M) 698..960 MHz, 1710..2170 MHz, 2400..2700 MHz 205.8 x 58 x 12.4 mm
Taoglas	GSA.8827.A.101111	Wideband I–Bar adhesive mount IP65 antenna with cable and SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2700 Mhz 105 x 30 x 7.7 mm
Taoglas	GSA.8835.A.101111	Wideband I–Bar adhesive mount IP67 antenna with cable and SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 105 x 30 x 7.7 mm
Laird Tech.	CMS69273	GSM / WCDMA / LTE ceiling-mount antenna with cable and N-type(F) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM	GSM / WCDMA / LTE pole-mount antenna with N-type(M) 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Pulse Electronics	SPDA24617/3900	Multiband swivel dipole antenna with SMA(M) 617..960 MHz, 1400..2700 MHz, 3200..3900 MHz 223.24 x 56.13 x 10.97 mm
AMOTECH	ACA556022-S0-A1	Low-profile, screw-type LTE/Sub6G antenna, Waterproof IP67 699..3800 MHz 80.0 x 60.0 x 22.5 mm
AMOTECH	ACA556022-S0-A2	Low-profile, adhesive-type LTE/Sub6G antenna, Waterproof IP67 699..3800 MHz 55.0 x 60.0 x 22.0 mm
AMOTECH	ACAD6623-S0-A1	Low-profile, roof-mount LTE/Sub6G antenna, Waterproof IP67 699..3800 MHz 23.0 x Ø 60.0 mm

Table 22: Examples of external antennas

2.4.1.6 Antenna trace design used for LEXI-R422 modules' type approvals

The conformity assessment of u-blox LEXI-R422 LGA surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc. has been carried out with the modules mounted on a u-blox host printed circuit board (PCB) with a 50 Ω grounded coplanar waveguide designed on it, herein referenced as "antenna trace design". The antenna trace design implements the connection of the **ANT** LGA pad of the module, which is the cellular RF input/output of the module, up to a dedicated 50 Ω SMA connector, which is the cellular RF input/output of the host PCB for external antenna and/or RF cable access.

☞ Manufacturers of mobile or fixed devices incorporating LEXI-R422 modules are authorized to use the FCC United States Grants and ISED Canada Certificates of the modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for regulatory type approvals of the modules, described in this section.

☞ In case of antenna trace design change, an FCC Class II Permissive Change and/or ISED Class IV Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID and/or the ISES Multiple Listing (new application) procedure followed by an FCC C2PC and/or ISED C4PC application.

The antenna trace design is implemented on the u-blox host PCB as illustrated in Figure 34, using the parts listed in Table 23, with the support of the additional optional antenna detection capability.

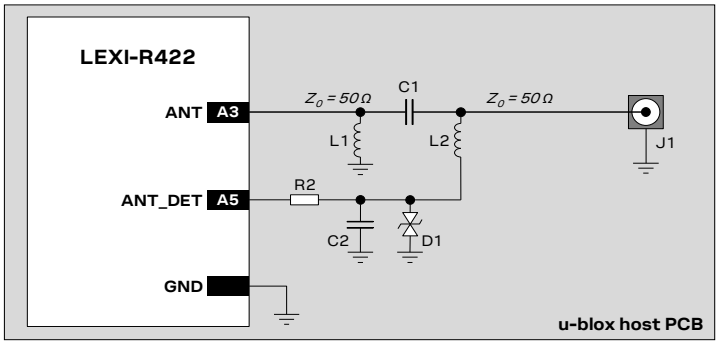

Figure 34: Antenna trace design implemented on the u-blox host PCB, with additional antenna detection circuit

Reference	Description	Part number – Manufacturer
C1	47 pF capacitor ceramic C0G 0201 2% 50 V	GRM0335C1H470GA01 – Murata
C2	39 pF capacitor ceramic C0G 0201 5% 50 V	GRM0332C1H390JA01 – Murata
D1	Low capacitance ESD protection	CG0402MLE-18G – Bourns
L1	39 nH multilayer inductor 0402 (SRF ~1 GHz)	Not Installed
L2	82 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS82NJ02B – Murata
R2	10 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 – Amphenol

Table 23: Parts in use on the u-blox host PCB for the antenna trace design, with additional antenna detection circuit

The u-blox host PCB has a structure of 6 copper layers with 35 µm thickness (1 oz/ft^2) for all the layers except the two inner buried layers, having 18 µm thickness (1/2 oz/ft^2), using FR4 dielectric substrate material with 4.3 typical permittivity and 0.013 typical loss tangent at 1 GHz.

The top layer layout of the u-blox host PCB is described in Figure 35, implementing the RF antenna trace designed as a 50 Ω grounded coplanar waveguide, with ~24 mm length from the pad designed to accommodate the **ANT** pad of LEXI-R422 module up to the pads designed to accommodate the SMA RF connector for an external cellular antenna and/or RF coaxial cable.

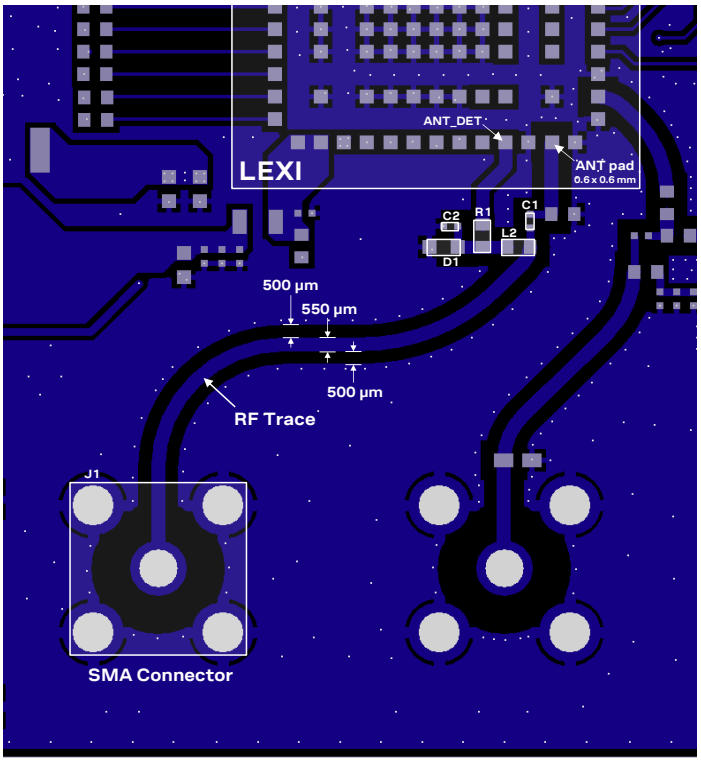

Figure 35: Top layer (L1) layout of the u-blox host PCB with the antenna RF trace design

The PCB stack-up structure of the 6-layer u-blox host PCB is illustrated in Figure 36.

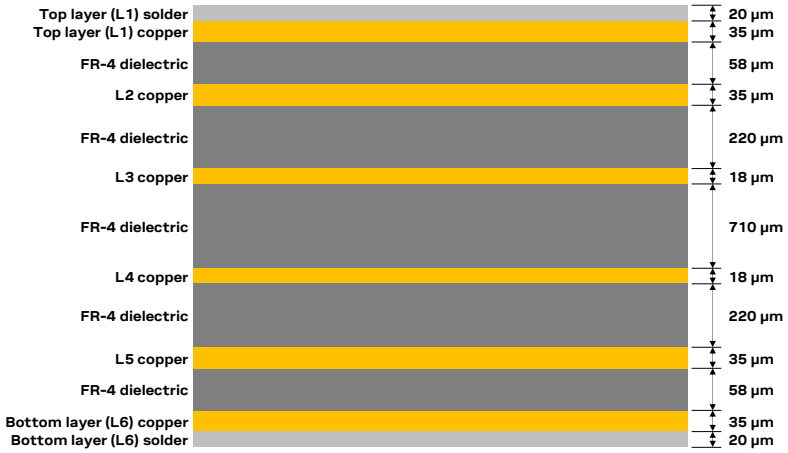

Figure 36: Stack-up structure of the u-blox host PCB

Considering that the thickness of the dielectric material from the top layer to the buried layer is less than 200 µm, GND keep-out is implemented on the buried metal layer area below the **ANT** pad and the antenna RF trace as illustrated in Figure 37.

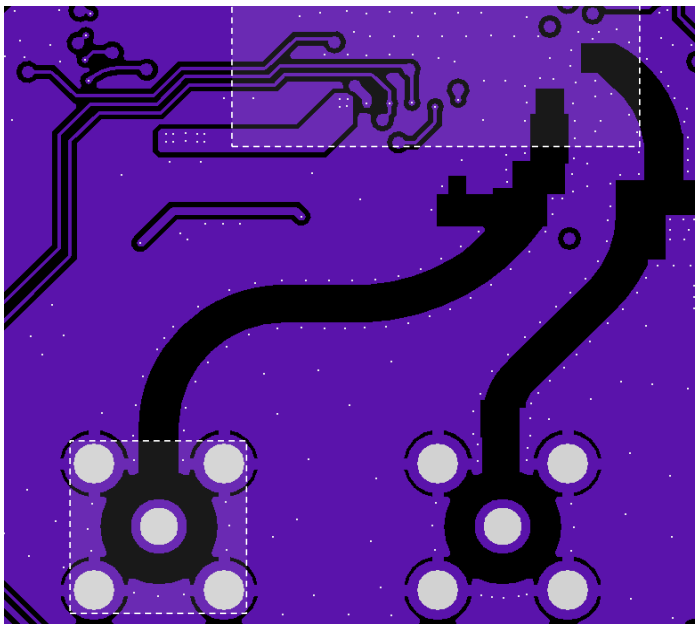

Figure 37: Buried metal layer (L2) layout of the u-blox host PCB, below the antenna RF trace design

Guidelines to design an equivalent proper connection for the **ANT** pad are available in section 2.4.1.1. Guidelines to design an equivalent proper 50 Ω transmission line are available in section 2.4.1.2. Guidelines to design a proper equivalent 50 Ω termination are available in section 2.4.1.3, with further guidelines for cellular antenna selection and design available in section 2.4.1.4. Guidelines to design a proper equivalent (optional) antenna detection circuit are available in section 2.4.3.

The 50 Ω characteristic impedance of the antenna trace design on a host PCB can be verified using a Vector Network Analyzer, as done on the u-blox host PCB, with calibrated RF coaxial cable soldered at the pad corresponding to RF input/output of the module and with the transmission line terminated to a 50 Ω load at the 50 Ω SMA connector.

Compliance of the design with regulatory rules and specifications defined by the FCC, ISED, RED, etc. can be verified using a radio communication tester (callbox) as the Rohde & Schwarz CMW500, or any equivalent equipment for multi-technology signaling conformance tests.

2.4.2 Cellular and GNSS RF coexistence

Overview

Desensitization or receiver blocking is a form of electromagnetic interference where a radio receiver is unable to detect a weak signal that it might otherwise be able to receive when there is no interference (see Figure 38). Good blocking performance is particularly important in the scenarios where several radios of various forms are used in close proximity to each other.

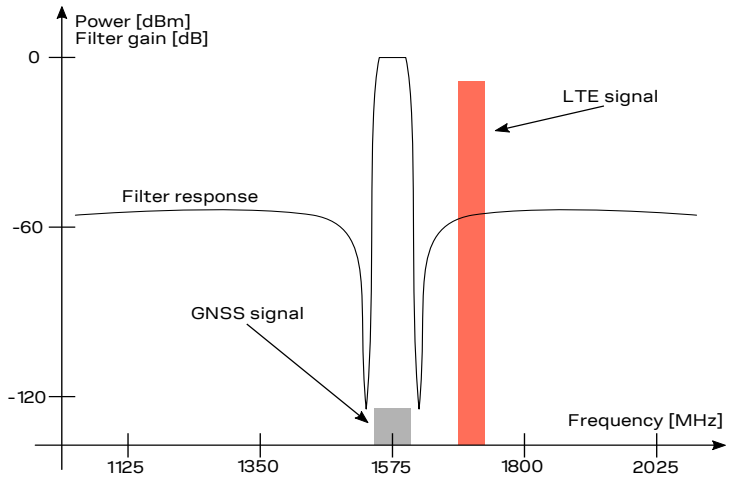

Figure 38: Interference due to transmission in LTE B3, B4 and B66 low channels (1710 MHz) adjacent to GNSS frequency range (1561 to 1605 MHz). Harmonics due to transmission in LTE B13 high channels (787 MHz) may fall into the GNSS bands

Jamming signals may come from in-band and out-of-band frequency sources. In-band jamming is caused by signals with frequencies falling within the GNSS frequency range, while the out-of-band jamming is caused by very strong signals adjacent to the GNSS frequency range so that part of the strong signal power may leak at the input of the GNSS receiver and/or block GNSS reception.

If not properly taken into consideration, in-band and out-band jamming signals may cause a reduction in the carrier-to-noise power density ratio (C/No) of the GNSS satellites.

In-band interference

In-band interference signals are typically caused by harmonics from displays, switching converters, micro-controllers and bus systems. Moreover, considering for example the LTE band 13 high channel transmission frequency (787 MHz) and the GPS operating band (1575.42 MHz ± 1.023 MHz), the second harmonic of the cellular signal is exactly within the GPS operating band. Therefore, depending on the board layout and the transmit power, the highest channel of LTE band 13 is the channel that has the greatest impact on the C/No reduction.

Countermeasures against in-band interference include:

- Maintaining a good grounding concept in the design
- Ensuring proper shielding of the different RF paths
- Ensuring proper impedance matching of RF traces
- Placing the GNSS antenna away from noise sources
- Add a notch filter along the GNSS RF path, just after the antenna, at the frequency of the jammer

Out-of-band interference

Out-of-band interference is caused by signal frequencies that are different from the GNSS, the main sources being cellular, Wi-Fi, bluetooth transmitters, etc. For example, the lowest channels in LTE band 3, 4 and 66 can compromise the good reception of the GLONASS satellites. Again, the effect can be explained by comparing the LTE frequencies (low channel transmission frequency is 1710 MHz) with the GLONASS operating band (1602 MHz ± 8 MHz). In this case the LTE signal is outside the useful GNSS band, but provided that the power received by the GNSS subsystem at 1710 MHz is high enough, blocking and leakage effects may appear reducing once again the C/No.

Countermeasures against out-of-band interference include:

- Maintaining a good grounding concept in the design.
- Keeping the GNSS and cellular antennas more than the quarter-wavelength (of the minimum Tx frequency) away from each other. If for layout or size reasons this requirement cannot be met, then the antennas should be placed orthogonally to each other and/or on different side of the PCB.
- Selecting a cellular antenna providing the worst possible return loss / VSWR / efficiency figure in the GNSS frequency band: the lower is the cellular antenna efficiency between 1561 MHz and 1610 MHz, the higher is the isolation between the cellular and the GNSS systems.
- Ensuring at least 15 – 20 dB isolation between antennas in the GNSS band by implementing the most suitable placement for the antennas, considering in particular the related radiation diagrams of the antennas: better isolation results from antenna patterns with radiation lobes in different directions considering the GNSS frequency band.
- Adding a GNSS pass-band SAW filter along the GNSS RF line, providing very large attenuation in the cellular frequency bands.

Additional countermeasures

In case all the aforementioned countermeasures cannot be implemented, adding a GNSS stop-band SAW filter along the cellular RF line may be considered. The filter shall provide very low attenuation in the cellular frequency bands (see Table 24 for possible suitable examples). It has to be noted that the addition of an external filter along the cellular RF line has to be carefully evaluated, considering that the additional insertion loss of such filter may affect the cellular TRP and/or TIS RF figures.

Table 24 lists examples of GNSS band-stop SAW filters that may be considered for the cellular RF input/output in case enough isolation between the cellular and the GNSS RF systems cannot be provided by proper selection and placement of the antennas beside other proper RF design solutions.

Manufacturer	Part number	Description
Qualcomm RF360	B8666	GNSS (L1) SAW extractor filter 1.7 x 1.3 mm
Qualcomm RF360	B8939	GNSS (L1) SAW extractor filter 1.5 x 1.1 mm
Murata	SADAC1G56AB0E0A	GNSS (L1) SAW extractor filter 1.5 x 1.1 mm
TST	TE0123A	GPS (1575.42MHz) SAW band-stop filter 3.0 x 3.0 mm

Table 24: Examples of GNSS band-stop SAW filters

Additional considerations

As far as the RF Tx power is involved in the cellular / GNSS RF coexistence, it has to be noted that high-power transmission occurs very infrequently: typical values are in the range of -3 to 0 dBm (see Figure 1 in the GSMA official document TS.09 [10]). Therefore, depending on the application, careful PCB layout, antenna selection and placement should be sufficient to ensure accurate GNSS reception.

For an example of vehicle tracking application in a small form factor featuring cellular and short-range connectivity alongside a multi-constellation GNSS receiver, with successful RF coexistence between the systems, refer to the u-blox B36 vehicle tracking blueprint [17]. The distance between the cellular and GNSS antennas for the u-blox B36 blueprint is annotated in Figure 39.

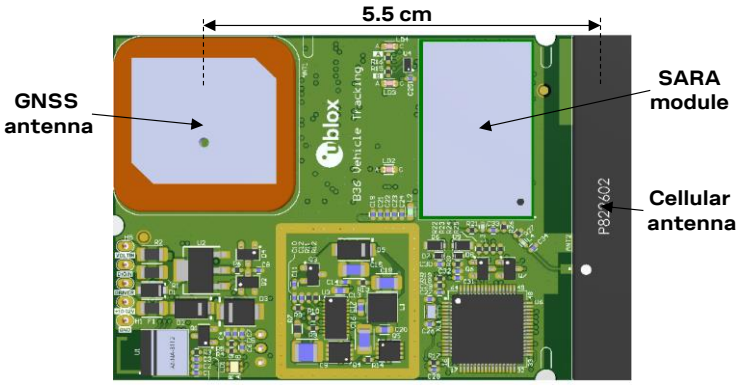

Figure 39: PCB top rendering for the u-blox B36 blueprint with annotated distance between cellular and GNSS antennas

2.4.3 Antenna detection interface (ANT_DET)

2.4.3.1 Guidelines for ANT_DET circuit design

Figure 40 and Table 25 describe the recommended schematic / components for the antenna detection circuit that must be provided on the application board and for the diagnostic circuit that must be provided on the antenna's assembly to achieve antenna detection functionality.

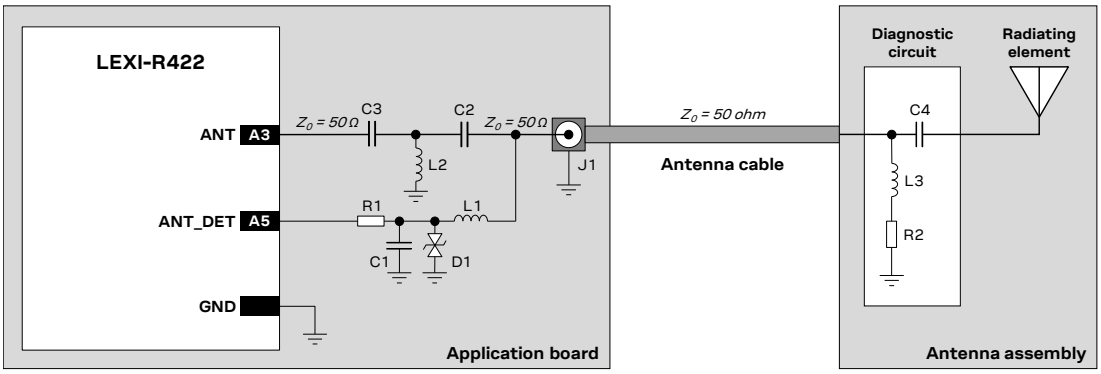

Figure 40: Suggested schematic for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Reference	Description	Part number - Manufacturer
C1	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2	33 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 - Amphenol
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150J - Murata
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 - Murata
C4	22 pF capacitor ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2	15 kΩ resistor for diagnostics	Generic manufacturer

Table 25: Suggested parts for antenna detection circuit on application PCB and diagnostic circuit on antennas assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 40 and Table 25 are here explained:

- When antenna detection is forced by the +UANTR AT command, the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C4) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self-Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L3), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Resistor on the **ANT_DET** path (R1) is needed for accurate measurements through the +UANTR AT command; it also acts as an ESD protection.
- Additional components (C1 and D1 in Figure 40) are provided as **ANT_DET** pin as ESD protection.
- Additional high pass filter (C3 and L2 in Figure 40) is provided as ESD immunity improvement.
- The **ANT** pin must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 40, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self-Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (for example from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is correctly connected.
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit “over range” report (see the AT commands manual [2]) means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an unclean connection, a damaged antenna or incorrect value of the antenna load resistor for diagnostics.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT** pin can be directly connected to the antenna connector by means of a 50 Ω transmission line as described in Figure 32.

2.4.3.2 Guidelines for ANT_DET layout design

Figure 41 describes the recommended layout for the antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 40 and Table 25:

- The **ANT** pin must be connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines in section 2.4.1.4 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT** pin (C2) must be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin must be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductor in series at the **ANT_DET** pin (L1) must be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) are provided as **ANT_DET** ESD protection.
- The additional high pass filter (C3 and L2) is provided as ESD immunity improvement.

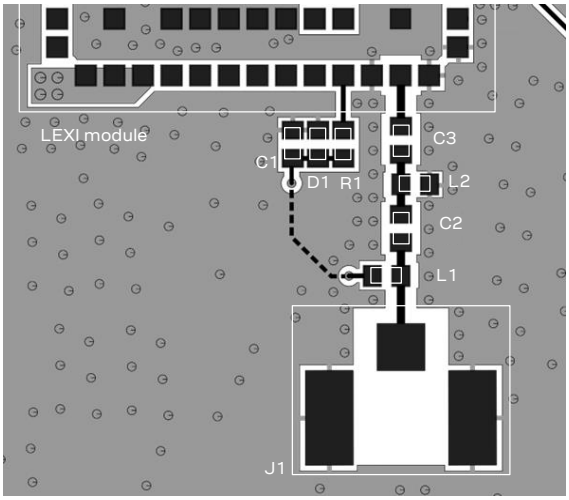

Figure 41: Suggested layout for antenna detection circuit on application board

☞ See section 2.4.1.6 for the description of the antenna trace design implemented on the u-blox host printed circuit board used for conformity assessment of LEXI-R422 surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc.

2.4.4 Cellular antenna dynamic tuner interface

LEXI-R422 modules include two output pins (named **RFCTRL1** and **RFCTRL2**) that can be configured, as optional feature, to change their output value dynamically according to the specific actual cellular band in use by the module. These pins, paired with an external antenna tuner IC or RF switch, can be used to:

- Tune antenna impedance to reduce power losses due to mismatch
- Tune antenna aperture to improve total antenna efficiency
- Select the optimal antenna for each operating band

Figure 42 shows the example application circuits implementing impedance tuning and aperture tuning. The module controls an RF switch which is responsible for selecting the appropriate matching element for the operating band. Table 26 reports suggested components implementing the SP4T RF switch functionality.

In Figure 42(a), tuning the antenna impedance optimizes the power delivered into the antenna by dynamically adjusting the RF impedance seen by **ANT** pin of LEXI-R422 module. By creating a tuned matching network for each operating band, the total radiated power (TRP) and the total isotropic sensitivity (TIS) metrics are improved.

In Figure 42(b), antenna aperture tuning enables higher antenna efficiency over a wide frequency range. The dynamically tunable components are added to the antenna structure itself, thereby modifying the effective electrical length of the radiating element. Thus, the resonant frequency of the antenna is shifted into the module's operating frequency band. Aperture tuning optimizes radiation efficiency, insertion loss, isolation, and rejection levels of the antenna.

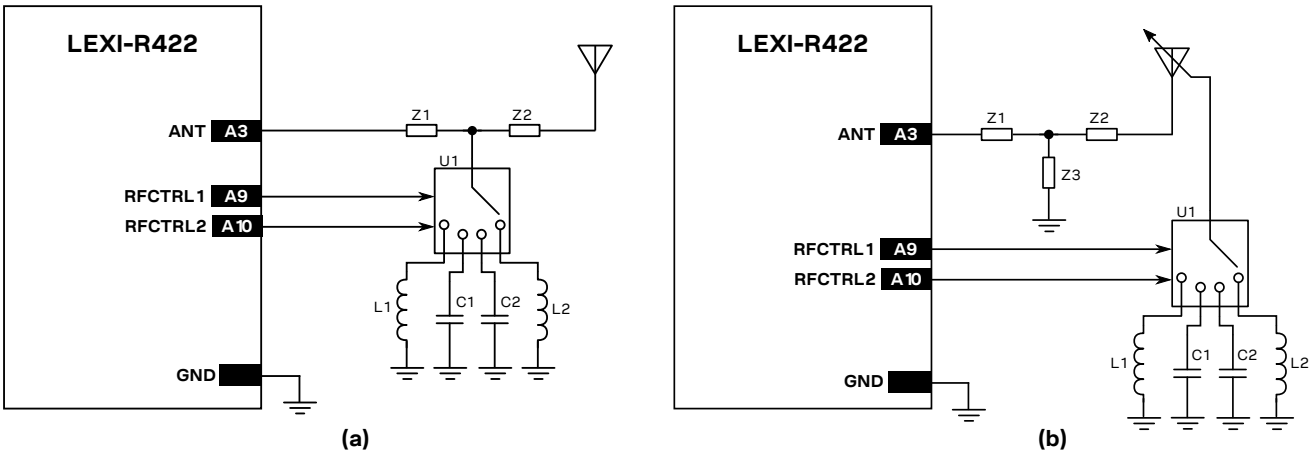

Figure 42: Examples of schematics for cellular antenna dynamic impedance tuning (a) and aperture tuning (b).

Refer to the antenna datasheet and/or manufacturer for proper values of matching components Z1, Z2, Z3, L1, L2, C1, C2. These components should have low losses to avoid degrading the radiating efficiency of the antenna, thereby hindering the positive effects of dynamic tuning.

Manufacturer	Part number	Description
Peregrine Semiconductor	PE42442	30..6000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE613050	5..3000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE42440	50..3000 MHz UltraCMOS SP4T RF switch
Skyworks Solutions	SKY13626-685LF	400..3800 MHz SP4T high-power RF switch
Skyworks Solutions	SKY13380-350LF	20..3000 MHz SP4T high-power RF switch
KYOCERA AVX	EC646	100..3000 MHz ultra-small SP4T RF switch
KYOCERA AVX	EC686-3	100..3000 MHz ultra-low R_{ON} SP4T RF switch
Qorvo	RF1654A	100..2700 MHz SP4T RF switch
Infineon	BGSA14GN10	100..6000 MHz SP4T RF switch for antenna tuning applications

Table 26: Examples of RF switches for cellular antenna dynamic tuning

2.5 SIM interface

2.5.1 Guidelines for SIM circuit design

2.5.1.1 Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP/SWP (Other function) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 6 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Surface-Mounted UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by the ETSI TS 102 671 as:

- Case pin 8 = UICC contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case pin 7 = UICC contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case pin 6 = UICC contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case pin 5 = UICC contact C4 = AUX1 (Aux.contact) → It must be left not connected
- Case pin 1 = UICC contact C5 = GND (Ground) → It must be connected to **GND**
- Case pin 2 = UICC contact C6 = VPP/SWP (Other) → It can be left not connected
- Case pin 3 = UICC contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case pin 4 = UICC contact C8 = AUX2 (Aux. contact) → It must be left not connected

A Surface-Mounted SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Surface-Mounted SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

2.5.1.2 Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of LEXI-R422 modules as described in Figure 43, where the optional SIM detection feature is not implemented.

Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal to match the SIM requirements (50 ns is the maximum allowed rise time on clock line, 1.0 µs is the maximum allowed rise time on data and reset lines).

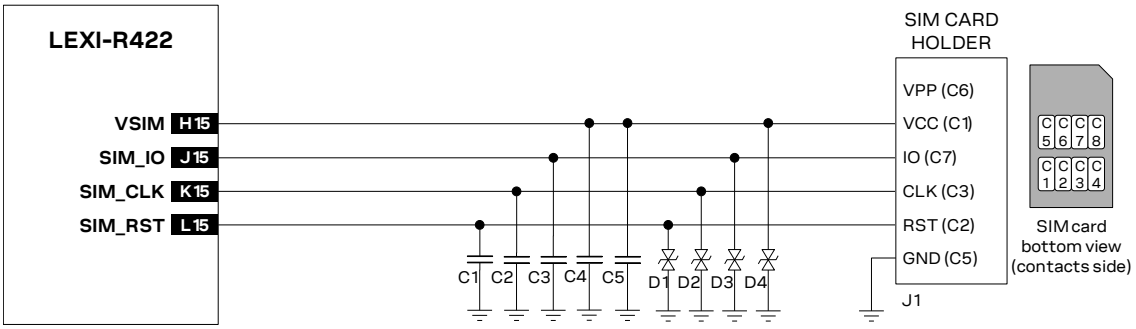

Figure 43: Application circuits for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
J1	SIM card holder, 6 positions, without card presence switch	Generic manufacturer, as C707 10M006 136 2 - Amphenol

Table 27: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

2.5.1.3 Guidelines for single SIM chip connection

A Surface-Mounted SIM chip (M2M UICC Form Factor) must be connected the SIM card interface of the LEXI-R422 modules as described in Figure 44.

Follow these guidelines to connect the module to a Surface-Mounted SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM lines.
- Limit capacitance and series resistance on each SIM signal to match the SIM requirements (50 ns is the maximum allowed rise time on clock line, 1.0 µs is the maximum allowed rise time on data and reset lines).

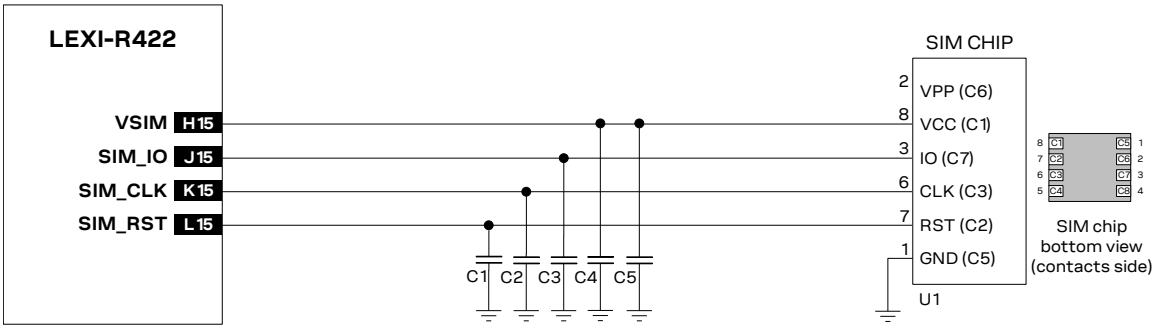

Figure 44: Application circuits for the connection to a single Surface-Mounted SIM chip

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC form factor)	Generic manufacturer

Table 28: Example of components for the connection to a single solderable SIM chip

2.5.1.4 Guidelines for single SIM card connection with detection

An application circuit for the connection to a single removable SIM card placed in a SIM card holder is described in Figure 45, where the optional SIM card detection feature is implemented.

Follow these guidelines connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.

- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (as the SW2 pin in Figure 45) to the **GPIO6** input pin, providing a weak pull-down resistor (e.g. 470 kΩ, as R2 in Figure 45).
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (SW1 pin in Figure 45) to **V_INT** 1.8 V supply output by means of a strong pull-up resistor (e.g. 1 kΩ, as R1 in Figure 45).
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (less than 10 pF) ESD protection (as Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector. The ESD sensitivity rating of SIM interface pins is 1 kV (HBM according to JS-001-2017), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface (50 ns = maximum rise time on **SIM_CLK**, 1.0 µs = maximum rise time on **SIM_IO** and **SIM_RST**).

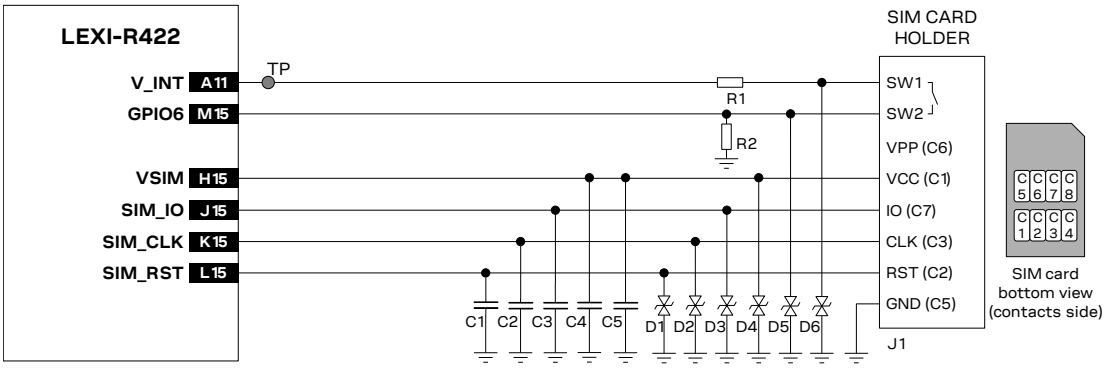

Figure 45: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D6	Very low capacitance ESD protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM card holder, 6 + 2 positions, with card presence switch	Generic manufacturer, as CCM03-3013LFT R102 - C&K Components

Table 29: Example of components for the connection to a single removable SIM card, with SIM detection implemented

2.5.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the LEXI-R422 modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE receiver channels whose carrier frequency is coincidental with harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 43, Figure 44, and Figure 45 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Data communication interfaces

2.6.1 UART interfaces

2.6.1.1 Guidelines for UART circuit design

Providing 1 UART with full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed, two different external voltage translators can be used to provide full RS-232 (9 lines) functionality: e.g. using the Texas Instruments SN74AVC8T245PW for the translation from 1.8 V to 3.3 V, and the Maxim MAX3237E for the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V Application Processor (DTE) is used and complete RS-232 functionality is required, then the complete 1.8 V UART of the module (DCE) should be connected to a 1.8 V DTE, as in Figure 46.

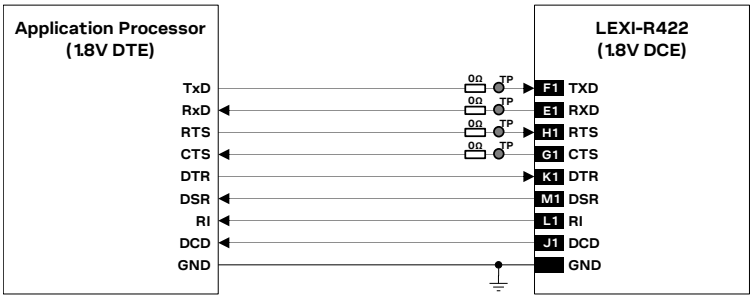

Figure 46: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 47.

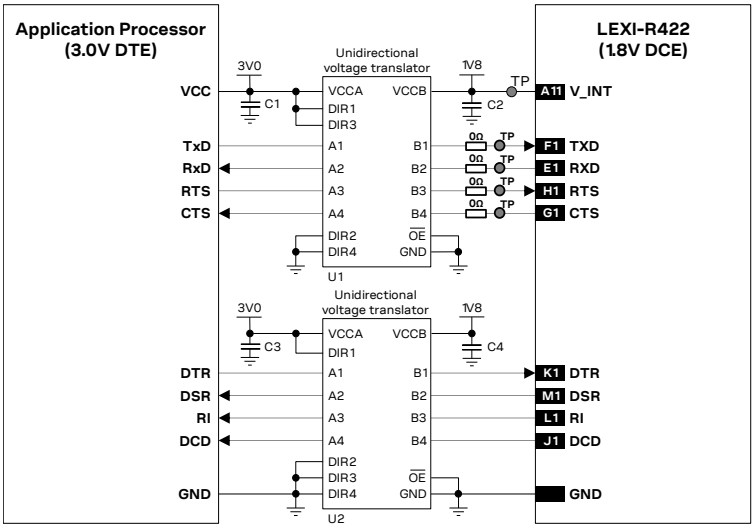

Figure 47: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774[3] - Texas Instruments

Table 30: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

[3] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with TXD, RXD, RTS, CTS and DTR lines only

If the functionality of the **DSR**, **DCD** and **RI** lines is not required, or the lines are not available:

- Leave **DSR**, **DCD** and **RI** lines of the module floating

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

Figure 48 describes the circuit that should be implemented as if a 1.8 V Application Processor (DTE) is used, given that the DTE will behave correctly regardless of the **DSR** input setting.

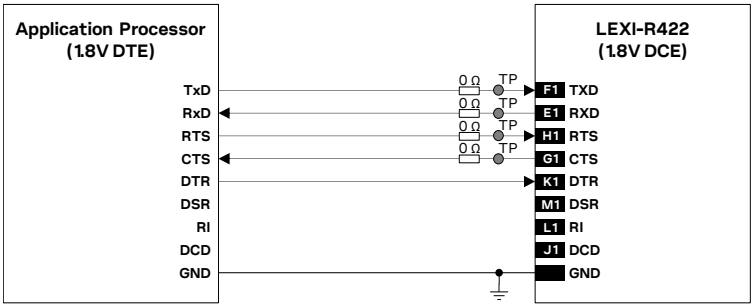

Figure 48: UART interface application circuit with partial V.24 link (6-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 49, given that the DTE will behave correctly regardless of the **DSR** input setting.

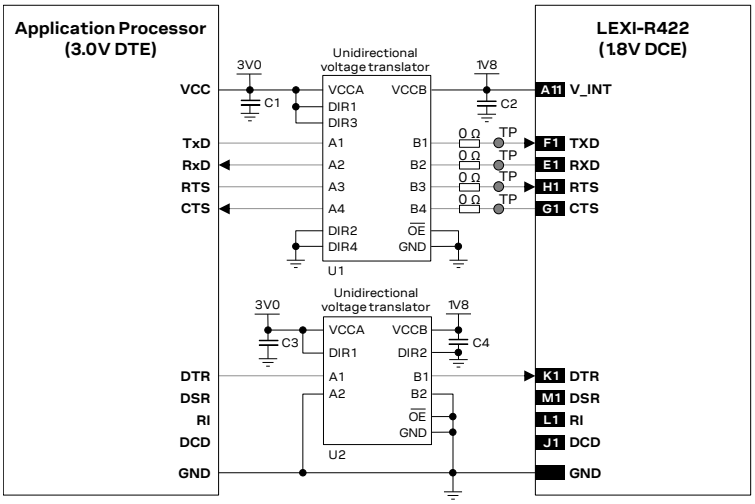

Figure 49: UART interface application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional voltage translator	SN74AVC4T774[4] - Texas Instruments
U2	Unidirectional voltage translator	SN74AVC2T245[4] - Texas Instruments

Table 31: UART application circuit components with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

[4] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with TXD, RXD, RTS and CTS lines only

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required, or the lines are not available:

- Connect the module **DTR** input to GND using a 0 Ω series resistor, since it may be useful to set **DTR** active if not specifically handled, in particular to have URCs presented over the UART interface (see the AT commands manual [2] for the &D, S0, +CNMI AT commands)
- Leave **DSR**, **DCD** and **RI** lines of the module floating

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard. If a 1.8 V Application Processor is used, the circuit should be implemented as described in Figure 50.

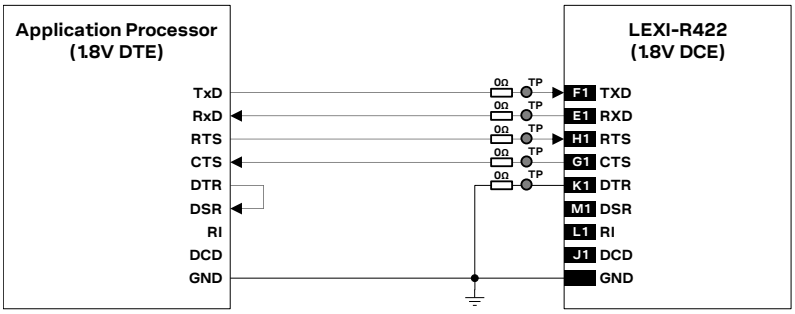

Figure 50: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 51.

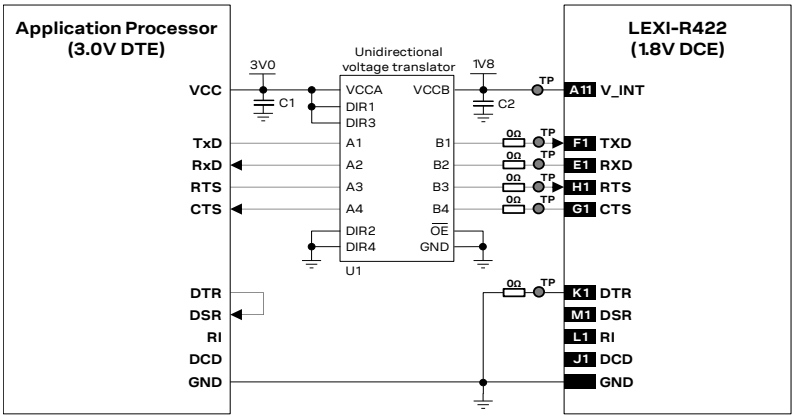

Figure 51: UART interface application circuit with a partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional voltage translator	SN74AVC4T774[5] - Texas Instruments

Table 32: UART application circuit components with a partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

[5] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with the TXD, RXD, RTS and CTS lines

LEXI-R422 modules include an auxiliary UART interface (UART AUX), as alternative mutually exclusive function over the **DTR**, **DSR**, **DCD** and **RI** pins, with settings configurable by dedicated AT commands (see the AT commands manual [2]):

- Data lines (**DCD** as data output, **DTR** as data input)
- HW flow control lines (**RI** as flow control output, **DSR** as flow control input)

If RS-232 compatible signal levels are needed, two Maxim MAX13234E voltage level translators can be used. These chips translate voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 52.

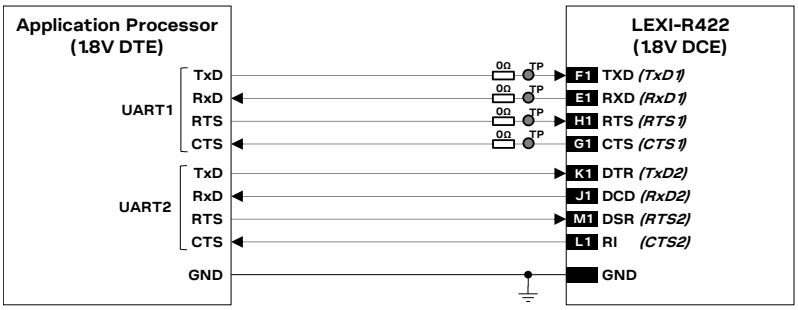

Figure 52: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 53.

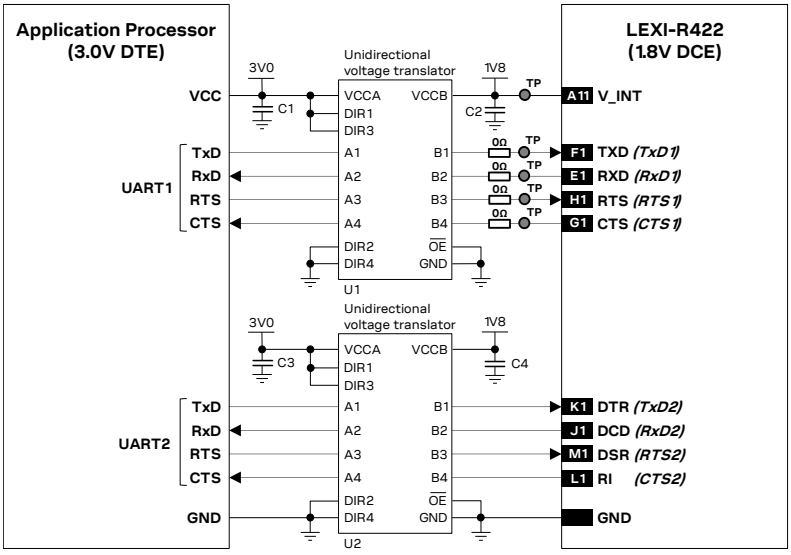

Figure 53: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [6] - Texas Instruments

Table 33: Components for 2 UARTs application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

[6] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with TXD and RXD lines only

☞ Providing the **TXD** and **RXD** lines only is not recommended if the multiplexer functionality is used in the application: providing also at least the HW flow control (**RTS** and **CTS** lines) is recommended, and it is in paricular necessary if the low power mode is enabled by +UPSV AT command.

If functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, then:

- Connect the **RTS** input line to GND or to the **CTS** output line of the module, since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, default setting)
- Connect the **DTR** input line to GND using a 0 Ω series resistor, because it is useful to set **DTR** active if not specifically handled, in particular to have URCs presented over the UART interface (see the AT commands manual [2], &D, S0, +CNMI AT commands)
- Leave **DSR**, **DCD** and **RI** lines of the module floating

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor (DTE) is used, the circuit should be implemented as in Figure 54.

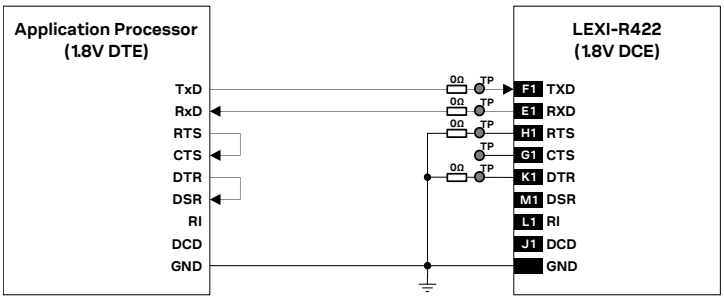

Figure 54: UART interface application circuit with a 3-wire link in the DTE/DCE serial communication (1.8V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 55.

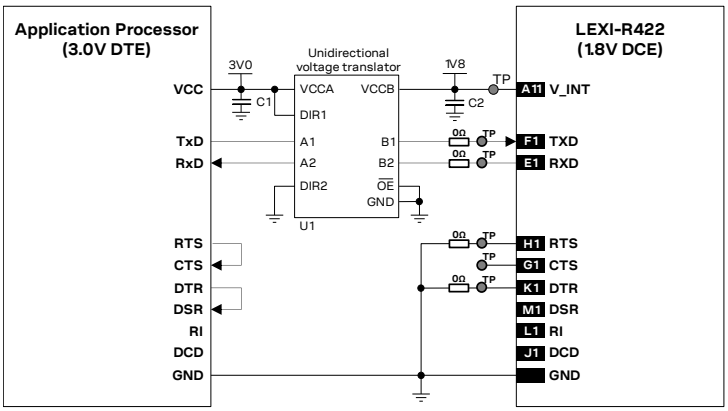

Figure 55: UART interface application circuit with a partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional voltage translator	SN74AVC2T245[7] - Texas Instruments

Table 34: UART application circuit components with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

[7] Voltage translator providing partial power down feature so that the DTE 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Additional considerations

If a 3.0 V Application Processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-down / pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values. Make sure that any DTE signal connected to the module is tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a clean boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the corresponding 3.0 V input of the Application Processor (DTE) can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

- The **TXD** data input line of the module has an internal active pull-up enabled.
- Do not apply voltage to any UART interface pin before the switch-on of the UART supply source, which is the **V_INT** supply of the module.
- ESD sensitivity rating of the UART interface pins is 1 kV (HBM according to JS-001-2017). Higher protection levels could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 USB interface

2.6.2.1 Guidelines for USB circuit design

The **USB_D+** and **USB_D-** lines carry the USB serial data and signaling. The lines are used in single-ended mode for full speed signaling handshake, as well as in differential mode for high speed signaling and data transfer.

USB pull-up or pull-down resistors and external series resistors on **USB_D+** and **USB_D-** lines as required by the USB 2.0 specification [4] are part of the module USB pins driver and do not need to be externally provided.

Routing the USB pins to a connector, they will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to accessible point on the line connected to this pin, as described in Figure 56 and Table 35.

- USB interface pins ESD sensitivity rating is 1 kV (HBM according to JS-001-2017). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ultra-low capacitance (i.e. < 1 pF) ESD protection (e.g. Littelfuse PESD0402-140 ESD protection device) on the lines connected to these pins, close to accessible points.

The LEXI-R422 modules do not support AT command / data communication over USB interface: the USB interface is available on these modules product versions for FW upgrade by means of the dedicated u-blox EasyFlash tool and for diagnostic purposes only. Therefore, the USB interface of these modules product versions is not designed to be connected to an external host processor mounted on the application board.

☞ It is highly recommended to provide access to **V_INT**, **PWR_CTRL**, **USB_5V0**, **USB_3V3**, **USB_D+**, **USB_D-**, and **RSVD #99** pins for FW upgrade and/or for diagnostic purpose, making available:

(a) accessible test points, directly connected to the related pins of the module, as illustrated in the application circuit example of Figure 56(a), or

(b) the specific SAMTEC FTSH-103-01-L-DV male header connector, directly connected to the related pins of the module, as shown in the application circuit example of Figure 56(b), or

(c) a generic USB device connector, connected to the related pins of the module through the specific circuit illustrated in the application circuit example of Figure 56(c) and Table 35.

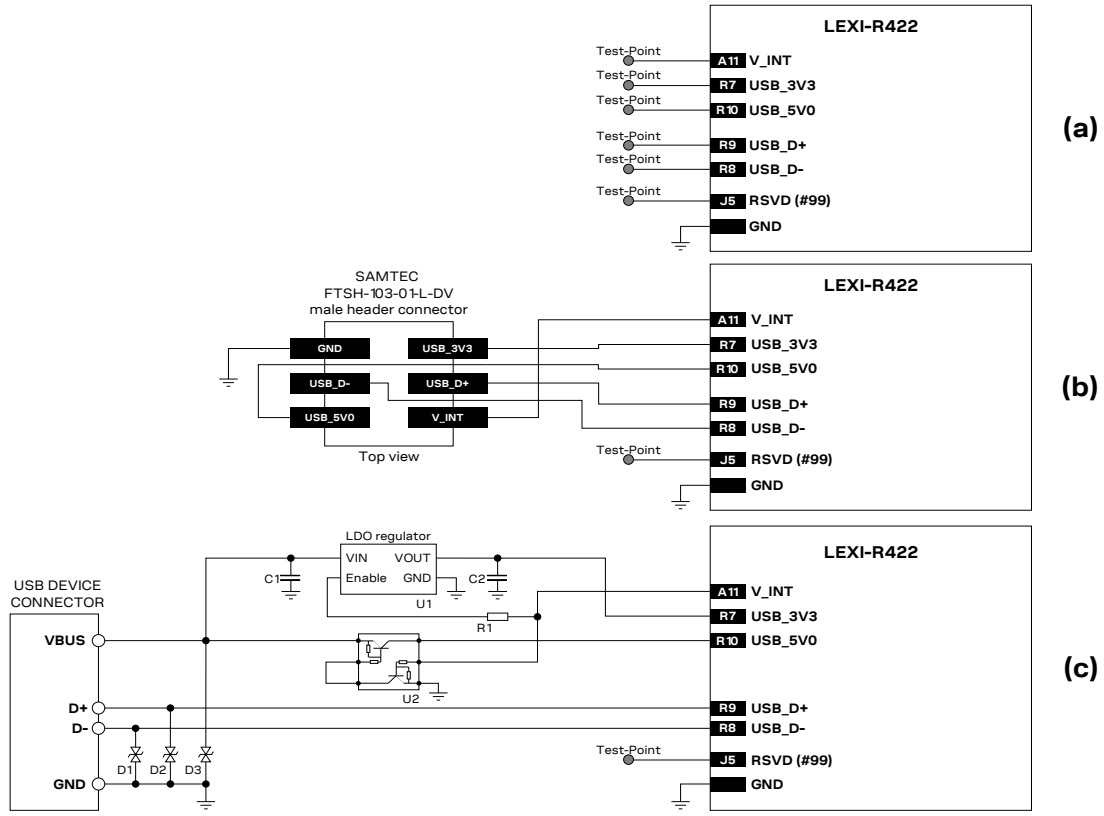

Figure 56: USB Interface application circuits for LEXI-R422 modules

Reference	Description	Part number - Manufacturer
C1, C2	1 µF capacitor ceramic X7R 16 V	Generic manufacturer
D1, D2, D3	Very low capacitance ESD protection	PESD0402-140 - Littelfuse
R1	10 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1	LDO linear regulator 3.3 V 150 mA	NCP600SN330T1G - ON Semiconductor
U2	NPN/PNP 10k/47k biased silicon transistor	BCR35PN - Infineon Technologies

Table 35: Components for USB application circuits for LEXI-R422 modules

2.6.2.2 Guidelines for USB layout design

The **USB_D+** / **USB_D-** lines require accurate layout design to achieve reliable signaling at the high speed data rate (up to 480 Mb/s) supported by the USB serial interface.

The characteristic impedance of **USB_D+** / **USB_D-** lines is specified by the USB 2.0 specification [4]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if PCB layout is not optimal, especially when the USB signaling lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route **USB_D+** / **USB_D-** lines as a differential pair
- Route **USB_D+** / **USB_D-** lines as short as possible
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω
- Use design rules for **USB_D+** / **USB_D-** as RF transmission lines, being them coupled differential micro-strip or buried stripline: avoid stubs, abrupt change of layout, and route on clear PCB area

Figure 57 and Figure 58 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

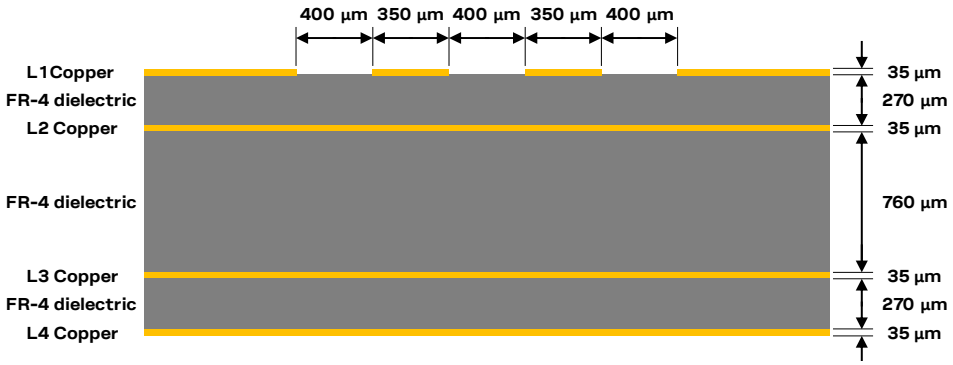

Figure 57: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 4-layer board layup

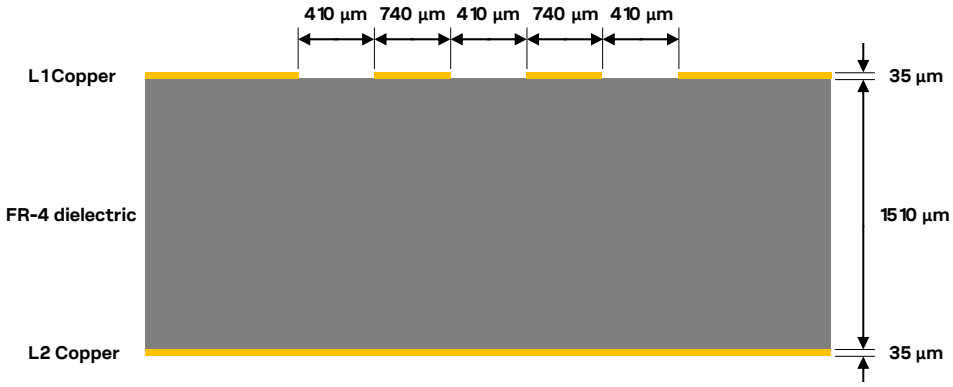

Figure 58: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 2-layer board layup

2.6.3 I2C interface

2.6.3.1 Guidelines for I2C circuit design

The I2C-bus host interface can be used to communicate with u-blox GNSS receivers and other external I2C-bus devices.

The **SDA** and **SCL** pins of the module are open drain output as per I2C bus specifications [9], and they have internal pull-up resistors to the **V_INT** 1.8 V supply rail of the module, so there is no need of additional pull-up resistors on the external application board.

☞ Capacitance and series resistance must be limited on the bus to match the I2C specifications (maximum proper rise time for **SCL** / **SDA** lines is 1.0 µs): route connections as short as possible.

☞ ESD sensitivity rating of the I2C pins is 1 kV (HBM according to JS-001-2017). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

☞ If the pins are not used as I2C bus interface, they can be left unconnected.

Connection with u-blox 1.8 V GNSS receivers

Figure 59 shows an application circuit for connecting the cellular module to an external u-blox 1.8 V GNSS receiver:

- The **SDA** and **SCL** pins of the cellular module are directly connected to the related pins of the u-blox 1.8 V GNSS receiver. External pull-up resistors are not needed, as they are already integrated in the cellular module.
- The **GPIO2** pin is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 1.8 V GNSS receiver providing the “GNSS supply enable” function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the cellular module is switched off or in the reset state.
- The **GPIO3** pin is connected to the **TxD** pin of the u-blox 1.8 V GNSS receiver providing the additional “GNSS Tx data ready” function.

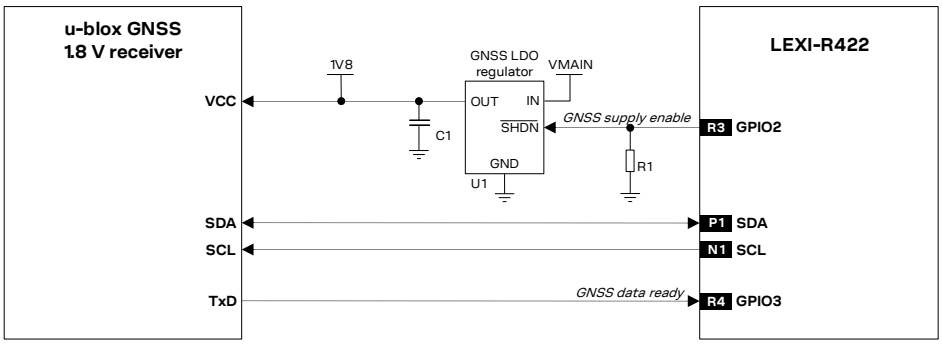

Figure 59: Application circuit for connecting LEXI-R422 modules to u-blox 1.8 V GNSS receivers

Reference	Description	Part number - Manufacturer
R1	47 kΩ resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
U1	Voltage regulator for GNSS receiver	See GNSS receiver hardware integration manual

Table 36: Components for connecting LEXI-R422 modules to u-blox 1.8 V GNSS receivers

☞ For additional guidelines regarding the design of applications with u-blox 1.8 V GNSS receivers, see the hardware integration manual of the u-blox GNSS receivers.

☞ For additional guidelines regarding cellular and GNSS RF coexistence, see section 2.4.2

Connection with u-blox 3.0 V GNSS receivers

Figure 60 shows an application circuit for connecting the cellular module to an external u-blox 3.0 V GNSS receiver:

- As the **SDA** and **SCL** pins of the cellular module are not tolerant up to 3.0 V, the connection to the related I2C pins of the u-blox 3.0 V GNSS receiver must be provided using a suitable I2C-bus bidirectional voltage translator (e.g. TI TCA9406, which additionally provides the partial power down feature so that the GNSS 3.0 V supply can be ramped up before the **V_INT** 1.8 V cellular supply). External pull-up resistors are not needed on the cellular module side, as they are already integrated in the cellular module.
- The **GPIO2** is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 3.0 V GNSS receiver providing the "GNSS supply enable" function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the cellular module is switched off or in the reset state.
- The **GPIO3** pin is connected to the **TxD** pin of the u-blox 3.0 V GNSS receiver providing the additional "GNSS Tx data ready" function, using a suitable unidirectional general purpose voltage translator (e.g. TI SN74AVC2T245, which additionally provides the partial power down feature so that the 3.0 V GNSS supply can be also ramped up before the **V_INT** 1.8 V cellular supply.

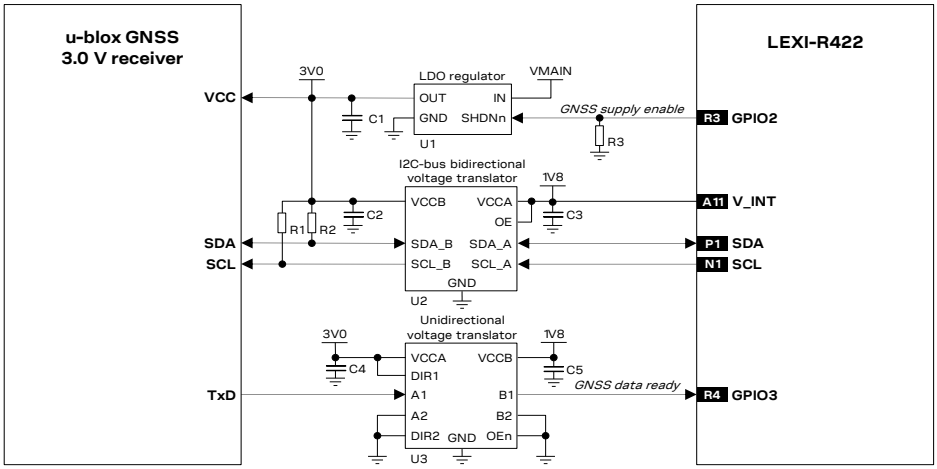

Figure 60: Application circuit for connecting LEXI-R422 modules to u-blox 3.0 V GNSS receivers

Reference	Description	Part number - Manufacturer
R1, R2	4.7 kΩ resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3, C4, C5	100 nF capacitor ceramic X5R 0402 10% 10V	GRM155R71C104KA01 - Murata
U1, C1	Voltage regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver hardware integration manual
U2	I2C-bus bidirectional voltage translator	TCA9406DCUR - Texas Instruments
U3	Generic unidirectional voltage translator	SN74AVC2T245 - Texas Instruments

Table 37: Components for connecting LEXI-R422 modules to u-blox 3.0 V GNSS receivers

☞ For additional guidelines regarding the design of applications with u-blox 3.0 V GNSS receivers, see the hardware integration manual of the u-blox GNSS receivers.

☞ For additional guidelines regarding celluar and GNSS RF coexistence, see section 2.4.2

2.6.3.2 Guidelines for I2C layout design

The I2C serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.7 General purpose input / output

2.7.1 Guidelines for GPIO circuit design

A typical usage of LEXI-R422 modules GPIOs can be the following:

- Network indication provided over **GPIO1** pin (see Figure 61 / Table 38 below)
- GNSS supply enable function provided by the **GPIO2** pin (see section 2.6.3)
- GNSS Tx data ready function provided by the **GPIO3** pin (see section 2.6.3)
- Module operating status indication provided by a **GPIO** pin (see section 1.6.1)
- SIM card detection provided over **GPIO6** pin (see Figure 45 / Table 29 in section 2.5)
- Antenna dynamic tuning function provided by **RFCTRL1** and **RFCTRL2** pins (see section 2.4.4)

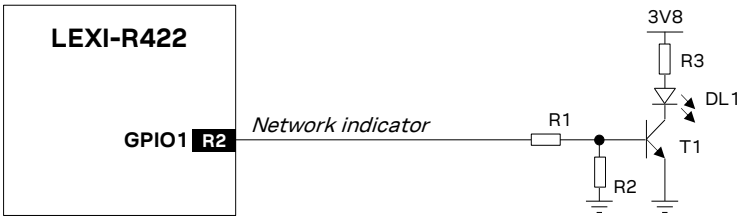

Figure 61: Application circuit for network indication provided over GPIO1

Reference	Description	Part number - Manufacturer
R1	10 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	820 Ω resistor 0402 5% 0.1 W	Generic manufacturer
DL1	LED red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT transistor	BC847 - Infineon

Table 38: Components for network indication application circuit

- Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of LEXI-R422 modules.
- Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply, which is the **V_INT** supply of the module.
- ESD sensitivity rating of the GPIO pins is 1 kV (HBM according to JS-001-2017). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.
- If the GPIO pins are not used, they can be left unconnected on the application board.

2.7.2 Guidelines for general purpose input/output layout design

The general purpose inputs / outputs pins are generally not critical for layout.

2.8 Reserved pins (RSVD)

LEXI-R422 modules have pins reserved for future use, marked as **RSVD**, which can all be left unconnected on the application board, except for the **RSVD** pin number **99** (also identified as J5), which is recommended to be externally accessible by connecting it to a dedicated Test-Point.

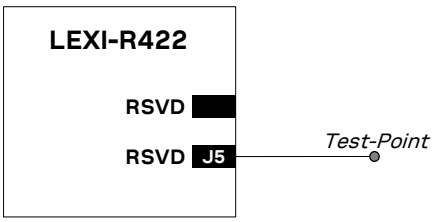

Figure 62: Application circuit for RSVD pins

☞ It is highly recommended to provide accessible test point directly connected to the **RSVD #99** (J5) pin for diagnostic purposes (see Figure 62).

☞ It is also highly recommended to provide access to the **V_INT**, **PWR_CTRL**, **USB_5V0**, **USB_3V3**, **USB_D+**, **USB_D-** pins for FW update and/or for diagnostic purposes, making available accessible dedicated Test-Points directly connected to each of these pins, or making available a dedicated connector / circuit (see Figure 56).

2.9 Module placement

An optimized placement allows a minimum RF line's length and closer path from DC source for **VCC**.

Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce electro-magnetic interference that affects the module, analog parts and RF circuits performance. Implement suitable countermeasures to avoid any possible electro-magnetic compatibility issue.

Make sure that the module is placed in order to keep the antenna as far as possible from VCC supply line and related parts (refer to Figure 27), from high speed digital lines (as USB) and from any possible noise source.

Provide enough clearance between the module and any external part: clearance of at least 0.4 mm per side is recommended to let suitable mounting of the parts.

☞ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the LEXI-R422 modules: avoid placing temperature sensitive devices close to the module.

2.10 Module footprint and paste mask

Figure 63 describes the suggested footprint (i.e. copper mask) and paste mask layout for LEXI-R422 modules: the proposed land pattern layout and the proposed stencil apertures layout reflect the modules pads layout described in the LEXI-R422 data sheet [1].

The recommended thickness of the stencil for the soldering paste is 130 µm, according to application production process requirements.

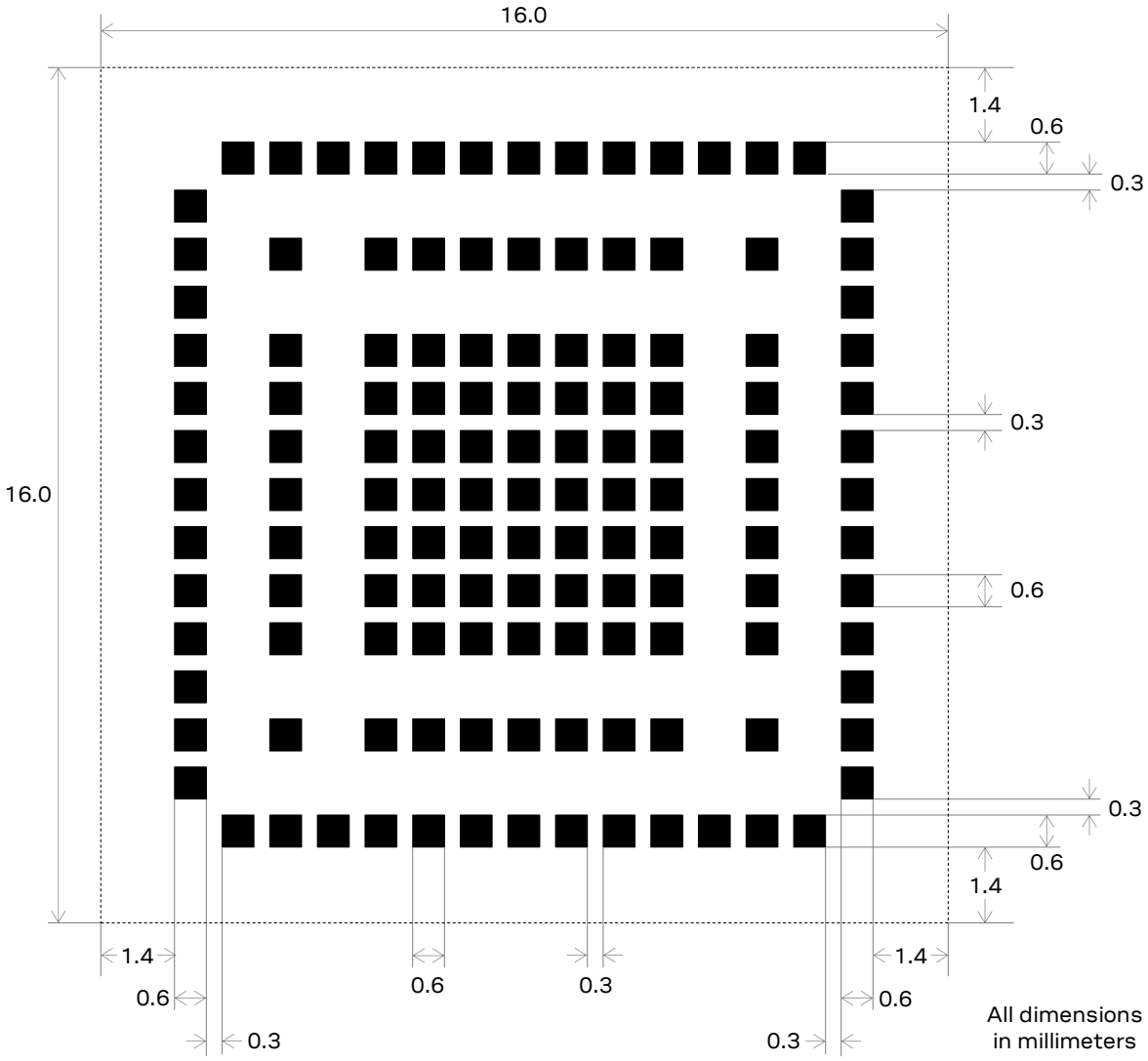

Figure 63: Suggested footprint and paste mask for LEXI-R422 modules (application board top view)

☞ These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) implemented.

2.11 Thermal guidelines

☞ The module operating temperature range is specified in the LEXI-R422 data sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload in connected mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks (for example, see the Terminal Tx Power distribution for WCDMA, taken from operation on a live network, described in the GSMA TS.09 Official Document [10]); however the application should be correctly designed to cope with it.

During transmission at maximum RF power the LEXI-R422 modules generate thermal power that may exceed 0.5 W: this is an indicative value since the exact generated power strictly depends on operating condition such as the actual antenna return loss, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition. The overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

☞ The Module-to-Ambient thermal resistance value and the relative increase of module temperature will differ according to the specific mechanical deployments of the module, e.g. application PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of the thermal dissipation, i.e. the reduction of the Module-to-Ambient thermal resistance, will decrease the temperature of the modules internal circuitry for a given operating ambient temperature. This improves the device long-term reliability in particular for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each **GND** pin with solid ground layer of the application PCB and connect each ground area of the multilayer application PCB with complete thermal via stacked down to main ground layer.
- Provide a ground plane as wide as possible on the application board.
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the application.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.

Beside the reduction of the Module-to-Ambient thermal resistance implemented by correct application hardware design, the increase of module temperature can be moderated by a correspondingly correct application software implementation:

- Enable power saving configuration using the +CPSMS AT command
- Enable module connected mode for a given time period and then disable it for a time period long enough to adequately mitigate the temperature increase.

2.12 Schematic for LEXI-R422 modules integration

Figure 64 is an example of a schematic diagram where a LEXI-R422 module is integrated into an application board using almost all available interfaces and functions.

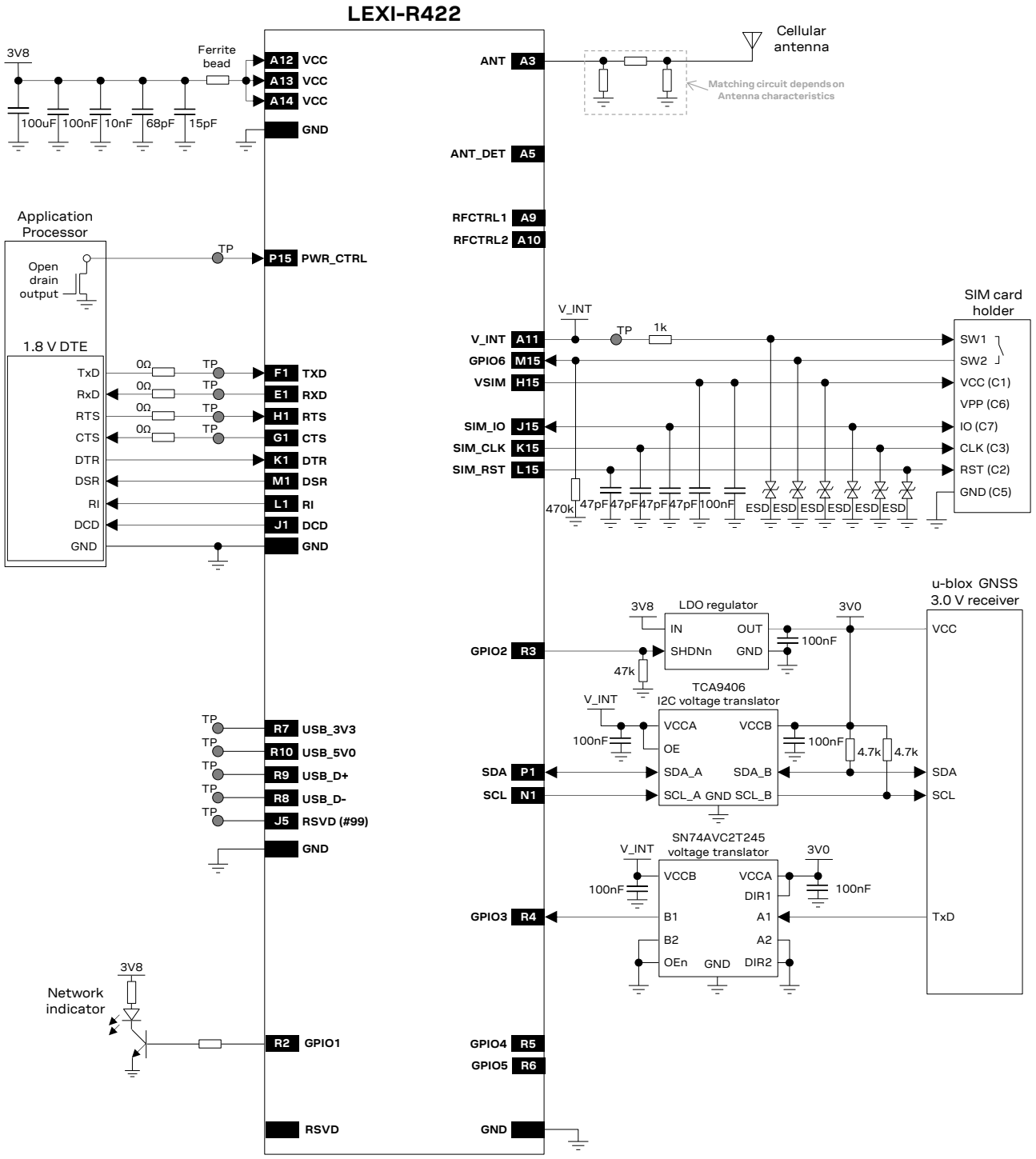

Figure 64: Example of schematic diagram to integrate a LEXI-R422 module using all available interfaces

2.13 Design-in checklist

This section provides a design-in checklist.

2.13.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting the highest peak / pulse current consumption values and the maximum averaged current consumption values in connected mode, as specified in the LEXI-R422 data sheet [1].
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, as the modules signal names follow the ITU-T V.24 recommendation [5].
- ☑ Capacitance and series resistance must be limited on each high speed line of the USB interface.
- ☑ It is strongly recommended to provide accessible test points directly connected to the **V_INT**, **PWR_CTRL**, **USB_5V0**, **USB_3V3**, **USB_D+**, **USB_D-**, and **RSVD #99** pins for diagnostic and/or FW update purposes.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide adequate precautions for EMC / ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of LEXI-R422 modules before the switch-on of the generic digital interface supply source (**V_INT**).
- ☑ All unused pins can be left unconnected.

2.13.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** port (antenna RF interface).
- ☑ Check cellular antenna trace design for regulatory compliance perspective (see section 4.2 for FCC United States, and related section 2.4.1.6).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (SIM signals, high-speed digital lines such as USB, and other data lines).
- ☑ Optimize placement for minimum length of RF line.
- ☑ Check the footprint and paste mask designed for the LEXI-R422 module as illustrated in section 2.10.
- ☑ **VCC** line should be enough wide and as short as possible.

- ☑ Route **VCC** supply line away from RF line / part (refer to Figure 27) and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picoFarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Ensure an optimal grounding connecting each **GND** pin with application board solid ground layer.
- ☑ Use as many vias as possible to connect the ground planes on multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along RF and high speed lines.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.
- ☑ Ensure appropriate RF precautions for the GNSS and cellular technologies coexistence.

2.13.3 Antenna checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement, as reported in section 4.2 for FCC United States, in section 4.3 for ISED Canada, in section 4.4 for CE Europe, in section 4.5 for UKCA Great Britain, etc.
- ☑ Ensure high isolation between the cellular antenna and any other antennas or transmitters present on the end device.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to LEXI-R422 reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the LEXI-R422 data sheet [1] and the u-blox package information user guide [16].

3.2 Handling

The LEXI-R422 modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ Ensure ESD precautions are implemented during handling of the module.

Electro-Static Discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of LEXI-R422 modules (considering the Human Body Model according to JS-001-2017 and the Charged Device Model according to JS-002-2018) is specified in LEXI-R422 data sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from the International Electrotechnical Commission (IEC) or the American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be considered whenever handling the LEXI-R422 modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect the ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in a non-ESD protected work area, implement adequate ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD-safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

"No Clean" soldering paste is strongly recommended for LEXI-R422 modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper) 95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	217 °C
Stencil Thickness:	130 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.10.

☞ The quality of the solder joints should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type soldering oven is strongly recommended for LEXI-R422 modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the “IPC-7530A Guidelines for temperature profiling for mass soldering (reflow and wave) processes”.

Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s
  If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 – 120 s
  If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End temperature: +150 - +200 °C
  If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 - 60 s
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

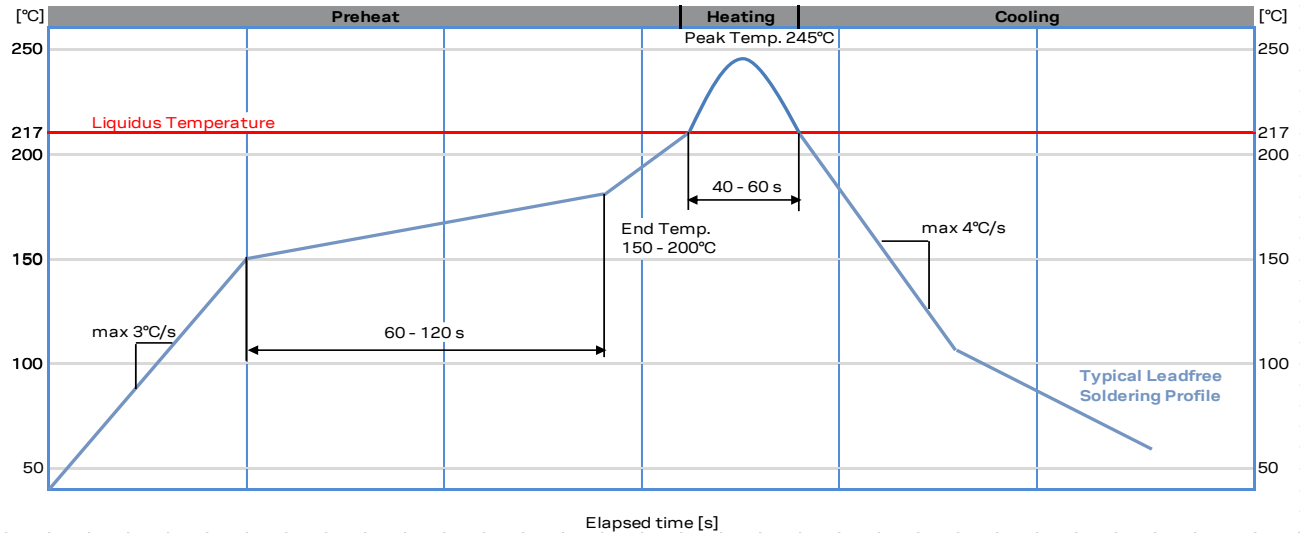

Figure 65: Recommended soldering profile

The modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the module, inspect it optically to verify that it is correctly aligned and centered.

3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside-down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ u-blox gives no warranty against damages to the LEXI-R422 modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the LEXI-R422 module, plus one reflow soldering process to mount other parts).

3.3.6 Wave soldering

LEXI-R422 LGA modules must not be soldered with a wave soldering process.

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for a board with a LEXI-R422 module already populated on it.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ u-blox gives no warranty against damages to the LEXI-R422 modules caused by performing more than a total of two soldering processes (one reflow soldering process to mount the LEXI-R422 module, plus one wave soldering process to mount other THT parts on the application board).

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the HF properties of the cellular modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interference and noise.

☞ u-blox gives no warranty for damages to the cellular modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

The cellular modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the cellular modules caused by any ultrasonic processes.

4 Approvals

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called “certification schemes”, which can be divided into:

- Regulatory certifications
  - Country-specific approval required by local government in most regions and countries, as:
    - CE (European Conformity) marking for European Union
    - FCC (Federal Communications Commission) approval for the United States
- Industry certifications
  - Telecom industry-specific approval verifying interoperability between devices and networks:
    - GCF (Global Certification Forum)
    - PTCRB (PCS Type Certification Review Board)
- Operator certifications
  - Operator-specific approvals required by some mobile network operator, such as:
    - AT&T network operator in United States
    - Verizon Wireless network operator in United States

Manufacturers of end-devices integrating a LEXI-R422 module must take care of all certification approvals required by the specific integrating device to be deployed in the market.

The required certification scheme approvals and relative testing specifications applicable to the end-device that integrates a LEXI-R422 module differ depending on the country or the region where the integrating device is intended to be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device is intended to operate.

☞ Check appropriate applicability of LEXI-R422 module’s approvals while starting the certification process of the device integrating the module: the re-use of the u-blox cellular module’s approval can significantly reduce the cost and time to market of the application device certification.

☞ For the complete list and specific details about LEXI-R422 module’s approvals, see the LEXI-R422 data sheet [1], or contact the u-blox office or sales representatives.

LEXI-R422 modules include the capability to configure the device by selecting the operating mobile network operator profile, radio access technology, and bands. In the AT commands manual [2], see the +UMNOPROF, +URAT, and +UBANDMASK AT commands. As these configuration decisions are made, u-blox reminds manufacturers of the end-device integrating the LEXI-R422 modules to take care of compliance with all the certification approvals requirements applicable to the specific integrating device to be deployed in the market.

☞ It is strongly recommended to configure the module to the applicable MNO profile, RAT, and LTE bands intended for the application device and within regulatory compliance.

☞ The certification of the application device that integrates a LEXI-R422 module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

☞ Check the specific settings required for mobile network operators approvals as they may differ from the AT commands settings defined in the module as integrated in the application device.

☞ For further guidelines about certification of end-devices integrating a LEXI-R422 module, see the application development guide application note [3].

4.2 US Federal Communications Commission notice

FCC ID of LEXI-R422 modules: XPYUBX22VA03

4.2.1 Integration instructions for host product manufacturers

This chapter includes the LEXI-R422 cellular modules' integration instructions for host product manufactures according to FCC KDB 996369 D03 v01r01. General FCC guidelines for host product manufactures integrating transmitter modules are available in the FCC KDB 996369 D04 v02.

4.2.1.1 List of applicable FCC / ISED rules

FCC United States	ISED Canada
47 CFR Part 22 / 24 / 27 / 90	RSS-130, RSS-132, RSS-133, RSS-139

Table 39: List of FCC / ISED rules applicable to LEXI-R422 modules

The LEXI-R422 modular transmitter is only FCC authorized for the specific rule parts listed on the FCC grant. The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. See section 4.2.1.9 below regarding additional testing for the host product.

4.2.1.2 Specific operational use conditions

Host product manufacturers are responsible for following all the integration guidelines included in this manual, and to perform a set of verification testing to ensure the host product complies with any applicable functional and/or conformity requirements.

LEXI-R422 modular transmitter must be supplied with operating voltage and current rating specified in the LEXI-R422 data sheet [1].

LEXI-R422 modular transmitter is an equipment for building-in. Requirements for fire enclosure must be evaluated in the host end product. No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed.

See RF exposure considerations section 4.2.1.5 below for fixed, mobile, and portable use conditions, operation in conjunction with any other transmitter, and maximum gain of the system antenna.

Changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Host product manufacturers are responsible to include any applicable restrictions imposed by FCC rules, any other applicable notices, or regulatory statements in host's manual for the end-user.

4.2.1.3 Limited module procedures

Not applicable, as LEXI-R422 modular transmitter is granted with FCC Single Modular Approval rather than a Limited Single Modular Approval.

4.2.1.4 Trace antenna designs

Manufacturers of mobile or fixed devices incorporating the LEXI-R422 modular transmitter are authorized to use the FCC Grant of the module for their own host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host printed circuit board used for regulatory type approvals of the modular transmitter described in details in section 2.4.1.6.

Other additional guidelines for RF design are available in section 1.7.1 and the whole section 2.4.

Guidelines regarding test procedures for design verification and validation with the aim of ensuring compliance with any applicable functional and/or conformity requirements are included in section 5.1.

Guidelines regarding production test procedures are included in section 5.2.

In case of antenna trace design change, an FCC Class II Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by an FCC Class II Permissive Change application.

4.2.1.5 RF exposure considerations

LEXI-R422 modular transmitter complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. Manufacturers of mobile or fixed devices incorporating the modular transmitter are authorized to use the FCC Grants of the modular transmitter for their own final products according to the conditions referenced in the certificates.

LEXI-R422 modular transmitter should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. Manufacturers of portable applications incorporating LEXI-R422 modules are required to have their final product evaluated and tested, applying for their own FCC Grant related to the specific portable device, or executing an FCC Class II Permissive Change application. This is mandatory to meet the SAR requirements for portable devices, with the modular transmitter installed in host products intended to be operated with less than 20 cm between the radiator and the body of the user or nearby persons.

LEXI-R422 modular transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC procedures and as authorized in the modular transmitter FCC certification filing.

The gain of the system cellular antenna(s) used for the LEXI-R422 modular transmitter (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value specified in the FCC Grant for mobile and/or fixed operating configurations

4.2.1.6 Antennas

LEXI-R422 surface-mounted LGA modular transmitter includes the **ANT** pad, consisting in the RF port of the module that can be connected through an RF antenna trace designed on the host PCB to any antenna compliant with any appliable rules for RF exposure or any other.

4.2.1.7 Label and compliance information

If the FCC Grant of the LEXI-R422 modular transmitter can be used for the final host product, as the conditions referenced in the certificates and in this chapter 4.2.1 are met, the FCC Label of the module shall be visible from the outside, or the host device shall bear a second label stating:

"Contains FCC ID: XPYUBX22VA03"

See the general FCC guidelines for labeling and other information required to be provided to users of RF devices available in the KDB Publication 784748.

4.2.1.8 Information on test modes and additional testing requirements

The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. Compliance of the host product with RF regulatory rules defined by the FCC can be verified using a radio communication tester (callbox), as for example the Rohde & Schwarz CMW500, or any equivalent equipment for multi-radio technology signaling conformance tests. Test modes should also take into consideration different operational conditions for a stand-alone modular transmitter in a host product, as well as for multiple simultaneously transmitting modules or other transmitters co-located in a host product. Consider involving an accredited testing laboratory to verify compliance with RF regulatory rules.

Additional guidance for testing host products is given in the FCC KDB Publication 996369 D04.

4.2.1.9 Additional testing, Part 15 Subpart B disclaimer

LEXI-R422 modular transmitter is only FCC authorized for the specific rule parts listed on the FCC grant (see section 4.2.1.1). The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

This device complies with Part 15 of the FCC rules Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

Part 15 limits of the FCC Rules for a Class B digital device are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the device into an outlet on a circuit different from that to which the receiver is connected
- Consultant the dealer or an experienced radio/TV technician for help

LEXI-R422 modular transmitter is Part 15 Subpart B compliant, but the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

4.3 Innovation, Science, Economic Development Canada notice

ISED Canada Certification Number of LEXI-R422 modules: 8595A-UBX22VA03

4.3.1 Declaration of Conformity

This device complies with the ISED Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

- This device may not cause harmful interference.
- This device must accept any interference received, including interference that may cause undesired operation.

⚠ Radiofrequency radiation exposure information: this equipment complies with the radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for the LEXI-R422 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value stated in the ISED Canada Grant for mobile and fixed or mobile operating configurations

4.3.2 Modifications

ISED Canada requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating the LEXI-R422 modules are authorized to use the ISED Canada Certificates of the LEXI-R422 modules for their own final products according to the conditions referenced in the certificates.

⚠ The ISED Canada Label shall in the above case be visible from the outside, or the host device shall bear a second label stating: "Contains IC: 8595A-UBX22VA03"

⚠ **Innovation, Science and Economic Development Canada (ISED) Notices**

This Class B digital apparatus complies with Canadian CAN ICES-3(B) / NMB-3(B).
Operation is subject to the following two conditions:

- this device may not cause interference
- this device must accept any interference, including interference that may cause undesired operation of the device

Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Cellular Module is below the Innovation, Science and Economic Development Canada (ISED) radio frequency exposure limits. The u-blox Cellular Module should be used in a manner such that the potential for human contact during normal operation is minimized.
This device has been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).
This device has been certified for use in Canada. Status of the listing in the Industry Canada's REL (Radio Equipment List) can be found at the following web address:
http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng
Additional Canadian information on RF exposure also can be found at the following web address:
http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

⚠ IMPORTANT: Manufacturers of portable applications incorporating the LEXI-R422 modules are required to have their final product certified and apply for their own Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

⚠ **Avis d'Innovation, Sciences et Développement économique Canada (ISDE)**

Cet appareil numérique de classe B est conforme aux normes canadiennes CAN ICES-3(B) / NMB-3(B). Son fonctionnement est soumis aux deux conditions suivantes:

- cet appareil ne doit pas causer d'interférence
- cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans-fil u-blox Cellular Module est inférieure à la limite d'exposition aux fréquences radio d'Innovation, Sciences et Développement économique Canada (ISDE). Utilisez l'appareil de sans-fil u-blox Cellular Module de façon à minimiser les contacts humains lors du fonctionnement normal.
Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des

conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).
Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur: http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra
Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur: http://www.ic.gc.ca/eic/site/smt-gst.nsf/fra/sf08792.html

⚠ IMPORTANT: les fabricants d'applications portables contenant les modules de la LEXI-R422 doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat ISDE Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.
Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

4.4 European Conformance CE mark

LEXI-R422 radio modules have been evaluated against the essential requirements of the Radio Equipment Directive 2014/53/EU.

In order to satisfy the essential requirements of the 2014/53/EU RED, the modules are compliant with the following standards:

- Radio Spectrum Efficiency (Article 3.2):
  - EN 301 511
  - EN 301 908-1
  - EN 301 908-13
- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1
  - EN 301 489-52
- Health and Safety (Article 3.1a)
  - EN 62368-1
  - EN 62311

⚠ Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for LEXI-R422 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the values reported in the Declaration of Conformity, for mobile and fixed or mobile operating configurations

The conformity assessment procedure for the LEXI-R422 modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU, has been followed.

Thus, the following marking is included in the product:

CE

4.5 UK Conformity Assessed (UKCA)

☞ The United Kingdom is made up of the Great Britain (including England, Wales and Scotland) and the Northern Ireland. The Northern Ireland continues to accept the CE marking. Following notice is applicable to the Great Britain only.

LEXI-R422 radio modules have been evaluated against the essential requirements of the Radio Equipment Regulations 2017 (SI 2017 No. 1206, as amended by SI 2019 No. 696). To satisfy the essential requirements of the UK Legislation, the modules are compliant with the following standards:

- Radio Spectrum Efficiency (Article 6.2):
  - EN 301 511
  - EN 301 908-1
  - EN 301 908-13
- Electromagnetic Compatibility (Article 6.1b):
  - EN 301 489-1
  - EN 301 489-52
- Health and Safety (Article 6.1a)
  - EN 62368-1
  - EN 62311

⚠ Radiofrequency radiation exposure information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for LEXI-R422 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the values reported in the Declaration of Conformity, for mobile and fixed or mobile operating configurations

The conformity assessment procedure for the modules, referred to Part 3 of the Radio Equipment Regulations 2017, has been followed.

Guidance about using the UKCA marking: https://www.gov.uk/guidance/using-the-ukca-marking

UK CA

5 Product testing

5.1 Validation testing and qualification

LEXI-R422 modules are validated and tested by u-blox in the operating conditions and in certain integration, but not all the specific characteristics of the host application end-product integrating the module can be validated and tested by u-blox.

LEXI-R422 modules are also qualified by u-blox according to u-blox reliability stress tests policy, based on the AEC-Q104 standard, but the specific characteristics of the host application end-product integrating the module cannot be qualified by u-blox.

Therefore, and to be on the safe side, u-blox recommends integrators of LEXI-R422 modules to validate, verify, qualify and test in details the host product integrating the SMD module considering all the possible aspects, to make sure that the specific characteristics of the host application do not lead to reduced / non-performance of LEXI-R422 modules.

Host product manufacturers are responsible to follow all the integration guidelines included in this manual, and to perform a set of verification testing to ensure the host end-product complies with applicable functional and/or conformity requirements.

Care has to be taken in the validation of the antennas RF circuits implemented in the host product for the module, as they may affect compliance with applicable RF conformity requirements.

The 50 Ω characteristic impedance of the antenna trace design on a host printed circuit board can be verified using a Vector Network Analyzer, as done on the u-blox host PCB, with calibrated RF coaxial cable soldered at the pad corresponding to RF input/output of the module and with the transmission line terminated to a 50 Ω load at the 50 Ω SMA female connector.

Compliance of the design with RF regulatory rules defined by the FCC, ISED, RED, etc. can be verified using a radio communication tester (callbox) as the Rohde & Schwarz CMW500, or any equivalent equipment for multi-technology signaling conformance tests.

Care has to be taken in the validation of the VCC power supply circuit implemented in the host product for the module, as the specific characteristics of the power supply circuit may affect compliance with applicable functional and/or conformity requirements.

Adequateness of the power supply circuit capability can be checked by forcing the module to transmit at the maximum power level in the supported radio access technologies using a radio communication tester (callbox) as the Rohde & Schwarz CMW500 or any equivalent equipment.

Care has to be taken in the validation of the SIM interface circuit implemented in the host product for the module, checking in particular rise times of the signals, as the external circuit design may affect compliance with applicable functional and/or specification requirements.

Care has to be taken in the validation of any interface circuit connected to the module as implemented in the host product, checking in particular the power-on, power-off and reset circuits with also any related switch-on, switch-off and reset procedure, the communication interfaces (as UARTs, USB, I2C), and any other circuit designed in the host product in combination with any other interface of the module (as GPIOs, etc.), as the external design implemented in the host product may affect compliance with applicable functional requirements.

☞ The validation, verification, qualification, and testing of the application host device integrating a LEXI-R422 module and the compliance of the application host device with all the applicable functional and/or conformity specifications and requirements are under the sole responsibility of the application host device manufacturer.

5.2 Production testing

5.2.1 u-blox in-line production tests

u-blox focuses on high quality for its products. All units produced are tested automatically in all their interfaces along the production line. Stringent quality control processes have been implemented in the production line. Defective units are analyzed in detail to improve production quality.

This is achieved with automatic test equipment (ATE) in the production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. The Figure 66 illustrates the typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests.

- Digital self-test (firmware download, flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of the reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of the RF characteristics after calibration (i.e. modulation, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

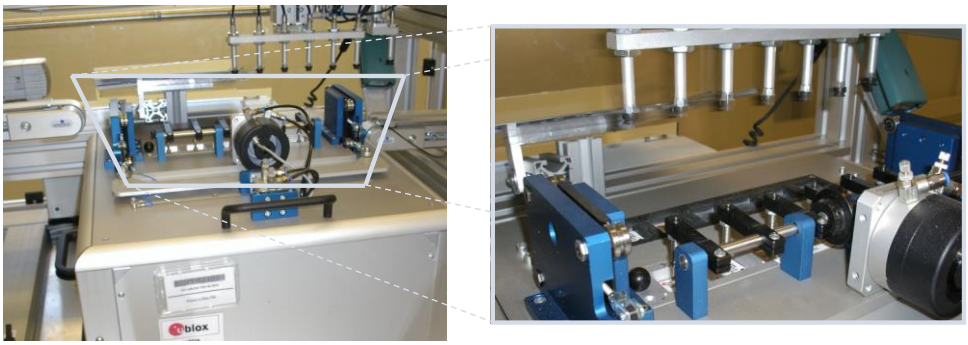

Figure 66: Automatic test equipment for module tests

5.2.2 Production test parameters for OEM manufacturers

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat the firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - The soldering and handling process did not damage the module components
  - All module pins are well soldered on the device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with the host controller can be established
  - The interfaces between the module and device are working
  - The RF interfaces of the device including the antennas are working

Dedicated tests can be implemented to check the device. For example, the consumption measured in a specified status can help detect a short circuit if compared with a “Golden Device” result.

In addition, module AT commands can be used to perform functional tests on the digital interfaces. For example (for more details about AT commands, see the AT commands manual [2]):

- Communication with the host controller can be checked by AT command
- Communication with the SIM card/chip can be checked using the dedicated +CPIN read command
- Communication with external I2C devices can be checked using dedicated I2C AT commands
- GPIO functionality can be checked using the dedicated +UGPIOC AT command, etc.

Please contact the u-blox office or sales representative nearest you for further guidelines about OEM production testing guidelines.

5.2.2.1 "Go/No go" production tests for integrated devices

A "Go/No go" test is typically used to compare the signal quality with a "Golden Device" in a location with excellent network coverage and known signal quality. This test should be performed after the data connection has been established. AT+CSQ is the typical AT command used to check signal quality in term of RSSI. See the AT command manual [2] for detail usage of the AT command.

☞ These kinds of test may be useful as a "go/no go" test but not for RF performance measurements.

This test is suitable to check the functionality of communications with the host controller, the SIM , and the power supply. It can also verify if parts at the antenna interface are well soldered.

5.2.2.2 Persistent configurations

The modules are delivered by u-blox with predefined factory-programmed settings that can be changed using AT commands according to application-specific requirements. Some settings are persistent, stored in the module's non-volatile memory, and re-used at any subsequent reboot. Among these, for example, there are the UART interfaces baud rate, frame format, flow control, etc., the greeting text, the MNO profile, the APN for Internet connectivity, etc. For more details, see the AT command manual [2].

After verifying the proper assembly of the module and related parts on the application device, execute a persistent configuration setting phase in OEM production line, configuring the module according to the intended use in the specific application, as the persistent configurations are intended to be set only once and then re-used at any subsequent reboot.

During the persistent configuration setting phase, it is recommended to configure the baud rate, frame format, flow control and any other settings for the serial UART interfaces according to the use case. It is also recommended to configure the greeting text, the MNO profile and the APN for internet connectivity, etc.. For more details and guidelines regarding persistent configurations of user settings, see the LEXI-R422 application development guide [3].

Appendix

A Migration from SARA-R42 series modules

SARA-R42 series modules (26 x 16 mm, 96-pin LGA), consisting of the SARA-R422, SARA-R422S, SARA-R422M8S and SARA-R422M10S modules, and LEXI-R422 modules (16 x 16 mm, 133-pin LGA) have a different form-factor, but they integrate the same key internal components, offering the same electrical characteristics and allowing the use of the same external circuits.

Therefore, migrating from SARA-R42 series to LEXI-R422 modules is a straightforward procedure that allows integrators to take maximum advantage of their hardware and software investments.

Due to the different form-factor of the modules, the various interfaces and functions are in different layout positions on the LGA pads of the modules.

The pin assignment comparison SARA-R42 series to LEXI-R422 modules, with remarks for migration, is illustrated in the following Table 40.

SARA-R42 series		LEXI-R422 module			
No	**Name**	**ID**	**No**	**Name**	**Remark for migration**
1	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
2	USB_3V3	R7	19	USB_3V3	Same 3.3 V (typical) USB supply input function / characteristics
3	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
4	V_INT	A11	43	V_INT	Same 1.8 V generic digital interfaces supply output function / characteristics
5	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
6	DSR	M1	11	DSR	Same UART DSR input and AUX UART flow ctrl input function / characteristics
7	RI	L1	10	RI	Same UART RI output and AUX UART flow ctrl output function / characteristics
8	DCD	J1	8	DCD	Same UART DCD output and AUX UART data output function / characteristics
9	DTR	K1	9	DTR	Same UART DTR input and AUX UART data input function / characteristics
10	RTS	H1	7	RTS	Same UART HW flow control input function / characteristics
11	CTS	G1	6	CTS	Same UART HW flow control output function / characteristics
12	TXD	F1	5	TXD	Same UART data input function / characteristics
13	RXD	E1	4	RXD	Same UART data output function / characteristics
14	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
15	PWR_CTRL	P15	27	PWR_CTRL	Same power-on/off control input function / characteristics
16	GPIO1	R2	14	GPIO1	Same GPIO function / characteristics
17	USB_5V0	R10	22	USB_5V0	Same 5 V (typical) USB detection input function / characteristics
18	RSVD	--	--	--	Leave unconnected
19	GPIO6	R6	18	GPIO5	Same GPIO function / characteristics
20	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
21	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
22	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
23	GPIO2	R3	15	GPIO2	Same GPIO function / characteristics
24	GPIO3	R4	16	GPIO3	Same GPIO function / characteristics
25	GPIO4	R5	17	GPIO4	Same GPIO function / characteristics
26	SDA	P1	13	SDA	Same I2C data input / output function / characteristics
27	SCL	N1	12	SCL	Same I2C clock output function / characteristics
28	USB_D-	R8	20	USB_D-	Same USB data line D- input / output function / characteristics
29	USB_D+	R9	21	USB_D+	Same USB data line D+ input / output function / characteristics

SARA-R42 series		LEXI-R422 module			
No	**Name**	**ID**	**No**	**Name**	**Remark for migration**
30	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
31	ANT_GNSS	--	--	--	No GNSS receiver function supported by LEXI-R422 modules
32	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
33	RSVD	J5	99	RSVD	Same function / characteristics. Provide test point for diagnostic purposes
34	I2S_WA	A10	44	RFCTRL2	Same antenna tuner function / characteristics
35	I2S_TXD	A9	45	RFCTRL1	Same antenna tuner function / characteristics
36	I2S_CLK	--	--	--	No function supported on both SARA-R42 series and LEXI-R422 modules
37	I2S_RXD	--	--	--	No function supported on both SARA-R42 series and LEXI-R422 modules
38	SIM_CLK	K15	31	SIM_CLK	Same clock output for external SIM function / characteristics
39	SIM_IO	J15	32	SIM_IO	Same data input/output for external SIM function / characteristics
40	SIM_RST	L15	30	SIM_RST	Same reset output for external SIM function / characteristics
41	VSIM	H15	33	VSIM	Same supply output for external SIM function / characteristics
42	GPIO5	M15	29	GPIO6	Same GPIO with external SIM detection function / characteristics
43	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
44	ANT_ON	--	--	--	No GNSS receiver function supported by LEXI-R422 modules
45	TIMEPULSE	--	--	--	No GNSS receiver function supported by LEXI-R422 modules
46	EXTINT	--	--	--	No GNSS receiver function supported by LEXI-R422 modules
47	TXD_GNSS	--	--	--	No GNSS receiver function supported by LEXI-R422 modules
48	RSVD	--	--	--	Leave unconnected
49	RSVD	--	--	--	Leave unconnected
50	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
51	VCC	A12	42	VCC	Same internal Power Management Unit supply input function / characteristics
52	VCC	A13	41	VCC	Same internal RF Power Amplifiers supply input function / characteristics
53	VCC	A14	40	VCC	Same internal RF Power Amplifiers supply input function / characteristics
54	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
55	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
56	ANT	A3	51	ANT	Same RF input/output for cellular Rx/Tx antenna function / characteristics
57	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
58	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
59	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
60	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
61	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
62	ANT_DET	A5	49	ANT_DET	Same antenna detection function / characteristics
63	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
64	GND	--	--	--	Several ground pins are available with LEXI-R422 modules
65-96	GND	--	--	--	Several ground pins are available with LEXI-R422 modules

Table 40: Pin assignment of SARA-R42 series and LEXI-R422 modules, with remarks for migration

☞ For more information about SARA-R42 series modules, see the SARA-R4 series data sheet [18], the SARA-R4 series system integration manual [19], and the AT commands manual [2].

B Glossary

Abbreviation	Definition
2G	2nd Generation Cellular Technology (GSM, GPRS, EGPRS)
3G	3rd Generation Cellular Technology (UMTS, HSDPA, HSUPA)
3GPP	3rd Generation Partnership Project
ACMA	Australian Communications and Media Authority
ADC	Analog to Digital Converter
ANATEL	Agência Nacional de Telecomunicações – National Telecommunications Agency (Brazil)
AT	AT Command Interpreter Software Subsystem, or attention
BeiDou	Chinese satellite navigation system
BJT	Bipolar Junction Transistor
C/No	Carrier to Noise ratio
Cat	Category
CE	European Conformity
CSFB	Circuit Switched Fall Back
DC	Direct Current
DCE	Data Communication Equipment
DL	Down-Link (Reception)
DTE	Data Terminal Equipment
EDGE	Enhanced Data rates for GSM Evolution (EGPRS)
eDRX	Extended Discontinuous Reception
EGPRS	Enhanced General Packet Radio Service (EDGE)
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
E-UTRA	Evolved Universal Terrestrial Radio Access
FCC	Federal Communications Commission United States
FDD	Frequency Division Duplex
FOAT	Firmware Over AT commands
FOTA	Firmware Over The Air
FTP	File Transfer Protocol
FW	Firmware
Galileo	European satellite navigation system
GCF	Global Certification Forum
GITEKI	Gijutsu kijun tekigō shōmei – technical standard conformity certification (Japan)
GLONASS	GLObal Navigation Satellite System (Russian satellite navigation system)
GMSK	Gaussian Minimum-Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
HBM	Human Body Model
HTTP	HyperText Transfer Protocol

Abbreviation	Definition
HW	Hardware
I2C	Inter-Integrated Circuit interface
I2S	Inter IC Sound interface
IFT	Federal Telecommunications Institute Mexico
ISED	Innovation, Science and Economic Development Canada
ITU-T	International Telecommunication Union - Telecommunication Standardization Sector
KC	Korean Certification
LDO	Low-Dropout
LGA	Land Grid Array
LPWA	Low Power Wide Area
LTE	Long Term Evolution
LWM2M	Open Mobile Alliance Lightweight Machine-to-Machine protocol
M2M	Machine-to-Machine
MNO	Mobile Network Operator
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MQTT	Message Queuing Telemetry Transport
N/A	Not Applicable
NAS	Non-Access Stratum
NCC	National Communications Commission Taiwan
OEM	Original Equipment Manufacturer device: an application device integrating a u-blox cellular module
OTA	Over The Air
PA	Power Amplifier
PCN	Product Change Notification / Sample Delivery Note / Information Note
PFM	Pulse Frequency Modulation
PICS	Protocol Implementation Conformance Statement
PSM	Power Saving Mode
PTCRB	PCS Type Certification Review Board
PWM	Pulse Width Modulation
RAT	Radio Access Technology
RCM	Regulatory Compliance Mark
RED	Radio Equipment Directive
RF	Radio Frequency
RSSI	Received Signal Strength Indication
RSVD	Reserved
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SI	Statutory Instruments (United Kingdom)
SIM	Subscriber Identification Module
SMA	Sub-Miniature version A
SMD	Surface Mounting Device
SMS	Short Message Service
SRF	Self-Resonant Frequency
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
TIS	Total Isotropic Sensitivity
TP	Test-Point

Abbreviation	Definition
TRP	Total Radiated Power
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UE	User Equipment
UICC	Universal Integrated Circuit Card
UKCA	United Kingdom Conformity Assessed
UL	Up-Link (Transmission)
UMTS	Universal Mobile Telecommunications System
US	United States
USB	Universal Serial Bus
VSWR	Voltage Standing Wave Ratio

Related documentation

[1] u-blox LEXI-R422 data sheet, UBX-22020834
[2] u-blox LEXI-R422 / SARA-R4 series AT commands Manual, UBX-17003787
[3] u-blox LEXI-R422 / SARA-R42 series application development guide, UBX-20050829
[4] Universal Serial Bus revision 2.0 specification, https://www.usb.org/
[5] ITU-T Recommendation V.24 – 02-2000 – List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE), http://www.itu.int/rec/T-REC-V.24-200002-I/en
[6] 3GPP TS 27.007 – AT command set for User Equipment (UE)
[7] 3GPP TS 27.005 – Use of Data Terminal Equipment – Data Circuit terminating; Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[8] 3GPP TS 27.010 – Terminal Equipment to User Equipment (TE-UE) multiplexer protocol
[9] I2C-bus specification and user manual – UM10204 – NXP semiconductors, https://www.nxp.com/docs/en/user-guide/UM10204.pdf
[10] GSM Association TS.09 – Battery Life Measurement and Current Consumption Technique, https://www.gsma.com/newsroom/wp-content/uploads//TS.09-v12.pdf
[11] 3GPP TS 51.010-1 – Mobile Station conformance specification; part 1: conformance specification
[12] 3GPP TS 51.010-2 – Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; part 2: Protocol Implementation Conformance Statement (PICS)
[13] 3GPP TS 36.521-1 – Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; part 1: conformance testing
[14] 3GPP TS 36.521-2 – Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)
[15] 3GPP TS 36.523-2 – Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)
[16] u-blox package information user guide, UBX-14001652
[17] u-blox B36 vehicle tracking blueprint product summary, UBX-20012630
[18] u-blox SARA-R4 series data sheet, UBX-16024152
[19] u-blox SARA-R4 series system integration manual, UBX-16029218

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	30-Jun-2023	fvid	Initial release
R02	06-Oct-2023	sses	Updated LEXI-R422-01B product status to engineering sample. Added memory-safe emergency power-off function description and recommendation. Minor other corrections and clarifications

Contact

u-blox AG

Address: Zürcherstrasse 68
8800 Thalwil
Switzerland

For further support and contact information, visit us at www.u-blox.com/support.