LARA-R6 series

Multi-band / multi-mode LTE Cat 1 modules with global coverage

System integration manual

Abstract

This document describes the features and integration guidelines for the LARA-R6 series modules. These cellular modules are featuring uncompromised global connectivity in smallest form factor. With three variants, global, multi-regional, and regional, customers have great flexibility and can simplify logistics. Comprehensive certification scheme, versatile interfaces, secure by design, feature rich and with multi-band and multi-mode capabilities make LARA-R6 series modules ideally suitable for use in any region and in wide range of applications.

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This document applies to the following products:

Product name	Type number	Modem version	Application version	PCN reference	Product status
LARA-R6001	LARA-R6001-00B				Functional sample
LARA-R6401	LARA-R6401-00B				Functional sample
LARA-R6801	LARA-R6801-00B				Functional sample

Contents

1 System description

1.1 Overview

The LARA-R6 series comprises multi-band and multi-mode modules supporting LTE Cat 1 FDD and LTE Cat 1 TDD radio access technology, with 3G UMTS/HSPA and 2G GSM/GPRS/EGPRS fallback, providing the ideal solution for global and multi-regional coverage in the small LARA LGA form-factor (26.0 x 24.0 mm, 100-pin), which is easy to integrate in compact designs.

With 3 variants, consisting of the LARA-R6001 solution with global coverage, the LARA-R6801 solution for multi-regional operations, and the LARA-R6401 solution mainly for North America, customers have great flexibility, can maximize reusing development efforts, and can simplify logistics. Customers can take advantage of embedded IoT protocols (LwM2M, MQTT) and security features (TLS/DTLS, secure update/secure boot) to implement various applications, such as device management, remote device actions, and secure FOTA updates.

Versatile interfaces, features, multi-band and multi-mode capabilities make the LARA-R6 series modules ideally suited to a wide range of applications, such as asset tracking, telematics, remote monitoring, alarm panels, video surveillance, connected health, point of sale terminal, and mobile cameras. Generally, the modules are suited to applications that require medium speed data, seamless connectivity, superior coverage, low latency, streaming services (data or voice), and to industrial applications focused on product life-cycle longevity.

Table 1 summarizes the main features and interfaces of the LARA-R6 series modules.

Model	Region	Radio Access Technology				Positioning				Interfaces					Features												Grade		
		LTE Cat 1 FDD bands	LTE Cat 1 TDD bands	UMTS/HSPA FDD bands	GSM/GPRS/EGPRS bands	Internal GNSS receiver	External GNSS control via modem	AssistNow Software	CellLocate®	UART	USB 2.0	I2C	GPIOs	Digital audio	VoLTE/CSFB	Rx Diversity	Dual stack IPv4 / IPv6	Embedded TCP/IP, UDP/IP, HTTP/FTP	Embedded MQTT	FOAT / uFOTA	Device and Data Security	TSL/DTLS	3GPP Power Saving Mode	eDRX	LwM2M	Antenna and SIM detection	Standard	Professional	Automotive
LARA-R6001	Global	1,2,3,4,5,7,8 12,13,18,19 20,26,28	38,39 40,41	1,2 5,8	Quad		•	•	•	2	1	1	9	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•	
LARA-R6401	North America	2,4,5 12,13,14 66,71					•	•	•	2	1	1	9	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•	
LARA-R6801	EMEA APAC Japan LATAM	1,2,3,4,5,7,8 18,19 20,26,28		1,2 5,8	Quad		•	•	•	2	1	1	9	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•	

Table 1: LARA-R6 series main features summary

LARA-R6 series modules include three variants providing flexibility to use the bands and the radio access technology available by specific region or operators:

- LARA-R6001 is the smallest LTE Cat 1 multi-mode module for global coverage. It is single SKU for the world, provides universal connectivity, and simplifies logistics. This truly global module with comprehensive band support has 18 LTE bands plus 3G/2G fallback.
- LARA-R6401 offers an ideal LTE Cat 1 solution for North America, as it supports all relevant LTE bands and is designed for use on AT&T, FirstNet, Verizon, or T-Mobile. Managing a single SKU for the North American market simplifies logistics and reduces associated costs.
- LARA-R6801 is a multi-regional variant specifically designed for use in Europe, Middle East, Africa, Asia-Pacific, Japan and Latin America regions, supporting all relevant LTE Cat 1 bands deployed in these regions, plus 3G/2G fallback.

The modules provide Voice over LTE (VoLTE) and Circuit-Switched-Fall-Back (CSFB)[1] audio capability.

Table 2 summarizes cellular radio access technology characteristics of LARA-R6 series modules.

4G LTE	3G UMTS/HSDPA/HSUPA [2]	2G GSM/GPRS/EDGE [3]
Long Term Evolution (LTE) Evolved UTRA (E-UTRA) Frequency Division Duplex (FDD) Time Division Duplex (TDD) [4] DL Rx diversity	High Speed Packet Access (HSPA) UMTS Terrestrial Radio Access (UTRA) Frequency Division Duplex (FDD) DL Rx diversity	Enhanced Data rate GSM Evolution (EDGE) GSM EGPRS Radio Access (GERA) Time Division Multiple Access (TDMA) DL Advanced Rx Performance Phase 1
LTE Power Class • Power Class 3 (23 dBm)	UMTS/HSDPA/HSUPA Power Class • Class 3 (24 dBm)	GSM/GPRS (GMSK) Power Class • Class 4 (33 dBm) for 850/900 band • Class 1 (30 dBm) for 1800/1900 band EDGE (8-PSK) Power Class • Class E2 (27 dBm) for 850/900 band • Class E2 (26 dBm) for 1800/1900 band
Data rate • LTE category 1: up to 10.3 Mbit/s DL, up to 5.2 Mbit/s UL	Data rate • HSDPA category 8: up to 7.2 Mbit/s DL • HSUPA category 6: up to 5.76 Mbit/s UL	Data rate[5] • GPRS multi-slot class 33[6], CS1-CS4, up to 107 kbit/s DL, 85.6 kbit/s UL • EDGE multi-slot class 33[6], MCS1-MCS9, up to 296 kbit/s DL, 236.8 kbit/s UL

Table 2: LARA-R6 series LTE, 3G and 2G characteristics

[1] Circuit-Switched-Fall-Back (CSFB) is not supported by LARA-R6401 modules.
[2] 3G radio access technology is not supported by LARA-R6401 modules.
[3] 2G radio access technology is not supported by LARA-R6401 modules.
[4] LTE TDD radio access technology is not supported by LARA-R6401, or LARA-R6801 modules.
[5] GPRS/EDGE multislot class determines the number of timeslots available for upload and download and thus the speed at which data can be transmitted and received, with higher classes typically allowing faster data transfer rates.
[6] GPRS/EDGE multislot class 33 implies a maximum of 5 slots in DL (reception), 4 slots in UL (transmission) with 6 slots in total.

1.2 Architecture

Figure 1 summarizes the internal architecture of the LARA-R6 series modules.

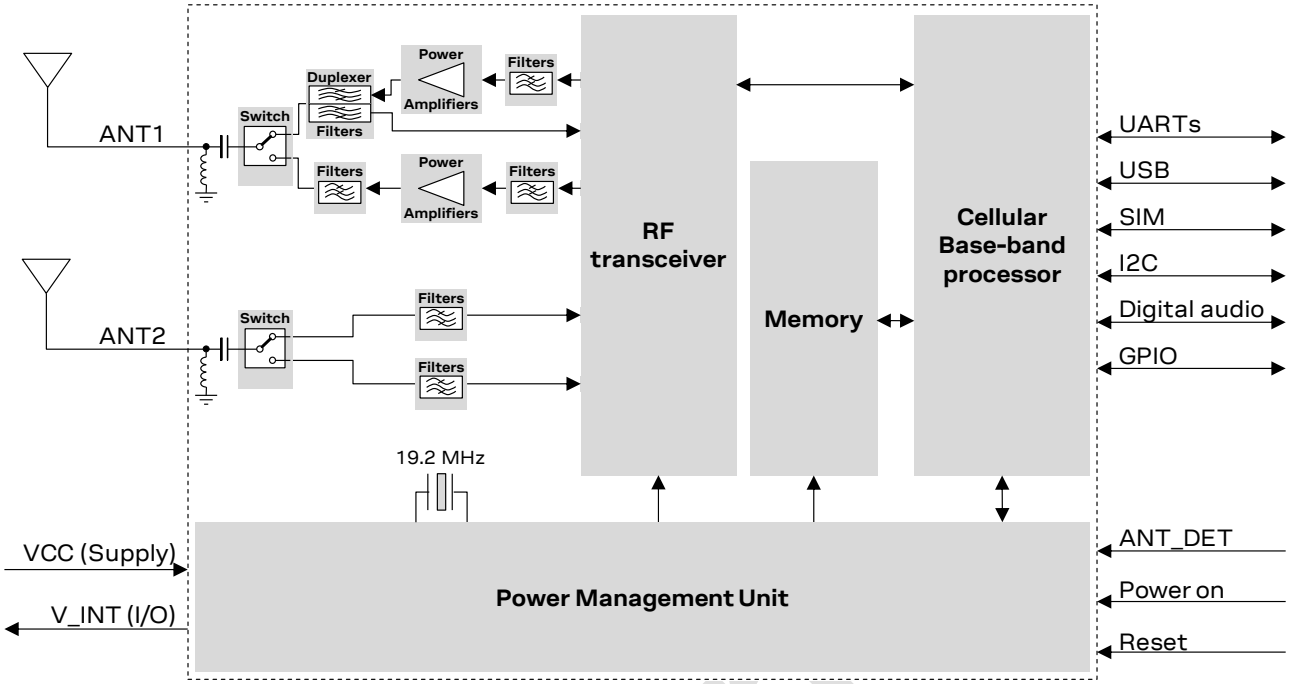

Figure 1: LARA-R6 series modules simplified block diagram

LARA-R6 series modules internally consist of the RF, baseband and power management sections described herein with more details than the simplified block diagrams of Figure 1.

RF section

The RF section is composed section is composed of the following main elements:

- RF transceiver performs modulation, up-conversion of the baseband signals for transmission, down-conversion and demodulation of the dual RF signals for reception
- Power amplifiers (PA) amplify the Tx signal modulated by the RF transceiver
- RF switches connect primary (**ANT1**) and secondary (**ANT2**) ports to the suitable Tx / Rx path
- SAW RF duplexers and RF filters separate the Tx and Rx signal paths and provide RF filtering
- 19.2 MHz crystal oscillator generates the clock reference in active mode or connected mode.

Baseband and power management section

The baseband and power management section is composed of the following main elements:

- Baseband processor IC, integrating:
  - Microprocessor and DSP for control functions and digital processing
  - Memory interface controller
  - Dedicated peripheral blocks for control of the USB, SIM and generic digital interfaces
  - Interfaces to RF transceiver ASIC
- Memory system, which includes NAND flash and LPDDR2 RAM
- Power management IC, integrating:
  - Voltage regulators to derive all the internal supply voltages from **VCC** module supply input
  - Voltage sources for external use: **VSIM** and **V_INT**
  - Hardware power on / off
  - Low power modes support

1.3 Pin-out

Table 3 lists the pin-out of the LARA-R6 series modules, with pins grouped by function.

Function	Pin name	Pin no.	I/O	Description	Remarks
Power	VCC	51,52,53	I	Module supply input	VCC supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for description and requirements. See section 2.2.1 for external circuit design-in.
	GND	1,3,5,14,20, 21,22,30,32, 43,50,54,55, 57,58,60,61, 63-96	N/A	Ground	GND pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.
	V_INT	4	O	Generic Digital Interfaces supply output	V_INT = 1.8 V (typ.), generated by internal linear regulator when the module is switched on, outside PSM deep-sleep. Test-Point for diagnostic access is recommended. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.
System	PWR_ON	15	I	Power-on input	Internal pull-up to internal voltage domain. Test-Point for diagnostic access is recommended. See section 1.6.1 for functional description. See section 2.3.1 for external circuit design-in.
	RESET_N	18	I	External reset input	Internal pull-up to internal voltage domain. Test-Point for diagnostic access is recommended. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.
Antenna	ANT1	56	I/O	RF input/output for main Tx/Rx antenna	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for description and requirements. See section 2.4 for external circuit design-in.
	ANT2	62	I	RF input/output for Rx diversity antenna	50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for description and requirements. See section 2.4 for external circuit design-in.
	ANT_DET	59	I	Input for antenna detection	ADC for antenna presence detection function. See section 1.7.2 for functional description. See section 2.4.2 for external circuit design-in.
SIM	VSIM	41	O	SIM supply output	VSIM = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	39	I/O	SIM data	Data input/output for external 1.8 V / 3 V SIM Internal 4.7 kΩ pull-up to VSIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	38	O	SIM clock	Clock output for external 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	40	O	SIM reset	Reset output for external 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.

Function	Pin name	Pin no.	I/O	Description	Remarks
UART	RXD	13	O	UART data output	1.8 V output, UART Circuit 104 (RXD) per ITU-T V.24, supporting AT and data, FOAT, Multiplexer. Test-Point and series 0 Ω for diagnostic to be considered. See section 1.9.1.1 for functional description. See section 2.6.1 for external circuit design-in.
	TXD	12	I	UART data input	1.8 V input, UART Circuit 103 (TXD) per ITU-T V.24, supporting AT and data, FOAT, Multiplexer. Internal active pull-up to V_INT. Test-Point and series 0 Ω for diagnostic to be considered. See section 1.9.1.1 for functional description. See section 2.6.1 for external circuit design-in.
	CTS	11	O	UART clear to send output	1.8 V output, UART Circuit 106 (CTS) per ITU-T V.24. See section 1.9.1.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	10	I	UART ready to send input	1.8 V input, UART Circuit 105 (RTS) per ITU-T V.24. Internal active pull-up to V_INT. See section 1.9.1.1 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	6	O	UART data set ready output	1.8 V output, UART Circuit 107 (DSR) per ITU-T V.24. Alternatively configurable as AUX UART RTS input. See section 1.9.1.1 for functional description. See section 2.6.1 for external circuit design-in.
	RI	7	O	UART ring indicator output	1.8 V output, UART Circuit 125 (RI) per ITU-T V.24. Alternatively configurable as AUX UART CTS output. See section 1.9.1.1 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	9	I	UART data terminal ready input	1.8 V input, UART Circuit 108/2 (DTR) per ITU-T V.24. Internal active pull-up to V_INT. Alternatively configurable as AUX UART data input. See section 1.9.1.1 for functional description. See section 2.6.1 for external circuit design-in.
	DCD	8	O	UART data carrier detect output	1.8 V input, UART Circuit 109 (DCD) per ITU-T V.24. Alternatively configurable as AUX UART data output. See section 1.9.1.1 for functional description. See section 2.6.1 for external circuit design-in.
AUX UART	DCD	8	O	AUX UART data output	1.8 V output, AUX UART Circuit 104 (RXD) per ITU-T V.24, supporting AT and data, FOAT, GNSS tunneling. The second auxiliary UART interface is disabled by default, and it can be enabled by +USIO AT command. See section 1.9.1.2 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	9	I	AUX UART data input	1.8 V input, AUX UART Circuit 103 (TXD) per ITU-T V.24, supporting AT and data, FOAT, GNSS tunneling. Internal active pull-up to V_INT. The second auxiliary UART interface is disabled by default, and it can be enabled by +USIO AT command. See section 1.9.1.2 for functional description. See section 2.6.1 for external circuit design-in.
	RI	7	O	AUX UART clear to send output	1.8 V output, AUX UART Circuit 106 (CTS) per ITU-T V.24. See section 1.9.1.2 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	6	I	AUX UART ready to send input	1.8 V input, AUX UART Circuit 105 (RTS) per ITU-T V.24. Internal active pull-up to V_INT. See section 1.9.1.2 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin name	Pin no.	I/O	Description	Remarks
USB	VUSB_DET	17	I	USB detect input	VBUS (5 V typ) must be connected to this pin to enable the USB interface, supporting AT / data communication, FOAT, GNSS tunneling, FW update by u-blox tool, diagnostic. Test-Point for diagnostic / FW update highly recommended See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	USB_D-	28	I/O	USB Data Line D-	USB interface supporting AT / data communication, FOAT, GNSS tunneling, FW update by u-blox tool, diagnostic. 90 Ω nominal differential impedance (Z0) 30 Ω nominal common mode impedance (ZCM) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [7] are part of the USB pin driver and need not be provided externally. Test-Point for diagnostic / FW update highly recommended See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	USB_D+	29	I/O	USB Data Line D+	USB interface supporting AT / data communication, FOAT, GNSS tunneling, FW update by u-blox tool, diagnostic. 90 Ω nominal differential impedance (Z0) 30 Ω nominal common mode impedance (ZCM) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [7] are part of the USB pin driver and need not be provided externally. Test-Point for diagnostic / FW update highly recommended See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
I2C	SCL	27	O	I2C bus clock line	1.8 V open drain, for communication with external u-blox GNSS chips / modules, and other I2C devices. Internal 2.2 kΩ pull-up resistor: no external pull-up required. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	SDA	26	I/O	I2C bus data line	1.8 V open drain, for communication with external u-blox GNSS chips / modules, and other I2C devices. Internal 2.2 kΩ pull-up resistor: no external pull-up required. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
Audio	I2S_TXD	35	O	I2S transmit data	Digital audio data output. Alternatively configurable as GPIO. See sections 1.10 and 1.12 for functional description. See sections 2.7 and 2.8 for external circuit design-in.
	I2S_RXD	37	I	I2S receive data	Digital audio data input. Alternatively configurable as GPIO. See sections 1.10 and 1.12 for functional description. See sections 2.7 and 2.8 for external circuit design-in.
	I2S_CLK	36	O	I2S bit clock	Digital audio bit clock. Alternatively configurable as GPIO. See sections 1.10 and 1.12 for functional description. See sections 2.7 and 2.8 for external circuit design-in.
	I2S_WA	34	O	I2S word alignment	Digital audio word alignment synchronization signal. Alternatively configurable as GPIO. See sections 1.10 and 1.12 for functional description. See sections 2.7 and 2.8 for external circuit design-in.
Clock output	GPIO6	19	O	Clock output	1.8 V configurable clock output. See section 1.11 for functional description. See section 2.7 for external circuit design-in.

Function	Pin name	Pin no.	I/O	Description	Remarks
GPIO	GPIO1	16	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	GPIO2	23	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	GPIO3	24	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	GPIO4	25	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	GPIO5	42	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	I2S_TXD	35	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	I2S_RXD	37	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	I2S_CLK	36	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	I2S_WA	34	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
Reserved	RSVD	33	N/A	RESERVED pin	Pin with reserved use. Test-Point for diagnostic highly recommended. See sections 1.13 and 2.9
	RSVD	2, 31	N/A	RESERVED pin	Pin reserved for future use. Internally not connected. Leave unconnected. See sections 1.13 and 2.9
	RSVD	44-49, 97-100	N/A	RESERVED pin	Pin reserved for future use. Leave unconnected. See sections 1.13 and 2.9

Table 3: LARA-R6 series modules pin definition, grouped by function

1.4 Operating modes

LARA-R6 series modules have several operating modes, which are defined in Table 4.

General status	Operating mode	Definition
Power-down	**Not-powered mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-off mode	**VCC** supply within operating range and module is switched off.
Normal Operation	**Deep-sleep mode**	Only the RTC runs. The processor and other parts of the module are switched off.
	Idle mode	Module processor runs at the minimum frequency to save power consumption.
	Active mode	Module processor runs at normal operating frequency to enable related functions.
	Connected mode	RF Tx/Rx enabled with processor running at related operating frequency.

Table 4: Module operating modes definition

The initial operating mode of LARA-R6 series modules has the **VCC** supply not present or below the operating range: the modules are switched off in not-powered mode.

Once a valid **VCC** supply is applied to the LARA-R6 series modules, they remain switched off in the power-off mode. Then the proper toggling of the **PWR_ON** input line is necessary to trigger the switch-on routine of the modules that subsequently enter the active mode.

LARA-R6 series modules are fully ready to operate when in active mode. The available communication interfaces are completely functional and the module can accept and respond to AT commands, entering connected mode upon cellular RF signal reception / transmission.

LARA-R6 series modules switch from active mode to the low power idle mode whenever possible, if the low power configuration is enabled by the dedicated +UPSV AT command. The low power idle mode can last for different time periods according to the specific +UPSV AT command setting, according to the DRX / eDRX setting, and according to the concurrent activities executed.

LARA-R6 series modules enter the user equipment power saving mode (PSM) defined in 3GPP Rel.13 whenever possible, if the use of the PSM is enabled by the +CPSMS / +UCPSMS AT commands, and according to the +UMNOPROF AT command settings. The PSM can last for different time periods according to the T3412 periodic TAU timer set by the network. Then, the modules enter the ultra-low power deep-sleep mode whenever possible, if no other concurrent activities are executed.

Once the modules enter the ultra-low power deep-sleep mode, the available communication interfaces are not functional: a wake-up event, consisting in proper toggling of the **PWR_ON** input line or the expiration of the timer set by the network, is necessary to trigger the wake-up routine of the modules that subsequently enter back into the active mode.

LARA-R6 series modules can be gracefully switched off by the dedicated +CPWROFF AT command, or by proper toggling of the **PWR_ON** input line.

Figure 2 summarizes the transition between the different operating modes.

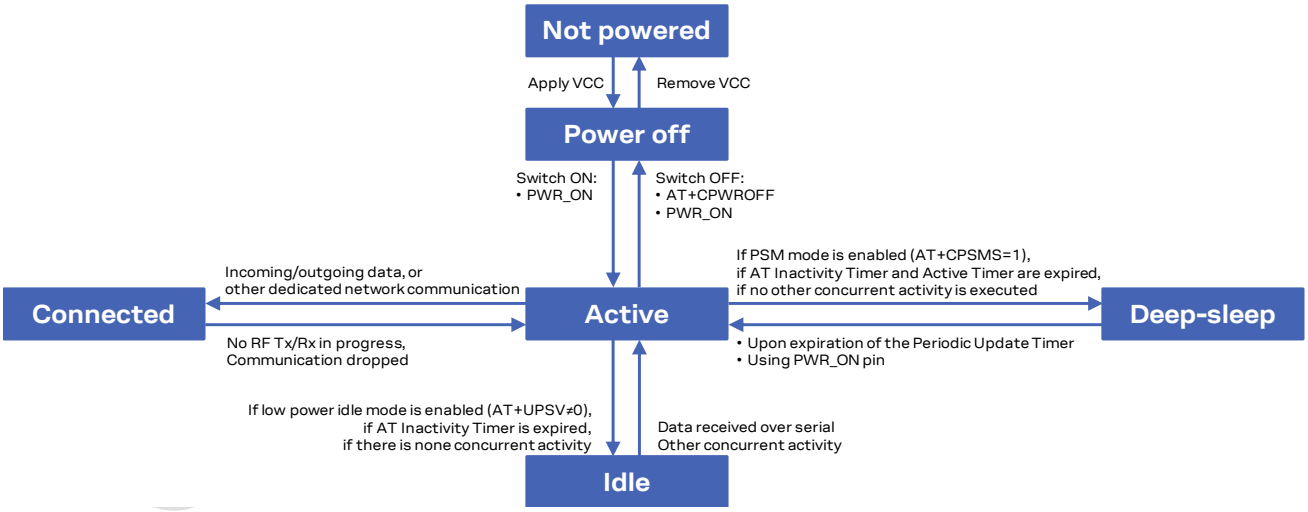

Figure 2: LARA-R6 series modules operating modes transitions

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

The **VCC** pins are internally connected to the RF power amplifier and to the integrated Power Management Unit: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators, including the **V_INT** supply for generic digital interfaces (as the UARTs, I2C, I2S, GPIOs) and the **VSIM** supply for the SIM interface.

During operation, the current drawn by the LARA-R6 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the pulse of current consumption during GSM transmitting bursts at maximum power level in connected mode (as described in section 1.5.1.4) to the ultra-low current consumption during the ultra-low power deep-sleep mode with PSM enabled (as described in section 1.5.1.6).

LARA-R6 series modules provide separate supply inputs over the three **VCC** pins:

- **VCC** pins #52 and #53 represent the supply input for the internal RF power amplifier, demanding most of the total current drawn of the module when RF transmission is enabled during a voice/data call
- **VCC** pin #51 represents the supply input for the internal baseband Power Management Unit and the internal transceiver, demanding minor part of the total current drawn of the module when RF transmission is enabled during a voice/data call

Figure 3 provides a simplified block diagram of LARA-R6 series modules internal VCC supply routing.

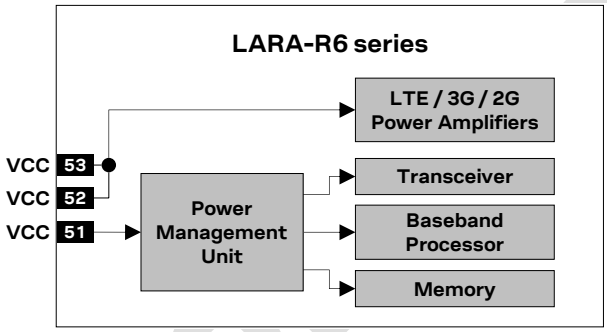

Figure 3: LARA-R6 series modules internal VCC supply routing simplified block diagram

1.5.1.1 VCC supply requirements

Table 5 summarizes the requirements for the **VCC** module supply. See section 2.2.1 for all the suggestions to properly design a **VCC** supply circuit compliant to the requirements listed in Table 5.

⚠ **VCC** supply circuit affects the RF compliance of the device integrating LARA-R6 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is met by fulfilling the requirements for the **VCC** supply summarized in Table 5.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.3 V min. / 4.5 V max.	RF performance is guaranteed when **VCC** PA voltage is inside the normal operating range limits. RF performance may be affected when **VCC** PA voltage is outside the normal operating range limits, though the module is still fully functional until the **VCC** voltage is inside the extended operating range limits.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.1 V min. / 4.5 V max.	**VCC** voltage must be above the extended operating range minimum limit to switch-on the module. The module may switch-off when the **VCC** voltage drops below the extended operating range minimum limit. Operation above **VCC** extended operating range is not recommended and may affect device reliability.
VCC average current	Support with adequate margin the highest averaged **VCC** current consumption value in connected mode conditions specified in the LARA-R6 series data sheet [1]	The highest averaged **VCC** current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and **VCC** voltage. See 1.5.1.4, 1.5.1.3 and 1.5.1.2 for connected mode current profiles.
VCC peak current	Support with margin the highest peak **VCC** current consumption value in connected mode conditions specified in the LARA-R6 series data sheet [1]	The specified highest peak of **VCC** current consumption occurs during GSM single transmit slot in 850/900 MHz connected mode, in case of a mismatched antenna. See 1.5.1.4 for 2G connected mode current profiles.
VCC voltage drop during 2G Tx slots	Lower than 400 mV	**VCC** voltage drop directly affects the RF compliance with applicable certification schemes. Figure 7 describes **VCC** voltage drop during Tx slots.
VCC voltage ripple during 2G/3G/LTE Tx	Noise in the supply must be minimized	**VCC** voltage ripple directly affects the RF compliance with applicable certification schemes. Figure 7 describes **VCC** voltage ripple during Tx slots.
VCC under/over-shoot at start/end of Tx slots	Absent or at least minimized	**VCC** under/over-shoot directly affects the RF compliance with applicable certification schemes. Figure 7 describes **VCC** voltage under/over-shoot.

Table 5: Summary of VCC supply requirements

1.5.1.2 VCC consumption in LTE connected mode

During an LTE connection, the module may transmit and receive continuously due to the frequency division duplex (FDD) mode of operation or it may transmit and receive alternatively due to the time division duplex (TDD) mode of operation available with LTE radio access technology.

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 0.5 ms (time length of one Resource Block), thus the rate of power change can reach a maximum rate of 2 kHz.

In the worst case scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 0.25 W), the average current drawn by the module at the VCC pins is considerable (see the "Current consumption" section in LARA-R6 series data sheet [1]). At the lowest output RF power (approximately 0.1 µW), the current drawn by the internal power amplifier is strongly reduced and the total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

The maximum peak of current consumption in LTE is similar to that in 3G radio access technology, because in both cases the maximum output RF power is roughly 0.25 W. In the LTE connected mode, as in the 3G connected mode, there are no high current peaks like the 2G connection mode, which uses the Time Division Multiple Access (TDMA) mode of operation, because the maximum output RF power in the 2G low bands (850 MHz or 900 MHz) is roughly 2.0 W.

Figure 4 shows an example of the module current consumption profile versus time in the LTE FDD connected mode. Detailed current consumption values can be found in LARA-R6 series data sheet [1].

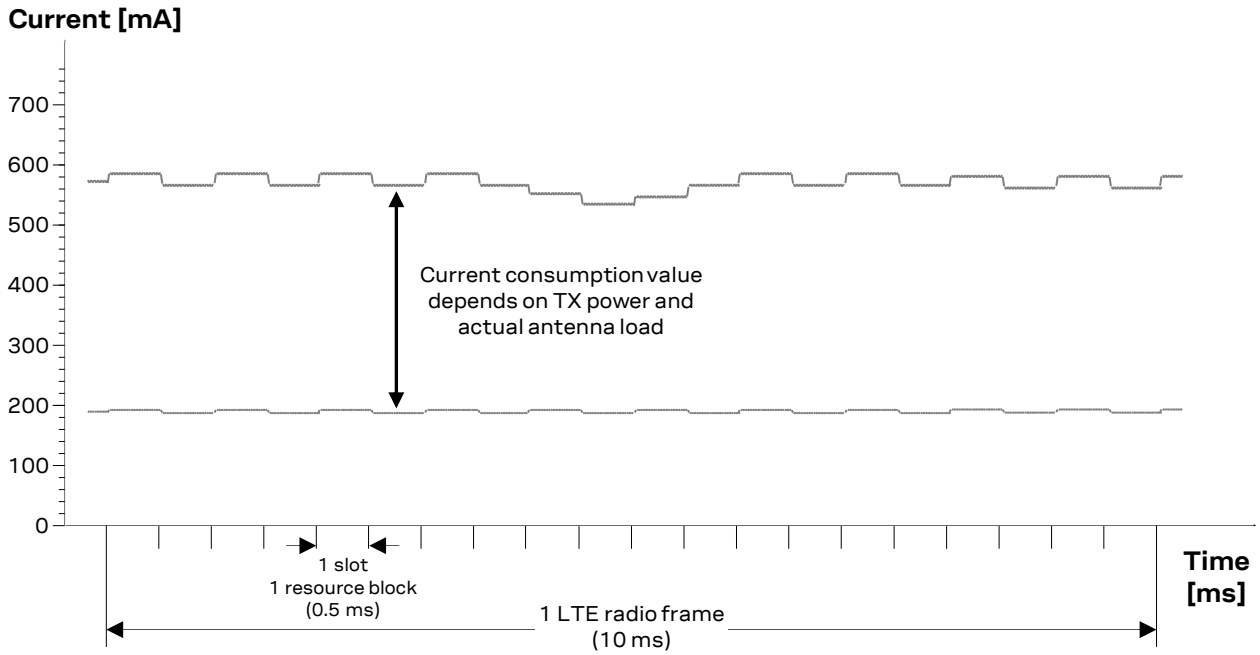

Figure 4: VCC current consumption profile versus time during LTE connection (TX and RX continuously enabled)

1.5.1.3 VCC consumption in 3G connected mode

During a 3G connection, the module can transmit and receive continuously due to the frequency division duplex (FDD) mode of operation with the wideband code division multiple access (WCDMA).

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 666 µs, so the rate of power change can reach a maximum rate of 1.5 kHz.

There are no high current peaks as in the 2G connection, since transmission and reception are continuously enabled due to FDD WCDMA implemented in the 3G that differs from the TDMA implemented in the 2G case.

In the worst case scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 0.25 W), the average current drawn by the module at the VCC pins is considerable (see the "Current consumption" section in LARA-R6 series data sheet [1]). At the lowest output RF power (approximately 0.01 µW), the current drawn by the internal power amplifier is strongly reduced. The total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

Figure 5 shows an example of the current consumption profile of the module in 3G WCDMA/HSPA continuous transmission mode.

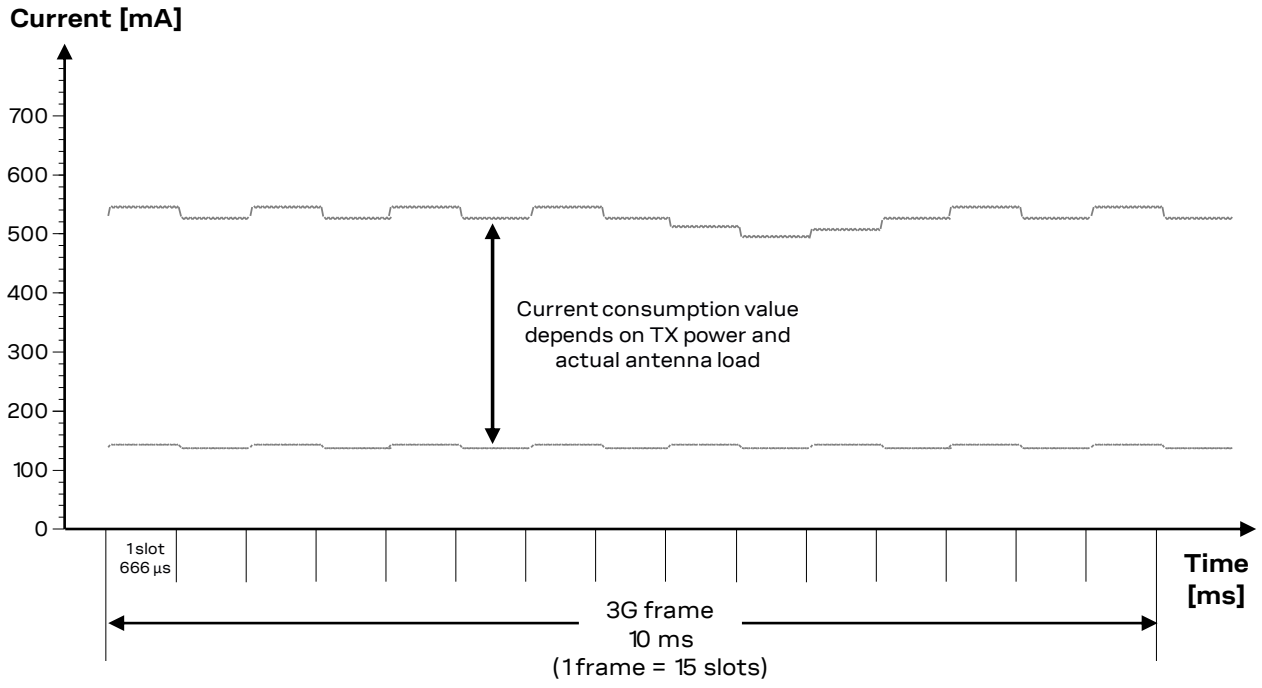

Figure 5: VCC current consumption profile versus time during a 3G connection (TX and RX continuously enabled)

1.5.1.4 VCC consumption in 2G connected mode

When a GSM call is established, the **VCC** consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The current consumption peak during a transmission slot is strictly dependent on the transmitted power, which is regulated by the network. The transmitted power in the transmit slot is also the more relevant factor for determining the average current consumption.

If the module is transmitting in 2G single-slot mode (as in GSM talk mode) in the 850 or 900 MHz bands, at the maximum RF power control level (approximately 2 W or 33 dBm in the Tx slot/burst), the current consumption can reach an high peak / pulse (see LARA-R6 series data sheet [1]) for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access).

If the module is transmitting in 2G single-slot mode in the 1800 or 1900 MHz bands, the current consumption figures are quite less high than the one in the low bands, due to the 3GPP transmitter output power specifications.

During a GSM call, current consumption is not so significantly high in receiving or in monitor bursts and it is low in the bursts unused to transmit / receive.

Figure 6 shows an example of the module current consumption profile versus time in GSM talk mode.

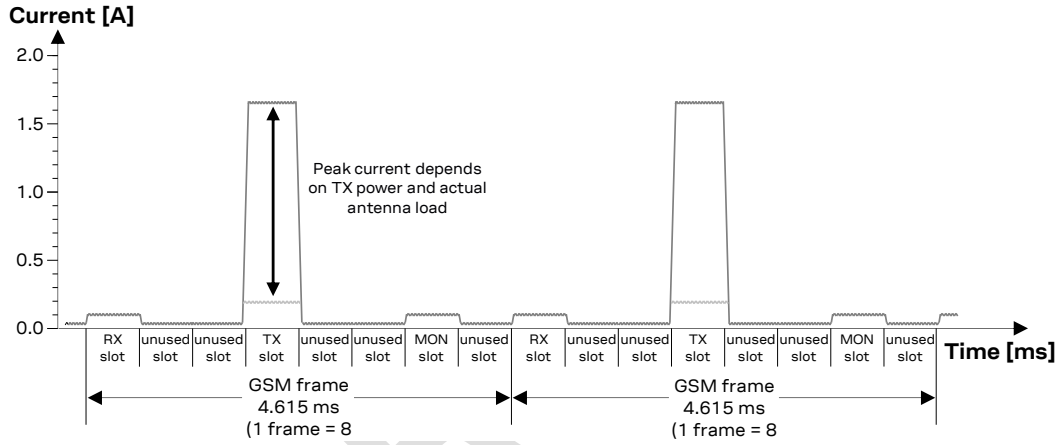

Figure 6: VCC current consumption profile versus time during a GSM call (1 TX slot, 1 RX slot)

Figure 7 illustrates **VCC** voltage profile versus time during a GSM call, according to the related **VCC** current consumption profile described in Figure 6.

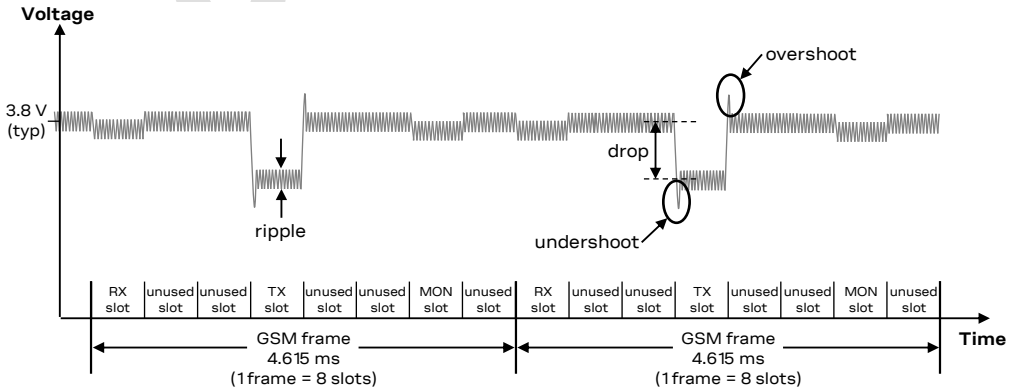

Figure 7: Description of the VCC voltage profile versus time during a GSM call (1 TX slot, 1 RX slot)

1.5.1.5 VCC consumption in ultra low power deep-sleep mode

The use of the user equipment power saving mode defined in 3GPP Rel.13 is by default disabled, but it can be enabled using the +CPSMS AT command (see the AT commands manual [2]). When the use of the PSM is enabled, the module automatically enters the PSM and the ultra low power deep-sleep mode whenever possible.

When in ultra low power deep-sleep mode, the consumption is reduced to a value in the µA range as only the RTC runs. Detailed consumption values can be found in the LARA-R6 series data sheet [1].

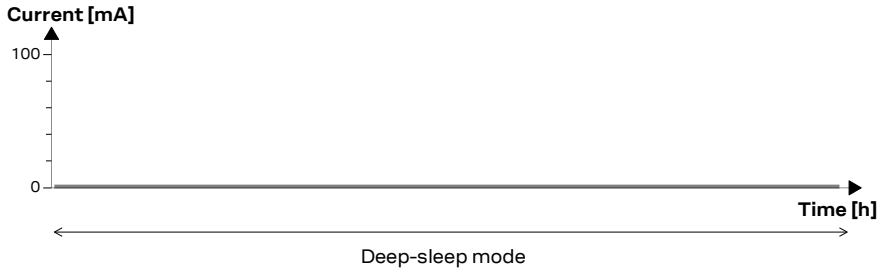

Figure 8: Example of VCC current consumption profile in ultra low power deep-sleep mode

1.5.1.6 VCC consumption in low power idle mode

The power saving configuration is disabled by default, but it can be enabled using the appropriate AT command (see u-blox AT commands manual [2], +UPSV AT command). When power saving is enabled, the module automatically enters low power idle mode whenever possible, reducing consumption.

When the power saving configuration is enabled and the module is registered or attached to a network, the module automatically enters the low power idle mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to the 2G / 3G / LTE system requirements, even if the connected mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active mode to enable the reception of the paging block. In between, the module switches to low power idle mode. This is known as discontinuous reception (DRX) or extended discontinuous reception (eDRX).

Figure 9 illustrates a typical example of the module current consumption profile when power saving is enabled. The module is registered with the network, automatically enters the low power idle mode and periodically wakes up to active mode to monitor the paging channel for the paging block reception. Detailed current consumption values can be found in the LARA-R6 series data sheet [1]).

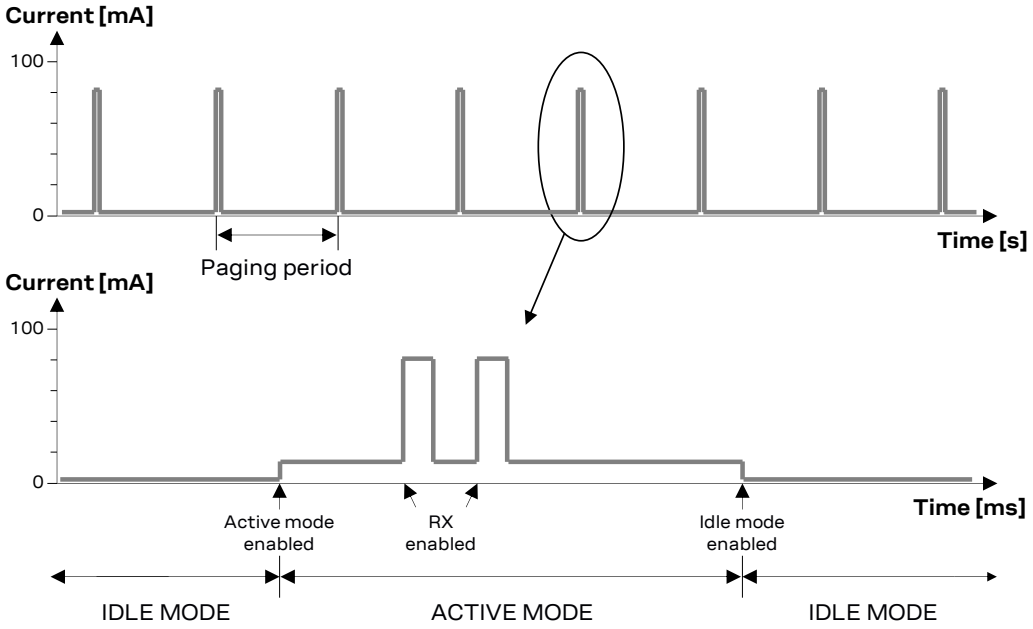

Figure 9: VCC current consumption profile with power saving enabled and module registered with the network: the module is in low-power idle mode and periodically wakes up to active mode to monitor the paging channel for paging block reception

1.5.1.7 VCC consumption in active mode (low power idle mode disabled)

The active mode is the state where the module is switched on and ready to communicate with an external device by means of the application interfaces (as the USB or the UART serial interface). The module processor core is active, and the 19.2 MHz reference clock frequency is used.

If the low power idle mode configuration is disabled, as it is by default (see the u-blox AT commands manual [2], +UPSV AT commands for details), the module remains in active mode. Otherwise, if the low power idle mode configuration is enabled, the module enters the low power idle mode whenever possible, reducing consumption.

Figure 10 illustrates a typical example of the module current consumption profile when power saving is disabled. In such case, the module is registered with the network and while active mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception. Detailed current consumption values can be found in the LARA-R6 series data sheet [1].

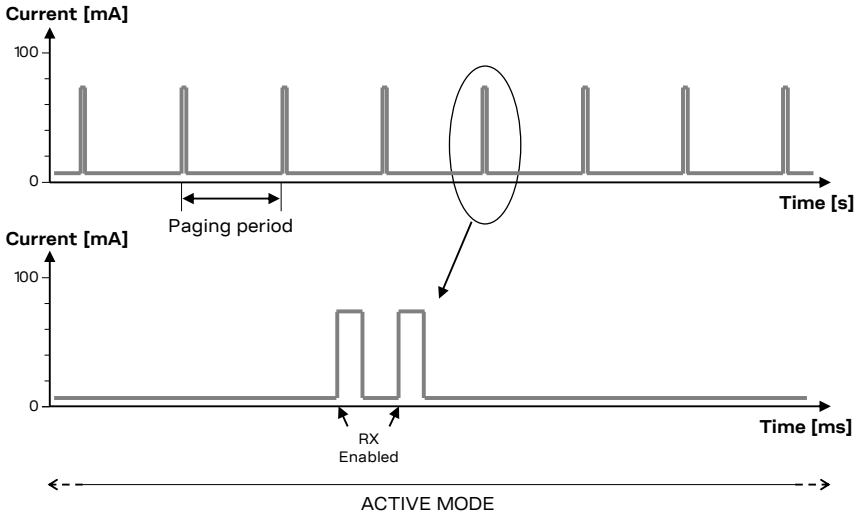

Figure 10: VCC current consumption profile with power saving disabled and module registered with the network: active mode is always held and the receiver is periodically activated to monitor the paging channel for paging block reception

1.5.2 Generic digital interfaces supply output (V_INT)

The V_INT output pin of the LARA-R6 series modules is connected to an internal 1.8 V supply with a current capability specified in the LARA-R6 series data sheet [1]. This supply is internally generated by a linear LDO regulator integrated in the Power Management Unit and it is internally used to source the generic digital interfaces of the cellular module (as the UARTs, I2C, I2S, GPIOs), as described in Figure 11. The output of this regulator is enabled when the module is switched on, outside deep-sleep PSM mode, and it is disabled when the module is switched off or in deep-sleep PSM mode.

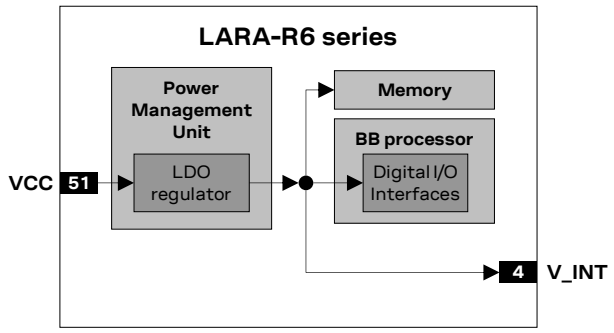

Figure 11: LARA-R6 series interfaces supply output (V_INT) simplified block diagram

1.6 System function interfaces

1.6.1 Module power-on

When LARA-R6 series modules are not powered, they can be switched on as following:

- Applying a voltage at the **VCC** module supply input within the operating range (see LARA-R6 series data sheet [1]), and then forcing a low level at the **PWR_ON** input pin, which is normally set high by an internal pull-up, for a valid time period (see LARA-R6 series data sheet [1]).

When LARA-R6 series modules are in power-off mode (switched off, with a voltage at the **VCC** module supply input within the normal operating range reported in LARA-R6 series data sheet [1]), they can be switched on by:

- Forcing a low level at the **PWR_ON** input pin, which is normally set high by an internal pull-up, for a valid time period (see LARA-R6 series data sheet [1]).

When the LARA-R6 series modules are in ultra-low power PSM deep-sleep mode, with a valid voltage present at the **VCC** module supply input within the operating range reported in LARA-R6 series data sheet [1], they can be woken up as follows:

- Forcing a low level at the **PWR_ON** input pin, which is normally set high by an internal pull-up, for a valid time period (see LARA-R6 series data sheet [1]).

The **PWR_ON** input line is intended to be driven by open drain, open collector, or contact switch.

As described in Figure 12, the **PWR_ON** input line is pulled up to an internal voltage rail minus a diode drop: the voltage value present at **PWR_ON** input pin is normally 0.8 V typical, and the input voltage thresholds are different from the other generic digital interfaces. Detailed electrical characteristics are described in the LARA-R6 series data sheet [1].

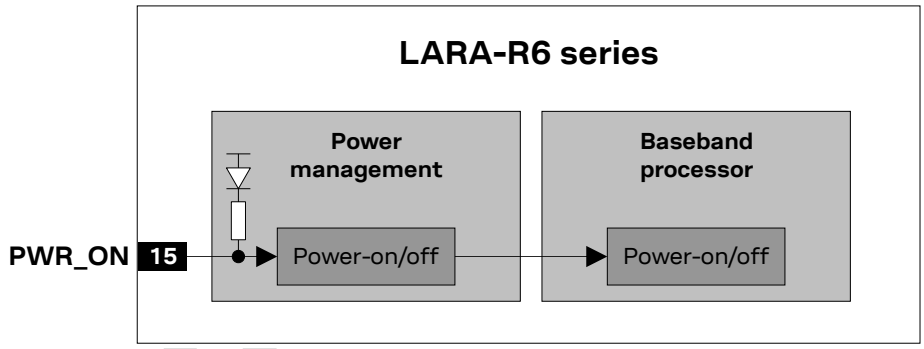

Figure 12: LARA-R6 series PWR_ON input description

Figure 13 shows the module switch-on sequence from the not-powered mode, with following phases:

- The external power supply is applied to the **VCC** module pins
- The **PWR_ON** and the **RESET_N** lines suddenly rise to high logic level due to internal pull-ups.
- The **PWR_ON** input line is held low for a valid time, triggering the module switch-on sequence.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The internal reset signal is held low: the baseband core and all digital pins are held in reset state. When the internal reset signal is released, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces and USB interface due to host / device enumeration timings.
- The module is fully ready to operate after all interfaces are configured.

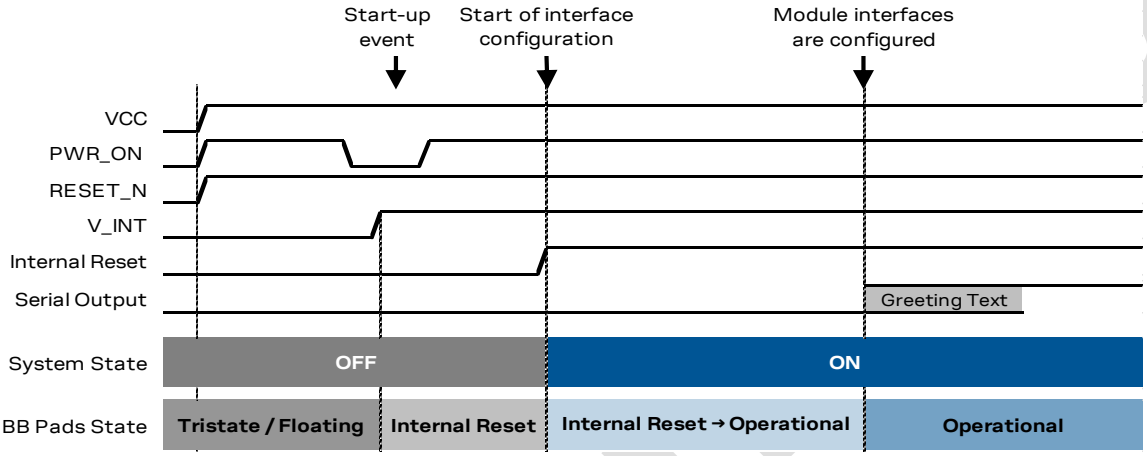

Figure 13: LARA-R6 series switch-on sequence description

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor:
- the **V_INT** pin, to sense the start of the LARA-R6 series module switch-on sequence
- the greeting text configured on the serial interface (see AT commands manual [2], +CSGT AT command), to sense when the module is ready to operate

☞ Before the switch-on of the generic digital interface supply (**V_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the module.

☞ Before the LARA-R6 series module is fully ready to operate, the host application processor should not send any AT command over AT communication interfaces (USB, UART) of the module.

☞ The duration of the LARA-R6 series modules' switch-on routine can largely vary depending on the application / network settings and the concurrent module activities.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply, or forcing an abrupt emergency switch off by asserting the **RESET_N** input, during the boot sequence of the modules.

1.6.2 Module power-off

LARA-R6 series can be gracefully switched off, with storage of the current parameter settings in the module's internal non-volatile memory and a clean network detach, in one of these ways:

- AT+CPWROFF command (see the u-blox AT commands manual [2]).
- Forcing a low pulse at the **PWR_ON** input pin, which is normally set high by an internal pull-up, for a valid time period (see the LARA-R6 series data sheet [1]).

☞ The graceful switched off procedure triggered by the +CPWROFF AT command is the recommended method to properly switch off the LARA-R6 series modules.

☞ The gracefully switch-off procedure must be started as indicated above, and then a proper **VCC** supply must be held at least until the end of the modules' internal switch-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

An emergency faster and safe power-off procedure of LARA-R6 series modules, without proper network detach, can be triggered by:

- AT+CFUN=10 command (see the u-blox AT commands manual [2]).
- Toggling the GPIO input pin configured with the fast and safe power-off function (see section 1.12)

☞ The graceful switched off procedure triggered by the +CPWROFF AT command must be preferred rather than the faster and safe power-off procedure triggered by the AT+CFUN=10 command or by toggling the configured GPIO pin, as the faster and safe power-off procedure is intended to be used in case of emergency only.

An abrupt shutdown occurs on LARA-R6 series modules, without storage of the current parameter settings and without a clean network detach, when:

- The **VCC** supply drops below the extended operating range minimum limit
- Forcing a low level at the **RESET_N** input pin, which is normally set high by an internal pull-up, for a valid time period (see the LARA-R6 series data sheet [1]). The **RESET_N** line is intended to be driven by open drain, open collector or contact switch.

☞ It is highly recommended to avoid an abrupt shutdown, removing the **VCC** supply or asserting the **RESET_N** input line, during LARA-R6 series modules normal operations: it is highly recommended to start the gracefully switch-off procedure as indicated above, and then held a proper **VCC** supply voltage at least until the end of the modules' internal switch-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module

Figure 14 and Figure 15 describe the LARA-R6 series modules switch-off sequence started by means of the AT+CPWROFF command and by means of the **PWR_ON** input pin respectively, allowing storage of current parameter settings in the module's non-volatile memory and a clean network detach, with the following phases:

- When the +CPWROFF AT command is sent, or when a low pulse with appropriate time duration (see the LARA-R6 series data sheet [1]) is applied at the **PWR_ON** input pin, the module starts the switch-off routine.
- Then, if the +CPWROFF AT command has been sent, the module returns the "OK" final result code on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in switch-off mode as long as a switch on event does not occur (applying a low level to **PWR_ON** input pin), and it enters not-powered mode if the **VCC** supply is removed.

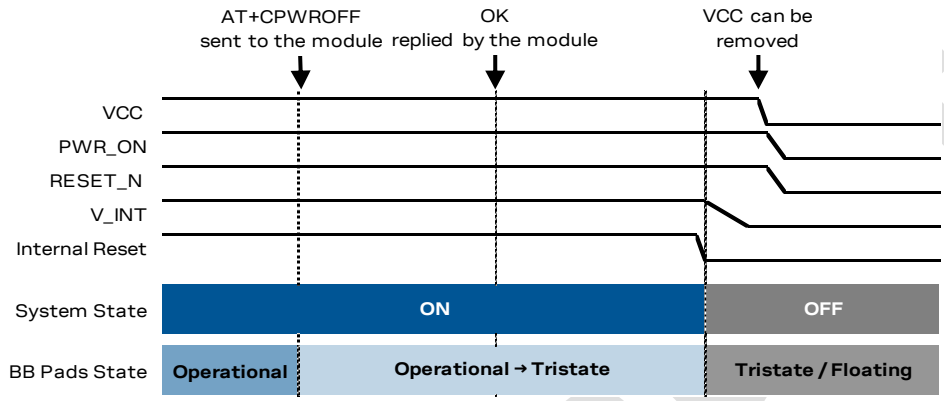

Figure 14: LARA-R6 series modules switch-off sequence by means of AT+CPWROFF command

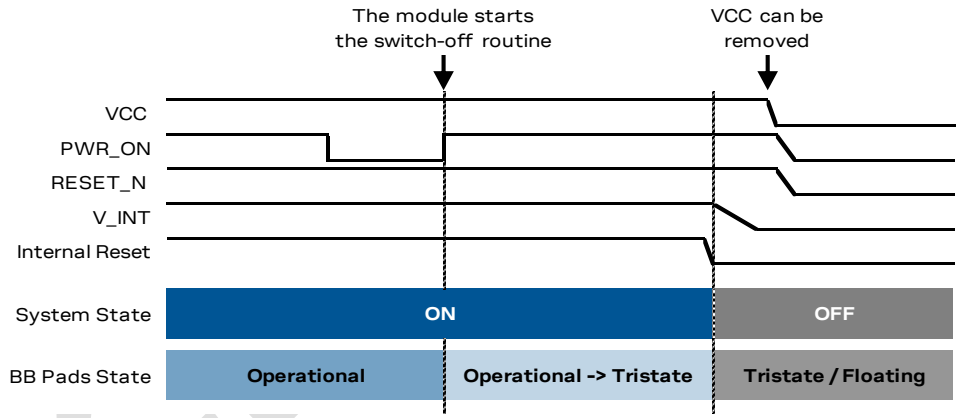

Figure 15: LARA-R6 series modules switch-off sequence by means of PWR_ON pin

☞ The Internal Reset signal is not available on a module pin, but it is highly recommended to monitor:
- the **V_INT** pin, or
- the UART break condition,

to sense the end of the LARA-R6 series module switch-off sequence

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply, or forcing an abrupt switch off by asserting the **RESET_N** input, before the end of the module switch-off sequence

☞ The duration of each phase in the LARA-R6 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

LARA-R6 series modules can be gracefully reset (rebooted) by:

- AT+CFUN=16 command (see the u-blox AT commands manual [2] for detailed description and other possible options).

This command causes an "internal" or "software" reset of the module. The current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed: this is the correct way to reset the modules.

An abrupt hardware shutdown occurs on LARA-R6 series modules when a low level is applied on **RESET_N** input pin for a specific time period. In this case, the current parameter settings are not saved in the module's non-volatile memory and a clean network detach is not performed. Then, the LARA-R6 series modules remain in power-off mode as long as a switch on event does not occur with appropriate toggling of the **PWR_ON** input line.

☞ It is highly recommended to avoid an abrupt hardware reset of the module by forcing a low level on the **RESET_N** input during modules normal operation: the **RESET_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the u-blox AT commands manual [2].

As described in Figure 16, the **RESET_N** input line is equipped with an internal pull-up to internal voltage supply rail.

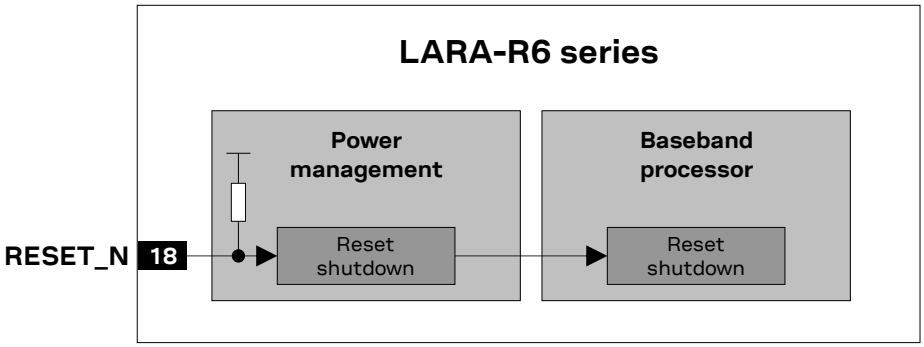

Figure 16: LARA-R6 series RESET_N input equivalent circuit description

☞ For more electrical characteristics details, see the LARA-R6 series data sheet [1].

1.7 Antenna interfaces

1.7.1 Antenna RF interfaces (ANT1 / ANT2)

LARA-R6 series modules provide two RF interfaces for connecting the external antennas:

- **ANT1** represents the primary RF input/output for transmission and reception of RF signals. **ANT1** pin has a nominal characteristic impedance of 50 Ω and must be connected to the primary Tx / Rx antenna through a 50 Ω transmission line to allow proper RF transmission and reception.
- **ANT2** represents the secondary RF input for the reception of LTE / 3G RF signals for Down-Link Rx diversity radio technology supported by the modules as a required feature for LTE Cat 1 UEs. **ANT2** pin has a nominal characteristic impedance of 50 Ω and must be connected to the secondary Rx antenna through a 50 Ω transmission line to allow proper RF reception.

1.7.1.1 Antenna RF interface requirements

Table 6, Table 7 and Table 8 summarize the requirements for the RF interfaces (**ANT1** / **ANT2**). See section 2.4.1 for suggestions to properly design the circuits compliant with these requirements.

⚠ The antenna circuits affect the RF compliance of the host end-device integrating the LARA-R6 series modules with applicable required certification schemes (for more details see section 4). Compliance is met by fulfilling the requirements for the antenna RF interfaces (**ANT1** / **ANT2**) summarized in Table 6, Table 7 and Table 8.

Item	Requirement	Remark
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the ANT1 port.
Frequency Range	See the LARA-R6 series data sheet [1]	The required frequency range of the antenna connected to the ANT1 port depends on the operating bands of the used cellular module and the used mobile network.
Return Loss	S11 < -10 dB (VSWR < 2:1) recommended S11 < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S11, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the ANT1 port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the ANT1 port over the operating frequency range, reducing as much as possible the reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to the antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the ANT1 port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as the Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by the applicable related certification schemes.
Maximum Gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to the ANT1 port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits. For additional info, see sections 4.2.2, 4.3.1 and/or 4.4.
Input Power	> 33 dBm (> 2 W) for modules supporting 2G > 24 dBm (> 0.25 W) for modules not supporting 2G	The antenna connected to the ANT1 port must support the maximum power transmitted by the modules with an adequate margin.

Table 6: Summary of primary Tx/Rx antenna RF interface (ANT1) requirements

Item	Requirement	Remark
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT2** port.
Frequency Range	See the LARA-R6 series data sheet [1]	The required frequency range of the antennas connected to the **ANT2** port depends on the operating bands of the used cellular module and the used mobile network.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT2** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT2** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT2** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as the TIS, specified by applicable related certification schemes.

Table 7: Summary of secondary Rx antenna RF interface (ANT2) requirements

Item	Requirement	Remark
Efficiency imbalance	< 0.5 dB recommended < 1.0 dB acceptable	The radiation efficiency imbalance is the ratio of the primary (**ANT1**) antenna efficiency to the secondary (**ANT2**) antenna efficiency: the efficiency imbalance is a measure of how much better an antenna receives or transmits compared to the other antenna. The radiation efficiency of the secondary antenna needs to be roughly the same of the radiation efficiency of the primary antenna for good RF performance.
Envelope Correlation Coefficient	< 0.4 recommended < 0.5 acceptable	The Envelope Correlation Coefficient (ECC) between the primary (**ANT1**) and the secondary (**ANT2**) antennas is an indicator of the 3D radiation pattern similarity between the two antennas: low ECC arises from antenna patterns with radiation lobes in different directions. The ECC between primary and secondary antennas needs to be sufficiently low to comply with radiated performance requirements specified by the related certification schemes.
Isolation	> 15 dB recommended > 10 dB acceptable	The antenna to antenna isolation is the loss between the primary (**ANT1**) and the secondary (**ANT2**) antennas: high isolation arises from weakly coupled antennas. The isolation between primary and secondary antenna needs to be high for good RF performance.

Table 8: Summary of the primary (ANT1) and secondary (ANT2) antennas relationship requirements

1.7.2 Antenna detection (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an analog to digital converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by the **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the u-blox AT commands manual [2] for more details on this feature.

The **ANT_DET** pin generates a DC current (for detailed characteristics, see the LARA-R6 series data sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. The requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.2 for the antenna detection circuit on the application board and the diagnostic circuit on the antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM card / chip interface

LARA-R6 series modules provide a high-speed SIM/ME interface, including automatic detection and configuration of the voltage required by the connected SIM card or chip.

Both 1.8 V and 3 V SIM types are supported: activation and deactivation with an automatic voltage switch from 1.8 V to 3 V is implemented, according to the ISO-IEC 7816-3 specifications.

The **VSIM** supply output pin provides internal short circuit protection to limit the start-up current and protect the device in short circuit situations.

The SIM driver of the module supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM Card.

1.8.2 SIM card detection interface

The **GPIO5** pin is configured by default to detect the external SIM card mechanical / physical presence. The pin is configured as input, and it can sense SIM card presence as intended to be properly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **GPIO5** input pin is recognized as SIM card not present
- High logic level at **GPIO5** input pin is recognized as SIM card present

The SIM card detection function provided by the **GPIO5** pin is an optional feature that can be implemented / used or not according to the application requirements: an Unsolicited Result Code (URC) is generated each time that there is a change of status (for more details, see the u-blox AT commands manual [2], +UGPIOC, +CIND, +CMER AT commands).

The optional function “SIM card hot insertion/removal” can be additionally configured on the **GPIO5** pin by the specific AT command (see the u-blox AT commands manual [2], +UDCONF=50 AT command), in order to enable / disable the SIM interface upon detection of the external SIM card physical insertion / removal.

1.9 Serial communication interfaces

LARA-R6 series modules provide the following serial communication interfaces:

- Main UART interface: Universal asynchronous receiver/transmitter serial interface available for the communication with a host application processor, supporting AT and data communication, multiplexer functionality including virtual channel for GNSS tunneling, and FW update by means of FOAT (see section 1.9.1.1).
- Auxiliary UART interface: Universal asynchronous receiver/transmitter serial interface available for the communication with a host application processor, supporting AT and data communication, and FW update by means of FOAT (see section 1.9.1.2).
- USB interface: Universal Serial Bus 2.0 compliant interface available for the communication with a host application processor, supporting AT command and data communication, GNSS tunneling, FW update by means of the FOAT, FW update by means of the u-blox EasyFlash tool, and diagnostics (see section 1.9.2).
- I2C interface: I2C-bus compliant interface available for the communication with external u-blox GNSS chips or modules and with external I2C devices as an audio codec (see section 1.9.3).

1.9.1 UART interfaces

1.9.1.1 Main UART interface

LARA-R6 series modules include a main primary universal asynchronous receiver/transmitter serial interface (UART) for communication with an application host processor, supporting:

- AT / data communication
- Multiplexer protocol functionality, including virtual channel for GNSS data tunneling (see 1.9.1.3)
- FW upgrades by means of the FOAT feature

The UART interface provides RS-232 functionality conforming to ITU-T V.24 recommendation [3], with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state (for detailed electrical characteristics, see the LARA-R6 series data sheet [1]), providing:

- data lines (**RXD** as output, **TXD** as input),
- hardware flow control lines (**CTS** as output, **RTS** as input),
- modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output)[7].

The module is designed to operate as cellular modem, as data circuit-terminating equipment (DCE) according to the ITU-T V.24 recommendation [3]. A host application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

☞ UART signal names of the modules conform to the ITU-T V.24 [3]: e.g. **TXD** line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

The UART interface is configured by default in AT command mode: the module waits for AT command instructions and interprets all the characters received as commands to execute.

All the functionalities supported by the modules can be set and configured by AT commands:

- AT commands according to 3GPP TS 27.007 [4], 3GPP TS 27.005 [5], 3GPP TS 27.010 [6]
- u-blox AT commands (for the complete list and syntax, see the u-blox AT commands manual [2])

Hardware flow control is enabled by default, and flow control handshakes can be set by appropriate AT commands (see u-blox AT commands manual [2], &K, +IFC, \Q AT commands).

[7] Alternatively, **DTR**, **DSR**, **DCD** and **RI** pins can be mutually exclusively configured as auxiliary secondary UART interface.

The 115,200 b/s baud rate is enabled by default, and other baud rates can be set by appropriate AT command (see the u-blox AT commands manual [2], +IPR AT command).

The 8N1 (8 data bits, no parity, 1 stop bit) frame format configuration is enabled by default (illustrated in Figure 17), and other frame formats can be set by appropriate AT command (see the u-blox AT commands manual [2], +ICF AT command).

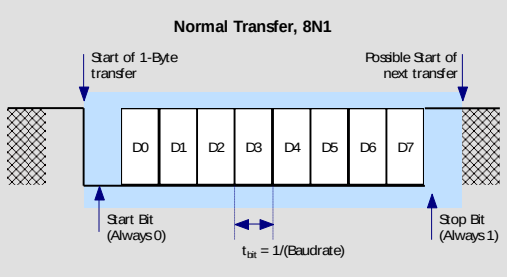

Figure 17: Description of the UART 8N1 frame format (8 data bits, no parity, 1 stop bit)

The UART interface of LARA-R6 series modules is available as the AT command interface with the default configuration described in Table 9 (for more details and information about further settings, see the u-blox AT commands manual [2]).

Interface	AT Settings	Comments
UART interface	AT interface: enabled	AT command interface is enabled by default on the UART physical interface
	AT+IPR=115200	115,200 b/s baud rate enabled by default
	AT+ICF=3,1	8N1 frame format enabled by default
	MUX protocol: disabled	Multiplexing mode is disabled by default and it can be enabled by the AT+CMUX command. For more details, see section 1.9.1.3.

Table 9: Default UART AT interface configuration

1.9.1.2 Auxiliary UART interface

The modules include an auxiliary secondary universal asynchronous receiver/transmitter serial interface (AUX UART) for communication with an application host processor, supporting:

- AT / data communication
- GNSS data tunneling
- FW upgrades by means of the FOAT feature

The auxiliary secondary UART interface is disabled by default, and it can be enabled by dedicated AT command (see the u-blox AT commands manual [2], +USIO AT command) as alternative function of the **DTR**, **DSR**, **DCD** and **RI** pins of the main primary UART interface, in mutually exclusive way.

The AUX UART interface provides RS-232 functionality conforming to ITU-T V.24 [3], with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state (for detailed electrical characteristics, see the LARA-R6 series data sheet [1]), providing:

- data lines (**DCD** as data output, **DTR** as data input),
- hardware flow control lines (**RI** as flow control output, **DSR** as flow control input).

Once the AUX UART interface is made available by +USIO AT command (see the u-blox AT commands manual [2]), the hardware flow control is enabled, and flow control handshakes can be set by related AT commands (see u-blox AT commands manual [2], &K, +IFC, \Q AT commands).

Similarly, once the AUX UART is made available, the 115,200 b/s baud rate and the 8N1 (8 data bits, no parity, 1 stop bit) frame format are enabled, and other configurations can be set by related AT commands (see the u-blox AT commands manual [2], +IPR, +ICF AT commands).

1.9.1.3 Multiplexer protocol

LARA-R6 series modules include multiplexer functionality on the main UART physical interface as per 3GPP TS 27.010 [6]. The multiplexer functionality is not supported on the auxiliary UART interface.

The multiplexer functionality is a data link protocol which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE), allowing several simultaneous sessions over the physical link (main primary UART): the user can concurrently use AT interface on one MUX channel and data communication on another MUX channel.

The following functions over dedicated virtual channels can be made available (for more details, see the u-blox AT commands manual [2], +CMUX, +USIO AT commands):

- Multiplexer control
- AT commands / data connection
- GNSS data tunneling

1.9.2 USB interface

LARA-R6 series modules include a High-Speed USB 2.0 compliant interface with a 480 Mbit/s maximum data rate, representing the main interface for transferring high speed data with a host application processor, supporting:

- AT / data communication
- GNSS data tunneling over dedicated channel
- FW upgrades by means of the FOAT feature
- FW upgrades by means of the u-blox EasyFlash tool
- Trace log capture (diagnostic purposes)

The module itself acts as a USB device and can be connected to a USB host such as a Personal Computer or an embedded application microprocessor equipped with compatible drivers.

The **USB_D+**/**USB_D-** lines carry USB serial bus data and signaling according to the Universal Serial Bus Revision 2.0 specification [7], while the **VUSB_DET** input pin senses the VBUS USB supply presence (nominally 5 V at the source) to detect the host connection and enable the interface.

The USB interface of the module is enabled only if a valid voltage is detected by the **VUSB_DET** input (see the LARA-R6 series data sheet [1]). Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs only a few microamperes.

The USB interface is controlled and operated with:

- AT commands according to 3GPP TS 27.007 [4], 3GPP TS 27.005 [5]
- u-blox AT commands (for the complete list and syntax, see the u-blox AT commands manual [2])

The USB interface of LARA-R6 series modules, according to the configured USB profile (see the u-blox AT commands manual [2], +USIO, +UUSBCONF AT commands), can provide several USB functions with various capabilities and purposes, such as:

- CDC-ACM for AT commands and data communication
- CDC-ACM for GNSS tunneling
- CDC-ACM for Diagnostic logs

It is not required to install a specific driver for each Linux-based or Android-based operating system to use the USB module interface, which is compatible with standard Linux/Android USB kernel drivers.

The full capability and configuration of the USB module interface can be reported by running “lsusb -v” or an equivalent command available in the host operating system when the module is connected.

1.9.3 I2C interface

LARA-R6 series modules include an I2C bus compliant interface (**SDA** and **SCL** pins), available for

- communication with external u-blox GNSS chips / modules,
- communication with other external I2C devices, as audio codecs.

The AT command interface is not available on the I2C interface.

The I2C device-mode operation is not supported: the LARA-R6 series module can act as the I2C host that can communicate with I2C devices in accordance with the I2C bus specifications [9].

The I2C interface pins of the module, serial data (**SDA**) and serial clock (**SCL**), are open drain outputs conforming to the I2C bus specifications [9].

u-blox has implemented special features to ease the design effort required for the integration of a u-blox cellular module with a u-blox GNSS receiver.

Combining a u-blox cellular module with a u-blox GNSS receiver allows designers to have full access to the positioning receiver directly via the cellular module: it relays control messages to the GNSS receiver via a dedicated I2C interface. A second interface connected to the positioning receiver is not necessary: AT commands and/or the GNSS data tunneling mode via the UART or USB serial interface of the cellular module allow for full control of the GNSS receiver from any host processor.

The modules feature embedded GNSS aiding, that is, a set of specific features developed by u-blox to enhance GNSS performance, decreasing the Time-To-First-Fix (TTFF), thus allowing the calculation of the position in a shorter time with higher accuracy:

- Local aiding
- AssistNow Online
- AssistNow Offline
- AssistNow Autonomous

The embedded GNSS aiding features can be used only if the I2C interface of the cellular module is connected to the u-blox GNSS receivers.

The cellular modules provide additional custom functions over GPIO pins to improve the integration with u-blox positioning chips and modules. GPIO pins can handle:

- External GNSS receiver power-on/off control: the “GNSS supply enable” function, available by default on the **GPIO2** pin.
- The wake-up from idle mode when the GNSS receiver is ready to send data: “GNSS Tx data ready” function, available by default on the **GPIO3** pin.

☞ For more details regarding the handling of the I2C interface, the GNSS aiding features and the GNSS related functions over GPIOs, see section 1.12, and the u-blox AT commands manual [2] (+UGPS, +UGPRF, +UGPIOC and I2C AT commands).

1.10 Audio interface

LARA-R6 series modules support Voice over LTE (VoLTE) as well as circuit-switched fall-back (CSFB) from LTE to 3G or 2G radio bearer for providing audio services.

LARA-R6 series modules include a 4-wire I2S digital audio interface (**I2S_TXD** data output, **I2S_RXD** data input, **I2S_CLK** clock output, **I2S_WA** world alignment / synchronization signal output), available for digital audio communication with external digital audio devices as an audio codec.

1.11 Clock output

LARA-R6 series modules provide digital clock output functionality on the **GPIO6** pin. This is mainly designed to feed the clock input of an external audio codec, as the clock output can be configured in "Audio dependent" mode (generated only when the audio is active), or in "Continuous" mode.

1.12 General Purpose Input/Output (GPIO)

LARA-R6 series modules include 9 pins (**GPIO1**-**GPIO5**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**) which can be configured as General Purpose Input/Output or to provide custom functions via u-blox AT commands (for more details, see the u-blox AT commands manual [2], +UGPIOC, +UGPIOR, +UGPIOW AT commands), as summarized in Table 10.

Function	Description	Default GPIO	Configurable GPIOs
Network status indication	Network status: registered home network, registered roaming, data transmission, no service	--	GPIO1-GPIO4
GNSS supply enable	Enable/disable the supply of u-blox GNSS receiver connected to the cellular module	GPIO2	GPIO1-GPIO4
GNSS data ready	Sense when u-blox GNSS receiver connected to the module is ready for sending data by the I2C	GPIO3	GPIO3
SIM card detection	External SIM card physical presence detection	GPIO5	GPIO5
SIM card hot insertion/removal	Enable / disable SIM interface upon detection of external SIM card physical insertion / removal	--	GPIO5
Last gasp	Input to trigger last gasp notification	--	GPIO3
Faster and safe power-off	Input to trigger emergency fast and safe shutdown of the module (as triggered by AT+CFUN=10 command)	--	GPIO3
I2S digital audio interface	I2S digital audio interface	I2S_RXD, I2S_TXD, I2S_CLK, I2S_WA	I2S_RXD, I2S_TXD, I2S_CLK, I2S_WA
General purpose input	Input to sense high or low digital level	--	All
General purpose output	Output to set the high or the low digital level	GPIO4	All
Pin disabled	Tri-state with an internal active pull-down enabled	GPIO1	All

Table 10: LARA-R6 series GPIO custom functions configuration

1.13 Reserved pins (RSVD)

LARA-R6 series modules have pins reserved for future use, named **RSVD**: they can all be left unconnected on the application board, except

- the **RSVD** pin number **33**, that is highly recommended to be externally connected to an accessible Test-Point for diagnostic

2 Design-in

2.1 Overview

For an optimal integration of LARA-R6 series modules in the final application board, follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the related interface, but a number of points require greater attention during the design of the application device.

The following list provides a ranking of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT1**, **ANT2** and **ANT_DET** pins.
   Antenna circuit directly affects the RF compliance of the device integrating a LARA-R6 series module with the applicable certification schemes. Very carefully follow the suggestions provided in section 2.4 for schematic and layout design.
2. Module supply: **VCC** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a LARA-R6 series module with applicable certification schemes as well as antenna circuit design. Very carefully follow the suggestions provided in section 2.2.1 for schematic and layout design.
3. USB interface: **USB_D+**, **USB_D-** and **VUSB_DET** pins.
   Accurate design is required to guarantee USB 2.0 high-speed interface functionality. Carefully follow the suggestions provided in the related section 2.6.2 for schematic and layout design.
4. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins.
   Accurate design is required to guarantee SIM card functionality and compliance with applicable conformance standards, also reducing the risk of RF coupling. Carefully follow the suggestions provided in section 2.5 for schematic and layout design.
5. System functions: **RESET_N**, **PWR_ON** pins.
   Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in section 2.3 for schematic and layout design.
6. Other digital interfaces: UARTs, I2C, I2S, GPIOs, and Reserved pins.
   Accurate design is required to guarantee proper functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in 2.6.1, 2.6.3, 2.7.1, 2.8 and 2.9 for schematic and layout design.
7. Other supply: the **V_INT** digital interfaces supply output.
   Accurate design is required to guarantee proper functionality. Follow the suggestions provided in sections 2.2.2 for schematic and layout design.

☞ It is recommended to follow the specific design guidelines provided by each manufacturer of any external part selected for the application board integrating the u-blox cellular modules.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All of the available **VCC** pins must be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected but connect all the available pins to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

LARA-R6 series modules must be supplied through the **VCC** pins by a proper DC power supply that should comply with the module **VCC** requirements summarized in Table 5.

The proper DC power supply can be selected according to application requirements (see Figure 18) between various possible supply sources types, of which the most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

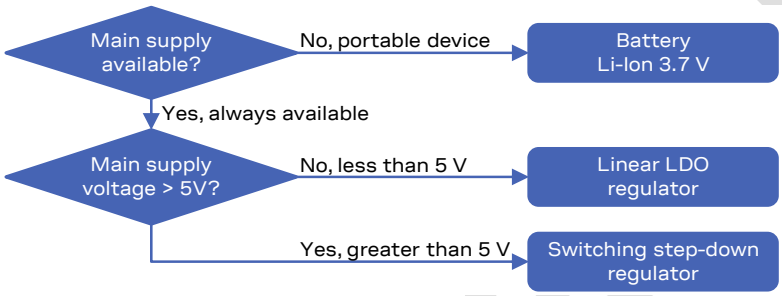

Figure 18: VCC supply concept selection

The DC/DC switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the modules **VCC** operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See sections 2.2.1.2 and 2.2.1.8, 2.2.1.10, 2.2.1.11, 2.2.1.12 for the specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See sections 2.2.1.3 and 2.2.1.8, 2.2.1.10, 2.2.1.11, 2.2.1.12 for the specific design-in.

If LARA-R6 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.6, 2.2.1.7, 2.2.1.8, 2.2.1.9, 2.2.1.10, 2.2.1.11, 2.2.1.12 for the specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit which is not included in the modules. The charger circuit must be designed to prevent over-voltage on the **VCC** pins, and it should be selected according to the application requirements: a

DC/DC switching charger is the typical choice when the charging source has an high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as a possible supply source, then a proper charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.6, 2.2.1.7, 2.2.1.4, 2.2.1.8, 2.2.1.9, 2.2.1.10, 2.2.1.11, 2.2.1.12 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected taking into account the maximum current specified in the LARA-R6 series data sheet [1] during connected mode, considering that primary cells might have weak power capability. See sections 2.2.1.5, 2.2.1.8, 2.2.1.9, 2.2.1.10, 2.2.1.11, 2.2.1.12 for the specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can be mutually exclusive.

The usage of a regulator or a battery not able to support the highest peak of **VCC** current consumption specified in the LARA-R6 series data sheet [1] is generally not recommended. However, if the selected regulator or battery is not able to support the highest peak current of the module, it must be able to support at least the highest averaged current consumption value specified in the LARA-R6 series data sheet [1] with an adequate margin. The additional energy required by the module during a 2G Tx slot can be provided by an appropriate bypass tank capacitor or super-capacitor with very large capacitance and very low ESR placed close to the module **VCC** pins. Depending on the actual capability of the selected regulator or battery, the required capacitance can be considerably larger than 1 mF and the required ESR can be in the range of few tens of mΩ. Carefully evaluate the super-capacitor characteristics, since aging and temperature may affect the actual characteristics.

The following sections highlight some design aspects for each of the supplies listed above, providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 5.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to the **VCC** pins should meet the following prerequisites to comply with the module's **VCC** requirements summarized in Table 5:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to the **VCC** pins the specified maximum peak / pulse current consumption during Tx burst at the maximum Tx power specified in the LARA-R6 series data sheet [1]
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications, it is recommended to select a switching frequency ≥ 600 kHz (since the L-C output filter is typically smaller for high switching frequencies). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be evaluated carefully, since this can produce noise in the **VCC** voltage profile and therefore negatively impact modulation spectrum performance.

- **PWM mode operation**: it is preferable to select regulators with a Pulse Width Modulation (PWM) mode. While in connected mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided in order to reduce noise on the **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the idle/active modes to connected mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 19 and the components listed in Table 11 show an example of a high reliability power supply circuit, where the **VCC** module is supplied by a step-down switching regulator capable of delivering the specified maximum peak / pulse current to the **VCC** pins, with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

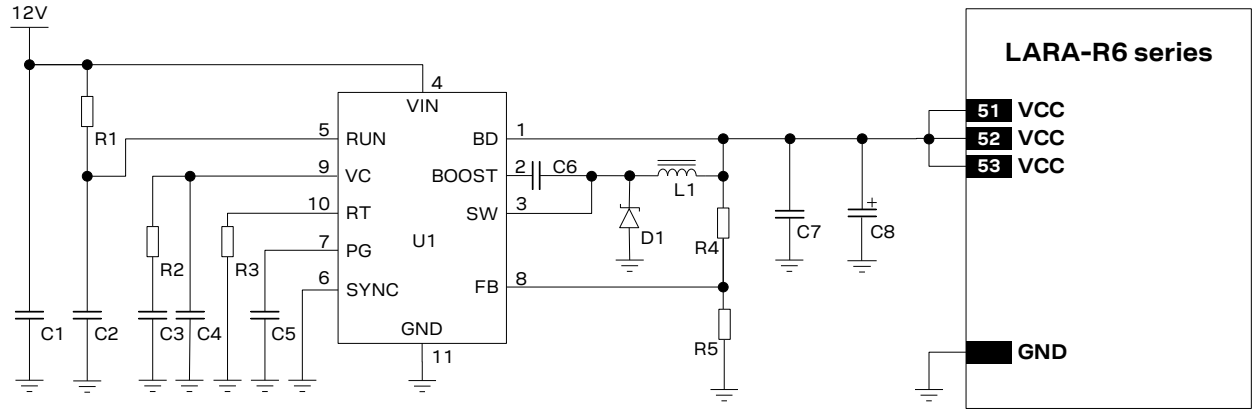

Figure 19: Example of high reliability VCC supply application circuit using a step-down regulator

Reference	Description	Part number - manufacturer
C1	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C7	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	15 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	22 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R4	390 kΩ Resistor 0402 1% 0.063 W	Various manufacturers
R5	100 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	Step-Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 11: Components for high reliability VCC supply application circuit using a step-down regulator

☞ See the section 2.2.1.8, and in particular Figure 26 / Table 17, for the parts recommended to be provided if the application device integrates an internal antenna.

Figure 20 and the components listed in Table 12 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by a step-down switching regulator capable of delivering the specified maximum peak / pulse current to the **VCC** pins, transforming a 12 V supply input.

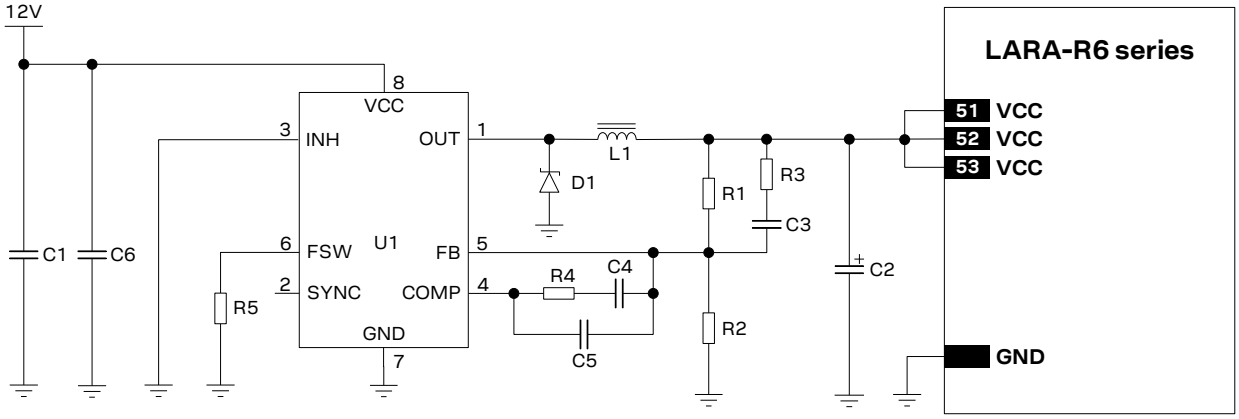

Figure 20: Example of low cost VCC supply application circuit using step-down regulator

Reference	Description	Part number - manufacturer
C1	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 – Murata
C2	100 µF Capacitor Tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H562KA88 – Murata
C4	6.8 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H682KA88 – Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H560JA01 – Murata
C6	220 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E224KA88 – Murata
D1	Schottky Diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 µH Inductor 30% 5.28A 22 mΩ	MSS1038-522NL – Coilcraft
R1	4.7 kΩ Resistor 0402 1% 0.063 W	Various manufacturers
R2	910 Ω Resistor 0402 1% 0.063 W	Various manufacturers
R3	82 Ω Resistor 0402 5% 0.063 W	Various manufacturers
R4	8.2 kΩ Resistor 0402 5% 0.063 W	Various manufacturers
R5	39 kΩ Resistor 0402 5% 0.063 W	Various manufacturers
U1	Step-Down Regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 12: Components for a low cost VCC supply application circuit using a step-down regulator

☞ See the section 2.2.1.8, and in particular Figure 26 / Table 17, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.3 Guidelines for VCC supply circuit design using a LDO linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following prerequisites to comply with the module's **VCC** requirements summarized in Table 5:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering the maximum peak / pulse current consumption to the **VCC** pins during a Tx burst at the maximum Tx power specified in the LARA-R6 series data sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the min output voltage to evaluate the power dissipation of the regulator).

Figure 21 and the components listed in Table 13 show an example of a high reliability power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator which is capable of delivering the specified highest peak / pulse current, with the proper power handling capability. The regulator described in this example supports a wide input voltage range, and it includes internal circuitry for reverse battery protection, current limiting, thermal limiting and reverse current protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V as in the circuit described in Figure 21 and Table 13). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

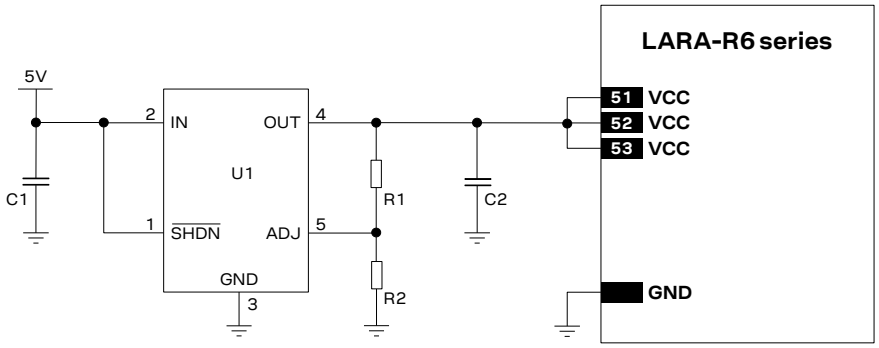

Figure 21: Example of a high reliability VCC supply application circuit using an LDO linear regulator

Reference	Description	Part number - manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	9.1 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	3.9 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 13: Components for a high reliability VCC supply application circuit using an LDO linear regulator

☞ See the section 2.2.1.8, and in particular Figure 26 / Table 17, for the parts recommended to be provided if the application device integrates an internal antenna.

Figure 22 and the components listed in Table 14 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified highest peak / pulse current, with the proper power handling capability. The regulator described in this example supports a limited input voltage range and it includes internal circuitry for current and thermal protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module VCC normal operating range (e.g. ~4.1 V as in the circuit described in Figure 22 and Table 14). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

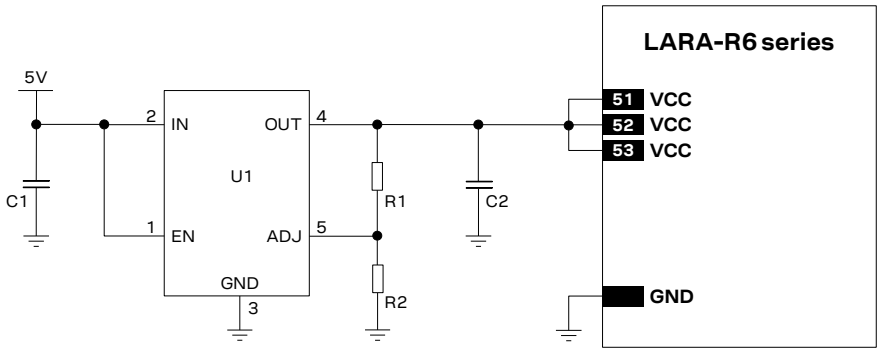

Figure 22: Example of a low cost VCC supply application circuit using an LDO linear regulator

Reference	Description	Part number - manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	27 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	4.7 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	LDO Linear Regulator ADJ 3.0 A	LP38501ATJ-ADJ/NOPB - Texas Instrument

Table 14: Components for a low cost VCC supply application circuit using an LDO linear regulator

☞ See the section 2.2.1.8, and in particular Figure 26 / Table 17, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering a pulse current as the maximum peak / pulse current consumption during a Tx burst at the maximum Tx power specified in the LARA-R6 series data sheet [1], and must be capable of extensively delivering a DC current as the maximum average current consumption specified in the LARA-R6 series data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 5 during transmit bursts.

2.2.1.5 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a primary (non-rechargeable) battery connected to the **VCC** pins should meet the following prerequisites to comply with the module's **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering a pulse current as the maximum peak current consumption during a Tx burst at the maximum Tx power specified in the LARA-R6 series data sheet [1], and must be capable of extensively delivering a DC current as the maximum average current consumption specified in the LARA-R6 series data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the max DC discharge current is typically almost equal to the battery capacity in amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a **VCC** voltage drop below the operating range summarized in Table 5 during transmit bursts.

2.2.1.6 Guidelines for external battery charging circuit

LARA-R6 series modules do not have an on-board charging circuit. Figure 23 provides an example of a battery charger design, suitable for applications powered with a Li-Ion (or Li-Polymer) battery.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features proper pulse and DC discharge current capabilities and proper DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB power source (5.0 V typ.), charges as a linear charger the battery, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA)
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 s.

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The L6924U, as a linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see the following section 2.2.1.7 for specific design-in).

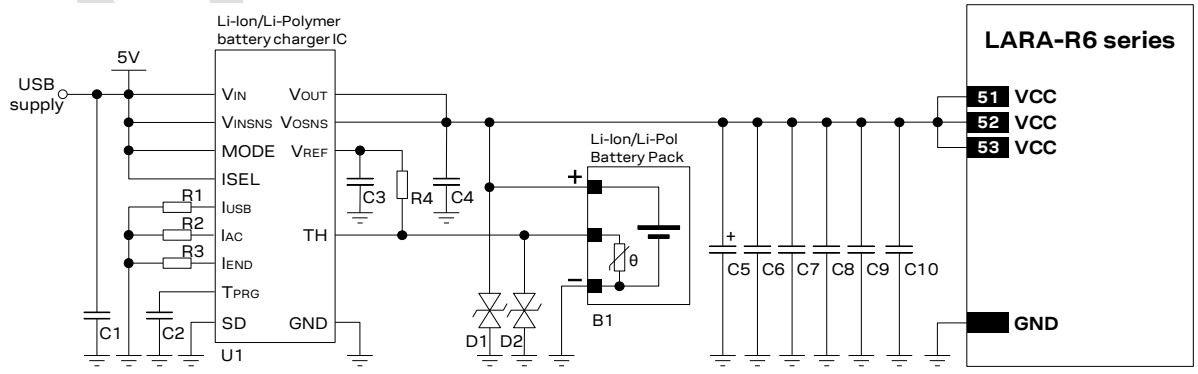

Figure 23: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part number - manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Various manufacturer
C1, C4	1 µF Capacitor Ceramic X7R 0603 10% 16 V	GRM188R71C105KA12 - Murata
C2, C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	1 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H102KA01 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C8	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C9	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C10	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R2	24 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	3.3 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R4	1.0 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC for USB port and AC Adapter	L6924U - STMicroelectronics

Table 15: Suggested components for a Li-Ion (or Li-Polymer) battery charging application circuit

☞ See the section 2.2.1.8, and in particular Figure 26 / Table 17, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.7 Guidelines for external charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as the possible supply source should implement a suitable charger / regulator with an integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 24 illustrates a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system: the power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- High efficiency internal step down converter, compliant with the performances specified in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

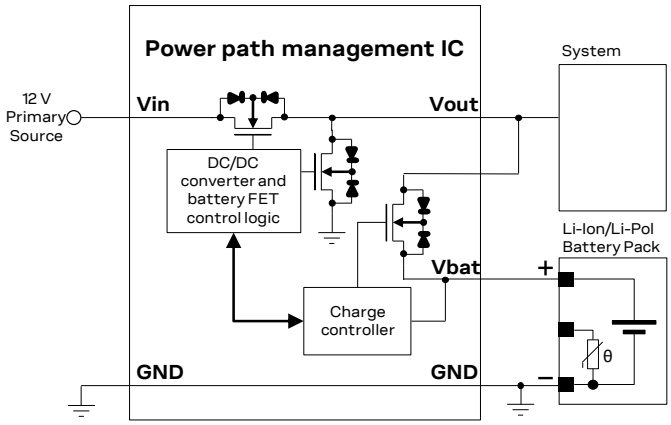

Figure 24: Charger / regulator with an integrated power path management circuit block diagram

Figure 25 and the components listed in Table 16 provide an application circuit example where the MPS MP2617H switching charger / regulator with an integrated power path management function provides the supply to the cellular module, while concurrently and autonomously charging a suitable Li-Ion (or Li-Polymer) battery with the proper pulse and DC discharge current capabilities and the proper DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617H IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as the supply source for the module, and starts a charging phase accordingly.

The MP2617H IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery conditions: the integrated switching step-down regulator is capable of provifing up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from the battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor.

Using a battery pack with an internal NTC resistor, the MP2617H IC can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters, such as the charging current, the charging timings, the input current limit, the input voltage limit, and the system output voltage, can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: proper resistors or capacitors must be accordingly connected to the related pins of the IC.

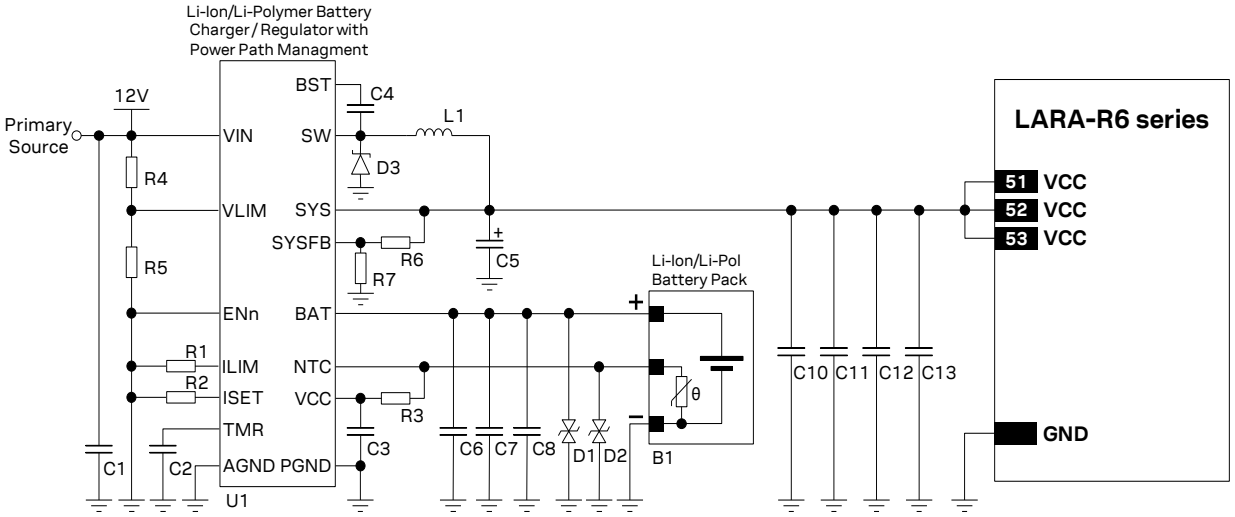

Figure 25: Li-Ion (or Li-Polymer) battery charging and power path management application circuit

Reference	Description	Part number - manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 10 kΩ NTC	Various manufacturer
C1, C6	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2, C4, C10	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	1 µF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7, C12	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C8, C13	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C11	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
D3	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
R1, R3, R5, R7	10 kΩ Resistor 0402 1% 1/16 W	Various manufacturers
R2	1.05 kΩ Resistor 0402 1% 0.1 W	Various manufacturers
R4	22 kΩ Resistor 0402 1% 1/16 W	Various manufacturers
R6	26.5 kΩ Resistor 0402 1% 1/16 W	Various manufacturers
L1	2.2 µH Inductor 7.4 A 13 mΩ 20%	SRN8040-2R2Y - Bourns
U1	Li-Ion/Li-Polymer Battery DC/DC Charger / Regulator with integrated Power Path Management function	MP2617H - Monolithic Power Systems (MPS)

Table 16: Suggested components for Li-Ion (or Li-Pol) battery charging and power path management application circuit

☞ See the section 2.2.1.8, and in particular Figure 26 / Table 17, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.8 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated for the **VCC** supply. Several pins are designated for the **GND** connection. It is recommended to properly connect all of them to supply the module to minimize series resistance losses.

Additional parts described in Figure 26 and Table 17 are recommended to be provided near the **VCC** pins of the module for various RF and/or EMI improvements purposes.

For modules supporting 2G or LTE TDD, to avoid voltage drop undershoot and overshoot at the start and end of a transmit burst and mitigate possible RF spurious emission, place a bypass capacitor with large capacitance (at least 100 µF) and low ESR near the **VCC** pins, for example:

- 330 µF capacitance, 45 mΩ ESR (e.g. KEMET T520D337M006ATE045, Tantalum Capacitor)

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins, narrowing the **VCC** line down to the pad of the capacitors, to improve the RF noise rejection in the band centered on the Self-Resonant Frequency of the capacitors:

- 82 pF 0402 ceramic capacitor with Self-Resonant Frequency in the 800/900 MHz range
- 15 pF 0402 ceramic capacitor with Self-Resonant Frequency in the 1800/1900 MHz range
- 8.2 pF 0402 ceramic capacitor with Self-Resonant Frequency in the 2500/2600 MHz range
- 10 nF 0402 ceramic capacitor, to filter digital logic noise from clocks and data sources
- 100 nF 0402 ceramic capacitor, to filter digital logic noise from clocks and data sources

An additional series ferrite bead can be properly placed on the **VCC** line for additional RF noise filtering, in particular if the application device integrates an internal antenna:

- Ferrite bead specifically designed for EMI / noise suppression in the ~GHz band (as the Murata BLM18EG221SN1), placed as close as possible to the **VCC** pins of the module, implementing the circuit described in Figure 26, to filter out EMI in all the cellular bands

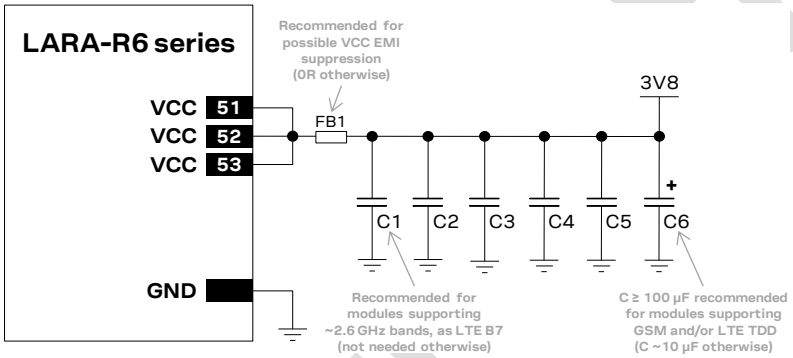

Figure 26: Suggested schematic for the VCC bypass capacitors to reduce ripple / noise on the supply voltage profile

Reference	Description	Part number - manufacturer
C1	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C2	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C3	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C6	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
FB1	Chip Ferrite Bead EMI Filter for GHz Band Noise 220 Ω at 100 MHz, 260 Ω at 1 GHz, 2000 mA	BLM18EG221SN1 - Murata

Table 17: Suggested components to reduce ripple / noise on VCC

☞ The necessity of each part depends on the specific design, but it is recommended to provide all the bypass capacitors described in Figure 26 / Table 17, and consider a ferrite bead designed for EMI suppression in the ~GHz band, if the application device integrates an internal antenna.

ESD sensitivity rating of the **VCC** pins is 1 kV (HBM as per JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, as if the accessible battery connector is directly connected to **VCC** pins. A higher protection level can be achieved by mounting an ESD protection (as EPCOS CA05P4S14THSG varistor) close to the accessible point.

2.2.1.9 Additional solution for VCC supply circuit design

LARA-R6 series modules provide separate supply inputs over the **VCC** pins (see Figure 3):

- **VCC** pins #52 and #53 represent the supply input for the internal RF power amplifiers, demanding most of the total current drawn when RF transmission is enabled during a voice/data call
- **VCC** pin #51 represents the supply input for the internal baseband Power Management Unit and the internal transceiver, demanding a minor part of the total current drawn of the module when RF transmission is enabled during a voice/data call

LARA-R6 series modules support two different extended operating voltage ranges: one for the **VCC** pins #52 and #53, and another one for the **VCC** pin #51 (see the LARA-R6 series data sheet [1]).

All the **VCC** pins are in general intended to be connected to the same external power supply circuit, but separate supply sources can be implemented for specific (e.g. battery-powered) applications considering that the voltage at the **VCC** pins #52 and #53 can drop to a value lower than the one at the **VCC** pin #51, keeping the module still switched-on and functional. Figure 27 describes a possible application circuit.

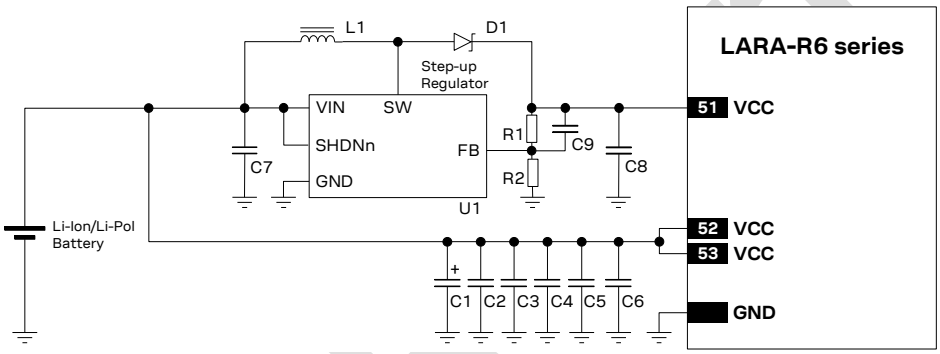

Figure 27: VCC circuit example with a separate supply for LARA-R6 series modules

Reference	Description	Part number - manufacturer
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C4	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C5	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C6	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C7	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C8	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C9	10 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E100JA01 - Murata
D1	Schottky Diode 40 V 1 A	SS14 - Vishay General Semiconductor
L1	10 µH Inductor 20% 1 A 276 mΩ	SRN3015-100M - Bourns Inc.
R1	1 MΩ Resistor 0402 5% 0.063 W	Various manufacturers
R2	412 kΩ Resistor 0402 5% 0.063 W	Various manufacturers
U1	Step-up Regulator 350 mA	AP3015 - Diodes Incorporated

Table 18: Example of components for VCC circuit with a separate supply for LARA-R6 series modules

2.2.1.10 Guidelines for removing VCC supply

As described in section 1.6.2, Figure 14 and Figure 15, the **VCC** supply can be removed after the end of LARA-R6 series modules internal power-off sequence, which must be properly started sending the AT+CPWROFF command (see the u-blox AT commands manual [2]). Removing the **VCC** power can be useful in order to minimize the current consumption when the LARA-R6 series modules are switched off. Afterwards, the modules can be switched on again by re-applying the **VCC** supply.

If the **VCC** supply is generated by a switching or an LDO regulator, the application processor may control the input pin of the regulator which is provided to enable / disable the output of the regulator (as for example, the RUN input pin for the regulator described in Figure 19, or the SHDNn input pin for the regulator described in Figure 21), in order to apply / remove the **VCC** supply.

If the regulator that generates the **VCC** supply does not provide an on / off pin, or for other applications such as the battery-powered ones, the **VCC** supply can be switched off using an appropriate external p-channel MOSFET controlled by the application processor by means of a proper inverting transistor as shown in Figure 28, given that the external pMOS has to provide:

- Very low $R_{DS(ON)}$ (for example, less than 50 mΩ), to minimize voltage drops
- Adequate maximum Drain current (see LARA-R6 series data sheet [1] for module consumption)
- Low leakage current, to minimize the consumption

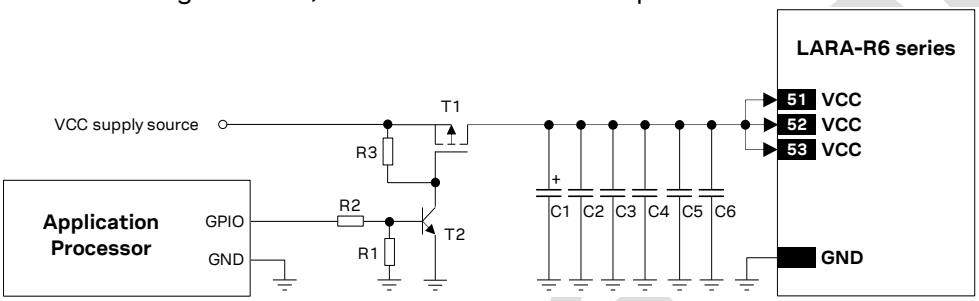

Figure 28: Example of application circuit for a VCC supply removal

Reference	Description	Part number - manufacturer
R1	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	10 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	100 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
T1	P-Channel MOSFET Low On-Resistance	AO3415 - Alpha & Omega Semiconductor Inc.
T2	NPN BJT Transistor	BC847 - Infineon
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C4	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C5	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C6	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata

Table 19: Components for a VCC supply removal application circuit

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during LARA-R6 series modules normal operations: the power-off procedure must be started by the AT+CPWROFF command, waiting the command response for a proper time period (see the u-blox AT commands manual [2]), and then a proper **VCC** supply must be held at least until the end of the modules' internal power-off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

2.2.1.11 Guidelines for VCC supply layout design

Good connection of the module **VCC** supply pins with a DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- The series resistance along the **VCC** path must be as minimum as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing.
- **VCC** connection must be routed as far as possible from the antenna, in particular if embedded in the application device: see Figure 29.
- **VCC** connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing.
- Coupling between **VCC** and audio lines (especially microphone inputs) must be avoided, because the typical GSM burst has a periodic nature of approximately 217 Hz, which lies in the audio range.
- The tank bypass capacitor with low ESR for current spikes smoothing described in section 2.2.1.8 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise, consider using separate large capacitors for the DC-DC converter and the cellular module.
- The bypass capacitors in the pF range described in section 2.2.1.8 should be placed as close as possible to the **VCC** pins, narrowing the **VCC** line down to the pad of the capacitors to improve the RF noise rejection in the band centered on the Self-Resonant Frequency of the pF capacitors. This is highly recommended if the device integrates an internal antenna.
- Since **VCC** is directly connected to RF Power Amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of the transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the LARA-R6 series modules in the worst case.
- Shielding of the switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency, high-power switching.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the cellular module, preferably closer to the DC source (otherwise protection functionality may be compromised).

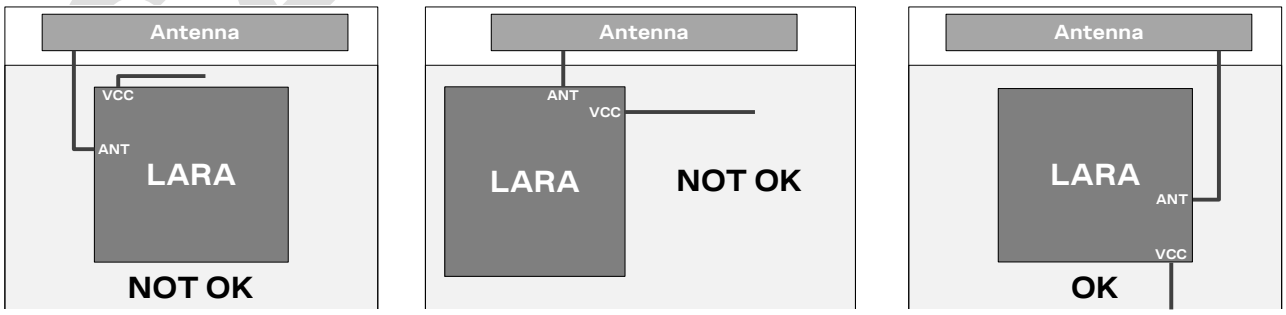

Figure 29: VCC line routing guideline for designs integrating an embedded antenna

2.2.1.12 Guidelines for grounding layout design

Good connection of the module **GND** pins with the application board solid ground layer is required for correct RF performance. It significantly improves RF and thermal heat sink figures for the module.

- Connect each **GND** pin with the application board solid GND layer. It is strongly recommended that each **GND** pin surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to the main DC source through GND as ground current: provide an adequate return path with a suitable uninterrupted ground plane to the main DC source.
- It is recommended to implement one layer of the application PCB as a ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with a complete via stack down to the main ground layer of the PCB. Use as many vias as possible to connect ground planes.
- Provide a dense line of vias at the edges of each GND area, in particular along RF and high speed lines.
- If the whole application device is composed of more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the multiple PCBs.
- Good grounding of **GND** pins also ensures thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating.

2.2.2 Interface supply (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

LARA-R6 series provide the **V_INT** 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on, outside PSM deep-sleep mode (see sections 1.4, 1.6.1, and 1.6.2 for more details)
- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply external voltage translators to connect the 1.8 V digital interfaces of the module to an external 3.0 V device (see section 2.6.1, 2.6.3, 2.7.1 for more details)
- Pull-up I2C interface signals (see section 2.6.3 for more details)
- Supply an external 1.8 V u-blox GNSS receiver (see section 2.6.3 for more details)
- Supply an external device as an external 1.8 V audio codec (see section 2.7.1 for more details)

The **V_INT** output pin provides internal short circuit protection to limit the start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply (see the LARA-R6 series data sheet [1]) as this can cause malfunctions in the internal circuitry.

☞ Since the **V_INT** supply is generated by an internal switching step-down regulator, the **V_INT** voltage ripple can range as specified in the LARA-R6 series data sheet [1]: it is not recommended to supply sensitive analog circuitry without adequate filtering for digital noise.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ ESD sensitivity rating of the **V_INT** pin is 1 kV (HBM as per JESD22-A114). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

☞ It is recommended to provide direct access to the **V_INT** pin on the application board by means of an accessible Test-Point directly connected to the **V_INT** pin, for diagnostic purpose.

2.2.2.2 Guidelines for V_INT layout design

The **V_INT** supply output is generated by an integrated switching step-down converter, used internally to supply the generic digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

LARA-R6 series modules' **PWR_ON** input line is internally pulled up as illustrated in Figure 30: an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 30 and Table 20.

☞ The ESD sensitivity rating of the **PWR_ON** pin is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, as if an accessible push button is directly connected to the **PWR_ON** pin, and it can be achieved by mounting an ESD protection (as EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as the pin is internally pulled up as illustrated in Figure 30.

☞ The **PWR_ON** input line should not be driven high, as it may cause start up issues.

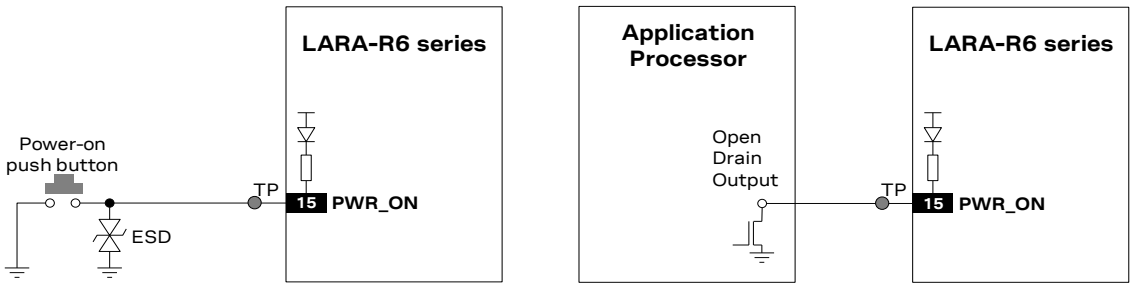

Figure 30: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Part number - manufacturer
ESD	Varistor array for ESD protection	CT0402S14AHSG - EPCOS

Table 20: Example of pull-up resistor and ESD protection for the PWR_ON application circuit

☞ It is recommended to provide direct access to the **PWR_ON** pin on the application board by means of an accessible Test-Point directly connected to the **PWR_ON** pin, for FW upgrade and/or for diagnostic purpose.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout since it is the sensitive input available to switch on the LARA-R6 series modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

LARA-R6 series modules' **RESET_N** input line is internally pulled up as illustrated in Figure 31: an external pull-up resistor is not required and should not be provided.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to the accessible point on the line connected to this pin, as described in Figure 31 and Table 21.

☞ The ESD sensitivity rating of the **RESET_N** pin is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the **RESET_N** pin, and it can be achieved by mounting an ESD protection (as EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain output is suitable to drive the **RESET_N** input from an application processor, as the line is internally pulled up as illustrated in Figure 31.

☞ **RESET_N** input should not be driven high by an external device, as it may cause start up issues.

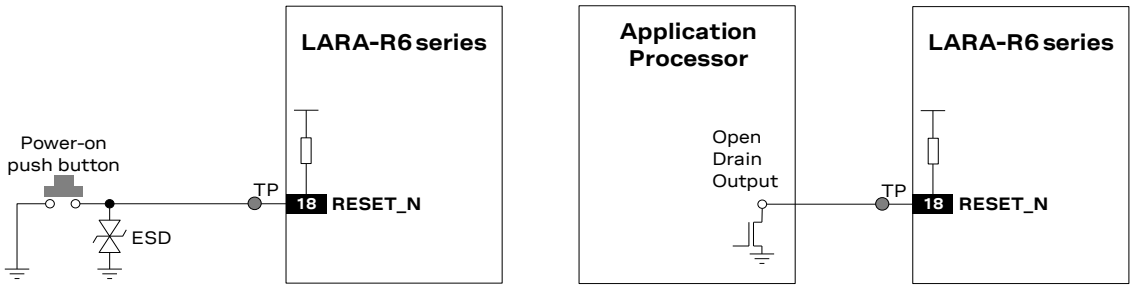

Figure 31: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Part number - manufacturer
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 21: Example of ESD protection component for the RESET_N application circuit

☞ If the external reset function is not required by the customer application, the **RESET_N** pin can be left unconnected to external components, but it is recommended to provide direct access on the application board by means of an accessible Test-Point directly connected to the **RESET_N** pin, for diagnostic purpose.

2.3.2.2 Guidelines for RESET_N layout design

The reset circuit (**RESET_N**) requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET_N** as short as possible.

2.4 Antenna interfaces

LARA-R6 series modules provide two RF interfaces for connecting the external antennas:

- **ANT1** represents the main RF input/output for LTE/3G/2G RF signals transmission and reception.
- **ANT2** represents the secondary RF input for LTE/3G Rx diversity RF signals reception.

Both the **ANT1** and the **ANT2** pins have a nominal characteristic impedance of 50 Ω and have to be connected to the related RF antenna system through a 50 Ω transmission line to allow proper transmission / reception of RF signals.

☞ Two antennas (one connected to **ANT1** pin and one connected to **ANT2** pin) must be used to support the LTE/3G Rx diversity radio technology. This is a required feature for LTE category 1 User Equipment (up to 10.2 Mb/s Down-Link data rate) according to the 3GPP specifications.

2.4.1 Antenna RF interface (ANT1 / ANT2)

2.4.1.1 General guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antennas from all perspectives at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating LARA-R6 series modules with all the applicable required certification schemes depends on the antenna radiating performance.

Cellular antennas are typically available in the types of linear monopole or PCB antennas such as patches or ceramic SMT elements.

- External antennas (e.g. linear monopole)
  - External antennas basically do not imply a physical restriction to the design of the PCB where the LARA-R6 series module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides proper PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
  - If antenna detection functionality is required, select an antenna assembly with a proper built-in diagnostic circuit with a resistor connected to ground: see guidelines in section 2.4.2.
- Integrated antennas (e.g. patch-like antennas):
  - Internal integrated antennas imply a physical restriction to the design of the PCB: integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that can be radiated. Thus, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that must be radiated, given that the orientation of the ground plane relative to the antenna element must be considered.
    As a numerical example, physical restriction to the PCB design can be considered as following:
    Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
    The isolation between the primary and the secondary antennas must be as high as possible and the correlation between the 3D radiation patterns of the two antennas must be as low as possible. In general, a separation of at least a quarter wavelength between the two antennas is required to achieve a good isolation and low pattern correlation.

- Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
- It is recommended to select a pair of custom antennas designed by an antennas' manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process.
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both cases, selecting external or internal antennas, these recommendations should be observed:

- Select antennas providing optimal return loss (or VSWR) figure over all the operating frequencies.
- Select antennas providing optimal efficiency figure over all the operating frequencies.
- Select antennas providing similar efficiency for both the primary (**ANT1**) and the secondary (**ANT2**) antenna.
- Select antennas providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in related countries (see the FCC United States notice reported in section 4.2.2, the ISED Canada notice reported in section 4.3.1, the RED Europe notice reported in section 4.4).
- Select antennas capable to provide low Envelope Correlation Coefficient between the primary (**ANT1**) and the secondary (**ANT2**) antenna: the 3D antenna radiation patterns should have lobes in different directions.

2.4.1.2 Guidelines for antenna RF interface design

Guidelines for ANT1 / ANT2 pins RF connection design

Proper transition between **ANT1** / **ANT2** pads and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT1** / **ANT2** pads:

- On a multilayer board, the whole layer stack below the RF connection should be free of digital lines.
- Increase GND keep-out (clearance) around **ANT1** / **ANT2** pads, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to GND, as described in the left example of Figure 32.
- Add GND keep-out (clearance) on the buried metal layer below **ANT1** / **ANT2** pads if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right example of Figure 32.

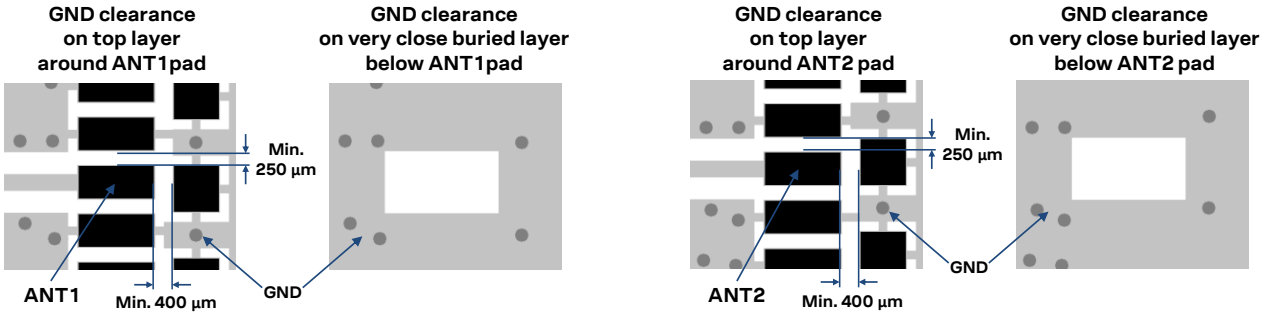

Figure 32: GND keep-out area on top layer around ANT1 / ANT2 pads and on very close buried layer below ANT1 / ANT2 pads

Guidelines for RF transmission line design

Any RF transmission line, such as the ones from the **ANT1** and **ANT2** pads up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.
RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit boards.

Figure 33 and Figure 34 provide two examples of proper 50 Ω coplanar waveguide designs. The first example of an RF transmission line can be implemented for a 4-layer PCB stack-up herein described, and the second example of an RF transmission line can be implemented for a 2-layer PCB stack-up herein described.

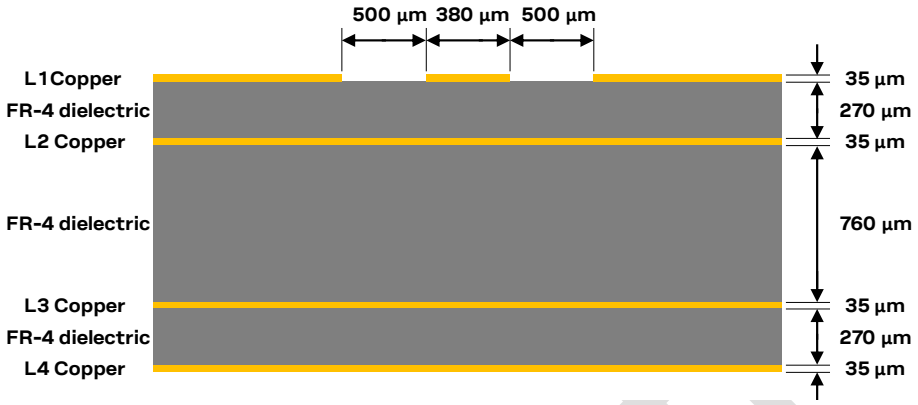

Figure 33: Example of a 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

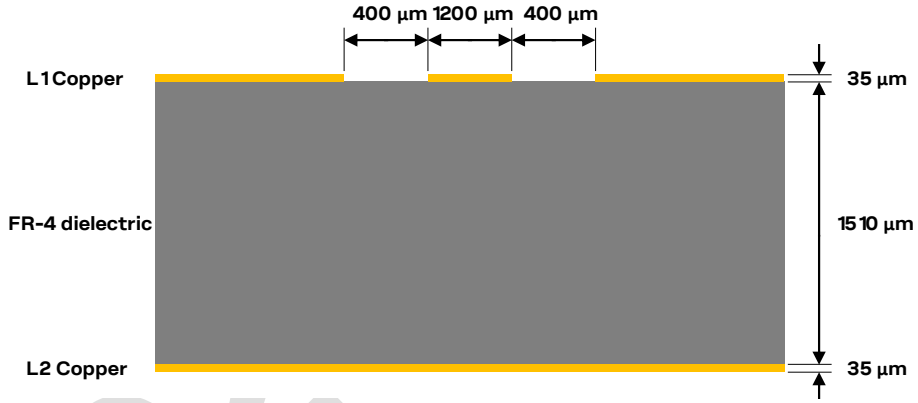

Figure 34: Example of a 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB layup, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the examples of Figure 33 and Figure 34)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 33, 1510 µm in Figure 34)

- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 33 and Figure 34)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 33, 400 µm in Figure 34)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for the transmission line design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission line, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground.
- The transmission line width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND vias around transmission line, as described in Figure 35.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to the main ground layer, providing enough on the adjacent metal layer, as described in Figure 35.
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as analog audio lines).
- Avoid stubs on the transmission line.
- Avoid signal routing in parallel to the transmission line or crossing the transmission line on buried metal layer.
- Do not route the microstrip line below discrete components or other mechanics placed on the top layer.

An example of proper RF circuit design is illustrated in Figure 35. In this case, the **ANT1** and **ANT2** pins are directly connected to SMA connectors by means of proper 50 Ω transmission lines, designed with proper layout.

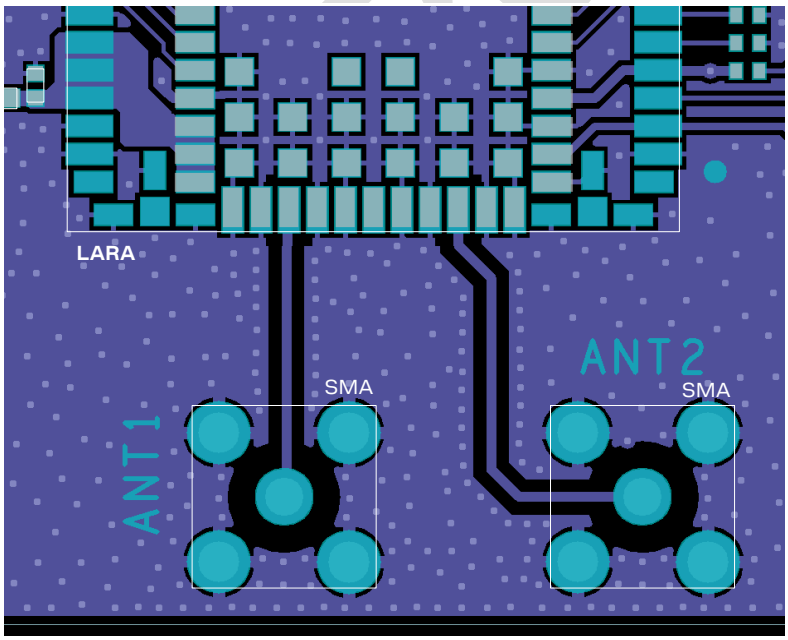

Figure 35: Example of the circuit and layout for antenna RF circuits on the application board

Guidelines for RF termination design

RF terminations must provide a characteristic impedance of 50 Ω as well as the RF transmission lines up to the RF terminations themselves, to match the characteristic impedance of the **ANT1** / **ANT2** ports of the modules.

However, real antennas do not have a perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible any performance degradation due to antennas mismatch, the RF terminations must provide optimal return loss (or VSWR) figure over all the operating frequencies, as summarized in Table 6 and Table 7.

If external antennas are used, the antenna connectors represent the RF termination on the PCB:

- Use suitable 50 Ω connectors providing proper PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts, as shown in Figure 35.
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads, as illustrated in Figure 36

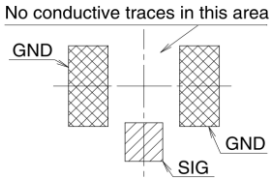

Figure 36: U.FL surface mounted connector mounting pattern layout

- Cut out the GND layer under RF connectors and close to buried vias, in order to remove stray capacitance and thus keep the RF line 50 Ω, e.g. the active pad of U.FL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

If integrated antennas are used, the RF terminations are represented by the integrated antennas themselves. The following guidelines should be followed:

- Use antennas designed by an antenna manufacturer, providing the best possible return loss (or VSWR).
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of a wavelength of the minimum frequency that must be radiated. As a numerical example,
  Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna matching relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place antennas within a closed metal case.
- Do not place the antennas in close vicinity to the end user since the emitted radiation in human tissue is limited by regulatory requirements.
- Place the antennas far from sensitive analog systems or employ countermeasures to reduce EMC issues.

- Take care of interaction between co-located RF systems since the cellular transmitted power may interact or disturb the performance of companion systems.
- Place the two LTE antennas providing low Envelope Correlation Coefficient (ECC) between primary (**ANT1**) and secondary (**ANT2**) antenna: the antenna 3D radiation patterns should have lobes in different directions. The ECC between the primary and secondary antennas needs to be enough low to comply with the radiated performance requirements specified by related certification schemes, as indicated in Table 8.
- Place the two LTE antennas providing enough high isolation (see Table 8) between primary (**ANT1**) and secondary (**ANT2**) antenna. The isolation depends on the distance between antennas (separation of at least a quarter wavelength required for good isolation), antenna type (using antennas with different polarization improves isolation), and the antenna 3D radiation patterns (uncorrelated patterns improve isolation).

Examples of antennas

Table 22 lists some examples of possible internal on-board surface-mount antennas.

Manufacturer	Part number	Product name	Description
Taoglas	PA.760.A	WarriorX	Wideband LTE SMD antenna 600..6000 MHz 40.0 x 5.0 x 6.0 mm
Taoglas	PA.740.A		Wideband LTE SMD antenna 698..4900 MHz 40.0 x 5.0 x 6.0 mm
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PA.711.A	Warrior II	GSM / WCDMA / LTE SMD Antenna Pairs with the Taoglas PA.710.A Warrior for LTE MIMO applications 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.26.A	Havok	LTE SMD dielectric antenna 617..960 MHz, 1710..2690 MHz 54.6 x 13.0 x 3.0 mm
Taoglas	PCS.66.A	Reach	Wideband LTE SMD antenna 600..6000 MHz 32.0 x 25.0 x 1.6 mm
Taoglas	PCS.06.A	Havok	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2690 MHz 42.0 x 10.0 x 3.0 mm
Antenova	SR4L002	Lucida	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm
AVX	P822601 / P822602		GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1710..2170 MHz, 2490..2700 MHz 50.0 x 8.0 x 3.2 mm
AVX	1002436		GSM / WCDMA / LTE vertical mount antenna 698..960 MHz, 1710..2700 MHz 50.6 x 19.6 x 1.6 mm
Fractus	NN03-310	TRIO mXTEND™	GSM / WCDMA / LTE SMD antenna 698..8000 MHz 30.0 x 3.0 x 1.0 mm

Manufacturer	Part number	Product name	Description
PulseLarsen Antennas	W3796	Domino	GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1427..1661 MHz, 1695..2200 MHz, 2300..2700 MHz 42.0 x 10.0 x 3.0 mm
TE Connectivity	2118310-1		GSM / WCDMA / LTE vertical mount antenna 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 74.0 x 10.6 x 1.6 mm
Molex	1462000001		GSM / WCDMA / LTE SMD antenna 698..960 MHz, 1700..2700 MHz 40.0 x 5.0 x 5.0 mm

Table 22: Examples of internal surface-mount antennas

Table 23 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

Manufacturer	Part number	Product name	Description
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE Antenna on flexible PCB with cable and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Taoglas	FXUB66.07.0150C	Maximus	GSM / WCDMA / LTE Antenna on flexible PCB with cable and U.FL 698..960 MHz, 1390..1435 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz, 3400..3600 MHz, 4800..6000 MHz 120.2 x 50.4 mm
Taoglas	FXUB70.A.07.C.001		GSM / WCDMA / LTE MIMO Antenna on flexible PCB with cable and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 182.2 x 21.2 mm
Ethertronics	1002289		GSM / WCDMA / LTE Antenna on flexible PCB with cable and U.FL 698..960 MHz, 1710..2700 MHz 50.0 x 8.0 x 3.2 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE Antenna on PCB with cable and U.FL 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm

Table 23: Examples of internal antennas with cable and connector

Table 24 lists some examples of possible external antennas.

Manufacturer	Part number	Product name	Description
Taoglas	GSA.8835.A.101111	Phoenix II	Wideband adhesive-mount antenna with cable and SMA(M) 600..6000 MHz 105 x 30 x 7.9 mm
Taoglas	GSA.8827.A.101111	Phoenix	Wideband adhesive-mount antenna with cable and SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2490..2690 MHz 105 x 30 x 7.7 mm
Taoglas	GSA.8842.A.105111		Wideband I-Bar adhesive antenna with cable and SMA(M) 617..960 MHz, 1710..2700 MHz, 4900..5850 MHz 176.5 x 59.2 x 13.6 mm
Taoglas	GSA.8845.A.105111		Wideband I-Bar adhesive antenna with cable and SMA(M) 450..470 MHz, 698..960 MHz, 1710..2700 MHz, 4900..5850 MHz 176.5 x 59.2 x 13.6 mm
Taoglas	TG.55.8113		LTE terminal mount monopole antenna with 90° hinged SMA(M) 617..960 MHz, 1427..2170 MHz, 2300..2690 MHz 172.0 x 23.88 x 13 mm

Manufacturer	Part number	Product name	Description
Taoglas	TG.35.8113W	Apex II	Wideband LTE dipole terminal antenna hinged SMA(M) 617..1200 MHz, 1710..2700 MHz, 4900..5900 MHz 224 x 58 x 13 mm
Taoglas	TG.30.8112		GSM / WCDMA / LTE swivel dipole antenna with SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz 148.6 x 49 x 10 mm
Taoglas	MA241.BI.001	Genesis	GSM / WCDMA / LTE MIMO 2in1 adhesive-mount combination antenna waterproof IP67 rated with cable and SMA(M) 698..960 MHz, 1710..2170 MHz, 2400..2700 MHz 205.8 x 58 x 12.4 mm
Laird Tech.	TRA6927M3PW-001		GSM / WCDMA / LTE screw-mount antenna with N-type(F) 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm
Laird Tech.	CMS69273		GSM / WCDMA / LTE ceiling-mount antenna with cable and N-type(F) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount antenna with N-type(M) 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Laird Tech.	CMD69273-30NM		GSM / WCDMA / LTE ceiling-mount MIMO antenna with cables & N-type(M) 698..960 MHz, 1710..2700 MHz 43.5 x Ø 218.7 mm
Pulse Electronics	WA700/2700SMA		GSM / WCDMA / LTE clip-mount MIMO antenna with cables and SMA(M) 698..960 MHz,1710..2700 MHz 149 x 127 x 5.1 mm

Table 24: Examples of external antennas

2.4.2 Antenna detection interface (ANT_DET)

2.4.2.1 Guidelines for ANT_DET circuit design

Figure 37 and Table 25 describe the recommended schematic / components for the antennas detection circuit that must be provided on the application board and for the diagnostic circuit that must be provided on the antennas' assembly to achieve primary and secondary antenna detection functionality.

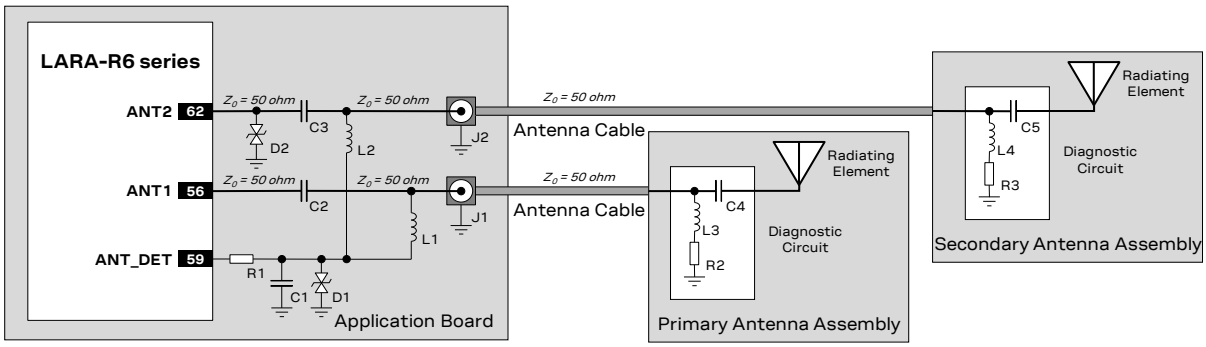

Figure 37: Suggested schematic for the antenna detection circuit on the application board and the diagnostic circuit on the antennas assembly

Reference	Description	Part number - manufacturer
C1	27 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2, C3	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
D2	Ultra Low Capacitance ESD Protection	ESD0P2RF-02LRH - Infineon
L1, L2	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	Various Manufacturers
J1, J2	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C4, C5	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3, L4	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2, R3	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 25: Suggested components for the antenna detection circuit on the application board and the diagnostic circuit on the antennas assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 37 and Table 25 are explained here:

- When antenna detection is forced by the AT+UANTR command, **ANT_DET** generates a DC current measuring the resistance (R2 // R3) from the antenna connectors (J1, J2) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT1** / **ANT2** pins (C2, C3) and at the antenna radiating element (C4, C5) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1, L2) and in series at the diagnostic resistor (L3, L4), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Additional components (R1, C1 and D1 in Figure 37) are needed at the **ANT_DET** pin as ESD protection
- The **ANT1** / **ANT2** pins must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at the RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 37, the measured DC resistance is always at the limits of the measurement range (respectively

open or short), and there is no means to distinguish between a defect on the antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for a PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from an ANT connector to a radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with a built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see the u-blox AT commands manual [2]) means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at the antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostics.
- The reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity or the measurement method used.

☞ If the primary / secondary antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT1** / **ANT2** pins can be directly connected to the related antenna connector by means of a 50 Ω transmission line as described in Figure 35.

2.4.2.2 Guidelines for ANT_DET layout design

The recommended layout for the primary antenna detection circuit to be provided on the application board to achieve the primary antenna detection functionality, implementing the recommended schematic described in Figure 37 and Table 25, is explained here:

- The **ANT1** / **ANT2** pins must be connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT1** / **ANT2** pins (C2, C3) must be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin must be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductors in series at the **ANT_DET** pin (L1, L2) must be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to **ANT_DET** pin.
- The additional components (R1, C1, D1) on the **ANT_DET** line must be placed as ESD protection.

2.5 SIM interface

2.5.1.1 Guidelines for SIM circuit design

Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC) which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the cellular network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP/SWP (Other function) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 6 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without an integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as:

- Case pin 8 = UICC contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case pin 7 = UICC contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case pin 6 = UICC contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case pin 5 = UICC contact C4 = AUX1 (Aux.contact) → It must be left not connected
- Case pin 1 = UICC contact C5 = GND (Ground) → It must be connected to **GND**
- Case pin 2 = UICC contact C6 = VPP/SWP (Other) → It can be left not connected
- Case pin 3 = UICC contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case pin 4 = UICC contact C8 = AUX2 (Aux. contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of LARA-R6 series modules as described in Figure 38, where the optional SIM detection feature is not implemented.

Follow these guidelines connecting the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially when the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Littelfuse PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: the ESD sensitivity rating of the SIM interface pins is 1 kV (HBM), so that, according to the EMC/ESD requirements of the custom application, a higher protection level can be required if the lines are externally accessible on the application device.
- Limit the capacitance and series resistance on each signal of the SIM interface (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the SIM interface specifications requirements (as for example, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines).

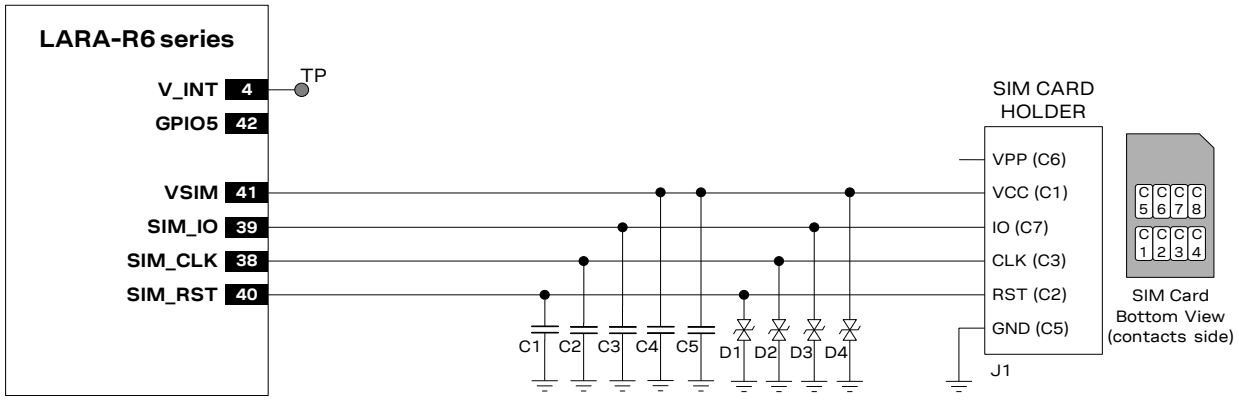

Figure 38: Application circuit for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part number - manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Littelfuse
J1	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, as C707 10M006 136 2 - Amphenol

Table 26: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

Guidelines for single SIM chip connection

A solderable SIM chip (M2M UICC Form Factor) must be connected the SIM card interface of LARA-R6 series modules as described in Figure 39.

Follow these guidelines, connecting the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**) close to the related pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Limit the capacitance and series resistance on each signal of the SIM interface (**SIM_CLK**, **SIM_IO**, **SIM_RST**) to match the SIM specifications requirements (as for example, 1.0 µs is the max allowed rise time on the **SIM_IO** and **SIM_RST** lines).

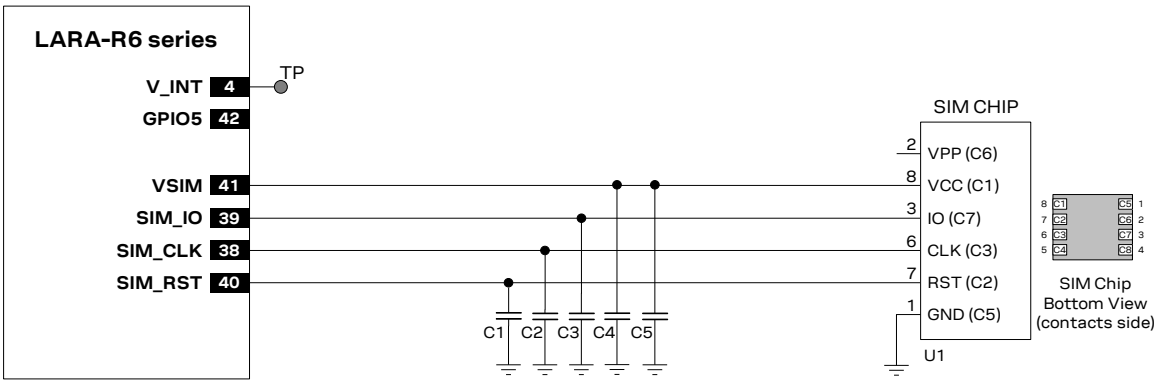

Figure 39: Application circuit for the connection to a single solderable SIM chip, with SIM detection not implemented

Reference	Description	Part number - manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 27: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented

Guidelines for single SIM card connection with detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of LARA-R6 series modules as described in Figure 40, where the optional SIM card detection feature is implemented.
Follow these guidelines connecting the module to a SIM connector implementing SIM detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW2 pin as described in Figure 40) to the **GPIO5** input pin of the module.
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW1 pin as described in Figure 40) to the **V_INT** 1.8 V supply output of the module by means of a strong (e.g. 1 kΩ) pull-up resistor, as the R1 resistor in Figure 40.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Littelfuse PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: the ESD sensitivity rating of SIM interface pins is 1 kV (HBM according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible.
- Limit the capacitance and series resistance on each SIM signal to match the SIM specifications (as for example, 1.0 µs is the max allowed rise time on the **SIM_IO** and **SIM_RST**).

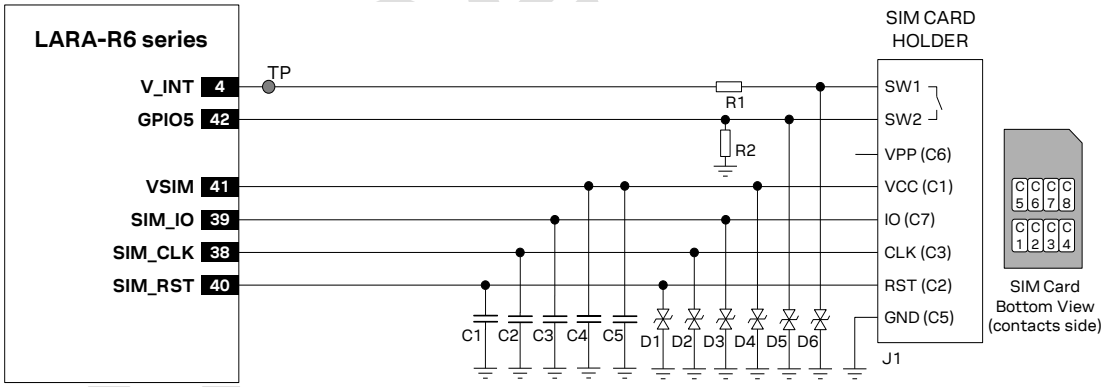

Figure 40: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part number - manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D6	Very Low Capacitance ESD Protection	PESD0402-140 - Littelfuse
R1	1 kΩ Resistor 0402 5% 0.1 W	Various Manufacturers
R2	470 kΩ Resistor 0402 5% 0.1 W	Various Manufacturers
J1	SIM Card Holder 6 + 2 positions, with card presence switch	Various Manufacturers, as CCM03-3013LFT R102 - C&K Components

Table 28: Example of components for the connection to a single removable SIM card, with SIM detection implemented

Guidelines for dual SIM card / chip connection

Two SIM cards / chips can be connected to LARA-R6 series modules' SIM interface as in Figure 41.

LARA-R6 series modules do not support the usage of two SIMs at the same time, but two SIMs can be populated on the application board, providing a proper switch to connect only the first or only the second SIM at a time to the SIM interface of the modules, as described in Figure 41.

LARA-R6 series modules support SIM hot insertion / removal on the **GPIO5** pin, to enable / disable SIM interface upon detection of external SIM card physical insertion / removal: if the feature is enabled using the specific AT commands (see sections 1.8.2 and 1.12, and the u-blox AT commands manual [2], +UGPIOC, +UDCONF=50 commands), the switch from the first SIM to the second SIM can be properly done when a Low logic level is present on the **GPIO5** pin ("SIM not inserted" = SIM interface not enabled), without the necessity of a module re-boot, so that the SIM interface will be re-enabled by the module to use the second SIM when a high logic level is re-applied on the **GPIO5**.

In the application circuit example represented in Figure 41, the application processor will drive the SIM switch using its own GPIO to properly select the SIM that is used by the module. Another GPIO may be used to handle the SIM hot insertion / removal function of LARA-R6 series modules, which can also be handled by other external circuits or by the cellular module GPIO according to the application requirements.

The dual SIM connection circuit described in Figure 41 can be implemented for SIM chips as well, providing proper connection between SIM switch and SIM chip as described in Figure 39.

If it is required to switch between more than 2 SIM, a circuit similar to the one described in Figure 41 can be implemented: for a 4 SIM circuit, using proper 4-throw switch instead of the suggested 2-throw switches.

Follow these guidelines connecting the module to two SIM connectors:

- Use a proper low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) 2-throw analog switch (e.g. Fairchild FSA2567) as SIM switch to ensure high-speed data transfer according to SIM requirements.
- Connect the contacts C1 (VCC) of the two UICC / SIM to the **VSIM** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C7 (I/O) of the two UICC / SIM to the **SIM_IO** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C3 (CLK) of the two UICC / SIM to the **SIM_CLK** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C2 (RST) of the two UICC / SIM to the **SIM_RST** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C5 (GND) of the two UICC / SIM to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the two SIM connectors, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the two SIM connectors, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holders.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Littelfuse PESD0402-140) on each externally accessible SIM line, close to each related pad of the two SIM connectors, according to the EMC/ESD requirements of the custom application.
- Limit capacitance and series resistance on each SIM signal to match the SIM specifications (as for example, 1.0 µs is the max allowed rise time on **SIM_IO** and **SIM_RST**).

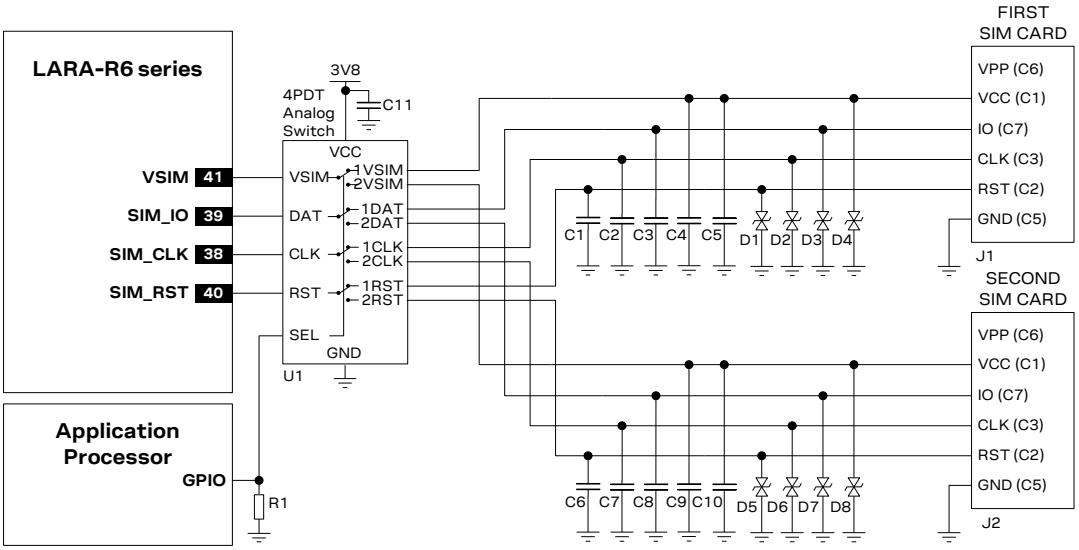

Figure 41: Application circuit for the connection to two removable SIM cards, with SIM detection not implemented

Reference	Description	Part number - manufacturer
C1 – C4, C6 – C9	33 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5, C10, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D8	Very Low Capacitance ESD Protection	PESD0402-140 - Littelfuse
R1	47 kΩ Resistor 0402 5% 0.1 W	Various Manufacturers
J1, J2	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, as C707 10M006 136 2 - Amphenol
U1	4PDT Analog Switch, with Low On-Capacitance and Low On-Resistance	FSA2567 - Fairchild Semiconductor

Table 29: Example of components for the connection to two removable SIM cards, with SIM detection not implemented

2.5.1.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the LARA-R6 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface: keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of cellular receiver channels whose carrier frequency is coincidental with harmonic frequencies: placing the RF bypass capacitors suggested in Figure 40 near the SIM connector will mitigate the problem.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection as suggested in Figure 40 to protect the module SIM pins near the SIM connector.

Limit the capacitance and series resistance on each SIM signal to match the SIM specifications: the connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Serial communication interfaces

2.6.1 UART interfaces

2.6.1.1 Guidelines for UART circuit design

Providing 1 UART with full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed, two different external voltage translators can be used to provide full RS-232 (with all the signal lines part of the complete V.24 link) functionality: e.g. using the Texas Instruments SN74AVC8T245PW for the translation from 1.8 V to 3.3 V, and the Maxim MAX3237E for the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V Application Processor (DTE) is used, and complete RS-232 function is required, the complete 1.8 V UART interface of the module (DCE) should be connected to a 1.8 V DTE, as in Figure 42.

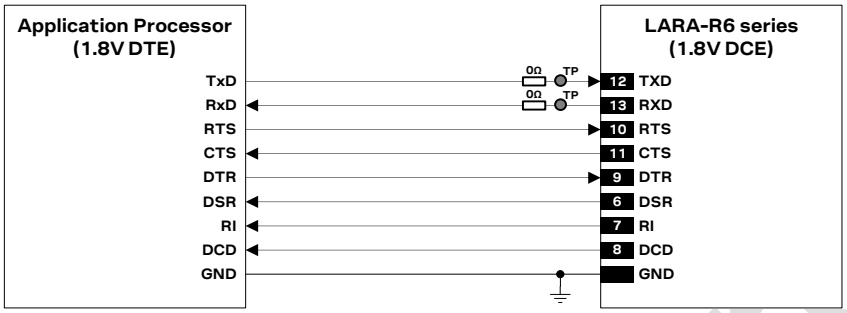

Figure 42: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as a 1.8 V supply for the voltage translators on the module side, as in Figure 43.

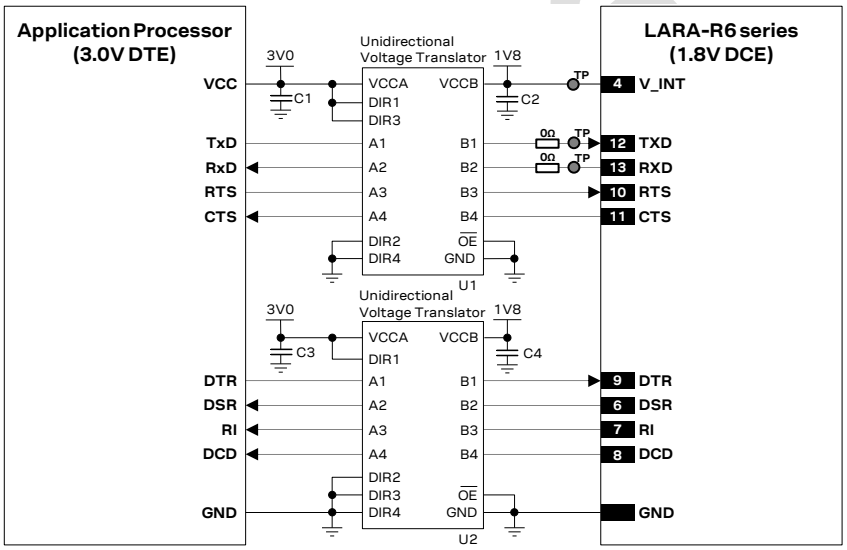

Figure 43: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic	Various Manufacturers
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774[9] - Texas Instruments

Table 30: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

[9] Voltage translator providing partial power down feature so that the 3 V supply can be ramped up before **V_INT** 1.8 V supply

Providing 1 UART with TXD, RXD, RTS and CTS lines only

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required, or the lines are not available:

- Connect the module **DTR** input to GND, since it may be useful to set **DTR** active if not specifically handled (see the u-blox AT commands manual [2], &D, S0, +CSGT, +CNMI AT commands)
- Leave the **DSR**, **DCD** and **RI** lines of the module floating

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor is used, the circuit should be implemented as described in Figure 44.

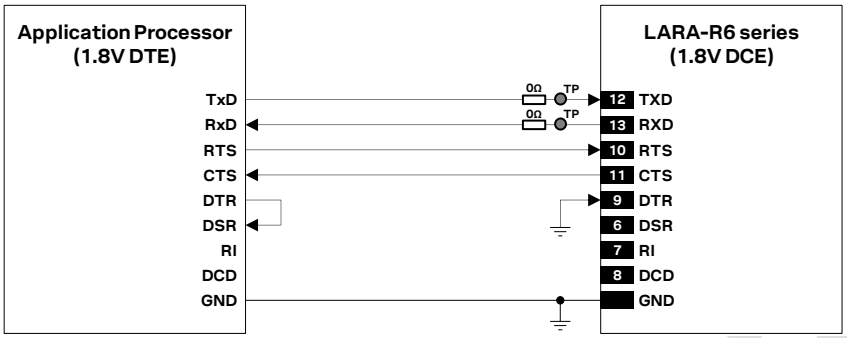

Figure 44: UART interface application circuit with partial V.24 link in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 45.

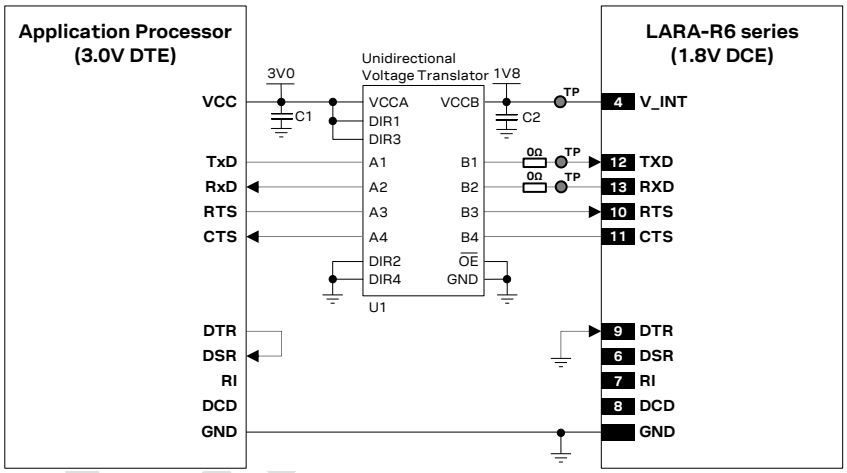

Figure 45: UART interface application circuit with partial V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - manufacturer
C1, C2	100 nF Capacitor Ceramic	Various Manufacturers
U1	Unidirectional Voltage Translator	SN74AVC4T774[11] - Texas Instruments

Table 31: Parts for UART application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

[11] Voltage translator providing partial power down feature so that the 3 V supply can be ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with TXD, RXD, RTS and CTS lines only

The auxiliary secondary UART interface is disabled by default, and it can be enabled by dedicated AT command (see the u-blox AT commands manual [2], +USIO AT command) as alternative function of the **DTR**, **DSR**, **DCD** and **RI** pins of the main primary UART interface, in mutually exclusive way.

If RS-232 compatible signal levels are needed, two Maxim MAX13234E voltage level translators can be used. These chips translate voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 46.

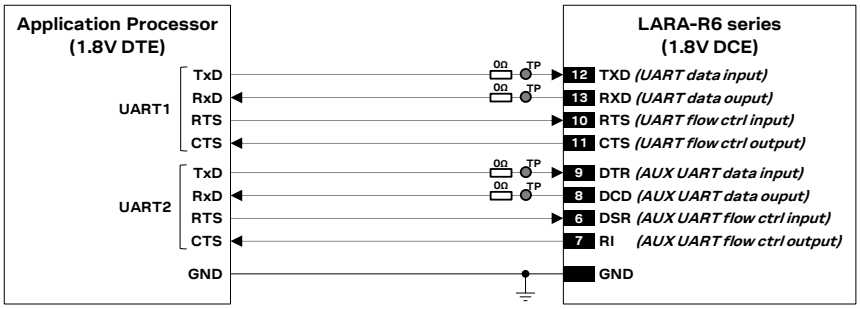

Figure 46: 2 UART interfaces application circuit with HW flow control in DTE/DCE serial communications (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 47.

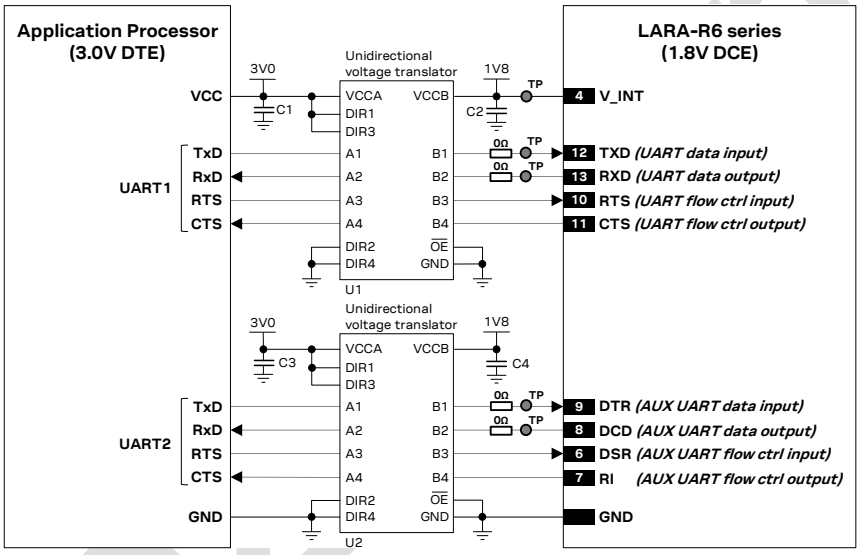

Figure 47: 2 UART interfaces application circuit with HW flow control in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic	Various Manufacturers
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [12] - Texas Instruments

Table 32: Components for 2 UARTs application circuit with HW flow control in DTE/DCE serial communications (3.0 V DTE)

[12] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with TXD and RXD lines only

☞ Providing the **TXD** and **RXD** lines only is not recommended if the multiplexer functionality is used in the application: providing also at least the HW flow control (**RTS** / **CTS** lines) is recommended, and it is in particular necessary if the low power mode is enabled by +UPSV AT command.

If the functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available:

- Connect the module **RTS** input line to GND: since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, which is the default setting).
- Connect the module **DTR** input to GND, since it may be useful to set **DTR** active if not specifically handled (see the u-blox AT commands manual [2], &D, S0, +CSGT, +CNMI AT commands)
- Leave the **DSR**, **DCD** and **RI** lines of the module floating, with a test-point on **DCD**

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.
If a 1.8 V Application Processor (DTE) is used, the circuit should be implemented as in Figure 48:

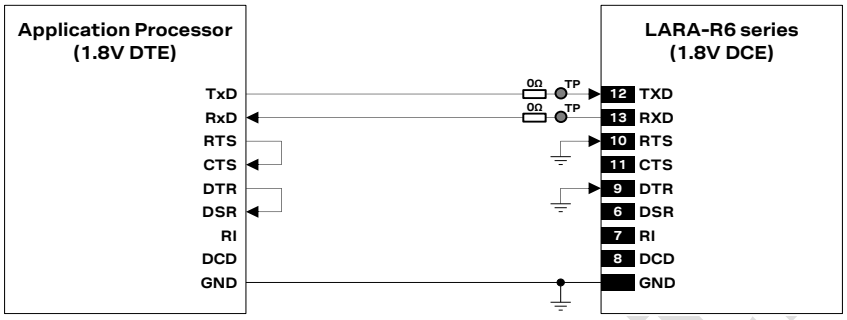

Figure 48: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3 V Application Processor (DTE) is used, it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as described in Figure 49.

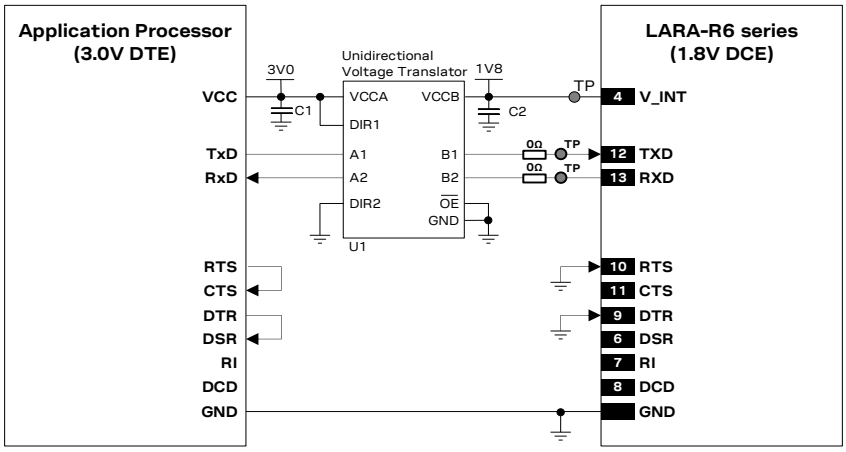

Figure 49: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - manufacturer
C1, C2	100 nF Capacitor Ceramic	Various Manufacturers
U1	Unidirectional Voltage Translator	SN74AVC2T245[13] - Texas Instruments

Table 33: Parts for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

[13] Voltage translator providing partial power down feature so that the 3 V supply can be ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with TXD and RXD lines only

☞ Providing the **TXD** and **RXD** lines only is not recommended if the multiplexer functionality is used in the application: providing also at least the HW flow control (**RTS** / **CTS** lines) is recommended, and it is in particular necessary if the low power mode is enabled by +UPSV AT command.

The auxiliary secondary UART interface is disabled by default, and it can be enabled by dedicated AT command (see the u-blox AT commands manual [2], +USIO AT command) as alternative function of the **DTR**, **DSR**, **DCD** and **RI** pins of the main primary UART interface, in mutually exclusive way.

If the HW flow-control functionality is not required in the application, or the lines are not available:

- Connect the module HW flow-control input line to GND: since the module requires HW flow-control active (low electrical level) if HW flow-control is enabled (AT&K3, which is the default setting).

If RS-232 compatible signal levels are needed, two Maxim MAX13234E voltage level translators can be used. These chips translate voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 50.

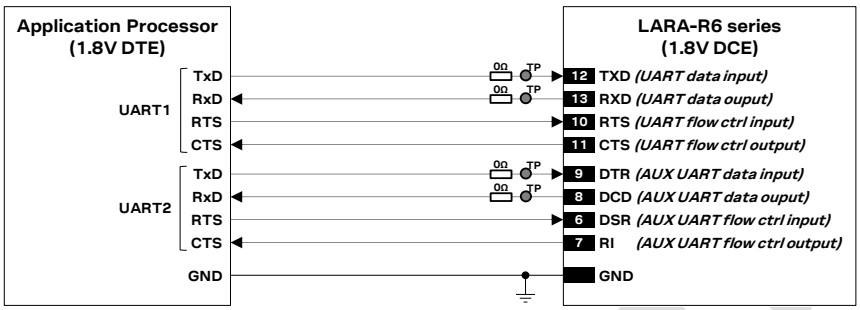

Figure 50: 2 UART interfaces application circuit without HW flow control in DTE/DCE serial communications (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 47.

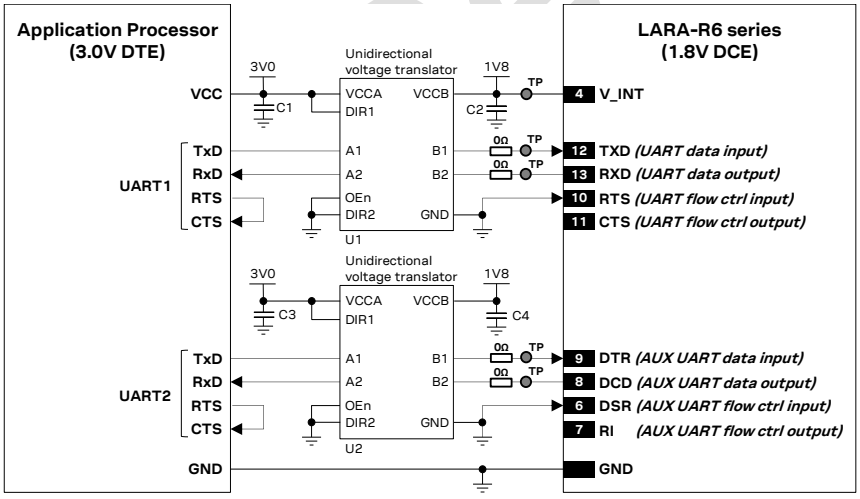

Figure 51: 2 UART interfaces application circuit without HW flow control in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic	Various Manufacturers
U1, U2	Unidirectional voltage translator	SN74AVC2T245[14] - Texas Instruments

Table 34: Components for 2 UARTs application circuit without HW flow ctrl in DTE/DCE serial communications (3.0 V DTE)

[14] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Additional considerations

If a 3.0 V Application Processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented, as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values and mind that any DTE signal connected to the module must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the corresponding 3.0 V input of the Application Processor (DTE) can be implemented by means of a proper low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

☞ Do not apply voltage to any UART interface pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module.

☞ The ESD sensitivity rating of the UART interface pins is 1 kV (Human Body Model according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

☞ It is recommended to consider providing accessible test points on the UART **TXD** / **RXD** data lines and on the AUX UART **DTR** / **DCD** data lines, with a 0 Ω series jumper on each line, to detach the application processor for diagnostic purposes.

2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same considerations regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 USB interface

2.6.2.1 Guidelines for USB circuit design

The **USB_D+** and **USB_D-** lines carry the USB serial data and signaling. The lines are used in single-ended mode for full speed signaling handshake, as well as in differential mode for high speed signaling and data transfer.

USB pull-up or pull-down resistors and external series resistors on **USB_D+** and **USB_D-** lines as required by the USB 2.0 specification [7] are part of the module USB pins driver and do not need to be externally provided.

The USB interface of the module is enabled only if a valid high logic level is detected by the **VUSB_DET** input (see the LARA-R6 series data sheet [1]). Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs few microamperes.

Routing the USB pins to a connector, they will be externally accessible on the application device. According to the EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to the accessible point on the line connected to this pin, as described in Figure 52 and Table 35.

☞ ESD sensitivity rating of USB pins is 1 kV (HBM as per JESD22-A114F). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Littelfuse PESD0402-140 ESD protection device) on the lines connected to these pins, close to accessible points.

The USB pins of the modules can be directly connected to the USB host application processor without additional ESD protections if they are not externally accessible

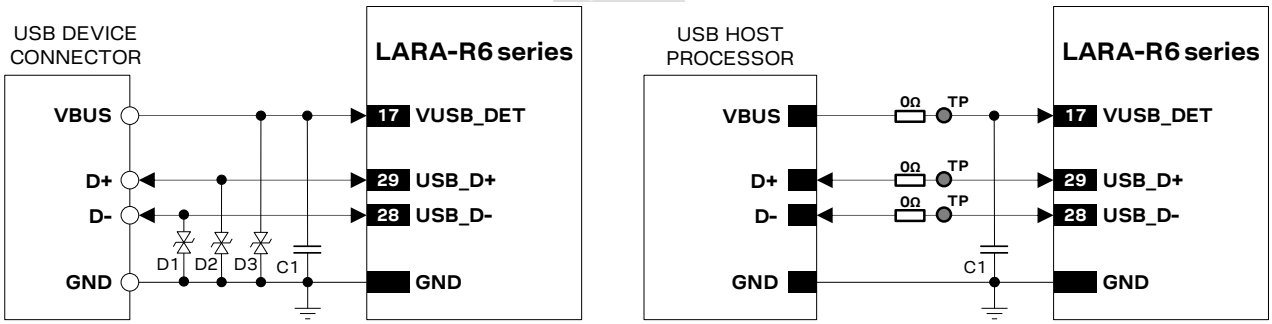

Figure 52: USB Interface application circuits

Reference	Description	Part number - manufacturer
C1	100 nF Capacitor Ceramic	Various Manufacturers
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Littelfuse

Table 35: Component for USB application circuits

☞ If the USB interface pins are not used, they can be left unconnected on the application board, but it is highly recommended to provide accessible Test-Points directly connected to the **VUSB_DET**, **USB_D+**, **USB_D-** pins, with a 0 Ω series jumper on each line to detach the external host processor for FW upgrade and/or for diagnostic purpose.

2.6.2.2 Guidelines for USB layout design

The **USB_D+** / **USB_D-** lines require accurate layout design to achieve reliable signaling at the high speed data rate (up to 480 Mb/s) supported by the USB serial interface.
The characteristic impedance of the **USB_D+** / **USB_D-** lines is specified by the Universal Serial Bus Revision 2.0 specification [7]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if the PCB layout is not optimal, especially when the USB signaling lines are very long.
Use the following general routing guidelines to minimize signal quality problems:

- Route **USB_D+** / **USB_D-** lines as a differential pair.
- Route **USB_D+** / **USB_D-** lines as short as possible.
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω.
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω.
- Consider design rules for **USB_D+** / **USB_D-** similar to RF transmission lines, these being coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area.
- Avoid coupling with any RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Figure 53 and Figure 54 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented for a 4-layer PCB stack-up herein described, the second transmission line can be implemented for a 2-layer PCB stack-up herein described.

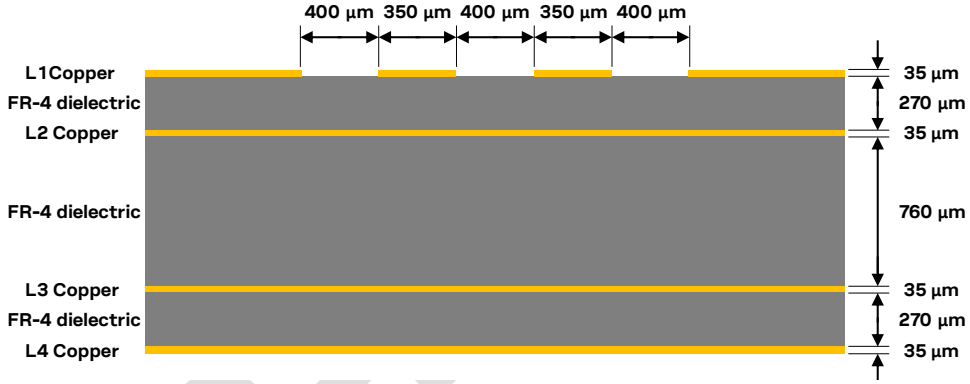

Figure 53: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 4-layer board layup

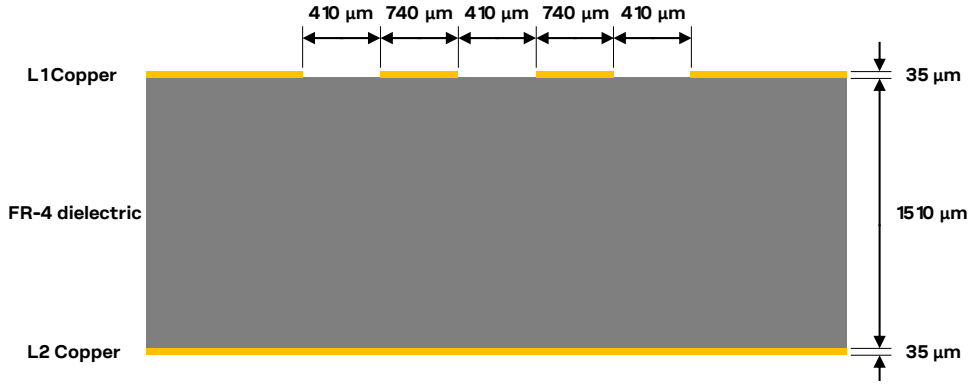

Figure 54: Example of USB line design, with Z0 close to 90 Ω and ZCM close to 30 Ω, for the described 2-layer board layup

2.6.3 I2C interface

2.6.3.1 Guidelines for I2C circuit design

General considerations

The I2C-bus interface can be used to communicate with external u-blox GNSS receivers and other external I2C-bus devices as an audio codec. Beside the general considerations explained below, see:

- the following parts of this section 2.6.3.1 for guidelines to connect external u-blox GNSS receivers.
- the section 2.7.1 for an application circuit example with an external audio codec I2C-bus device.

The **SDA** and **SCL** pins of the module are open drain output as per I2C bus specifications [9], and they have internal pull-up resistors to the **V_INT** 1.8 V supply rail, so there is no necessity of providing external pull-up resistors on the application board.

☞ Capacitance and series resistance must be limited on the bus to match the I2C specifications (maximum proper rise time for **SCL** / **SDA** lines is 1.0 µs): route connections as short as possible.

☞ Do not apply voltage to any UART interface pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module.

☞ The ESD sensitivity rating of the I2C pins is 1 kV (HBM as per JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

☞ If the pins are not used as I2C bus interface, they can be left unconnected.

Connection with u-blox 1.8 V GNSS receivers

Figure 55 shows an application circuit for connecting the module to a u-blox 1.8 V GNSS receiver:

- The **SDA** and **SCL** pins of the cellular module are directly connected to the related pins of the u-blox 1.8 V GNSS receiver, with appropriate pull-up resistors connected to the 1.8 V GNSS supply enabled after the **V_INT** supply of the I2C pins of the cellular module.
- The **GPIO2** pin is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 1.8 V GNSS receiver, providing the “GNSS supply enable” function. A pull-down resistor is provided to avoid a switch-on of the GNSS when LARA-R6 is switched off or in PSM deep-sleep.
- The **GPIO3** pin is directly connected to the **TXD1** pins of the u-blox 1.8 V GNSS receiver providing “GNSS Tx data ready” function.

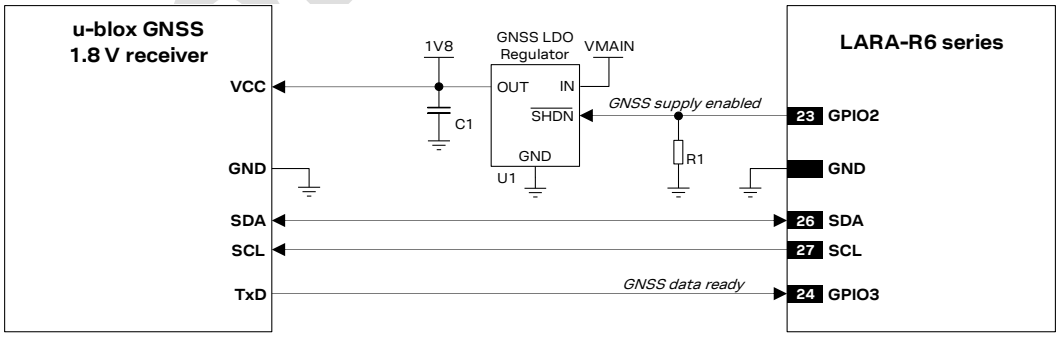

Figure 55: Application circuit for connecting LARA-R6 series modules to u-blox 1.8 V GNSS receivers

Reference	Description	Part number - manufacturer
R1	47 kΩ Resistor	Various Manufacturers
U1, C1	Voltage Regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver Hardware Integration Manual

Table 36: Components for connecting LARA-R6 series modules to u-blox 1.8 V GNSS receivers

Figure 56 illustrates an alternative solution as a supply circuit for u-blox 1.8 V GNSS receivers, using the **V_INT** 1.8 V supply output of the cellular module, generated by an internal linear LDO regulator, to supply an external u-blox 1.8 V GNSS receiver instead of using an external voltage regulator as in the previous Figure 55. The **V_INT** 1.8 V supply output of the cellular module can sustain the maximum current consumption of the u-blox 1.8 V GNSS receivers.

The internal linear LDO regulator that generates the **V_INT** supply is set to 1.8 V (typical) when the cellular module is switched on, and it is disabled when the cellular module is switched off or when the cellular module is in the PSM deep-sleep mode: in such cases, implementing the circuit illustrated in Figure 56, the external u-blox 1.8 V GNSS receiver will result not supplied when the cellular module is switched off or when the cellular module is in the PSM deep-sleep mode.

In the application circuit example illustrated in Figure 56, the supply of the u-blox 1.8 V GNSS receiver is switched on/off using an external p-channel MOSFET controlled by the **GPIO2** output of the cellular module by means of a proper inverting transistor, implementing the “GNSS supply enable” function. If this feature is not required, the **V_INT** supply output can be directly connected to the u-blox 1.8 V GNSS receiver, so that it will be switched on when the **V_INT** output is enabled.

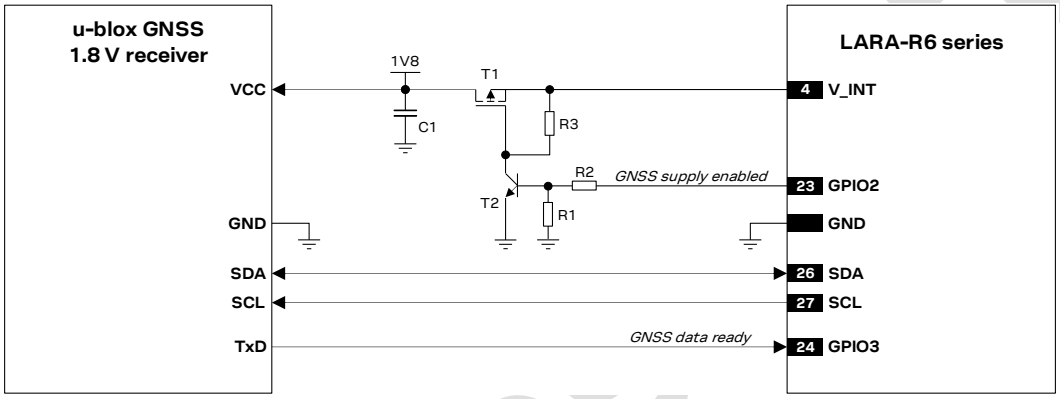

Figure 56: Application circuit for connecting LARA-R6 series modules to u-blox 1.8 V GNSS receivers using V_INT as supply

Reference	Description	Part number - manufacturer
R1	47 kΩ Resistor	Various Manufacturers
R2	10 kΩ Resistor	Various Manufacturers
R3	100 kΩ Resistor	Various Manufacturers
T1	P-Channel MOSFET Low On-Resistance	IRLML6401 - International Rectifier or NTZS3151P - ON Semi
T2	NPN BJT Transistor	BC847 - Infineon
C1	100 nF Capacitor Ceramic	Various Manufacturers

Table 37: Components for connecting LARA-R6 series modules to u-blox 1.8 V GNSS receivers using V_INT as supply

For additional guidelines regarding the design of applications with u-blox 1.8 V GNSS receivers, see the GNSS implementation application note [20] and the Hardware Integration Manual of the selected u-blox GNSS receiver. It is recommended to consider and implement all the possible measures for proper RF coexistence of the Cellular and the GNSS systems.

Connection with u-blox 3.0 V GNSS receivers

Figure 57 shows an application circuit for connecting the module to a u-blox 3.0 V GNSS receiver:

- The 1.8 V pins **SDA** and **SCL** of the cellular module are connected to the related pins of the u-blox 3.0 V GNSS receiver using a proper I2C-bus Bidirectional Voltage Translator (as the TI TCA9406), with pull-up resistors where appropriate.
- The **GPIO2** is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 3.0 V GNSS receiver providing the "GNSS supply enable" function. A pull-down resistor is provided to avoid a switch-on of the positioning receiver when the cellular module is switched off or in the PSM deep-sleep state.
- The 1.8 V pin **GPIO3** of the cellular module is connected to the related pin of the u-blox 3.0 V GNSS receiver implementing the "GNSS Tx data ready" function using a proper Unidirectional Voltage Translator (as the TI SN74AVC2T245).

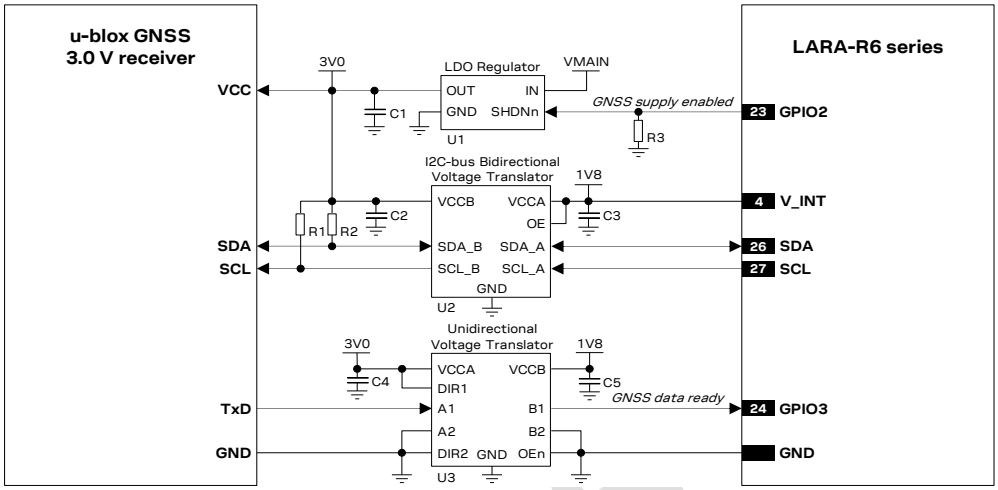

Figure 57: Application circuit for connecting LARA-R6 series modules to u-blox 3.0 V GNSS receivers

Reference	Description	Part number - manufacturer
R1, R2, R4, R5	4.7 kΩ Resistor	Various Manufacturers
R3	47 kΩ Resistor	Various Manufacturers
C2, C3, C4, C5	100 nF Capacitor Ceramic	Various Manufacturers
U1, C1	Voltage Regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver Hardware Integration Manual
U2	I2C-bus Bidirectional Voltage Translator	TCA9406DCUR [15] - Texas Instruments
U3	Unidirectional Voltage Translator	SN74AVC2T245 [15] - Texas Instruments

Table 38: Components for connecting LARA-R6 series modules to u-blox 3.0 V GNSS receivers

For additional guidelines regarding the design of applications with u-blox 3.0 V GNSS receivers, see the GNSS implementation application note [20] and the Hardware Integration Manual of the selected u-blox GNSS receiver. It is recommended to consider and implement all the possible measures for proper RF coexistence of the Cellular and the GNSS systems.

2.6.3.2 Guidelines for I2C layout design

The I2C serial interface requires the same considerations regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

[15] Voltage Translator providing the partial power down feature for back-drive protection.

2.7 Audio interface

2.7.1 Digital audio interface

2.7.1.1 Guidelines for digital audio circuit design

I2S digital audio interface can be connected to an external digital audio device for voice applications.

Any external digital audio device compliant with the configuration of the digital audio interface of the LARA-R6 series cellular module can be used.

An appropriate specific audio application circuit must be implemented and configured according to the selected external digital audio device or audio codec, and according to the general application requirements regarding the audio system.

Figure 58 and Table 39 describe an application circuit for the I2S digital audio interface providing basic voice capability using an external audio voice codec, in particular the Maxim MAX9860 audio codec:

- DAC and ADC integrated in the external audio codec respectively converts an incoming digital data stream to analog audio output through a mono amplifier and converts the microphone input signal to the digital bit stream over the digital audio interface,
- A digital side-tone mixer integrated in the external audio codec provides loopback of the microphones/ADC signal to the DAC/headphone output.
- The module's I2S interface (I2S host) is connected to the related pins of the external audio codec (I2S local device).
- The **GPIO6** digital clock output is connected to the clock input of the external audio codec to provide clock reference.
- The external audio codec is controlled by the LARA-R6 series module using the I2C interface, which can concurrently communicate with other I2C devices and control an external audio codec.
- The **V_INT** 1.8 V supply output is connected to the supply input pins of the external audio codec.
- Additional components are provided for EMC / EMI / ESD immunity: a 10 nF bypass capacitor and a series ferrite bead noise/EMI suppression filter provided on each microphone line and speaker line of the external codec. The necessity of these or other additional parts for possible EMC, EMI or ESD immunity improvement may depend on the specific application board design.

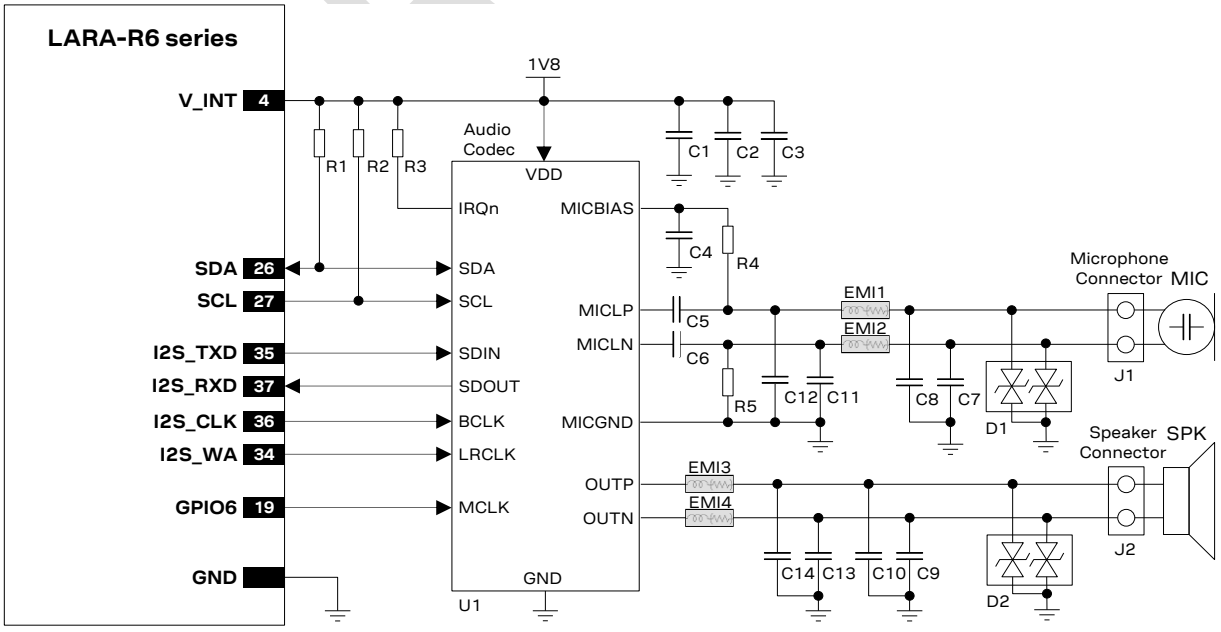

Figure 58: I2S interface application circuit with an external audio codec to provide voice capability

Reference	Description	Part number - manufacturer
C1	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
C2, C4, C5, C6	1 µF Capacitor Ceramic X5R 0402 10% 6.3 V	GRM155R60J105KE19 – Murata
C3	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C7, C8, C9, C10	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 – Murata
C11, C12, C13, C14	10 nF Capacitor Ceramic X5R 0402 10% 50V	GRM155R71C103KA88 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
EMI1, EMI2, EMI3, EMI4	Chip Ferrite Bead Noise/EMI Suppression Filter 1800 Ohm at 100 MHz, 2700 Ohm at 1 GHz	BLM15HD182SN1 – Murata
J1	Microphone Connector	Various manufacturers
J2	Speaker Connector	Various manufacturers
MIC	2.2 kΩ Electret Microphone	Various manufacturers
R1, R2	4.7 kΩ Resistor	Various manufacturers
R3	10 kΩ Resistor	Various manufacturers
R4, R5	2.2 kΩ Resistor	Various manufacturers
SPK	32 Ω Speaker	Various manufacturers
U1	16-Bit Mono Audio Voice Codec	MAX9860ETG+ - Maxim

Table 39: Example of components for audio voice codec application circuit

- Do not apply voltage to any I2S pin before the switch-on of I2S supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module.
- The ESD sensitivity rating of I2S interface pins is 1 kV (HBM according to JESD22-A114). A higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.
- If the I2S digital audio pins are not used, they can be left unconnected on the application board.

2.7.1.2 Guidelines for digital audio layout design

I2S interface and clock output lines require the same consideration regarding electro-magnetic interference as any other high speed digital interface. Keep the traces short and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.7.1.3 Guidelines for analog audio layout design

Accurate design of the analog audio circuit is very important to obtain clear and high quality audio. The GSM signal burst has a repetition rate of 217 Hz that lies in the audible range. A careful layout is required to reduce the risk of noise from audio lines due to both **VCC** burst noise coupling and RF detection.

General guidelines for the uplink path (microphone), which is commonly the most sensitive, are the following:

- Avoid coupling of any noisy signal to microphone lines: it is strongly recommended to route microphone lines away from the module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Avoid coupling between the microphone and speaker / receiver lines.

- Optimize the mechanical design of the application device, the position, orientation and mechanical fixing (for example, using rubber gaskets) of microphone and speaker parts in order to avoid echo interference between the uplink path and downlink path.
- Keep ground separation from microphone lines to other noisy signals. Use an intermediate ground layer or vias wall for coplanar signals.
- For an external audio device providing differential microphone input, route the microphone signal lines as a differential pair embedded in ground to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place bypass capacitor for RF very close to the active microphone. The preferred microphone should be designed for GSM applications which typically have an internal built-in bypass capacitor for RF very close to active device. If the integrated FET detects the RF burst, the resulting DC level will be in the pass-band of the audio circuitry and cannot be filtered by any other device.

General guidelines for the downlink path (speaker / receiver) are the following:

- The physical width of the audio output lines on the application board must be wide enough to minimize series resistance since the lines are connected to low impedance speaker transducers.
- Avoid coupling of any noisy signal to speaker lines: it is recommended to route speaker lines away from the module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Avoid coupling between speaker / receiver and microphone lines.
- Optimize the mechanical design of the application device, the position, orientation and mechanical fixing (for example, using rubber gaskets) of speaker and microphone parts in order to avoid echo interference between the downlink path and uplink path.
- For an external audio device providing differential speaker / receiver output, route the speaker signal lines as a differential pair embedded in ground up to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place the bypass capacitor for RF close to the speaker.

2.8 General Purpose Input/Output (GPIO)

2.8.1.1 Guidelines for GPIO circuit design

A typical usage of LARA-R6 series modules' GPIOs can be the following:

- Network indication provided over **GPIO1** pin (see Figure 59 / Table 40 below)
- GNSS supply enable function provided by the **GPIO2** pin (see section 2.6.3)
- GNSS Tx data ready function provided by the **GPIO3** pin (see section 2.6.3)
- SIM card detection provided over the **GPIO5** pin (see Figure 40 / Table 28 in section 2.5)

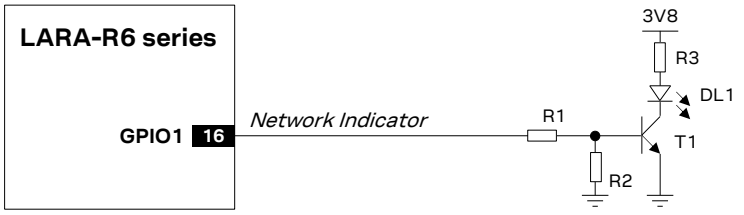

Figure 59: Application circuit for network indication provided over GPIO1

Reference	Description	Part number - manufacturer
R1	10 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	820 Ω Resistor 0402 5% 0.1 W	Various manufacturers
DL1	LED Red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT Transistor	BC847 - Infineon

Table 40: Components for network indication application circuit

☞ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of LARA-R6 series modules.

☞ Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply (**V_INT**), to avoid latch-up of circuits and allow a proper module boot.

☞ ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

☞ If the GPIO pins are not used, they can be left unconnected on the application board.

2.8.1.2 Guidelines for GPIO layout design

The general purpose input/output pins are generally not critical for layout.

2.9 Reserved pins (RSVD)

LARA-R6 series modules have pins reserved for future use, named **RSVD**: they can all be left unconnected on the application board, except

- the **RSVD** pin number **33**, that is highly recommended to be externally connected to an accessible Test-Point for diagnostic, as illustrated in Figure 60

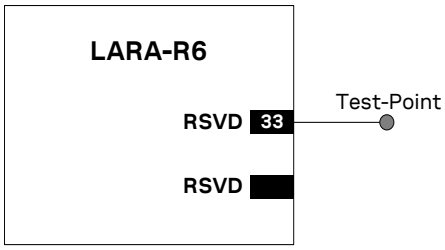

Figure 60: Application circuit for the reserved pins (RSVD)

2.10 Module placement

Optimize placement for a minimum length of RF line and a closer path from the DC source for **VCC**.

Make sure that the module, RF and analog parts / circuits are clearly separated from any possible source of radiated energy, including digital circuits that can radiate some digital frequency harmonics, which can produce Electro-Magnetic Interference affecting module, RF and analog parts / circuits' performance or implement proper countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Routing of noisy signals below the module, on the top layer of the application PCB, is not recommended.

Make sure that the module, RF and analog parts / circuits, high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by Electro-Magnetic Interference or employ countermeasures to avoid any possible Electro-Magnetic Compatibility issues.

Provide enough clearance between the module and any external part.

☞ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the LARA-R6 series modules: avoid placing temperature sensitive devices close to the module.

2.11 Module footprint and paste mask

Figure 61 and Table 41 describe the suggested footprint (i.e. copper mask) and paste mask layout for LARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder resist Mask Defined (NSMD) pad type is recommended over the Solder resist Mask Defined (SMD) pad type, implementing the solder mask opening 50 µm larger per side than the corresponding copper pad.

The recommended solder paste thickness is 150 µm, according to application production process requirements.

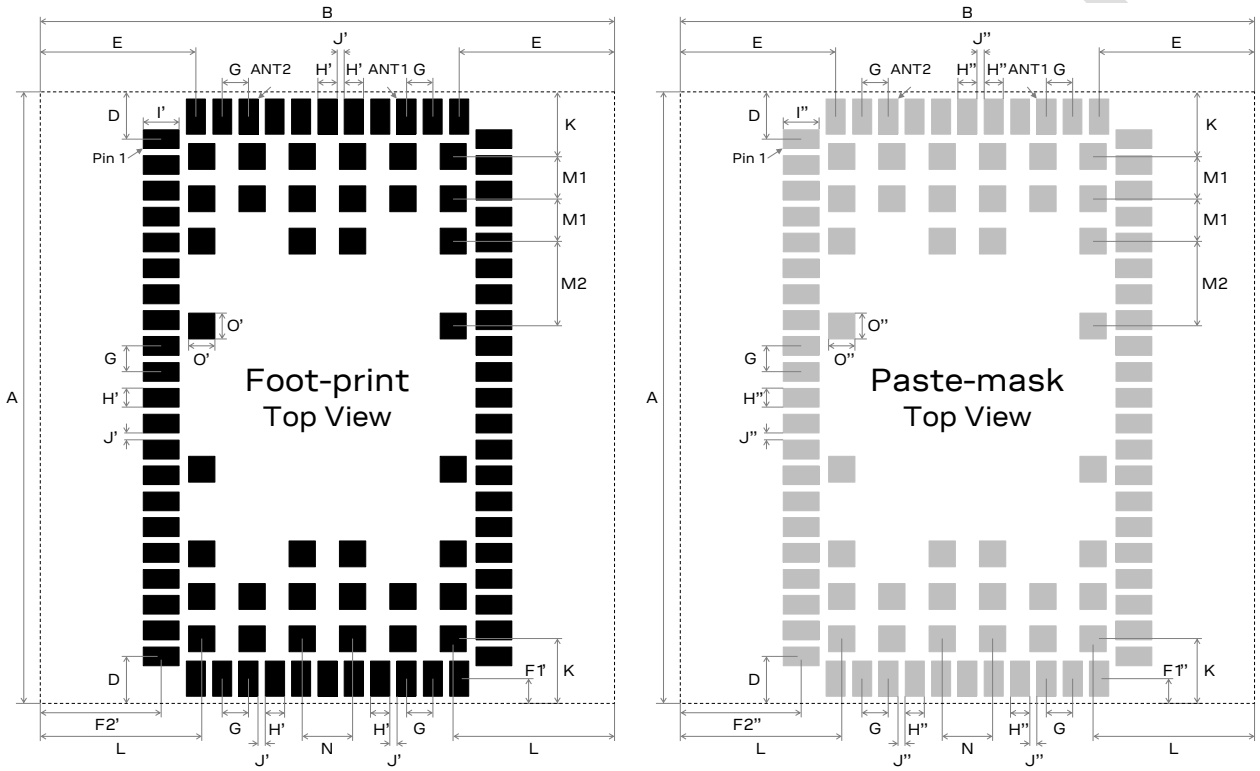

Figure 61: LARA-R6 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	F2''	5.00 mm	K	2.75 mm
B	24.0 mm	G	1.10 mm	L	6.75 mm
C	2.60 mm	H'	0.80 mm	M1	1.80 mm
D	2.00 mm	H''	0.75 mm	M2	3.60 mm
E	6.50 mm	I'	1.50 mm	N	2.10 mm
F1'	1.05 mm	I''	1.55 mm	O'	1.10 mm
F1''	1.00 mm	J'	0.30 mm	O''	1.05 mm
F2'	5.05 mm	J''	0.35 mm		

Table 41: LARA-R6 series modules suggested footprint and paste mask dimensions

☞ These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.12 Thermal guidelines

☞ Modules' operating temperature range is specified in the LARA-R6 series data sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload in connected mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks (for example, see the Terminal Tx Power distribution for WCDMA, taken from operation on a live network, described in the GSMA TS.09 Battery Life Measurement and Current Consumption Technique [15]); however the application should be correctly designed to cope with it.

During transmission at maximum RF power, the LARA-R6 series modules generate thermal power that may exceed 2 W: this is an indicative value since the exact generated power strictly depends on operating condition such as the actual antenna return loss, the number of allocated TX resource blocks, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition. The overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

☞ The Module-to-Ambient thermal resistance value and the relative increase of module temperature will differ according to the specific mechanical deployments of the module, e.g. application PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of the thermal dissipation, i.e. the reduction of the Module-to-Ambient thermal resistance, will decrease the temperature of the modules' internal circuitry for a given operating ambient temperature. This improves the device long-term reliability in particular for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with a complete thermal via stacked down to the main ground layer.
- Provide a ground plane as wide as possible on the application board.
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the device.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.

Further HW techniques that may be considered to improve the heat dissipation in the application:

- Force ventilation air-flow within the mechanical enclosure.
- Provide a heat sink component attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads of the LARA-R6 series LGA modules and dissipated over the backside of the application board.

For example, the Module-to-Ambient thermal resistance ($R_{th,M-A}$) is strongly reduced with forced air ventilation and a heat-sink installed on the back of the application board, decreasing the module temperature variation.

2.13 Schematic for LARA-R6 series module integration

Figure 62 is an example of a schematic diagram where a LARA-R6 series cellular module is integrated into an application board, using all the available interfaces and functions of the module.

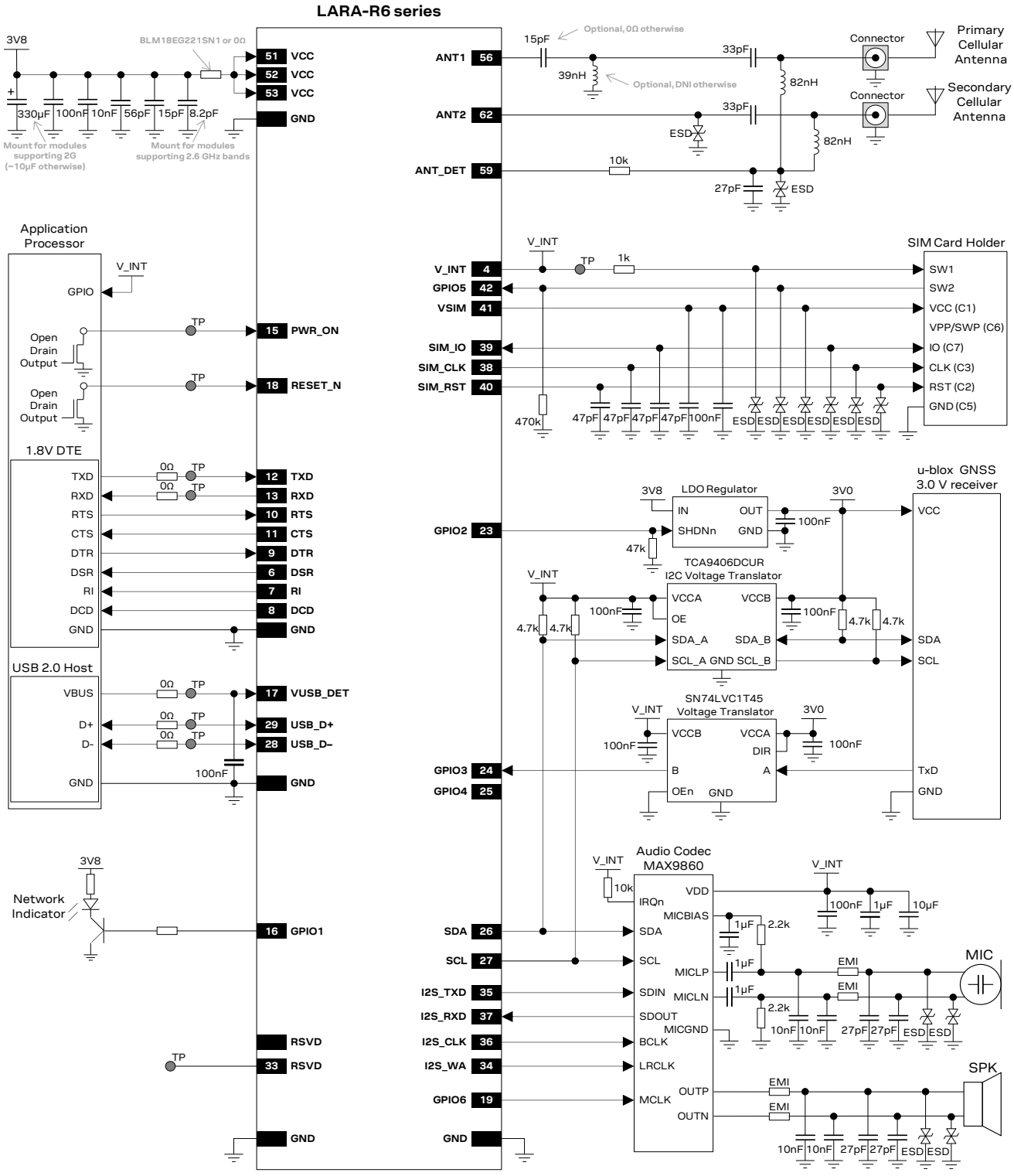

Figure 62: Example of schematic diagram to integrate a LARA-R6 series module using all interfaces

2.14 Design-in checklist

This section provides a design-in checklist.

2.14.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at the **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting both the highest peak and the highest averaged current consumption values in connected mode, as specified in the LARA-R6 series data sheet [1].
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Minimize series resistance along the **VCC** path.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that the voltage level of any connected pin does not exceed the relative operating range.
- ☑ Provide accessible test points directly connected to the following pins of the modules:
  - **V_INT**, **PWR_ON**, **RESET_N** and the **RSVD** pin number **33**, for diagnostic purpose,
  - **VUSB_DET**, **USB_D+** and **USB_D-**, for FW update and diagnostic purpose.
- ☑ Consider providing accessible test points on the UART **TXD** / **RXD** data lines and on the AUX UART **DTR** / **DCD** data lines, with a 0 Ω series jumper on each line, to detach the application processor for diagnostic purposes.
- ☑ Capacitance and series resistance must be limited on each line of the SIM interface to match the rise / fall time defined by SIM interface specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART interfaces signals direction, as the modules' signal names follow the ITU-T V.24 Recommendation [3].
- ☑ Capacitance and series resistance must be limited on each high speed line of the USB interface.
- ☑ Check the digital audio interface specifications to connect a proper external audio device.
- ☑ Capacitance and series resistance must be limited on clock output line and each I2S interface line.
- ☑ Consider passive filtering parts on each used analog audio line.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of LARA-R6 series modules before the switch-on of the generic digital interface supply source (**V_INT**).

2.14.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT1** and the **ANT2** ports (antenna RF interfaces).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (primarily the **VCC** line, analog audio input/output signals, SIM signals, high-speed digital lines such as USB, and other data lines).
- ☑ Optimize placement for minimum length of RF line.
- ☑ Check the footprint and paste mask designed for the module as illustrated in section 2.11.
- ☑ Route **VCC** supply line away from RF lines / parts and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picoFarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Ensure an optimal grounding connecting each **GND** pin with application board solid ground layer.

- ☑ Use as many vias as possible to connect the ground planes on a multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along the RF and high speed lines.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.
- ☑ Ensure appropriate RF precautions for the RF coexistence of GNSS and Cellular technologies.
- ☑ Route analog audio signals away from noisy sources (primarily RF interface, **VCC**, switching supplies).
- ☑ The audio outputs lines on the application board must be wide enough to minimize series resistance.

2.14.3 Antenna checklist

- ☑ Antenna termination should provide a 50 Ω characteristic impedance with VSWR at least less than 3:1 (recommended 2:1) on operating bands in the deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement, as for example reported in sections 4.2.2 and/or 4.3.1 for FCC US and/or ISED Canada.
- ☑ Ensure high and similar efficiency for both the primary (**ANT1**) and the secondary (**ANT2**) antenna.
- ☑ Ensure high isolation between the primary (**ANT1**) and the secondary (**ANT2**) antenna.
- ☑ Ensure a low Envelope Correlation Coefficient between the primary (**ANT1**) and the secondary (**ANT2**) antenna: the 3D antenna radiation patterns should have radiation lobes in different directions.
- ☑ Ensure high isolation between the cellular antennas and any other antenna or transmitter.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to LARA-R6 series reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the LARA-R6 series data sheet [1] and the u-blox package information user guide [23].

3.2 Handling

The LARA-R6 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ Ensure ESD precautions are implemented during handling of the module.

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of the LARA-R6 series modules (as Human Body Model according to JESD22-A114F) is specified in the LARA-R6 series data sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the LARA-R6 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect the ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron,...).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in a non-ESD protected work area, implement proper ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	+217 °C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The stencil geometry for applying soldering paste should meet the recommendations in section 2.11.

☞ The quality of the solder joints should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530A Guidelines for temperature profiling for mass soldering (reflow and wave) processes".

Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s
  If the temperature rise is too rapid in the preheat phase, it may cause excessive slumping.
- Time: 60 to 120 s
  If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 °C to 200 °C
  If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 to 60 s
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors, such as the choice of soldering paste, size, thickness and properties of the base board, etc.

Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

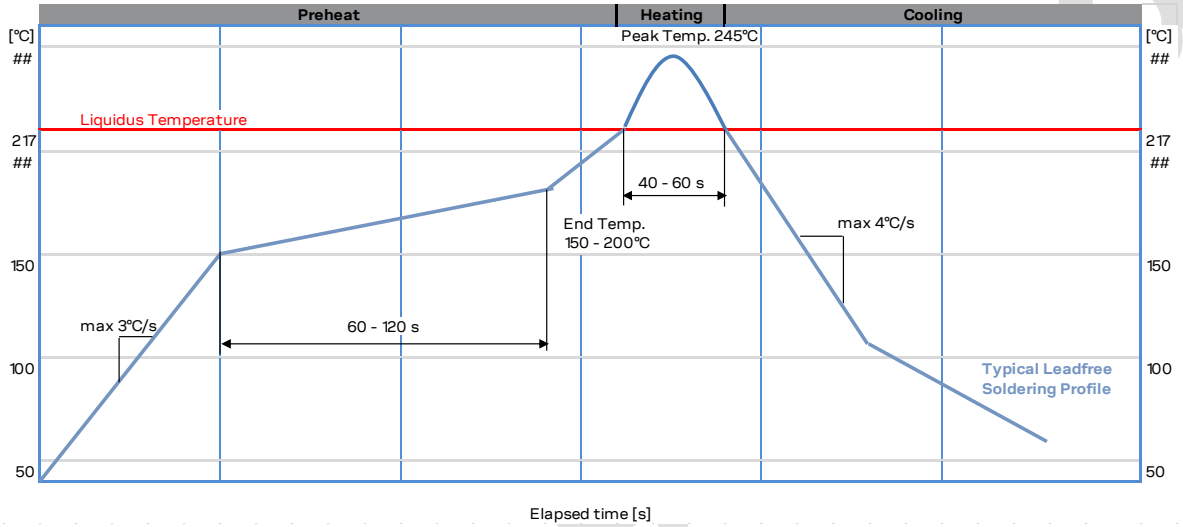

Figure 63: Recommended soldering profile

LARA-R6 series modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the module, inspect it optically to verify that it is properly aligned and centered.

3.3.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside-down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ u-blox gives no warranty against damages to the LARA-R6 series modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the LARA-R6 series module, plus one reflow soldering process to mount other parts).

3.3.6 Wave soldering

LARA-R6 series LGA modules must not be soldered with a wave soldering process.

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for a board with a LARA-R6 series module already populated on it.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ u-blox gives no warranty against damages to the LARA-R6 series modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the LARA-R6 series module, plus one plus one wave soldering process to mount other THT parts on the application board).

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products. These materials affect the RF properties of the LARA-R6 series modules and it is important to prevent them from flowing into the module. The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, and therefore care is required in applying the coating.

☞ Conformal coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the LARA-R6 series modules before implementing this in production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the LARA-R6 series modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

LARA-R6 series modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the LARA-R6 series modules caused by any ultrasonic processes.

4 Approvals

☞ For the complete list and specific details of the certification schemes approvals, see the LARA-R6 series data sheet [1], or please contact the u-blox office or sales representative nearest you.

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called “certification schemes” that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, as:
    - CE (European Conformity) marking for European Union
    - FCC (Federal Communications Commission) approval for United States
- Industry certification
  - Telecom industry specific approval verifying interoperability between devices and networks:
    - GCF (Global Certification Forum), a partnership between device manufacturers and network operators to ensure and verify global devices / networks interoperability
    - PTCRB (PCS Type Certification Review Board), created by US network operators to ensure and verify interoperability between devices and North America networks
- Operator certification
  - Operator specific approval required by some mobile network operators, such as:
    - AT&T network operator in the United States
    - Verizon Wireless network operator in the United States
    - T-Mobile network operator in the United States

Even if the LARA-R6 series modules are approved under all major certification schemes, the application device that integrates the modules must be approved under all the certification schemes required by the specific application device to be deployed in the market.

The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device that integrates LARA-R6 series modules must be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device must operate.

☞ Check the appropriate applicability of the module’s approvals while starting the certification process of the device integrating the module: the re-use of the u-blox cellular module’s approval can significantly reduce the cost and time to market of the application device certification.

☞ The certification of the application device that integrates a LARA-R6 series module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

LARA-R6 series modules are certified according to capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to the 3GPP TS 51.010-2 [10], 3GPP TS 34.121-2 [11], 3GPP TS 36.521-2 [13] and 3GPP TS 36.523-2 [14], is a statement of the implemented and supported capabilities and options of a device.

☞ The PICS document of the application device integrating a LARA-R6 module must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device. For more details regarding the AT commands settings that affect the PICS, see the u-blox AT commands manual [2].

☞ Check the specific settings required for mobile network operators approvals as they may differ from the AT commands settings defined in the module as integrated in the application device.

4.2 US Federal Communications Commission notice

FCC IDs of LARA-R6 series modules:

- u-blox LARA-R6001 cellular modules: XPYUBX21BE01
- u-blox LARA-R6401 cellular modules: XPYUBX21BE02

4.2.1 Safety warnings review the structure

- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed

4.2.2 Declaration of conformity

This device complies with Part 15 of the FCC rules and with the ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

⚠ Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC procedures and as authorized in the module certification filing.

⚠ The gain of the system antenna(s) used for the LARA-R6 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value specified in the FCC Grant for mobile and fixed or mobile operating configurations

4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating the LARA-R6 series modules are authorized to use the FCC Grants of the LARA-R6 series modules for their own final products according to the conditions referenced in the certificates.

⚠ The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains FCC ID: XPYUBX21BE01" resp.
"Contains FCC ID: XPYUBX21BE02" resp.

⚠ IMPORTANT: Manufacturers of portable applications incorporating the LARA-R6 series modules are required to have their final product certified and apply for their own FCC Grant related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

⚠ Additional Note: as per 47CFR15.105 this equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consultant the dealer or an experienced radio/TV technician for help

4.3 Innovation, Science, Economic Development Canada notice

ISED Certification Numbers of LARA-R6 series modules:

- u-blox LARA-R6001 cellular modules: 8595A-UBX21BE01
- u-blox LARA-R6401 cellular modules: 8595A-UBX21BE02

4.3.1 Declaration of Conformity

This device complies with the ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

⚠ Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for the LARA-R6 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed not exceed the values specified in the ISED Canada Certificate Grant for mobile and fixed or mobile operating configurations.

4.3.2 Modifications

The ISED Canada requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating the LARA-R6 series modules are authorized to use the ISED Canada Certificates of the LARA-R6 series modules for their own final products according to the conditions referenced in the certificates.

The ISED Canada Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains IC: 8595A-UBX21BE01" resp.
"Contains IC: 8595A-UBX21BE02" resp.

Innovation, Science and Economic Development Canada (ISED) Notices

This Class B digital apparatus complies with Canadian CAN ICES-3(B) / NMB-3(B) and RSS-210. Operation is subject to the following two conditions:

- this device may not cause interference
- this device must accept any interference, including interference that may cause undesired operation of the device

Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Cellular Module is below the Innovation, Science and Economic Development Canada (ISED) radio frequency exposure limits. The u-blox Cellular Module should be used in such a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the ISED RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).

This device has been certified for use in Canada. Status of the listing in the Innovation, Science and Economic Development's REL (Radio Equipment List) can be found at the following web address: http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng

Additional Canadian information on RF exposure also can be found at the following web address: http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

IMPORTANT: Manufacturers of portable applications incorporating the LARA-R6 series modules are required to have their final product certified and apply for their own Innovation, Science and Economic Development Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Avis d'Innovation, Sciences et Développement économique Canada (ISDE)

Cet appareil numérique de classe B est conforme aux normes canadiennes CAN ICES-3(B) / NMB-3(B) et CNR-210. Son fonctionnement est soumis aux deux conditions suivantes :

- cet appareil ne doit pas causer d'interférence
- cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans fil u-blox Cellular Module est inférieure à la limite d'exposition aux fréquences radio d'Innovation, Sciences et Développement économique Canada (ISDE). Utilisez l'appareil de sans fil u-blox Cellular Module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur: http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur: http://www.ic.gc.ca/eic/site/smt-gst.nsf/fra/sf08792.html

⚠ IMPORTANT: les fabricants d'applications portables contenant les modules LARA-R6 series doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat ISDE Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

4.4 European Conformance CE mark

LARA-R6001 and LARA-R6801 modules have been evaluated against the essential requirements of the Radio Equipment Directive 2014/53/EU.

In order to satisfy the essential requirements of the 2014/53/EU RED, the modules are compliant with the following standards:

- Radio Spectrum Efficiency (Article 3.2):
  - EN 301 511
  - EN 301 908-1
  - EN 301 908-2
  - EN 301 908-13
- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1
  - EN 301 489-52
- Health and Safety (Article 3.1a)
  - EN 62368-1
  - EN 62311

⚠ Radiofrequency radiation exposure information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for the LARA-R6 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the values reported in the Declaration of Conformity for mobile and fixed or mobile operating configurations.

The conformity assessment procedure for the modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU, has been followed.

Thus, the following marking is included in the product:

CE

5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically in the production line. A stringent quality control process has been implemented in the production line. Defective units are analyzed in detail to improve production quality.

This is achieved with automatic test equipment (ATE) in the production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. Figure 64 illustrates the typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests.

- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of the reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of RF characteristics after calibration (i.e. modulation accuracy, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

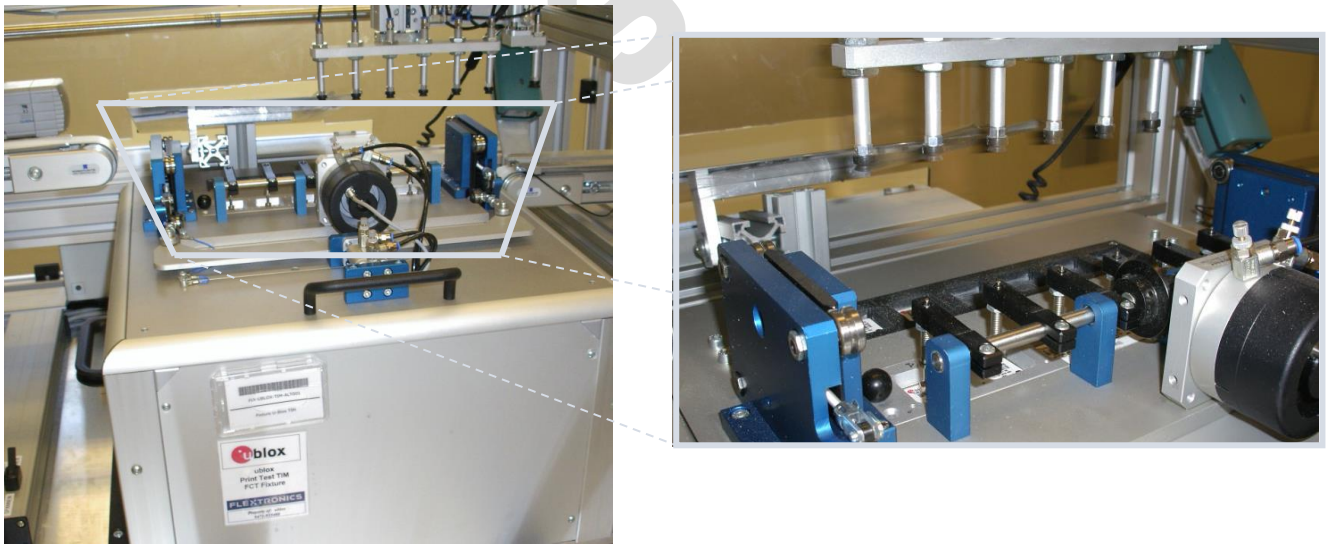

Figure 64: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturers

Because of the testing performed by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

An OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling processes did not damage the module components
  - All module pins are well soldered on the device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communications with host controller can be established
  - The interfaces between the module and device are working
  - Overall RF functional test of the device including the antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

In addition, module AT commands can be used to perform functional tests on digital interfaces (communication with host controller, check SIM interface, GPIOs, etc.), on audio interfaces (audio loop for test purposes can be enabled by the AT+UPAR=2 command as described in the u-blox AT commands manual [2]), and to perform RF functional tests (see following section 5.2.2 for details).

5.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test is typically performed to compare the signal quality with a "Golden Device" in a location with excellent network coverage and known signal quality. This test should be performed after data connection has been established. AT+CSQ is the typical AT command used to check signal quality in term of RSSI (for more details, see the u-blox AT commands manual [2]).

☞ These kinds of test may be useful as a "go / no go" test, not for RF performance measurements.

This test is suitable to check the functionality of communication with the host controller or SIM card, as well as the power supply. It is also a means to verify if the components at antenna interface are well soldered.

5.2.2 Functional tests providing RF operation

As mentioned before, OEM manufacturers need only to verify proper assembly of the module in the OEM production line, i.e. proper soldering joint of the **ANT1** and **ANT2** pads and related parts along the RF path, and this can be done by performing a simple RF functional test with basic instruments such as a spectrum analyzer (or an RF power meter), and optionally a signal generator, with the assistance of the +UTEST AT command over the AT command user interface.

The +UTEST AT command provides a simple interface to set the module to Rx or Tx test modes ignoring the cellular signaling protocol. The command can set the module into:

- transmitting mode in a specified channel and power level in all supported bands
- receiving mode in a specified channel to returns the measured power level in all supported bands

The minimum recommended RF verification in production consists in forcing the module to transmit in a supported frequency the +UTEST AT command, and then checking that some power is emitted from the antenna system using any suitable power detector, power meter or equivalent equipment, as well as checking if the module receives some power form a suitable signal generator while forced to receive in a supported frequency the +UTEST AT command.

☞ See the u-blox AT commands manual [2], for the +UTEST AT command syntax description and examples of use.

This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces on which RF performance depends.

⚠ To avoid module damage during transmitter test, a proper antenna according to module specifications or a 50 Ω termination must be connected to the **ANT1** port.

⚠ To avoid module damage during receiver, test the maximum power level received at the **ANT1** and **ANT2** ports which must meet the module specifications.

☞ The +UTEST AT command sets the module to emit RF power ignoring cellular signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purposes in controlled environments by qualified users and must not be used during normal module operation. Follow the instructions suggested in u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Figure 65 illustrates a typical test setup for such an RF functional test.

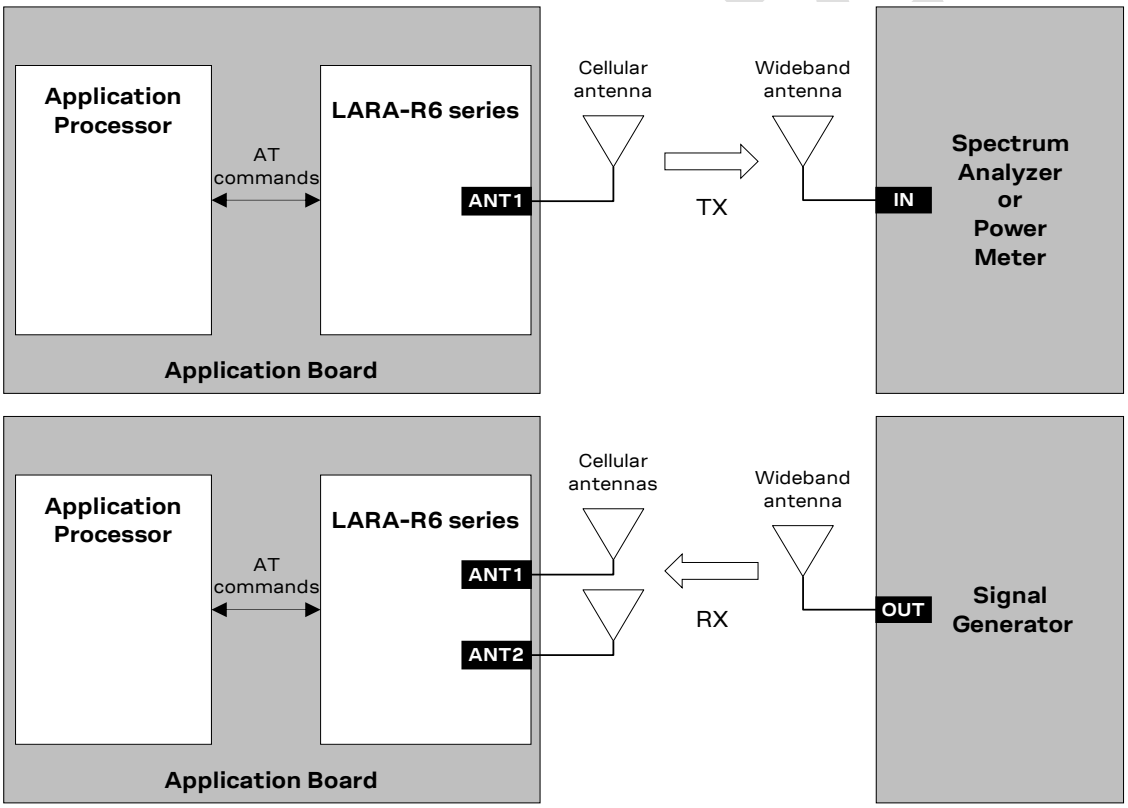

Figure 65: Setup with spectrum analyzer or power meter and signal generator for radiated measurements

Appendix

A Migration from LARA-R2 to LARA-R6 modules

☞ Detailed and updated guidelines to migrate from u-blox LARA-R2 modules to u-blox LARA-R6 modules are available in the LARA-R2 / LARA-R6 series modules migration guidelines application note [24].

B Glossary

Abbreviation	Definition
2G	2nd Generation Cellular Technology (GSM, GPRS, EGPRS)
3G	3rd Generation Cellular Technology (UMTS, HSDPA, HSUPA)
3GPP	3rd Generation Partnership Project
8-PSK	8 Phase-Shift Keying modulation
16QAM	16-state Quadrature Amplitude Modulation
ACM	Abstract Control Model
ADC	Analog to Digital Converter
AP	Application Processor
APAC	Asia-Pacific
APN	Access Point Name
ASIC	Application-Specific Integrated Circuit
AT	AT Command Interpreter Software Subsystem
ATE	Automatic Test Equipment
AUX	Auxiliary
BAW	Bulk Acoustic Wave
BIP	Bearer Independent Protocol
BJT	Bipolar Junction Transistor
Cat	Category
CDC	Communication Device Class
CDMA	Code-Division Multiple Access
CE	Certification Mark for EHS compliance in the European Economic Area
CENELEC	Comité Européen de Normalisation Électrotechnique
CSFB	Circuit Switched Fall-Back
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTLS	Datagram Transport Layer Security

Abbreviation	Definition
DTR	Data Terminal Ready
ECC	Envelope Correlation Coefficient
EDGE	Enhanced Data rates for GSM Evolution (EGPRS)
eDRX	Extended Discontinuous Reception
EGPRS	Enhanced General Packet Radio Service (EDGE)
EMC	Electro-magnetic Compatibility
EMEA	Europe, the Middle East and Africa
EMI	Electro-magnetic Interference
EPA	Electrostatic Protective Area
ESD	Electro-static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
FCC	Federal Communications Commission
FDD	Frequency Division Duplex
FEM	Front End Module
FOAT	(Update via) Firmware Over AT commands
FOTA	Firmware Over The Air
FTP	File Transfer Protocol
FW	Firmware
GERA	GSM EGPRS Radio Access
GMSK	Gaussian Minimum Shift Keying modulation
GLONASS	(Russian) GLObal Navigation Satellite System
GMSK	Gaussian Minimum-Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Services
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HBM	Human Body Model
HSIC	High Speed Inter Chip
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	HyperText Transfer Protocol
HW	Hardware
I/Q	In-phase and Quadrature
I2C	Inter-Integrated Circuit interface
I2S	Inter IC Sound interface
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronics Engineers
IMEI	International Mobile Equipment Identity
IP	Internet Protocol
ISO	International Organization for Standardization
ITU	International Telecommunications Union
LATAM	Latin America
LCC	Leadless Chip Carrier

Abbreviation	Definition
LDO	Low-Dropout
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPDDR	Low Power Double Data Rate synchronous dynamic RAM memory
LPWA	Low Power Wide Area
LTE	Long Term Evolution
LwM2M	Open Mobile Alliance Lightweight Machine-to-Machine protocol
M2M	Machine to machine
MCS	Modulation Coding Scheme
MIMO	Multiple In Multiple Out
MQTT	Message Queuing Telemetry Transport
MSD	Moisture Sensitive Device
N/A	Not Applicable
NCM	Network Control Model
NSMD	Non Solder Mask Defined
NTC	Negative Temperature Coefficient
OEM	Original Equipment Manufacturer device: an application device integrating a u-blox cellular module
OTA	Over The Air
PA	Power Amplifier
PCM	Pulse Code Modulation
PCN	Product Change Notification
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PTCRB	PCS Type Certification Review Board
PWM	Pulse Width Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RSE	Radiated Spurious Emission
RTC	Real Time Clock
Rx	Receive
SAR	Specific Absorption Rate
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input Output
SIM	Subscriber Identification Module
SMD	Solder Mask Defined
SMS	Short Message Service
SMT	Surface-Mount Technology
SMTP	Simple Mail Transfer Protocol
SRF	Self Resonant Frequency
SSL	Secure Sockets Layer
STS	Smart Temperature Supervisor
TBD	To Be Defined
TCP	Transmission Control Protocol
TDD	Time Division Duplex
TDMA	Time Division Multiple Access

Abbreviation	Definition
THT	Through-Hole Technology
TI	Texas Instruments
TIS	Total Isotropic Sensitivity
TLS	Transport Layer Security
TP	Test-Point
TRP	Total Radiated Power
TTFF	Time-To-First-Fix
Tx	Transmit
UART	Universal Asynchronous Receiver-Transmitter
uCSP	u-blox Common Services Platform
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
uFOTA	u-blox Firmware update Over The Air
UL	Up-Link (Transmission)
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
UTRA	UMTS Terrestrial Radio Access
VCC	Voltage Collector Collector
VCO	Voltage Controlled Oscillator
VoLTE	Voice over LTE
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code-Division Multiple Access
Wi-Fi	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WLAN	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WWAN	Wireless Wide Area Network (GSM / UMTS / LTE cellular radio technology)

Table 42: Explanation of the abbreviations and terms used

Related documentation

[1] u-blox LARA-R6 series data sheet, UBX-21004391
[2] u-blox AT commands manual, UBX-13002752
[3] ITU-T recommendation V.24 - List of definitions for interchange circuits between the Data Terminal Equipment (DTE) and the Data Circuit-terminating Equipment (DCE), https://www.itu.int/rec/T-REC-V.24-200002-I/en
[4] 3GPP TS 27.007 – AT command set for User Equipment (UE)
[5] 3GPP TS 27.005 – Use of Data Terminal Equipment - Data Circuit-terminating Equipment (DTE-DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[6] 3GPP TS 27.010 – Terminal Equipment to User Equipment (TE-UE) multiplexer protocol
[7] Universal Serial Bus Revision 2.0 specification, https://www.usb.org/
[8] High-Speed Inter-Chip USB Specification, V.1.0, https://www.usb.org/
[9] I2C-bus specification and user manual - NXP Semiconductors, https://www.nxp.com/docs/en/user-guide/UM10204.pdf
[10] 3GPP TS 51.010-2 – Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS)
[11] 3GPP TS 34.121-2 - Technical Specification Group Radio Access Network; User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 2: Implementation Conformance Statement (ICS)
[12] 3GPP TS 36.521-1 - Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing
[13] 3GPP TS 36.521-2 - Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)
[14] 3GPP TS 36.523-2 - Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)
[15] GSM Association TS.09 - Battery Life Measurement and Current Consumption Technique https://www.gsma.com/newsroom/wp-content/uploads//TS.09-v11.0.pdf
[16] CENELEC EN 61000-4-2 – Electromagnetic compatibility (EMC); Part 4-2: Testing and measurement techniques; Electrostatic discharge immunity test
[17] ETSI EN 301 489-1 – Electromagnetic compatibility and Radio spectrum Matters; EMC standard for radio equipment and services; Part 1: Common technical requirements
[18] ETSI EN 301 489-52 – Electromagnetic Compatibility (EMC) standard for radio equipment and services; Part 52: Specific conditions for Cellular Communication Mobile and portable (UE) radio and ancillary equipment
[19] u-blox multiplexer implementation application note, UBX-13001887
[20] u-blox GNSS implementation application note, UBX-13001849
[21] u-blox firmware update application note, UBX-13001845
[22] u-blox end user test application note, UBX-13001922
[23] u-blox package information user guide, UBX-14001652
[24] u-blox LARA-R2 and LARA-R6 series migration guidelines application note, UBX-21010015

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	20-May-2021	sses	Initial release

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