2.6 Data communication interfaces

2.6.1 UART interfaces

2.6.1.1 Guidelines for UART circuit design

Providing 1 UART with the full RS-232 functionality (using the complete V.24 link)

☞ Compatible with USIO variant 1; not compatible with USIO variants 0 / 2 / 3 / 4 (see section 1.9.1.1).

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V application processor (DTE) is used and complete RS-232 functionality is required, then the complete 1.8 V UART of the module (DCE) should be connected to a 1.8 V DTE, as in Figure 49.

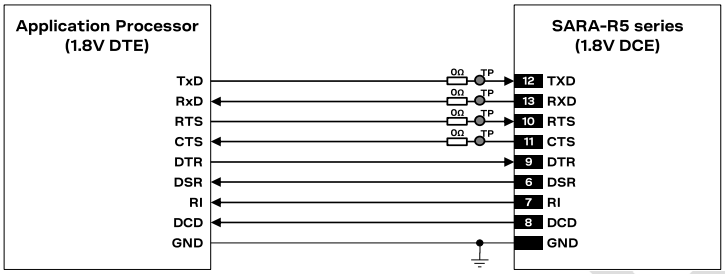

Figure 49: 1 UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART of the module (DCE) by means of appropriate unidirectional voltage translators using the module V_INT output as 1.8 V supply for the voltage translators on the module side, as described in Figure 50.

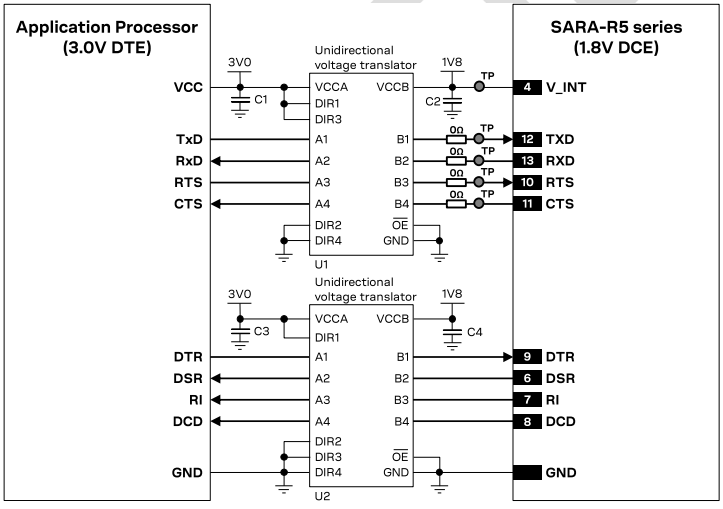

Figure 50: 1 UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [7] - Texas Instruments

Table 29: Components for 1 UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

[7] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD, RXD, RTS, CTS, DTR and RI lines only

☞ Compatible with USIO variants 0/1; not compatible with USIO variants 2/3/4 (see section 1.9.1.1).

If the functionality of the **DSR** and **DCD** lines is not required, or the lines are not available:

- Leave **DSR** and **DCD** lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

Figure 51 describes the circuit that should be implemented if a 1.8 V application processor (DTE) is used, given that the DTE will behave correctly regardless of the **DSR** input setting.

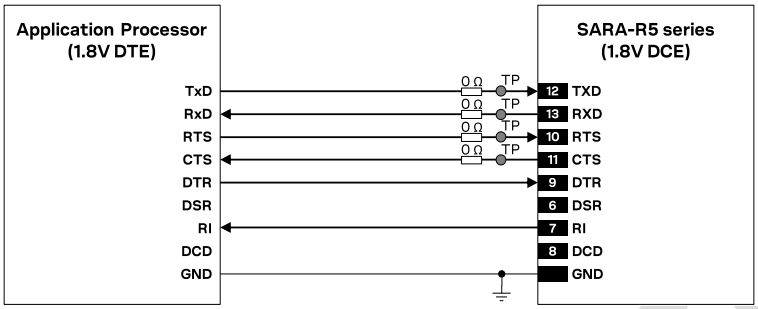

Figure 51: 1 UART interface application circuit with 7-wire link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module V_INT output as 1.8 V supply for the voltage translators on the module side, as described in Figure 52, given that the DTE will behave correctly regardless of the **DSR** input setting.

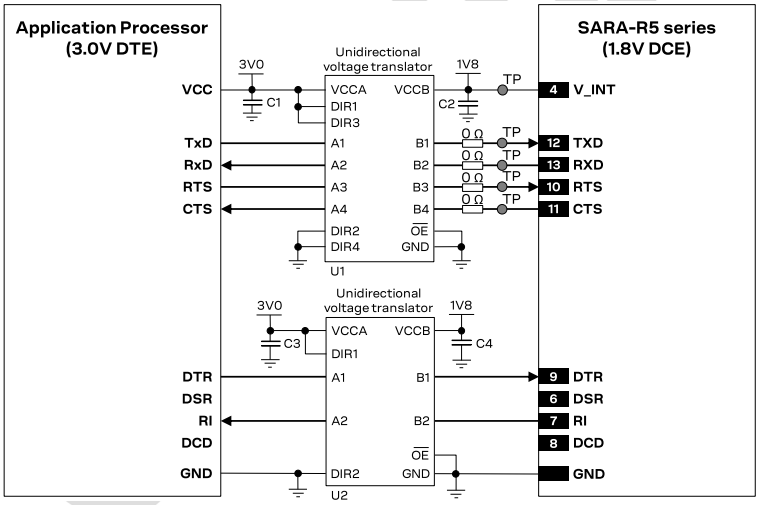

Figure 52: 1 UART interface application circuit with 7-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [8] - Texas Instruments
U2	Unidirectional voltage translator	SN74AVC2T245 [8] - Texas Instruments

Table 30: Components for 1 UART application circuit with 7-wire link in DTE/DCE serial communication (3.0 V DTE)

[8] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD, RXD, RTS and CTS lines only

☞ Compatible with USIO variants 0/1/3; not compatible with USIO variants 2/4 (see section 1.9.1.1).

If the functionality of the **DSR**, **DCD**, **RI** and **DTR** lines is not required, or the lines are not available:

- Leave **DSR**, **DCD**, **RI** and **DTR** lines of the module floating; it is recommended to provide a test point on these lines

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 53.

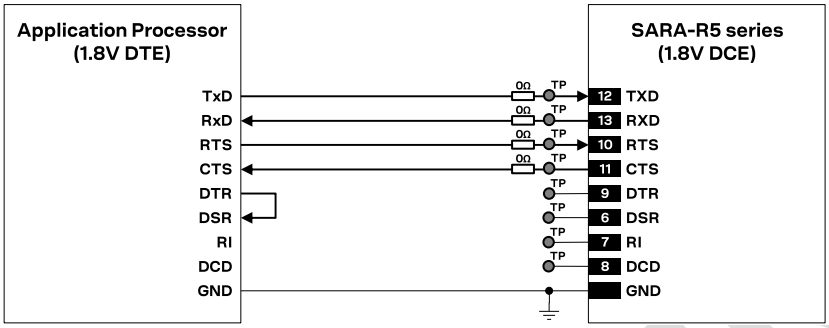

Figure 53: 1 UART interface application circuit with 5-wire link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 54.

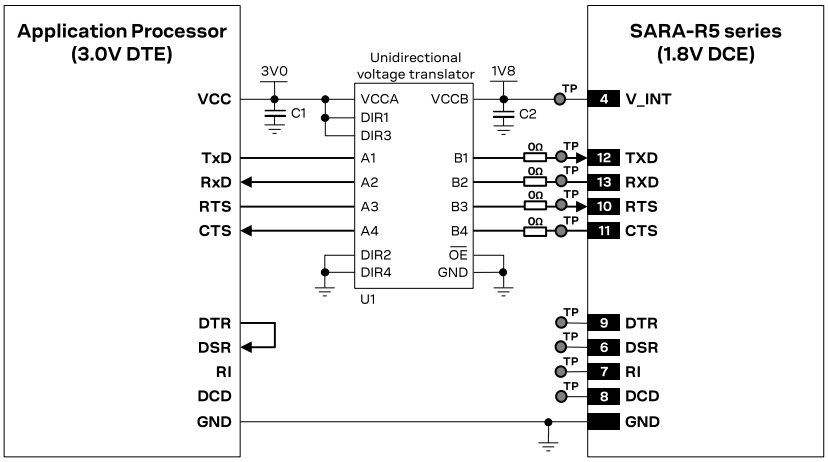

Figure 54: 1 UART interface application circuit with 5-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [9] - Texas Instruments

Table 31: Components for 1 UART application circuit with 5-wire link in DTE/DCE serial communication (3.0 V DTE)

[9] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with the TXD, RXD, RTS and CTS lines only

☞ Compatible with USIO variants 2/3/4; not compatible with USIO variants 0/1 (see section 1.9.1.1).

If RS-232 compatible signal levels are needed, two Maxim MAX13234E voltage level translators can be used. These chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 55.

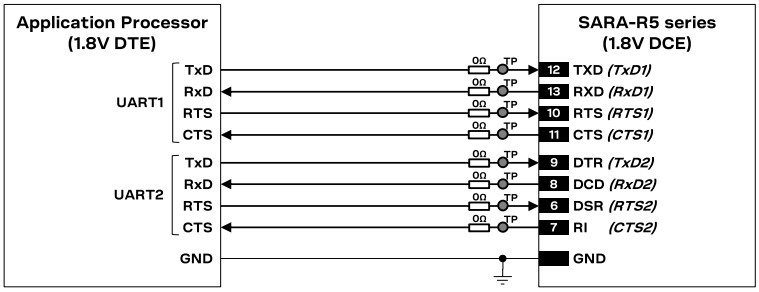

Figure 55: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (1.8V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 56.

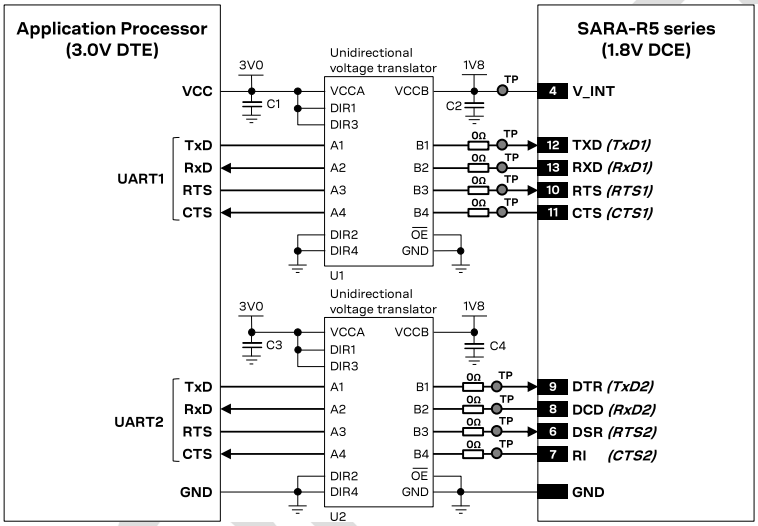

Figure 56: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [10] - Texas Instruments

Table 32: Components for 2 UARTs application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

[10] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD and RXD lines only

☞ Compatible with USIO variants 0/1/3; not compatible with USIO variants 2/4 (see section 1.9.1.1).

If the functionality of the **RTS**, **CTS**, **DTR**, **DSR**, **RI** and **DCD** lines is not required in the application, or the lines are not available, then:

- Connect the module **RTS** input line to GND or to the **CTS** output of the module, since the module requires **RTS** active (low electrical level) if HW flow control is enabled (as it is by default)
- Leave **DTR**, **DSR**, **RI** and **DCD** lines of the module floating; it is recommended to provide a test point on these lines

If RS-232 compatible signal levels are needed, the Maxim MAX13236E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor (DTE) is used, the circuit should be implemented as in Figure 57.

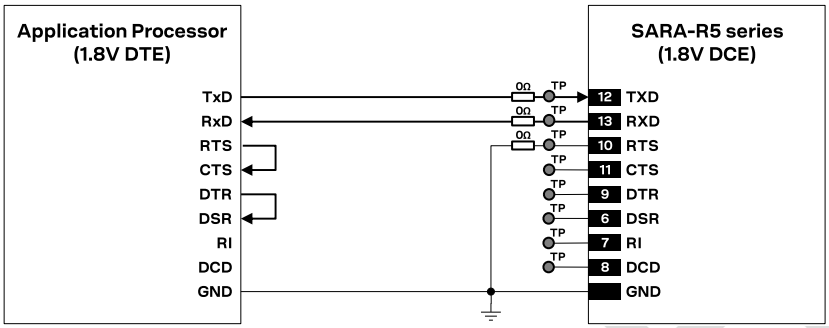

Figure 57: 1 UART interface application circuit with 3-wire link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 58.

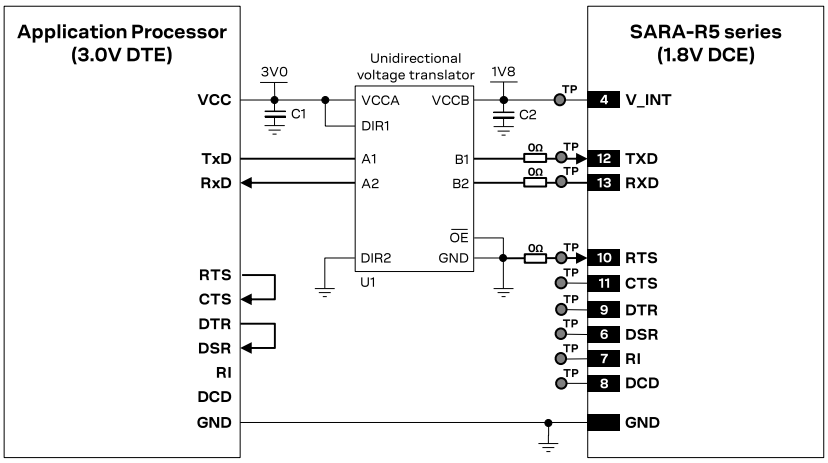

Figure 58: 1 UART interface application circuit with 3-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
U1	Unidirectional voltage translator	SN74AVC2T245 [11] - Texas Instruments

Table 33: Components for 1 UART application circuit with 3-wire link in DTE/DCE serial communication (3.0 V DTE)

[11] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with the TXD and RXD lines only

☞ Compatible with USIO variants 2/3/4; not compatible with USIO variants 0/1 (see section 1.9.1.1).

If the functionality of the **RTS**, **CTS**, **DSR** and **RI** lines is not required in the application, or the lines are not available, then:

- Connect the module **RTS** and **DSR** input lines to GND or respectively to the **CTS** and **RI** output of the module, since the module requires **RTS** and **DSR** active (low electrical level) if HW flow control is enabled (as it is by default)

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor (DTE) is used, the circuit should be implemented as in Figure 59.

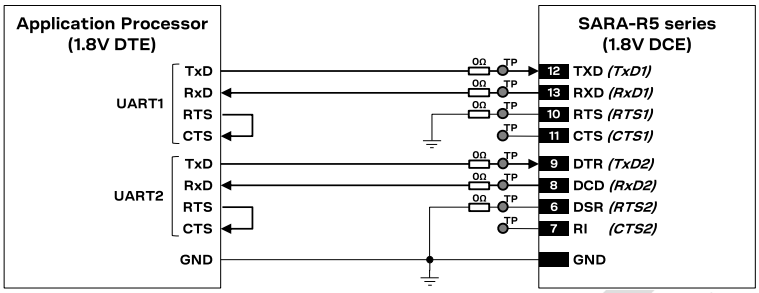

Figure 59: 2 UART interfaces application circuit with 3-wire links in DTE/DCE serial communications (1.8V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by means of an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 58.

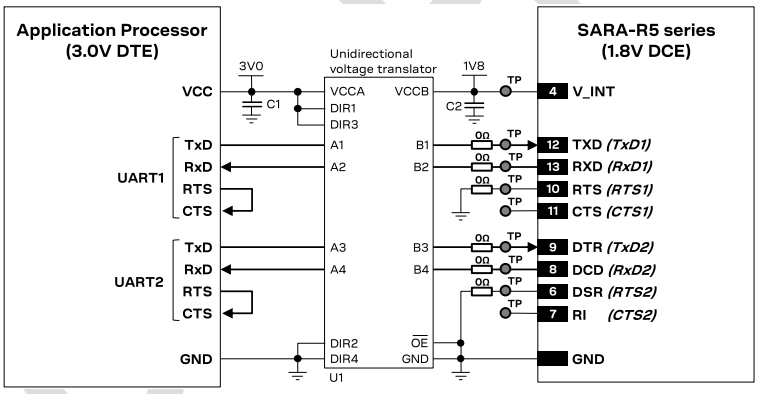

Figure 60: 2 UART interfaces application circuit with 3-wire links in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number - Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 - Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [12] - Texas Instruments

Table 34: Components for 2 UARTs application circuit with 3-wire links in DTE/DCE serial communications (3.0 V DTE)

[12] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Additional considerations

If a 3.0 V application processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-down / pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values. Make sure that any DTE signal connected to the module is tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a clean boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the corresponding 3.0 V input of the application processor (DTE) can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

- Do not apply voltage to any UART interface pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi-channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.
- ESD sensitivity rating of the UART interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection levels could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible points.

2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 USB interface

The USB interface is available for diagnostic purpose only.

2.6.2.1 Guidelines for USB circuit design

A suitable application circuit can be similar to the one illustrated in Figure 61, where direct external access is provided for diagnostic purpose by means of testpoints made available on the application board for **VUSB_DET**, **USB_D+** and **USB_D-** lines.

USB pull-up or pull-down resistors and external series resistors on **USB_D+** and **USB_D-** lines as required by the USB 2.0 specification [4] are part of the module USB pins driver and do not need to be externally provided.

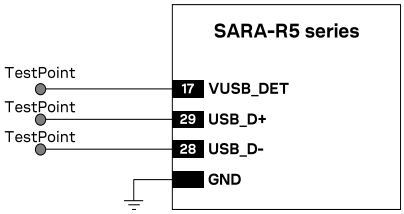

Figure 61: SARA-R5 series modules USB application circuit providing access for diagnostic purpose

The USB interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) on the lines connected to these pins, close to accessible points.

It is recommended to provide accessible test points directly connected to the USB interface pins (**VUSB_DET**, **USB_D+**, **USB_D-**).

2.6.2.2 Guidelines for USB layout design

The characteristic impedance of the **USB_D+** / **USB_D-** lines is specified by the USB 2.0 specification [4]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if PCB layout is not optimal, especially when the USB signaling lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route **USB_D+** / **USB_D-** lines as a differential pair
- Route **USB_D+** / **USB_D-** lines as short as possible
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω
- Consider design rules for **USB_D+** / **USB_D-** similar to RF transmission lines, whether coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area

Figure 62 and Figure 63 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

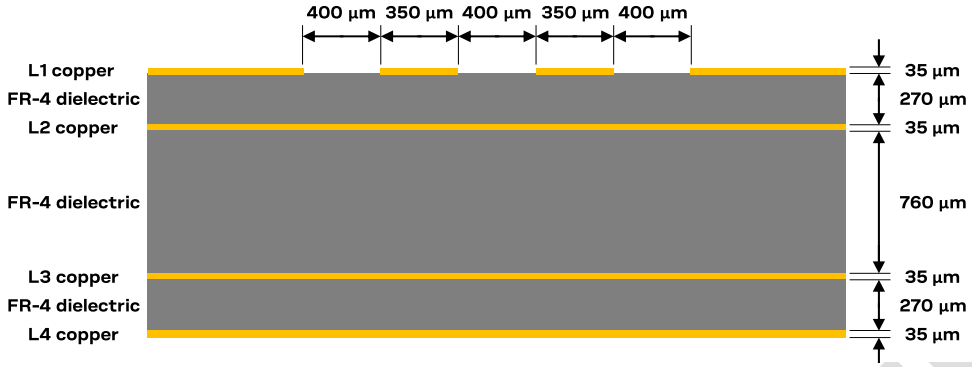

Figure 62: Example of USB line design, with Z0 close to 90 Ω and ZCM close to 30 Ω, for the described 4-layer board layup

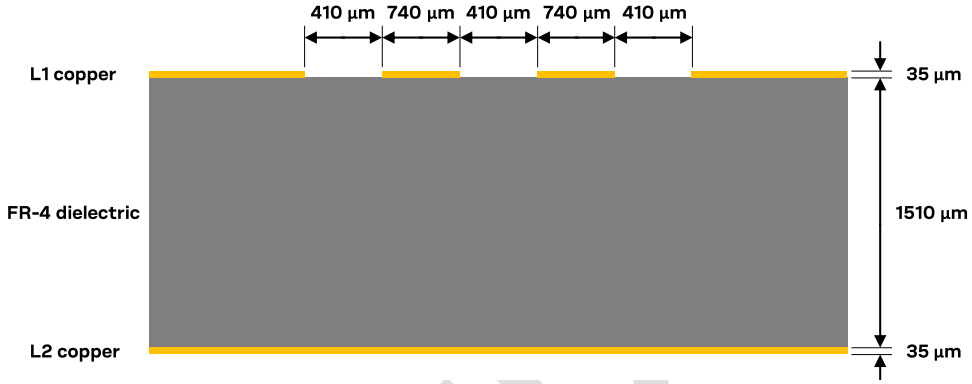

Figure 63: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 2-layer board layup

2.6.3 SPI interfaces

- The SPI interfaces are not supported by the “00” product version of SARA-R5 series modules, except for diagnostic purpose.
- It is recommended to provide accessible test points directly connected to the **SDIO_D0**, **SDIO_D1**, **SDIO_D2** and **SDIO_D3** pins for diagnostic purpose.

2.6.4 SDIO interface

- The SDIO interface is not supported by the “00” product version of SARA-R5 series modules.
- It is recommended to provide accessible test points directly connected to the **SDIO_D0**, **SDIO_D1**, **SDIO_D2** and **SDIO_D3** pins for diagnostic purpose.

2.6.5 DDC (I2C) interface

2.6.5.1 Guidelines for DDC (I2C) circuit design

Communication with an external GNSS receiver is not supported by SARA-R510M8S modules.

The DDC I2C-bus master interface can be used to communicate with u-blox GNSS receivers and other external I2C-bus slaves as an audio codec.

The **SDA** and **SCL** pins of the module are open drain output as per I2C bus specifications [9], and they have internal pull-up resistors to the **V_INT** 1.8 V supply rail of the module, so there is no need of additional pull-up resistors on the external application board.

Capacitance and series resistance must be limited on the bus to match the I2C specifications (1.0 µs is the max allowed rise time on **SCL** and **SDA** lines): route connections as short as possible.

ESD sensitivity rating of the DDC (I2C) pins is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

If the pins are not used as DDC bus interface, they can be left unconnected.

Connection with u-blox 1.8 V GNSS receivers

Figure 64 shows a circuit example for connecting the cellular module to a u-blox 1.8 V GNSS receiver:

- The **SDA** and **SCL** pins of the cellular module are directly connected to the related pins of the u-blox 1.8 V GNSS receiver. External pull-up resistors are not needed, as they are already integrated in the cellular module.
- The **GPIO2** pin is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 1.8 V GNSS receiver providing the “GNSS supply enable” function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the cellular module is switched off or in the reset state.
- The **GPIO3** and **GPIO4** pins are directly connected respectively to **TXD1** and **EXTINT0** pins of the u-blox 1.8 V GNSS receiver providing “GNSS data ready” and “GNSS RTC sharing” functions.

For additional guidelines regarding the design of applications with u-blox 1.8 V GNSS receivers, see the hardware integration manuals of the u-blox GNSS receivers.

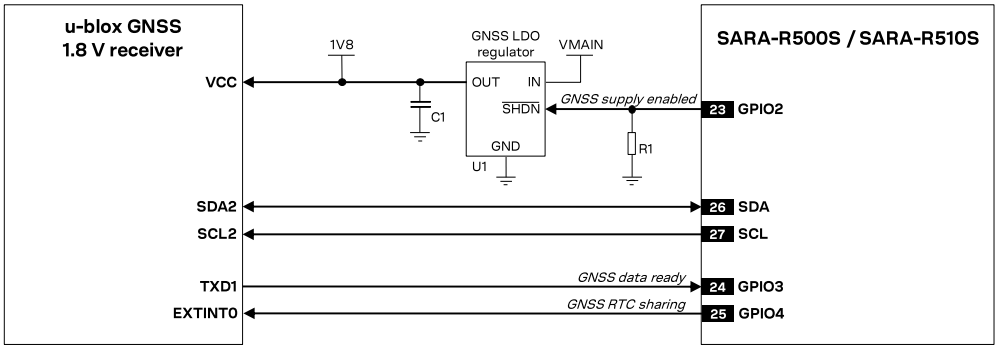

Figure 64: Application circuit for connecting SARA-R500S/SARA-R510S modules to a u-blox 1.8 V GNSS receiver

Reference	Description	Part number - Manufacturer
R1	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
U1, C1	Voltage regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver hardware integration manual

Table 35: Components for connecting SARA-R500S/SARA-R510S modules to a u-blox 1.8 V GNSS receiver

Connection with u-blox 3.0 V GNSS receivers

☞ Communication with an external GNSS receiver is not supported by SARA-R510M8S modules.

Figure 65 shows an application circuit for connecting the cellular module to a u-blox 3.0 V GNSS receiver:

- As the **SDA** and **SCL** pins of the cellular module are not tolerant up to 3.0 V, the connection to the related I2C pins of the u-blox 3.0 V GNSS receiver must be provided using a suitable I2C-bus bidirectional voltage translator (e.g. TI TCA9406, which additionally provides the partial power down feature so that the GNSS 3.0 V supply can be ramped up before the **V_INT** 1.8 V cellular supply). External pull-up resistors are not needed on the cellular module side, as they are already integrated in the cellular module.
- The **GPIO2** is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 3.0 V GNSS receiver providing the "GNSS supply enable" function. A pull-down resistor is provided to avoid a switch-on of the positioning receiver when the cellular module is switched off or in the reset state.
- The **GPIO3** and **GPIO4** pins are connected respectively to the **TXD1** and **EXTINT0** pins of the u-blox 3.0 V GNSS receiver providing "GNSS data ready" and "GNSS RTC sharing" functions, using a suitable unidirectional general purpose voltage translator (e.g. TI SN74AVC2T245, which additionally provides the partial power down feature so that the 3.0 V GNSS supply can be also ramped up before the **V_INT** 1.8 V cellular supply).

For additional guidelines regarding the design of applications with u-blox 3.0 V GNSS receivers, see the hardware integration manuals of the u-blox GNSS receivers.

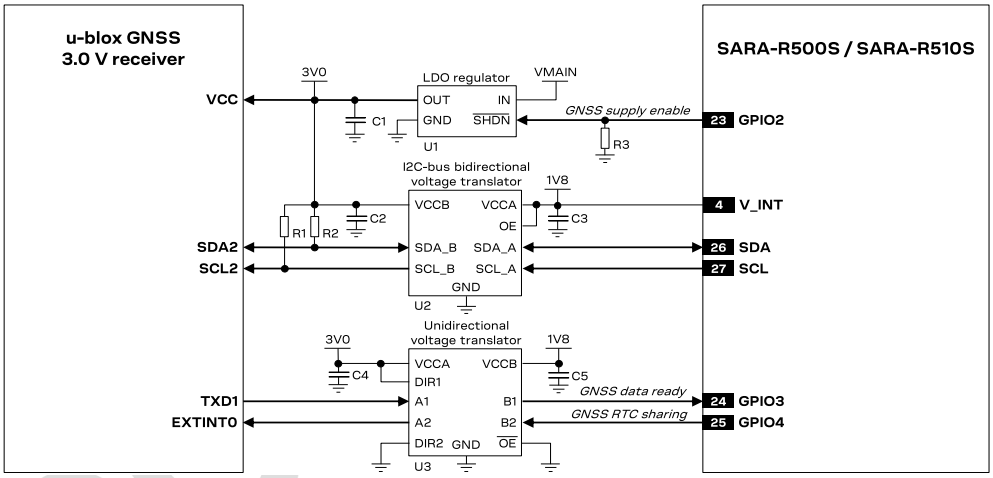

Figure 65: Application circuit for connecting SARA-R500S/SARA-R510S modules to a u-blox 3.0 V GNSS receiver

Reference	Description	Part number - Manufacturer
R1, R2	4.7 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
C2, C3, C4, C5	100 nF capacitor ceramic X5R 0402 10% 10V	GCM155R71C104KA55 - Murata
U1, C1	Voltage regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver hardware integration manual
U2	I2C-bus bidirectional voltage translator	TCA9406DCUR - Texas Instruments
U3	Generic unidirectional voltage translator	SN74AVC2T245 - Texas Instruments

Table 36: Components for connecting SARA-R500S/SARA-R510S modules to a u-blox 3.0 V GNSS receiver

2.6.5.2 Guidelines for DDC (I2C) layout design

The DDC (I2C) serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.7 Audio

Audio is not supported by the "00" product version of SARA-R5 series modules.

2.8 General purpose input / output (GPIO)

2.8.1 Guidelines for GPIO circuit design

A typical usage of SARA-R5 series modules' GPIOs can be the following:

- Network indication provided over **GPIO1** pin (see Figure 66 / Table 37 below)
- "GNSS supply enable" function provided by the **GPIO2** pin [13] (see section 2.6.5)
- "GNSS data ready" function provided by the **GPIO3** pin [13] (see section 2.6.5)
- "GNSS RTC sharing" function provided by the **GPIO4** pin [13] (see section 2.6.5)
- Module status / operating mode indication provided by a GPIO pin (see section 1.6.1)
- SIM card detection provided over **GPIO5** pin (see Figure 48 / Table 28 in section 2.5)
- Antenna dynamic tuning provided over **I2S_TXD** and **I2S_WA** pins (see section 2.4.5)

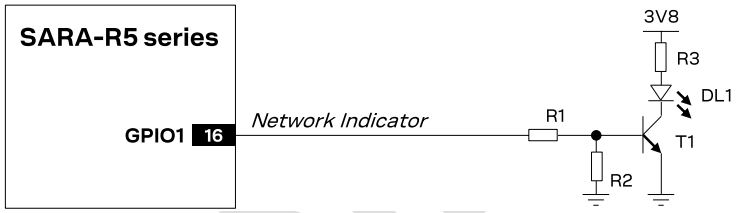

Figure 66: Application circuit for network indication provided over GPIO1

Reference	Description	Part number - Manufacturer
R1	10 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	820 Ω resistor 0402 5% 0.1 W	Generic manufacturer
DL1	LED red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT transistor	BC847 - Infineon

Table 37: Components for network indication application circuit

[13] Not supported by SARA-R510M8S modules

- Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of SARA-R5 series modules.
- Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply (**V_INT**), to avoid latch-up of circuits and allow a clean module boot. If the external signals connected to the module cannot be tri-stated or set low, insert a multi-channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.
- ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.
- If the GPIO pins are not used, they can be left unconnected on the application board.

2.8.2 Guidelines for general purpose input/output layout design

The general purpose input / output pins are generally not critical for layout.

2.9 Reserved pin (RSVD)

SARA-R5 series modules have a pin reserved for future use, marked as **RSVD**. This pin is to be left unconnected on the application board.

2.10 Module placement

An optimized placement allows minimum RF lines' length and closer path from DC source for **VCC**.

Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce electro-magnetic interference that affects the module, analog parts and RF circuits' performance. Implement suitable countermeasures to avoid any possible electro-magnetic compatibility issue.

Make sure that the module is placed in order to keep the antenna (or antennas, for SARA-R510M8S) as far as possible from VCC supply line and related parts (refer to Figure 27), from high speed digital lines (as USB) and from any possible noise source.

Provide enough clearance between the module and any external part: clearance of at least 0.4 mm per side is recommended to let suitable mounting of the parts.

- The heat dissipation during continuous transmission at maximum power can raise the temperature of the application base-board below the SARA-R5 series modules: avoid placing temperature sensitive devices close to the module.

2.11 Module footprint and paste mask

Figure 67 and Table 38 describe the suggested footprint (i.e. copper mask) and paste mask layout for SARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder-resist Mask Defined (NSMD) pad type is recommended over the Solder-resist Mask Defined (SMD) pad type, as it implements the solder resist mask opening 50 μm larger per side than the corresponding copper pad.

The recommended thickness of the stencil for the soldering paste is 150 μm, according to application production process requirements.

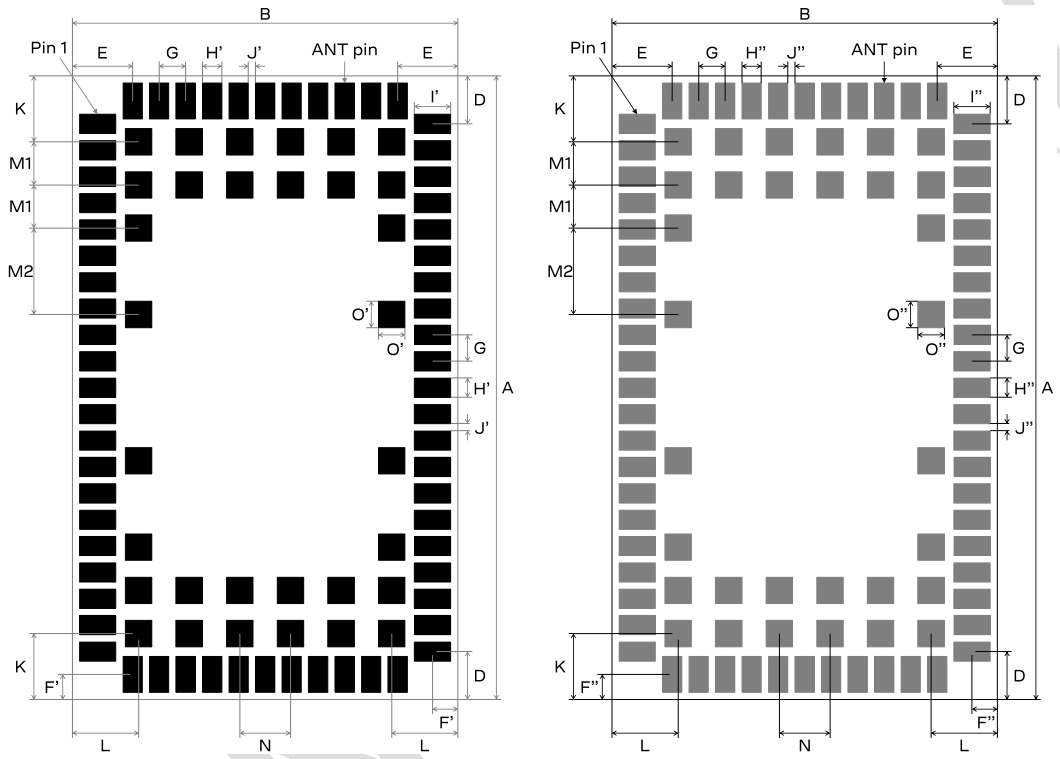

Figure 67: SARA-R5 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	G	1.10 mm	K	2.75 mm
B	16.0 mm	H'	0.80 mm	L	2.75 mm
C	3.00 mm	H''	0.75 mm	M1	1.80 mm
D	2.00 mm	I'	1.50 mm	M2	3.60 mm
E	2.50 mm	I''	1.55 mm	N	2.10 mm
F'	1.05 mm	J'	0.30 mm	O'	1.10 mm
F''	1.00 mm	J''	0.35 mm	O''	1.05 mm

Table 38: SARA-R5 series modules suggested footprint and paste mask dimensions

These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) implemented.

2.12 Schematic for SARA-R5 series module integration

Figure 68 is an example of a schematic diagram where a SARA-R5 series product is integrated into an application board using most of the available interfaces and functions of the module.

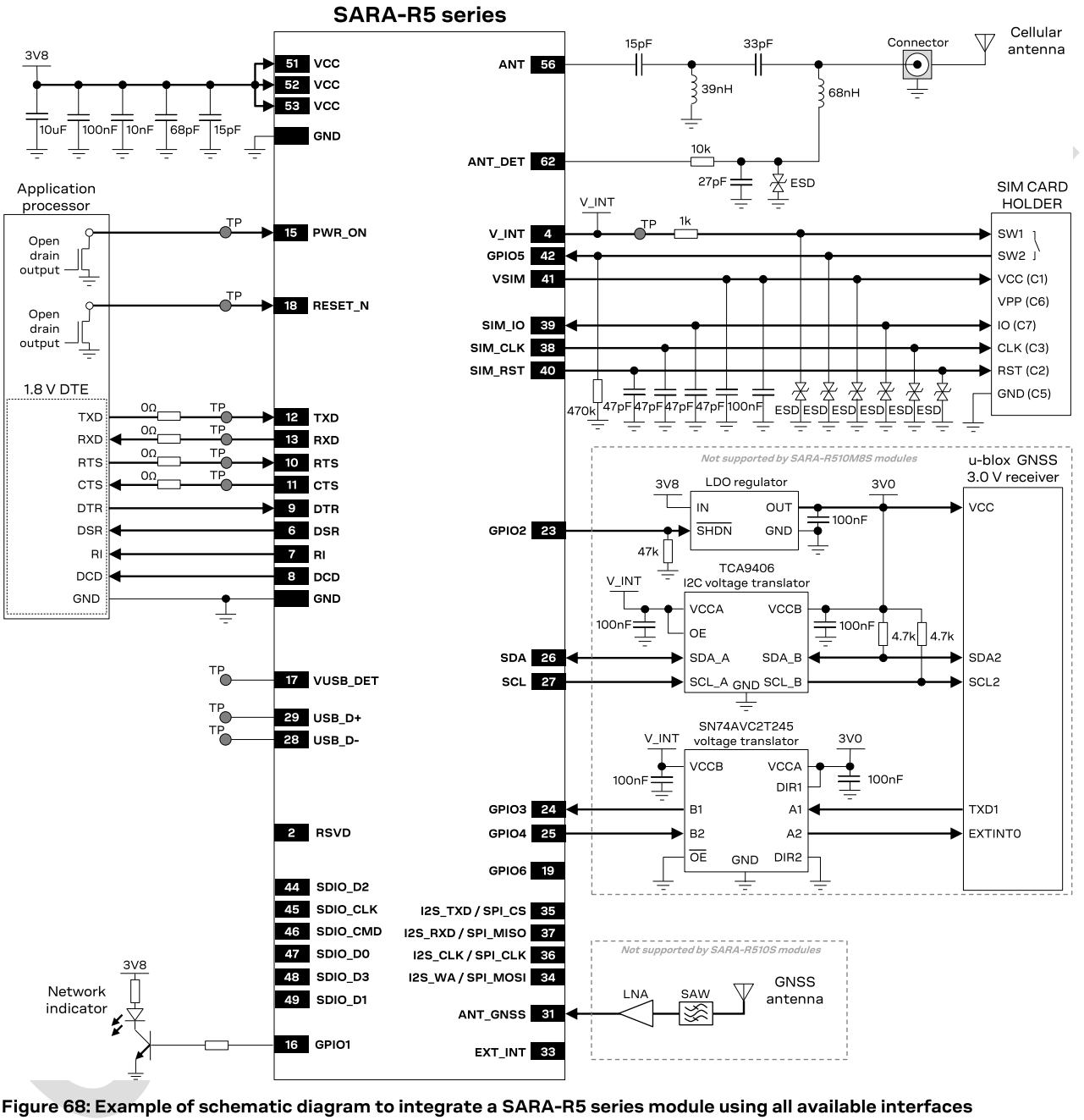

Figure 68: Example of schematic diagram to integrate a SARA-R5 series module using all available interfaces

2.13 Design-in checklist

This section provides a design-in checklist.

2.13.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting the highest peak / pulse current consumption values and the maximum averaged current consumption values in connected mode, as specified in the SARA-R5 series data sheet [1].
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Provide accessible test points directly connected to the following pins of the SARA-R5 series modules: **V_INT**, **PWR_ON** and **RESET_N** for diagnostic purposes.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, as the modules' signal names follow the ITU-T V.24 recommendation [5].
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ It is recommended to provide accessible test points directly connected to the UART and USB interface pins (see sections 2.6.1, 2.6.2).
- ☑ Provide adequate precautions for EMC / ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of SARA-R5 series modules before the switch-on of the generic digital interface supply source (**V_INT**).
- ☑ All unused pins can be left unconnected.

2.13.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** port (cellular antenna RF interface).
- ☑ Check cellular antenna trace design for regulatory compliance perspective (see section 4.2.3 for FCC United States, section 4.3.2 for ISED Canada, and related section 2.4.2.3)
- ☑ For SARA-R510M8S, check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT_GNSS** port (GNSS antenna RF interface).
- ☑ Ensure no coupling occurs between the RF interfaces and noisy or sensitive signals (like SIM signals and high-speed digital lines).
- ☑ Optimize placement for minimum length of RF lines.
- ☑ Check the footprint and paste mask designed for SARA-R5 series module as illustrated in section 2.11.
- ☑ **VCC** line should be enough wide and as short as possible.
- ☑ Route **VCC** supply line away from RF lines / parts (refer to Figure 27) and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picoFarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Ensure an optimal grounding connecting each **GND** pin with application board solid ground layer.
- ☑ Use as many vias as possible to connect the ground planes on multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along RF and high speed lines.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.

2.13.3 Antennas checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement, as reported in section 4.2.2 for FCC United States, in section 4.3.1 for ISED Canada, and in section 4.4 for RED Europe.
- ☑ Ensure high isolation between the cellular antenna and any other antennas or transmitters present on the end device.
- ☑ For SARA-R510M8S, ensure high isolation between the cellular antenna and the GNSS antenna (see also section 1.7.4)

3 Handling and soldering

No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to SARA-R5 series reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the SARA-R5 series data sheet [1] and the u-blox package information user guide [15].

3.2 Handling

The SARA-R5 series modules are Electro-Static Discharge (ESD) sensitive devices.

Ensure ESD precautions are implemented during handling of the module.

Electro-Static Discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of SARA-R5 series modules (as Human Body Model according to JESD22-A114F) is specified in the SARA-R5 series data sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from the International Electrotechnical Commission (IEC) or the American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the SARA-R5 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect the ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in a non-ESD protected work area, implement adequate ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD-safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

"No Clean" soldering paste is strongly recommended for SARA-R5 series modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% tin / 3.9% silver / 0.6% copper) 95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% tin / 4.0% silver / 0.5% copper)
Melting temperature:	217 °C
Stencil thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.11.

☞ The quality of the solder joints should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended for SARA-R5 series modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the “IPC-7530A Guidelines for temperature profiling for mass soldering (reflow and wave) processes”. Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s
  If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 ÷ 120 s
  If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End temperature: +150 ÷ +200 °C
  If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 ÷ 60 s
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects of the solder (solder becomes more brittle) and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

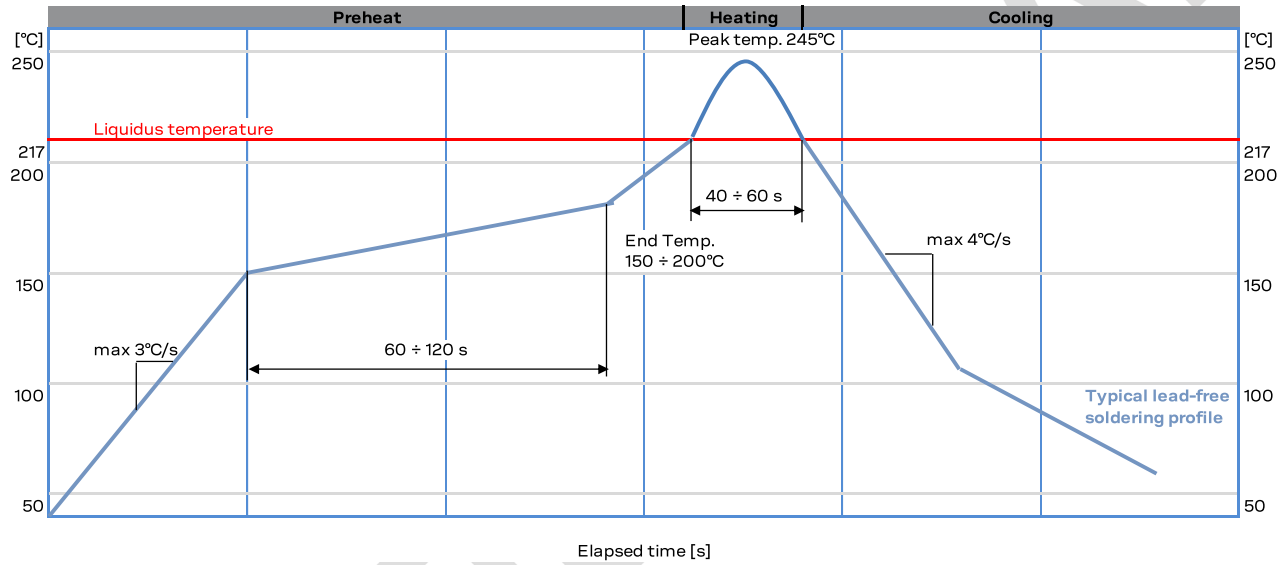

Figure 69: Recommended soldering profile

The modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the module, inspect it optically to verify that it is correctly aligned and centered.

3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the housing, area that is not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside-down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ u-blox gives no warranty against damages to the SARA-R5 series modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the SARA-R5 series module, plus one reflow soldering process to mount other parts).

3.3.6 Wave soldering

SARA-R5 series LGA modules must not be soldered with a wave soldering process.

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for a board with a SARA-R5 series module already populated on it.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ u-blox gives no warranty for damages to the SARA-R5 series modules caused by performing more than a total of two soldering processes (one reflow soldering process to mount the SARA-R5 series module, plus one wave soldering process to mount other THT parts on the application board).

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the RF properties of the cellular modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interference and noise.

☞ u-blox gives no warranty for damages to the cellular modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

The cellular modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty for damages to the cellular modules caused by any ultrasonic processes.

4 Approvals

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called “certification schemes”, which can be divided into:

- Regulatory certifications
  - Country-specific approval required by local government in most regions and countries, as:
    - CE (European Conformity) marking for European Union
    - FCC (Federal Communications Commission) approval for the United States
- Industry certifications
  - Telecom industry-specific approval verifying interoperability between devices and networks:
    - GCF (Global Certification Forum)
    - PTCRB (PCS Type Certification Review Board)
- Operator certifications
  - Operator-specific approvals required by some mobile network operator, such as:
    - AT&T network operator in United States
    - Verizon Wireless network operator in United States

The manufacturer of the end-device that integrates a SARA-R5 series module must take care of all certification approvals required by the specific integrating device to be deployed in the market.

The required certification scheme approvals and relative testing specifications applicable to the end-device that integrates a SARA-R5 series module differ depending on the country or the region where the integrating device is intended to be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device is intended to operate.

Table 39 summarizes the main approvals planned for SARA-R5 series modules.

Certification	SARA-R500S-00B	SARA-R510S-00B	SARA-R510M8S-00B
PTCRB	LTE Cat M1 bands 2,3,4,5,8,12,13,20,25,26	LTE Cat M1 bands 2,3,4,5,8,12,13,20,25,26	LTE Cat M1 bands 2,3,4,5,8,12,13,20,25,26
GCF	LTE Cat M1 bands 2,3,4,5,8,12,13,20,25,26	LTE Cat M1 bands 2,3,4,5,8,12,13,20,25,26	LTE Cat M1 bands 2,3,4,5,8,12,13,20,25,26
CE Europe	LTE Cat M1 bands 3,8,20	LTE Cat M1 bands 3,8,20	LTE Cat M1 bands 3,8,20
FCC US FCC ID	LTE Cat M1 bands 2,4,5,12,13,25,26 XPYUBX19KM01	LTE Cat M1 bands 2,4,5,12,13,25,26 XPYUBX19KM01	LTE Cat M1 bands 2,4,5,12,13,25,26 XPYUBX19KM01
ISED Canada ISED ID	LTE Cat M1 bands 2,4,5,12,13,25,26 8595A-UBX19KM01	LTE Cat M1 bands 2,4,5,12,13,25,26 8595A-UBX19KM01	LTE Cat M1 bands 2,4,5,12,13,25,26 8595A-UBX19KM01
Verizon	LTE Cat M1 bands 4,13	LTE Cat M1 bands 4,13	LTE Cat M1 bands 4,13
AT&T	LTE Cat M1 bands 2,4,5,12	LTE Cat M1 bands 2,4,5,12	LTE Cat M1 bands 2,4,5,12

Table 39: SARA-R5 series main certification approvals summary

☞ For the complete list of planned approvals and for specific details on all country, conformance and network operators’ certifications available for all the different SARA-R5 series modules’ ordering numbers, including related certificates of compliancy, please contact your nearest u-blox office or sales representative.

☞ Check the appropriate applicability of the SARA-R5 series module’s approvals while starting the certification process of the device integrating the module: the re-use of the u-blox cellular module’s approval can significantly reduce the cost and time to market of the application device certification.

The SARA-R5 series modules include the capability to configure the device by selecting the operating Mobile Network Operator Profile, Radio Access Technology, and bands. In the SARA-R5 series AT commands manual [2], see the +UMNOPROF, +URAT, and +UBANDMASK AT commands.

As these configuration decisions are made, u-blox reminds manufacturers of the host application device integrating the SARA-R5 series modules to take care of compliance with all the certification approvals requirements applicable to the specific integrating device to be deployed in the market.

☞ It is strongly recommended to configure the module to the applicable MNO profile, RAT, and LTE bands intended for the host end-device and within regulatory compliance.

☞ The certification of the host application device that integrates a SARA-R5 series module and the compliance of the host application device with all the applicable certification schemes, directives and standards are the sole responsibility of the host application device manufacturer.

SARA-R5 series modules are certified according to all capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to the 3GPP TS 36.521-2 [12] and 3GPP TS 36.523-2 [13], is a statement of the implemented and supported capabilities and options of a device.

☞ The PICS document of the host device integrating SARA-R5 series modules must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the host application device. For more details regarding the AT commands settings that affect the PICS, see the SARA-R5 series AT commands manual [2].

☞ Check the specific settings required by the mobile network operators in use by the host application device, as they may differ from the AT commands factory-programmed settings of the module.

4.2 US Federal Communications Commission notice

United States Federal Communications Commission (FCC) ID: XPYUBX19KM01

4.2.1 Safety warnings review the structure

- Equipment for building-in. Requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, hygroscopic materials, or materials containing asbestos are employed

4.2.2 Declaration of Conformity

This device complies with Part 15 of the FCC rules. Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

⚠ Radiofrequency radiation exposure information: this equipment complies with the radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for the SARA-R5 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value specified in the FCC Grant for mobile and fixed or mobile operating configurations:

- 7.8 dBi in 700 MHz, i.e. LTE FDD-12 band
- 9.2 dBi in 750 MHz, i.e. LTE FDD-13 band
- 9.4 dBi in 850 MHz, i.e. LTE FDD-5 band
- 7.4 dBi in 850 MHz, i.e. LTE FDD-26 band
- 6.8 dBi in 1700 MHz, i.e. LTE FDD-4 band
- 10.3 dBi in 1900 MHz, i.e. LTE FDD-2 band
- 10.4 dBi in 1900 MHz, i.e. LTE FDD-25 band

4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the FCC Grants of the SARA-R5 series modules for their own final host products according to the conditions referenced in the certificates.

⚠ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the FCC Grants of the SARA-R5 series modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for regulatory type approvals of the SARA-R5 series modules, described in details in section 2.4.2.3.

⚠ In case of antenna trace design change, an FCC Class II Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by an FCC Class II Permissive Change application.

⚠ If the FCC Grants of the SARA-R5 series modules can be used for the final host product, as the conditions above are met, the FCC Label of the module shall be visible from the outside, or the host device shall bear a second label stating:

"Contains FCC ID: XPYUBX19KM01"

⚠ IMPORTANT: Manufacturers of portable applications incorporating the SARA-R5 series modules are required to have their final product certified and apply for their own FCC Grant related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices. Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

⚠ Additional Note: as per 47 CFR 15.105 this equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consultant the dealer or an experienced radio/TV technician for help

4.3 Innovation, Science, Economic Development Canada notice

ISED Canada (formerly known as IC - Industry Canada) Certification Number: 8595A-UBX19KM01

4.3.1 Declaration of Conformity

This device complies with the ISED Canada license-exempt RSS standard(s). Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

⚠ Radiofrequency radiation exposure information: this equipment complies with the radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for the SARA-R5 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value stated in the ISED Canada Grant for mobile and fixed or mobile operating configurations:

- 5.6 dBi in 700 MHz, i.e. LTE FDD-12 band
- 5.9 dBi in 750 MHz, i.e. LTE FDD-13 band
- 6.1 dBi in 850 MHz, i.e. LTE FDD-5 band
- 6.1 dBi in 850 MHz, i.e. LTE FDD-26 band
- 6.8 dBi in 1700 MHz, i.e. LTE FDD-4 band
- 8.5 dBi in 1900 MHz, i.e. LTE FDD-2 band
- 8.5 dBi in 1900 MHz, i.e. LTE FDD-25 band

4.3.2 Modifications

ISED Canada requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

⚠ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the ISED Canada Certificates of the SARA-R5 series modules for their own final host products according to the conditions referenced in the certificates.

⚠ Manufacturers of mobile or fixed devices incorporating SARA-R5 series modules are authorized to use the ISED Certificates of SARA-R5 series modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for the regulatory type approvals of the SARA-R5 series modules, described in details in section 2.4.2.3.

⚠ In case of antenna trace design change, a Class IV Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the ISED Multiple Listing (new application) procedure followed by an ISED Class IV Permissive Change application.

⚠ If the ISED Certificates of the SARA-R5 series modules can be used for the final host product, as the conditions above are met, the ISED Label of the module shall be visible from the outside, or the host device shall bear a second label stating:

"Contains IC: 8595A-UBX19KM01"

Innovation, Science and Economic Development Canada (ISED) Notices

This Class B digital apparatus complies with Canadian CAN ICES-3(B) / NMB-3(B).
Operation is subject to the following two conditions:

- this device may not cause interference
- this device must accept any interference, including interference that may cause undesired operation of the device

Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Cellular Module is below the Innovation, Science and Economic Development Canada (ISED) radio frequency exposure limits. The u-blox Cellular Module should be used in a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).

This device has been certified for use in Canada. Status of the listing in the Industry Canada's REL (Radio Equipment List) can be found at the following web address:
http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng

Additional Canadian information on RF exposure also can be found at the following web address:
http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

IMPORTANT: Manufacturers of portable applications incorporating the SARA-R5 series modules are required to have their final product certified and apply for their own Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.
Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Avis d'Innovation, Sciences et Développement économique Canada (ISDE)

Cet appareil numérique de classe B est conforme aux normes canadiennes CAN ICES-3(B) / NMB-3(B). Son fonctionnement est soumis aux deux conditions suivantes:

- cet appareil ne doit pas causer d'interférence
- cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans-fil u-blox Cellular Module est inférieure à la limite d'exposition aux fréquences radio d'Innovation, Sciences et Développement économique Canada (ISDE). Utilisez l'appareil de sans-fil u-blox Cellular Module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur: http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur: http://www.ic.gc.ca/eic/site/smt-gst.nsf/fra/sf08792.html

⚠ IMPORTANT: les fabricants d'applications portables contenant les modules de la SARA-R5 series doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat ISDE Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.
Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

4.4 European Conformance

The SARA-R5 series modules have been evaluated against the essential requirements of the Radio Equipment Directive 2014/53/EU (RED). In order to satisfy the essential requirements of the RED, the modules are compliant with the following standards:

- Radio Spectrum Efficiency (Article 3.2):
  - EN 301 908-1
  - EN 301 908-13
- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1
  - EN 301 489-52
- Health and Safety (Article 3.1a)
  - EN 62368-1
  - EN 62311

⚠ Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

⚠ The gain of the system antenna(s) used for SARA-R5 series modules (i.e. combined transmission line, connector, cable losses and radiating element gain) must not exceed the values stated in the Declaration of Conformity of the modules, for mobile and fixed or mobile operating configurations

The conformity assessment procedure for the SARA-R5 series modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU, has been followed.

Thus, the following marking is included in the product:

CE

5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically on the production line. Stringent quality control processes have been implemented in the production line. Defective units are analyzed in detail to improve production quality.

This is achieved with automatic test equipment (ATE) in the production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. The following Figure 70 illustrates the typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests.

- Digital self-test (firmware download, flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of the reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of the RF characteristics after calibration (i.e. modulation accuracy, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

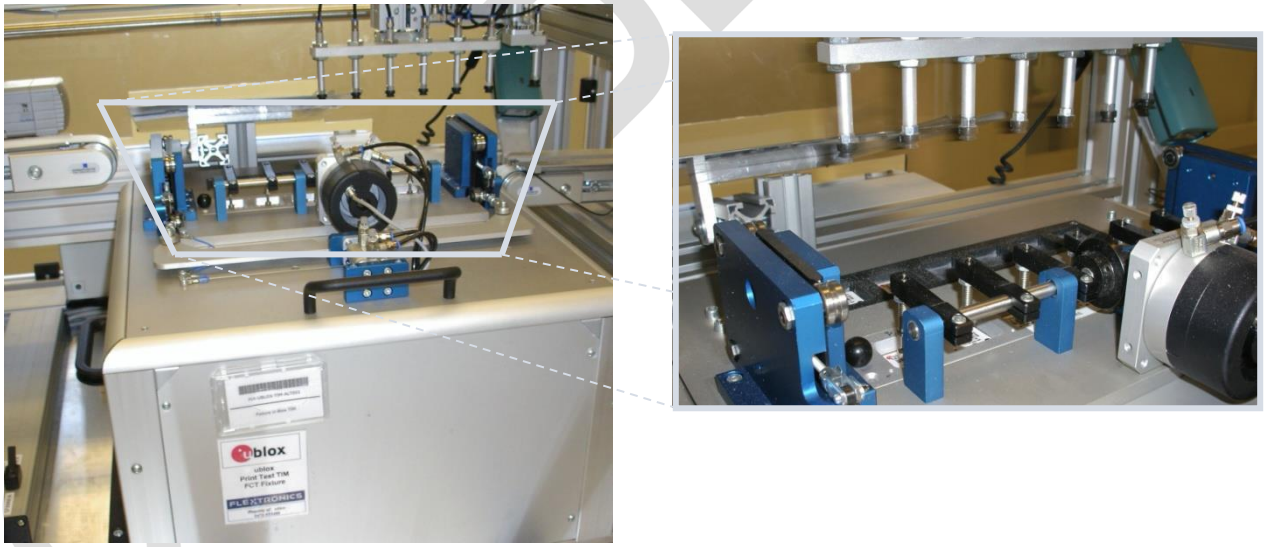

Figure 70: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturers

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat the firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - The soldering and handling process did not damage the module components
  - All module pins are well soldered on the device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with the host controller can be established
  - The interfaces between the module and device are working
  - Overall RF functional test of the device including the antenna/s

Dedicated tests can be implemented to check the device. For example, the measurement of the module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

In addition, module AT commands can be used to perform functional tests on the digital interfaces (communication with the host controller, check the SIM interface, GPIOs, etc.) or to perform RF functional tests (see the following section 5.2.2 for details).

5.2.1 "Go / No go" tests for integrated devices

A "Go / No go" test is typically used to compare the signal quality with a "Golden Device".

The cellular RF functionality should be checked with the DUT (Device Under Test) placed in a location with excellent cellular network coverage and known cellular signal quality. This test should be performed after the data connection has been established. +CSQ is the typical AT command used to check signal quality in term of RSSI, comparing the DUT with a "Golden Device". See the SARA-R5 series AT commands manual [2] for detail usage of the AT command.

☞ These kinds of test may be useful as a "go / no go" test but not for cellular RF performance measurements neither for certifications purpose.

This test is suitable also to check the communications with the host controller, the SIM card and the power supply. It is also a mean to verify if components at the cellular RF interface are well soldered.

The GNSS RF functionality should be checked with the device under test (DUT) placed in an outdoor position, with excellent sky view (HDOP < 3.0). Let the receiver acquire satellites and compare the signal strength with a "Golden Device".

☞ As the electro-magnetic field of a redistribution antenna is not homogenous, indoor tests are in most cases not reliable to check the GNSS RF functionality. These kind of tests may be useful as a 'go/no go' test but not for GNSS sensitivity measurements.

5.2.2 Cellular RF functional tests

The overall cellular RF functional test of the device including the antenna can be performed with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator with the assistance of the +UTEST AT command over the AT command user interface.

The +UTEST AT command provides a simple interface to set the module to Rx or Tx test modes ignoring the LTE signaling protocol. The command can set the module into:

- transmitting mode in a specified channel and power level in all supported bands
- receiving mode in a specified channel to return the measured power level in all supported bands

☞ See the SARA-R5 series AT commands manual [2] for the +UTEST AT command syntax description and detail guide of usage.

This feature allows the measurement of the transmitter and receiver power levels to check the component assembly related to the module cellular antenna interface and to check other device interfaces on which the RF performance depends.

⚠ To avoid module damage during a transmitter test, a suitable antenna according to module specifications or a 50 Ω termination must be connected to the **ANT** port.

⚠ To avoid module damage during a receiver test, the maximum power level received at the **ANT** port must meet module specifications.

☞ The +UTEST AT command sets the module to emit RF power ignoring LTE signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purposes in controlled environments by qualified users and must not be used during the normal module operation. Follow the instructions suggested in the u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Figure 71 illustrates a typical test setup for such an RF functional test.

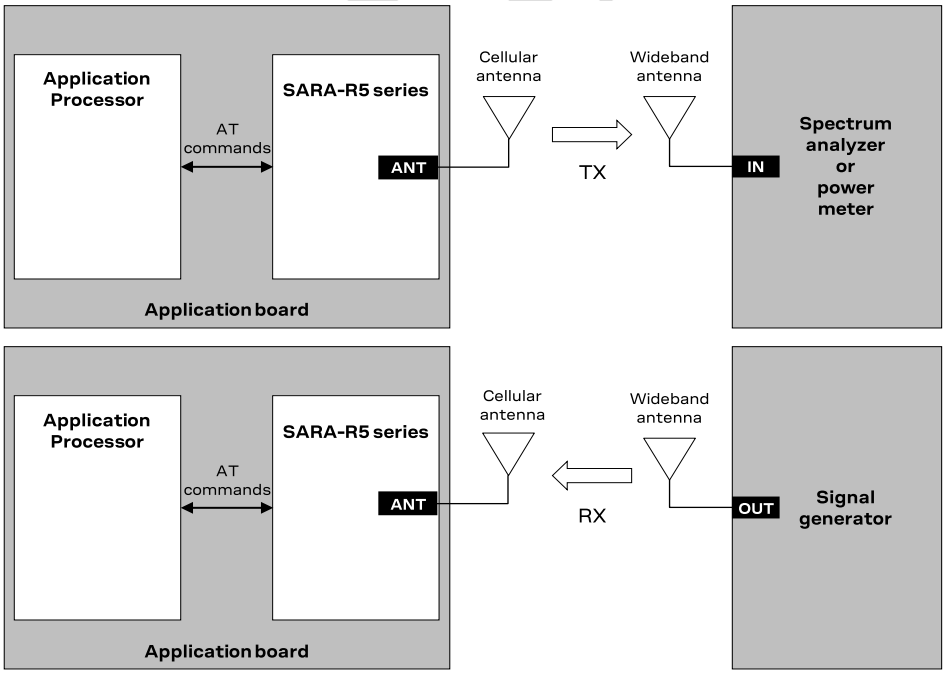

Figure 71: Setup with spectrum analyzer or power meter and signal generator for SARA-R5 series RF measurements

5.2.3 GNSS RF functional tests

The best way to test the GNSS RF functionality is with the use of a Multi-GNSS generator, as it assures reliable and constant signals at every measurement.

u-blox recommends the following Multi-GNSS generator:

- Spirent GSS6300
  Spirent Communications Positioning Technology
  www.positioningtechnology.co.uk

Guidelines for GNSS RF functionality tests:

1. Connect a Multi-GNSS generator to the OEM product.
2. Choose the power level in a way that the “Golden Device” would report a C/No ratio of 38-40 dBHz.
3. Power up the DUT (Device Under Test) and allow enough time for the acquisition.
4. Read the C/No value from the NMEA GSV or the UBX-NAV-SVINFO message (e.g. with u-center).
5. Compare the results to a “Golden Device”.

Appendix

A Migration between SARA modules

A.1 Overview

The u-blox SARA form factor (26.0 x 16.0 mm, 96-pin LGA) includes the following series of modules, with compatible pin assignments as described in Figure 72, so that the modules can be alternatively mounted on a single application PCB using exactly the same copper, solder resist and paste mask:

- SARA-R41x modules supporting LTE Cat M1, LTE Cat NB1 and 2G radio access technologies
- SARA-R42x modules supporting LTE Cat M1, LTE Cat NB2 and 2G radio access technologies
- SARA-R5xx modules supporting LTE Cat M1 and LTE Cat NB2 radio access technologies
- SARA-N2xx modules supporting LTE Cat NB1 radio access technology
- SARA-N3xx modules supporting LTE Cat NB2 radio access technology
- SARA-G3xx modules supporting 2G radio access technology
- SARA-G4xx modules supporting 2G radio access technology
- SARA-U2xx modules supporting 3G and 2G radio access technologies

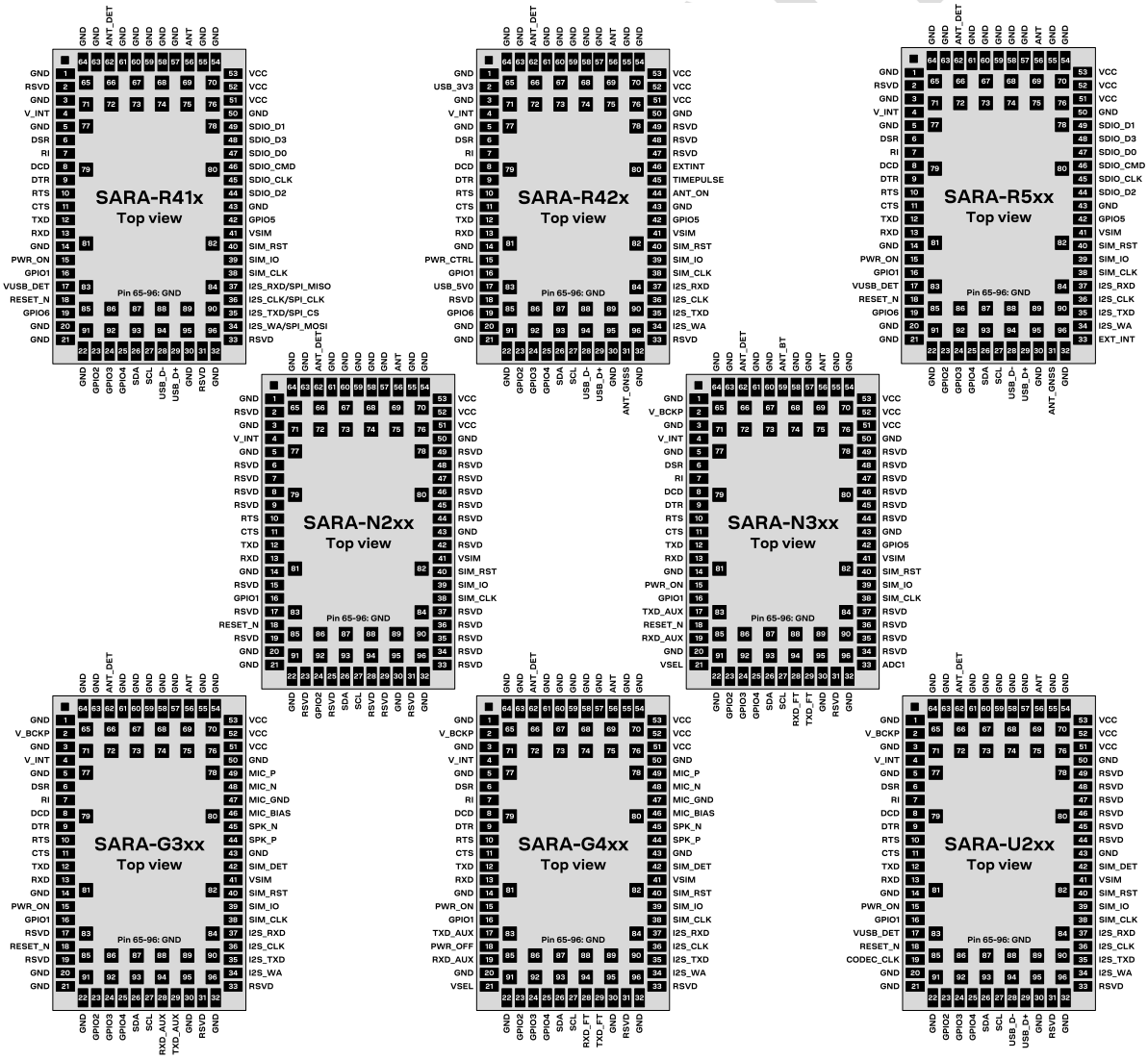

Figure 72: SARA-R4, SARA-R5, SARA-N2, SARA-N3, SARA-G3, SARA-G4, and SARA-U2 modules' layout and pin assignment

The SARA modules are also form-factor compatible with the u-blox LARA, LISA and TOBY cellular module families: although each has a different form factor, the footprints for the TOBY, LISA, LARA and SARA modules have been developed to ensure layout compatibility.

With the u-blox "nested design" solution, any TOBY, LISA, LARA or SARA module can be alternatively mounted on the same space of a single "nested" application board as described in Figure 73. Guidelines to implement a nested application board, description of the u-blox reference nested design and comparison between TOBY, LISA, LARA and SARA modules are provided in the nested design application note [21].

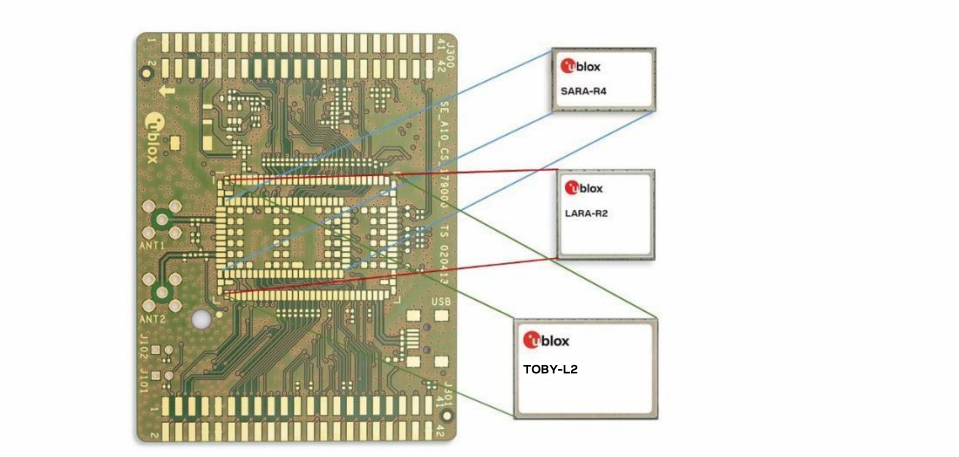

Figure 73: Cellular modules' layout compatibility: all modules can be mounted on the same nested footprint

Table 40 summarizes the main interfaces provided by SARA modules:

Modules	RF						Power			System			SIM		Serial						Audio			Other			
	LTE Cat M1	LTE Cat NB1	LTE Cat NB2	2G	3G	Integrated GNSS receiver	RTC supply I/O	V_INT supply at 1.8V	V_INT supply configurable	Switch-on input pin	Switch-off input pin	Reset input pin	SIM interface	SIM detection	UART	UART AUX	USB	SPI	SDIO	DDC (I²C)	Analog audio	Digital audio	13/26 MHz output	GPIOs	Network indication	Antenna detection	External GNSS control
SARA-R41x	●	●		●				●		●	●		●	●	●		●			●				●	●	●	●
SARA-R42x	●		●	●		●		●		●	●	●	●	●	●	●	●			●		○	○	●	●	●	●
SARA-R5xx	●		○			●		●		●	●	●	●	●	●	●	●	○	○	●		○	○	●	●	●	●
SARA-N2xx		●						●				●	●		●									●	●		
SARA-N3xx			●				●	●	●	●	●	●	●	●	●	○				○				●	●	●	
SARA-G3xx				●			●	●		●		●	●	●	●	●				●	●	●		●	●	●	●
SARA-G4xx				●			●	●	●	●	●		●	●	●	○				○	○	○			●	●	●	○
SARA-U2xx				●	●		●	●		●	●	●	●	●	●	●	●			●		●	●	●	●	●	●

● = supported by available product version ○ = supported by future product versions

Table 40: Summary of the main interfaces in SARA modules

Figure 74 summarizes the frequency ranges of the modules' operating bands.

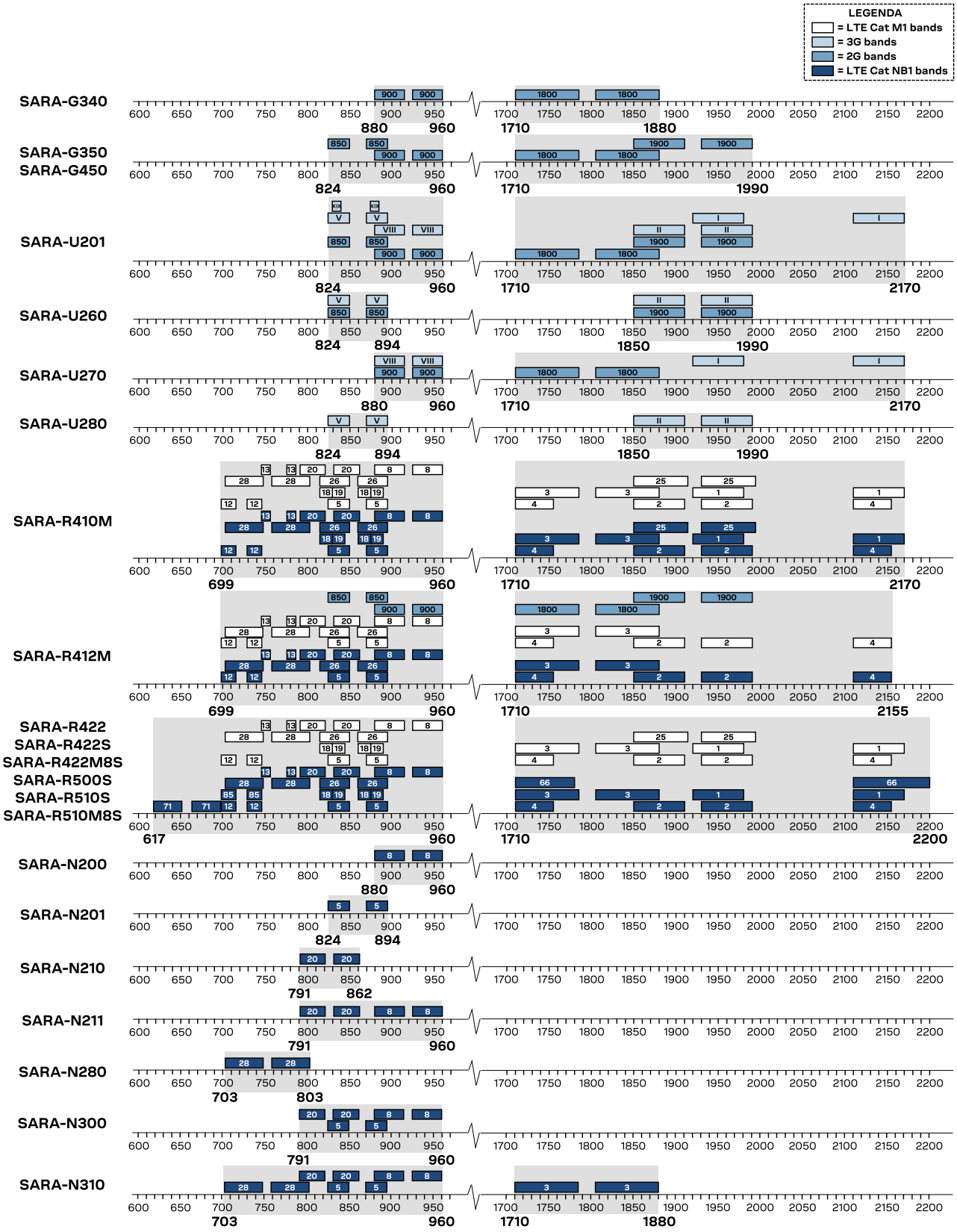

Figure 74: Summary of operating frequency bands supported by SARA modules

A.2 Pin-out comparison between SARA modules

Table 41 shows a pin-out comparison between the SARA-R4, SARA-R5, SARA-N2, SARA-N3, SARA-G3, SARA-G4, and SARA-U2 modules.

No	SARA-R41x	SARA-R42x	SARA-R5xx	SARA-N2xx	SARA-N3xx	SARA-G3xx	SARA-G4xx	SARA-U2xx
1	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground
2	**RSVD** Reserved	**USB_3V3** USB 3V3 supply Input	**RSVD** Reserved	**RSVD** Reserved	**V_BCKP** RTC supply I/O	**V_BCKP** RTC supply I/O	**V_BCKP** RTC supply I/O	**V_BCKP** RTC supply I/O
3	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground
4	**V_INT** Supply output: 1.8 V typ ON when SARA is on TestPoint recommended	**V_INT** Supply output: 1.8 V typ ON when SARA is on TestPoint recommended	**V_INT** Supply output: 1.8 V typ ON when SARA is on TestPoint recommended	**V_INT** Supply output: 1.8 V typ ON when radio is on TestPoint recommended	**V_INT** Supply output: 1.8 V typ / 2.8 V typ ON when SARA is on Voltage value set by VSEL TestPoint recommended	**V_INT** Supply output: 1.8 V typ ON when SARA is on TestPoint recommended	**V_INT** Supply output: 1.8 V typ / 3.0 V typ ON when SARA is on Voltage value set by VSEL TestPoint recommended	**V_INT** Supply output: 1.8 V typ ON when SARA is on TestPoint recommended
5	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground	**GND** Ground
6	**DSR** UART DSR output V_INT level (1.8 V) Driver strength: 2 mA	**DSR** UART DSR output V_INT level (1.8 V) Driver strength: 2 mA	**DSR** UART DSR output V_INT level (1.8 V) Driver strength: 2 mA Configurable as RTS for second auxiliary UART	**RSVD** Reserved	**DSR** UART DSR output[14] V_INT level (1.8 / 2.8 V)	**DSR** UART DSR output V_INT level (1.8 V) Driver strength: 6 mA	**DSR** UART DSR output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	**DSR** UART DSR output V_INT level (1.8 V) Driver strength: 1 mA
7	**RI** UART RI output V_INT level (1.8 V) Driver strength: 2 mA	**RI** UART RI output V_INT level (1.8 V) Driver strength: 2 mA	**RI** UART RI output V_INT level (1.8 V) Driver strength: 2 mA Configurable as CTS for second auxiliary UART	**RSVD** Reserved	**RI** UART RI output V_INT level (1.8 / 2.8 V) Driver strength: 3 mA Configurable as GPIO	**RI** UART RI output V_INT level (1.8 V) Driver strength: 6 mA	**RI** UART RI output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	**RI** UART RI output V_INT level (1.8 V) Driver strength: 2 mA
8	**DCD** UART DCD output V_INT level (1.8 V) Driver strength: 2 mA	**DCD** UART DCD output V_INT level (1.8 V) Driver strength: 2 mA	**DCD** UART DCD output V_INT level (1.8 V) Driver strength: 2 mA Configurable as RXD for second auxiliary UART	**RSVD** Reserved	**DCD** UART DCD output[14] V_INT level (1.8 / 2.8 V)	**DCD** UART DCD output V_INT level (1.8 V) Driver strength: 6 mA	**DCD** UART DCD output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	**DCD** UART DCD output V_INT level (1.8 V) Driver strength: 2 mA

[14] Not supported by '00' product version

No	SARA-R41x	SARA-R42x	SARA-R5xx	SARA-N2xx	SARA-N3xx	SARA-G3xx	SARA-G4xx	SARA-U2xx
9	**DTR**	**DTR**	**DTR**	**RSVD**	**DTR**	**DTR**	**DTR**	**DTR**
	UART DTR input V_INT level (1.8 V) Internal pull-up: ~100 kΩ Set low for URCs/Greeting	UART DTR input V_INT level (1.8 V) Internal pull-up: ~100 kΩ Set low for greeting text	UART DTR input V_INT level (1.8 V) Internal pull-up: ~56 kΩ Set low for greeting text Configurable as TXD for second auxiliary UART	Reserved	UART DTR input[14] V_INT level (1.8 / 2.8 V)	UART DTR input V_INT level (1.8 V) Internal pull-up: ~33 kΩ	UART DTR input V_INT level (1.8 / 3.0 V) Internal pull-up: ~166 kΩ	UART DTR input V_INT level (1.8 V) Internal pull-up: ~14 kΩ Set low for greeting text
10	**RTS**	**RTS**	**RTS**	**RTS**	**RTS**	**RTS**	**RTS**	**RTS**
	UART RTS input V_INT level (1.8 V) Internal pull-up: ~100 kΩ Must be low to use UART on '00', '01' versions	UART RTS input V_INT level (1.8 V) Internal pull-up: ~100 kΩ	UART RTS input V_INT level (1.8 V) Internal pull-up: ~56 kΩ	UART RTS input[15] VCC level (3.6 V typ.) Internal pull-up: ~78 kΩ	UART RTS input V_INT level (1.8 / 2.8 V) Internal pull-up: ~171 kΩ Configurable as GPIO	UART RTS input V_INT level (1.8 V) Internal pull-up:~58 kΩ	UART RTS input V_INT level (1.8 / 3.0 V) Internal pull-up: ~166 kΩ	UART RTS input V_INT level (1.8 V) Internal pull-up: ~8 kΩ
11	**CTS**	**CTS**	**CTS**	**CTS**	**CTS**	**CTS**	**CTS**	**CTS**
	UART CTS output V_INT level (1.8 V) Driver strength: 2 mA	UART CTS output V_INT level (1.8 V) Driver strength: 2 mA	UART CTS output V_INT level (1.8 V) Driver strength: 2 mA	UART CTS output[15] VCC level (3.6 V typ.) Driver strength: 1 mA Configurable as RI or Network Indicator	UART CTS output V_INT level (1.8 / 2.8 V) Driver strength: 3 mA Configurable as GPIO or Network Indicator	UART CTS output V_INT level (1.8 V) Driver strength: 6 mA	UART CTS output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	UART CTS output V_INT level (1.8 V) Driver strength: 6 mA
12	**TXD**	**TXD**	**TXD**	**TXD**	**TXD**	**TXD**	**TXD**	**TXD**
	UART data input V_INT level (1.8 V) Internal PU/PD ~100 kΩ	UART data input V_INT level (1.8 V) Internal pull-up ~100 kΩ	UART data input V_INT level (1.8 V) Internal pull-up: ~56 kΩ	UART data input VCC level (3.6 V typ.) No internal pull-up/down	UART data input V_INT level (1.8 / 2.8 V) Internal pull-up: ~171 kΩ	UART data input V_INT level (1.8 V) Internal pull-up:~18 kΩ	UART data input V_INT level (1.8 / 3.0 V) Internal pull-up: ~166 kΩ	UART data input V_INT level (1.8 V) Internal pull-up: ~8 kΩ
13	**RXD**	**RXD**	**RXD**	**RXD**	**RXD**	**RXD**	**RXD**	**RXD**
	UART data output V_INT level (1.8 V) Driver strength: 2 mA	UART data output V_INT level (1.8 V) Driver strength: 2 mA	UART data output V_INT level (1.8 V) Driver strength: 2 mA	UART data output VCC level (3.6 V typ.) Driver strength: 1 mA	UART data output V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	UART data output V_INT level (1.8 V) Driver strength: 6 mA	UART data output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	UART data output V_INT level (1.8 V) Driver strength: 6 mA
14	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
15	**PWR_ON**	**PWR_CTRL**	**PWR_ON**	**RSVD**	**PWR_ON**	**PWR_ON**	**PWR_ON**	**PWR_ON**
	Power-on/off input Internal pull-up: ~200 kΩ L-level: -0.30 ÷ 0.35 V ON L-level time: 0.15 s min – 3.2 s max OFF L-level pulse time: 1.5 s min TestPoint recommended	Power-on/off / Reset input Internal pull-up L-level: -0.30 ÷ 0.35 V ON L-level pulse time: 0.01 s min – 1.7 s max OFF L-level pulse time: 1.5 s min – 14 s max Reset L-level pulse time: 16 s min TestPoint recommended	Power-on/off input Internal pull-up: ~10 kΩ L-level: -0.30 ÷ 0.30 V ON L-level time: 1 s min – 2 s max OFF L-level pulse time: 1 s min – 5 s max TestPoint recommended	Reserved	Power-on/off input Internal pull-up: ~90 kΩ L-level: 0.00 ÷ 0.20 V ON L-level pulse time: 1 s min – 2.5 s max OFF L-level pulse time: 2.5 s min TestPoint recommended	Power-on input No internal pull-up L-level: -0.10 ÷ 0.65 V ON L-level time: 5 ms min OFF L-level pulse time: Not Available TestPoint recommended	Power-on input Internal pull-up: ~28 kΩ L-level: 0.00 ÷ 0.30 V ON L-level time: 2 s min OFF L-level time: Not Available TestPoint recommended	Power-on/off input No internal pull-up L-level: -0.30 ÷ 0.65 V ON L-level pulse time: 50 µs min / 80 µs max OFF L-level pulse time: 1 s min TestPoint recommended

[15] Not supported by '02' product version

No	SARA-R41x	SARA-R42x	SARA-R5xx	SARA-N2xx	SARA-N3xx	SARA-G3xx	SARA-G4xx	SARA-U2xx
16	**GPIO1**	**GPIO1**	**GPIO1**	**GPIO1**	**GPIO1**	**GPIO1**	**GPIO1**	**GPIO1**
	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	Trace data output V_INT level (1.8 V) Driver strength: 1 mA TestPoint recommended	GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO V_INT level (1.8 V) Driver strength: 6 mA	GPIO V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	GPIO V_INT level (1.8 V) Driver strength: 6 mA
17	**VUSB_DET**	**USB_5V0**	**VUSB_DET**	**RSVD**	**TXD_AUX**	**RSVD**	**TXD_AUX**	**VUSB_DET**
	5 V, USB detect input TestPoint recommended	USB 5V0 supply Input TestPoint recommended	5 V, USB detect input TestPoint recommended	Reserved	AUX UART data input[14] V_INT level (1.8 / 2.8 V)	Reserved	AUX UART data input[14] V_INT level (1.8 / 3.0 V)	5 V, USB detect input TestPoint recommended
18	**RESET_N**	**RSVD**	**RESET_N**	**RESET_N**	**RESET_N**	**RESET_N**	**PWR_OFF**	**RESET_N**
	Shutdown input Internal pull-up: ~37 kΩ L-level: -0.30 ÷ 0.63 V H-level: 1.17 ÷ 2.10 V It triggers shutdown of the whole module when set low or toggled. TestPoint recommended	Reserved	Reset input Internal pull-up: ~56 kΩ L-level: -0.30 ÷ 0.50 V H-level: 1.3 ÷ 2.1 V It triggers module reboot when toggled, without PMU shutdown when low. TestPoint recommended	Reset input Internal pull-up: ~78 kΩ L-level: 0 ÷ 0.36*VCC H-level: 0.52*VCC ÷ VCC It triggers module reboot when toggled, without PMU shutdown when low. TestPoint recommended	Reset shutdown input Internal pull-up: ~70 kΩ L-level: 0.00 ÷ 0.20 V H-level: 0.90 ÷ 1.10 V It triggers module reboot when toggled, with PMU shutdown when low. TestPoint recommended	Reset input Internal diode & pull-up L-level: -0.10 ÷ 0.15 V H-level: 1.40 ÷ 4.50 V It triggers module reboot when toggled, without PMU shutdown when low. TestPoint recommended	Shutdown input Internal diode L-level: 0.00 ÷ 0.10 V H-level: 1.20 ÷ 1.50 V It triggers shutdown of the whole module when set low or toggled. TestPoint recommended	Reset shutdown input Internal pull-up: 10 kΩ L-level: -0.30 ÷ 0.51 V H-level: 1.32 ÷ 2.01 V It triggers module reboot when toggled, with PMU shutdown when low. TestPoint recommended
19	**GPIO6**	**GPIO6**	**GPIO6**	**RSVD**	**RXD_AUX**	**RSVD**	**RXD_AUX**	**CODEC_CLK**
	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	Reserved	AUX UART data output[14] V_INT level (1.8 / 2.8 V)	Reserved	AUX UART data output[14] V_INT level (1.8 / 3.0 V)	13 or 26 MHz output V_INT level (1.8 V) Driver strength: 4 mA
20	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
21	**GND**	**GND**	**GND**	**GND**	**VSEL**	**GND**	**VSEL**	**GND**
	Ground	Ground	Ground	Ground	V_INT voltage selection VSEL connected to GND: V_INT = 1.8 V VSEL unconnected: V_INT = 2.8 V	Ground	V_INT voltage selection VSEL connected to GND: V_INT = 1.8 V VSEL unconnected: V_INT = 3.0 V	Ground
22	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
23	**GPIO2**	**GPIO2**	**GPIO2**	**RSVD**	**GPIO2**	**GPIO2**	**GPIO2**	**GPIO2**
	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	Reserved	GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO V_INT level (1.8 V) Driver strength: 6 mA	GPIO V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	GPIO V_INT level (1.8 V) Driver strength: 6 mA
24	**GPIO3**	**GPIO3**	**GPIO3**	**GPIO2**	**GPIO3**	**GPIO3**	**GPIO3**	**GPIO3**
	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO[15] V_INT level (1.8 V) Driver strength: 1 mA	GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO V_INT level (1.8 V) Driver strength: 5 mA	GPIO V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	GPIO V_INT level (1.8 V) Driver strength: 6 mA
25	**GPIO4**	**GPIO4**	**GPIO4**	**RSVD**	**GPIO4**	**GPIO4**	**GPIO4**	**GPIO4**
	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	GPIO V_INT level (1.8 V) Driver strength: 2 mA	Reserved	GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	GPIO V_INT level (1.8 V) Driver strength: 6 mA	GPIO V_INT level (1.8 / 3.0 V) Driver strength: 3 mA	GPIO V_INT level (1.8 V) Driver strength: 6 mA

No	SARA-R41x	SARA-R42x	SARA-R5xx	SARA-N2xx	SARA-N3xx	SARA-G3xx	SARA-G4xx	SARA-U2xx
26	**SDA**	**SDA**	**SDA**	**SDA**	**SDA**	**SDA**	**SDA**	**SDA**
	I2C data[16] V_INT level (1.8 V) Open drain Internal pull-up: 2.2 kΩ	I2C data V_INT level (1.8 V) Open drain Internal pull-up: 2.2 kΩ	I2C data V_INT level (1.8 V) Open drain Internal active pull-up	I2C data[15] V_INT level (1.8 V) Open drain No internal pull-up	I2C data[14] V_INT level (1.8 / 2.8 V) Open drain Internal pull-up: 10 kΩ	I2C data V_INT level (1.8 V) Open drain No internal pull-up	I2C data[14] V_INT level (1.8 / 3.0 V) Open drain No internal pull-up	I2C data / AUX UART input V_INT level (1.8 V) Open drain No internal pull-up
27	**SCL**	**SCL**	**SCL**	**SCL**	**SCL**	**SCL**	**SCL**	**SCL**
	I2C clock[17] V_INT level (1.8 V) Open drain Internal pull-up: 2.2 kΩ	I2C clock V_INT level (1.8 V) Open drain Internal pull-up: 2.2 kΩ	I2C clock V_INT level (1.8 V) Open drain Internal active pull-up	I2C clock[15] V_INT level (1.8 V) Open drain No internal pull-up	I2C clock V_INT level (1.8 / 2.8 V) Open drain Internal pull-up: 10 kΩ	I2C clock V_INT level (1.8 V) Open drain No internal pull-up	I2C clock[14] V_INT level (1.8 / 3.0 V) Open drain No internal pull-up	I2C clock / AUX UART out V_INT level (1.8 V) Open drain No internal pull-up
28	**USB_D-**	**USB_D-**	**USB_D-**	**RSVD**	**RXD_FT**	**RXD_AUX**	**RXD_FT**	**USB_D-**
	USB data I/O (D-) High-speed USB 2.0 TestPoint recommended	USB data I/O (D-) High-speed USB 2.0, only for FW update / diagnostic TestPoint recommended	USB data I/O (D-) High-speed USB 2.0 TestPoint recommended	Reserved	FW update & Trace output V_INT level (1.8 / 2.8 V) Driver strength: 3 mA TestPoint recommended	AUX UART data output V_INT level (1.8 V) Driver strength: 5 mA TestPoint recommended	FW update & Trace output V_INT level (1.8 / 3.0 V) Driver strength: 3 mA TestPoint recommended	USB data I/O (D-) High-speed USB 2.0 TestPoint recommended
29	**USB_D+**	**USB_D+**	**USB_D+**	**RSVD**	**TXD_FT**	**TXD_AUX**	**TXD_FT**	**USB_D+**
	USB data I/O (D+) High-speed USB 2.0 TestPoint recommended	USB data I/O (D+) High-speed USB 2.0, only for FW update / diagnostic TestPoint recommended	USB data I/O (D+) High-speed USB 2.0 TestPoint recommended	Reserved	FW update & Trace input V_INT level (1.8 / 2.8 V) Internal pull-up: ~171 kΩ TestPoint recommended	AUX UART data input V_INT level (1.8 V) Internal pull-up:~18 kΩ TestPoint recommended	FW update & Trace input V_INT level (1.8 / 3.0 V) Internal pull-up: ~166 kΩ TestPoint recommended	USB data I/O (D+) High-speed USB 2.0 TestPoint recommended
30	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
31	**RSVD**	**ANT_GNSS**	**ANT_GNSS**	**RSVD**	**RSVD**	**RSVD**	**RSVD**	**RSVD**
	Reserved	GNSS RF input[18]	GNSS RF input[18]	Reserved	Reserved	Reserved	Reserved	Reserved
32	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
33	**RSVD**	**RSVD**	**EXT_INT**	**RSVD**	**ADC1**	**RSVD**	**RSVD**	**RSVD**
	Reserved It can be grounded	Reserved TestPoint recommended	External interrupt It can be grounded	Reserved It can be grounded	ADC input It can be grounded	Reserved It must be grounded	Reserved It can be grounded	Reserved It must be grounded
34	**I2S_WA / SPI_MOSI**	**I2S_WA**	**I2S_WA**	**RSVD**	**RSVD**	**I2S_WA**	**I2S_WA**	**I2S_WA**
	I2S W.A.[19] / SPI MOSI[19] V_INT level (1.8 V) Driver strength: 2 mA	I2S Word Alignment[20] V_INT level (1.8 V) Driver strength: 2 mA	I2S Word Alignment[20] V_INT level (1.8 V) Configurable as Antenna Dynamic Tuner	Reserved	Reserved	I2S Word Alignment V_INT level (1.8 V) Driver strength: 6 mA	I2S Word Alignment[14] V_INT level (1.8 V / 3.0 V)	I2S Word Alignment / GPIO V_INT level (1.8 V) Driver strength: 2 mA
35	**I2S_TXD / SPI_CS**	**I2S_TXD**	**I2S_TXD**	**RSVD**	**RSVD**	**I2S_TXD**	**I2S_TXD**	**I2S_TXD**
	I2S out[19] / SPI CS[19] V_INT level (1.8 V) Driver strength: 2 mA	I2S data output[20] V_INT level (1.8 V) Driver strength: 2 mA	I2S data output[20] V_INT level (1.8 V) Configurable as Antenna Dynamic Tuner	Reserved	Reserved	I2S data output V_INT level (1.8 V) Driver strength: 5 mA	I2S data output[14] V_INT level (1.8 V / 3.0 V)	I2S data output / GPIO V_INT level (1.8 V) Driver strength: 2 mA

[16] Not supported by '00' and '01' product versions
[17] Not supported by '00' and '01' product versions
[18] Not supported by SARA-R422, SARA-R422S, SARA-R500S, SARA-R510S
[19] Not supported by '00', '01', 'x2' and 'x3' product versions
[20] Not supported by '00' product version

No	SARA-R41x	SARA-R42x	SARA-R5xx	SARA-N2xx	SARA-N3xx	SARA-G3xx	SARA-G4xx	SARA-U2xx
36	**I2S_CLK / SPI_CLK**	**I2S_CLK**	**I2S_CLK**	**RSVD**	**RSVD**	**I2S_CLK**	**I2S_CLK**	**I2S_CLK**
	I2S clock[19] / SPI clock[19] V_INT level (1.8 V) Driver strength: 2 mA	I2S clock[20] V_INT level (1.8 V) Driver strength: 2 mA	I2S clock[20] V_INT level (1.8 V)	Reserved	Reserved	I2S clock V_INT level (1.8 V) Driver strength: 5 mA	I2S clock[14] V_INT level (1.8 V / 3.0 V)	I2S clock / GPIO V_INT level (1.8 V) Driver strength: 2 mA
37	**I2S_RXD / SPI_MISO**	**I2S_RXD**	**I2S_RXD**	**RSVD**	**RSVD**	**I2S_RXD**	**I2S_RXD**	**I2S_RXD**
	I2S input[21] / SPI MISO[21] V_INT level (1.8 V)	I2S input[22] V_INT level (1.8 V)	I2S data input[22] V_INT level (1.8 V)	Reserved	Reserved	I2S data input V_INT level (1.8 V) Internal pull-down: ~18 kΩ	I2S data input[14] V_INT level (1.8 V / 3.0 V)	I2S data input / GPIO V_INT level (1.8 V) Internal pull-down: ~8 kΩ
38	**SIM_CLK**	**SIM_CLK**	**SIM_CLK**	**SIM_CLK**	**SIM_CLK**	**SIM_CLK**	**SIM_CLK**	**SIM_CLK**
	1.8 V / 3 V SIM clock	1.8 V / 3 V SIM clock	1.8 V / 3 V SIM clock	1.8 V SIM clock	1.8 V / 3 V SIM clock	1.8 V / 3 V SIM clock	1.8 V / 3 V SIM clock	1.8 V / 3 V SIM clock
39	**SIM_IO**	**SIM_IO**	**SIM_IO**	**SIM_IO**	**SIM_IO**	**SIM_IO**	**SIM_IO**	**SIM_IO**
	1.8 V / 3 V SIM data I/O Internal pull-up: 4.7 kΩ	1.8 V / 3 V SIM data I/O Internal pull-up: 4.7 kΩ	1.8 V / 3 V SIM data I/O Internal pull-up: 4.7 kΩ	1.8 V SIM data I/O Internal pull-up: 4.7 kΩ	1.8 V / 3 V SIM data I/O Internal pull-up: 4.7 kΩ	1.8 V / 3 V SIM data I/O Internal pull-up: 4.7 kΩ	1.8 V / 3 V SIM data I/O Internal pull-up: 4.7 kΩ	1.8 V / 3 V SIM data I/O Internal pull-up: 4.7 kΩ
40	**SIM_RST**	**SIM_RST**	**SIM_RST**	**SIM_RST**	**SIM_RST**	**SIM_RST**	**SIM_RST**	**SIM_RST**
	1.8 V / 3 V SIM reset	1.8 V / 3 V SIM reset	1.8 V / 3 V SIM reset	1.8 V SIM reset	1.8 V / 3 V SIM reset	1.8 V / 3 V SIM reset	1.8 V / 3 V SIM reset	1.8 V / 3 V SIM reset
41	**VSIM**	**VSIM**	**VSIM**	**VSIM**	**VSIM**	**VSIM**	**VSIM**	**VSIM**
	1.8 V / 3 V SIM supply	1.8 V / 3 V SIM supply	1.8 V / 3 V SIM supply	1.8 V SIM supply	1.8 V / 3 V SIM supply	1.8 V / 3 V SIM supply	1.8 V / 3 V SIM supply	1.8 V / 3 V SIM supply
42	**GPIO5**	**GPIO5**	**GPIO5**	**RSVD**	**GPIO5**	**SIM_DET**	**SIM_DET**	**SIM_DET**
	GPIO / SIM detection input V_INT level (1.8 V) Driver strength: 2 mA	GPIO / SIM detection input V_INT level (1.8 V) Driver strength: 2 mA	SIM detection input V_INT level (1.8 V) Driver strength: 2 mA	Reserved	SIM detection input / GPIO V_INT level (1.8 / 2.8 V) Driver strength: 3 mA	SIM detection input V_INT level (1.8 V)	SIM detection input V_INT level (1.8 V / 3.0 V)	SIM detection input V_INT level (1.8 V) Configurable as GPIO
43	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
44	**SDIO_D2**	**ANT_ON**	**SDIO_D2**	**RSVD**	**RSVD**	**SPK_P**	**SPK_P**	**RSVD**
	SDIO serial data [2][21]	GNSS LNA on/off signal connected to internal LNA	SDIO serial data [2][22] Configurable as SPI_CLK (diagnostic only)	Reserved	Reserved	Analog audio output (+)	Analog audio output (+)[14]	Reserved
45	**SDIO_CLK**	**TIMEPULSE**	**SDIO_CLK**	**RSVD**	**RSVD**	**SPK_N**	**SPK_N**	**RSVD**
	SDIO serial clock[21]	GNSS time pulse output	SDIO serial clock[22]	Reserved	Reserved	Analog audio output (-)	Analog audio output (-)[14]	Reserved
46	**SDIO_CMD**	**EXTINT**	**SDIO_CMD**	**RSVD**	**RSVD**	**MIC_BIAS**	**MIC_BIAS**	**RSVD**
	SDIO command[21]	GNSS external interrupt	SDIO command[22] Configurable as Time Synchronization Input	Reserved	Reserved	Microphone supply	Microphone supply[14]	Reserved
47	**SDIO_D0**	**RSVD**	**SDIO_D0**	**RSVD**	**RSVD**	**MIC_GND**	**MIC_GND**	**RSVD**
	SDIO serial data [0][21]	Reserved	SDIO serial data [0][22] Configurable as SPI_MOSI (diagnostic only)	Reserved	Reserved	Microphone ground	Microphone ground[14]	Reserved
48	**SDIO_D3**	**RSVD**	**SDIO_D3**	**RSVD**	**RSVD**	**MIC_N**	**MIC_N**	**RSVD**
	SDIO serial data [3][21]	Reserved	SDIO serial data [3][22] Configurable as SPI_CS (diagnostic only)	Reserved	Reserved	Analog audio input (-)	Analog audio input (-)[14]	Reserved

[21] Not supported by '00', '01', 'x2' and 'x3' product versions
[22] Not supported by '00' product version

No	SARA-R41x	SARA-R42x	SARA-R5xx	SARA-N2xx	SARA-N3xx	SARA-G3xx	SARA-G4xx	SARA-U2xx
49	**SDIO_D1**	**RSVD**	**SDIO_D1**	**RSVD**	**RSVD**	**MIC_P**	**MIC_P**	**RSVD**
	SDIO serial data [1][23]	Reserved	SDIO serial data [1][24] Configurable as SPI_MISO (diagnostic only)	Reserved	Reserved	Analog audio input (+)	Analog audio input (+)[14]	Reserved
50	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
51-53	**VCC**	**VCC**	**VCC**	**VCC**	**VCC**	**VCC**	**VCC**	**VCC**
	Module supply input Normal op. range: 3.20 ÷ 4.20 V Extended op. range: 3.00 ÷ 4.30 V No turn-on by VCC apply	Module supply input Normal op. range: 3.20 ÷ 4.50 V Extended op. range: 3.00 ÷ 4.50 V No turn-on by VCC apply	Module supply input Normal op. range: 3.30 ÷ 4.40 V Extended op. range: 3.00 ÷ 4.50 V SARA-R510S: No turn-on by VCC apply SARA-R500S /-R510M8S: Turn-on by VCC apply	Module supply input Normal op. range: 3.10 ÷ 4.00 V Extended op. range: 2.75 ÷ 4.20 V Turn-on by VCC apply	Module supply input Normal op. range: 3.20 ÷ 4.20 V Extended op. range: 2.60 ÷ 4.20 V No turn-on by VCC apply	Module supply input Normal op. range: 3.35 ÷ 4.50 V Extended op. range: 3.00 ÷ 4.50 V Turn-on by VCC apply	Module supply input Normal op. range: 3.40 ÷ 4.20 V Extended op. range: 3.10 ÷ 4.50 V No turn-on by VCC apply	Module supply input Normal op. range: 3.30 ÷ 4.40 V Extended op. range: 3.10 ÷ 4.50 V Turn-on by VCC apply
54-55	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
56	**ANT**	**ANT**	**ANT**	**ANT**	**ANT**	**ANT**	**ANT**	**ANT**
	Cellular RF I/O	Cellular RF I/O	Cellular RF I/O	Cellular RF I/O	Cellular RF I/O	Cellular RF I/O	Cellular RF I/O	Cellular RF I/O
57-58	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
59	**GND**	**GND**	**GND**	**GND**	**ANT_BT**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Bluetooth RF I/O[24] It can be grounded	Ground	Ground	Ground
60-61	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground
62	**ANT_DET**	**ANT_DET**	**ANT_DET**	**ANT_DET**	**ANT_DET**	**ANT_DET**	**ANT_DET**	**ANT_DET**
	Antenna detection	Antenna detection	Antenna detection	Antenna detection[25]	Antenna detection / ADC	Antenna detection	Antenna detection	Antenna detection
63-96	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**	**GND**
	Ground	Ground	Ground	Ground	Ground	Ground	Ground	Ground

Table 41: SARA-R4, SARA-R5, SARA-N2, SARA-N3, SARA-G3, SARA-G4 and SARA-U2 series modules pin assignment and description, with remarks for migration

☞ For further details regarding characteristics, capabilities, usage or settings applicable for each interface of the SARA-R4, SARA-R5, SARA-N2, SARA-N3, SARA-G3, SARA-G4 and SARA-U2 cellular modules, see the related data sheet [1], [16], [17], [18], [22], [23], [24], the related system integration manual [19], [20], [25], [26], and the nested design application note [21].

[23] Not supported by '00', '01', 'x2' and 'x3' product versions
[24] Not supported by '00' product version
[25] Not supported by '02' product version

A.3 Schematic for SARA modules integration

Figure 75 shows an example of a simple schematic diagram where a SARA-N2, SARA-N3, SARA-R4, SARA-R5, SARA-G3, SARA-G4 and/or SARA-U2 module is integrated in the same application board, using the main available interfaces and functions of the modules.

The different mounting options for the external parts are highlighted in different colors as described in the legend, according to the interfaces supported by the each module, and related characteristics.

In the simple schematic diagram shown in Figure 75, the **VCC** supply of the SARA modules is provided by a suitable supply source, at 3.6 V nominal voltage, not illustrated in the diagram. The application processor controls the **VCC** supply of the modules by means of a high-side switch. Proper bypass capacitors and EMI filter parts are placed close to the **VCC** input pins of the modules.

While selecting the supply source for SARA cellular modules, consider with adequate safe design margin the maximum current consumption of each SARA cellular module (see the related data sheet [1], [16], [17], [18], [22], [23], [24]), as it reflects the RATs supported. For additional specific design guidelines, see the **VCC** interface sections in related system integration manual [19], [20], [25], [26].

The switch-on sequence of SARA-N2, SARA-R500S, SARA-R510M8S, SARA-G3 and SARA-U2 starts by applying a valid **VCC** supply.

Instead, SARA-N3, SARA-R4, SARA-R510S and SARA-G4 modules continue to be switched off even after a valid **VCC** supply has been applied: the **PWR_ON** / **PWR_CTRL** line has to be properly toggled, with valid **VCC** supply present, to start the switch-on sequence of these modules.

The application processor is connected to the SARA modules over main UART interface in the simple schematic diagram illustrated in Figure 75.

The design is implemented with the UART interface configured at the same voltage level on both sides (application processor and SARA module), without using voltage translators, as it is recommended in order to minimize any possible leakage and benefit from the extremely low current consumption of the u-blox LPWA modules, in particular in deep-sleep power saving mode.

Thus, the supply level of the application processor is selected to properly set its UART voltage level:

- at the **VCC** level of the module (3.6 V nominal), in case of SARA-N2
- at the **V_INT** level of the module (2.8 V nominal, with **VSEL** unconnected), in case of SARA-N3
- at the **V_INT** level of the module (3.0 V nominal, with **VSEL** unconnected), in case of SARA-G4
- at the **V_INT** level of the module (1.8 V nominal), for all the other SARA modules

The **TXD** and **RXD** data lines, supported by all the SARA modules for AT and data communication, are directly connected with the application processors. For additional specific design guidelines, see the UART sections in the related system integration manual [19], [20], [25], [26].

The **RTS**, **CTS** and **RI** lines are connected with the application processors by 0 Ω jumpers for all the SARA modules except the SARA-N2 series, which does not support hardware flow control functionality and instead supports **RI** functionality over the **CTS** output pin.

The other UART lines are not implemented in the simple example of design shown in Figure 75, and the **DTR** input is grounded as required to have URCs and the greeting text sent by SARA-R4, SARA-R5 and SARA-U2 modules.

The application processor controls the **PWR_ON** / **PWR_CTRL** line by means of an open drain driver in the circuit illustrated in Figure 75, with an external pull-up to **V_BCKP** for SARA-G3 and SARA-U2 modules. The whole circuit need not be populated for SARA-N2 modules, which do not provide **PWR_ON** / **PWR_CTRL** input.

The application processor controls the **RESET_N** / **PWR_OFF** line by means of open drain driver too. The assertion or toggling of this line causes different actions:

- the **RESET_N** line triggers an unconditional reboot of the module when toggled, without internal PMU shutdown when set low, in case of SARA-N2, SARA-R5 and SARA-G3
- the **RESET_N** line triggers an unconditional reboot of the module when toggled, with internal PMU shutdown when set low, in case of SARA-N3 and SARA-U2
- the **RESET_N** / **PWR_OFF** line triggers an unconditional shutdown of the module when set low or toggled, in case of SARA-R4 and SARA-G4

The circuit need not be populated for SARA-R42x modules, not providing **RESET_N** / **PWR_OFF** input.

The timings for proper control of the **PWR_ON** / **PWR_CTRL**, **RESET_N** / **PWR_OFF** lines of the SARA modules are reported in the related data sheet [1], [16], [17], [18], [22], [23], [24].

The **ANT** cellular antenna circuit is implemented in Figure 75 with also the optional **ANT_DET** antenna detection circuit according to the design guidelines provided in the Antenna interface sections of the related system integration manual [19], [20], [25], [26].

While selecting the antenna for SARA cellular modules, consider the frequency range supported by each SARA module, as illustrated in Figure 74.

Designers have to take care of the antenna from all perspective at the very start of the design phase, when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the end-device integrating cellular modules with all the applicable required certification schemes depending on the antenna's radiating performance.

While implementing the RF antenna design for SARA cellular modules, consider providing the best possible return loss in the frequency range supported by the modules, and place the antenna far from **VCC** supply line and related parts, as well as far from any possible noise source.

The **ANT_GNSS** circuit is implemented in Figure 75 for SARA-R422M8S and SARA-R510M8S, with also the optional external SAW and LNA for best performance and improved jamming immunity

The SIM interface circuit is implemented in Figure 75 with also the optional SIM detection function, according to the design guidelines provided in SIM interface sections of the related system integration manual [19], [20], [25], [26]: bypass capacitors with proper self-resonant frequency are recommended to be placed close to the SIM connector, as well as ESD protections.

The **GPIO1** that controls a LED as shown in Figure 75, to provide the network status indication, is supported by all SARA modules except SARA-N2 series that can provide this function on the **CTS** pin. Other functions can be enabled on the GPIOs of the SARA modules, as described in the related data sheet [1], [16], [17], [18], [22], [23], [24], and related AT commands manual [2], [27], [28], [29].

Test-points for diagnostic or FW upgrade are provided as recommended in Figure 75 at these pins:

- **V_INT**
- **PWR_ON / PWR_CTRL**
- **RESET_N / PWR_OFF**
- **GPIO1**
- **VUSB_DET / USB_5V0**
- **USB_3V3**
- **USB_D+ / TXD_FT / TXD_AUX**
- **USB_D- / RXD_FT / RXD_AUX**
- **RSVD #33**

All the GND pins are intended to be externally connected to ground, while other interfaces are not implemented or not used in the simple example of design as shown in Figure 75.

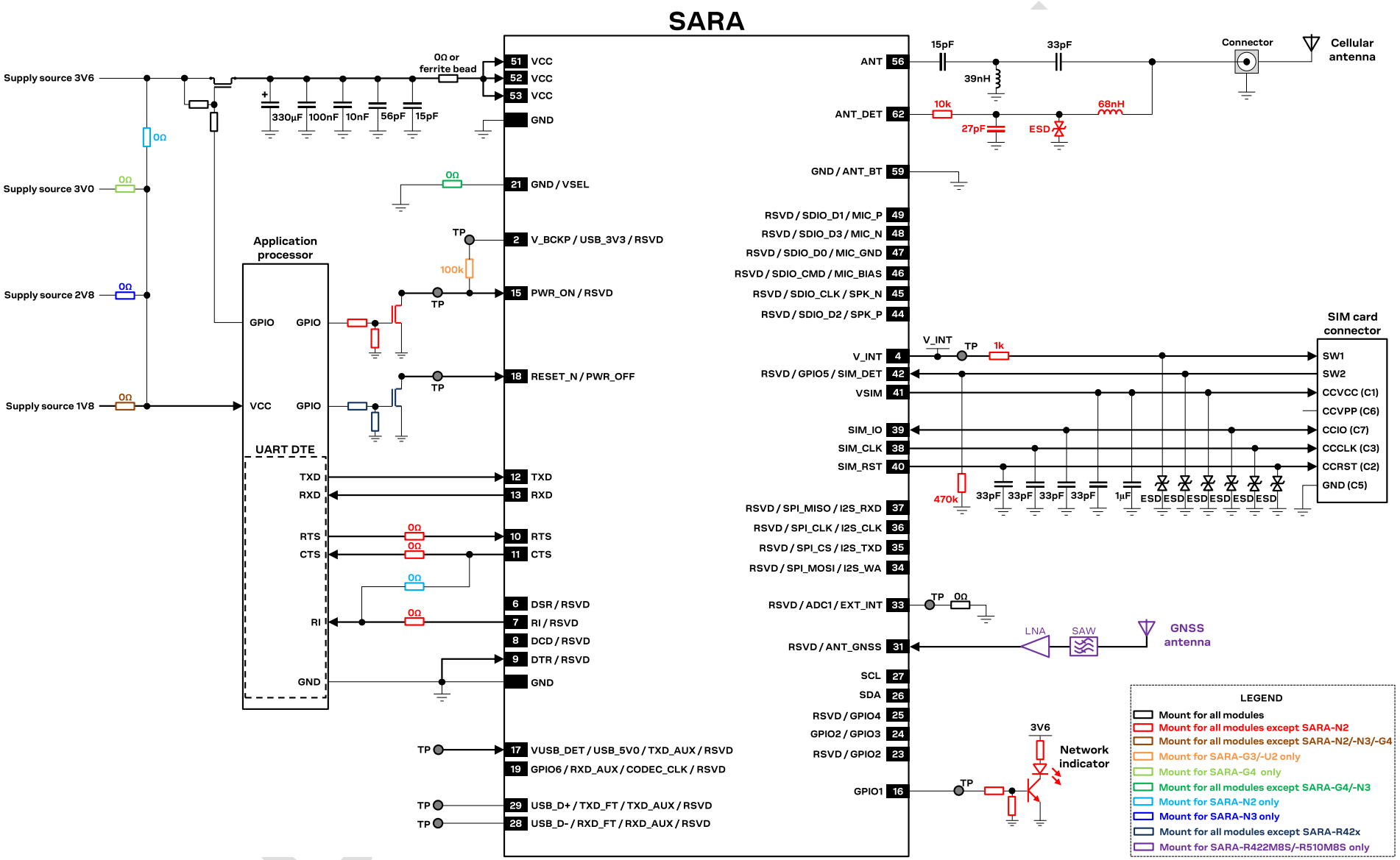

Figure 75: Example schematic to integrate a SARA-R4, SARA-R5, SARA-N2, SARA-N3, SARA-G3, SARA-G4 and/or SARA-U2 module in the same application PCB, using main interfaces

B Glossary

Abbreviation	Definition
2G	2nd Generation Cellular Technology (GSM, GPRS, EGPRS)
3G	3rd Generation Cellular Technology (UMTS, HSDPA, HSUPA)
3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
AR	Axial Ratio
AT	AT Command Interpreter Software Subsystem, or attention
BB	Baseband
BeiDou	Chinese satellite navigation system
BJT	Bipolar Junction Transistor
C/No	Carrier to Noise ratio
C2PC	Class II Permissive Change
C4PC	Class IV Permissive Change
Cat	Category
CDMA	Code Division Multiple Access
CE	European Conformity
CMOS	Complementary Metal-Oxide-Semiconductor
CoAP	Constrained Application Protocol
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTLS	Datagram Transport Layer Security
DTR	Data Terminal Ready
EDGE	Enhanced Data rates for GSM Evolution (EGPRS)
eDRX	Extended Discontinuous Reception
EGPRS	Enhanced General Packet Radio Service (EDGE)
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
E-UTRA	Evolved Universal Terrestrial Radio Access
FCC	Federal Communications Commission United States
FDD	Frequency Division Duplex
FOAT	Firmware Over AT commands
FOTA	Firmware Over The Air
FTP	File Transfer Protocol
FW	Firmware

Abbreviation	Definition
Galileo	European satellite navigation system
GCF	Global Certification Forum
GLONASS	GLObal NAvigation Satellite System (Russian satellite navigation system)
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile communication
HBM	Human Body Model
HDLC	High-level Data Link Control
HSPA	High-Speed Packet Access
HTTP	HyperText Transfer Protocol
HW	Hardware
I2C	Inter-Integrated Circuit interface
I2S	Inter IC Sound interface
IC	Integrated Circuit
IEC	International Electrotechnical Commission
IoT	Internet of Things
IP	Internet Protocol
IPC	Institute of Printed Circuits
ISED	Innovation, Science and Economic Development Canada
ISO	International Organization for Standardization
LDO	Low-Dropout
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPWA	Low Power Wide Area
LTE	Long Term Evolution
LwM2M	Open Mobile Alliance Lightweight Machine-to-Machine protocol
M2M	Machine-to-Machine
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MQTT	Message Queuing Telemetry Transport
MQTT-SN	Message Queuing Telemetry Transport for Sensor Networks
N/A	Not Applicable
NAS	Non Access Stratum
NB	Narrow Band
NTC	Negative Temperature Coefficient
OEM	Original Equipment Manufacturer device: an application device integrating a u-blox cellular module
OTA	Over The Air
PA	Power Amplifier
PCB	Printed Circuit Board
PCN	Product Change Notification / Sample Delivery Note / Information Note
PFM	Pulse Frequency Modulation
PIFA	Planar Inverted-F Antenna
PPS	Pulse Per Second

Abbreviation	Definition
PSM	Power Saving Mode
PTCRB	PCS Type Certification Review Board
PWM	Pulse Width Modulation
QZSS	Quasi-Zenith Satellite System
RAT	Radio Access Technology
RF	Radio Frequency
RI	Ring Indicator
RSSI	Received Signal Strength Indication
RSVD	Reserved
RTC	Real Time Clock
RTS	Request To Send
Rx	Receiver
SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation System
SDIO	Secure Digital Input Output
SIM	Subscriber Identification Module
SMA	SubMiniature version A
SMD	Surface Mounting Device
SMS	Short Message Service
SMT	Surface Mount Technology
SP4T	Single-Pole, 4-Throws
SPI	Serial Peripheral Interface
SRF	Self-Resonant Frequency
TBD	To Be Defined
TCP	Transmission Control Protocol
THT	Through-Hole Technology
TIS	Total Isotropic Sensitivity
TLS	Transport Layer Security
TP	Test-Point
TRP	Total Radiated Power
Tx	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-Link (Transmission)
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

Table 42: Explanation of the abbreviations and terms used

Related documents

[1] u-blox SARA-R5 series data sheet, doc. no. UBX-19016638
[2] u-blox SARA-R5 series AT commands manual, doc. no. UBX-19047455
[3] u-blox EVK-R5 user guide, doc. no. UBX-19042592
[4] Universal Serial Bus revision 2.0 specification, https://www.usb.org/
[5] ITU-T recommendation V.24 - 02-2000 - List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE), http://www.itu.int/rec/T-REC-V.24-200002-I/en
[6] 3GPP TS 27.007 - AT command set for User Equipment (UE)
[7] 3GPP TS 27.005 - Use of Data Terminal Equipment - Data Circuit terminating; Equipment (DTE - DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[8] 3GPP TS 27.010 - Terminal Equipment to User Equipment (TE-UE) multiplexer protocol
[9] I2C-bus specification and user manual - UM10204 - NXP Semiconductors, https://www.nxp.com/docs/en/user-guide/UM10204.pdf
[10] GSM Association TS.09 - Battery Life Measurement and Current Consumption Technique, https://www.gsma.com/newsroom/wp-content/uploads//TS.09-v10.2.pdf
[11] 3GPP TS 36.521-1 - Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing
[12] 3GPP TS 36.521-2 - Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)
[13] 3GPP TS 36.523-2 - Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)
[14] u-blox end user test application note, doc. no. UBX-13001922
[15] u-blox package information user guide, doc. no. UBX-14001652
[16] u-blox SARA-G3 series data sheet, doc. no. UBX-13000993
[17] u-blox SARA-U2 series data sheet, doc. no. UBX-13005287
[18] u-blox SARA-N2 series data sheet, doc. no. UBX-15025564
[19] u-blox SARA-G3/SARA-U2 series system integration manual, doc. no. UBX-13000995
[20] u-blox SARA-N2/SARA-N3 series system integration manual, doc. no. UBX-17005143
[21] u-blox nested design application note, doc. no. UBX-16007243
[22] u-blox SARA-R4 series data sheet, doc. no. UBX-16024152
[23] u-blox SARA-N3 series data sheet, doc. no. UBX-18066692
[24] u-blox SARA-G4 series data sheet, doc. no. UBX-18006165
[25] u-blox SARA-R4 series system integration manual, doc. no. UBX-16029218
[26] u-blox SARA-G4 series system integration manual, doc. no. UBX-18046432
[27] u-blox AT commands manual, doc. no. UBX-13002752
[28] u-blox SARA-N2/SARA-N3 series AT commands manual, doc. no. UBX-16014887
[29] u-blox SARA-R4 series AT commands manual, doc. no. UBX-17003787

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	20-Dec-2019	fvid/psca/sses	Initial release
R02	10-Mar-2020	sses/fvid	Extended document applicability to SARA-R500S-00B Updated SARA-R510S-00B and SARA-R510M8S-00B product status Added regulatory certification approval info GPIO, power-on, power-off, reset sections updated Other minor corrections and clarifications
R03	26-Mar-2020	sses	Revised regulatory certification approval info Added antenna trace design used for SARA-R5 series modules' type approvals Other minor corrections and clarifications

Contact

For complete contact information, visit us at www.u-blox.com.

u-blox Offices

North, Central and South America

u-blox America, Inc.
Phone: +1 703 483 3180
E-mail: info_us@u-blox.com

Regional Office West Coast:
Phone: +1 408 573 3640
E-mail: info_us@u-blox.com

Technical Support:
Phone: +1 703 483 3185
E-mail: support@u-blox.com

Headquarters
Europe, Middle East, Africa

u-blox AG
Phone: +41 44 722 74 44
E-mail: info@u-blox.com
Support: support@u-blox.com

Asia, Australia, Pacific

u-blox Singapore Pte. Ltd.
Phone: +65 6734 3811
E-mail: info_ap@u-blox.com
Support: support_ap@u-blox.com

Regional Office Australia:
Phone: +61 2 8448 2016
E-mail: info_anz@u-blox.com
Support: support_ap@u-blox.com

Regional Office China (Beijing):
Phone: +86 10 68 133 545
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Chongqing):
Phone: +86 23 6815 1588
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shanghai):
Phone: +86 21 6090 4832
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office China (Shenzhen):
Phone: +86 755 8627 1083
E-mail: info_cn@u-blox.com
Support: support_cn@u-blox.com

Regional Office India:
Phone: +91 80 405 092 00
E-mail: info_in@u-blox.com
Support: support_in@u-blox.com

Regional Office Japan (Osaka):
Phone: +81 6 6941 3660
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Japan (Tokyo):
Phone: +81 3 5775 3850
E-mail: info_jp@u-blox.com
Support: support_jp@u-blox.com

Regional Office Korea:
Phone: +82 2 542 0861
E-mail: info_kr@u-blox.com
Support: support_kr@u-blox.com

Regional Office Taiwan:
Phone: +886 2 2657 1090
E-mail: info_tw@u-blox.com
Support: support_tw@u-blox.com