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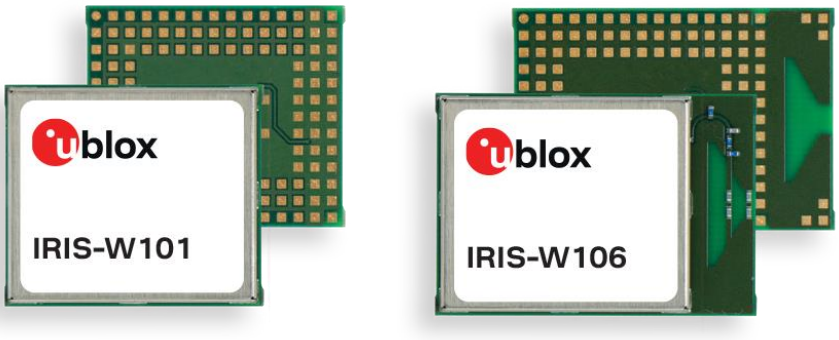
IRIS-W10 series

Stand-alone multi-radio module with dual band Wi-Fi 6, Bluetooth® Low Energy 5.3 or IEEE 802.15.4

System integration manual



Abstract

This manual provides a functional overview combined with best-practice design guidelines for integrating IRIS-W10 in customer applications. Targeted towards hardware and software engineers, the document describes the hardware design-in, software, component handling, regulatory compliance and testing of the module. It also includes a list of approved external antennas for use with the module. IRIS-W10 provides tri-radio Wi-Fi 6, Bluetooth® 5.3 low energy and 802.15.4. IRIS-W10 has an open CPU architecture with a powerful MCU for customer applications. The module series also includes variants with or without an internal antenna.

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This document applies to the following products:

Product name	**Document status**
IRIS-W101	Advance Information
IRIS-W106	Advance Information

☞ IRIS-W101 is under definition and all related information in this document is subject to change. For information about the related hardware, software, and status of listed product types, see also the data sheet [2].

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1 Product overview

IRIS-W10 series an ultra-compact module including NXP RW610/612 tri-radio Wireless MCU System-On-Chip (SoC). The module is intended for stand-alone products with the application SW running on the embedded Arm® Cortex®-M33 MCU.

IRIS-W10 supports Wi-Fi 6 IEEE 802.11a/b/g/n/ac/ax dual band 2.4 GHz and 5 GHz with 20 MHz channel width, Bluetooth Low Energy (LE) 5.3 / IEEE 802.15.4, and long-range PHY and isochronous channels for Bluetooth LE audio and Thread. IRIS-W10 also supports Matter over Wi-Fi, Thread*, and Ethernet connectivity. A Wi-Fi / Bluetooth coexistence protocol is also included.

IRIS-W10 modules are applicable for a wide range of different applications:

- Industrial automation
- Smart buildings and cities
- Smart devices
- Smart appliances
- Smart accessories
- Wireless-connected and configurable equipment
- Gateways

IRIS-W10 module series includes variants with an internal antenna or ANT pin for external antenna. Table 1 shows the ordering codes and antenna configurations for each module variant.

Ordering code	Antenna configuration	Antenna type
IRIS-W101-00B	ANT1: Bluetooth LE 5.3, or IEEE 802.15.4 and Wi-Fi dual band (2.4 GHz and 5 GHz), 8 MB flash	One antenna pin
IRIS-W106-00B	Bluetooth LE 5.3, or IEEE 802.15.4, and Wi-Fi dual band (2.4 GHz and 5 GHz), 8 MB flash	Internal PCB antenna
IRIS-W101-10B	ANT1: Bluetooth LE 5.3, or IEEE 802.15.4 and Wi-Fi dual band (2.4 GHz and 5 GHz), 16 MB flash	One antenna pin
IRIS-W106-10B	Bluetooth LE 5.3, or IEEE 802.15.4, and Wi-Fi dual band (2.4 GHz and 5 GHz), 16MB flash	Internal PCB antenna
IRIS-W101-30B*	ANT1: Bluetooth LE 5.3 and Wi-Fi dual band (2.4 GHz and 5 GHz), 8 MB flash	One antenna pin
IRIS-W106-30B*	Bluetooth LE 5.3 and Wi-Fi dual band (2.4 GHz and 5 GHz), 8 MB flash	Internal PCB antenna

Table 1: Module configurations ordering codes

☞ * IRIS-W10x-30B is without IEEE 802.15.4/Thread

Radio type approvals for Europe (RED), Great Britain, United States (FCC), Canada (ISED), and other country certifications (South Korea, Australia, New Zeeland, Japan, Taiwan, Brazil) are planned and currently pending.

1.1 Module Architecture

IRIS-W10 includes an Arm Cortex-M33 MCU @ 260 MHz with integrated 1.2MB SRAM and 8 MB eXecute-In-Place (XIP) Flash. It also includes subsystems for Wi-Fi 6, and Bluetooth LE/IEEE 802.15.4. An integrated Power management provides supply voltage to the internal power nodes and only a single external power supply is needed.

Wi-Fi and Bluetooth LE, RF front-end components configure the RF section for the different module variants. RF calibration data and MAC address are available in the IRIS-W10's OTP memory.

IRIS-W10 includes USB 2.0, SDIO 3.0, and RMII Ethernet interface. For connection to peripheral components serial communication interfaces, QSPI, I2C, USART, and I2S are available.

A display interface is available to connect an up to QVGA (320x240) resolution display.

1.1.1 Block diagram

The block diagram of the IRIS-W101 module is shown in Figure 1.

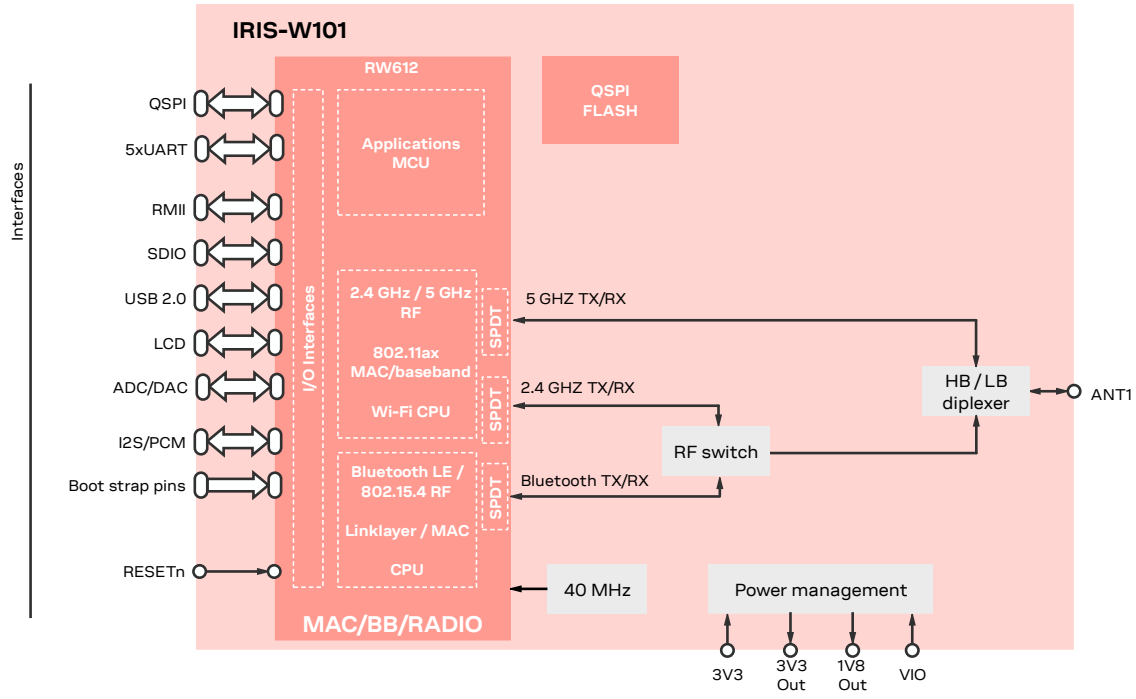


Figure 1: IRIS-W101 block diagram

The block diagram of the IRIS-W106 module is shown in Figure 2.

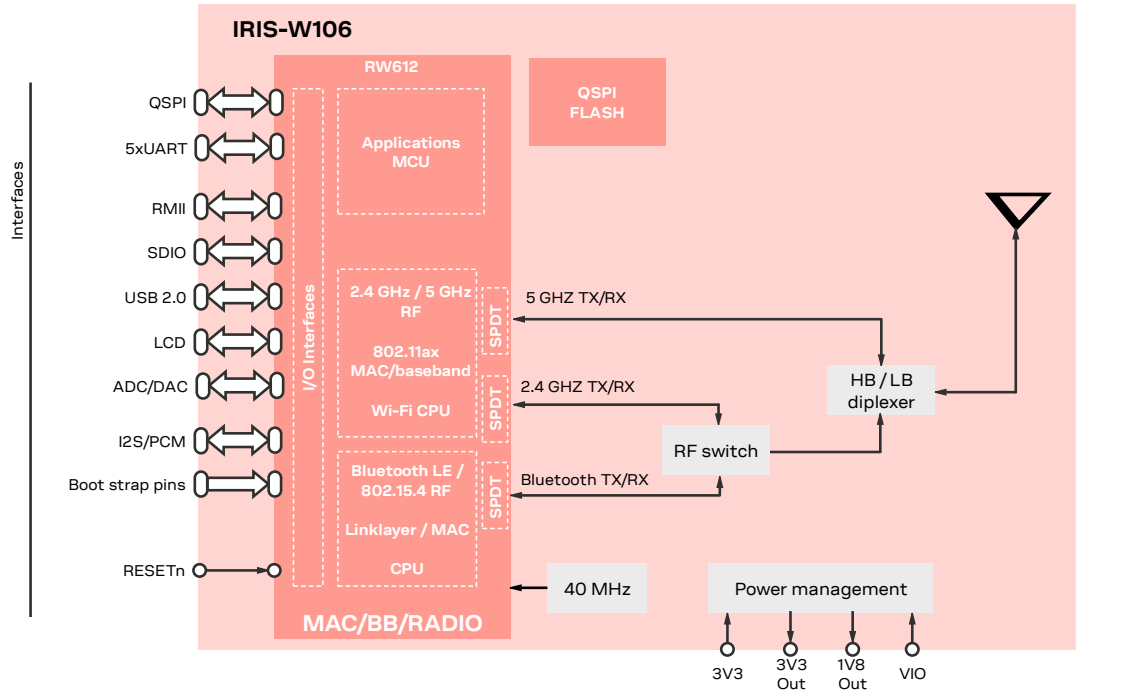


Figure 2: IRIS-W106 block diagram

1.2 Software options

IRIS-W10 module provides a software implementation with an open-CPU configuration.

- IRIS-W10 module includes a MCU host that enables customers to easily develop applications using the MCUXpresso SDK [17] in an open-CPU configuration right out of the box. This feature is also referred to as Open CPU.
- Additionally, the IRIS-W10 software can be programmed using various integrated Development Environments (IDE) that are supported by the MCUXpresso SDK [17]
  - MCUXpresso IDE [19]
  - IAR Embedded Workbench [22]
  - Arm GCC [23]

1.2.1 Open CPU

The Open CPU architecture of IRIS-W10 series module allows module integrators to build their own applications. Table 2 describes the possible connectivity and application support in recommended MCUXpresso SDK environments for IRIS-W10 hardware. See also Open CPU software.

Feature	Support
Development environment	MCUXpresso SDK (including basic example application)
Hardware interfaces	5 x universal serial interface modules (FlexComm, configurable as SPI/I2C/I2S/UART)
	1 x SDIO 3.0
	IEEE 1588 RMII/Fast Ethernet interface
	OTG (USB2.0)
	QVGA LED Support (8080 interface)
	16-bit ADC and 10-bit ADC
	32-bit General purpose timers/PWM
	4 x digital microphone support
Security	NXP EdgeLock™ Assurance
	Trusted execution environment (TEE) based on Arm TrustZone®-M
	Wi-Fi WPA2/WPA3 security
	OTP-based device configuration and life cycle management
	Cryptography accelerators (symmetric, asymmetric, secure hash, KDF)
	Bluetooth Low Energy secure connections

Table 2: Open CPU software support

See also Open CPU software.

2 Module integration

IRIS-W10 module is intended for stand-alone applications running on its embedded Arm Cortex-M33 MCU – implemented either with MCUXpresso or FreeRTOS . The module includes an on-chip 1.2 MB SRAM and an 8 MB eXecute-In-Place Flash. Memory expansion with up to 128 MB PSRAM is possible through the QSPI PSRAM interface.

Figure 3 shows the software architecture and implementation of software components for IRIS-W1.

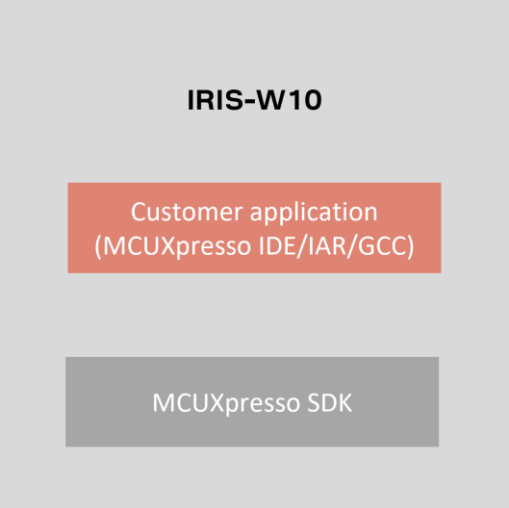


Figure 3: IRIS-W10 software structure

IRIS-W10 includes communication peripheral interfaces including USB 2.0 OTG, SDIO 3.0, RMII Ethernet, and Flexcomm serial communication interface.

The Flexcomm serial communication interfaces include SPI, UART, I2S, and I2C. Other interfaces, like GPIOs, DACs, ADCs, and a 32-bit general purpose timer/PWM, are also supported. These interfaces can be used to connect peripheral devices.

A display interface is available supporting QVGA resolution (320x240) with SPI and 8080 interfaces.

IRIS-W10's integrated power management circuitry requires just a single external 3.3 V supply. The IO voltage is set to either 1.8 V or 3.3 V by an external PCB pad connection.

The module is set in power down mode by asserting **PDn** pin. Other power save modes can be configured to optimize the application power consumption. Power-Down, Sleep, and Deep-Sleep modes can be activated by using the power API library from the SDK software package.

A 256 kB ROM memory is embedded on chip including among others secure boot loader and application programming interface, API. For further details see [2].

A 2 kB one-time programing OTP memory is included on chip containing factory calibration data and security parameters. The OTP can be used to configure boot options and store customer specific data parameters. For further details see [2].

2.1 Power supply interface

The power for IRIS-W10 modules is supplied through the **VCC** pin. IRIS-W10 use integrated DC/DC converters and LDO's to transform the supply voltage presented at the **VCC** pin to the internal power domains.

The VCC supply can be taken from any of the following sources:

- Switched Mode Power Supply (SMPS)

- Low Drop Out (LDO) regulator

It is important that any power source complies with specified voltage tolerances and can source the required peak currents.

When using IRIS-W10 with a battery, it is important that the chosen battery can handle the peak power of the module. In case of battery supply, consider adding extra capacitance on the supply line to avoid capacity degradation. For information about voltage supply requirement and current consumption see also IRIS-W10 data sheet [2].

2.1.1 Digital I/O interfaces reference voltage, VCCIO

IRIS-W10 I/O interface voltage is set to either 1.8 V or 3.3 V by connecting the **VCCIO** pin to the **+1V8** or **+3V3** pin.

To configure the interface voltage, VCCIO:

- Connect pin L6 to pin L7 for 1.8V
- Connect pin L6 to pin L8 for 3.3 V

2.2 Configuration pins

IRIS-W10 has seven boot configuration pins. For normal operation, the pins must have the correct settings during boot and power-up. Further details are available in the EVK-IRIS-W1 user guide [3].

Configuration bits	Pin name	Pin number	Description
CON[11]	RF_CNTL2 / CONFIG_DAP_USE_JTAG	B7	0: SWD 1: (Default): JTAG
CON[8]	RF_CNTL1 / CONFIG_DIS_KEY_ROT_DBG	A7	0: Enable key rotation, 1: (Default): Disable key rotation
CON[7]	RF_CNTL3 / CONFIG_VTOR_SEL	A8	0: address defined by software (hard coded value, 0x1300_0000) is multiplexed to CM33 VTOR 1: (Default): CM 33 hardware default boot address is multiplexed to CM33 VTOR (0x1303_0000)
CON[3,2,1,0]	EXT_FREQ, ECT_PRI, EXT_GNT, CEXT_REQ / CONFIG HOST BOOT [3..0]	M14, N14I, M12, N12	CONFIG HOST BOOT [3..0] table: 1111: (Default) boot from QSPI FLASH 1110: ISP boot 1101: Serial boot 1100: SDIO boot 1011: USB boot 1010: SPI EEPROM boot

Table 3: Boot strapping pins and options

2.3 Antenna interface

Figure 4 summarizes each of the available antenna options.

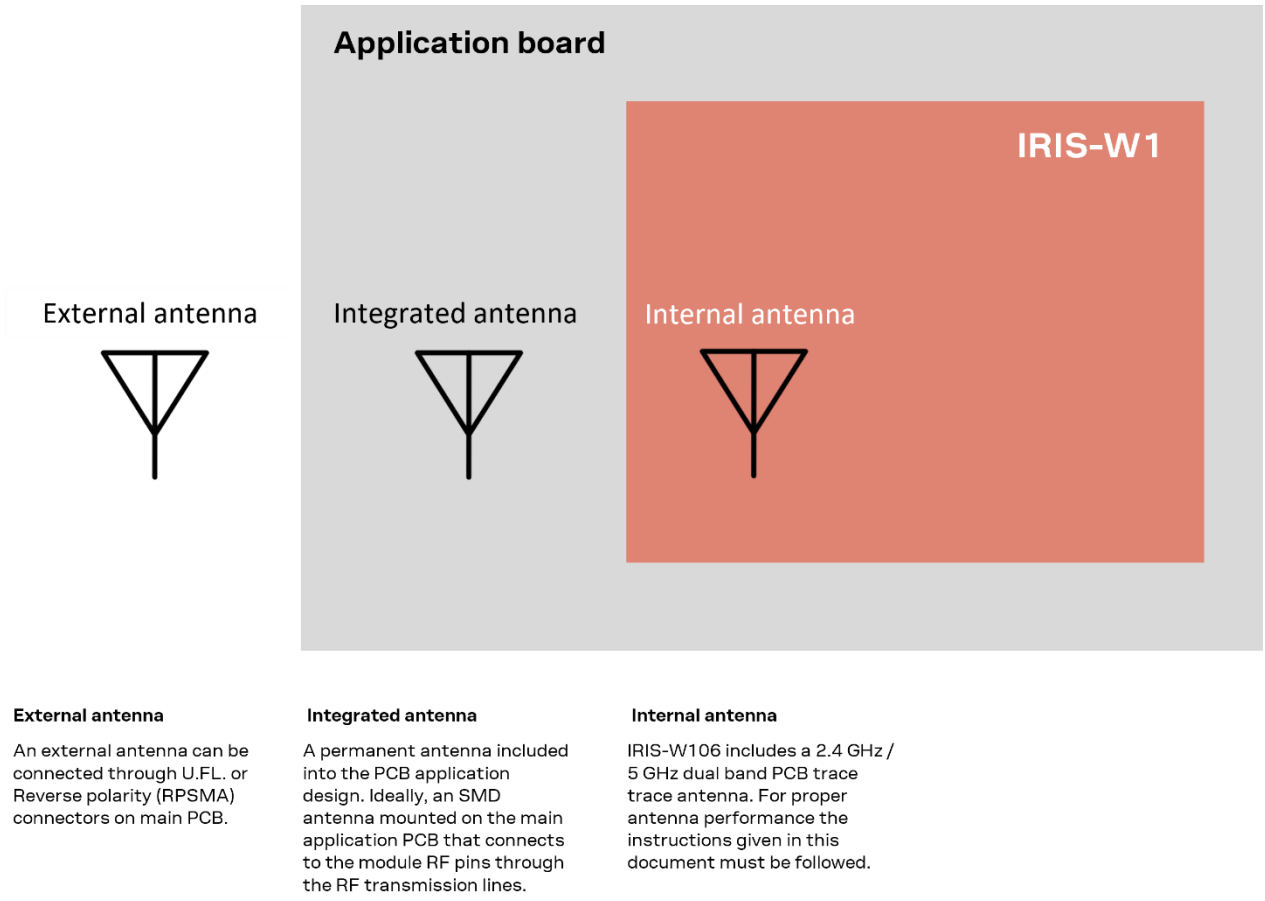


Figure 4: Antenna options

IRIS-W10 series modules are equipped either with an internal PCB trace antenna or RF pin.

- IRIS-W106 is equipped with an internal 2.4 and 5-6 GHz dual band Niche PCB trace antenna.
- IRIS-W101 supports an antenna pin to be used with either an integrated antenna placed on the main PCB or an external antenna that is connected through a coax cable to a U.FL or RP-SMA connector on the application PCB.

It is important to choose an antenna with optimal radiating characteristics for the best radio link stability and best throughput data rates. Use either IRIS-W106 with the internal antenna, or IRIS-W101 with integrated or external antenna connected to the main PCB through a 50 Ω transmission line or U.FL. connector and coaxial cable.

If a metal housing or any other limiting factor of the application product needs to be considered, it might be necessary to mount external antennas on the product housing.

☞ IRIS-W10 is pre-certified with the integrated antenna and with external antennas. To take advantage of this certification, the module must be integrated in strict accordance with the IRIS-W10 Antenna reference design. See also Pre-approved antennas.

☞ The module may be integrated with other antennas. In which case, the OEM installer must certify his design with respective regulatory agencies.

⚠ When integrating the u-blox reference design into an end-product, the application designer is solely responsible for any unintentional electromagnetic emission generated by the end-product.

⚠ Make sure the correct antenna impedance is connected to the RF port prior to power-on. Failing to do so may cause undesirable operation of the module.

2.3.1 Internal antenna (IRIS-W106)

For proper antenna performance observe the following design considerations.

- To enable good antenna radiation performance, it is important to place the module on the edge of the main PCB with the antenna facing outwards.
- A ground plane extending at least 10 mm on both sides of the module is recommended.
- Include a non-disruptive GND plane underneath the module with a clearance cut out underneath the antenna, as shown in Figure 5.
- Observe the antenna clearance shall be implemented on all layers.
- To avoid degradation of the antenna characteristics, don't place physically tall or large components closer than 10 mm to the module antenna.
- To avoid any adverse impact on antenna performance, include a 5 mm clearance between the antenna and the casing. Polycarbonate (PC) and Acrylonitrile butadiene styrene (ABS) materials have less impact on antenna performance than other types of thermoplastic.
- Include plenty of stitching vias from the module ground pins to the GND plane layer. Ensure that the impedance between the module pins and ground reference is minimal.
- Consider the end products use case and assembly to make sure that the antenna is not obstructed by any external item.

Figure 5 shows the PCB artwork on the main PCB top layer for IRIS-W106. It also shows the placement and GND clearance of the internal PCB trace antenna. An antenna clearance is only required for these module variants.

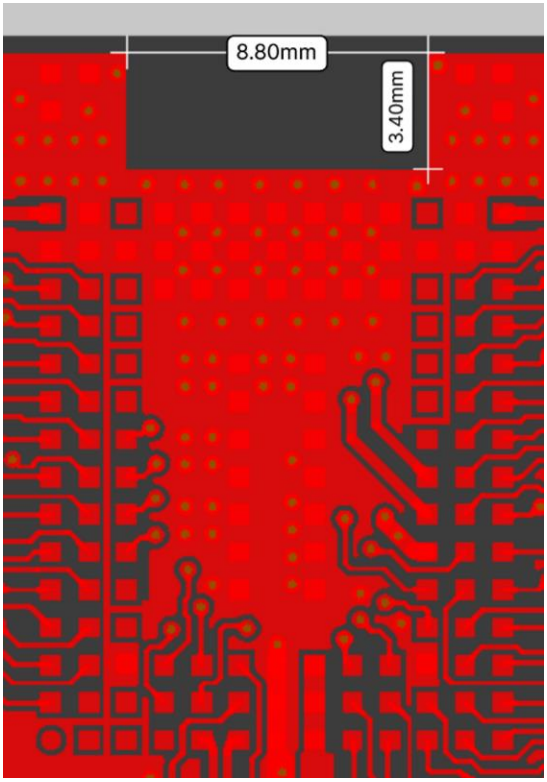


Figure 5: PCB artwork on main PCB top layer

2.3.2 Antenna reference design (IRIS-W101)

The module reference design is used for certification. To leverage u-blox FCC pre-certifiation, the application product must have an identical design to that of the module reference design.

Figure 6 and Figure 7 show layout of the microstrip from RF-1 respectively RF-2 to the corresponding U.FL.connector. The microstrip width is 0.38 mm or 15 mil. Note, RF-2 is not connected but reserved for future use.

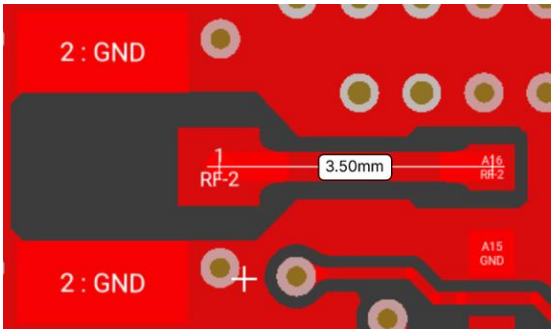


Figure 6: IRIS-W101 RF-2 microstrip implementation

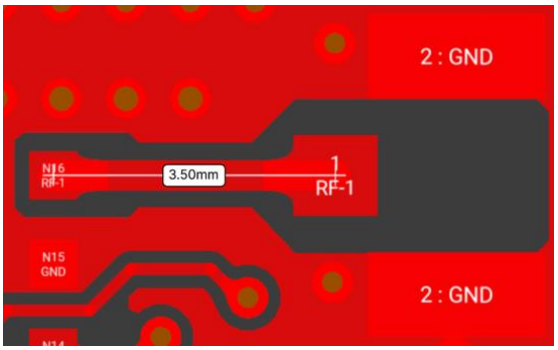


Figure 7: IRIS-W101 RF-1 microstrip implementation

Figure 8 show the stack-up of the PCB reference board. Layer L2 is used for reference GND.

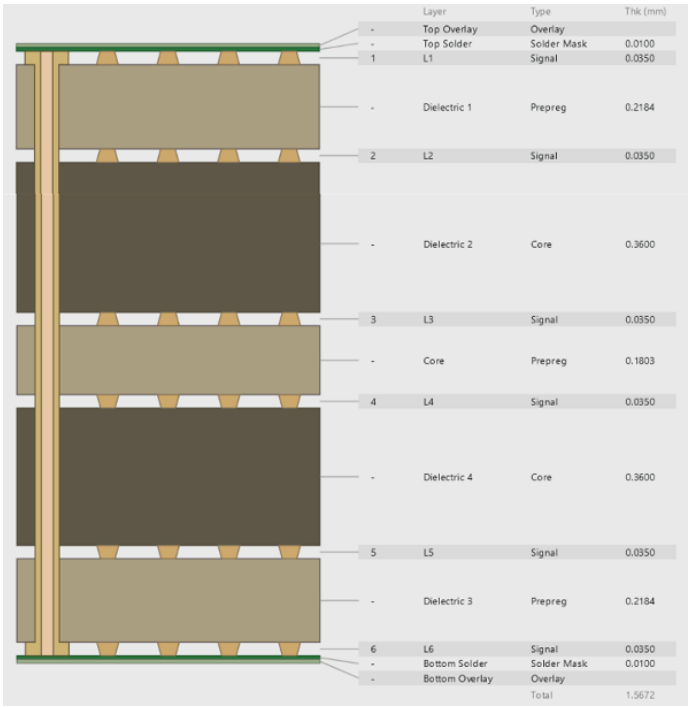


Figure 8: IRIS-W1 reference design PCB stack-up

2.4 Module reset

IRIS-W10 series module is reset and set in Power-down mode by applying a low level on the **PDn** input pin. A low logic level on this pin initiates an "external" or "hardware" reset of the module. The prevailing parameter settings at the time of the reset are not saved in the non-volatile memory of the module and a proper Wi-Fi and Bluetooth LE network detach is not performed. **PDn** must be set high for normal operation. **PDn** has an always-on internal weak pull down.

Item	Parameter	Min	Typ	Max	Unit
T_{PU_RESET}	Delay from power on to de-assert PDn	0	-	-	ms
T_{RPW}	Pulse width	60	-	-	us
V_{IH}	Input high voltage	1.4	-	4.5	V
V_{IL}	Input low voltage	-0.4	-	0.5	V

Table 5. PDn pulse characteristics

2.5 Low power clock

IRIS-W10 uses a 32.768 kHz low power clock to enable different power modes. For further information about power modes, see also the IRIS-W10 data sheet [2].

The clock can be generated from either of the following internal or external clock sources:

- Internal oscillator
- External clock source, TCXO

To get the lowest possible current consumption from the module in sleep mode, an external TCXO is needed. If an external clock source is not connected, the internal, less accurate, oscillator is used.

2.5.1 External clock source, TCXO

Table 4 shows the applicable requirements for an external 32 kHz crystal oscillator. Input for LPO clock is multiplexed with RMII signals.

Parameter	Min	Typ	Max	Unit
Clock frequency range accuracy CMOS input clock signal type +/-250 ppm (initial, aging, temperature)	-	32.768	-	kHz
Phase noise requirement @ 100 kHz	60	-125	-	dBc/Hz
Cycle jitter	-	1.5	-	ns (RMS)
Slew rate limit (10-90%)	-	-	100	ns
Duty cycle tolerance	20	-	80	%

Table 4: TCXO crystal oscillator requirements

2.6 Communication interfaces

The application product can be designed to connect to a communication device either through USB, RMII (Ethernet), or SDIO interface:

- 1 x 100 Mbit Ethernet RMII
- 1 × High speed USB 2.0 OTG (480Mbit/s)
- 1 × SDIO 3.0 host interfaces with 50 MHz maximum clock frequency
- FlexSPI Flash interface connected to the internal flash (mounted on IRIS-W1)
- FlexSPI pSRAM interface with 160 MHz maximum clock frequency

Either of these interfaces can source and receive data from wireless communication systems.

2.6.1 USB 2.0

IRIS-W10 includes a USB 2.0 UTMI+ level 3 PHY handling the low-level USB 2.0 protocol and signaling.

The USB 2.0 supports:

- 480 Mbps HS mode
- 12 Mbps FS mode
- 1.5 Mbps LS mode

The USB electrical specification is described in IRIS-W10 data sheet [4].

Name	I/O	Description	Remarks
USB_VBUS	I/O		
USB_DP	I/O		
USB_DM	I/O		
USB_ID	I		

Table 5: USB Interface signals

2.6.2 RMII

The MAC/NET core includes a 10/100 MAC, with layer 3 network acceleration. It supports all IEEE 1588 features and implements the full 802.3 specification.

IRIS-W10 includes a seamless 2-bit Reduced MII ethernet interface operating at 50 MHz intended to connect an external PHY.

The RMII interface requires an external 50 MHz clock source either from a compatible PHY chip or from an external oscillator.

Table 6 shows the signals to use when connecting an external PHY.

Signal	Description	Comment	Direction	MUX
CLK	50 MHz clock			GPIO[25]
TxD0	Bit 0 of ethernet transmit data		MAC to PHY	GPIO[58]
TxD1	Bit 1 of ethernet transmit data		MAC to PHY	GPIO[59]
TxEN	Ethernet transmit mode enable		MAC to PHY	GPIO[60]
RxD0	Bit 0 of ethernet receive data		PHY to MAC	GPIO[22]
RxD1	Bit 1 of ethernet receive data		PHY to MAC	GPIO[23]
CRSVD	Carrier sense and receive data valid		PHY to MAC	GPIO[62]
MDIO	Ethernet controller data input / output management		Bidirectional	GPIO[57]
MDC	Ethernet controller data clock		MAC to PHY	GPIO[56]
RxERR	Receive error		PHY to MAC	GPIO[63]

Table 6 : RMII interface signals

2.6.3 SDIO 3.0

IRIS-W10 series modules include a SDIO device interface that is compatible with the industry standard SDIO 3.0 specification (UHS-I, up to 104 Mbyte/s). It allows a controller using the SDIO bus protocol to access Wi-Fi and Bluetooth LE functions. The module also supports legacy modes, such as default speed and High-Speed modes.

IRIS-W10 acts as a device on the SDIO bus. Table 7 shows the supported bus speed modes.

Bus speed mode	Max. bus speed [MB/s]	Max. clock frequency [MHz]	Signal voltage [V]
SDR104	104	208	1.8
SDR50	50	100	1.8
DDR50	50	50	1.8
SDR25	25	50	1.8
SDR12	12.5	25	1.8
High Speed	25	50	3.3
Default Speed	12.5	25	3.3

Table 7: SDIO supported rates for IRIS-W1

Pull-up resistors are required for all SDIO data lines and the command line. Termination resistors in series to the traces might also be needed. This to improve signal integrity or reduce EMC radiation. See also Data communication interfaces.

Name	I/O	Description	Remarks
SD_CLK	I	SDIO Clock input	
SD_CMD	I/O	SDIO Command line	Pull-up resistor is required
SD_D0	I/O	SDIO Data line bit [0]	Pull-up resistor is required
SD_D1	I/O	SDIO Data line bit [1]	Pull-up resistor is required
SD_D2	I/O	SDIO Data line bit [2]	Pull-up resistor is required
SD_D3	I/O	SDIO Data line bit [3]	Pull-up resistor is required

Table 8: SDIO signal definition

The SDIO host interface pins of the module are powered by the **VIO** voltage domain.

2.7 Serial interfaces

Peripheral devices can connect to IRIS-W10 through any of the Flexcomm serial communication interfaces: SPI, USART, I2S, and I2C, and any of the supported GPIOs, DACs, ADCs, and 32-bit general purpose timer/PWM.

- Up to five configurable (Flexcomm) universal serial interfaces are independently configured for:
  - UART with maximum 6.25 Mbit/s speed (excluding delays introduced by external device)
  - USART with maximum 20 Mbit/s speed (excluding delays introduced by external device)
  - SPI with maximum 30Mbit/s speed (excluding delays introduced by external device)
  - I2C, with maximum 1 Mbit/s speed (supporting high-speed target mode up to 3.4 Mbit/s)

2.7.1 Serial peripheral interface (SPI)

The IRIS-W10 SPI interface supports Main and Sub modes with up to four Main selects. The module supported bitrates up to 30 Mbps.

IRIS-W10 series supports QSPI interface for use with an external PSRAM memory. The interfaces are supplied from the VIO power domain.

Name	I/O	Description	Remarks	Pin
RCCLK		Clock		A2
RCE		Chip enable		A5
RDQS		Strobe		D3
RD0		Data 0		B4
RD1		Data 1		A4
RD2		Data 2		B3
RD3		Data 3		A3

Table 9: External RAM QSPI interface

2.7.2 Universal synchronous asynchronous serial interface (USART)

IRIS-W10 series modules provide four USART Universal Synchronous / Asynchronous Serial Interface (USART) for data communication, FC0, FC2, FC3, and FC14.

FC14 is multiplexed with the RMII interface.

FC2 and FC3 are multiplexed with the SDIO interface.

Signal	FC0	FC2	FC3	FC14
RXD	M10	A6	B9	L1
TXD	N10	B5	A10	L2
CTS	M11	A7	A9	N3
RTS	N9	B7	B8	L4
SCK	M9	A8		N2

Table 10: USART data communication, FC0, FC2, FC3, and FC14

The following UART signals are available:

- Data lines (**RXD** as input, **TXD** as output)
- Hardware flow control lines (**CTS** as input, **RTS** as output)
- **SCK** synchronous clock

The maximum bit rate in asynchronous mode is 6.25 Mbit/s and 20 Mbit/s in synchronous mode.

For more information about the UART interface characteristics, see also the IRIS-W10 data sheet [2].

Interface	Default configuration
COM port	115200 baud, 8 data bits, no parity, 1 stop bit, hardware flow control

Table 11: Default settings for the COM port while using u-connectXpress software

It is advisable to make the UART available as either test points or made available through a connected header for software upgrade.

2.7.3 I2C interface

The Inter-Integrated Circuit (I2C) interfaces can be used to transfer or receive data on a 2-wire bus network. The IRIS-W10 series contains up to two I2C bus interfaces and can operate as both Main and Sub modes using both standard (100 kbps) and fast (400 kbps) transmission speeds. The interface uses the **SCL** signal to clock instructions and data on the **SDA** signal.

External pull up resistors are required for the I2C interface. The value of the pull-up resistor should be selected depending on the speed and capacitance of the bus.

2.7.4 I2S interface

To connect to external audio codec or other audio circuitry, configure an I2S audio interface. An I2S interface includes Clock (**SCK)**, Word select (**WS)**, and Serial Data (**SD)**.

2.8 GPIO pins

IRIS-W10 series IRIS-W10 provides up to 64 GPIO's, which can be configured as general-purpose input or output. You can use two GPIOs for digital-to-analog conversion (DAC) and eight for analog-to-digital conversion (ADC) with common trigger and voltage reference pins.

Configure up to eight GPIOs for use as an analog comparator, as described in Table 12.

- 64 programmable GPIOs
  - Eight 16-bit ADC
  - Two 10-bit DAC
  - 32-bit general purpose timers/PWM

Function	Description		Configurable GPIOs
General purpose input	Digital input with configurable edge detection and interrupt generation.		Any
General purpose output	Digital output with configurable drive strength, pull-up, pull-down, open-source, open-drain and/or slew rate.		Any
Pin disabled	Pin is disconnected from input buffers and output drivers.	All*	Any
Timer/ counter	High precision time measurement between two pulses/ Pulse counting with interrupt/event generation.		Any
Interrupt/ Event trigger	Interrupt/event trigger to the software application/ Wake up event.		Any
ADC input	12/14/16-bit analog to digital converter		Any analog
Analog comparator input	Compare two voltages, capable of generating wake-up events and interrupts		Any analog
PWM output	Output complex pulse width modulation waveforms		Any

* = If left unconfigured ** = If using u-connectXpress software. For pin number, see also the IRIS-W10 data sheet **[2]**.

Table 12: GPIO custom functions configuration

2.9 JTAG and SWD Debug interface

IRIS-W10 modules support both Serial Wire debug (SWD) and JTAG debug (software download), see EVK-IRIS-W10 User guide [3].

When designing an application product with IRIS-W1, the SWD interface pins to the module (**SWDCLK**, **SWDIO**) and JTAG pins (**JTAG_TCK**, **JTAG_TDI**, **JTAG_TDO**, **JTAG_TMS**, **JTAG_TRSTn**) should ideally be made accessible in the application design.

Flash IRIS-W10 over the UART or SWD interface. The module is preloaded with bootloader software, which is without security. A debug connector to the module is also useful for software development.

For security reasons, disable the debug interface to prevent the upload or download of insecure software – or software that has not been validated.

2.10 Integrated thermal management

RW612 includes an integrated thermal management engine.

2.11 Reserved pins (RSVD, aux)

Don't connect any reserved (**RSVD**) pins. The reserved pins can be allocated for future interfaces and functionality.

3 Design-in

3.1 Overview

All application circuits must be properly designed, but several points require special attention during the application design. In an order of importance::

- Select appropriate antenna type and part.
- Follow the schematic and layout reference design recommendations provided in this document. Antenna circuit affects the RF compliance of the device integrating the module with applicable certification schemes.
- Select appropriate power supply source and bypass capacitors and carefully route the power supply nets or planes.
- Follow the schematic and layout design recommendations for Supply interfaces. The power supply circuit might impact the performance of the module.
- Analog signals are sensitive to noise, route analog signals away from high frequency signals.
- For correct schematic and layout design, follow the Universal asynchronous serial interface (UART) and General layout guidelines. High speed interfaces can become a source of noise, which affects compliance with regulatory standards for radiated emissions.
- Utilize the system functions, available through **PDn** and configuration pins, in the application design. These functions ensure that the voltage level is correctly defined during module boot, so it is important to follow the pin recommendations given in the General high-speed layout guidelines. Other pins also require an accurate design to ensure proper functionality.
- Make sure not to exceed the electrical specification for any pin.

3.2 RF interface options

IRIS-W10 modules offer several RF interface options for connecting external antennas:

- IRIS- W101
  - IRIS-W101 includes a single RF pin for connecting external antennas:
    - **ANT1** for Wi-Fi 2.4 and 5 GHz operation and Bluetooth LE connectivity
    - **ANT2** is not connected (NC)
  - The **RF** pin has a nominal characteristic impedance of 50 Ω. For correct impedance matching, this port must connect to the antenna through a 50 Ω characteristic impedance transmission line – depending on the type of module connector. Poor termination of **RF** pins can result in degraded performance of the module.
  - Follow the requirements described in in Table 13 and Table 14 to optimize the isolation between the antennas and ensure good application performance.
- IRIS-W106
  - IRIS-W106 includes an embedded antenna for dual band Wi-Fi and Bluetooth LE/IEEE 802.15.4 operation, which for optimal performance requires the module to be placed on the edge of the host PCB with the “antenna side” closest to the edge.

⚠ According to FCC regulations, the transmission line (from the module antenna pin to the physical antenna or antenna connector on the host PCB) is considered part of the approved antenna design. Therefore, module integrators must use the antenna reference design used in the module FCC type approval exactly or certify their own design.

To design circuits that comply with these requirements, see also Antenna interfaces.

3.2.1 Antenna design

To optimize the radiated performance of the final product, the selection and placement of both the module and antenna must be chosen with due regard to the mechanical structure and electrical design of the product. To avoid later redesigns, it is important to decide the positioning of these components at an early phase of the product design.

The compliance and subsequent certification of the RF design depends heavily on the radiating performance of the antennas.

To ensure that the RF certification of IRIS-W10 modules is extended through to the application design, carefully follow the guidelines outlined below.

- External antennas, including, linear monopole classes:
  - Place the module and antenna in any convenient area on the board. External antennas don't impose any restriction on where the module is placed on the PCB.
  - Select antennas with an optimal radiating performance in the operating bands. The radiation performance depends mainly on the antennas.
  - Choose RF cables that offer minimum insertion loss. Unnecessary insertion loss is introduced by low quality or long cables. Large insertion losses reduce radiation performance.
  - Use a high-quality 50 Ω coaxial connector for proper PCB-to-RF cable transition.
- Integrated antennas, such as patch-like antennas:
  - Internal integrated antennas impose some physical restrictions on the PCB design:
    - Integrated antennas excite RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna; its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane related to the antenna element must be considered.
    - Find a numerical example to estimate the physical restrictions on a PCB, where: Frequency = 2.4 GHz → Wavelength = 12.5 cm → Quarter wavelength = 3.5 cm in free space or 1.5 cm on a FR4 substrate PCB.
- Choose antennas with optimal radiating performance in the operating bands. Radiation performance depends on the complete product and antenna system design, including the mechanical design and usage of the product. Table 13 summarizes the requirements for the antenna RF interface.
- Make the RF isolation between the system antennas as high as possible, and make the correlation between the 3D radiation patterns of the two antennas as low as possible. In general, an RF separation of at least a quarter wavelength between the two antennas is required to achieve a minimum isolation and low pattern correlation. If possible, increase the separation to maximize the performance and fulfill the requirements in Table 13.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the antenna pins.
Frequency Range	2400 - 2500 MHz 5150 - 5850 MHz	For 802.11b/g/n/ax and Bluetooth LE. For 802.11a/n/ac/ax.
Return Loss	S11 < -10 dB (VSWR < 2:1) recommended S11 < -6 dB (VSWR < 3:1) acceptable	The Return loss or S_{11} S parameter (normally represented on vector network analyzers) in the voltage standing-wave ratio (VSWR) refers to reflected power. This loss is a measurement of how well the primary RF antenna connection matches the 50 Ω characteristic impedance of the antenna pins.

Item	Requirements	Remarks
		To maximize the amount of power transferred to the antenna, the impedance of the antenna termination must match (as far as possible) the 50 Ω nominal impedance of antenna pins over the operating frequency range,.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	Radiation efficiency is the ratio of the radiated power to the power fed to the antenna input. This is a measurement of how well an antenna receives or transmits data.
Maximum Gain		To comply with regulatory agencies radiation exposure limits, the maximum antenna gain must not exceed the value specified in Antennas for equivalent antenna type.

Table 13: Summary of antenna interface requirements

Table 14 specifies additional requirements for implementing a dual antenna design.

Item	Requirements	Remarks
Isolation (in-band)	S21 > 30 dB recommended	The antenna-to-antenna isolation is the S21 parameter between the two antennas in the band of operation. Lower isolation might be acceptable depending on use-case scenario and performance requirements.
Isolation (out-of-band)	S21 > 35 dB recommended S21 > 30 dB acceptable	Out-of-band isolation is evaluated in the band of the aggressor. This ensures that the transmitting signal from the other radio is sufficiently attenuated by the receiving antenna. It also avoids any saturation and intermodulation effect on the receiver port.

Table 14: Summary of Wi-Fi/Bluetooth coexistence requirements

Select antennas that provide:

- Optimal return loss (or VSWR) over all the operating frequencies
- Optimal efficiency figure over all the operating frequencies
- An appropriate gain that does not exceed the regulatory limits specified in some regulatory country authorities like the FCC in the United States.

A useful approach for the antenna microstrip design is to place an U.FL connector close to the embedded PCB or chip antenna. The U.FL connector only needs to be mounted on units used for verification.

3.2.1.1 Integrated antenna design

If integrated antennas are used, the transmission line is terminated by the antennas themselves or by the antenna together with the connected coaxial cable and U.FL connector.

Consider the following the guidelines when designing the antenna:

- The antenna design process should commence at the same time as the mechanical design of the product. PCB mock-ups are useful in estimating overall efficiency and radiation path of the intended design during early development stages.
- Use antenna manufacturer designs that provide the best possible return loss (or VSWR).
- Provide a ground plane large enough to meet the related integrated antenna requirements. The ground plane of the application PCB may be reduced to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. The overall antenna efficiency may benefit from larger ground planes.
- Proper placement of the antenna and its surroundings is also critical for antenna performance. Avoid placing the antenna close to conductive or RF-absorbing parts, such as metal objects or ferrite sheets, as these may absorb part of the radiated power, shift the resonant antenna frequency of the antenna, or otherwise affect the antenna radiation pattern.

- Ensure that correct the installation and deployment of the antenna system, including PCB layout and matching circuitry, is done correctly. Strictly follow the specific guidelines provided by the antenna manufacturer.
- Further to the custom PCB and product restrictions, antennas can also require some tuning/matching to reach the target performance. Plan the measurement and validation activities with the antenna manufacturer before releasing the end-product to manufacturing.
- The receiver section can be affected by noise sources like hi-speed digital busses. Avoid placing the antenna close to busses as DDR. Otherwise, consider taking specific countermeasures, like metal shields or ferrite sheets, to reduce the interference.

Be aware of interaction between co-located RF systems, like LTE sidebands on 2.4 GHz band. Transmitted power can interact or disturb the performance of IRIS-W1 modules in instances where a specific LTE filter isn't included.

3.2.2 RF transmission line design

RF transmission lines, such as those that connect from the RF pin to the antenna or antenna connector, must be designed with a characteristic impedance of 50 Ω.

Figure 9 shows the design options for implementing a transmission line, namely:

- Microstrip – track separated with dielectric material and coupled to a single ground plane.
- Coplanar microstrip – track separated with dielectric material and coupled to both the ground plane and side conductor. A coplanar microstrip is the most common configuration for a printed circuit board (PCB).
- Stripline – track separated by dielectric material and sandwiched between two parallel ground planes.

In Figure 9, the parameters shown in the cross-sectional area of each trace design include:

- Width (W) – shows the width of the transmission line.
- Distance (S) – shows the distance between the coplanar transmission line and the adjacent GND on the top layer.
- Dielectric substrate thickness (H, H1, and H2) – shows the dielectric layer thickness.
- Thickness of the copper layer (T) – can also be represented by "Base Copper Weight", which is commonly used as the parameter for PCB stack-up.
- Dielectric constant (ε_r) is defined as the ratio between the electric permeability of the PCB substrate against the electric permeability of free space.

☞ The width of a 50 Ω microstrip depends on "ε_r" and "H", which must be calculated for each PCB layer stack-up and dielectric substrate that is used.

Figure 9 shows the cross-sectional area of each trace design.

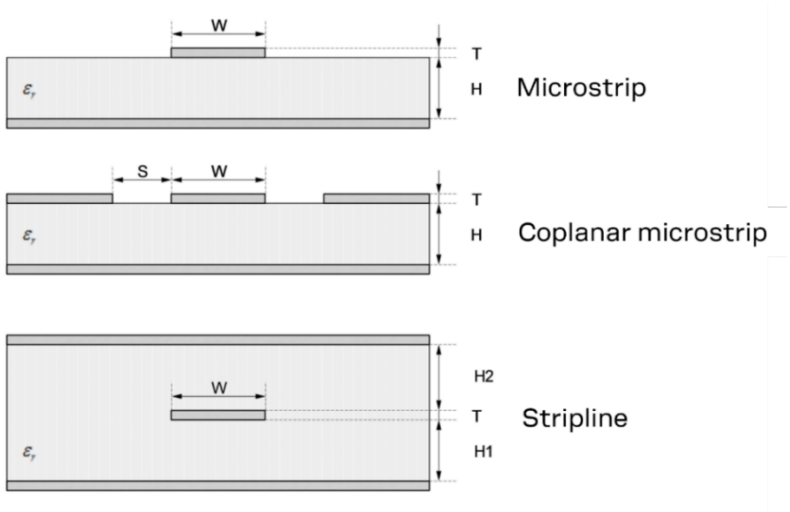


Figure 9: Transmission line trace design

Follow these recommendations to design a 50 Ω transmission line correctly:

- Designers must provide enough clearance from surrounding traces and ground in the same layer. In general, the trace to ground clearance should be at least twice that of the trace width. The transmission line should also be "guarded" by the ground plane area on each side.
- In the first iteration, calculate the characteristic impedance using tools provided by the layout software. Ask the PCB manufacturer to provide the final values usually calculated using dedicated software and production stack-ups. It is sometimes possible to request an impedance test coupon on side of the panel to measure the real impedance of the traces.
- Although FR-4 dielectric material can result in high losses at high frequencies, it can still be an appropriate choice for RF designs. In which case, aim to:
  - Minimize RF trace lengths to reduce dielectric losses.
  - If traces longer than few centimeters are needed, use a coaxial connector and cable to reduce losses.
  - For good impedance control over the PCB manufacturing process, design the stack-up with wide 50 Ω traces with width of at least 200 µm.
  - To make the trace less lossy and to have better impedance control, the trace shall be made wide. This is achieved by clearing copper in the inner layers closest under the trace, which increases the distance to reference GND.
  - Contact the PCB manufacturer for specific tolerance of controlled impedance traces. FR-4 materials exhibit poor thickness stability and offer less control of impedance over the trace width.
- For PCBs with components larger than 0402 and dielectric thickness below 200 µm, add a keep-out area; that is, some clearance (void area) on the ground reference layer below any pin on the RF transmission lines. This helps to reduce the parasitic capacitance to ground.
- Route RF traces with smooth shapes try not to exceed 45 ° bends and avoid acute angles. The transmission lines width and spacing to GND must be uniform.
- Add GND stitching vias around transmission lines.
- Provide a sufficient number of vias on the adjacent metal layer. Include a solid metal connection between the adjacent metal layer on the PCB stack-up to the main ground layer.
- To avoid crosstalk between RF traces and Hi-impedance or analog signals, route RF transmission lines as far from noise sources (like switching supplies and digital lines) and any other sensitive circuit.

- Avoid stubs on the transmission lines. Any component on the transmission line should be placed with the connected pin located over the trace. Also avoid any unnecessary components on RF traces.

3.2.3 RF connector design

If an external antenna is required, the designer should consider using a proper RF connector. The designer must verify the compatibility between plugs and receptacles used in the design.

Based on the declarations of the respective manufacturers, Table 15 suggests some RF connector plugs that can be used by designers to connect RF coaxial cables.

Manufacturer	Series	Remarks
Hirose	U.FL® Ultra Small Surface Mount Coaxial Connector	Recommended
I-PEX	MHF® Micro Coaxial Connector	
Tyco	UMCC® Ultra-Miniature Coax Connector	
Amphenol RF	AMC® Amphenol Micro Coaxial	
Lighthorse Technologies, Inc.	IPX ultra micro-miniature RF connector	

Table 15: U.FL compatible plug connector

The Hirose U.FL-R-SMT RF receptacles (or similar parts) require a suitably mated RF plug from the same connector series. Due to wide usage of this connector, several manufacturers offer compatible equivalents. The RF plug is normally available as a cable assembly. Different types of cable assembly are available; the user should select the cable assembly best suited to the application.

The key characteristics of the cable assembly include:

- RF plug type: select U.FL or equivalent
- Nominal impedance: 50 Ω
- Cable thickness: Typically, 0.8 mm to 1.37 mm. Select thicker cables to minimize insertion loss.
- Cable length: Standard length is typically 100 mm or 200 mm; custom lengths may be available on request. Select shorter cables to minimize insertion loss.
- RF connector on the other side of the cable, For example, another U.FL (for board-to-board connection) or SMA (for panel mounting)

Note that SMT connectors are typically rated for a limited number of insertion cycles. In addition, the RF coaxial cable may be relatively fragile compared to other types of cables. To increase application ruggedness, connect U.FL connector to a more robust connector such as a sub-miniature A (SMA) connector fixed to the panel.

☞ A de-facto standard for SMA connectors suggests that the use of reverse polarity connectors (RP-SMA) on Wi-Fi and Bluetooth end products can deter end users from replacing the antenna with higher gain types that exceed regulatory limits.

Observe the following recommendations for a proper layout of the connector:

- Strictly follow the connector layout recommended by the manufacturer.
- SMA Pin-Through-Hole (PTH) connectors require GND keep-out (void clearance) areas on all layers around the central pin – up to the annular pads of the four GND posts.
- U.FL surface mounted connectors require non-conductive traces. Include a void clearance area between the GND land pads below the connector.
- If the RF pad size of the connector is wider than the microstrip, remove the GND layer beneath the RF connector to minimize the stray capacitance and retain a 50 Ω RF line resistance. To reduce the parasitic capacitance to ground for example, the active pad of the UF.L connector must include, at the very least, a GND keep-out (void clearance area) on the first inner layer.

Figure 10 shows a proper layout example for a U.FL connector.

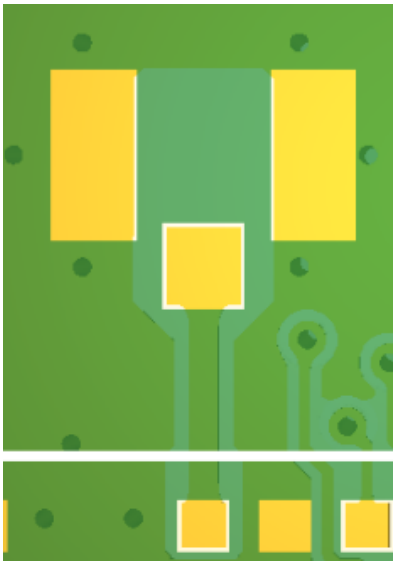


Figure 10: U.FL connector layout example

3.3 Supply interfaces

3.3.1 Module supply design

Although the GND pins are internally connected, it is advisable to connect all available ground pins on the application board to solid ground with a good (low impedance) connection to external ground. This minimizes power loss, improves RF performance, and betters thermal performance.

Good connection of the module supply pins, supplied by a DC supply source, is required for accurate RF performance.

Consider the following guidelines when developing the schematic:

- All power supply pins must be connected to an appropriate DC source.
- Any series component with an Equivalent Series Resistance (ESR) greater than a few mΩ should be avoided. The only exception to this general rule is the use of ferrite beads for DC filtering. To avoid possible instability in the DC supply, only use ferrite beads if needed.
- For high-frequency filtering, additional bypass capacitors in the range of 100 nF to 1 µF are required on all supply pins. Offering low ESR/ESL resistance, a class II ceramic capacitor with an X7R or X5R dielectric is well suited for this purpose. Bypass capacitors of a smaller size can be chosen to minimize ESL (Equivalent Series Inductance) in the manufacturing process. The capacitor should be placed as close as possible to the module supply pin.
  To help filter current spikes from the RF section and avoid ground bounce, a minimum bulk capacitance of 10 µF should be applied to the VCC rail and placed close to the module supply pins. Offering low ESR/ESL resistance, a class II ceramic capacitor with an X7R or X5R dielectric is well suited for this purpose. Special care should be taken in the selection of X5R/X7R dielectrics due to capacitance derating versus DC bias voltage.

3.3.2 VCC application circuits

VCC application circuits designed with a switched mode power supply (SMPS) makes for ideal choice when the available primary supply source has a more than moderately higher voltage than the operating supply of the module. An SMPS provides the best power efficiency for the overall application and minimizes the current drawn from the main supply source. Customers are advised to perform power and thermal budgets to find the solution that is best suited for their full application.

⚠ When using an SMPS, ensure that AC voltage ripple at switching frequency is kept as low as possible. Layout the design to minimize impact of high frequency ringing.

VCC application circuits designed with a linear, low drop-out (LDO) regulator makes for a convenient main supply with a relatively low voltage, where the typical 85-90% efficiency of the switching regulator only provides minimal current saving. As linear regulators dissipate a considerable amount of energy, LDOs are not recommended for stepping-down high voltages. The benefit of an LDO source over SMPS is that an LDO is simpler to integrate and does not generate switching noise. However, with a larger voltage difference the superior efficiency of an SMPS converter dissipates less heat and a significantly longer operating time than that of battery-powered products.

The overall DC/DC efficiency of an SMPS depends on the current consumption during the active and idle states of the specific application. Although some DC/DC converters provide high efficiency with extremely light loads, their efficiency typically worsens when idle current drops below a few milliamps and reduces the battery life.

As a contingency against “latch up”, include an over-current limiter to protect the module from electrical over stress (EOS). An LDO or SMPS serves this purpose.

3.3.2.1 Battery

In battery-powered devices ensure that the battery capacity matches the application. Battery-powered devices also deliver the peak current required by the module.

For further information about current consumption and other performance data, see also the electrical specifications provided in the data sheet [2].

3.4 GND pins

Good connection of the module GND pins, with a solid ground layer on the main PCB, is required for module stability and correct RF performance. A good ground connection significantly reduces EMC issues and provides a thermal heat sink for the module.

3.5 Data communication interfaces

3.5.1 SDIO 3.0

The design of the SDIO 3.0 bus demands special attention to meet signal integrity requirements and minimize electromagnetic interference (EMI) issues. Route these signals with a single ended impedance of 50 Ω.

Route all signals in the bus with the same length and have appropriate grounding in the surrounding layers. Also minimize the total bus length. Layout the SDIO bus so that crosstalk with other parts of the circuit is minimized. This provides adequate isolation between the signals, clock, and surrounding busses/traces. Also include an undisrupted return current path in close vicinity to the signal traces.

Figure 11 shows the suggested application schematic for the SDIO bus. The electrical requirements of the bus are described in Table 16.

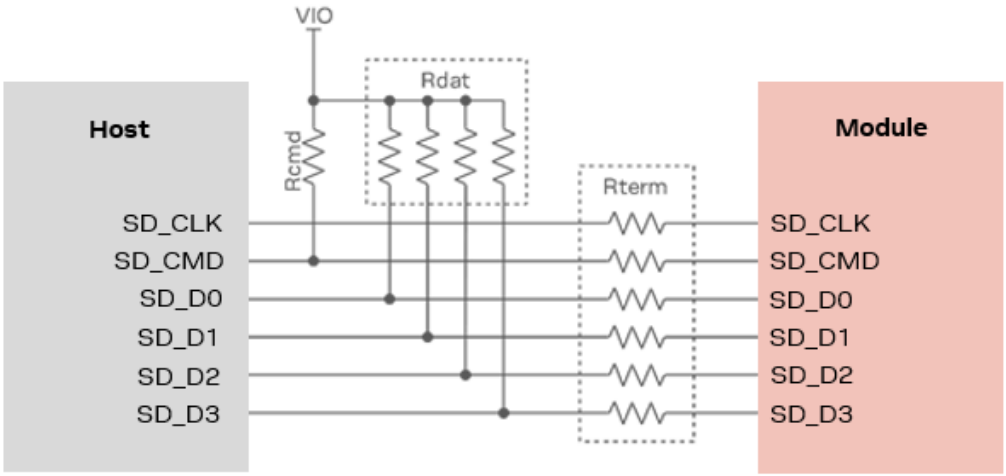


Figure 11: SDIO application schematic

☞ As an EMI debug option and signal termination for **SDIO_CLK**, consider using a small-value capacitor in the range of few picofarads to GND. Place the capacitor as close as possible to the clock input pin on the module. Mount the capacitor only if it is needed for EMI protection. The capacitor increases the total line capacitance which must not be so great that it violates the clock rise time and the timing specifications.

Signal Group	Parameter	Min.	Typ.	Max.	Unit
CLK, CMD, DAT[0:3]	Single ended impedance, Z_0		50		Ω
CLK, CMD, DAT[0:3]	Impedance control	$Z_0 - 10\%$	Z_0	$Z_0 + 10\%$	Ω
DAT[0:3]	Pull-Up range, Rdat	10	47	100	kΩ
CMD	Pull-Up range, Rcmd	10	10	50	kΩ
CLK, CMD, DAT[0:3]	Series termination (Host side), Rterm[1]	0	0		Ω
CLK, CMD, DAT[0:3]	Bus length[2]			100	mm
CMD, DAT[0:3]	Bus skew length mismatch to CLK	-3		+3	mm
CLK	Center to center CLK to other SDIO signals[3]	4*W			
CMD, DAT[0:3]	Center to center between signals[11]	3*W			

Table 16: SDIO bus requirements

[1] Series termination values larger than typical recommended only for addressing EMI issues.
[2] Routing should minimize the total bus length.
[3] Center to center spacing requirement can be ignored for up to 10 mm of routed length to accommodate BGA escape.

3.5.2 USB 2.0

The USB bus supports Hi-Speed connectivity with a transfer rate of 480 Mb/s. USB 2.0 offers a controlled impedance bus that uses a single differential pair. The main parameters to considerr when calculating the track impedance are shown in Figure 12.

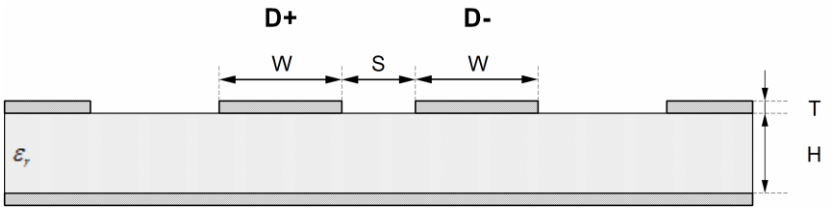


Figure 12: USB differential pair, controlled impedance parameters

To ensure bus signal integrity and avoid EMI issues, the USB data lines, follow the recommendations described in Table 17.

Signal Group	Parameter	Min.	Typ.	Max.	Unit
USB differential data	Single Ended impedance, Z_{SE}	45			Ω
	Differential impedance, Z_{diff}		90		Ω
	Common mode impedance, Z_{CM}		30		Ω
	Impedance control, Z_{SE}, Z_{diff}, Z_{CM}	$Z_0 - 10\%$	Z_0	$Z_0 + 10\%$	
	Shunt capacitance to GND			5	pF
	Bus skew length mismatch between differential pair		0	15[4]	mm
	Isolation to other signals	4 w			

Table 17: USB bus requirements

☞ USB data signals routed on the host board can influence RF performance. So, shunt capacitors or an ESD protection filter connected to GND might be needed to reduce any possible in-band noise caused by USB harmonics.

If the USB data link is routed on a connector, consider the use of a common mode choke with ESD protection on USB lines. To avoid signal degradation, only use common mode chokes to avoid possible EMI issues. For more information about proper ESD protection, see also the ESD guidelines.

3.5.3 Ethernet RMII

It is advisable to route all signals in the RMII bus with the same length. The signals should have appropriate grounding in the surrounding layers, and the total bus length should be minimized. Arrange the RMII bus layout to minimize crosstalk with other parts of the circuit, and provide adequate isolation between the signals, the clock, and the surrounding busses/traces.

Termination resistors are recommended for the RX and TX lines on the RMII bus.

A pull-up resistor is required for **RMII_MDIO** and **RMII_CRSDV**.

General high-speed layout guidelines are applicable for the RMII and SMI bus.

[4] Total mismatch includes skew introduced by cable and host side routing, keep it at minimum if USB bus is routed on a connector.

3.6 General layout guidelines

This section describes the best practice for the schematic design and circuit layout of the application.

3.6.1 Considerations for schematic design and PCB floor-planning

- Low frequency signals are generally not critical to the layout and designers should focus on the higher speed buses. One exception to this general rule is when high impedance traces, such as signals driven by weak pull resistors, might be affected by crosstalk. For these and similar traces, a supplementary isolation of 4w (four times the line width) from other buses is recommended.
- Verify which interface bus requires termination and add series resistor terminations to these buses.
- Carefully consider the placement of the module with respect to antenna position and host processor.
- Verify the controlled impedance dimensions of the selected PCB stack-up. The PCB manufacturer might be able to provide test coupons.
- Verify that the power supply design and power sequence are compliant with module specifications, as described in the module's data sheet.

⚠ Take particular care not to place components close to the antenna area and follow the recommendations from the antenna manufacturer to determine the safe distance between the antenna and any other part of the system. Designers should also maximize the distance between the antenna and high-frequency buses, like DDRs and related components, or consider the use of an optional metal shield to reduce the potential interference picked up by the module antenna.

3.6.2 Layout and manufacturing

- Place the module such that it provides optimum RF performance. This includes short low loss antenna connections and unobstructed antenna placement.
- Place bypass capacitors as close as possible to the module. Prioritize the placement of capacitors with the least capacitance so that these are closest to module pads. The supply rails must be routed through the capacitors from the power supply to the supply pad on the module.
- Avoid stubs and through-hole vias on high-speed signals which might adversely affect signal quality.
- Verify the recommended maximum signal skew for differential pairs and length matching of buses.
- Minimize the routing length. Ensure that the maximum allowable length for high-speed buses is not exceeded. Longer traces generally degrade signal performance.
- For impedance matched traces, consult with your PCB manufacturer early in the project for proper stack-up definition.
- Separate the RF and digital sections of the board.
- Don't split ground layers under the module.
- Minimize the bus length to reduce potential EMI issues from digital buses.
- Couple all traces (including low speed or DC traces) with a reference plane (GND or power), and reference all hi-speed buses against the ground plane. If any ground reference needs to be changed, add an adequate number of GND vias in the area in which the layer is switched. This is necessary to provide a low impedance path between the two GND layers for the return current.
- Don't change the reference plane for Hi-Speed buses. If changes in the reference plane are unavoidable, add capacitors in the transition area of the reference planes. This is necessary to ensure that a low impedance return path exists through the different reference planes.
- Following the "3w rule", keep traces at a distance no less than three times that of its own width from the routing edge of the ground plane.

- For EMC purposes and the need to shield against any potential radiation, it is advisable to add GND stitching vias around the edge of the PCB. Traces on the PCB peripheral are not recommended.

3.6.3 Module footprint and paste mask

Figure 13 and Figure 14 show the pin layout for the IRIS-W10 series module. The proposed land pattern layout corresponds with the pin layout of the module. Both Solder Mask Defined (SMD) and Non Solder Mask Defined (NSMD) pins can be used.

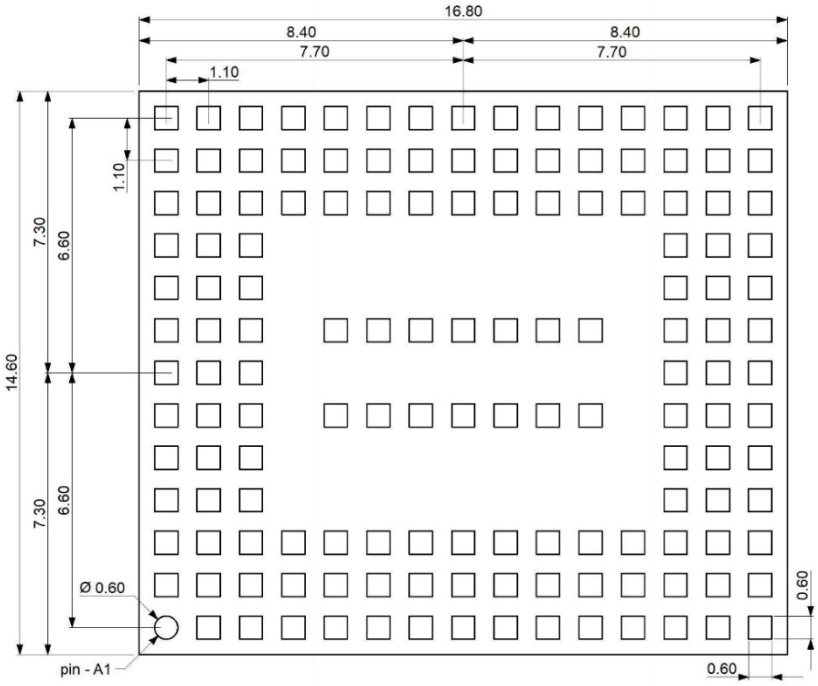


Figure 13: IRIS-W101 recommended PCB footprint (top view)

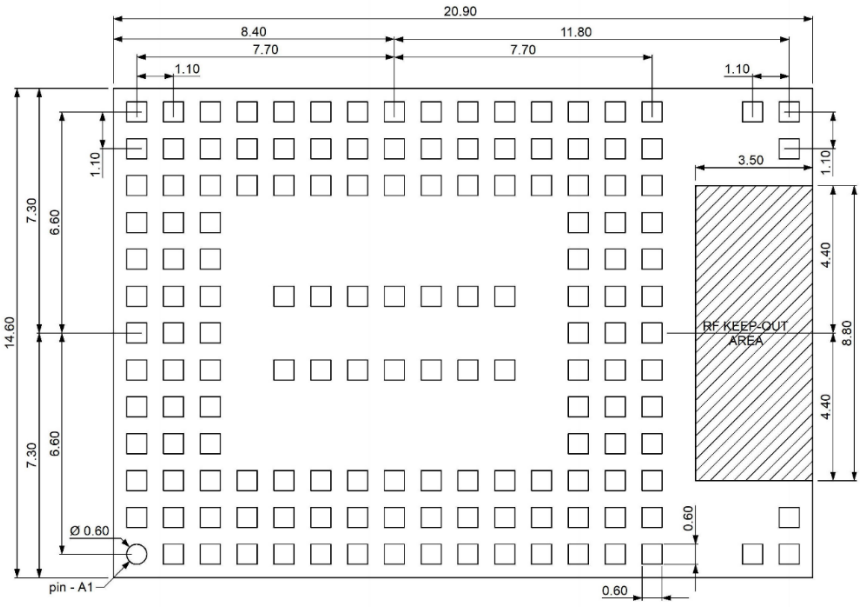


Figure 14: IRIS-W106 recommended PCB footprint (top view)

3.6.4 Thermal guidelines

IRIS-W10 series modules are designed to operate in a specified temperature range at an ambient temperature inside the enclosure box. The PCB generates heat during high loads that must be dissipated to sustain the lifetime of the components.

The improvement of thermal dissipation in the module decreases its internal temperature and consequently increases the long-term reliability of device applications operating at high ambient temperatures.

For best performance, layouts should adhere to the following guidelines:

- Vias specification for ground filling: $300/600\mu m$ with no thermal reliefs allowed on vias.
- Ground via densities under the module: $50\ vias/cm^2$. Place thermal vias in the gaps between the thermal pads of the module.
- Minimum layer count and copper thickness: $4\ layers, 35\ \mu m$.
- Minimum board size: $55x70\ mm$.
- To optimize the heat flow from the module, avoid crossing the layers of power planes and signal beneath the module.

Use the following hardware techniques to further improve thermal dissipation in the module and optimize its performance in customer applications:

- Maximize the return loss of the antenna to reduce reflected RF power to the module.
- Improve the efficiency of any component that generates heat, including power supplies and processor, by dissipating it evenly throughout the application device.
- Provide sufficient ventilation in the mechanical enclosure of the application.
- For continuous operation at high temperatures, particularly in high-power density applications or smaller PCB sizes, include a heat sink on the bottom side of the main PCB. The heat sink is best connected using electrically insulated / high thermal conductivity adhesive[5].

3.6.5 ESD guidelines

Device immunity against Electrostatic Discharge (ESD) is a requirement for Electromagnetic Compatibility (EMC) conformance and use of the CE marking for products intended for sale in Europe. To bear the CE mark, all application products integrating u-blox modules must be conformance tested in accordance with the R&TTE Directive (99/5/EC), EMC Directive (89/336/EEC), and Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with the above directives also implies conformity to the following European norms for device ESD immunity: ESD testing standard CENELEC EN 61000-4-2 and radio equipment standards ETSI EN 301 489-1, ETSI EN 301 489-7, ETSI EN 301 489-24. The ESD immunity requirements for each of these standards are summarized in Table 18.

The ESD immunity test is performed at the enclosure port, which is defined by ETSI EN 301 489-1 as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is seen as all-insulating and includes conductive surfaces to house the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

Any extension of the ESD immunity test to the whole device is dependent on the device classification, as defined by ETSI EN 301 489-1. Applicability of the ESD immunity test to the related device ports, or the interconnecting cables to auxiliary equipment, depends on the device-accessible interfaces and manufacturer requirements, as defined by ETSI EN 301 489-1.

[5] Typically not required.

Contact discharges are performed on conductive surfaces, while air discharges are performed on insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in CENELEC EN 61000-4-2.

☞ The terms “integral antenna”, “removable antenna”, “antenna port”, “device classification” used in the context of this guideline are defined in ETSI EN 301 489-1. The terms “contact discharge” and “air discharge” are defined in CENELEC EN 61000 4-2.

Table 18 describes the ESD immunity requirements as defined by CENELEC EN 61000-4-2, ETSI EN 301 489-1, ETSI EN 301 489-7, ETSI EN 301 489-24.

Application	Category	Immunity level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration	Indirect Contact Discharge	* ±8 kV

*Tested on IRIS-W1 evaluation board - Pending.

Table 18: Electromagnetic Compatibility ESD immunity requirements

IRIS-W10 is manufactured with consideration to specific standards that minimize the occurrence of ESD events; the highly automated process complies with IEC61340-5-1 (STM5.2-1999 Class M1 devices) standard, and designers should subsequently implement proper measures to protect any pin that might be exposed to the end user from ESD events.

Compliance with the standard protection level specified in EN61000-4-2 is achieved by including ESD protection close to any areas that are accessible to the end user.

3.7 Design-in checklists

3.7.1 Schematic checklist

- ☐ The module pins are properly numbered and designated on the schematic, as shown in the pin list of the data sheet [2].
- ☐ Power supply design comply with the voltage supply requirement, as described in the respective IRIS-W10 data sheet [2].
- ☐ Adequate bypassing is present in front of the power pins, as described in the respective IRIS-W10 data sheet [2].
- ☐ Each signal group is consistent with its own power rail supply or proper signal translation has been provided, as described in the respective IRIS-W10 data sheet [2].
- ☐ When using an external antenna, provide a pi-filter in front of it for final matching. See Antenna integration guidelines section 3.3.

3.7.2 Layout checklist

- ☐ PCB stack-up and controlled impedance traces follow the recommendations given by the PCB manufacturer. See RF transmission line design.
- ☐ All pins are properly connected, and the footprint follows u-blox recommendations for pin design. See the solder mask information in the IRIS-W10 data sheet [2].
- ☐ Proper clearance has been provided between RF section and digital section.
- ☐ Proper isolation has been provided between Antennas for co-location RF systems.
- ☐ Bypass capacitors are placed close to the module. See Layout and manufacturing.
- ☐ Low impedance power path or power plane has been provided to the module.
- ☐ Controlled impedance traces are properly implemented on the layout (both RF and digital) and follow PCB manufacturer recommendations. See RF transmission line design.
- ☐ 50 Ω RF traces and connectors follow the rules described in Antenna interface.
- ☐ Antenna design has been reviewed by the antenna manufacturer. See Antenna integration guidelines.
- ☐ Proper grounding has been provided to the module for low impedance return path. See Layout and manufacturing.
- ☐ Reference plane skipping has been minimized for high frequency busses.
- ☐ All traces and planes are routed inside the area defined by the main ground plane.
- ☐ u-blox has reviewed and approved the PCB[6].

[6] This is applicable only for end-products based on u-blox reference designs.

4 Open CPU software

This section describes how to download and setup the software for different applications. The MCU software development toolkit, MCUXpresso SDK [17], currently supports the following environments:

- MCUXpresso IDE
- IAR Embedded Workbench
- Arm GCC

The SDK allows customer to develop the applications with support of FreeRTOS, which is available in the development kit. This chapter describes the steps necessary to configure, compile, debug, flash, and run the Wi-Fi and Bluetooth sample applications included in the MCUXpresso SDK. It also covers the configuration and required tool setup for the Integrated Development Environment (IDE).

☞ The publicly available MCUXpresso SDK doesn't support the NXP RW61x MCU yet. Contact your local u-blox support team for information how to gain the necessary download access.

4.1 MCUXpresso SDK

MCUXpresso SDK [17] is a widely adopted open-source Real Time Operating System (RTOS). The toolkit is supported by NXP chipsets, including the RW61x chip integrated in the IRIS-W10 module.

NXP Semiconductor provides the MCUXpresso IDE [19] and SDK [17] for development using the FreeRTOS.

4.1.1 Download MCUXpresso SDK

To get MCUXpresso SDK:

1. Go to MCUXpresso SDK Builder page [18].
2. Click **Select Development Board**
   - RDRW610**:** RW61x BGA board
   - RDRW610QFN: RW61x QFN board
   - Define the **Developer Environment Setting** (Select Host OS and IDE)
   - Build MCUXpresso SDK
   - Download the SDK Archive (includes documentation)
3. Import the SDK archive into either the MCUXpresso IDE [19] GCC setup [23], or IAR Workbench setup [22].

4.1.2 Board configuration

No special settings are required.

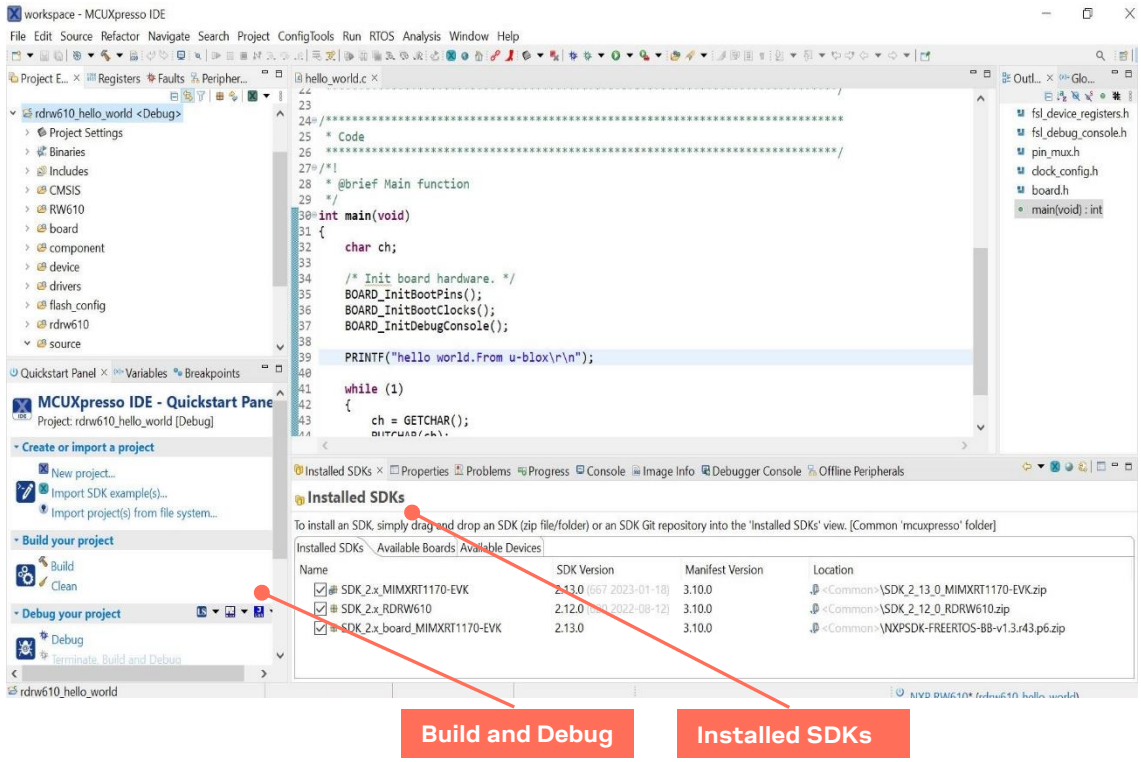
4.2 Open CPU IDE

Use this guide to import, configure, build, debug, and run the IRIS-W10 demo in the supported IDEs.

4.2.1 Building for IRIS-W10 with MCUXpresso IDE setup

To build a demo application:

1. Download the MCUXpresso SDK [17]
2. Download and open the MCUXpresso IDE [19]
3. From the “Installed SDKs” tab is located at the bottom of the central window, drag-and-drop the SDK into the designated area.
4. Select the evaluation board (RW61X)
5. Select a Wi-Fi or Bluetooth LE example and verify default project option
6. Build the application
7. To flash the software, select Debug from the menu (make sure IRIS-W10 is connected)
   By default, the project is configured to use the WIFI_BOARD_AW_RW610 in `app_config.h` from the source code directory.



All instructions are based on MCUXpresso IDE version v11.6.0 and pre-release SDK.

4.2.2 Building for IRIS-W10 with Arm GCC setup

This section outlines the process of configuring the command-line Arm® GCC tools for building and running demo applications, with the `wifi_cli` application serving as an example. This procedure can be applied to any example application available through the MCUXpresso SDK [17]. The instructions are based on the use of Linux, which is one of the operating systems supported by Arm GCC tools. For additional information on setting up the Arm GCC Toolchain [20]:

To get started with the MCUXpresso SDK, see MCUXSDKGSUG [26].

4.2.2.1 Install Arm GCC toolchain

To install the toolchain:

1. Download the toolchain [20] for Linux x86_64 system and cmake [21].

```
gcc-arm-none-eabi-XXXXXX-x86_64- linux.tar.bz2 (Linux x86_64 tarball)

tar -xf gcc-arm-none-eabi-10-2020-q4-major-x86_64-linux.tar.bz2
```

2. Export the `ARMGCC_DIR`

```
export ARMGCC_DIR=/toolchain-dir/gcc-arm-none-eabi-XXXXXX
```

3. Add toolchain path to **PATH** environment

```
export PATH=$PATH:/toolchain-dir/gcc-arm-none-eabi-XXXXXX/bin/
```

4.2.2.2 Build the application

To build the application using the Arm GCC toolchain [20]:

1. Go to the `armgcc` directory of the application.

```
cd /boards/rdrw610/wifi_examples/wifi_cli/armgcc
```

2. Build the application binary

```
 sh build_flash_debug.sh

[100%] Linking C executable flash_debug/wifi_cli.elf
[100%] Built target wifi_cli.elf
```

3. The application image `sdk20-app.bin` is autogenerated.

```
ls ./flash_debug
sdk20-app.bin wifi_cli.elf
```

Given commands are based on `SDK_2_12_0_RDRW610`. See also the latest NXP User Manual or SDK documentation [24].

4.2.2.3 Flash the application program

To flash the binary on the RW61x EVK board:

1. Connect the board to the Windows host system.
2. Open J-Link commander and connect to IRIS-W10.

```
J-Link> con
Device> RW610
TIF>S
Speed> enter
```

3. Flash the application image `sdk20-app.bin` to RW61x EVK FlexSPI NOR flash

```
J-Link>loadbin sdk20_app.bin,0x08001000s
```

4.2.3 Building for IRIS-W10 with IAR Workbench IDE

The software development process for the IRIS-W10 module can be accomplished using the IAR Embedded Workbench IDE.

To build a demo application:

1. Download MCUXpresso SDK [17]
2. Download and open IAR Embedded Workbench IDE [22]
3. Import SDK
4. Open the SDK and select the *.eww* extension file into workspace IDE
5. Select a Wi-Fi or Bluetooth LE example and verify default project option
6. Build the application
7. To flash the software, press Debug from the menu (make sure IRIS-W1 is connected)
8. By default, the project is configured to use the `WIFI_BOARD_AW_RW610` in `app_config.h` from the source code directory.

☞ The guidelines given in this section are specific to version 9.10.2 of the IAR Embedded Workbench IDE [22]. See also the latest NXP User manual [24].

4.3 Flashing open CPU software

IRIS-W10 open CPU modules are flashed using various utility programs over the SWD or JTAG interface.

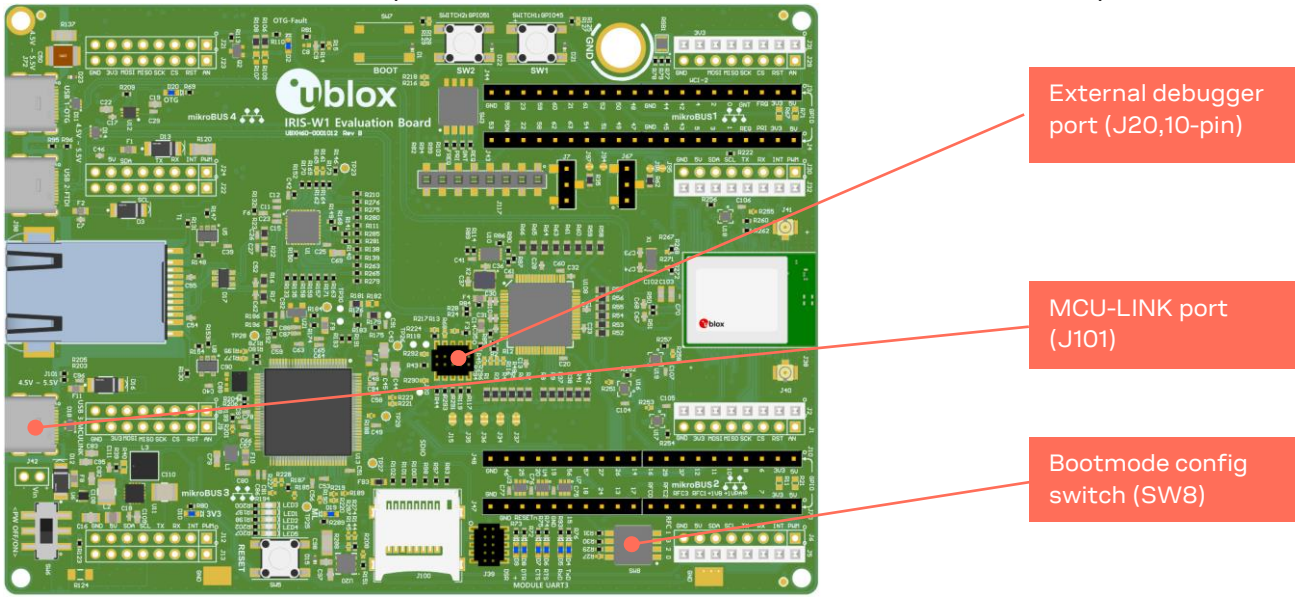
IAR IDE and SEGGER J-Link don't officially support RW61x, which means that additional patches for these two tools are needed to work with the RW61x MCU.

☞ To add additional patches, contact NXP support or check the user manual [24] [25].

4.3.1 Flashing over MCULINK port using the SWD interface

To flash the IRIS-W10 module:

1. Connect the USB-3 MCULINK port (**J101**) of the EVK-IRIS-W10 board to the host computer.



2. Select the SWD interface on tools like J-Link Commander or J Flash-Lite to flash the IRIS-W10 without an external debugger.

3. Launch the flashing tool on the computer.

Figure 15 and Figure 16 show flashing examples using the SEGGER J-link Lite Software flashing tool running on the host computer.

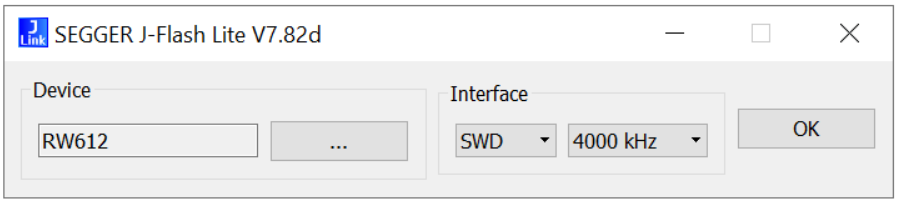


Figure 13: J-Flash Lite device SWD interface

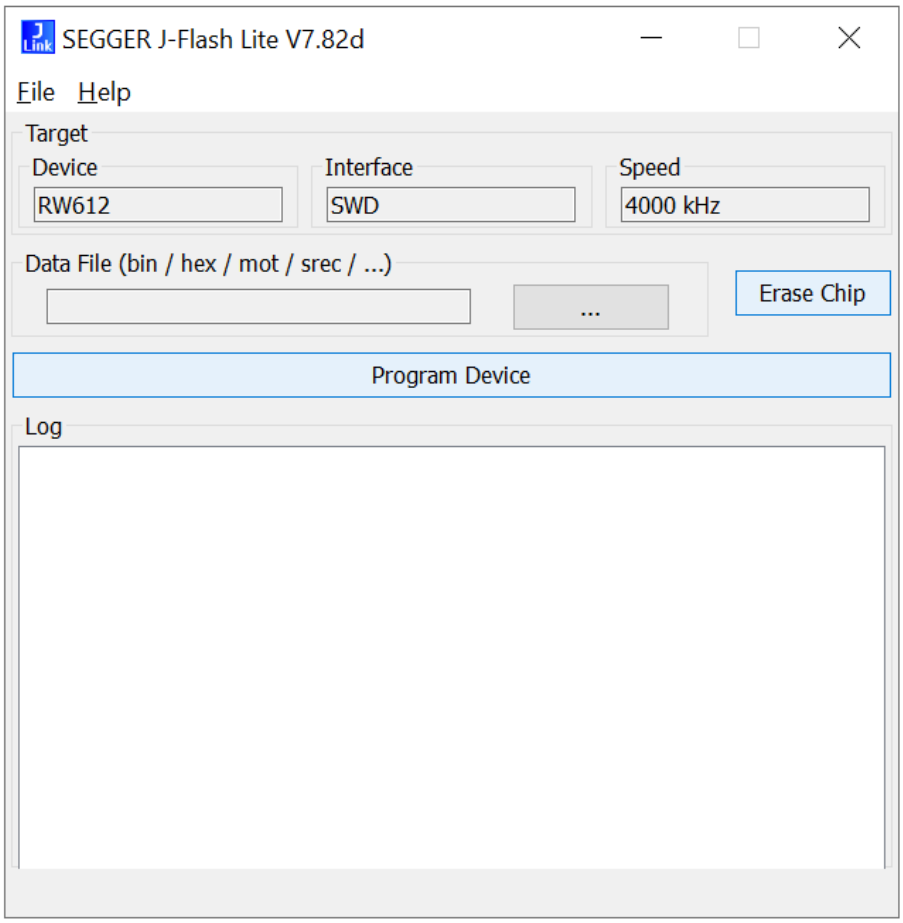


Figure 14: J-Flash Lite program target device over SWD interface

4.3.2 Flashing over the JTAG interface using an external debugger

To flash IRIS-W10 over the JTAG interface an external debugger must be connected to the JTAG interface of the module. Third-party tools, like J-Link Commander, J-Flash, J-Flash-Lite are used to flash the module.

☞ For information about connecting the external debugger to the 10-pin port, see the EVK-IRIS-W10 user guide [3].

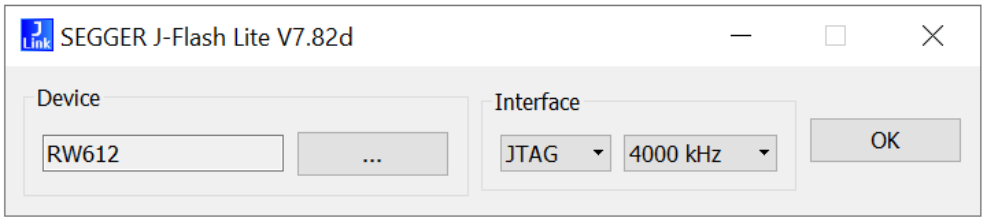


Figure 15: J-Flash Lite device over JTAG interface

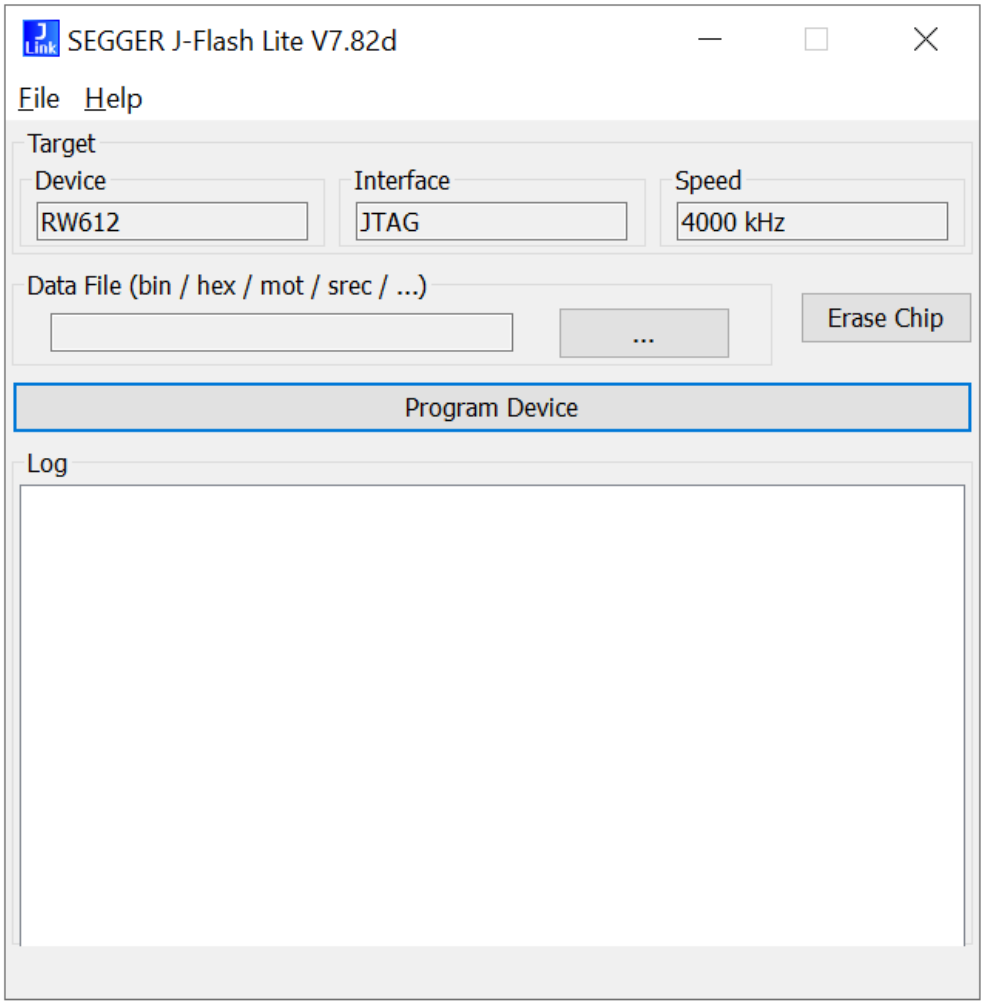


Figure 16: J-Flash Lite program target device over JTAG

- SEGGER J-Link BASE or NXP MCU-link Probe external debugger works with IRIS-W10 module.
- To generate a `.bin/.hex` application, it is necessary to utilize an internal feature of the MCUXpresso IDE during the application building process.
- EVK-IRIS-W10 incorporates an onboard debugger, which means that it can be flashed via SWD without an external debugger.

4.4 blhost application

The `blhost` application is a command-line utility used on the host computer to initiate communication and send commands to the IRIS-W1 bootloader. `blhost` supports multi-platforms like Windows, Linux (x86-based), macOS, and Linux (arm-based). The host computer can communicate directly with the IRIS-W1 bootloader over the UART (serial port) or USB connection.

The `blhost` tool is used to recover hardware from a bad or unknown state to normal mode. By using `blhost`, users can diagnose and resolve software-related issues and restore the hardware to a stable and functional state. Use `blhost` for flashing the firmware on IRIS-W1.

To use `blhost`, the EVK-IRIS-W10 must be in ISP boot (bootloader mode) during the start-up of the module.

After successfully recovering the board from an unknown state, proceed to switch the EVK back to QSPI Flash mode and initiate a restart of the EVK-IRIS-W10. This restores the board to its original out-of-the-box condition.

For more information about boot mode configuration, see also Configuration pins.

Use the following example to update the IRIS-W1 bootloader.

```
blhost [options] -- [command]
```

To reset and erase entire flash memory.

```
blhost.exe -p COMXX -- flash-erase-all 0
```

For further information about `blhost` use cases, see the NXP blhost User Manual [12].

5 Handling and soldering

⚠ IRIS-W10 series modules are Electrostatic Sensitive Devices that demand the observance of special handling precautions against static damage. Failure to observe these precautions can result in severe damage to the product.

5.1 ESD handling precautions

⚠ As the risk of electrostatic discharge in the RF transceivers and patch antennas of the module is of particular concern, standard ESD safety practices are prerequisite. See also Figure 15.

Consider also:

- When connecting test equipment or any other electronics to the module (as a standalone or PCB-mounted device), the first point of contact must always be to local GND.
- Before mounting an antenna patch, connect the device to ground.
- When handling the RF pin, don't touch any charged capacitors. Be especially careful when handling materials like patch antennas (~10 pF), coaxial cables (~50-80 pF/m), soldering irons, or any other materials that can develop charges.
- To prevent electrostatic discharge through the RF input, don't touch any exposed antenna area. If there is any risk of the exposed antenna being touched in an unprotected ESD work area, be sure to implement proper ESD protection measures in the design.
- When soldering RF connectors and patch antennas to the RF pin on the receiver, be sure to use an ESD-safe soldering iron (tip).

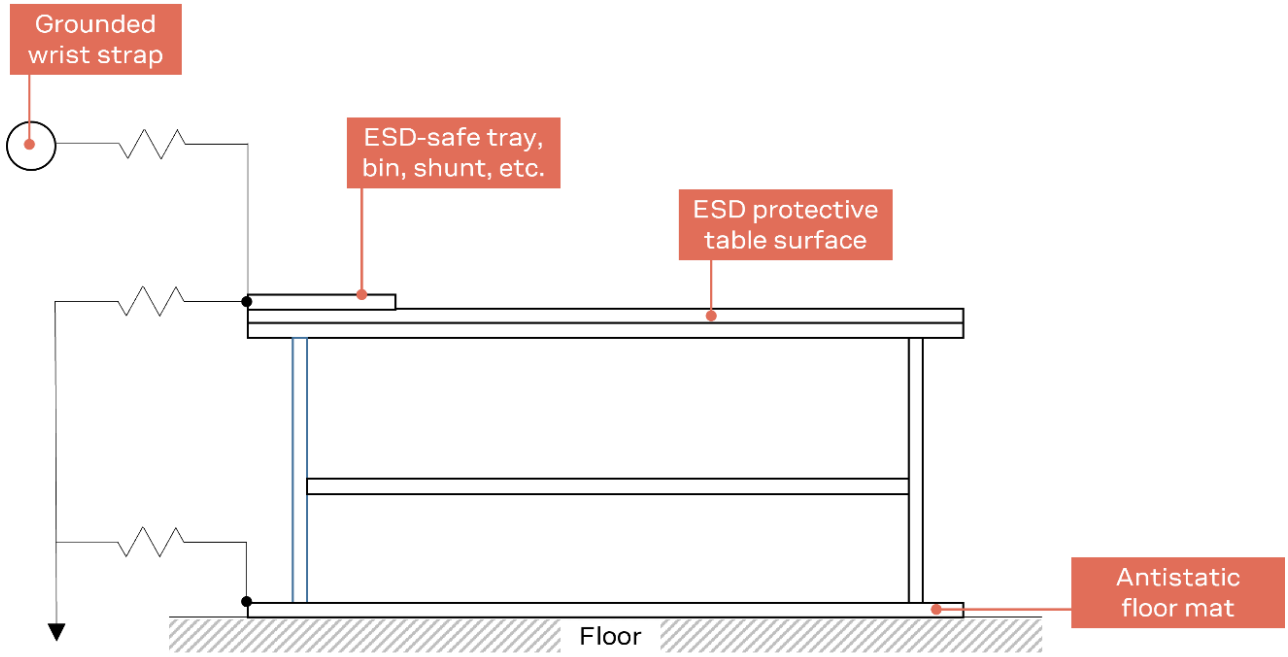


Figure 15: Standard workstation setup for safe handling of ESD-sensitive devices

5.2 Packaging, shipping, storage, and moisture preconditioning

For information pertaining to reels, tapes or trays, moisture sensitivity levels (MSL), shipment and storage, as well as drying for preconditioning, refer to the IRIS-W10 data sheet [2] and Packaging information reference guide [14].

5.3 Soldering

☞ No natural rubbers, hygroscopic materials, or materials containing asbestos are employed.

5.3.1 Reflow soldering process

IRIS-W10 modules are surface mounted devices supplied in a Land Grid Array (LGA) package with gold-plated solder lands. The modules are manufactured in a lead-free process with lead-free soldering paste.

The thickness of solder resist between the top side of host PCB and the bottom side of IRIS-W1 must be considered for the soldering process.

IRIS-W10 modules are compatible with the industrial reflow profile for common SAC type RoHS solders. No-clean soldering paste is strongly recommended.

The reflow profile is dependent on the thermal mass of the fully populated host PCB, the heat transfer efficiency of the oven, and the type of solder paste that is used. The optimal soldering profile that is used must be trimmed for each case depending on the specific soldering process and layout of the host PCB.

⚠ The target parameter values shown in Table 19 are only general guidelines for a Pb-free process and all given values are tentative and subject to change. For further information, see also the JEDEC J-STD-020C standard [4].

Process parameter		Unit	Value
Pre-heat	Ramp up rate to T_{SMIN}	K/s	3
	T_{SMIN}	°C	150
	T_{SMAX}	°C	200
	t_S (from 25 °C)	s	110
	t_S (Pre-heat)	s	60
Peak	T_L	°C	217
	t_L (time above T_L)	s	60
	T_P (absolute max)	°C	245
	t_P (time above T_P -5 °C)	s	10
Cooling	Ramp-down from T_L (absolute max)	K/s	6
General	$T_{to\ peak}$	s	300
	Allowed reflow soldering cycles	-	2

Table 19: Recommended reflow profiles

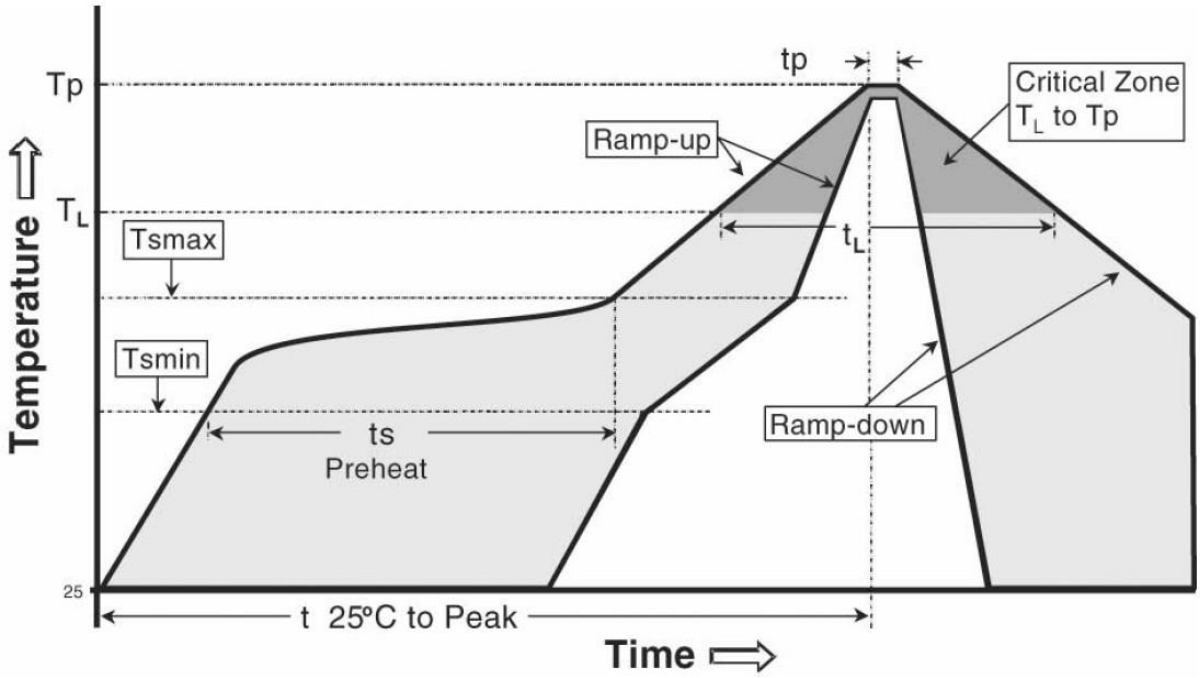


Figure 16: Reflow profile

☞ The lower value of T_P and slower ramp down rate (2–3 °C/sec) is preferred.

5.3.2 Cleaning

Cleaning the module is not recommended.

Residues underneath the module can't be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the label and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into areas that are not accessible for post-wash inspections. The solvent will also damage the label and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module and the crystal oscillators in particular. For best results use a "no clean" soldering paste and circumvent the need for a cleaning stage after the soldering process.

5.3.3 Other remarks

- Only a single wave soldering process is allowed for boards populated with the module.
- Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices might require THT components to be wave soldered.
- Miniature Wave Selective Solder processes are preferred over traditional wave soldering processes.
- Hand soldering is not recommended.
- Rework is not recommended.
- Conformal coating can affect the performance of the module, which means that it is important to prevent the liquid from flowing into the module. RF shields don't provide protection for the module from coating liquids with low viscosity; therefore, care is required while applying the coating. Conformal coating of the module will void the warranty.

- Grounding metal covers: Attempts to improve grounding by soldering ground cables, wick, or other forms of metal strips directly onto the EMI covers is done so at the customer's own risk and will void the module warranty. The numerous ground pins on the module are adequate to provide optimal immunity to interferences.
- The modules contain components that are sensitive to Ultrasonic Waves. Use of any ultrasonic processes, like cleaning and welding, might damage the module. Use of ultrasonic processes on an end product integrating this module will void the warranty.

6 Qualifications and approvals

⚠ Approvals for the IRIS-W1 module series are currently pending. For further information about the current approval status, see the Qualifications and approvals in the data sheet [2].

6.1 General requirements

IRIS-W1 modules are designed to comply with the regulatory demands of Federal Communications Commission (FCC), Innovation, Science and Economic Development Canada (ISED)[7] and the CE mark. This chapter contains instructions on the process needed for an integrator when including the IRIS-W1 module into an end-product.

- Any deviation from the process described may cause the IRIS-W1 module not to comply with the regulatory authorizations of the module and thus void the user's authority to operate the equipment.
- Any changes to hardware, hosts or co-location configuration may require new radiated emission and SAR evaluation and/or testing.
- The regulatory compliance of IRIS-W1 does not exempt the end-product from being evaluated against applicable regulatory demands; for example, FCC Part 15B criteria for unintentional radiators [9].
- The end-product manufacturer must follow all the engineering and operating guidelines as specified by the grantee (u-blox).
- IRIS-W1 is for OEM integrators only.
- Only authorized antenna(s) may be used. For the list of authorized antennas, see the IRIS-W1 data sheet [2].
- In the end-product, the IRIS-W1 module must be installed in such a way that only authorized antennas can be used.
- The end-product must use the specified Antenna reference design (IRIS-W101).
- Any notification to the end user about how to install or remove the integrated radio module is NOT allowed.

If these conditions can't be met or any of the operating instructions are violated, the u-blox regulatory authorization will be considered invalid. Under these circumstances, the integrator is responsible for re-evaluating the end-product including the IRIS-W1 module. The integrator is then also responsible for obtaining their own regulatory authorization, or u-blox may be able to support updates of the u-blox regulatory authorization.

6.2 European Union regulatory compliance

⚠ **Approvals are pending**

For information about the regulatory compliance of IRIS-W1 series modules against requirements and provisions in the European Union, see also the IRIS-W1 Declaration of Conformity [15].

⚠ Module integrators are required to make their own "Declaration of Conformity", in which test standards and directives that are tested and fulfilled by the end product are listed.

[7] Formerly known as IC (Industry Canada).

6.2.1 CE End-product regulatory compliance

6.2.1.1 Safety standard

In order to fulfill the safety standard EN 60950-1 [8], the IRIS-W10 module must be supplied with a Class-2 Limited Power Source.

6.2.2 CE Equipment classes

In accordance with Article 1 of Commission Decision 2000/299/EC[8], IRIS-W10 is defined as either Class-1 or Class-2 radio equipment, the end-product integrating IRIS-W10 inherits the equipment class of the module.

☞ For guidance on end product marking in according with RED, see http://ec.europa.eu/

⚠ The EIRP of the IRIS-W10 module must not exceed the limits of the regulatory domain in which the module operates. Depending on the host platform implementation and antenna gain, integrators must limit the maximum output power of the module through the host software. For information about the corresponding maximum transmit power levels, see Pre-approved antennas.

6.2.3 Radio Equipment Directive (RED) 2014/53/EU

IRIS-W1 series modules comply with the essential requirements and other relevant provisions of Radio Equipment Directive (RED) 2014/53/EU.

6.2.4 Compliance with the RoHS directive

IRIS-W1 series modules comply with the Directive 2011/65/EU (EU RoHS 2) and its amendment Directive (EU) 2015/863 (EU RoHS 3).

6.3 Great Britain regulatory compliance

⚠ **Approvals are pending**

For information about the regulatory compliance of IRIS-W10 modules against requirements and provisions in Great Britain, see also the IRIS-W10 UKCA Declaration of Conformity [16].

6.3.1 UK Conformity Assessed (UKCA)

☞ The United Kingdom is made up of the Great Britain (including England, Scotland, and Wales) and the Northern Ireland. Northern Ireland continues to accept the CE marking. The following notice is applicable to Great Britain only.

IRIS-W10 series modules have been evaluated against the essential requirements of the Radio Equipment Regulations 2017 (SI 2017 No. 1206, as amended by SI 2019 No. 696).

For guidance about using the UKCA marking: https://www.gov.uk/guidance/using-the-ukca-marking

[8] 2000/299/EC: Commission Decision of 6 April 2000 establishing the initial classification of radio equipment and telecommunications terminal equipment and associated identifiers.

6.4 FCC/ISED End-product regulatory compliance (pending)

u-blox represents that the modular transmitter fulfills the FCC/ISED regulations when operating in authorized modes on any host-product given that the integrator follows the instructions as described in this document. Accordingly, the host-product manufacturer acknowledges that all host-products referring to the FCC ID or ISED certification number of the modular transmitter and placed on the market by the host-product manufacturer need to fulfil all of the requirements mentioned below. Non-compliance with these requirements may result in revocation of the FCC approval and removal of the host-products from the market. These requirements correspond to questions featured in the FCC guidance for software security requirements for U-NII devices, FCC OET KDB 594280 D02 [11].

⚠ The modular transmitter approval of IRIS-W10, or any other radio module, does not exempt the end product from being evaluated against applicable regulatory demands.

The evaluation of the end product shall be performed with the IRIS-W10 module installed and operating in a way that reflects the intended end product use case. The upper frequency measurement range of the end product evaluation is the 5th harmonic of 5.8 GHz as described in KDB 996369 D04.

The following requirements apply to all products that integrate a radio module:

- Subpart B - UNINTENTIONAL RADIATORS
  To verify that the composite device of host and module comply with the requirements of FCC part 15B, the integrator shall perform sufficient measurements using ANSI 63.4-2014.
- Subpart C - INTENTIONAL RADIATORS
  It is required that the integrator carries out sufficient verification measurements using ANSI 63.10-2013 to validate that the fundamental and out of band emissions of the transmitter part of the composite device complies with the requirements of FCC part 15C.

When the items listed above are fulfilled, the end product manufacturer can use the authorization procedures as mentioned in Table 1 of 47 CFR Part 15.101, before marketing the end product. This means the customer has to either market the end product under a Suppliers Declaration of Conformity (SDoC) or to certify the product using an accredited test lab.

The description is a subset of the information found in applicable publications of FCC Office of Engineering and Technology (OET) Knowledge Database (KDB). We recommend the integrator to read the complete document of the referenced OET KDB's.

- KDB 178919 D01 Permissive Change Policy
- KDB 447498 D01 General RF Exposure Guidance
- KDB 594280 D01 Configuration Control
- KDB 594280 D02 U-NII Device Security
- KDB 784748 D01 Labelling Part 15 18 Guidelines
- KDB 996369 D01 Module certification Guide
- KDB 996369 D02 Module Q&A
- KDB 996369 D04 Module Integration Guide

6.4.1 United States compliance statement (FCC)

IRIS-W10 series modules have modular approval and comply with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

⚠ Any changes or modifications NOT explicitly APPROVED by u-blox could cause the IRIS-W10 series module to cease to comply with FCC rules part 15 thus void the user's authority to operate the equipment.

Table 20 shows the FCC IDs allocated to IRIS-W10 series modules.

Model	FCC ID
IRIS-W101-00B	XPYIRISW1
IRIS-W106-00B	XPYIRISW1
IRIS-W101-10B	XPYIRISW1
IRIS-W106-10B	XPYIRISW1
IRIS-W101-30B	XPYIRISW1
IRIS-W106-30B	XPYIRISW1

Table 20: FCC IDs for different variants of IRIS-W10 series modules

For FCC end-product labeling requirements, see End product labeling requirements.

6.4.2 Canada compliance statement (ISED)

IRIS-W10 series modules are certified for use in accordance with Innovation, Science and Economic Development Canada (ISED) Radio Standards Specification (RSS) RSS-247 Issue 2 and RSS-Gen. Table 21 shows the ISED certification IDs allocated to IRIS-W10 series modules.

Model	ISED certification ID
IRIS-W101-00B	8595A-IRISW1
IRIS-W106-00B	8595A-IRISW1
IRIS-W101-10B	8595A-IRISW1
IRIS-W106-10B	8595A-IRISW1
IRIS-W101-30B	8595A-IRISW1
IRIS-W106-30B	8595A-IRISW1

Table 21: ISED IDs for different variants of IRIS-W10 series modules

IRIS-W10 complies with ISED (Innovation, Science and Economic Development Canada)[9] license-exempt RSS(s). Operation is subject to the following two conditions:

1. This device may not cause interference, and
2. This device must accept any interference, including interference that may cause undesired operation of the device.

☞ Any notification to the end user of installation or removal instructions about the integrated radio module is NOT allowed. Unauthorized modification could void authority to use this equipment.

[9] Formerly known as IC (Industry Canada).

This radio transmitter IC: 8595A-IRISW1 has been approved by ISED to operate with the antenna types listed in Pre-approved antennas with the maximum permissible gain indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

☞ Operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

☞ Operation in the 5600-5650 MHz band is not allowed in Canada. High-power radars are allocated as primary users (i.e., priority users) of the bands 5250-5350 MHz and 5650-5850 MHz and that these radars could cause interference and/or damage to LE-LAN devices.

Le présent appareil est conforme aux CNR d'ISED applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

(1) l'appareil ne doit pas produire de brouillage, et

(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Cet émetteur radio, IC: 8595A-IRISW1 été approuvé par ISED pour fonctionner avec les types d'antenne énumérés ci-dessous avec le gain maximum autorisé et l'impédance nécessaire pour chaque type d'antenne indiqué. Les types d'antennes non inclus dans la liste des antennes approuvées et ayant un gain supérieur au gain maximum indiqué pour ce type sont strictement interdits pour une utilisation avec cet appareil.

☞ Le dispositif de fonctionnement dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur pour réduire le risque d'interférences nuisibles à la co-canal systèmes mobiles par satellite

☞ Opération dans la bande 5600-5650 MHz n'est pas autorisée au Canada. Haute puissance radars sont désignés comme utilisateurs principaux (c.-à utilisateurs prioritaires) des bandes 5250-5350 MHz et 5650-5850 MHz et que ces radars pourraient causer des interférences et / ou des dommages à dispositifs LAN-EL.

For ISED end-product labeling requirements, see End product labeling requirements.

☞ The approval type for all IRIS-W10 series variants is a single modular approval. Due to ISED Modular Approval Requirements (Source: RSP-100 Issue 10), any application which includes the module must be approved by the module manufacturer (u-blox). The application manufacturer must provide design data for the review procedure.

6.4.1 RF exposure statement

6.4.1.1 ISED compliance

All transmitters regulated by ISED must comply with RF exposure requirements listed in RSS-102 - Radio Frequency (RF) Exposure Compliance of Radiocommunication Apparatus (All Frequency Bands). This module is approved for installation into mobile and/or portable host platforms and must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with Innovation, Science and Economic Development Canada (ISED) multi-transmitter guidelines. End-users must be provided with transmitter operating conditions for satisfying RF Exposure compliance.

To fulfil the requirements of the SAR evaluation Exemption limits defined in RSS-102 issue 5, an OEM integrator implementing IRIS-W10 series modules into an end-product must ensure a separation distance of 45 mm between the user (or bystander) and the antenna (or radiating element).

6.4.1.2 FCC compliance

All transmitters regulated by FCC must comply with RF exposure requirements. KDB 447498 General RF Exposure Guidance provides guidance in determining whether proposed or existing transmitting facilities, operations or devices comply with limits for human exposure to Radio Frequency (RF) fields adopted by the Federal Communications Commission (FCC).

IRIS-W10 modules are approved for installation into mobile and/or portable host platforms and must not be co-located or operating in conjunction with any other antenna or transmitter – except in accordance with FCC multi-transmitter guidelines.

To ensure that the max output power of IRIS-W10 series modules remains below the SAR Test Exclusion Threshold defined in KDB 447498 D01v06, an OEM integrator integrating IRIS-W10 series modules into an end-product must ensure a separation distance of 40 mm between the user (or bystander) and the antenna (or radiating element).

6.4.2 Referring to the u-blox FCC/ISED certification ID

If the General requirements, FCC/ISED End-product regulatory compliance and all Antenna requirements are met, the u-blox modular FCC/ISED regulatory authorization is valid and the end-product may refer to the u-blox FCC ID and ISED certification number. u-blox may be able to support updates to the u-blox regulatory authorization by adding new antennas to the u-blox authorization for example. See also Antenna requirements.

⚠ To use the u-blox FCC / ISED grant and refer to the u-blox FCC ID / ISED certification ID, the integrator must confirm with u-blox that the all requirements associated with the software configuration and Software configuration and control are fulfilled.

6.4.3 Obtaining own FCC/ISED certification ID

Integrators who do not want to refer to the u-blox FCC/ISED certification ID, or who do not fulfil all requirements to do so may instead obtain their own certification. With their own certification, the integrator has full control of the grant to make changes.

Integrators who want to base their own certification on the u-blox certification can do so via a process called “Change in ID” (FCC) / “Multiple listing” (ISED). With this, the integrator becomes the grantee of a copy of the u-blox FCC/ISED certification. u-blox will support with an approval letter that shall be filed as a Cover Letter exhibit with the application.

⚠ It is the responsibility of the integrator to comply with any upcoming regulatory requirements.

6.4.4 Antenna requirements

☞ To support verification activities that may be required by certification laboratories, customers applying for Class-II Permissive changes must implement the setup described in Software configuration and control.

6.4.4.1 Separation distance

If the required separation distance defined in section 6.4.1 cannot be fulfilled, a SAR evaluation must be performed. This consists of additional calculations and/or measurements. The result must be added to the grant file as a Class II Permissive Change.

6.4.4.2 Co-location (simultaneous transmission)

If the module is to be co-located with another transmitter, additional measurements for simultaneous transmission are required. The results must be added to the grant file as a Class II Permissive Change.

6.4.4.3 Adding a new antenna for authorization

If the authorized antennas and/or antenna trace design cannot be used, the new antenna and/or antenna trace designs must be added to the grant file. This is done by a Class I Permissive Change or a Class II Permissive Change, depending on the specific antenna and antenna trace design.

- Antennas of the same type and with less or same gain as those included in the list of Pre-approved antennas can be added under a Class I Permissive Change.
- Antenna trace designs deviating from the u-blox reference design and new antenna types are added under a Class II Permissive Change.
- For 5 GHz modules, the combined minimum gain of antenna trace and antenna must be greater than 0 dBi to comply with DFS testing requirements.

⚠ Integrators intending to refer to the u-blox FCC ID / ISED certification ID must contact their local support team to discuss the Permissive Change Process. Class II Permissive Changes are subject to NRE costs.

6.4.5 Software configuration and control

☞ “Modular transmitter” hereafter refers to IRIS-W10 series (FCC ID XPYIRISW1).

As the end product must comply with the requirements addressed by the OET KDB 594280 [10], the host-product integrating the IRIS-W10 must comply with the following requirements:

- Upon request from u-blox, the host-product manufacturer will provide all of the necessary information and documentation to demonstrate how the requirements listed below are met.
- The host-product manufacturer will not modify the modular transmitter hardware.
- The configuration of the modular transmitter when installed into the host-product must be within the authorization of the modular transmitter at all times and cannot be changed to include unauthorized modes of operation through accessible interfaces of the host-product. The Wi-Fi transmit output power limits must be followed. In particular, the modular transmitter installed in the host-product will not have the capability to operate on the operating channels/frequencies referred to in the section(s) below, namely the following channels: 12 (2467 MHz), 13 (2472 MHz)). The channels 120 (5600 MHz), 124 (5620 MHz), and 128 (5640 MHz) are allowed to be used in the US in client mode only. IRIS-W10 use is certified as supporting DFS client functionality.
- The host-product uses only authorized firmware images provided by the host-product manufacturer, u-blox, and/or by the manufacturer of the RF chipset used inside the modular transmitter.

- The configuration of the modular transmitter must always follow the requirements specified in Operating frequencies and cannot be changed to include unauthorized modes of operation through accessible interfaces of the host-product.
- The modular transmitter must when installed into the host-product have a regional setting that is compliant with authorized US modes and the host-product is protected from being modified by third parties to configure unauthorized modes of operation for the modular transmitter, including the country code.
- The host-product into which the modular transmitter is installed does not provide any interface for the installer to enter configuration parameters into the end product that exceeds those authorized.
- The host-product into which the modular transmitter is installed does not provide any interface to third parties to upload any unauthorized firmware images into the modular transmitter and prevents third parties from making unauthorized changes to all or parts of the modular transmitter device driver software and configuration.

☞ OET KDB 594280 D01 [10] lists the topics that must be addressed to ensure that the end-product specific host meets the Configuration Control requirements.

☞ OET KDB 594280 D02 [11] lists the topics that must be addressed to ensure that the end-product specific host meets the Software Security Requirements for U-NII Devices.

6.4.6 Operating frequencies

IRIS-W10 802.11b/g/n operation outside the 2412–2462 MHz band is prohibited in the US and Canada and 802.11a/n operation in the 5600–5650 MHz band is prohibited in Canada. Configuration of the module to operate on channels 12–13 and 120–128 must be prevented accordingly.

The channels allowed while operating under the definition of a master or client device[10] are described in Table 22.

Channel number	Channel center frequency [MHz]	Master device	Client device	Remarks
1 – 11	2412 – 2462	Yes	Yes	
12 – 13	2467 – 2472	No	No	
36 – 48	5180 – 5240	Yes	Yes	Canada (ISED): Devices are restricted to indoor operation only and the end product must be labelled accordingly.
52 – 64	5260 – 5320	No	Yes	
100 – 116	5500 – 5580	No	Yes	
120 – 128	5600 – 5640	No	Yes	USA (FCC): Client device operation allowed under KDB 905462 Canada (ISED): Operation is prohibited in this band
132 – 144	5660 – 5720	No	Yes	
149 – 165	5745 – 5825	Yes	Yes	

Table 22: Allowed channel usage under FCC/ISED regulation

☞ 15.407 (j) Operator Filing Requirement:
Before deploying an aggregate total of more than one thousand outdoor access points within the 5.15–5.25 GHz band, parties must submit a letter to the Commission acknowledging that, should harmful interference to licensed services in this band occur, they will be required to take corrective action. Corrective actions may include reducing power, turning off devices, changing frequency bands, and/or further reducing power radiated in the vertical direction. This material shall be

[10] 47 CFR §15.202

submitted to Laboratory Division, Office of Engineering and Technology, Federal Communications Commission, 7435 Oakland Mills Road, Columbia, MD 21046. Attn: U-NII Coordination, or via Web site at https://www.fcc.gov/labhelp with the subject line: “U-NII-1 Filing”.

6.4.7 End product labeling requirements

For an end-product using the IRIS-W10, there must be a label containing, at least, the following information:

This device contains
FCC ID: XPYIRISW1
IC: 8595A-IRISW1

“XPY” represents the FCC "Grantee Code" for u-blox AG, this code may consist of Arabic numerals, capital letters, or other characters, the format for this code will be specified by the Commission's Office of Engineering and Technology[12]. “8595A” is the Company Number for u-blox AG registered at ISED. “IRISW1” is the Unique Product Number decided by the grant owner.

The label must be affixed to an exterior surface of the end product such that it will be visible upon inspection in compliance with the modular labeling requirements of OET KDB 784748. The host user manual must also contain clear instructions on how end users can find and/or access the FCC ID of the end product.

The label on the IRIS-W10 module containing the original FCC ID acquired by u-blox can be replaced with a new label stating the end-product’s FCC/ISED ID in compliance with the modular labeling requirements of OET KDB 784748.

FCC end product labeling

In accordance with 47 CFR § 15.19, the end product shall bear the following statement in a conspicuous location on the device:

Contains FCC ID: XPYIRISW1
This device complies with part 15 of the FCC rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

The following statement must be included in the end-user manual or guide:

Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user’s authority to operate the equipment.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

[12] 47 CFR 2.926

ISED end product labeling

The end product shall bear the following statement in both English and French in a conspicuous location on the device:

Contains transmitter module IC: 8595A-IRISW1 This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development Canada's licence-exempt RSS(s). Operation is subject to the following two conditions: 1. This device may not cause interference. 2. This device must accept any interference, including interference that may cause undesired operation of the device.

Contient le module émetteur IC: 8595A-IRISW1 L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: 1. L' appareil ne doit pas produire de brouillage; 2. L'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre lefonctionnement.

Labels of end products capable of operating within the band 5150–5250 MHz shall also include:

For indoor use only
Pour usage intérieur seulement

When the device is so small or for such use that it is not practicable to place the statements above on it, the information shall be placed in a prominent location in the instruction manual or pamphlet supplied to the user or, alternatively, shall be placed on the container in which the device is marketed. However, the FCC/ISED ID label must be displayed on the device as described above.

In cases where the final product will be installed in locations where the end-consumer is unable to see the FCC/ISED ID and/or this statement, the FCC/ISED ID and the statement shall also be included in the end-product manual.

6.5 Japan radio equipment compliance

⚠ **Approvals are pending**

6.5.1 Compliance statement

IRIS-W1 series modules comply with the Japanese Technical Regulation Conformity Certification of Specified Radio Equipment (ordinance of MPT N°. 37, 1981), Article 2, Paragraph 1:

- Item 19 "2.4 GHz band wide band low power data communication system".

6.5.2 End product labelling requirement

End products based on IRIS-W1 series modules and targeted for distribution in Japan must be affixed with a label with the "Giteki" marking, as shown in Figure 17. The marking must be visible for inspection.

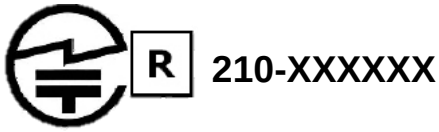


Figure 17: Giteki "R" mark and IRIS-W1 MIC certification number

6.5.3 End product user manual requirement

As the MIC ID is not included on the IRIS-W1 marking, the end product manufacturer must include a copy of the IRIS-W1 Japan Radio Certificate in the end product technical documentation.

6.6 NCC Taiwan compliance

⚠ **Approvals are pending**

6.6.1 Taiwan NCC Warning Statement

取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。
低功率射頻器材之使用不得影響飛航安全及干擾合法通信；經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。前述合法通信，指依電信管理法規定作業之無線電通信。低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

系統廠商應於平台上標示「本產品內含射頻模組：XXXyyyLPDzzzz-x」字樣

Statement translation:

- Without permission granted by the NCC, any company, enterprise, or user is not allowed to change frequency, enhance transmitting power, or alter original characteristic as well as performance to an approved low power radio-frequency device.
- The low power radio-frequency devices shall not influence aircraft security and interfere legal communications; If any interference is found or suspected, the user shall immediately cease operating the equipment until the interference has been prevented. The said legal communications means radio communications is operated in compliance with the Telecommunications Act. The low power radio-frequency devices must be susceptible with the interference from legal communications or ISM radio wave radiated devices.

6.6.2 Labeling requirements for end product

End products based on IRIS-W1 series modules and targeted for distribution in Taiwan must carry labels with the textual and graphical elements shown in Figure 18.

Contains Transmitter Module

內含發射器模組: **xxxxxxxyyyyyyy**

Figure 18: Taiwan logo and certification reference

Other wording can be used, but only if the meaning of original messaging remains unchanged. The label must be physically attached to the product and made clearly visible for inspection.

6.7 KCC South Korea compliance

⚠ **Approvals are pending**

IRIS-W1 series modules are certified by the Korea Communications Commission (KCC).

End products based on IRIS-W1 series modules and targeted for distribution in South Korea must carry labels containing the KCC logo and certification number, as shown Figure 19. This information must also be included in the product user manuals.

TBD

Figure 19: KCC logo and certification number

☞ The height of the KCC logo must be at least 5 mm.

6.8 Brazil compliance

⚠ **Approvals are pending**

End products based on IRIS-W1 series modules and targeted for distribution in Brazil must carry labels that include the Anatel logo, IRIS-W1 Homologation number: xxxxx-xx-yyyyy and a statement claiming that the device may not cause harmful interference but must accept it (Resolution No 506).

ANATEL
xxxxx-xx-yyyyy

"Este equipamento opera em caráter secundário, isto é, não tem direito a proteção contra interferência prejudicial, mesmo de estações do mesmo tipo, e não pode causar interferência a sistemas operando em caráter primário."

Statement translation:

"This equipment operates on a secondary basis and, consequently, must accept harmful interference, including from stations of the same kind, and may not cause harmful interference to systems operating on a primary basis."

When the device is so small or for such use that it is not practicable to place the statement above on the label, the information shall be placed in a prominent location in the instruction manual or pamphlet supplied to the user or, alternatively, shall be placed on the packaging in which the device is marketed.

In cases where the final product is to be installed in locations where the end user is unable to see the Anatel logo, IRIS-W1 Homologation number and/or statement, these graphical and textual elements must be included in the end product manual.

6.9 Australia and New Zealand regulatory compliance

IRIS-W1 modules are compliant with the standards made by the Australian Communications and Media Authority (ACMA).

⚠ **Approvals are pending**

The modules are compliant with AS/NZS 4268:2012 standard – Radio equipment and systems – Short range devices – Limits and methods of standard measurement. The test reports for IRIS-W1 modules can be used as part of the product certification and compliance folder. Contact your local support team for more information.

To meet the overall Australian and/or New Zealand end product compliance standards, the integrator must create a compliance folder containing all the relevant compliance test reports such as RF, EMC, electrical safety and DoC (Declaration of Conformity). It is the responsibility of the integrator to know what is required in the compliance folder for ACMA compliance.

For more information on Australia compliance, refer to the Australian Communications and Media Authority web site http://www.acma.gov.au/.

For more information on New Zealand compliance, refer to the New Zealand Radio Spectrum Management Group web site www.rsm.govt.nz.

6.10 South Africa regulatory compliance

Approvals are pending

IRIS-W1 series modules are compliant and certified by the Independent Communications Authority of South Africa (ICASA). End products that are made available for sale or lease or supplied in any other manner in South Africa shall have a legible label permanently affixed to its exterior surface. The label shall include the ICASA logo and the ICASA issued license number, as shown in the figure below. The minimum width and height of the ICASA logo shall be 3 mm. The approval labels must be purchased by the customer's local representative directly from the approval authority ICASA.

A sample of a IRIS-W1 ICASA label is in Figure 20.

Figure 20: ICASA label

More information on registration as a Responsible Integrator and labeling requirements can be found at the following website:

Independent Communications Authority of South Africa (ICASA) web site - https://www.icasa.org.za

7 Antennas

This chapter describes the antennas that are planned for pre-approval with IRIS-W1 modules.

⚠ All approvals are currently pending

☞ Note that not all antennas are approved for use in all markets/regions.

7.1 Antenna accessories

Name	U.FL to SMA adapter cable
Connector	U.FL and SMA jack (outer thread and pin receptacle)
Impedance	50 Ω
Minimum cable loss	0.5 dB, The cable loss must be above the minimum cable loss to meet the regulatory requirements. Minimum cable length 100 mm.
Comment	The SMA connector can be mounted in a panel. For information describing how to integrate the U.FL connector,
Approval	RED, UKCA, MIC, KCC, ANATEL, RCM, and ICASA

Name	U.FL to Reverse Polarity SMA adapter cable
Connector	U.FL and Reverse Polarity SMA jack (outer thread and pin)
Impedance	50 Ω
Minimum cable loss	0.5 dB. The cable loss must be above the minimum cable loss to meet the regulatory requirements. Minimum cable length 100 mm.
Comment	The Reverse Polarity SMA connector can be mounted in a panel. This reference design must be followed to comply with the IRIS-W10 FCC/IC modular approvals.
Approval	FCC, ISED, RED, UKCA, MIC, KCC, ANATEL, RCM, NCC, and ICASA

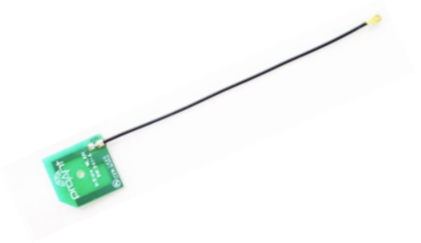
7.2 Pre-approved antennas

7.2.1 Dual band antennas

IRIS-W106	
Manufacturer	Abracon
Gain	1.74 dBi (2.4 GHz), 1.63 dBi (5 GHz)
Impedance	50 Ω
Size (HxWxL)	Embedded into the PCB
Type	PIFA
Comment	Embedded PCB antenna on IRIS-W106. Should not be mounted inside a metal enclosure. See also Embedded PCB antenna. .
Approval	FCC, ISED, RED, UKCA, MIC, KCC, ANATEL, RCM, NCC, and ICASA

PRO-IS-432	
Manufacturer	Abracon
Gain	0.8 dBi (2.4 GHz), 3.4 dBi (5 GHz)
Impedance	50 Ω

PRO-IS-432	
Size	22 x 20 x 0.8 mm
Type	Patch
Cable length	100 mm
Connector	U.FL. connector
Comment	Should be attached to a plastic enclosure or part for best performance.
Approval	FCC, ISED, RED, UKCA, MIC, KCC, ANATEL, RCM, NCC, and ICASA



ANTX100P002B24553	
Manufacturer	Pulse Electronics / Yageo
Gain	0.7 dBi (2.4 GHz), 1.9 dBi (5 GHz)
Impedance	50 Ω
Size	40 x 43 x 0.55 mm
Type	PCB patch
Cable length	100 mm
Connector	U.FL. connector
Comment	Should be attached to a plastic enclosure or part for best performance.
Approval	FCC, ISED, RED, UKCA, MIC, KCC, ANATEL, RCM, NCC, and ICASA

W1039B030	
Manufacturer	Pulse Electronics / Yageo
Gain	+1.5 dBi (2.4 GHz), +3.2 dBi (5 GHz)
Impedance	50 Ω
Size	104.8 mm (Straight)
Type	¼ wave monopole dual-band antenna
Cable length	76 mm
Polarization	Vertical
Connector	U.FL
Comment	For optimal performance this antenna should be mounted on a metal ground plane.
Approval	FCC, ISED, RED, UKCA, MIC, KCC, ANATEL, RCM, NCC, and ICASA

GW.59.3153	
Manufacturer	Taoglas
Gain	2.37 dBi (2.4 GHz), 2.93 dBi (5 GHz)
Impedance	50 Ω
Size	156 mm (Straight)
Type	½ wave monopole dual-band antenna
Polarization	Vertical
Connector	Reverse Polarity SMA plug (inner thread and pin receptacle)
Comment	To be mounted on the U.FL to Reverse Polarity SMA adapter cable. For optimal performance this antenna should be mounted on a metal ground plane. This antenna may only be used for host devices subject to professional installation or the integrator permanently attaches this external antenna to the adaptor cable plug in the host

	device by loctite, super glue etc. so that the antenna cannot be replaced by the end user.
Approval	FCC, ISED, RED, UKCA, MIC, KCC, ANATEL, RCM, NCC, and ICASA

8 Product testing

8.1 u-blox in-line production testing

As part of our focus on high quality products, u-blox maintain stringent quality controls throughout the production process. This means that all units in our manufacturing facilities are fully tested and that any identified defects are carefully analyzed to improve future production quality.

The Automatic test equipment (ATE) deployed in u-blox production lines logs all production and measurement data – from which a detailed test report for each unit can be generated. Figure 21 shows the ATE typically used during u-blox production.

u-blox in-line production testing includes:

- Digital self-tests (firmware download, MAC address programming)
- Measurement of voltages and currents
- Functional tests (host interface communication)
- Digital I/O tests
- Measurement and calibration of RF characteristics in all supported bands, including RSSI calibration, frequency tuning of reference clock, calibration of transmitter power levels, etc.
- Verification of Wi-Fi and Bluetooth RF characteristics after calibration, like modulation accuracy, power levels, and spectrum, are checked to ensure that all characteristics are within tolerance when the calibration parameters are applied.

Figure 21: Automatic test equipment for module test

8.2 OEM manufacturer production test

As all u-blox products undergo thorough in-series production testing prior to delivery, OEM manufacturers don't need to repeat any firmware tests or measurements that might otherwise be necessary to confirm RF performance. Testing over analog and digital interfaces is also unnecessary during an OEM production test.

OEM manufacturer testing should ideally focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damage the module components
  - All module pins are well soldered on application board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

In addition to this testing, OEMs can also perform other dedicated tests to check the device. For example, the measurement of module current consumption in a specified operating state can identify a short circuit if the test result deviates that from that taken against a "Golden Device".

The standard operational module firmware and test software on the host can be used to perform functional tests (communication with the host controller, check interfaces) and perform basic RF performance testing. Special manufacturing firmware can also be used to perform more advanced RF performance tests.

8.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test compares the signal quality of the Device under Test (DUT) with that of "Golden Device" in a location with a known signal quality. This test can be performed after establishing a connection with an external device.

A very simple test can be performed by just scanning for a known Bluetooth low energy device and checking that the signal level (Received Signal Strength Indicator (RSSI) is acceptable.

☞ Tests of this kind may be useful as a "go/no go" test but are not appropriate for RF performance measurements.

Go/No go tests are suitable for checking communication between the host controller and the power supply. The tests can also confirm that all components on the DUT are well soldered.

A basic RF functional test of the device that includes the antenna can be performed with standard Bluetooth low energy devices configured as remote stations. In this scenario, the device containing IRIS-W1 and the antennas should be arranged in a fixed position inside an RF shield box. The shielding prevents interference from other possible radio devices to ensure stable test results.

Appendix

A Wi-Fi transmit output power limits

All power settings apply to the IRIS-W101 and IRIS-W106 unless otherwise noted.

A.1 FCC / ISED regulatory domain

Table 23 through Table list the maximum allowable conducted[13] output power limits for operation in the FCC/ISED regulatory domains.

A.1.1 FCC / ISED Wi-Fi output power for 2.4 GHz band

The output power limits are for use with a max allowed antenna gain of 3 dBi.

Mode	Channel(s)	Maximum power setting (IRIS-W101)	Maximum power setting (IRIS-W106)
802.11b	1	17 dBm	17 dBm
	2 – 10	17 dBm	17 dBm
	11	15.5 dBm	15.5 dBm
802.11g	1, 9, 10	14 dBm	14 dBm
	2 – 4	15 dBm	15 dBm
	5 – 8	16 dBm	16 dBm
	11	13 dBm	13 dBm
802.11n	1, 9, 11	11 dBm	11 dBm
	2, 10	12 dBm	12 dBm
	3, 8	13 dBm	13 dBm
	4, 5, 7	14 dBm	14 dBm
	6	15.5 dBm	15.5 dBm
802.11ac	1, 9, 11	11 dBm	11 dBm
	2, 10	12 dBm	12 dBm
	3, 8	13 dBm	13 dBm
	4, 5, 7	14 dBm	14 dBm
	6	15.5 dBm	15.5 dBm
802.11ax	1, 9, 11	11 dBm	11 dBm
	2, 10	12 dBm	12 dBm
	3, 8	13 dBm	13 dBm
	4, 5, 7	14 dBm	14 dBm
	6	15.5 dBm	15.5 dBm
802.11ax RU	1, 9, 10	11.5 dBm	11.5 dBm
	2, 4	12.5 dBm	12.5 dBm
	3, 5, 8	13.5 dBm	13.5 dBm
	6, 7	14.5 dBm	14.5 dBm
	11	11 dBm	11 dBm

Table 23: FCC / ISED Wi-Fi power table for operation in the 2.4 GHz band

[13] Output power at the antenna connector, without antenna gain.

A.1.2 FCC / ISED Wi-Fi output power for 5 GHz band

The output power limits are for use with a max allowed antenna gain of 3.4 dBi.

Mode	Channel(s)	Maximum power setting (IRIS-W101)	Maximum power setting (IRIS-W106)
802.11a	100	13 dBm	13 dBm
	36, 64, 104	16 dBm	16 dBm
	40 – 60, 108 – 140, 149 – 165	17 dBm	17 dBm
802.11n	100	13 dBm	13 dBm
	36, 64, 104	16 dBm	16 dBm
	40 – 60, 108 – 140, 149 – 165	17 dBm	17 dBm
802.11ac	100	13 dBm	13 dBm
	36, 64, 104	16 dBm	16 dBm
	40 – 60, 108 – 140, 149 – 165	17 dBm	17 dBm
802.11ax	100	13 dBm	13 dBm
	36, 64, 104	16 dBm	16 dBm
	40 – 60, 108 – 140, 149 – 165	17 dBm	17 dBm
802.11ax RU	36 – 48	13 dBm	13 dBm
	52 – 64	14 dBm	14 dBm
	100 – 140	11 dBm	11 dBm
	149 – 165	17 dBm	17 dBm

Table 24: FCC Wi-Fi power table for operation in the 5 GHz bands

A.2 RED and UKCA regulatory domains

Table and Table list the maximum allowable conducted[13] output power limits for operation in the RED and UKCA regulatory domains.

A.2.1 Wi-Fi output power for 2.4 GHz band

The output power limits are for use with a max allowed antenna gain of 3 dBi.

Mode	Channel(s)	Maximum power setting (IRIS-W101)	Maximum power setting (IRIS-W106)
802.11b	1	17 dBm	17 dBm
	2 – 10	17 dBm	17 dBm
	11	15.5 dBm	15.5 dBm
802.11g	1, 9, 10	14 dBm	14 dBm
	2 – 4	15 dBm	15 dBm
	5 – 8	16 dBm	16 dBm
	11	13 dBm	13 dBm
802.11n	1, 9, 11	11 dBm	11 dBm
	2, 10	12 dBm	12 dBm
	3, 8	13 dBm	13 dBm
	4, 5, 7	14 dBm	14 dBm
	6	15.5 dBm	15.5 dBm
802.11ac	1, 9, 11	11 dBm	11 dBm
	2, 10	12 dBm	12 dBm
	3, 8	13 dBm	13 dBm
	4, 5, 7	14 dBm	14 dBm
	6	15.5 dBm	15.5 dBm
802.11ax	1, 9, 11	11 dBm	11 dBm
	2, 10	12 dBm	12 dBm
	3, 8	13 dBm	13 dBm
	4, 5, 7	14 dBm	14 dBm
	6	15.5 dBm	15.5 dBm
802.11ax RU	1, 9, 10	11.5 dBm	11.5 dBm
	2, 4	12.5 dBm	12.5 dBm
	3, 5, 8	13.5 dBm	13.5 dBm
	6, 7	14.5 dBm	14.5 dBm
	11	11 dBm	11 dBm

Table 25: RED Wi-Fi power table for operation in the 2.4 GHz band

A.2.2 Wi-Fi output power for 5 GHz band

The output power limits are for use with a max allowed antenna gain of 3.4 dBi.

Mode	Channel(s)	Maximum power setting (IRIS-W101)	Maximum power setting (IRIS-W106)
802.11a	100	13 dBm	13 dBm
	36, 64, 104	16 dBm	16 dBm
	40 – 60, 108 – 140	17 dBm	17 dBm
	149 – 165	10 dBm	10 dBm
802.11n	100	13 dBm	13 dBm
	36, 64, 104	16 dBm	16 dBm
	40 – 60, 108 – 140	16 dBm	16 dBm
	149 – 165	10 dBm	10 dBm
802.11ac	100	13 dBm	13 dBm
	36, 64, 104	16 dBm	16 dBm
	40 – 60, 108 – 140	16 dBm	16 dBm
	149 – 165	10 dBm	10 dBm
802.11ax	100	13 dBm	13 dBm
	36, 64, 104	16 dBm	16 dBm
	40 – 60, 108 – 140	16 dBm	16 dBm
	149 – 165	10 dBm	10 dBm
802.11ax RU	36 – 48	13 dBm	13 dBm
	52 – 64	14 dBm	14 dBm
	100 – 140	11 dBm	11 dBm
	149 – 165	10 dBm	10 dBm

Table 26: RED Wi-Fi power table for operation in the 5 GHz bands

B Antenna reference designs

Designers can take full advantage of IRIS-W10's Single-Modular Transmitter certification approval by integrating the u-blox reference design into their products. This approach requires compliance with the following rules:

- Only listed antennas can be used. Refer to the list of Pre-approved antennas.
- Schematics and parts used in the design must be identical to the reference design. Use only parts validated by u-blox for antenna matching.
- PCB layout must be identical to the one provided by u-blox. Implement one of the reference designs described in this section or contact u-blox.
- The designer must use the PCB stack-up provided by u-blox. RF traces on the carrier PCB are part of the certified design.

When using the IRIS-W101 with this antenna reference design, the circuit trace layout must be made in strict compliance with the antenna reference design described in this appendix.

B.1 Reference design for external antennas (U.FL connector)

The reference design uses a U.FL micro-coaxial connector to connect the external antenna via a 50 Ω coaxial cable. Figure 22 shows the placement of the connector in relation and module footprint. The components connected to the RF trace must be kept as shown in the reference design.

Figure 22: U.FL connector placement (left) and module footprint (right)

B.1.1 Floor plan

Figure 23 and Figure 24 show the critical components and positioning of the copper traces in the reference design. The itemized references are described in Table 24.

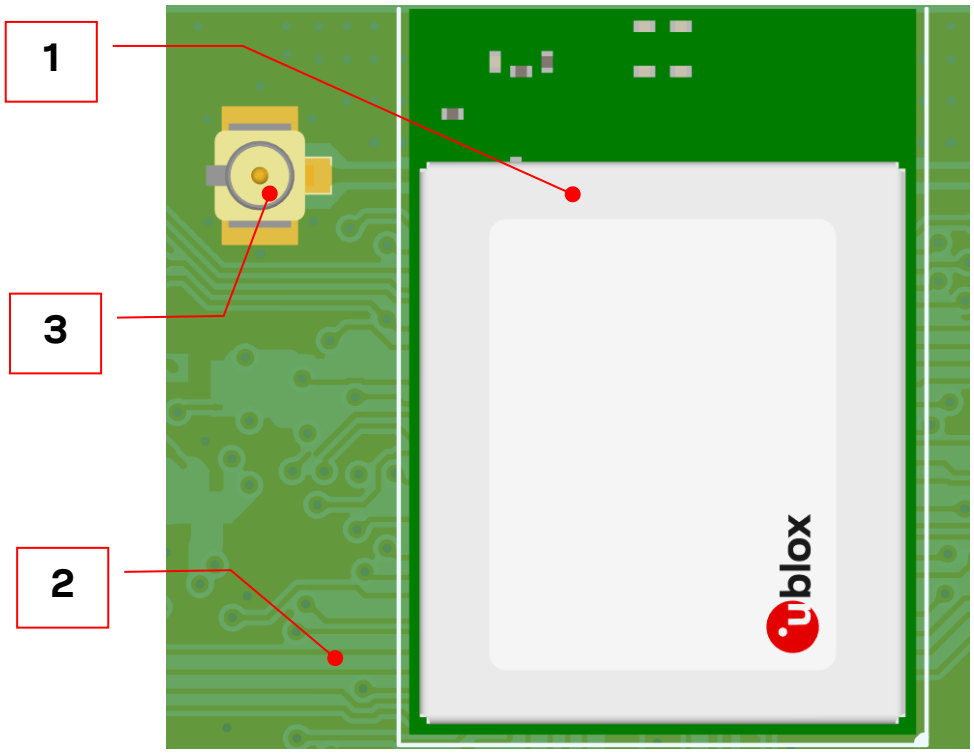


Figure 23: IRIS-W101 antenna reference design - 1

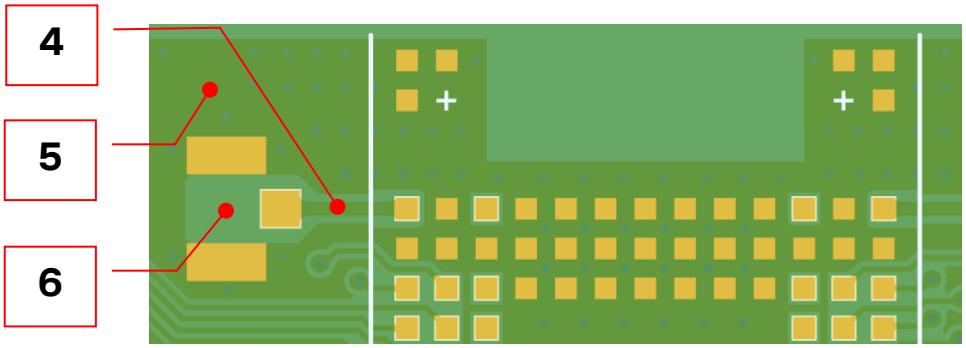


Figure 24: IRIS-W101 antenna reference design – 2

Reference	Part	Manufacturer	Description
1	IRIS-W101	u-blox	IRIS-W10 module with antenna pin
2	Carrier PCB		Should have a solid GND inner layer underneath and around the RF components (vias and small openings are allowed)
3	U.FL-R-SMT-1(10)	Hirose	Coaxial connector, 0 – 6 GHz, for external antennas
4	RF trace		Antenna coplanar microstrip, matched to 50 Ω
5	GND trace		Minimum required top layer GND-trace. See also All dimensions are shown in mm Figure 26.
6	Copper keep-out		Keep this area free from any copper on the top layer

Table 247: Antenna reference design – item descriptions

B.1.2 RF trace specification

The 50 Ω coplanar micro-strip dimensions used in the reference design are shown in Figure 25 and described in Table 2. GND stitching vias should be used around the RF trace to ensure a proper GND connection. No other components are allowed within this area.

The solid GND layer beneath the "top layer" shall surround at least the entire RF trace and connector. No signal traces are allowed to be routed on the GND layer within this area but vias and small openings are allowed.

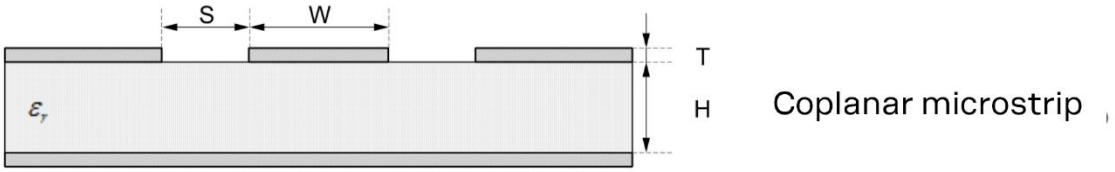


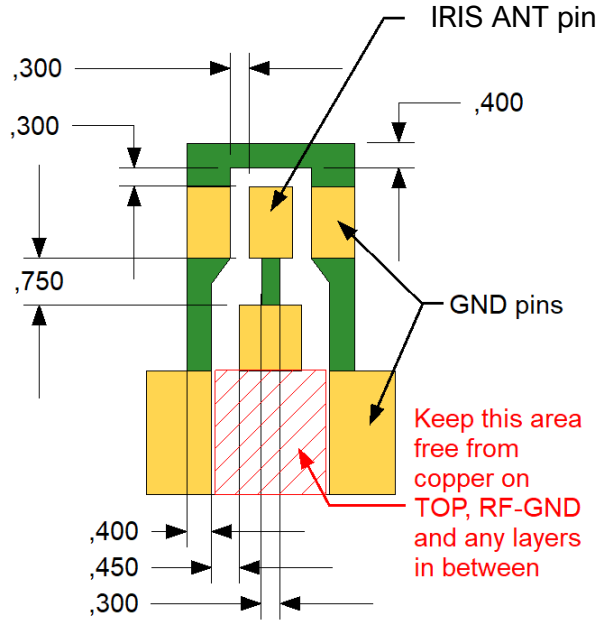
Figure 25: Coplanar micro-strip dimension specification

Reference	Item	Value
S	Spacing	200 +/- 50 µm
W	Conductor width	300 +/- 30 µm (match as close to 50 Ω as possible)
T	Copper and plating/surface coating thickness	35 +/- 15 µm
H	Conductor height	150 +/- 20 µm
ε_r	Dielectric constant (relative permittivity)	3.77 +/- 0.5 @ 2 GHz

Table 28: Coplanar micro-strip specification

☞ The GND spacing requirements of the IRIS ANT and U.FL connector RF pins are greater than the spacing requirement of a 50 Ω coplanar microstrip. However, when using the conductor width and height specified in Table 2, the increased spacing to GND does not significantly affect the trace impedance for short trace lengths. Therefore, the impedance is still close to 50 Ω.

Figure 26 shows the **ANT** and **GND** pins, with the dimensions of the U.FL connector, and the copper-free area on RF-GND.



All dimensions are shown in mm

Figure 26: RF trace and minimum required GND trace of the U.FL antenna connector reference design

C Glossary

Abbreviation	Definition
ABS	Acrylonitrile butadiene styrene
ADC	Analog to Digital Converter
ATE	Automatic Test Equipment
LE	Bluetooth Low Energy
CTS	Clear To Send
DCX	Data/Command Signal
DFU	Device Firmware Update
DDR	Dual-Data Rate
DUT	Device Under Test
EMC	Electro Magnetic Compatibility
EMI	Electro Magnetic Interference
ESD	Electro Static Discharge
FCC	Federal Communications Commission
GATT	Generic ATTribute profile
GND	Ground
GPIO	General Purpose Input/Output
I2C	Inter-Integrated Circuit
I2S	Inter-IC sound interface
IDE	Integrated Development Environment
IEEE	Institute of Electrical and Electronics Engineers
LDO	Low Drop Out
LED	Light-Emitting Diode
MAC	Media Access Control
MISO	Master Input, Slave Output
MOSI	Master Output, Slave Input
MSL	Moisture Sensitivity Level
NFC	Near Field Communication
NSMD	Non Solder Mask Defined
PCB	Printed Circuit Board
PIFA	Planar Inverted-F Antenna
PC	Polycarbonate
QDEC	Quadrature DECoder
QSPI	Quad Serial Peripheral Interface
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RSSI	Received Signal Strength Indicator
RTS	Request to Send
RXD	Receive Data
SCL	Signal Clock
SWD	Serial Wire Debug
SDL	Specification and Description Language
SMA	SubMiniature version A

Abbreviation	Definition
SMD	Solder Mask Defined
SMPS	Switching Mode Power Supply
SMT	Surface-Mount Technology
SPI	Serial Peripheral Interface
SWD	Serial Wire Debug
Thread	Networking protocol for Internet of Things (IoT) "smart" home automation devices to communicate on a local wireless mesh network
THT	Through-Hole Technology
TRP	Total Radio Power
TXD	Transmit Data
UART	Universal Asynchronous Receiver/Transmitter
UICR	User Information Configuration Registers
USB	Universal Serial Bus
VCC	IC power-supply pin
VSWR	Voltage Standing Wave Ratio
Zigbee	Open standard protocol, full-stack solution for a majority of large smart home ecosystem providers

Table 25: Explanation of the abbreviations and terms used

Related documentation

[1] IRIS-W10 product summary, UBX-23000279
[2] IRIS-W10 data sheet, UBX-23002331
[3] EVK-IRIS-W1 user guide, UBX-23007837
[4] JEDEC J-STD-020C - Moisture/Reflow Sensitivity Classification for Non Hermetic Solid State Surface Mount Devices
[5] IEC EN 61000-4-2 - Electromagnetic compatibility (EMC) - Part 4-2: Testing and measurement techniques – Electrostatic discharge immunity test
[6] ETSI EN 301 489-1 - Electromagnetic compatibility and Radio spectrum Matters (ERM); ElectroMagnetic Compatibility (EMC) standard for radio equipment and services; Part 1: Common technical requirements
[7] IEC61340-5-1 - Protection of electronic devices from electrostatic phenomena – General requirements
[8] ETSI EN 60950-1:2006 - Information technology equipment – Safety – Part 1: General requirements
[9] FCC Regulatory Information – Title 47 - Telecommunications
[10] FCC guidance 594280 D01 Configuration Control v02 r01,
[11] FCC guidance 594280 D02 U-NII Device Security v01r03
[12] NXP blhost User Manual (login required)
[13] u-blox shortrange open CPU GitHub repository, https://github.com/u-blox/u-blox-sho-OpenCPU
[14] Product packaging guide, UBX-14001652
[15] IRIS-W10 EU Declaration of Conformity (TBC)
[16] IRIS-W10 UKCA Declaration of Conformity (TBC)
[17] MCUXpresso SDK, https://www.nxp.com/design/designs/mcuxpresso-software-development-kit-sdk:MCUXpresso-SDK
[18] MCUXpresso SDK Builder, https://mcuxpresso.nxp.com/en/welcome
[19] MCUXpresso IDE, https://www.nxp.com/design/software/development-software/mcuxpresso-software-and-tools-/mcuxpresso-integrated-development-environment-ide:MCUXpresso-IDE
[20] Arm GNU Toolchain, https://developer.arm.com/Tools%20and%20Software/GNU%20Toolchain
[21] CMake software, https://cmake.org/download/
[22] IAR Embedded Workbench for ARM: https://www.iar.com/products/architectures/arm/iar-embedded-workbench-for-arm/
[23] GNU Compiler Collection (GCC): https://gcc.gnu.org/install/
[24] NXP RW610 User Manual (UM11799) (login required): https://www.nxp.com/products/wireless/wi-fi-plus-bluetooth-plus-802-15-4/wireless-mcu-with-integrated-radiobr-1x1-wi-fi-6-plus-bluetooth-low-energy-5-3-radios:RW610
[25] NXP RW610 User Manual (UM11798)(login required): https://www.nxp.com/products/wireless/wi-fi-plus-bluetooth-plus-802-15-4/wireless-mcu-with-integrated-radiobr-1x1-wi-fi-6-plus-bluetooth-low-energy-5-3-radios:RW610
[26] Getting Started with MCUXpresso SDK, MCUXSDKGSUG

☞ For product change notifications and regular updates of u-blox documentation, register on our website, www.u-blox.com.

Revision history

Revision	Date	Name	Comments
R01	28-Mar-2023	lber, tpat	Initial release
R02	21-Sep-2023	lber, tpat	Deleted pin list, product features list, and table data describing country code approvals status (with all relevant content now maintained in data sheet). Added General requirements for qualification and approval. Moved information describing the potting and conformal coating to Other remarks. Updated module configuration ordering codes in Table 1: Module configurations ordering codes. Revised flashing instructions to describe EVK-IRIS-W10 flashing over MCULINK (USB-C) port using the SWD interface. Added Flashing over the JTAG interface, and blhost application sections. Revised number of USARTs in Universal synchronous asynchronous serial interface (USART) and updated design recommendations in Antenna interface.
R03	16-10-2023	lber, hisa, ovik	Updated the pre-approved antenna list. Updated the regulatory statements for EU. Moved Internal antenna (IRIS-W106 to section 2. Added Antenna reference design (IRIS-W101 and Module footprint and paste mask sections. Updated table data describing Boot strapping pins and options in Configuration pins section. Removed country code approvals status and pending Bluetooth statement (maintained in data sheet). Added General requirements for qualification and approval. Included other minor editorial changes throughout the document. Removed figure in section 2.9 and referenced EVK User guide instead.
R04	23-10-2023	hisa	Updated document status to Public. Added note about MCUXpresso SDK and tools support for RW612 in Open CPU software.
R05	31-05-2024	hisa, ovik, kbhi, lkis	Updated IRIS-W1 images. Updated antenna list in ch 7.2.1. Added ordering codes for 10B and 30B. Added Antenna reference designs. Added Wi-Fi transmit output power limits.

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