CELLULAR

LARA-R2 series

LTE Cat 1 / EGPRS modules

System Integration Manual

Abstract

This document describes the features and the system integration of LARA-R2 series multi-mode cellular modules.

These modules are a complete, cost efficient and performance optimized LTE Cat 1 / 2G multi-mode solution covering up to three LTE bands and up to two 2G GSM/EGPRS bands in the very small and compact LARA form factor.

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Document status explanation	
Objective Specification	Document contains target values. Revised and supplementary data will be published later.
Advance Information	Document contains data based on early testing. Revised and supplementary data will be published later.
Early Production Information	Document contains data from product verification. Revised and supplementary data may be published later.
Production Information	Document contains the final product specification.

This document applies to the following products:

Name	Type number	Modem version	Application version	SDN / IN / PCN
LARA-R204	LARA-R204-02B-00	TBD	TBD	TBD
LARA-R211	LARA-R211-02B-00	30.17	A01.00	UBX-16024242

Preface

u-blox Technical Documentation

As part of our commitment to customer support, u-blox maintains an extensive volume of technical documentation for our products. In addition to our product-specific technical data sheets, the following manuals are available to assist u-blox customers in product design and development.

- **AT Commands Manual:** This document provides the description of the AT commands supported by the u-blox cellular modules.
- **System Integration Manual:** This document provides the description of u-blox cellular modules' system from the hardware and the software point of view, it provides hardware design guidelines for the optimal integration of the cellular modules in the application device and it provides information on how to set up production and final product tests on application devices integrating the cellular modules.
- **Application Notes:** These documents provide guidelines and information on specific hardware and/or software topics on u-blox cellular modules. See Related documents for a list of application notes related to your cellular module.

How to use this Manual

The LARA-R2 series System Integration Manual provides the necessary information to successfully design in and configure these u-blox cellular modules.

This manual has a modular structure. It is not necessary to read it from the beginning to the end.

The following symbols are used to highlight important information within the manual:

☞ An index finger points out key information pertaining to module integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the module.**

Questions

If you have any questions about u-blox cellular Integration:

- Read this manual carefully.
- Contact our information service on the homepage http://www.u-blox.com

Technical Support

Worldwide Web

Our website (http://www.u-blox.com) is a rich pool of information. Product information and technical documents can be accessed 24h a day.

By E-mail

If you have technical problems or cannot find the required information in the provided documents, contact the closest Technical Support office. To ensure that we process your request as soon as possible, use our service pool email addresses rather than personal staff email addresses. Contact details are at the end of the document.

Helpful Information when Contacting Technical Support

When contacting Technical Support, have the following information ready:

- Module type (e.g. LARA-R204) and firmware version
- Module configuration
- Clear description of your question or the problem
- A short description of the application
- Your complete contact details

Contents

1 System description

1.1 Overview

The LARA-R2 series comprises LTE Cat 1 / 2G multi-mode modules supporting up to three LTE bands and up to two 2G GSM/(E)GPRS bands for voice and/or data transmission in the very small LARA LGA form-factor (26.0 x 24.0 mm), easy to integrate in compact designs:

- LARA-R204 is designed primarily for operation in North America (on Verizon network)
- LARA-R211 is designed primarily for operation in Europe, Asia and other countries

LARA-R2 series modules are form-factor compatible with u-blox SARA, LISA and TOBY cellular module families: this facilitates easy migration from u-blox GSM/GPRS, CDMA, UMTS/HSPA, and LTE high data rate modules, maximizes the investments of customers, simplifies logistics, and enables very short time-to-market.

The modules are ideal for applications that are transitioning to LTE from 2G and 3G, due to the long term availability and scalability of LTE networks.

With a range of interface options and an integrated IP stack, the modules are designed to support a wide range of data-centric applications. The unique combination of performance and flexibility make these modules ideally suited for medium speed M2M applications, such as smart energy gateways, remote access video cameras, digital signage, telehealth and telematics.

LARA-R2 series modules support Voice over LTE (VoLTE) and voice service over 2G (CSFB) for applications that require voice, such as security and surveillance systems.

Table 1 summarizes the main features and interfaces of LARA-R2 series modules.

Model	Region	Radio Access Technology		Positioning			Interfaces						Audio		Features									Grade		
		LTE Bands	GSM Bands	GNSS via modem	Assist Now Software	CellLocate®	UART	USB 2.0	HSIC	SDIO	DDC (I^2C)	GPIOs	Analog audio	Digital audio	Network indication	Antenna supervisor	Rx Diversity	Jamming detection	Embedded TCP/UDP stack	Embedded HTTP,FTP,SSL	FOTA	eCall / ERA GLONASS	Dual stack IPv4/IPv6	Standard	Professional	Automotive
LARA-R204	North America	4,13		•	•	•	•	•	•	•	•	•		•	•	•	•	•	•	•	•		•		■	
LARA-R211	Europe, APAC	3,7,20	900,1800	•	•	•	•	•	•	•	•	•		•	•	•	•	•	•	•	•	•	•		■	

Table 1: LARA-R2 series main features summary

Table 2 reports a summary of cellular radio access technologies characteristics of LARA-R2 series modules.

4G LTE	2G GSM/GPRS/EDGE
3GPP Release 9 Long Term Evolution (LTE) Evolved Uni.Terrestrial Radio Access (E-UTRA) Frequency Division Duplex (FDD) DL Rx diversity	3GPP Release 9 Enhanced Data rate GSM Evolution (EDGE) GSM EGPRS Radio Access (GERA) Time Division Multiple Access (TDMA) DL Advanced Rx Performance

Band support[1]:
• LARA-R204:
  • Band 13 (750 MHz)
  • Band 4 (1700 MHz)
• LARA-R211:
  • Band 20 (800 MHz)
  • Band 3 (1800 MHz)
  • Band 7 (2600 MHz)
	Band support:
	• LARA-R211:
	  • E-GSM 900 MHz
	  • DCS 1800 MHz

LTE Power Class • Power Class 3 (23 dBm)	GSM/GPRS (GMSK) Power Class • Power Class 4 (33 dBm) for E-GSM band • Power Class 1 (30 dBm) for DCS band EDGE (8-PSK) Power Class Power Class E2 (27 dBm) for E-GSM band • Power Class E2 (26 dBm) for DCS band
Data rate • LTE category 1: up to 10.3 Mb/s DL, 5.2 Mb/s UL	Data Rate[2] • GPRS multi-slot class 12[3], CS1-CS4, up to 85.6 kb/s DL/UL • EDGE multi-slot class 12[3], MCS1-MCS9, up to 236.8 kb/s DL/UL

Table 2: LARA-R2 series LTE and 2G characteristics

LARA-R2 modules provide Voice over LTE (VoLTE) as well as Circuit-Switched-Fall-Back (CSFB) audio capability[4].

[1] LARA-R2 series modules support all the E-UTRA channel bandwidths for each operating band according to 3GPP TS 36.521-1 .
[2] GPRS/EDGE multi-slot class determines the number of timeslots available for upload and download and thus the speed at which data can be transmitted and received, with higher classes typically allowing faster data transfer rates.
[3] GPRS/EDGE multi-slot class 12 implies a maximum of 4 slots in DL (reception) and 4 slots in UL (transmission) with 5 slots in total.
[4] Not supported by LARA-R204 module "02" product version.

1.2 Architecture

Figure 1 summarizes the internal architecture of LARA-R2 series modules.

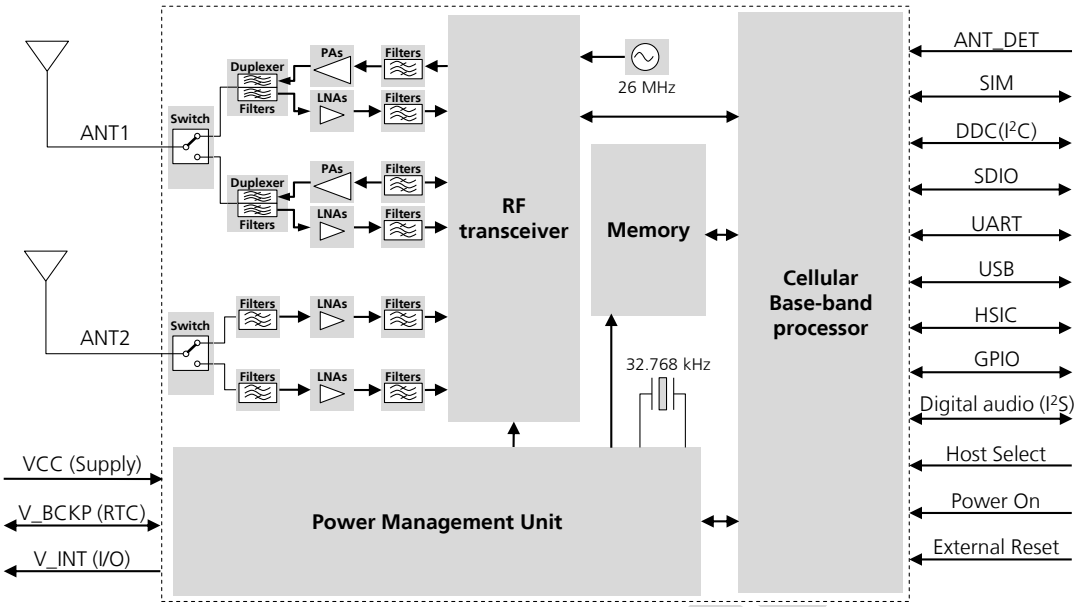


Figure 1: LARA-R2 series modules simplified block diagram

LARA-R2 series modules internally consists of the RF, Baseband and Power Management sections here described with more details than the simplified block diagrams of Figure 1.

RF section

The RF section is composed of RF transceiver, PAs, LNAs, crystal oscillator, filters, duplexers and RF switches.

Tx signal is pre-amplified by RF transceiver, then output to the primary antenna input/output port (**ANT1**) of the module via power amplifier (PA), SAW band pass filters band, specific duplexer and antenna switch.

Dual receiving paths are implemented according to LTE Receiver Diversity radio technology supported by the modules as LTE category 1 User Equipments: incoming signal is received through the primary (**ANT1**) and the secondary (**ANT2**) antenna input ports which are connected to the RF transceiver via specific antenna switch, diplexer, duplexer, LNA, SAW band pass filters.

- RF transceiver performs modulation, up-conversion of the baseband I/Q signals for Tx, down-conversion and demodulation of the dual RF signals for Rx. The RF transceiver contains:
  - Single chain high linearity receivers with integrated LNAs for multi band multi mode operation,
  - Highly linear RF demodulator / modulator capable GMSK, 8-PSK, QPSK, 16-QAM,
  - RF synthesizer,
  - VCO.
- Power Amplifiers (PA) amplify the Tx signal modulated by the RF transceiver
- RF switches connect primary (**ANT1**) and secondary (**ANT2**) antenna ports to the suitable Tx / Rx path
- SAW duplexers and band pass filters separate the Tx and Rx signal paths and provide RF filtering
- 26 MHz voltage-controlled temperature-controlled crystal oscillator generates the clock reference in active-mode or connected-mode.

Baseband and power management section

The Baseband and Power Management section is composed of the following main elements:

- A mixed signal ASIC, which integrates
  - Microprocessor for control functions
  - DSP core for cellular Layer 1 and digital processing of Rx and Tx signal paths
  - Memory interface controller
  - Dedicated peripheral blocks for control of the USB, SIM and generic digital interfaces
  - Interfaces to RF transceiver ASIC
- Memory system, which includes NAND flash and LPDDR2 RAM
- Voltage regulators to derive all the subsystem supply voltages from the module supply input **VCC**
- Voltage sources for external use: **V_BCKP** and **V_INT**
- Hardware power on
- Hardware reset
- Low power idle-mode support
- 32.768 kHz crystal oscillator to provide the clock reference in the low power idle-mode, which can be set by enable power saving configuration using the AT+UPSV command.

1.3 Pin-out

Table 3 lists the pin-out of the LARA-R2 series modules, with pins grouped by function.

Function	Pin Name	Pin No	I/O	Description	Remarks
Power	**VCC**	51, 52, 53	I	Module supply input	**VCC** supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for description and requirements. See section 2.2.1 for external circuit design-in.
	GND	1, 3, 5, 14, 20, 22, 30, 32, 43, 50, 54, 55, 57, 58, 60, 61, 63, 64, 65-96	N/A	Ground	**GND** pins are internally connected each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1 for functional description. See section 2.2.1 for external circuit design-in.
	V_BCKP	2	I/O	RTC supply input/output	**V_BCKP** = 1.8 V (typical) generated by internal regulator when valid **VCC** supply is present. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in.
	V_INT	4	O	Generic Digital Interfaces supply output	**V_INT** = 1.8 V (typical), generated by internal DC/DC regulator when the module is switched on. Test-Point for diagnostic access is recommended. See section 1.5.3 for functional description. See section 2.2.3 for external circuit design-in.
System	**PWR_ON**	15	I	Power-on input	Internal 10 kΩ pull-up resistor to **V_BCKP**. See section 1.6.1 for functional description. See section 2.3.1 for external circuit design-in.
	RESET_N	18	I	External reset input	Internal 10 kΩ pull-up resistor to **V_BCKP**. Test-Point for diagnostic access is recommended. See section 1.6.3 for functional description. See section 2.3.2 for external circuit design-in.
	HOST_SELECT	21	I/O	Selection of module / host configuration	Not supported by "02" product versions. Pin available to select, enable, connect, disconnect and subsequently re-connect the HSIC interface. Test-Point for diagnostic access is recommended. See section 1.6.4 for functional description. See section 2.3.3 for external circuit design-in.
Antenna	**ANT1**	56	I/O	Primary antenna	Main Tx / Rx antenna interface. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for description and requirements. See section 2.4 for external circuit design-in.
	ANT2	62	I	Secondary antenna	Rx only for Rx diversity. 50 Ω nominal characteristic impedance. Antenna circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.7 for description and requirements. See section 2.4 for external circuit design-in.
	ANT_DET	59	I	Input for antenna detection	ADC for antenna presence detection function. See section 1.7.2 for functional description. See section 2.4.2 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
SIM	**VSIM**	41	O	SIM supply output	**VSIM** = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	39	I/O	SIM data	Data input/output for 1.8 V / 3 V SIM Internal 4.7 kΩ pull-up to **VSIM**. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	38	O	SIM clock	3.25 MHz clock output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	40	O	SIM reset	Reset output for 1.8 V / 3 V SIM See section 1.8 for functional description. See section 2.5 for external circuit design-in.
UART	**RXD**	13	O	UART data output	1.8 V output, Circuit 104 (RXD) in ITU-T V.24, for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	TXD	12	I	UART data input	1.8 V input, Circuit 103 (TXD) in ITU-T V.24, for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. Internal active pull-up to **V_INT**. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	CTS	11	O	UART clear to send output	1.8 V output, Circuit 106 (CTS) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	10	I	UART ready to send input	1.8 V input, Circuit 105 (RTS) in ITU-T V.24. Internal active pull-up to **V_INT**. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	6	O	UART data set ready output	1.8 V output, Circuit 107 (DSR) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RI	7	O	UART ring indicator output	1.8 V output, Circuit 125 (RI) in ITU-T V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DTR	9	I	UART data terminal ready input	1.8 V input, Circuit 108/2 (DTR) in ITU-T V.24. Internal active pull-up to **V_INT**. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DCD	8	O	UART data carrier detect output	1.8 V input, Circuit 109 (DCD) in ITU-T V.24. Test-Point and series 0 Ω for diagnostic access recommended. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
USB	**VUSB_DET**	17	I	USB detect input	VBUS (5 V typical) USB supply generated by the host must be connected to this input pin to enable the USB interface. If the USB interface is not used by the Application Processor, Test-Point for diagnostic / FW update access is recommended See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	USB_D-	28	I/O	USB Data Line D-	USB interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 90 Ω nominal differential impedance (Z_0) 30 Ω nominal common mode impedance (Z_{CM}) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [9] are part of the USB pin driver and need not be provided externally. If the USB interface is not used by the Application Processor, Test-Point for diagnostic / FW update access is recommended See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
	USB_D+	29	I/O	USB Data Line D+	USB interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 90 Ω nominal differential impedance (Z_0) 30 Ω nominal common mode impedance (Z_{CM}) Pull-up or pull-down resistors and external series resistors as required by the USB 2.0 specifications [9] are part of the USB pin driver and need not be provided externally. If the USB interface is not used by the Application Processor, Test-Point for diagnostic / FW update access is recommended See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in.
HSIC	**HSIC_DATA**	99	I/O	HSIC USB data line	Not supported by "02" product versions. USB High-Speed Inter-Chip compliant interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 50 Ω nominal characteristic impedance. Test-Point for diagnostic / FW update access is recommended. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
	HSIC_STRB	100	I/O	HSIC USB strobe line	Not supported by "02" product versions. HSIC interface for AT commands, data communication, FOAT, FW update by u-blox EasyFlash tool and diagnostic. 50 Ω nominal characteristic impedance. Test-Point for diagnostic / FW update access is recommended. See section 1.9.3 for functional description. See section 2.6.3 for external circuit design-in.
DDC	**SCL**	27	O	I^2C bus clock line	1.8 V open drain, for communication with I2C-slave devices. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.
	SDA	26	I/O	I^2C bus data line	1.8 V open drain, for communication with I2C-slave devices. See section 1.9.4 for functional description. See section 2.6.4 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
SDIO	**SDIO_D0**	47	I/O	SDIO serial data [0]	Not supported by "02" product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D1	49	I/O	SDIO serial data [1]	Not supported by "02" product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D2	44	I/O	SDIO serial data [2]	Not supported by "02" product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_D3	48	I/O	SDIO serial data [3]	Not supported by "02" product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_CLK	45	O	SDIO serial clock	Not supported by "02" product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDIO_CMD	46	I/O	SDIO command	Not supported by "02" product versions. SDIO interface for communication with u-blox Wi-Fi module See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
Audio	**I2S_TXD**	35	O / I/O	I^2S transmit data / GPIO	I^2S transmit data output, alternatively configurable as GPIO. I^2S not supported by LARA-R204 module '02' product version. See sections 1.10 and 1.12 for functional description. See sections 2.7 and 2.8 for external circuit design-in.
	I2S_RXD	37	I / I/O	I^2S receive data / GPIO	I^2S receive data input, alternatively configurable as GPIO. I^2S not supported by LARA-R204 module '02' product version. See sections 1.10 and 1.12 for functional description. See sections 2.7 and 2.8 for external circuit design-in.
	I2S_CLK	36	I/O / I/O	I^2S clock / GPIO	I^2S serial clock, alternatively configurable as GPIO. I^2S not supported by LARA-R204 module '02' product version. See sections 1.10 and 1.12 for functional description. See sections 2.7 and 2.8 for external circuit design-in.
	I2S_WA	34	I/O / I/O	I^2S word alignment / GPIO	I^2S word alignment, alternatively configurable as GPIO. I^2S not supported by LARA-R204 module '02' product version. See sections 1.10 and 1.12 for functional description. See sections 2.7 and 2.8 for external circuit design-in.
Clock output	**GPIO6**	19	O	Clock output	1.8 V configurable clock output. See section 1.11 for functional description. See section 2.7 for external circuit design-in.

Function	Pin Name	Pin No	I/O	Description	Remarks
GPIO	**GPIO1**	16	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	GPIO2	23	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	GPIO3	24	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	GPIO4	25	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
	GPIO5	42	I/O	GPIO	1.8 V GPIO with alternatively configurable functions. See section 1.12 for functional description. See section 2.8 for external circuit design-in.
Reserved	**RSVD**	33	N/A	RESERVED pin	This pin must be connected to ground. See sections 1.13 and 2.9
	RSVD	31, 97, 98	N/A	RESERVED pin	Internally not connected. Leave unconnected. See sections 1.13 and 2.9

Table 3: LARA-R2 series modules pin definition, grouped by function

1.4 Operating modes

LARA-R2 series modules have several operating modes. The operating modes defined in Table 4 and described in detail in Table 5 provide general guidelines for operation.

General Status	Operating Mode	Definition
Power-down	**Not-Powered Mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-Off Mode	**VCC** supply within operating range and module is switched off.
Normal operation	**Idle-Mode**	Module processor core runs with 32 kHz reference generated by the internal oscillator.
	Active-Mode	Module processor core runs with 26 MHz reference generated by the internal oscillator.
	Connected-Mode	RF Tx/Rx data connection enabled and processor core runs with 26 MHz reference.

Table 4: Module operating modes definition

Mode	Description	Transition between operating modes
Not-Powered	Module is switched off. Application interfaces are not accessible.	When **VCC** supply is removed, the module enters not-powered mode. When in not-powered mode, the modules cannot be switched on by **PWR_ON**, **RESET_N** or RTC alarm. When in not-powered mode, the modules can be switched on applying **VCC** supply (see 2.3.1) so that the module switches from not-powered to active-mode.
Power-Off	Module is switched off: normal shutdown by an appropriate power-off event (see 1.6.2). Application interfaces are not accessible.	When the module is switched off by an appropriate power-off event (see 1.6.2), the module enters power-off mode from active-mode. When in power-off mode, the modules can be switched on by **PWR_ON**, **RESET_N** or RTC alarm (see 2.3.1): the module switches from power-off to active-mode. When in power-off mode, the modules enter not-powered mode by removing **VCC** supply.
Idle	Module is switched on with application interfaces temporarily disabled or suspended: the module is temporarily not ready to communicate with an external device by means of the application interfaces as configured to reduce the current consumption. The module enters the low power idle-mode whenever possible if power saving is enabled by AT+UPSV (see u-blox AT Commands Manual [2]) reducing power consumption (see 1.5.1.4). The **CTS** output line indicates when the UART interface is disabled/enabled due to the module idle/active-mode according to power saving and HW flow control settings (see 1.9.1.3, 1.9.1.4). Power saving configuration is not enabled by default: it can be enabled by AT+UPSV (see the u-blox AT Commands Manual [2]).	The module automatically switches from active-mode to idle-mode whenever possible if power saving is enabled (see sections 1.5.1.4, 1.9.1.4, 1.9.2.4 and to the u-blox AT Commands Manual [2], AT+UPSV command). The module wakes up from idle to active mode in the following events: • Automatic periodic monitoring of the paging channel for the paging block reception according to network conditions (see 1.5.1.3, 1.9.1.4) • Automatic periodic enable of the UART interface to receive and send data, if AT+UPSV=1 power saving is set (see 1.9.1.4) • Data received on UART interface, according to HW flow control (AT&K) and power saving (AT+UPSV) settings (see 1.9.1.4) • **RTS** input set ON by the host DTE, with HW flow control disabled and AT+UPSV=2 (see 1.9.1.4) • **DTR** input set ON by the host DTE, with AT+UPSV=3 (see 1.9.1.4) • USB detection, applying 5 V (typ.) to **VUSB_DET** input (see 1.9.2) • The connected USB host forces a remote wakeup of the module as USB device (see 1.9.2.4) • The connected u-blox GNSS receiver forces a wakeup of the cellular module using the GNSS Tx data ready function over the **GPIO3** pin (see 1.9.4) • The connected SDIO device forces a wakeup of the module as SDIO host (see 1.9.5) • RTC alarm occurs (see u-blox AT Commands Manual [2], +CALA)

Mode	Description	Transition between operating modes
Active	The module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by the AT+UPSV command (see sections 1.5.1.3, 1.9.1.4 and to the u-blox AT Commands Manual [2]).	When the module is switched on by an appropriate power-on event (see 2.3.1), the module enters active-mode from not-powered or power-off mode. If power saving configuration is enabled by the AT+UPSV command, the module automatically switches from active to idle-mode whenever possible and the module wakes up from idle to active-mode in the events listed above (see idle to active transition description). When a voice call or a data call is initiated, the module switches from active-mode to connected-mode.
Connected	A voice call or a data call is in progress. The module is ready to communicate with an external device by means of the application interfaces unless power saving configuration is enabled by the AT+UPSV command (see sections 1.5.1.3, 1.9.1.4 and the u-blox AT Commands Manual [2]).	When a data or voice connection is initiated, the module enters connected-mode from active-mode. Connected-mode is suspended if Tx/Rx data is not in progress, due to connected discontinuous reception and fast dormancy capabilities of the module and according to network environment settings and scenario. In such case, the module automatically switches from connected to active mode and then, if power saving configuration is enabled by the AT+UPSV command, the module automatically switches to idle-mode whenever possible. Vice-versa, the module wakes up from idle to active mode and then connected mode if RF Tx/Rx is necessary. When a data connection is terminated, the module returns to the active-mode.

Table 5: Module operating modes description

Figure 2 describes the transition between the different operating modes.

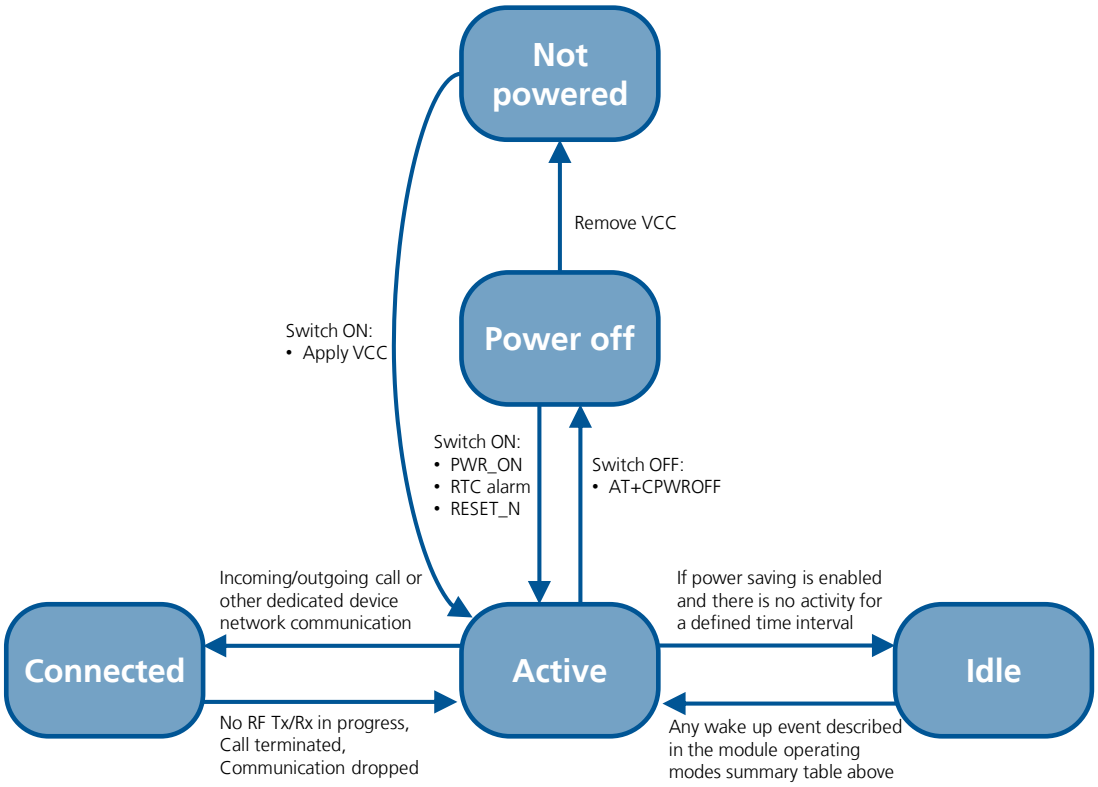


Figure 2: Operating modes transition

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

The **VCC** pins are internally connected to the RF power amplifier and to the integrated Power Management Unit: all supply voltages needed by the module are generated from the **VCC** supply by integrated voltage regulators, including **V_BCKP** Real Time Clock supply, **V_INT** digital interfaces supply and **VSIM** SIM card supply.

During operation, the current drawn by the LARA-R2 series modules through the **VCC** pins can vary by several orders of magnitude. This ranges from the pulse of current consumption during GSM transmitting bursts at maximum power level in connected-mode (as described in section 1.5.1.2) to the low current consumption during low power idle-mode with power saving enabled (as described in section 1.5.1.4).

LARA-R211 modules provide separate supply inputs over the three **VCC** pins:

- **VCC** pins #52 and #53 represent the supply input for the internal RF power amplifier, demanding most of the total current drawn of the module when RF transmission is enabled during a voice/data call
- **VCC** pin #51 represents the supply input for the internal baseband Power Management Unit and the internal transceiver, demanding minor part of the total current drawn of the module when RF transmission is enabled during a voice/data call

Figure 3 provides a simplified block diagram of LARA-R2 series modules internal VCC supply routing.

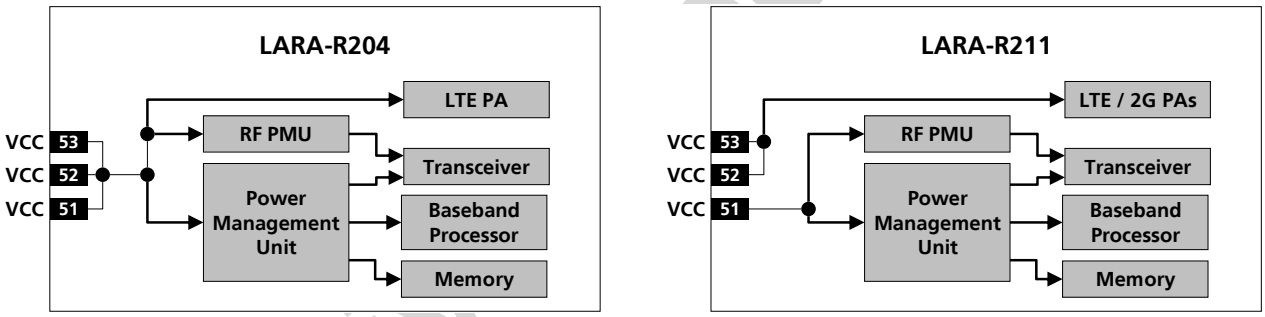


Figure 3: LARA-R2 series modules internal VCC supply routing simplified block diagram

1.5.1.1 VCC supply requirements

Table 6 summarizes the requirements for the **VCC** module supply. See section 2.2.1 for all the suggestions to properly design a **VCC** supply circuit compliant to the requirements listed in Table 6.

⚠ **VCC supply circuit affects the RF compliance of the device integrating LARA-R2 series modules with applicable required certification schemes as well as antenna circuit design. Compliance is guaranteed if the VCC requirements summarized in the Table 6 are fulfilled.**

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.30 V min. / 4.40 V max	RF performance is guaranteed when **VCC** PA voltage is inside the normal operating range limits. RF performance may be affected when **VCC** PA voltage is outside the normal operating range limits, though the module is still fully functional until the **VCC** voltage is inside the extended operating range limits.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.00 V min. / 4.50 V max	**VCC** voltage must be above the extended operating range minimum limit to switch-on the module. The module may switch-off when the **VCC** voltage drops below the extended operating range minimum limit. Operation above **VCC** extended operating range is not recommended and may affect device reliability.
VCC average current	Support with adequate margin the highest averaged **VCC** current consumption value in connected-mode conditions specified in LARA-R2 series Data Sheet [1]	The highest averaged **VCC** current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and **VCC** voltage. See 1.5.1.2, 1.5.1.3 for connected-mode current profiles.
VCC peak current	Support with margin the highest peak **VCC** current consumption value in connected-mode conditions specified in LARA-R2 series Data Sheet [1]	The specified highest peak of **VCC** current consumption occurs during GSM single transmit slot in 850/900 MHz connected-mode, in case of mismatched antenna. See 1.5.1.2 for 2G connected-mode current profiles.
VCC voltage drop during 2G Tx slots	Lower than 400 mV	**VCC** voltage drop directly affects the RF compliance with applicable certification schemes. Figure 5 describes **VCC** voltage drop during Tx slots.
VCC voltage ripple during 2G/LTE Tx	Noise in the supply has to be minimized	**VCC** voltage ripple directly affects the RF compliance with applicable certification schemes. Figure 5 describes **VCC** voltage ripple during Tx slots.
VCC under/over-shoot at start/end of Tx slots	Absent or at least minimized	**VCC** under/over-shoot directly affects the RF compliance with applicable certification schemes. Figure 5 describes **VCC** voltage under/over-shoot.

Table 6: Summary of VCC supply requirements

1.5.1.2 VCC current consumption in 2G connected-mode

When a GSM call is established, the **VCC** consumption is determined by the current consumption profile typical of the GSM transmitting and receiving bursts.

The current consumption peak during a transmission slot is strictly dependent on the transmitted power, which is regulated by the network. The transmitted power in the transmit slot is also the more relevant factor for determining the average current consumption.

If the module is transmitting in 2G single-slot mode (as in GSM talk mode) in the 850 or 900 MHz bands, at the maximum RF power control level (approximately 2 W or 33 dBm in the Tx slot/burst), the current consumption can reach an high peak / pulse (see LARA-R2 series Data Sheet [1]) for 576.9 µs (width of the transmit slot/burst) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/burst), so with a 1/8 duty cycle according to GSM TDMA (Time Division Multiple Access).

If the module is transmitting in 2G single-slot mode in the 1800 or 1900 MHz bands, the current consumption figures are quite less high than the one in the low bands, due to 3GPP transmitter output power specifications.

During a GSM call, current consumption is not so significantly high in receiving or in monitor bursts and it is low in the bursts unused to transmit / receive.

Figure 4 shows an example of the module current consumption profile versus time in GSM talk mode.

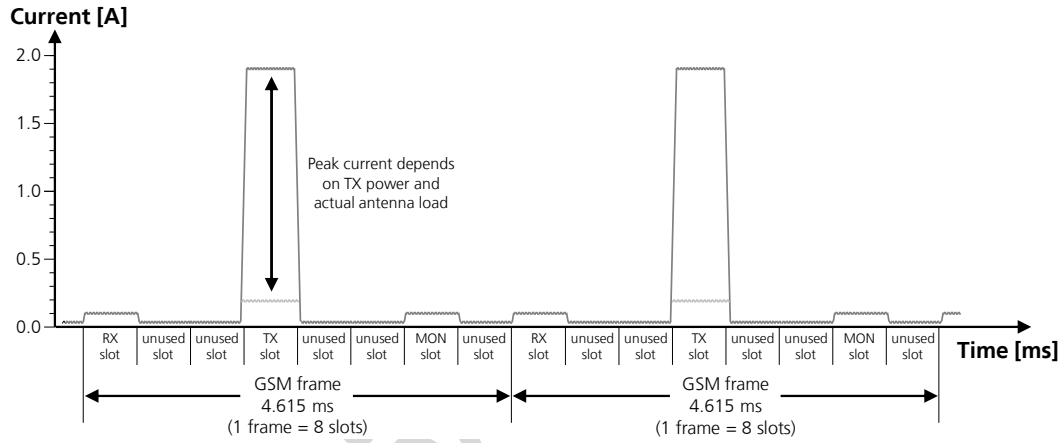


Figure 4: VCC current consumption profile versus time during a GSM call (1 TX slot, 1 RX slot)

Figure 5 illustrates **VCC** voltage profile versus time during a GSM call, according to the related **VCC** current consumption profile described in Figure 4.

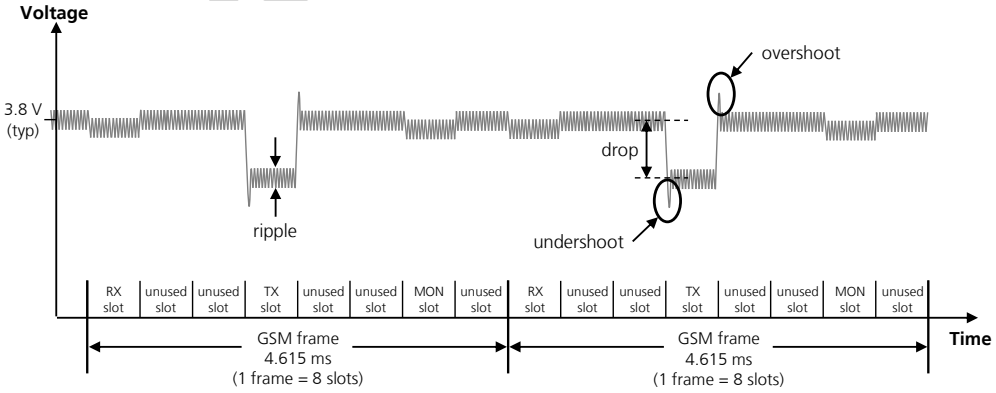


Figure 5: Description of the VCC voltage profile versus time during a GSM call (1 TX slot, 1 RX slot)

When a GPRS connection is established, more than one slot can be used to transmit and/or more than one slot can be used to receive. The transmitted power depends on network conditions, which set the peak current consumption, but following the 3GPP specifications the maximum Tx RF power is reduced if more than one slot is used to transmit, so the maximum peak of current is not as high as can be in case of a 2G single-slot call.

The multi-slot transmission power can be further reduced by configuring the actual Multi-Slot Power Reduction profile with the dedicated AT command, AT+UDCONF=40 (see the u-blox AT Commands Manual [2]).

If the module transmits in GPRS class 12 in the 850 or 900 MHz bands, at the maximum RF power control level, the current consumption can reach a quite high peak but lower than the one achievable in 2G single-slot mode. This happens for 2.307 ms (width of the 4 transmit slots/bursts) with a periodicity of 4.615 ms (width of 1 frame = 8 slots/bursts), so with a 1/2 duty cycle, according to 2G TDMA.

If the module is in GPRS connected mode in the 1800 or 1900 MHz bands, the current consumption figures are quite less high than the one in the low bands, due to 3GPP transmitter output power specifications.

Figure 6 reports the current consumption profiles in GPRS class 12 connected mode, in the 850 or 900 MHz bands, with 4 slots used to transmit and 1 slot used to receive.

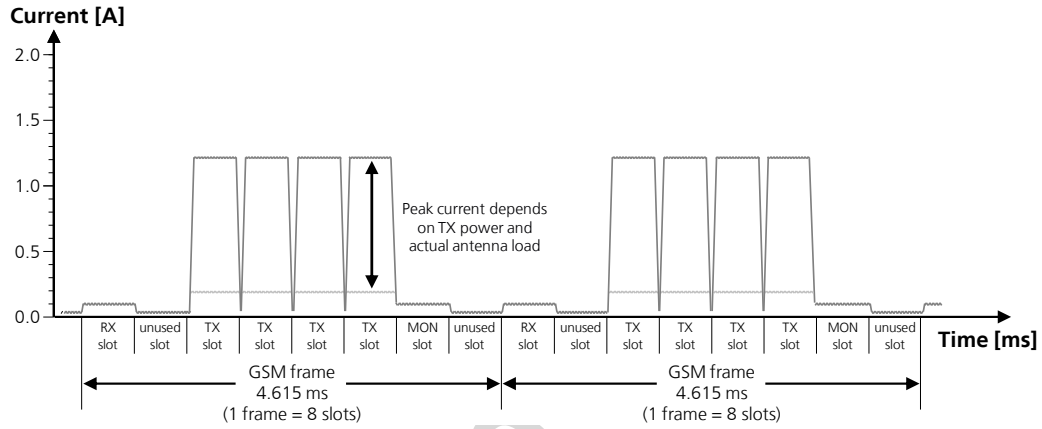


Figure 6: VCC current consumption profile versus time during a 2G GPRS/EDGE multi-slot connection (4 TX slots, 1 RX slot)

In case of EDGE connections the VCC current consumption profile is very similar to the GPRS current profile, so the image shown in Figure 6, representing the current consumption profile in GPRS class 12 connected mode, is valid for the EDGE class 12 connected mode as well.

1.5.1.3 VCC current consumption in LTE connected-mode

During an LTE connection, the module can transmit and receive continuously due to the Frequency Division Duplex (FDD) mode of operation used in LTE radio access technology.

The current consumption depends on output RF power, which is always regulated by the network (the current base station) sending power control commands to the module. These power control commands are logically divided into a slot of 0.5 ms (time length of one Resource Block), thus the rate of power change can reach a maximum rate of 2 kHz.

The current consumption profile is similar to that in 3G radio access technology. Unlike the 2G connection mode, which uses the TDMA mode of operation, there are no high current peaks since transmission and reception are continuously enabled in FDD.

In the worst scenario, corresponding to a continuous transmission and reception at maximum output power (approximately 250 mW or 24 dBm), the average current drawn by the module at the VCC pins is considerable (see the "Current consumption" section in LARA-R2 series Data Sheet [1]). At the lowest output RF power (approximately 0.1 µW or –40 dBm), the current drawn by the internal power amplifier is strongly reduced and the total current drawn by the module at the VCC pins is due to baseband processing and transceiver activity.

Figure 7 shows an example of the module current consumption profile versus time in LTE connected-mode. Detailed current consumption values can be found in LARA-R2 series Data Sheet [1].

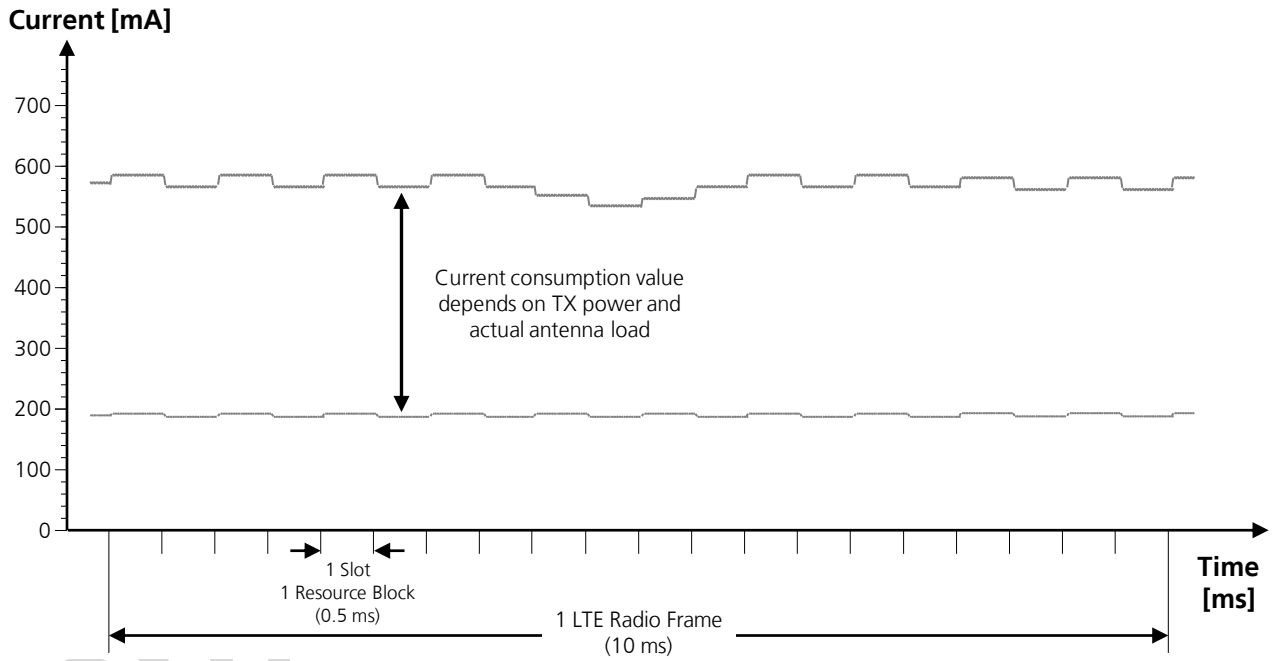


Figure 7: VCC current consumption profile versus time during LTE connection (TX and RX continuously enabled)

1.5.1.4 VCC current consumption in cyclic idle/active-mode (power saving enabled)

The power saving configuration is by default disabled, but it can be enabled using the appropriate AT command (see u-blox AT Commands Manual [2], AT+UPSV command). When power saving is enabled, the module automatically enters low power idle-mode whenever possible, reducing current consumption.

When the power saving configuration is enabled and the module is registered or attached to a network, the module automatically enters the low power idle-mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance to the 2G / LTE system requirements, even if connected-mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active-mode, to enable the reception of paging block. In between, the module switches to low power idle-mode. This is known as discontinuous reception (DRX).

The module processor core is activated during the paging block reception, and automatically switches its reference clock frequency from 32 kHz to the 26 MHz used in active-mode.

The time period between two paging block receptions is defined by the network. This is the paging period parameter, fixed by the base station through broadcast channel sent to all users on the same serving cell:

- In case of 2G radio access technology, the paging period can vary from 470.8 ms (DRX = 2, length of 2 x 51 2G frames = 2 x 51 x 4.615 ms) up to 2118.4 ms (DRX = 9, length of 9 x 51 2G frames = 9 x 51 x 4.615 ms)
- In case of LTE radio access technology, the paging period can vary from 320 ms (DRX = 5, i.e. length of 2^5 LTE frames = 32 x 10 ms) up to 2560 ms (DRX = 8, length of 2^8 LTE frames = 256 x 10 ms).

Figure 8 illustrates a typical example of the module current consumption profile when power saving is enabled. The module is registered with network, automatically enters the low power idle-mode and periodically wakes up to active-mode to monitor the paging channel for the paging block reception. Detailed current consumption values can be found in LARA-R2 series Data Sheet [1]).

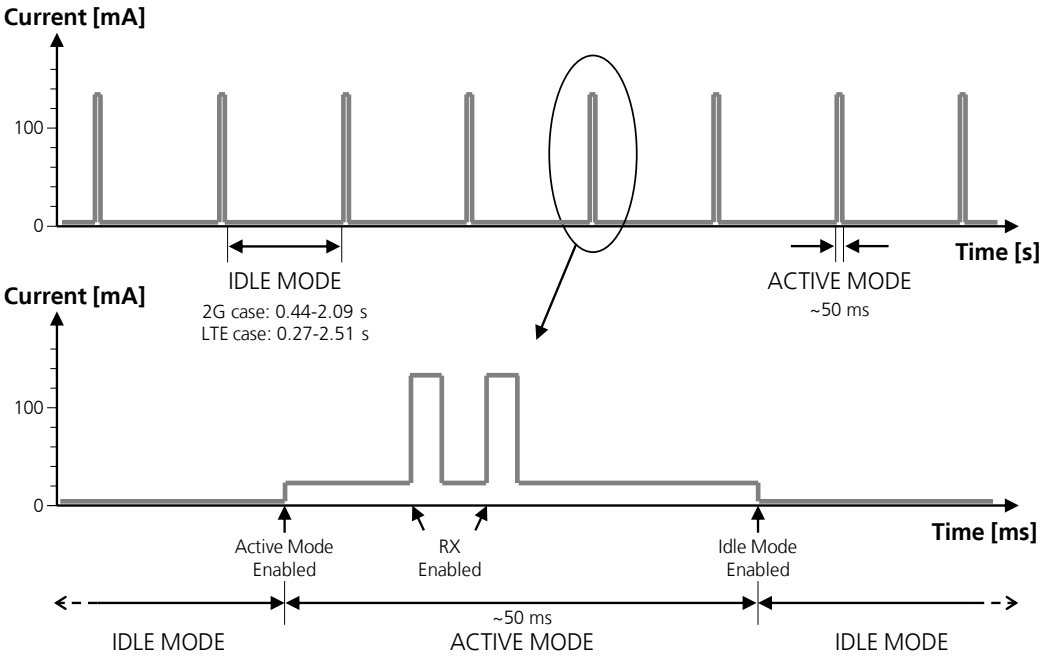


Figure 8: VCC current consumption profile with power saving enabled and module registered with the network: the module is in low-power idle-mode and periodically wakes up to active-mode to monitor the paging channel for paging block reception

1.5.1.5 VCC current consumption in fixed active-mode (power saving disabled)

Power saving configuration is by default disabled, or it can be disabled using the appropriate AT command (see u-blox AT Commands Manual [2], AT+UPSV command). When power saving is disabled, the module does not automatically enter idle-mode whenever possible: the module remains in active-mode.

The module processor core is activated during active-mode, and the 26 MHz reference clock frequency is used.

Figure 9 illustrates a typical example of the module current consumption profile when power saving is disabled. In such case, the module is registered with the network and while active-mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception. Detailed current consumption values can be found in LARA-R2 series Data Sheet [1].

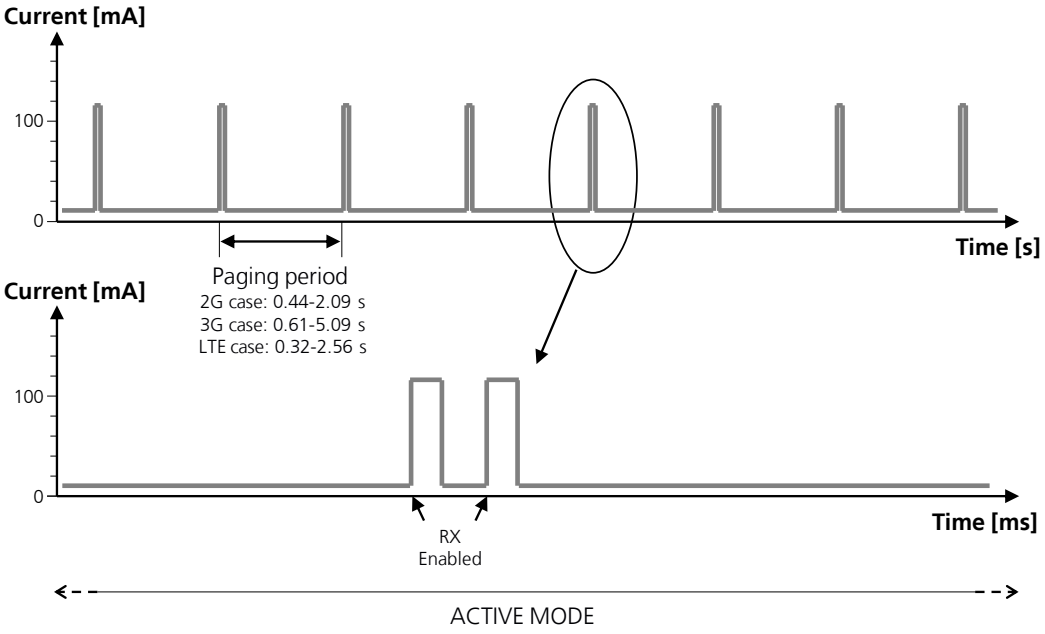


Figure 9: VCC current consumption profile with power saving disabled and module registered with the network: active-mode is always held and the receiver is periodically activated to monitor the paging channel for paging block reception

1.5.2 RTC supply input/output (V_BCKP)

The **V_BCKP** pin of LARA-R2 series modules connects the supply for the Real Time Clock (RTC) and Power-On internal logic. This supply domain is internally generated by a linear LDO regulator integrated in the Power Management Unit, as described in Figure 10. The output of this linear regulator is always enabled when the main voltage supply provided to the module through the **VCC** pins is within the valid operating range, with the module switched off or switched on.

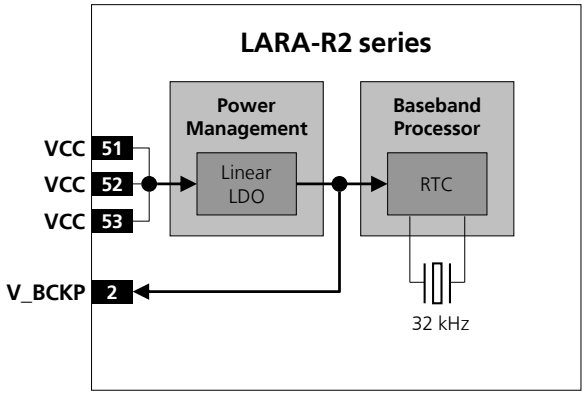


Figure 10: RTC supply input/output (V_BCKP) and 32 kHz RTC timing reference clock simplified block diagram

The RTC provides the module time reference (date and time) that is used to set the wake-up interval during the low power idle-mode periods, and is able to make available the programmable alarm functions.

The RTC functions are available also in power-down mode when the **V_BCKP** voltage is within its valid range (specified in the "Input characteristics of Supply/Power pins" table in LARA-R2 series Data Sheet [1]). The RTC can be supplied from an external back-up battery through the **V_BCKP**, when the main module voltage supply is not applied to the **VCC** pins. This lets the time reference (date and time) run until the **V_BCKP** voltage is within its valid range, even when the main supply is not provided to the module.

Consider that the module cannot switch on if a valid voltage is not present on **VCC** even when the RTC is supplied through **V_BCKP** (meaning that **VCC** is mandatory to switch on the module).

The RTC has very low current consumption, but is highly temperature dependent. For example, **V_BCKP** current consumption at the maximum operating temperature can be higher than the typical value at 25 °C specified in the "Input characteristics of Supply/Power pins" table in the LARA-R2 series Data Sheet [1].

If **V_BCKP** is left unconnected and the module main voltage supply is removed from **VCC**, the RTC is supplied from the bypass capacitor mounted inside the module. However, this capacitor is not able to provide a long buffering time: within few milliseconds the voltage on **V_BCKP** will go below the valid range. This has no impact on cellular connectivity, as all the module functionalities do not rely on date and time setting.

1.5.3 Generic digital interfaces supply output (V_INT)

The **V_INT** output pin of the LARA-R2 series modules is connected to an internal 1.8 V supply with current capability specified in the LARA-R2 series Data Sheet [1]. This supply is internally generated by a switching step-down regulator integrated in the Power Management Unit and it is internally used to source the generic digital I/O interfaces of the cellular module, as described in Figure 11. The output of this regulator is enabled when the module is switched on and it is disabled when the module is switched off.

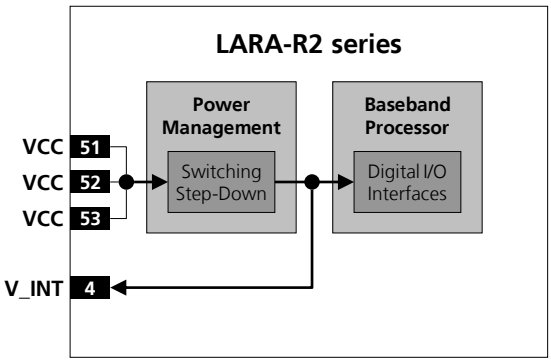


Figure 11: LARA-R2 series interfaces supply output (V_INT) simplified block diagram

The switching regulator operates in Pulse Width Modulation (PWM) mode for greater efficiency at high output loads and it automatically switches to Pulse Frequency Modulation (PFM) power save mode for greater efficiency at low output loads. The **V_INT** output voltage ripple is specified in the LARA-R2 series Data Sheet [1].

1.6 System function interfaces

1.6.1 Module power-on

When the LARA-R2 series modules are in the not-powered mode (switched off, i.e. the **VCC** module supply is not applied), they can be switched on as following:

- Rising edge on the **VCC** input pins to a valid voltage for module supply: the modules switch on if the **VCC** supply is applied with a rise time of less than 10 ms from 2.1 V to 3.0 V, reaching a proper nominal voltage value within the **VCC** operating range.

Alternately, in case for example the fast rise time on **VCC** rising edge cannot be guaranteed by the application, LARA-R2 series modules can be switched on from not-powered mode as following:

- **RESET_N** input pin is held low by the external application during the **VCC** rising edge, so that the modules will switch on when the external application releases the **RESET_N** input pin from the low logic level after that the **VCC** supply voltage stabilizes at its proper nominal value within the operating range
- **PWR_ON** input pin is held low by the external application during the **VCC** rising edge, so that the modules will switch on when the external application releases the **PWR_ON** input pin from the low logic level after that the **VCC** supply voltage stabilizes at its proper nominal value within the operating range

When the LARA-R2 series modules are in the power-off mode (i.e. switched off with valid **VCC** module supply applied), they can be switched on as following:

- Low pulse on the **PWR_ON** pin, which is normally set high by an internal pull-up, for a valid time period: the modules start the internal power-on sequence when the external application releases the **PWR_ON** pin from the low logic level after that it has been set low for an appropriate time period
- Rising edge on the **RESET_N** pin, i.e. releasing the pin from the low level, as that the pin is normally set high by an internal pull-up: the modules start the internal power-on sequence when the external application releases the **RESET_N** pin from the low logic level
- RTC alarm, i.e. pre-programmed alarm by AT+CALA command (see u-blox AT Commands Manual [2]).

As described in Figure 12, the LARA-R2 series **PWR_ON** input is equipped with an internal active pull-up resistor to the **V_BCKP** supply: the **PWR_ON** input voltage thresholds are different from the other generic digital interfaces. Detailed electrical characteristics are described in LARA-R2 series Data Sheet [1].

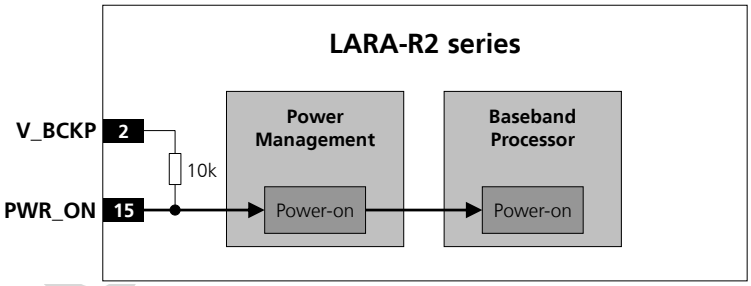


Figure 12: LARA-R2 series PWR_ON input description

Figure 13 shows the module power-on sequence from the not-powered mode, describing the following phases:

- The external supply is applied to the **VCC** module supply inputs, representing the start-up event.
- The **V_BCKP** RTC supply output is suddenly enabled by the module as **VCC** reaches a valid voltage value.
- The **PWR_ON** and the **RESET_N** pins suddenly rise to high logic level due to internal pull-ups.
- All the generic digital pins of the module are tri-stated until the switch-on of their supply source (**V_INT**).
- The internal reset signal is held low: the baseband core and all the digital pins are held in the reset state. The reset state of all the digital pins is reported in the pin description table of LARA-R2 series Data Sheet [1].
- When the internal reset signal is released, any digital pin is set in a proper sequence from the reset state to the default operational configured state. The duration of this pins' configuration phase differs within generic digital interfaces and the USB interface due to host / device enumeration timings (see section 1.9.2).
- The module is fully ready to operate after all interfaces are configured.

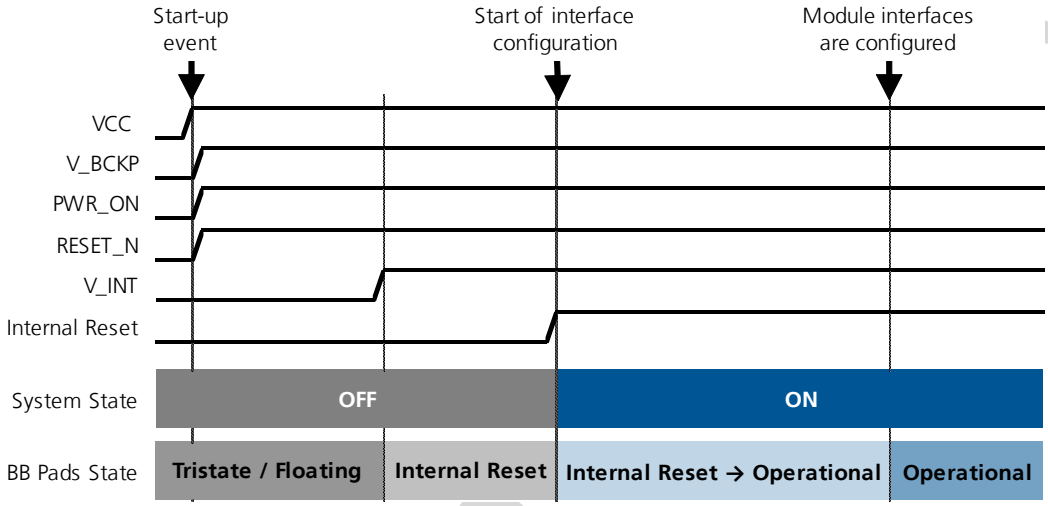


Figure 13: LARA-R2 series power-on sequence description

The greeting text can be activated by means of +CSGT AT command (see u-blox AT Commands Manual [2]) to notify the external application that the module is ready to operate (i.e. ready to reply to AT commands) and the first AT command can be sent to the module, given that autobauding has to be disabled on the UART to let the module sending the greeting text: the UART has to be configured at fixed baud rate (the baud rate of the application processor) instead of the default autobauding, otherwise the module does not know the baud rate to be used for sending the greeting text (or any other URC) at the end of the internal boot sequence.

☞ The Internal Reset signal is not available on a module pin, but the host application can monitor the **V_INT** pin to sense the start of the LARA-R2 series module power-on sequence.

☞ Before the switch-on of the generic digital interface supply source (**V_INT**) of the module, no voltage driven by an external application should be applied to any generic digital interface of the module.

☞ Before the LARA-R2 series module is fully ready to operate, the host application processor should not send any AT command over the AT communication interfaces (USB, UART) of the module.

1.6.2 Module power-off

LARA-R2 series can be properly switched off by:

- AT+CPWROFF command (see u-blox AT Commands Manual [2]). The current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

An abrupt under-voltage shutdown occurs on LARA-R2 series modules when the **VCC** module supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform the proper network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during LARA-R2 series modules normal operations: the power off procedure must be started by the AT+CPWROFF command, waiting the command response for a proper time period (see u-blox AT Commands Manual [2]), and then a proper **VCC** supply has to be held at least until the end of the modules' internal power off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

An abrupt hardware shutdown occurs on LARA-R2 series modules when a low level is applied on **RESET_N** pin. In this case, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

☞ It is highly recommended to avoid an abrupt hardware shutdown of the module by forcing a low level on the **RESET_N** input pin during module normal operation: the **RESET_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [2].

An over-temperature or an under-temperature shutdown occurs on LARA-R2 series modules when the temperature measured within the cellular module reaches the dangerous area, if the optional Smart Temperature Supervisor feature is enabled and configured by the dedicated AT command. For more details see section 1.14.15 and u-blox AT Commands Manual [2], +USTS AT command.

Figure 14 describes the LARA-R2 series modules power-off sequence, properly started sending the AT+CPWROFF command, allowing storage of current parameter settings in the module's non-volatile memory and a proper network detach, with the following phases:

- When the +CPWROFF AT command is sent, the module starts the switch-off routine.
- The module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**), except the RTC supply (**V_BCKP**).
- Then, the module remains in power-off mode as long as a switch on event does not occur (e.g. applying a proper low level to the **PWR_ON** input, or applying a proper low level to the **RESET_N** input), and enters not-powered mode if the supply is removed from the **VCC** pins.

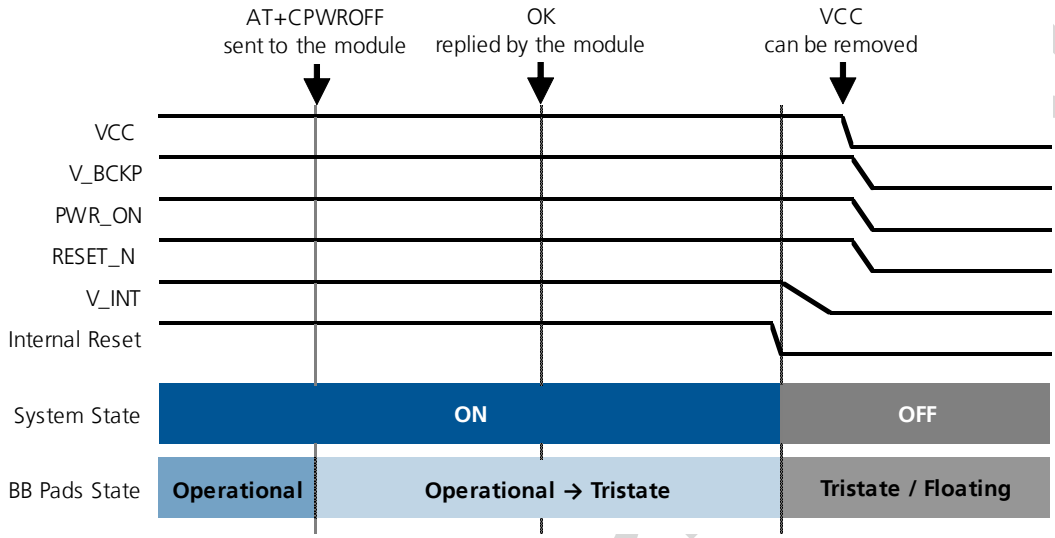


Figure 14: LARA-R2 series power-off sequence description

The Internal Reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the end of the LARA-R2 series power-off sequence.

The duration of each phase in the LARA-R2 series modules' switch-off routines can largely vary depending on the application / network settings and the concurrent module activities.

1.6.3 Module reset

LARA-R2 series modules can be properly reset (rebooted) by:

- AT+CFUN command (see the u-blox AT Commands Manual [2] for more details).

This command causes an "internal" or "software" reset of the module, which is an asynchronous reset of the module baseband processor. The current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed: this is the proper way to reset the modules.

An abrupt hardware reset occurs on LARA-R2 series modules when a low level is applied on the **RESET_N** input pin for a specific time period. In this case, the current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

☞ It is highly recommended to avoid an abrupt hardware reset of the module by forcing a low level on the **RESET_N** input during modules normal operation: the **RESET_N** line should be set low only if reset or shutdown via AT commands fails or if the module does not provide a reply to a specific AT command after a time period longer than the one defined in the u-blox AT Commands Manual [2].

As described in Figure 15, the **RESET_N** input pins are equipped with an internal pull-up to the **V_BCKP** supply.

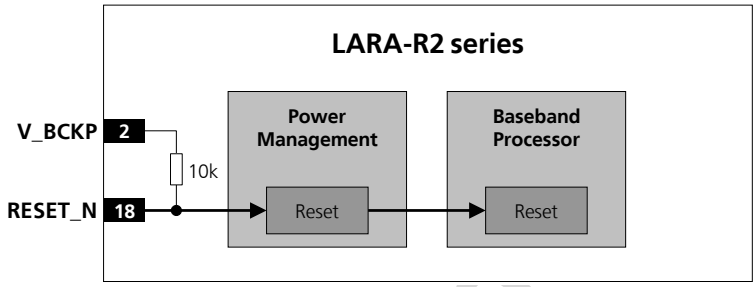


Figure 15: LARA-R2 series RESET_N input equivalent circuit description

☞ For more electrical characteristics details see LARA-R2 series Data Sheet [1].

1.6.4 Module / host configuration selection

☞ Selection of module / host configuration over **HOST_SELECT** is not supported by "02" product versions.

The modules include one pin (**HOST_SELECT**) to select the module / host application processor configuration: the pin is available to select, enable, connect, disconnect and subsequently re-connect the HSIC interface.

LARA-R2 series Data Sheet [1] describes the detailed electrical characteristics of the **HOST_SELECT** pin.

1.7 Antenna interface

1.7.1 Antenna RF interfaces (ANT1 / ANT2)

LARA-R2 series modules provide two RF interfaces for connecting the external antennas:

- The **ANT1** represents the primary RF input/output for transmission and reception of LTE/3G/2G RF signals.

  The **ANT1** pin has a nominal characteristic impedance of 50 Ω and must be connected to the primary Tx / Rx antenna through a 50 Ω transmission line to allow proper RF transmission and reception.
- The **ANT2** represents the secondary RF input for the reception of the LTE RF signals for the Down-Link Rx diversity radio technology supported by LARA-R2 series modules as required feature for LTE category 1 UEs.

  The **ANT2** pin has a nominal characteristic impedance of 50 Ω and must be connected to the secondary Rx antenna through a 50 Ω transmission line to allow proper RF reception.

1.7.1.1 Antenna RF interface requirements

Table 7, Table 8 and Table 9 summarize the requirements for the antennas RF interfaces (**ANT1** / **ANT2**). See section 0 for suggestions to properly design antennas circuits compliant with these requirements.

The antenna circuits affect the RF compliance of the device integrating LARA-R2 series modules with applicable required certification schemes (for more details see section 4). Compliance is guaranteed if the antenna RF interfaces (ANT1 / ANT2) requirements summarized in Table 7, Table 8 and Table 9 are fulfilled.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT1** port.
Frequency Range	See the LARA-R2 series Data Sheet [1]	The required frequency range of the antenna connected to **ANT1** port depends on the operating bands of the used cellular module and the used mobile network.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT1** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT1** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT1** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum Gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is transmitted in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT1** port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits. For additional info see sections 4.2.2 and/or 4.3.1
Input Power	> 33 dBm (> 2 W)	The antenna connected to the **ANT1** port must support with adequate margin the maximum power transmitted by the modules

Table 7: Summary of primary Tx/Rx antenna RF interface (ANT1) requirements

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT2** port.
Frequency Range	See the LARA-R2 series Data Sheet [1]	The required frequency range of the antennas connected to **ANT2** port depends on the operating bands of the used cellular module and the used Mobile Network.
Return Loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The Return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT2** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT2** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT2** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as the TIS, specified by applicable related certification schemes.

Table 8: Summary of secondary Rx antenna RF interface (ANT2) requirements

Item	Requirements	Remarks
Efficiency imbalance	< 0.5 dB recommended < 1.0 dB acceptable	The radiation efficiency imbalance is the ratio of the primary (**ANT1**) antenna efficiency to the secondary (**ANT2**) antenna efficiency: the efficiency imbalance is a measure of how much better an antenna receives or transmits compared to the other antenna. The radiation efficiency of the secondary antenna needs to be roughly the same of the radiation efficiency of the primary antenna for good RF performance.
Envelope Correlation Coefficient	< 0.4 recommended < 0.5 acceptable	The Envelope Correlation Coefficient (ECC) between the primary (**ANT1**) and the secondary (**ANT2**) antenna is an indicator of 3D radiation pattern similarity between the two antennas: low ECC results from antenna patterns with radiation lobes in different directions. The ECC between primary and secondary antenna needs to be enough low to comply with radiated performance requirements specified by related certification schemes.
Isolation	> 15 dB recommended > 10 dB acceptable	The antenna to antenna isolation is the loss between the primary (**ANT1**) and the secondary (**ANT2**) antenna: high isolation results from low coupled antennas. The isolation between primary and secondary antenna needs to be high for good RF performance.

Table 9: Summary of primary (ANT1) and secondary (ANT2) antennas relationship requirements

1.7.2 Antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an Analog to Digital Converter (ADC) provided to sense the antenna presence.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the u-blox AT Commands Manual [2] for more details on this feature.

The **ANT_DET** pin generates a DC current (for detailed characteristics see the LARA-R2 series Data Sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.2 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM card interface

LARA-R2 series modules provide a high-speed SIM/ME interface, including automatic detection and configuration of the voltage required by the connected SIM card or chip.

Both 1.8 V and 3 V SIM types are supported: activation and deactivation with automatic voltage switch from 1.8 V to 3 V is implemented, according to ISO-IEC 7816-3 specifications. The **VSIM** supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations.

The SIM driver supports the PPS (Protocol and Parameter Selection) procedure for baud-rate selection, according to the values determined by the SIM Card.

1.8.2 SIM card detection interface (SIM_DET)

The **GPIO5** pin is by default configured to detect the external SIM card mechanical / physical presence. The pin is configured as input, and it can sense SIM card presence as intended to be properly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **GPIO5** input pin is recognized as SIM card not present
- High logic level at **GPIO5** input pin is recognized as SIM card present

The SIM card detection function provided by **GPIO5** pin is an optional feature that can be implemented / used or not according to the application requirements: an Unsolicited Result Code (URC) is generated each time that there is a change of status (for more details see u-blox AT Commands Manual [2], +UGPIOC, +CIND, +CMER).

The optional function "SIM card hot insertion/removal" can be additionally configured on the **GPIO5** pin by specific AT command (see the u-blox AT Commands Manual [2], +UDCONF=50), in order to enable / disable the SIM interface upon detection of external SIM card physical insertion / removal.

1.9 Data communication interfaces

LARA-R2 series modules provide the following serial communication interfaces:

- UART interface: Universal Asynchronous Receiver/Transmitter serial interface available for the communication with a host application processor (AT commands, data communication, FW update by means of FOAT), for FW update by means of the u-blox EasyFlash tool and for diagnostic. (see section 1.9.1)
- USB interface: Universal Serial Bus 2.0 compliant interface available for the communication with a host application processor (AT commands, data communication, FW update by means of the FOAT feature), for FW update by means of the u-blox EasyFlash tool and for diagnostic. (see section 1.9.2)
- HSIC interface: High-Speed Inter-Chip USB compliant interface available for the communication with a host application processor (AT commands, data communication, FW update by means of the FOAT feature), for FW update by means of the u-blox EasyFlash tool and for diagnostic. (see section 1.9.3)
- DDC interface: I^2C bus compatible interface available for the communication with u-blox GNSS positioning chips or modules and with external I^2C devices as an audio codec. (see section 1.9.4)
- SDIO interface: Secure Digital Input Output interface available for the communication with compatible u-blox short range radio communication Wi-Fi modules. (see section 1.9.5)

1.9.1 UART interface

1.9.1.1 UART features

The UART interface is a 9-wire 1.8 V unbalanced asynchronous serial interface available on all the LARA-R2 series modules, supporting:

- AT command mode[5]
- Data mode and Online command mode[5]
- Multiplexer protocol functionality (see 1.9.1.5)
- FW upgrades by means of the FOAT feature (see 1.14.13 and Firmware update application note [23])
- FW upgrades by means of the u-blox EasyFlash tool (see the Firmware update application note [23])
- Trace log capture (diagnostic purpose)

UART interface provides RS-232 functionality conforming to the ITU-T V.24 Recommendation [5], with CMOS compatible signal levels: 0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state (for detailed electrical characteristics see LARA-R2 series Data Sheet [1]), providing:

- data lines (**RXD** as output, **TXD** as input),
- hardware flow control lines (**CTS** as output, **RTS** as input),
- modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output).

LARA-R2 series modules are designed to operate as cellular modems, i.e. as the data circuit-terminating equipment (DCE) according to the ITU-T V.24 Recommendation [5]. A host application processor connected to the module through the UART interface represents the data terminal equipment (DTE).

☞ UART signal names of the modules conform to the ITU-T V.24 Recommendation [5]: e.g. **TXD** line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

LARA-R2 series modules' UART interface is by default configured in AT command mode: the module waits for AT command instructions and interprets all the characters received as commands to execute.

[5] See the u-blox AT Commands Manual [2] for the definition of the command mode, data mode, and online command mode.

All the functionalities supported by LARA-R2 series modules can be set and configured by AT commands:

- AT commands according to 3GPP TS 27.007 [6], 3GPP TS 27.005 [7], 3GPP TS 27.010 [8]
- u-blox AT commands (for the complete list and syntax see the u-blox AT Commands Manual [2])

All flow control handshakes are supported by the UART interface and can be set by appropriate AT commands (see u-blox AT Commands Manual [2], &K, +IFC, \Q AT commands): hardware, software, or none flow control.

☞ Hardware flow control is enabled by default.

The one-shot autobauding is supported: the automatic baud rate detection is performed only once, at module start up. After the detection, the module works at the detected baud rate and the baud rate can only be changed by AT command (see u-blox AT Commands Manual [2], +IPR command).

☞ One-shot automatic baud rate recognition (autobauding) is enabled by default.

The following baud rates can be configured by AT command (see u-blox AT Commands Manual [2], +IPR):

- 9600 b/s
- 19200 b/s
- 38400 b/s
- 57600 b/s
- 115200 b/s, default value when one-shot autobauding is disabled
- 230400 b/s
- 460800 b/s
- 921600 b/s
- 3000000 b/s
- 3250000 b/s
- 6000000 b/s
- 6500000 b/s

☞ Baud rates higher than 460800 b/s cannot be automatically detected by LARA-R2 series modules.

The modules support the one-shot automatic frame recognition in conjunction with the one-shot autobauding. The following frame formats can be configured by AT command (see u-blox AT Commands Manual [2], +ICF):

- 8N1 (8 data bits, No parity, 1 stop bit), default frame configuration with fixed baud rate, see Figure 16
- 8E1 (8 data bits, even parity, 1 stop bit)
- 8O1 (8 data bits, odd parity, 1 stop bit)
- 8N2 (8 data bits, No parity, 2 stop bits)
- 7E1 (7 data bits, even parity, 1 stop bit)
- 7O1 (7 data bits, odd parity, 1 stop bit)

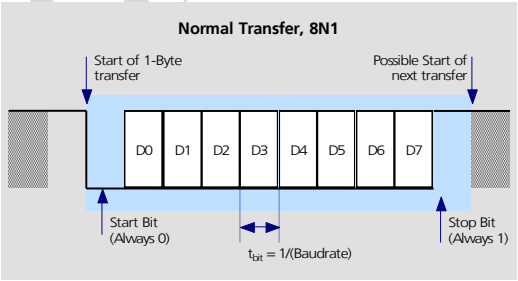


Figure 16: Description of UART 8N1 frame format (8 data bits, no parity, 1 stop bit)

1.9.1.2 UART AT interface configuration

The UART interface of LARA-R2 series modules is available as AT command interface with the default configuration described in Table 10 (for more details and information about further settings, see the u-blox AT Commands Manual [2]).

Interface	AT Settings	Comments
UART interface	AT interface: enabled	AT command interface is enabled by default on the UART physical interface
	AT+IPR=0	One-shot autobauding enabled by default on the modules
	AT+ICF=3,1	8N1 frame format enabled by default
	AT&K3	HW flow control enabled by default
	AT&S1	DSR line (Circuit 107 in ITU-T V.24) set ON in data mode[6] and set OFF in command mode[6]
	AT&D1	Upon an ON-to-OFF transition of DTR line (Circuit 108/2 in ITU-T V.24), the module (DCE) enters online command mode[6] and issues an OK result code
	AT&C1	DCD line (Circuit 109 in ITU-T V.24) changes in accordance with the Carrier detect status; ON if the Carrier is detected, OFF otherwise
	MUX protocol: disabled	Multiplexing mode is disabled by default and it can be enabled by AT+CMUX command. For more details, see the Mux Implementation Application Note [21]. The following virtual channels are defined: • Channel 0: control channel • Channel 1 – 5: AT commands / data connection • Channel 6: GNSS tunneling[7]

Table 10: Default UART AT interface configuration

1.9.1.3 UART signal behavior

At the module switch-on, before the UART interface initialization (as described in the power-on sequence reported in Figure 13), each pin is first tri-stated and then is set to its related internal reset state[8]. At the end of the boot sequence, the UART interface is initialized, the module is by default in active-mode, and the UART interface is enabled as AT commands interface.

The configuration and the behavior of the UART signals after the boot sequence are described below. See section 1.4 for definition and description of module operating modes referred to in this section.

RXD signal behavior

The module data output line (**RXD**) is set by default to the OFF state (high level) at UART initialization. The module holds **RXD** in the OFF state until the module does not transmit some data.

TXD signal behavior

The module data input line (**TXD**) is set by default to the OFF state (high level) at UART initialization. The **TXD** line is then held by the module in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **TXD** input.

[6] See the u-blox AT Commands Manual [2] for the definition of the command mode, data mode, and online command mode
[7] Not supported by "02" product versions
[8] Refer to the pin description table in the LARA-R2 series Data Sheet [1].

CTS signal behavior

The module hardware flow control output (**CTS** line) is set to the ON state (low level) at UART initialization.

If the hardware flow control is enabled, as it is by default, the **CTS** line indicates when the UART interface is enabled (data can be sent and received). The module drives the **CTS** line to the ON state or to the OFF state when it is either able or not able to accept data from the DTE over the UART (see 1.9.1.4 for more details).

☞ If hardware flow control is enabled, then when the **CTS** line is OFF it does not necessarily mean that the module is in low power idle-mode, but only that the UART is not enabled, as the module could be forced to stay in active-mode for other activities, e.g. related to the network or related to other interfaces.

☞ When the multiplexer protocol is active, the **CTS** line state is mapped to FCon / FCoff MUX command for flow control issues outside the power saving configuration while the physical **CTS** line is still used as a power state indicator. For more details, see Mux Implementation Application Note [21].

The **CTS** hardware flow control setting can be changed by AT commands (for more details, see u-blox AT Commands Manual [2], AT&K, AT\Q, AT+IFC, AT+UCTS AT command).

☞ When the power saving configuration is enabled by AT+UPSV command and the hardware flow-control is not implemented in the DTE/DCE connection, data sent by the DTE can be lost: the first character sent when the module is in low power idle-mode will not be a valid communication character (see section 1.9.1.4 and in particular the sub-section “Wake up via data reception” for further details).

RTS signal behavior

The hardware flow control input (**RTS** line) is set by default to the OFF state (high level) at UART initialization. The module then holds the **RTS** line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **RTS** input.

If the HW flow control is enabled, as it is by default, the module monitors the **RTS** line to detect permission from the DTE to send data to the DTE itself. If the **RTS** line is set to the OFF state, any on-going data transmission from the module is interrupted until the subsequent **RTS** line change to the ON state.

☞ The DTE must still be able to accept a certain number of characters after the **RTS** line is set to the OFF state: the module guarantees the transmission interruption within two characters from **RTS** state change.

Module behavior according to **RTS** hardware flow control status can be configured by AT commands (for more details, see u-blox AT Commands Manual [2], AT&K, AT\Q, AT+IFC command descriptions).

If AT+UPSV=2 is set and HW flow control is disabled, the module monitors the **RTS** line to manage the power saving configuration (For more details, see section 1.9.1.4 and u-blox AT Commands Manual [2], AT+UPSV):

- When an OFF-to-ON transition occurs on the **RTS** input, the UART is enabled and the module is forced to active-mode. After ~20 ms, the switch is completed and data can be received without loss. The module cannot enter low power idle-mode and the UART is enabled as long as the **RTS** is in the ON state
- If the **RTS** input line is set to the OFF state by the DTE, the UART is disabled (held in low power mode) and the module automatically enters low power idle-mode whenever possible

DSR signal behavior

If AT&S1 is set, as it is by default, the **DSR** module output line is set by default to the OFF state (high level) at UART initialization. The **DSR** line is then set to the OFF state when the module is in command mode[9] or in online command mode[9] and is set to the ON state when the module is in data mode[9].

If AT&S0 is set, the **DSR** module output line is set by default to the ON state (low level) at UART initialization and is then always held in the ON state.

[9] See the u-blox AT Commands Manual [2] for the definition of the command mode, data mode, and online command mode

DTR signal behavior

The **DTR** module input line is set by default to the OFF state (high level) at UART initialization. The module then holds the **DTR** line in the OFF state if the line is not activated by the DTE: an active pull-up is enabled inside the module on the **DTR** input.

Module behavior according to **DTR** status can be changed by AT command (for more details, see u-blox AT Commands Manual [2], AT&D command description).

If AT+UPSV=3 is set, the **DTR** line is monitored by the module to manage the power saving configuration (for more details, see section 1.9.1.4 and u-blox AT Commands Manual [2], AT+UPSV command):

- When an OFF-to-ON transition occurs on the **DTR** input, the UART is enabled and the module is forced to active-mode. After ~20 ms, the switch is completed and data can be received without loss. The module cannot enter low power idle-mode and the UART is enabled as long as the **DTR** is in the ON state
- If the **DTR** input line is set to the OFF state by the DTE, the UART is disabled (held in low power mode) and the module automatically enters low power idle-mode whenever possible

DCD signal behavior

If AT&C1 is set, as it is by default, the **DCD** module output line is set by default to the OFF state (high level) at UART initialization. The module then sets the **DCD** line according to the carrier detect status: ON if the carrier is detected, OFF otherwise.

In case of voice calls, **DCD** is set to the ON state when the call is established.

In case of data calls, there are the following scenarios regarding the **DCD** signal behavior:

- **Packet Switched Data call**: Before activating the PPP protocol (data mode) a dial-up application must provide the ATD*99***<context_number># to the module: with this command the module switches from command mode to data mode and can accept PPP packets. The module sets the **DCD** line to the ON state, then answers with a CONNECT to confirm the ATD*99 command. The **DCD** ON is not related to the context activation but with the data mode
- **Circuit Switched Data call**: To establish a data call, the DTE can send the ATD<number> command to the module which sets an outgoing data call to a remote modem (or another data module). Data can be transparent (non reliable) or non transparent (with the reliable RLP protocol). When the remote DCE accepts the data call, the module **DCD** line is set to ON and the CONNECT <communication baudrate> string is returned by the module. At this stage the DTE can send characters through the serial line to the data module which sends them through the network to the remote DCE attached to a remote DTE

☞ The **DCD** is set to ON during the execution of the +CMGS, +CMGW, +USOWR, +USODL AT commands requiring input data from the DTE: the **DCD** line is set to the ON state as soon as the switch to binary/text input mode is completed and the prompt is issued; **DCD** line is set to OFF as soon as the input mode is interrupted or completed (for more details see the u-blox AT Commands Manual [2]).

☞ The **DCD** line is kept in the ON state, even during the online command mode[10], to indicate that the data call is still established even if suspended, while if the module enters command mode[10], the **DSR** line is set to the OFF state. For more details see **DSR** signal behavior description.

☞ For scenarios when the **DCD** line setting is requested for different reasons (e.g. SMS texting during online command mode[10]), the **DCD** line changes to guarantee the correct behavior for all the scenarios. For example, in case of SMS texting in online command mode[10], if the data call is released, **DCD** is kept ON till the SMS command execution is completed (even if the data call release would request **DCD** set OFF).

If AT&C0 is set, the **DCD** module output line is set by default to the ON state (low level) at UART initialization and is then always held in the ON state.

[10] See the u-blox AT Commands Manual [2] for the definition of the command mode, data mode, and online command mode

RI signal behavior

The **RI** module output line is set by default to the OFF state (high level) at UART initialization. Then, during an incoming call, the **RI** line is switched from the OFF state to the ON state with a 4:1 duty cycle and a 5 s period (ON for 1 s, OFF for 4 s, see Figure 17), until the DTE attached to the module sends the ATA string and the module accepts the incoming data call. The RING string sent by the module (DCE) to the serial port at constant time intervals is not correlated with the switch of the **RI** line to the ON state.

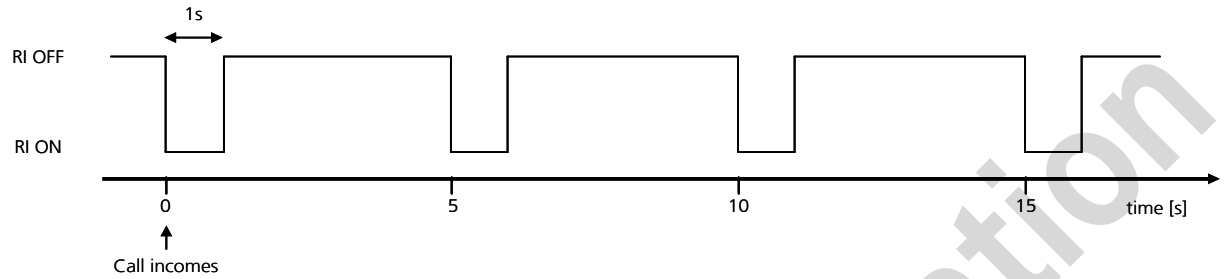


Figure 17: RI behavior during an incoming call

The **RI** line can notify an SMS arrival. When the SMS arrives, the **RI** line switches from OFF to ON for 1 s (see Figure 18), if the feature is enabled by the AT+CNMI command (see the u-blox AT Commands Manual [2]).

Figure 18: RI behavior at SMS arrival

This behavior allows the DTE to stay in power saving mode until the DCE related event requests service.
For SMS arrival, if several events coincidently occur or in quick succession each event independently triggers the **RI** line, although the line will not be deactivated between each event. As a result, the **RI** line may stay to ON for more than 1 s.

If an incoming call is answered within less than 1 s (with ATA or if auto-answering is set to ATS0=1) than the **RI** line is set to OFF earlier.

As a result:

- **RI** line monitoring cannot be used by the DTE to determine the number of received SMSes.
- For multiple events (incoming call plus SMS received), the **RI** line cannot be used to discriminate the two events, but the DTE must rely on the subsequent URCs and interrogate the DCE with proper commands.

The **RI** line can additionally notify all the URCs and all the incoming data (PPP, Direct Link, sockets, FTP), if the feature is enabled by the AT+URING command (for more details see u-blox AT Commands Manual [2]): the **RI** line is asserted when one of the configured events occur and it remains asserted for 1 s unless another configured event will happen, with the same behavior described in Figure 18.

1.9.1.4 UART and power-saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description, see u-blox AT Commands Manual [2]). When power saving is enabled, the module automatically enters low power idle-mode whenever possible, and otherwise the active-mode is maintained by the module (see section 1.4 for definition and description of module operating modes referred to in this section).

The AT+UPSV command configures both the module power saving and also the UART behavior in relation to the power saving. The conditions for the module entering low power idle-mode also depend on the UART power saving configuration, as the module does not enter the low power idle-mode according to any required activity related to the network (within or outside an active call) or any other required concurrent activity related to the functions and interfaces of the module, including the UART interface.

Three different power saving configurations can be set by the AT+UPSV command:

- AT+UPSV=0, power saving disabled (default configuration)
- AT+UPSV=1, power saving enabled cyclically
- AT+UPSV=2, power saving enabled and controlled by the UART **RTS** input line
- AT+UPSV=3, power saving enabled and controlled by the UART **DTR** input line

The different power saving configurations that can be set by the +UPSV AT command are described in details in the following subsections. Table 11 summarizes the UART interface communication process in the different power saving configurations, in relation with HW flow control settings and **RTS** input line status. For more details on the +UPSV AT command description, refer to u-blox AT commands Manual [2].

AT+UPSV	HW flow control	RTS line	DTR line	Communication during idle-mode and wake up
0	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module is correctly received by the DTE.
0	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
0	Disabled (AT&K0)	ON or OFF	ON or OFF	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
1	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE is buffered by the DTE and will be correctly received by the module when it is ready to receive data (when UART is enabled). Data sent by the module is correctly received by the DTE.
1	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE is buffered by the DTE and will be correctly received by the module when it is ready to receive data (when UART is enabled). Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
1	Disabled (AT&K0)	ON or OFF	ON or OFF	The first character sent by the DTE is lost by the module, but after ~20 ms the UART and the module are woken up: recognition of subsequent characters is guaranteed only after the UART / module complete wake-up (after ~20 ms). Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise the data is lost.
2	Enabled (AT&K3)	ON or OFF	ON or OFF	Not Applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Disabled (AT&K0)	ON	ON or OFF	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.
2	Disabled (AT&K0)	OFF	ON or OFF	Data sent by the DTE is lost by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data is lost.

AT+UPSV	HW flow control	RTS line	DTR line	Communication during idle-mode and wake up
3	Enabled (AT&K3)	ON	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE.
3	Enabled (AT&K3)	ON	OFF	Data sent by the DTE is lost by the module. Data sent by the module is correctly received by the DTE.
3	Enabled (AT&K3)	OFF	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
3	Enabled (AT&K3)	OFF	OFF	Data sent by the DTE is lost by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
3	Disabled (AT&K0)	ON or OFF	ON	Data sent by the DTE is correctly received by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data are lost.
3	Disabled (AT&K0)	ON or OFF	OFF	Data sent by the DTE is lost by the module. Data sent by the module is correctly received by the DTE if it is ready to receive data, otherwise data are lost.

Table 11: UART and power-saving summary

AT+UPSV=0: power saving disabled, fixed active-mode

The module does not enter low power idle-mode and the UART interface is enabled (data can be sent and received): the **CTS** line is always held in the ON state after UART initialization. This is the default configuration.

AT+UPSV=1: power saving enabled, cyclic idle/active-mode

When the AT+UPSV=1 command is issued by the DTE, the UART will be normally disabled, and then periodically or upon necessity enabled as following:

- During the periodic UART wake up to receive or send data, also according to the module wake up for the paging reception (see section 1.5.1.4) or other activities
- If the module needs to transmit some data (e.g. URC), the UART is temporarily enabled to send data
- If the DTE send data with HW flow control disabled, the first character sent causes the UART and module wake-up after ~20 ms: recognition of subsequent characters is guaranteed only after the complete wake-up (see the following subsection "wake up via data reception")

The module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to the UART periodic wake up so that the module cyclically enters the low power idle-mode and the active-mode. Additionally, the module wakes up to active-mode according to any required activity related to the network (e.g. for the periodic paging reception described in section 1.5.1.4, or for any other required RF Tx / Rx) or any other required activity related to module functions / interfaces (including the UART itself).

The time period of the UART enable/disable cycle is configured differently when the module is registered with a 2G network compared to when the module is registered with an LTE network:

- 2G: UART is enabled synchronously with some paging receptions: UART is enabled concurrently to a paging reception, and then, as data has not been received or sent, UART is disabled until the first paging reception that occurs after a timeout of 2.0 s, and therefore the interface is enabled again
- LTE: UART is asynchronously enabled to paging receptions, as UART is enabled for ~20 ms, and then, if data are not received or sent, UART is disabled for 2.5 s, and afterwards the interface is enabled again
- Not registered: when a module is not registered with a network, UART is enabled for ~20 ms, and then, if data has not been received or sent, UART is disabled for 2.5 s, and afterwards the interface is enabled again

When the UART interface is enabled, data can be received. When a character is received, it forces the UART interface to stay enabled for a longer time and it forces the module to stay in the active-mode for a longer time, according to the timeout configured by the second parameter of the +UPSV AT command. The timeout can be

set from 40 2G-frames (i.e. 40 x 4.615 ms = 184 ms) up to 65000 2G-frames (i.e. 65000 x 4.615 ms = 300 s). Default value is 2000 2G-frames (i.e. 2000 x 4.615 ms = 9.2 s). Every subsequent character received during the active-mode, resets and restarts the timer; hence the active-mode duration can be extended indefinitely.

The **CTS** output line is driven to the ON or OFF state when the module is either able or not able to accept data from the DTE over the UART: Figure 19 illustrates the **CTS** output line toggling due to paging reception and data received over the UART, with AT+UPSV=1 configuration.

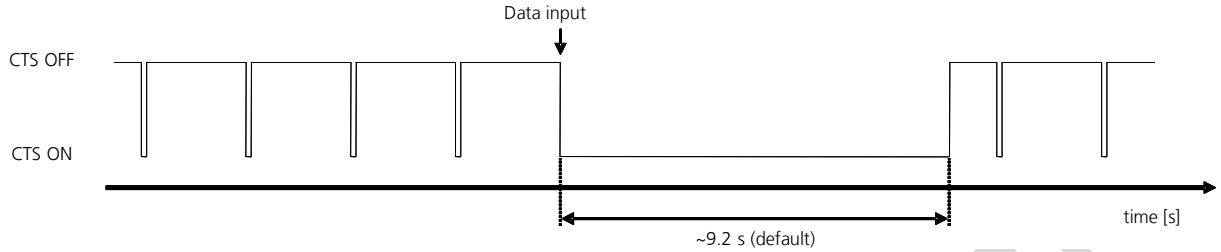


Figure 19: CTS output pin indicates when module's UART is enabled (CTS = ON = low level) or disabled (CTS = OFF = high level)

AT+UPSV=2: power saving enabled and controlled by the RTS line

This configuration can only be enabled with the module hardware flow control disabled (i.e. AT&K0 setting).

The UART interface is disabled after the DTE sets the **RTS** line to OFF.

Afterwards, the UART is enabled again, and the module does not enter low power idle-mode, as following:

- If an OFF-to-ON transition occurs on the **RTS** input, this causes the UART / module wake-up after ~20 ms: recognition of subsequent characters is guaranteed only after the complete wake-up, and the UART is kept enabled as long as the **RTS** input line is set to ON.
- If the module needs to transmit some data (e.g. URC), the UART is temporarily enabled to send data

The module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to any required activity related to the network (e.g. for the periodic paging reception described in section 1.5.1.4, or for any other required RF transmission / reception) or any other required activity related to the module functions / interfaces (including the UART itself).

AT+UPSV=3: power saving enabled and controlled by the DTR line

The UART interface is disabled after the DTE sets the **DTR** line to OFF.

Afterwards, the UART is enabled again, and the module does not enter low power idle-mode, as following:

- If an OFF-to-ON transition occurs on the **DTR** input, this causes the UART / module wake-up after ~20 ms: recognition of subsequent characters is guaranteed only after the complete wake-up, and the UART is kept enabled as long as the **DTR** input line is set to ON
- If the module needs to transmit some data (e.g. URC), the UART is temporarily enabled to send data

The module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to any required activity related to the network (e.g. for the periodic paging reception described in section 1.5.1.4, or for any other required RF signal transmission or reception) or any other required activity related to the functions / interfaces of the module.

The AT+UPSV=3 configuration can be enabled regardless the flow control setting on UART. In particular, the HW flow control can be enabled (AT&K3) or disabled (AT&K0) on UART during this configuration. In both cases, with the AT+UPSV=3 configuration, the **CTS** line indicates when the module is either able or not able to accept data from the DTE over the UART.

When the AT+UPSV=3 configuration is enabled, the **DTR** input line can still be used by the DTE to control the module behavior according to AT&D command configuration (see u-blox AT commands Manual [2]).

Wake up via data reception

The UART wake up via data reception consists of a special configuration of the module **TXD** input line that causes the system wake-up when a low-to-high transition occurs on the **TXD** input line. In particular, the UART is enabled and the module switches from the low power idle-mode to active-mode within ~20 ms from the first character received: this is the system "wake up time".

As a consequence, the first character sent by the DTE when the UART is disabled (i.e. the wake up character) is not a valid communication character even if the wake up via data reception configuration is active, because it cannot be recognized, and the recognition of the subsequent characters is guaranteed only after the complete system wake-up (i.e. after ~20 ms).

The UART wake up via data reception configuration is active in the following cases:

- AT+UPSV=1 is set with HW flow control disabled

Figure 20 and Figure 21 show examples of common scenarios and timing constraints:

- AT+UPSV=1 power saving configuration is active and the timeout from last data received to idle-mode start is set to 2000 frames (AT+UPSV=1,2000)
- Hardware flow control is disabled

Figure 20 shows the case where the module UART is disabled and only a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE module UART is disabled when the timeout from last data received expires (2000 frames without data reception, as the default case).

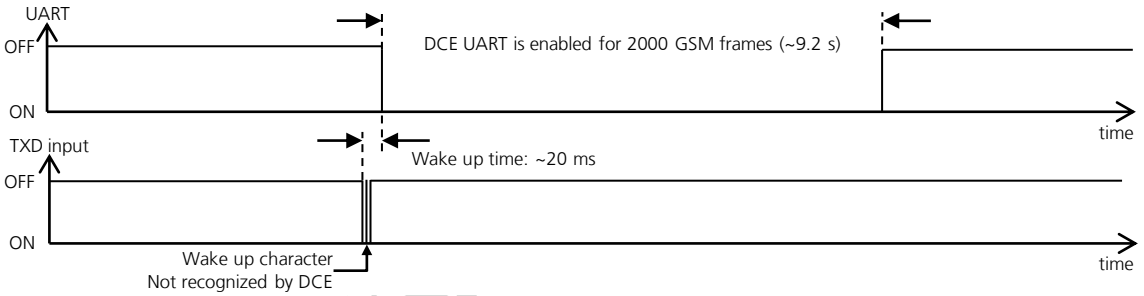


Figure 20: Wake-up via data reception without further communication

Figure 21 shows the case where in addition to the wake-up character further (valid) characters are sent. The wake up character wakes-up the module UART. The other characters must be sent after the "wake up time" of ~20 ms. If this condition is satisfied, the module (DCE) recognizes characters. The module will disable the UART after 2000 GSM frames from the latest data reception.

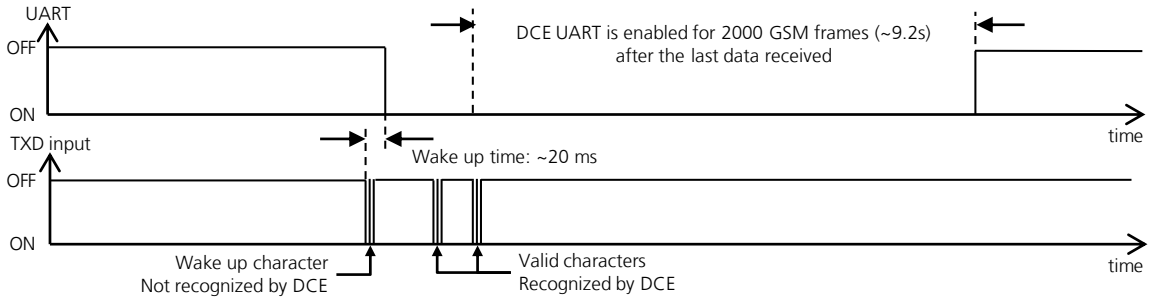


Figure 21: Wake-up via data reception with further communication

☞ The "wake-up via data reception" feature cannot be disabled.

☞ In command mode[11], with "wake-up via data reception" enabled and autobauding enabled, the DTE should always send a dummy character to the module before the "AT" prefix set at the beginning of each command line: the first dummy character is ignored if the module is in active-mode, or it represents the wake-up character if the module is in low power idle-mode.

☞ In command mode[11], with "wake-up via data reception" enabled and autobauding disabled, the DTE should always send a dummy "AT" to the module before each command line: the first dummy "AT" is not ignored if the module is in active-mode (i.e. the module replies "OK"), or it represents the wake up character if the module is in low power idle-mode (i.e. the module does not reply).

Additional considerations

If the USB is connected and not suspended, the module is kept ready to communicate over USB regardless the AT+UPSV settings, which have instead effect on the UART behavior, as they configure the UART power saving, so that UART is enabled / disabled according to the AT+UPSV settings.

To set the AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 configuration over the USB interface, the autobauding must be previously disabled on the UART by the +IPR AT command over the used USB AT interface, and this +IPR AT command configuration must be saved in the module' non-volatile memory (see the u-blox AT Commands Manual [2]). Then, after the subsequent module re-boot, AT+UPSV=1, AT+UPSV=2 or AT+UPSV=3 can be issued over the used AT interface (the USB): all the AT profiles are updated accordingly.

1.9.1.5 Multiplexer protocol (3GPP TS 27.010)

LARA-R2 series modules include multiplexer functionality as per 3GPP TS 27.010 [8], on the UART physical link.

This is a data link protocol which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART): the user can concurrently use AT interface on one MUX channel and data communication on another MUX channel.

The following virtual channels are defined (for more details, see Mux implementation Application Note [21]):

- Channel 0: Multiplexer control
- Channel 1 – 5: AT commands / data connection
- Channel 6: GNSS data tunneling

☞ The GNSS data tunneling channel is not supported by "02" product versions.

[11] See the u-blox AT Commands Manual [2] for the definition of the command mode, data mode, and online command mode.

1.9.2 USB interface

1.9.2.1 USB features

LARA-R2 series modules include a High-Speed USB 2.0 compliant interface with 480 Mb/s maximum data rate, representing the main interface for transferring high speed data with a host application processor, supporting:

- AT command mode[12]
- Data mode and Online command mode[12]
- FW upgrades by means of the FOAT feature (see 1.14.13 and Firmware update application note [23])
- FW upgrades by means of the u-blox EasyFlash tool (see the Firmware update application note [23])
- Trace log capture (diagnostic purpose)

The module itself acts as a USB device and can be connected to a USB host such as a Personal Computer or an embedded application microprocessor equipped with compatible drivers.

The **USB_D+/USB_D-** lines carry USB serial bus data and signaling according to the Universal Serial Bus Revision 2.0 specification [9], while the **VUSB_DET** input pin senses the VBUS USB supply presence (nominally 5 V at the source) to detect the host connection and enable the interface.

The USB interface of the module is enabled only if a valid voltage is detected by the **VUSB_DET** input (see the LARA-R2 series Data Sheet [1]). Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs few microamperes.

The USB interface is controlled and operated with:

- AT commands according to 3GPP TS 27.007 [6], 3GPP TS 27.005 [7]
- u-blox AT commands (for the complete list and syntax see the u-blox AT Commands Manual [2])

The USB interface of LARA-R2 series modules, according to the configured USB profile, can provide different USB functions with various capabilities and purposes, such as:

- CDC-ACM for AT commands and data communication
- CDC-ACM for GNSS tunneling
- CDC-ACM for SAP (SIM Access Profile)
- CDC-ACM for Diagnostic log
- CDC-NCM for Ethernet-over-USB

☞ CDC-ACM for GNSS tunneling, CDC-ACM for SAP, and CDC-NCM for Ethernet-over-USB are not supported by "02" product versions.

The USB profile of LARA-R2 series modules identifies itself by its VID (Vendor ID) and PID (Product ID) combination, included in the USB device descriptor according to the USB 2.0 specification [9].

If the USB is connected to the host before the module is switched on, or if the module is reset (rebooted) with the USB connected to the host, the VID and PID are automatically updated during the boot of the module. First, VID and PID are the following:

- VID = 0x8087
- PID = 0x0716

This VID and PID combination identifies a USB profile where no USB function described above is available: AT commands must not be sent to the module over the USB profile identified by this VID and PID combination.

[12] See the u-blox AT Commands Manual [2] for the definition of the command mode, data mode, and online command mode.

Then, after a time period (which depends on the host / device enumeration timings), the VID and PID are updated to the ones related to the default USB profile providing the following set of USB functions:

- 6 CDC-ACM modem COM ports enumerated as follows:
  - USB1: AT and data
  - USB2: AT and data
  - USB3: AT and data
  - USB4: GNSS tunneling
  - USB5: SAP (SIM Access Profile)
  - USB6: Primary Log (diagnostic purpose)

VID and PID of this USB profile with the set of functions described above (6 CDC-ACM) are the following:

- VID = 0x1546
- PID = 0x110A

Figure 22 summarizes the USB end-points available with the default USB profile.

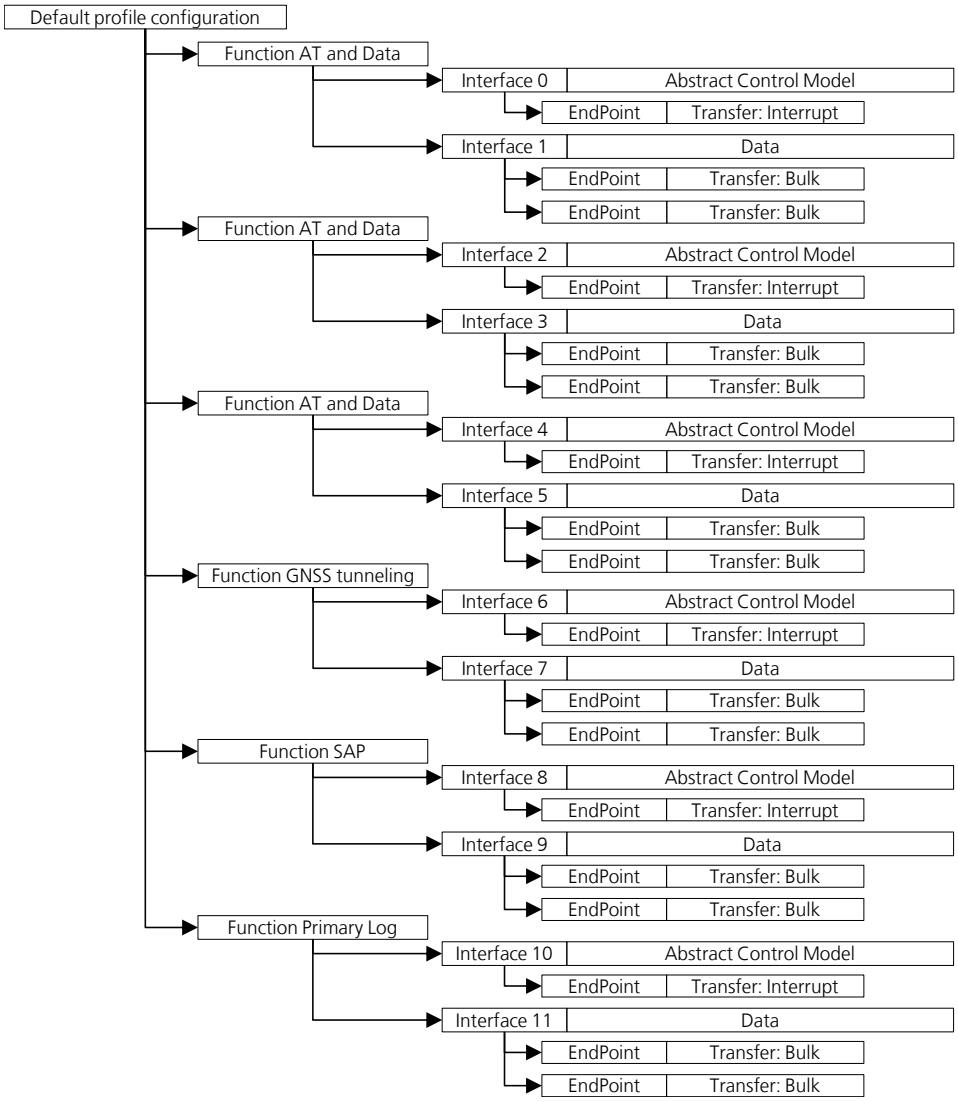


Figure 22: LARA-R2 series USB End-Points summary for the default USB profile configuration

1.9.2.2 USB in Windows

USB drivers are provided for Windows operating system platforms and should be properly installed / enabled by following the step-by-step instructions available in the EVK-R2xx User Guide [3] or in the Windows Embedded OS USB Driver Installation Application Note [4].

USB drivers are available for the following operating system platforms:

- Windows 7
- Windows 8
- Windows 8.1
- Windows 10
- Windows Embedded CE 6.0
- Windows Embedded Compact 7
- Windows Embedded Compact 2013

The module firmware can be upgraded over the USB interface by means of the FOAT feature, or using the u-blox EasyFlash tool (for more details see Firmware Update Application Note [23].

1.9.2.3 USB in Linux/Android

It is not required to install a specific driver for each Linux-based or Android-based operating system (OS) to use the module USB interface, which is compatible with standard Linux/Android USB kernel drivers.

The full capability and configuration of the module USB interface can be reported by running "lsusb –v" or an equivalent command available in the host operating system when the module is connected.

1.9.2.4 USB and power saving

The modules automatically enter the USB suspended state when the device has observed no bus traffic for a specific time period according to the USB 2.0 specifications [9]. In suspended state, the module maintains any USB internal status as device. In addition, the module enters the suspended state when the hub port it is attached to is disabled. This is referred to as USB selective suspend.

If the USB is suspended and a power saving configuration is enabled by the AT+UPSV command, the module automatically enters the low power idle-mode whenever possible but it wakes up to active-mode according to any required activity related to the network (e.g. the periodic paging reception described in section 1.5.1.4) or any other required activity related to the functions / interfaces of the module.

The USB exits suspend mode when there is bus activity. If the USB is connected and not suspended, the module is kept ready to communicate over USB regardless the AT+UPSV settings, therefore the AT+UPSV settings are overruled but they have effect on the power saving configuration of the other interfaces (see 1.9.1.4).

The modules are capable of USB remote wake-up signaling: i.e. it may request the host to exit suspend mode or selective suspend by using electrical signaling to indicate remote wake-up, for example due to incoming call, URCs, data reception on a socket. The remote wake-up signaling notifies the host that it should resume from its suspended mode, if necessary, and service the external event. Remote wake-up is accomplished using electrical signaling described in the USB 2.0 specifications [9].

For the module current consumption description with power saving enabled and USB suspended, or with power saving disabled and USB not suspended, see sections 1.5.1.4, 1.5.1.5 and LARA-R2 series Data Sheet [1].

The additional **VUSB_DET** input pin available on LARA-R2 series modules provides the complete bus detach functionality: the modules disable the USB interface when a low logic level is sensed after a high-to-low logic level transition on the **VUSB_DET** input pin. This allows a further reduction of the module current consumption, in particular as compared to the USB suspended status during low-power idle mode with power saving enabled.

1.9.3 HSIC interface

☞ The HSIC interface is not supported by "02" modules product versions except for diagnostic purpose.

1.9.3.1 HSIC features

LARA-R2 series modules include a USB High-Speed Inter-Chip compliant interface with maximum 480 Mb/s data rate according to the High-Speed Inter-Chip USB Electrical Specification Version 1.0 [10] and USB Specification Revision 2.0 [9]. The module itself acts as a device and can be connected to any compatible host.

The HSIC interface provides:

- AT command mode[13]
- Data mode and Online command mode[13]
- FW upgrades by means of the FOAT feature (see 1.14.13 and Firmware update application note [23])
- FW upgrades by means of the u-blox EasyFlash tool (see the Firmware update application note [23])
- Trace log capture (diagnostic purpose)

The HSIC interface consists of a bi-directional DDR data line (**HSIC_DATA**) for transmitting and receiving data synchronously with the bi-directional strobe line (**HSIC_STRB**).

The modules include also the **HOST_SELECT** pin to select the module / host application processor configuration: the pin is available to select, enable, connect, disconnect and subsequently re-connect the HSIC interface.

The USB interface is controlled and operated with:

- AT commands according to 3GPP TS 27.007 [6], 3GPP TS 27.005 [7]
- u-blox AT commands (for the complete list and syntax see the u-blox AT Commands Manual [2])

[13] See the u-blox AT Commands Manual [2] for the definition of the command mode, data mode, and online command mode.

1.9.4 DDC (I²C) interface

☞ Communication with u-blox GNSS receivers over I²C bus compatible Display Data Channel interface, AssistNow embedded GNSS positioning aiding, CellLocate® positioning through cellular info, and custom functions over GPIOs for the integration with u-blox positioning chips / modules are not supported by LARA-R2 series modules "02" product versions.

The **SDA** and **SCL** pins represent an I²C bus compatible Display Data Channel (DDC) interface available for

- communication with u-blox GNSS chips / modules,
- communication with other external I²C devices as audio codecs.

The AT commands interface is not available on the DDC (I²C) interface.

DDC (I²C) slave-mode operation is not supported: the LARA-R2 series module can act as I²C master that can communicate with more I²C slaves in accordance to the I²C bus specifications [11].

The DDC (I²C) interface pins of the module, serial data (**SDA**) and serial clock (**SCL**), are open drain outputs conforming to the I²C bus specifications [11].

u-blox has implemented special features to ease the design effort required for the integration of a u-blox cellular module with a u blox GNSS receiver.

Combining a u-blox cellular module with a u-blox GNSS receiver allows designers to have full access to the positioning receiver directly via the cellular module: it relays control messages to the GNSS receiver via a dedicated DDC (I²C) interface. A 2nd interface connected to the positioning receiver is not necessary: AT commands via the UART or USB serial interface of the cellular module allows a fully control of the GNSS receiver from any host processor.

The modules feature embedded GNSS aiding that is a set of specific features developed by u-blox to enhance GNSS performance, decreasing the Time To First Fix (TTFF), thus allowing to calculate the position in a shorter time with higher accuracy.

These GNSS aiding types are available:

- Local aiding
- AssistNow Online
- AssistNow Offline
- AssistNow Autonomous

The embedded GNSS aiding features can be used only if the DDC (I²C) interface of the cellular module is connected to the u-blox GNSS receivers.

The cellular modules provide additional custom functions over GPIO pins to improve the integration with u-blox positioning chips and modules. GPIO pins can handle:

- GNSS receiver power-on/off: "GNSS supply enable" function provided by **GPIO2** improves the positioning receiver power consumption. When the GNSS functionality is not required, the positioning receiver can be completely switched off by the cellular module that is controlled by AT commands
- The wake up from idle-mode when the GNSS receiver is ready to send data: "GNSS Tx data ready" function provided by **GPIO3** improves the cellular module power consumption. When power saving is enabled in the cellular module by the AT+UPSV command and the GNSS receiver does not send data by the DDC (I²C) interface, the module automatically enters idle-mode whenever possible. With the "GNSS Tx data ready" function the GNSS receiver can indicate to the cellular module that it is ready to send data by the DDC (I²C) interface: the positioning receiver can wake up the cellular module if it is in idle-mode, so the cellular module does not lose the data sent by the GNSS receiver even if power saving is enabled

- The RTC synchronization signal to the GNSS receiver: "GNSS RTC sharing" function provided by **GPIO4** improves GNSS receiver performance, decreasing the Time To First Fix (TTFF), and thus allowing to calculate the position in a shorter time with higher accuracy. When GPS local aiding is enabled, the cellular module automatically uploads data such as position, time, ephemeris, almanac, health and ionospheric parameter from the positioning receiver into its local memory, and restores this to the GNSS receiver at the next power up of the positioning receiver

☞ For more details regarding the handling of the DDC (I^2C) interface, the GNSS aiding features and the GNSS related functions over GPIOs, see section 1.12, to the u-blox AT Commands Manual [2] (AT+UGPS, AT+UGPRF, AT+UGPIOC AT commands) and the GNSS Implementation Application Note [22].

☞ "GNSS Tx data ready" and "GNSS RTC sharing" functions are not supported by all u-blox GNSS receivers HW or ROM/FW versions. See the GNSS Implementation Application Note [22] or to the Hardware Integration Manual of the u-blox GNSS receivers for the supported features.

As additional improvement for the GNSS receiver performance, the **V_BCKP** supply output of the cellular modules can be connected to the **V_BCKP** supply input pin of u-blox positioning chips and modules to provide the supply for the GNSS real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS receiver is disabled.

This enables the u-blox positioning receiver to recover from a power breakdown with either a hot start or a warm start (depending on the duration of the GNSS receiver **VCC** outage) and to maintain the configuration settings saved in the backup RAM.

1.9.5 SDIO interface

☞ Secure Digital Input Output interface is not supported by LARA-R2 series modules "02" product versions.

LARA-R2 series modules include a 4-bit Secure Digital Input Output interface (**SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK**, **SDIO_CMD**) designed to communicate with an external u-blox short range Wi-Fi module: the cellular module acts as an SDIO host controller which can communicate over the SDIO bus with a compatible u-blox short range radio communication Wi-Fi module acting as SDIO device.

The SDIO interface is the only one interface of LARA-R2 series modules dedicated for communication between the u-blox cellular module and the u-blox short range Wi-Fi module.

The AT commands interface is not available on the SDIO interface of LARA-R2 series modules.

Combining a u-blox cellular module with a u-blox short range communication module gives designers full access to the Wi-Fi module directly via the cellular module, so that a second interface connected to the Wi-Fi module is not necessary. AT commands via the AT interfaces of the cellular module allows a full control of the Wi-Fi module from any host processor, because Wi-Fi control messages are relayed to the Wi-Fi module via the dedicated SDIO interface.

u-blox has implemented special features in the cellular modules to ease the design effort for the integration of a u-blox cellular module with a u-blox short range Wi-Fi module to provide Router functionality.

Additional custom function over GPIO pins is designed to improve the integration with u-blox Wi-Fi modules:

- Wi-Fi enable Switch-on / switch-off the Wi-Fi

☞ Wi-Fi enable function over GPIO is not supported by LARA-R2 series modules "02" product versions.

1.10 Audio interface

☞ Audio is not supported by LARA-R204 module "02" product version.

1.10.1 Digital audio interface

LARA-R2 series modules include a 4-wire I²S digital audio interface (**I2S_TXD** data output, **I2S_RXD** data input, **I2S_CLK** clock input/output, **I2S_WA** world alignment / synchronization signal input/output), which can be configured by AT command for digital audio communication with external digital audio devices as an audio codec (for more details see the u-blox AT Commands Manual [2], +UI2S AT command).

The I²S interface can be alternatively set in different modes, by <I2S_mode> parameter of AT+UI2S command:

- PCM mode (short synchronization signal): I²S word alignment signal is set high for 1 or 2 clock cycles for the synchronization, and then is set low for 16 clock cycles according to the 17 or 18 clock cycles frame length.
- Normal I²S mode (long synchronization signal): I²S word alignment is set high / low with a 50% duty cycle (high for 16 clock cycles / low for 16 clock cycles, according to the 32 clock cycles frame length).

The I²S interface can be alternatively set in different roles, by <I2S_Master_Slave> parameter of AT+UI2S:

- Master mode
- Slave mode

The sample rate of transmitted/received words, which corresponds to the I²S word alignment / synchronization signal frequency, can be alternatively set by the <I2S_sample_rate> parameter of AT+UI2S to:

- 8 kHz
- 11.025 kHz
- 12 kHz
- 16 kHz
- 22.05 kHz
- 24 kHz
- 32 kHz
- 44.1 kHz
- 48 kHz

The modules support I²S transmit and I²S receive data 16-bit words long, linear, mono (or also dual mono in Normal I2S mode). Data is transmitted and read in 2's complement notation. MSB is transmitted and read first.

I²S clock signal frequency depends on the frame length, the sample rate and the selected mode of operation:

- 17 x <I2S_sample_rate> or 18 x <I2S_sample_rate> in PCM mode (short synchronization signal)
- 16 x 2 x <I2S_sample_rate> in Normal I2S mode (long synchronization signal)

☞ For the complete description of the possible configurations and settings of the I²S digital audio interface for PCM and Normal I²S modes refer to the u-blox AT Commands Manual [2], +UI2S AT command.

1.11 Clock output

LARA-R2 series modules provide master digital clock output function on **GPIO6** pin, which can be configured to provide a 13 MHz or 26 MHz square wave. This is mainly designed to feed the master clock input of an external audio codec, as the clock output can be configured in "Audio dependent" mode (generating the square wave only when the audio path is active), or in "Continuous" mode.

For more details see the u-blox AT Commands Manual [2], +UMCLK AT command.

1.12 General Purpose Input/Output (GPIO)

LARA-R2 series modules include 9 pins (**GPIO1**-**GPIO5**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**) which can be configured as General Purpose Input/Output or to provide custom functions via u-blox AT commands (for more details see the u-blox AT Commands Manual [2], +UGPIOC, +UGPIOR, +UGPIOW AT commands), as summarized in Table 12.

Function	Description	Default GPIO	Configurable GPIOs
Network status indication	Network status: registered home network, registered roaming, data transmission, no service	--	GPIO1-GPIO4
GNSS supply enable[14]	Enable/disable the supply of u-blox GNSS receiver connected to the cellular module	--	GPIO1-GPIO4
GNSS data ready[14]	Sense when u-blox GNSS receiver connected to the module is ready for sending data by the DDC (I^2C)	--	GPIO3
GNSS RTC sharing[14]	RTC synchronization signal to the u-blox GNSS receiver connected to the cellular module	--	GPIO4
SIM card detection	External SIM card physical presence detection	GPIO5	GPIO5
SIM card hot insertion/removal	Enable / disable SIM interface upon detection of external SIM card physical insertion / removal	--	GPIO5
I^2S digital audio interface[15]	I^2S digital audio interface	I2S_RXD, I2S_TXD, I2S_CLK, I2S_WA	I2S_RXD, I2S_TXD, I2S_CLK, I2S_WA
Wi-Fi control[14]	Control of an external Wi-Fi chip or module	--	--
General purpose input	Input to sense high or low digital level	--	All
General purpose output	Output to set the high or the low digital level	GPIO4	All
Pin disabled	Tri-state with an internal active pull-down enabled	GPIO1-GPIO3	All

Table 12: LARA-R2 series GPIO custom functions configuration

1.13 Reserved pins (RSVD)

LARA-R2 series modules have pins reserved for future use, named **RSVD**: they can all be left unconnected on the application board, except

- the **RSVD** pin number **33** that must be externally connected to ground

[14] Not supported by "02" product versions.
[15] Not supported by LARA-R204 module "02" product version.

1.14 System features

1.14.1 Network indication

GPIOs can be configured by the AT command to indicate network status (for further details see section 1.12 and to u-blox AT Commands Manual [2], GPIO commands):

- No service (no network coverage or not registered)
- Registered 2G / LTE home network
- Registered 2G / LTE visitor network (roaming)
- Call enabled (RF data transmission / reception)

1.14.2 Antenna detection

The antenna detection function provided by the **ANT_DET** pin is based on an ADC measurement as optional feature that can be implemented if the application requires it. The antenna supervisor is forced by the +UANTR AT command (see the u-blox AT Commands Manual [2] for more details).

The requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 1.7.2 for detailed antenna detection interface functional description and see section 2.4.2 for detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.14.3 Jamming detection

☞ Congestion detection (i.e. jamming detection) is not supported by "02" product versions.

In real network situations modules can experience various kind of out-of-coverage conditions: limited service conditions when roaming to networks not supporting the specific SIM, limited service in cells which are not suitable or barred due to operators' choices, no cell condition when moving to poorly served or highly interfered areas. In the latter case, interference can be artificially injected in the environment by a noise generator covering a given spectrum, thus obscuring the operator's carriers entitled to give access to the LTE/3G/2G service.

The congestion (i.e. jamming) detection feature can be enabled and configured by the +UCD AT command: the feature consists of detecting an anomalous source of interference and signaling the start and stop of such conditions to the host application processor with an unsolicited indication, which can react appropriately by e.g. switching off the radio transceiver of the module (i.e. configuring the module in "airplane mode" by means of the +CFUN AT command) in order to reduce power consumption and monitoring the environment at constant periods (for more details see the u-blox AT Commands Manual [2], +UCD AT command).

1.14.4 Dual stack IPv4/IPv6

LARA-R2 series support both Internet Protocol version 4 and Internet Protocol version 6 in parallel.

For more details about dual stack IPv4/IPv6 see the u-blox AT Commands Manual [2].

1.14.5 TCP/IP and UDP/IP

LARA-R2 series modules provide embedded TCP/IP and UDP/IP protocol stack: a PDP context can be configured, established and handled via the data connection management packet switched data commands.

LARA-R2 series modules provide Direct Link mode to establish a transparent end-to-end communication with an already connected TCP or UDP socket via serial interfaces. In Direct Link mode, data sent to the serial interface from an external application processor is forwarded to the network and vice-versa.

For more details about embedded TCP/IP and UDP/IP functionalities see the u-blox AT Commands Manual [2]

1.14.6 FTP

LARA-R2 series provide embedded File Transfer Protocol (FTP) services. Files are read and stored in the local file system of the module.

FTP files can also be transferred using FTP Direct Link:

- **FTP download**: data coming from the FTP server is forwarded to the host processor via serial interfaces (for FTP without Direct Link mode the data is always stored in the module's Flash File System)
- **FTP upload**: data coming from the host processor via serial interfaces is forwarded to the FTP server (for FTP without Direct Link mode the data is read from the module's Flash File System)

When Direct Link is used for a FTP file transfer, only the file content pass through USB / UART serial interface, whereas all the FTP commands handling is managed internally by the FTP application.

For more details about embedded FTP functionalities see u-blox AT Commands Manual [2].

1.14.7 HTTP

LARA-R2 series modules provide the embedded Hyper-Text Transfer Protocol (HTTP) services via AT commands for sending requests to a remote HTTP server, receiving the server response and transparently storing it in the module's Flash File System (FFS).

For more details about embedded HTTP functionalities see the u-blox AT Commands Manual [2].

1.14.8 SSL/TLS

LARA-R2 series modules support the Secure Sockets Layer (SSL) / Transport Layer Security (TLS) with certificate key sizes up to 4096 bits to provide security over the FTP and HTTP protocols.

The SSL/TLS support provides different connection security aspects:

- Server authentication: use of the server certificate verification against a specific trusted certificate or a trusted certificates list
- Client authentication: use of the client certificate and the corresponding private key
- Data security and integrity: data encryption and Hash Message Authentication Code (HMAC) generation

The security aspects used during a connection depend on the SSL/TLS configuration and features supported.

Table 13 contains the settings of the default SSL/TLS profile and Table 14 to Table 18 report the main SSL/TLS supported capabilities of the products. For a complete list of supported configurations and settings see the u-blox AT Commands Manual [2].

Settings	Value	Meaning
Certificates validation level	Level 0	The server certificate will not be checked or verified
Minimum SSL/TLS version	Any	The server can use any of the TLS1.0/TLS1.1/TLS1.2 versions for the connection
Cipher suite	Automatic	The cipher suite will be negotiated in the handshake process
Trusted root certificate internal name	None	No certificate will be used for the server authentication
Expected server host-name	None	No server host-name is expected
Client certificate internal name	None	No client certificate will be used
Client private key internal name	None	No client private key will be used
Client private key password	None	No client private key password will be used
Pre-shared key	None	No pre-shared key password will be used

Table 13: Default SSL/TLS profile

SSL/TLS Version	
SSL 2.0	NO
SSL 3.0	YES
TLS 1.0	YES
TLS 1.1	YES
TLS 1.2	YES

Table 14: SSL/TLS version support

Algorithm	
RSA	YES
PSK	YES

Table 15: Authentication

Algorithm	
RC4	NO
DES	YES
3DES	YES
AES128	YES
AES256	YES

Table 16: Encryption

Algorithm	
MD5	NO
SHA/SHA1	YES
SHA256	YES
SHA384	YES

Table 17: Message digest

Description	Registry value	
TLS_RSA_WITH_AES_128_CBC_SHA	0x00,0x2F	YES
TLS_RSA_WITH_AES_128_CBC_SHA256	0x00,0x3C	YES
TLS_RSA_WITH_AES_256_CBC_SHA	0x00,0x35	YES
TLS_RSA_WITH_AES_256_CBC_SHA256	0x00,0x3D	YES
TLS_RSA_WITH_3DES_EDE_CBC_SHA	0x00,0x0A	YES
TLS_RSA_WITH_RC4_128_MD5	0x00,0x04	NO
TLS_RSA_WITH_RC4_128_SHA	0x00,0x05	NO
TLS_PSK_WITH_AES_128_CBC_SHA	0x00,0x8C	YES
TLS_PSK_WITH_AES_256_CBC_SHA	0x00,0x8D	YES
TLS_PSK_WITH_3DES_EDE_CBC_SHA	0x00,0x8B	YES
TLS_RSA_PSK_WITH_AES_128_CBC_SHA	0x00,0x94	YES
TLS_RSA_PSK_WITH_AES_256_CBC_SHA	0x00,0x95	YES
TLS_RSA_PSK_WITH_3DES_EDE_CBC_SHA	0x00,0x93	YES
TLS_PSK_WITH_AES_128_CBC_SHA256	0x00,0xAE	YES
TLS_PSK_WITH_AES_256_CBC_SHA384	0x00,0xAF	YES
TLS_RSA_PSK_WITH_AES_128_CBC_SHA256	0x00,0xB6	YES
TLS_RSA_PSK_WITH_AES_256_CBC_SHA384	0x00,0xB7	YES

Table 18: TLS cipher suite registry

1.14.9 Bearer Independent Protocol

The Bearer Independent Protocol (BIP) is a mechanism by which a cellular module provides a SIM with access to the data bearers supported by the network. With the BIP for Over-the-Air SIM provisioning, the data transfer from and to the SIM uses either an already active PDP context or a new PDP context established with the APN provided by the SIM card. For more details, see the u-blox AT Commands Manual [2]..

1.14.10 AssistNow clients and GNSS integration

☞ AssistNow clients and u-blox GNSS receiver integration are not supported by "02" product versions.

For customers using u-blox GNSS receivers, the LARA-R2 series cellular modules feature embedded AssistNow clients. AssistNow A-GPS provides better GNSS performance and faster Time-To-First-Fix. The clients can be enabled and disabled with an AT command (see the u-blox AT Commands Manual [2]).

LARA-R2 series cellular modules act as a stand-alone AssistNow client, making AssistNow available with no additional requirements for resources or software integration on an external host micro controller. Full access to u-blox positioning receivers is available via the cellular modules, through a dedicated DDC (I^2C) interface, while the available GPIOs can handle the positioning chipset / module power-on/off. This means that the cellular module and the GNSS receiver can be controlled through a single serial port from any host processor.

1.14.11 Hybrid positioning and CellLocate®

☞ Hybrid positioning and CellLocate® are not supported by "02" product versions.

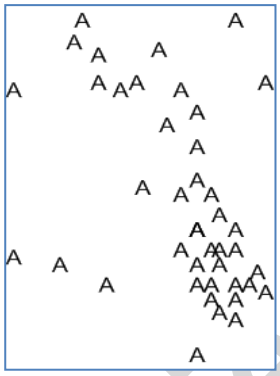
Although GNSS is a widespread technology, its reliance on the visibility of extremely weak GNSS satellite signals means that positioning is not always possible. Especially difficult environments for GNSS are indoors, in enclosed or underground parking garages, as well as in urban canyons where GNSS signals are blocked or jammed by multipath interference. The situation can be improved by augmenting GNSS receiver data with cellular network information to provide positioning information even when GNSS reception is degraded or absent. This additional information can benefit numerous applications.

Positioning through cellular information: CellLocate®

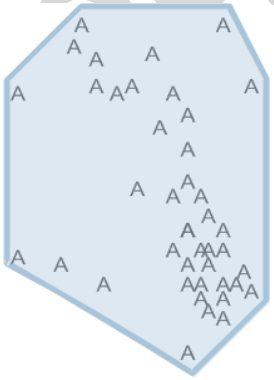
u-blox CellLocate® enables the device position estimation based on the parameters of the mobile network cells visible to the specific device. To estimate its position the u-blox cellular module sends the CellLocate® server the parameters of network cells visible to it using a UDP connection. In return the server provides the estimated position based on the CellLocate® database. The module can either send the parameters of the visible home network cells only (normal scan) or the parameters of all surrounding cells of all mobile operators (deep scan).

The CellLocate® database is compiled from the position of devices which observed, in the past, a specific cell or set of cells (historical observations) as follows:

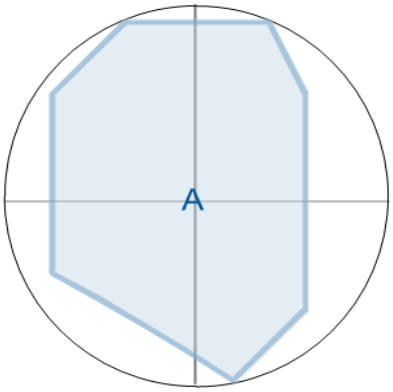
1. Several devices reported their position to the CellLocate® server when observing a specific cell (the As in the picture represent the position of the devices which observed the same cell A)



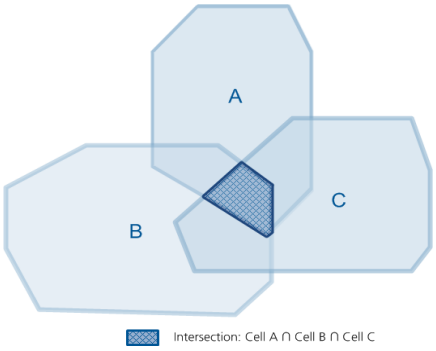
2. CellLocate® server defines the area of Cell A visibility



3. If a new device reports the observation of Cell A CellLocate® is able to provide the estimated position from the area of visibility



4. The visibility of multiple cells provides increased accuracy based on the intersection of areas of visibility.



CellLocate® is implemented using a set of two AT commands that allow configuration of the CellLocate® service (AT+ULOCCELL) and requesting position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy.

☞ The accuracy of the position estimated by CellLocate® depends on the availability of historical observations in the specific area.

Hybrid positioning

With u-blox hybrid positioning technology, u-blox cellular modules can be triggered to provide their current position using either a u-blox GNSS receiver or the position estimated from CellLocate®. The choice depends on which positioning method provides the best and fastest solution according to the user configuration, exploiting the benefit of having multiple and complementary positioning methods.

Hybrid positioning is implemented through a set of three AT commands that allow GNSS receiver configuration (AT+ULOCGNSS), CellLocate® service configuration (AT+ULOCCELL), and requesting the position according to the user configuration (AT+ULOC). The answer is provided in the form of an unsolicited AT command including latitude, longitude and estimated accuracy (if the position has been estimated by CellLocate®), and additional parameters if the position has been computed by the GNSS receiver.

The configuration of mobile network cells does not remain static (e.g. new cells are continuously added or existing cells are reconfigured by the network operators). For this reason, when a hybrid positioning method has been triggered and the GNSS receiver calculates the position, a database self-learning mechanism has been implemented so that these positions are sent to the server to update the database and maintain its accuracy.

The use of hybrid positioning requires a connection via the DDC (I^2C) bus between the cellular modules and the u-blox GNSS receiver (see section 2.6.4).

See GNSS Implementation Application Note [22] for the complete description of the feature.

☞ u-blox is extremely mindful of user privacy. When a position is sent to the CellLocate® server u-blox is unable to track the SIM used or the specific device.

1.14.12 Wi-Fi integration

☞ u-blox short range communication Wi-Fi modules integration is not supported by "02" product versions.

Full access to u-blox short range communication Wi-Fi modules is available through a dedicated SDIO interface (see sections 1.9.5 and 2.6.5). This means that combining a LARA-R2 series cellular module with a u-blox short range communication module gives designers full access to the Wi-Fi module directly via the cellular module, so that a second interface connected to the Wi-Fi module is not necessary.

AT commands via the AT interfaces of the cellular module (UART, USB) allows a full control of the Wi-Fi module from any host processor, because Wi-Fi control messages are relayed to the Wi-Fi module via the dedicated SDIO interface.

All the management software for Wi-Fi module operations runs inside the cellular module in addition to those required for cellular-only operation.

1.14.13 Firmware upgrade Over AT (FOAT)

This feature allows upgrading the module firmware over USB / UART serial interfaces, using AT commands.

- The +UFWUPD AT command triggers a reboot followed by the upgrade procedure at specified a baud rate
- A special boot loader on the module performs firmware installation, security verifications and module reboot
- Firmware authenticity verification is performed via a security signature during the download. The firmware is then installed, overwriting the current version. In case of power loss during this phase, the boot loader detects a fault at the next wake-up, and restarts the firmware download. After completing the upgrade, the module is reset again and wakes-up in normal boot

For more details about Firmware update Over AT procedure see the Firmware Update Application Note [23] and the u-blox AT Commands Manual [2], +UFWUPD AT command.

1.14.14 Firmware update Over The Air (FOTA)

This feature allows upgrading the module firmware over the LTE/3G/2G air interface.

In order to reduce the amount of data to be transmitted over the air, the implemented FOTA feature requires downloading only a "delta file" instead of the full firmware. The delta file contains only the differences between the two firmware versions (old and new), and is compressed. The firmware update procedure can be triggered using dedicated AT command with the delta file stored in the module file system via over the air FTP.

For more details about Firmware update Over The Air procedure see the Firmware Update Application Note [23] and the u-blox AT Commands Manual [2], .

1.14.15 Smart temperature management

Cellular modules – independently from the specific model – always have a well-defined operating temperature range. This range should be respected to guarantee full device functionality and long life span.

Nevertheless there are environmental conditions that can affect operating temperature, e.g. if the device is located near a heating/cooling source, if there is/is not air circulating, etc.

The module itself can also influence the environmental conditions; such as when it is transmitting at full power. In this case its temperature increases very quickly and can raise the temperature nearby.

The best solution is always to properly design the system where the module is integrated. Nevertheless an extra check/security mechanism embedded into the module is a good solution to prevent operation of the device outside of the specified range.

Smart Temperature Supervisor (STS)

The Smart Temperature Supervisor is activated and configured by a dedicated AT+USTS command. See u-blox AT Commands Manual [2] for more details. An URC indication is provided once the feature is enabled and at the module power on.

The cellular module measures the internal temperature (Ti) and its value is compared with predefined thresholds to identify the actual working temperature range.

☞ Temperature measurement is done inside the module: the measured value could be different from the environmental temperature (Ta).

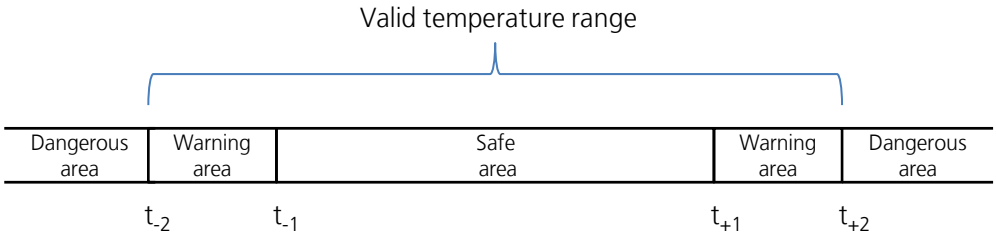


Figure 23: Temperature range and limits

The entire temperature range is divided into sub-regions by limits (see Figure 23) named t_{-2}, t_{-1}, t_{+1} and t_{+2}.

- Within the first limit, ($t_{-1} < Ti < t_{+1}$), the cellular module is in the normal working range, the Safe Area
- In the Warning Area, ($t_{-2} < Ti < t_{-1}$) or ($t_{+1} < Ti < t_{+2}$), the cellular module is still inside the valid temperature range, but the measured temperature is approaching the limit (upper or lower). The module sends a warning to the user (through the active AT communication interface), which can take, if possible, the necessary actions to return to a safer temperature range or simply ignore the indication. The module is still in a valid and good working condition
- Outside the valid temperature range, ($Ti < t_{-2}$) or ($Ti > t_{+2}$), the device is working outside the specified range and represents a dangerous working condition. This condition is indicated and the device shuts down to avoid damage

☞ For security reasons the shutdown is suspended in case an emergency call is in progress. In this case the device switches off at call termination.

☞ The user can decide at anytime to enable/disable the Smart Temperature Supervisor feature. If the feature is disabled there is no embedded protection against disallowed temperature conditions.

Figure 24 shows the flow diagram implemented for the Smart Temperature Supervisor.

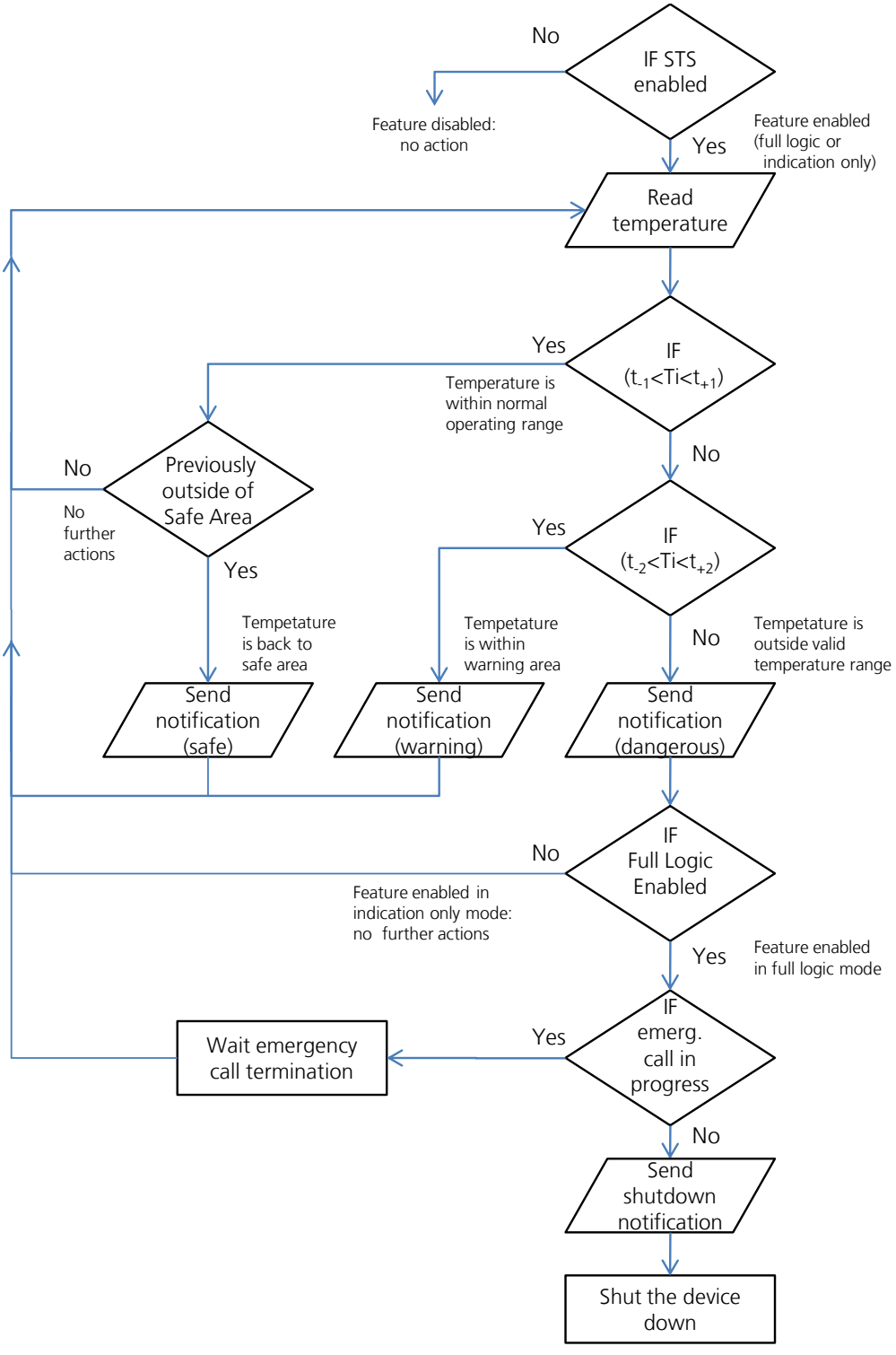


Figure 24: Smart Temperature Supervisor (STS) flow diagram

Threshold definitions

When the application of cellular module operates at extreme temperatures with Smart Temperature Supervisor enabled, the user should note that outside the valid temperature range the device will automatically shut down as described above.

The input for the algorithm is always the temperature measured within the cellular module (Ti, internal). This value can be higher than the working ambient temperature (Ta, ambient), since (for example) during transmission at maximum power a significant fraction of DC input power is dissipated as heat. This behavior is partially compensated by the definition of the upper shutdown threshold (t_{+2}) that is slightly higher than the declared environmental temperature limit.

☞ The sensor measures board temperature inside the shields, which can differ from ambient temperature.

1.14.16 Power Saving

The power saving configuration is by default disabled, but it can be enabled using the AT+UPSV command (for the complete description of the AT+UPSV command, see the u-blox AT Commands Manual [2]).

When power saving is enabled, the module automatically enters the low power idle-mode whenever possible, reducing current consumption (see section 1.5.1.4, LARA-R2 series Data Sheet [1]).

During the low power idle-mode, the module is temporarily not ready to communicate with an external device, as it is configured to reduce power consumption. The module wakes up from low power idle-mode to active-mode in the following events:

- Automatic periodic monitoring of the paging channel for the paging block reception according to network conditions (see 1.5.1.4, 1.9.1.4)
- Automatic periodic enable of the UART interface to receive / send data, with AT+UPSV=1 (see 1.9.1.4)
- **RTS** input set ON by the host DTE, with HW flow control disabled and AT+UPSV=2 (see 1.9.1.4)
- **DTR** input set ON by the host DTE, with AT+UPSV=3 (see 1.9.1.4)
- USB detection, applying 5 V (typ.) to **VUSB_DET** input (see 1.9.2)
- The connected USB host forces a remote wakeup of the module as USB device (see 1.9.2.4)
- The connected u-blox GNSS receiver forces a wakeup of the cellular module using the GNSS Tx data ready function over **GPIO3** (see 1.9.4)
- The connected SDIO device forces a wakeup of the module as SDIO host (see 1.9.5)
- A preset RTC alarm occurs (see u-blox AT Commands Manual [2], AT+CALA)

For the definition and the description of LARA-R2 series modules operating modes, including the events forcing transitions between the different operating modes, see the section 1.4.

2 Design-in

2.1 Overview

For an optimal integration of LARA-R2 series modules in the final application board follow the design guidelines stated in this section.

Every application circuit must be properly designed to guarantee the correct functionality of the related interface, however a number of points require higher attention during the design of the application device.

The following list provides a ranking of importance in the application design, starting from the highest relevance:

1. Module antenna connection: **ANT1**, **ANT2** and **ANT_DET** pins.
   Antenna circuit directly affects the RF compliance of the device integrating a LARA-R2 series module with the applicable certification schemes. Very carefully follow the suggestions provided in section 2.4 for schematic and layout design.
2. Module supply: **VCC** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a LARA-R2 series module with applicable certification schemes as well as antenna circuit design. Very carefully follow the suggestions provided in section 2.2.1 for schematic and layout design.
3. USB interface: **USB_D+**, **USB_D-** and **VUSB_DET** pins.
   Accurate design is required to guarantee USB 2.0 high-speed interface functionality. Carefully follow the suggestions provided in the related section 2.6.1 for schematic and layout design.
4. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**, **SIM_DET** pins.
   Accurate design is required to guarantee SIM card functionality and compliance with applicable conformance standards, reducing also the risk of RF coupling. Carefully follow the suggestions provided in section 2.5 for schematic and layout design.
5. HSIC interface: **HSIC_DATA**, **HSIC_STRB** pins.
   Accurate design is required to guarantee HSIC interface functionality. Carefully follow the suggestions provided in the relative section 2.6.3 for schematic and layout design.
6. SDIO interface: **SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK**, **SDIO_CMD** pins.
   Accurate design is required to guarantee SDIO interface functionality. Carefully follow the suggestions provided in the relative section 2.6.5 for schematic and layout design.
7. System functions: **RESET_N**, **PWR_ON** pins.
   Accurate design is required to guarantee that the voltage level is well defined during operation. Carefully follow the suggestions provided in section 2.3 for schematic and layout design.
8. Other digital interfaces: UART, I^2C, I^2S, Host Select, GPIOs, and Reserved pins.
   Accurate design is required to guarantee proper functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6.1, 2.6.4, 2.7.1, 2.3.3, 2.8 and 2.9 for schematic and layout design.
9. Other supplies: the **V_BCKP** RTC supply input/output and the **V_INT** digital interfaces supply output.
   Accurate design is required to guarantee proper functionality. Follow the suggestions provided in sections 2.2.2 and 2.2.3 for schematic and layout design.

☞ It is recommended to follow the specific design guidelines provided by each manufacturer of any external part selected for the application board integrating the u-blox cellular modules.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins have to be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected but connect all the available pins to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

LARA-R2 series modules must be supplied through the **VCC** pins by a proper DC power supply that should comply with the module **VCC** requirements summarized in Table 6.

The proper DC power supply can be selected according to the application requirements (see Figure 25) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

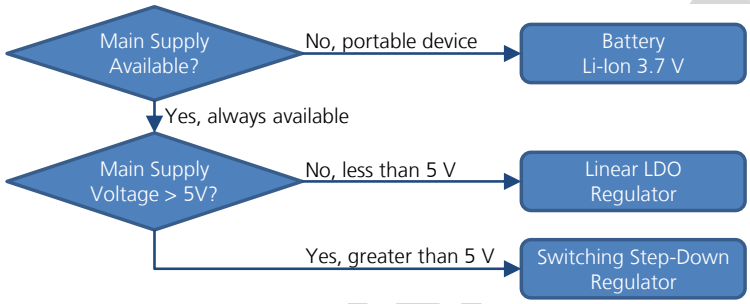


Figure 25: VCC supply concept selection

The DC/DC switching step-down regulator is the typical choice when the available primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the modules **VCC** operating supply voltage. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See sections 2.2.1.2 and 2.2.1.6, 0, 2.2.1.12 for specific design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less than 5 V). In this case the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See sections 2.2.1.3 and 2.2.1.6, 0, 2.2.1.12 for specific design-in.

If LARA-R2 series modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.6, 2.2.1.7, 0, 2.2.1.12 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit which is not included in the modules. The charger circuit has to be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements: a DC/DC switching charger is the typical choice when the charging source has an high nominal voltage (e.g. ~12 V), whereas a linear charger is

the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a proper charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.8, 2.2.1.9, and 2.2.1.4, 2.2.1.6, 2.2.1.7, 0, 2.2.1.12 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected taking into account the maximum current specified in LARA-R2 series Data Sheet [1] during connected-mode, considering that primary cells might have weak power capability. See sections 2.2.1.5, 2.2.1.6, 0, and 2.2.1.12 for specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The usage of a regulator or a battery not able to support the highest peak of **VCC** current consumption specified in the LARA-R2 series Data Sheet [1] is generally not recommended. However, if the selected regulator or battery is not able to support the highest peak current of the module, it must be able to support with adequate margin at least the highest averaged current consumption value specified in the LARA-R2 series Data Sheet [1]. The additional energy required by the module during a 2G Tx slot can be provided by an appropriate bypass tank capacitor or super-capacitor with very large capacitance and very low ESR placed close to the module **VCC** pins. Depending on the actual capability of the selected regulator or battery, the required capacitance can be considerably larger than 1 mF and the required ESR can be in the range of few tens of mΩ. Carefully evaluate the super-capacitor characteristics since aging and temperature may affect the actual characteristics.

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 6.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail to the **VCC** value is high: switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the specified maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in LARA-R2 series Data Sheet [1]
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **High switching frequency:** for best performance and for smaller applications it is recommended to select a switching frequency ≥ 600 kHz (since L-C output filter is typically smaller for high switching frequency). The use of a switching regulator with a variable switching frequency or with a switching frequency lower than 600 kHz must be carefully evaluated since this can produce noise in the **VCC** voltage profile and therefore negatively impact LTE/2G modulation spectrum performance. An additional L-C low-pass filter between the switching regulator output to **VCC** supply pins can mitigate the ripple on **VCC**, but adds extra voltage drop due to resistive losses on series inductors.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected-mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce noise on **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the idle/active-modes to connected-mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 26 and the components listed in Table 19 show an example of a high reliability power supply circuit, where the module **VCC** is supplied by a step-down switching regulator capable of delivering to **VCC** pins the specified maximum peak / pulse current, with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

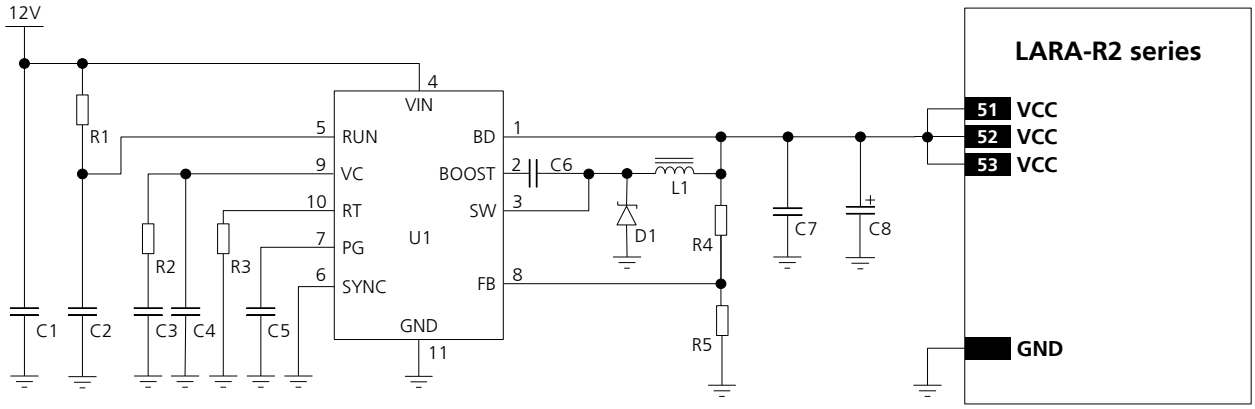


Figure 26: Example of high reliability VCC supply application circuit using a step-down regulator

Reference	Description	Part Number - Manufacturer
C1	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB - TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 - Murata
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220JZ01 - Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C6	470 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E474KA12 - Murata
C7	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C8	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G - ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 - Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	2322-705-87474-L - Yageo
R2	15 kΩ Resistor 0402 5% 0.1 W	2322-705-87153-L - Yageo
R3	22 kΩ Resistor 0402 5% 0.1 W	2322-705-87223-L - Yageo
R4	390 kΩ Resistor 0402 1% 0.063 W	RC0402FR-07390KL - Yageo
R5	100 kΩ Resistor 0402 5% 0.1 W	2322-705-70104-L - Yageo
U1	Step-Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF - Linear Technology

Table 19: Components for high reliability VCC supply application circuit circuit using a step-down regulator

Figure 27 and the components listed in Table 20 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by a step-down switching regulator capable of delivering to **VCC** pins the specified maximum peak / pulse current, transforming a 12 V supply input.

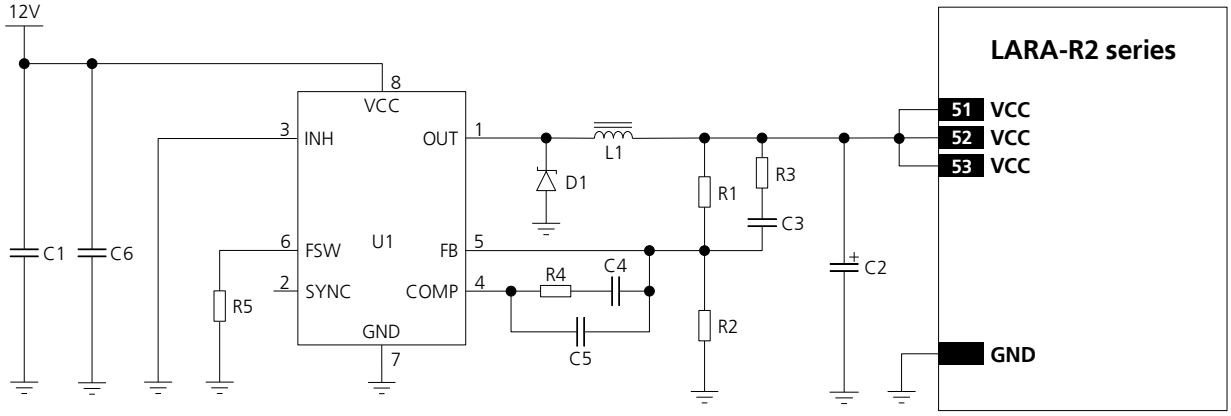


Figure 27: Example of low cost VCC supply application circuit using step-down regulator

Reference	Description	Part Number - Manufacturer
C1	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 – Murata
C2	100 µF Capacitor Tantalum B_SIZE 20% 6.3V 15mΩ	T520B107M006ATE015 – Kemet
C3	5.6 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H562KA88 – Murata
C4	6.8 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H682KA88 – Murata
C5	56 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H560JA01 – Murata
C6	220 nF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E224KA88 – Murata
D1	Schottky Diode 25V 2 A	STPS2L25 – STMicroelectronics
L1	5.2 µH Inductor 30% 5.28A 22 mΩ	MSS1038-522NL – Coilcraft
R1	4.7 kΩ Resistor 0402 1% 0.063 W	RC0402FR-074K7L – Yageo
R2	910 Ω Resistor 0402 1% 0.063 W	RC0402FR-07910RL – Yageo
R3	82 Ω Resistor 0402 5% 0.063 W	RC0402JR-0782RL – Yageo
R4	8.2 kΩ Resistor 0402 5% 0.063 W	RC0402JR-078K2L – Yageo
R5	39 kΩ Resistor 0402 5% 0.063 W	RC0402JR-0739KL – Yageo
U1	Step-Down Regulator 8-VFQFPN 3 A 1 MHz	L5987TR – ST Microelectronics

Table 20: Components for low cost VCC supply application circuit using a step-down regulator

2.2.1.3 Guidelines for VCC supply circuit design using a Low Drop-Out (LDO) linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the LDO linear regulator connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in LARA-R2 series Data Sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the maximum rated operating range (i.e. check the voltage drop from the max input voltage to the min output voltage to evaluate the power dissipation of the regulator).

Figure 28 and the components listed in Table 21 show an example of a high reliability power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified highest peak / pulse current, with proper power handling capability. The regulator described in this example supports a wide input voltage range, and it includes internal circuitry for reverse battery protection, current limiting, thermal limiting and reverse current protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V as in the circuit described in Figure 28 and Table 21). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

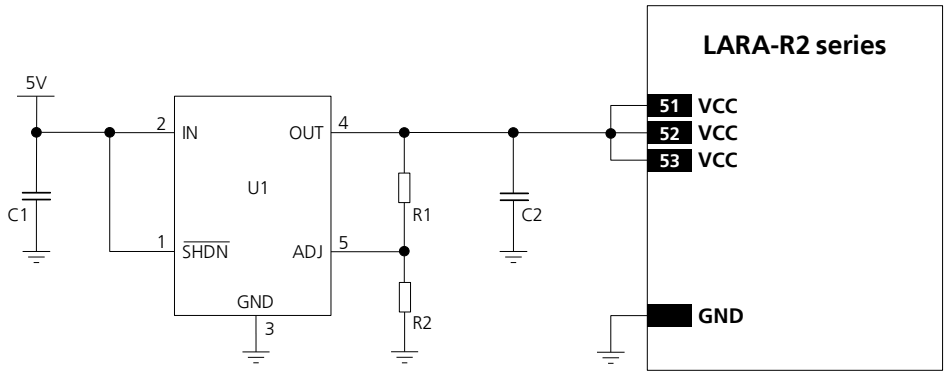


Figure 28: Example of high reliability VCC supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	9.1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-079K1L - Yageo Phycomp
R2	3.9 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K9L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LT1764AEQ#PBF - Linear Technology

Table 21: Components for high reliability VCC supply application circuit using an LDO linear regulator

Figure 29 and the components listed in Table 22 show an example of a low cost power supply circuit, where the **VCC** module supply is provided by an LDO linear regulator capable of delivering the specified highest peak / pulse current, with proper power handling capability. The regulator described in this example supports a limited input voltage range and it includes internal circuitry for current and thermal protection.

It is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module VCC normal operating range (e.g. ~4.1 V as in the circuit described in Figure 29 and Table 22). This reduces the power on the linear regulator and improves the whole thermal design of the supply circuit.

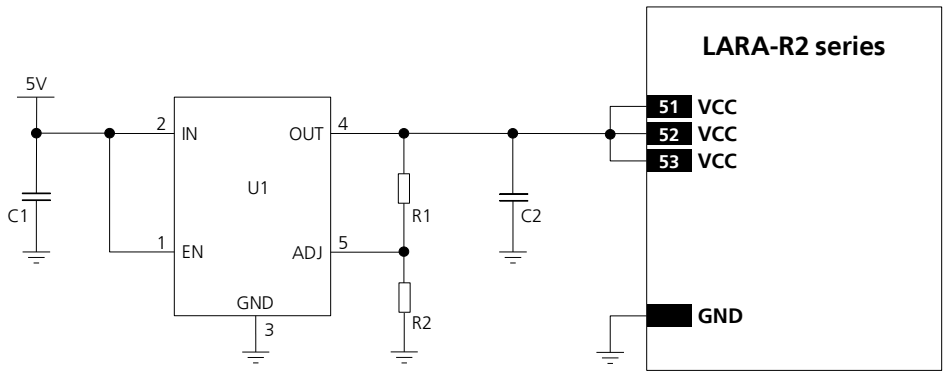


Figure 29: Example of low cost VCC supply application circuit using an LDO linear regulator

Reference	Description	Part Number - Manufacturer
C1, C2	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
R1	27 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0727KL - Yageo Phycomp
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
U1	LDO Linear Regulator ADJ 3.0 A	LP38501ATJ-ADJ/NOPB - Texas Instrument

Table 22: Components for low cost VCC supply application circuit using an LDO linear regulator

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable Li-Ion or Li-Pol battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering a pulse current as the maximum peak / pulse current consumption during Tx burst at maximum Tx power specified in LARA-R2 series Data Sheet [1] and must be capable of extensively delivering a DC current as the maximum average current consumption specified in LARA-R2 series Data Sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 6 during transmit bursts.

2.2.1.5 Guidelines for VCC supply circuit design using a primary (disposable) battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering a pulse current as the maximum peak current consumption during Tx burst at maximum Tx power specified in LARA-R2 series Data Sheet [1] and must be capable of extensively delivering a DC current as the maximum average current consumption specified in LARA-R2 series Data Sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the max DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 6 during transmit bursts.

2.2.1.6 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the power supply lines (connected to the **VCC** and **GND** pins of the module) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize power losses.

Three pins are allocated for **VCC** supply. Several pins are designated for **GND** connection. It is recommended to properly connect all of them to supply the module to minimize series resistance losses.

In case of modules supporting 2G radio access technology, to avoid voltage drop undershoot and overshoot at the start and end of a transmit burst during a GSM call (when current consumption on the **VCC** supply can rise up as specified in the LARA-R2 series Data Sheet [1]), place a bypass capacitor with large capacitance (at least 100 µF) and low ESR near the **VCC** pins, for example:

- 330 µF capacitance, 45 mΩ ESR (e.g. KEMET T520D337M006ATE045, Tantalum Capacitor)

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 68 pF capacitor with Self-Resonant Frequency in 800/900 MHz range (e.g. Murata GRM1555C1E560J)
- 15 pF capacitor with Self-Resonant Frequency in 1800/1900 MHz range (e.g. Murata GRM1555C1E150J)
- 8.2 pF capacitor with Self-Resonant Frequency in 2500/2600 MHz range (e.g. Murata GRM1555C1H8R2D)
- 10 nF capacitor (e.g. Murata GRM155R71C103K) to filter digital logic noise from clocks and data sources
- 100 nF capacitor (e.g Murata GRM155R61C104K) to filter digital logic noise from clocks and data sources

A suitable series ferrite bead can be properly placed on the **VCC** line for additional noise filtering if required by the specific application according to the whole application board design.

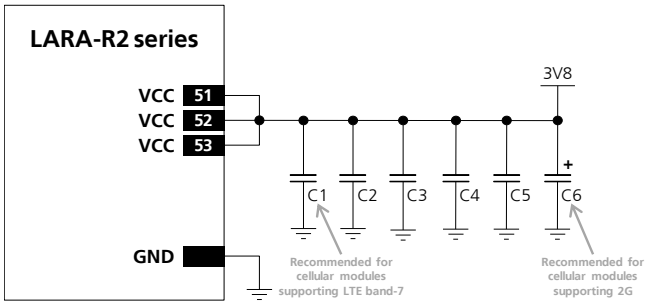


Figure 30: Suggested schematic for the VCC bypass capacitors to reduce ripple / noise on supply voltage profile

Reference	Description	Part Number - Manufacturer
C1	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C2	15 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H150JA01 - Murata
C3	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C4	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
C6	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET

Table 23: Suggested components to reduce ripple / noise on VCC

☞ The necessity of each part depends on the specific design, but it is recommended to provide all the bypass capacitors described in Figure 30 / Table 23 if the application device integrates an internal antenna.

☞ ESD sensitivity rating of the **VCC** supply pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to **VCC** pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

2.2.1.7 Additional guidelines for VCC supply circuit design of LARA-R211 modules

LARA-R211 modules provide separate supply inputs over the **VCC** pins (see Figure 3):

- **VCC** pins #52 and #53 represent the supply input for the internal RF power amplifier, demanding most of the total current drawn of the module when RF transmission is enabled during a voice/data call
- **VCC** pin #51 represents the supply input for the internal baseband Power Management Unit and the internal transceiver, demanding minor part of the total current drawn of the module when RF transmission is enabled during a voice/data call

All the **VCC** pins are in general intended to be connected to the same external power supply circuit, but separate supply sources can be implemented for specific (e.g. battery-powered) applications considering that the voltage at the **VCC** pins #52 and #53 can drop to a value lower than the one at the **VCC** pin #51, keeping the module still switched-on and functional. Figure 31 describes a possible application circuit.

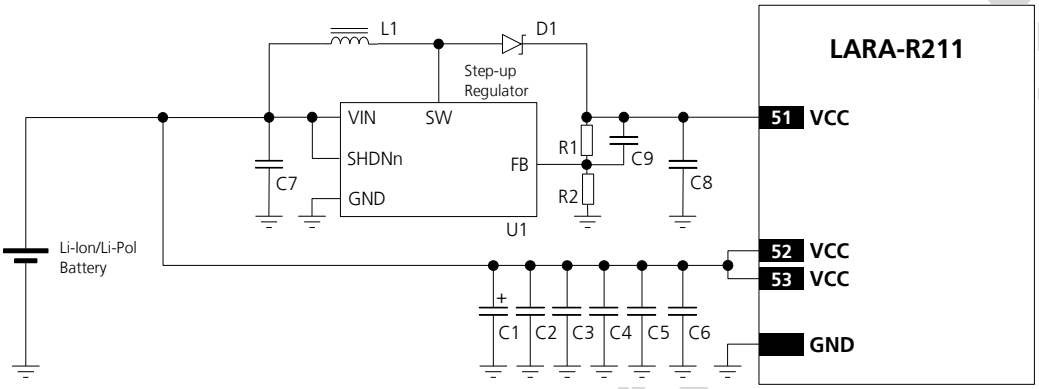


Figure 31: VCC circuit example with separate supply for LARA-R211 modules

Reference	Description	Part Number - Manufacturer
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C4	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C5	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C6	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C7	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 - Murata
C8	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C9	10 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E100JA01 - Murata
D1	Schottky Diode 40 V 1 A	SS14 - Vishay General Semiconductor
L1	10 µH Inductor 20% 1 A 276 mΩ	SRN3015-100M - Bourns Inc.
R1	1 MΩ Resistor 0402 5% 0.063 W	RC0402FR-071ML - Yageo Phycomp
R2	412 kΩ Resistor 0402 5% 0.063 W	RC0402FR-07412KL - Yageo Phycomp
U1	Step-up Regulator 350 mA	AP3015 - Diodes Incorporated

Table 24: Example of components for VCC circuit with separate supply for LARA-R211 modules

2.2.1.8 Guidelines for external battery charging circuit

LARA-R2 series modules do not have an on-board charging circuit. Figure 32 provides an example of a battery charger design, suitable for applications that are battery powered with a Li-Ion (or Li-Polymer) cell.

In the application circuit, a rechargeable Li-Ion (or Li-Polymer) battery cell, that features proper pulse and DC discharge current capabilities and proper DC series resistance, is directly connected to the **VCC** supply input of

the module. Battery charging is completely managed by the STMicroelectronics L6924U Battery Charger IC that, from a USB power source (5.0 V typ.), charges as a linear charger the battery, in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for USB power source (~500 mA)
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the L6924U starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor to ~15 mA or when the charging timer reaches the value configured by an external capacitor to ~9800 s

Using a battery pack with an internal NTC resistor, the L6924U can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The L6924U, as linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see the following section 2.2.1.9 for specific design-in).

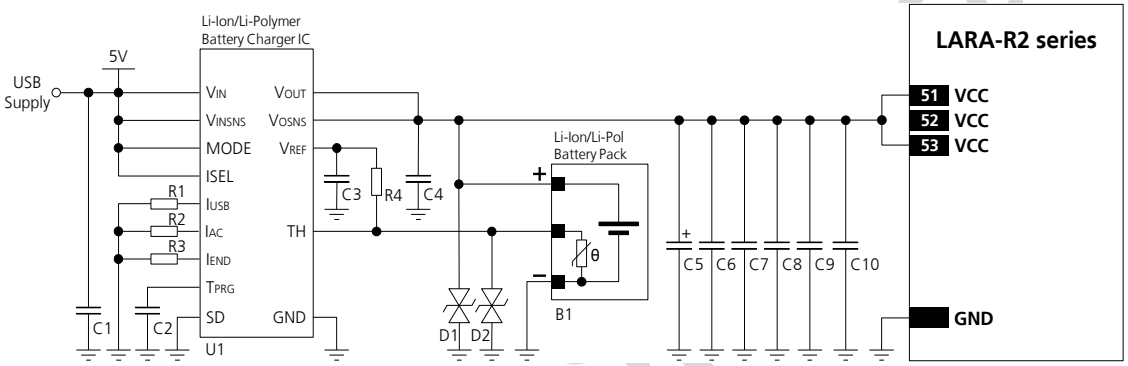


Figure 32: Li-Ion (or Li-Polymer) battery charging application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 470 Ω NTC	Various manufacturer
C1, C4	1 µF Capacitor Ceramic X7R 0603 10% 16 V	GRM188R71C105KA12 - Murata
C2, C6	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	1 nF Capacitor Ceramic X7R 0402 10% 50 V	GRM155R71H102KA01 - Murata
C5	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C7	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C8	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C9	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C10	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R2	24 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0724KL - Yageo Phycomp
R3	3.3 kΩ Resistor 0402 5% 0.1 W	RC0402JR-073K3L - Yageo Phycomp
R4	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
U1	Single Cell Li-Ion (or Li-Polymer) Battery Charger IC for USB port and AC Adapter	L6924U - STMicroelectronics

Table 25: Suggested components for Li-Ion (or Li-Polymer) battery charging application circuit

2.2.1.9 Guidelines for external battery charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source should implement a

suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 33 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system: the power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 6:

- High efficiency internal step down converter, compliant with the performances specified in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

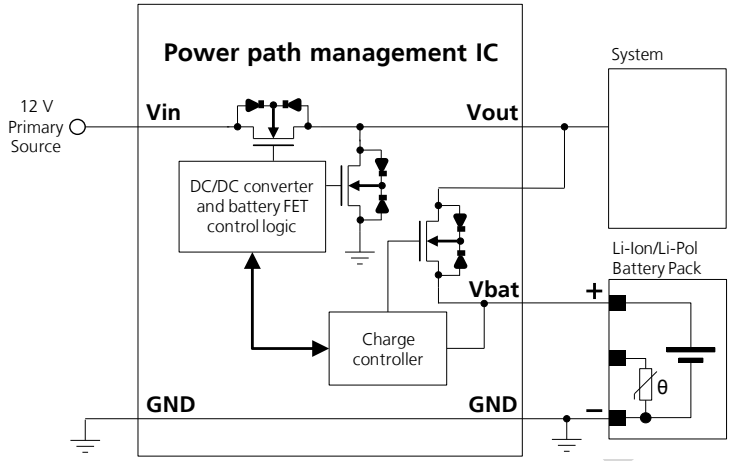


Figure 33: Charger / regulator with integrated power path management circuit block diagram

Figure 34 and the components listed in Table 26 provide an application circuit example where the MPS MP2617 switching charger / regulator with integrated power path management function provides the supply to the cellular module while concurrently and autonomously charging a suitable Li-Ion (or Li-Polymer) battery with proper pulse and DC discharge current capabilities and proper DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617 IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617 IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current

- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor

Using a battery pack with an internal NTC resistor, the MP2617 can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: proper resistors or capacitors have to be accordingly connected to the related pins of the IC.

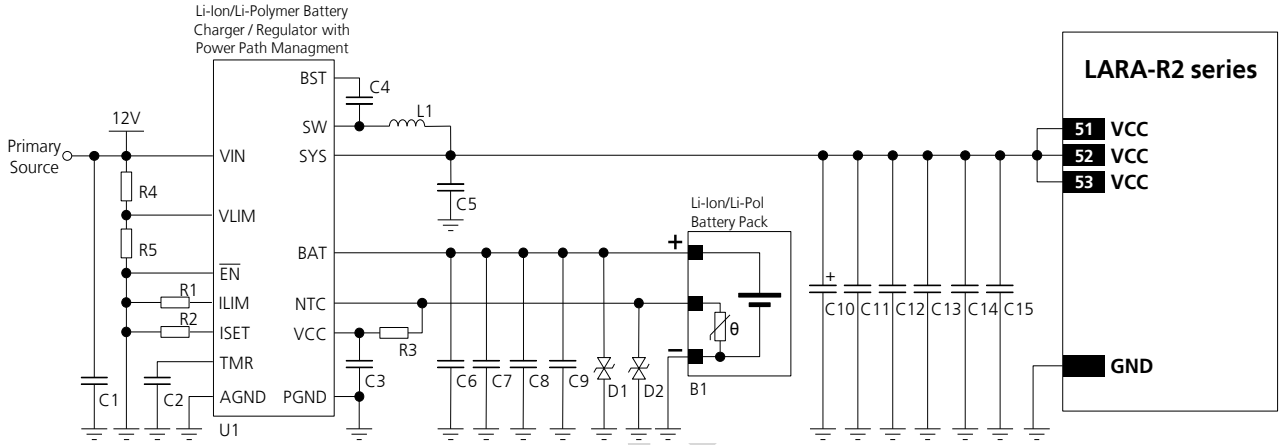


Figure 34: Li-Ion (or Li-Polymer) battery charging and power path management application circuit

Reference	Description	Part Number - Manufacturer
B1	Li-Ion (or Li-Polymer) battery pack with 10 kΩ NTC	Various manufacturer
C1, C5, C6	22 µF Capacitor Ceramic X5R 1210 10% 25 V	GRM32ER61E226KE15 - Murata
C2, C4, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C3	1 µF Capacitor Ceramic X7R 0603 10% 25 V	GRM188R71E105KA12 - Murata
C7, C13	68 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H680JA01 - Murata
C8, C14	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C9, C15	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata
C10	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C12	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
D1, D2	Low Capacitance ESD Protection	CG0402MLE-18G - Bourns
R1, R3, R5	10 kΩ Resistor 0402 5% 1/16 W	RC0402JR-0710KL - Yageo Phycomp
R2	1.0 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071K0L - Yageo Phycomp
R4	22 kΩ Resistor 0402 5% 1/16 W	RC0402JR-0722KL - Yageo Phycomp
L1	1.2 µH Inductor 6 A 21 mΩ 20%	7447745012 - Wurth
U1	Li-Ion/Li-Polymer Battery DC/DC Charger / Regulator with integrated Power Path Management function	MP2617 - Monolithic Power Systems (MPS)

Table 26: Suggested components for Li-Ion (or Li-Polymer) battery charging and power path management application circuit

2.2.1.10 Guidelines for removing VCC supply

As described in section 1.6.2 and Figure 14, the **VCC** supply can be removed after the end of LARA-R2 series modules internal power-off sequence, which has to be properly started sending the AT+CPWROFF command (see u-blox AT Commands Manual [2]).

Removing the **VCC** power can be useful in order to minimize the current consumption when the LARA-R2 series modules are switched off. Then, the modules can be switched on again by re-applying the **VCC** supply.

If the **VCC** supply is generated by a switching or an LDO regulator, the application processor may control the input pin of the regulator which is provided to enable / disable the output of the regulator (as for example the RUN input pin for the regulator described in Figure 26, the INH input pin for the regulator described in Figure 27, the SHDNn input pin for the regulator described in Figure 28, the EN input pin for the regulator described in Figure 29), in order to apply / remove the **VCC** supply.

If the regulator that generates the **VCC** supply does not provide an on / off pin, or for other applications such as the battery-powered ones, the **VCC** supply can be switched off using an appropriate external p-channel MOSFET controlled by the application processor by means of a proper inverting transistor as shown in Figure 35, given that the external p-channel MOSFET has provide:

- Very low $R_{DS(ON)}$ (for example, less than 50 mΩ), to minimize voltage drops
- Adequate maximum Drain current (see LARA-R2 series Data Sheet [1] for module consumption figures)
- Low leakage current, to minimize the current consumption

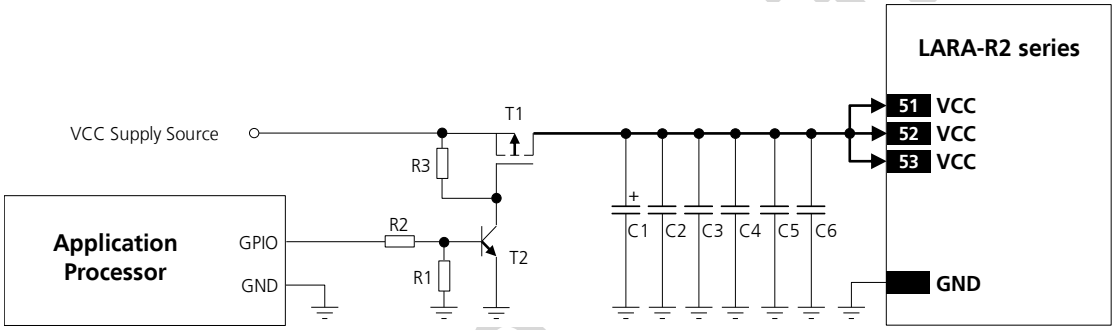


Figure 35: Example of application circuit for VCC supply removal

Reference	Description	Part Number - Manufacturer
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R2	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R3	100 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07100KL - Yageo Phycomp
T1	P-Channel MOSFET Low On-Resistance	AO3415 - Alpha & Omega Semiconductor Inc.
T2	NPN BJT Transistor	BC847 - Infineon
C1	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 - Murata
C3	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
C4	56 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E560JA01 - Murata
C5	15 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1E150JA01 - Murata
C6	8.2 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H8R2DZ01 - Murata

Table 27: Components for VCC supply removal application circuit

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during LARA-R2 series modules normal operations: the power off procedure must be started by the AT+CPWROFF command, waiting the command response for a proper time period (see u-blox AT Commands Manual [2]), and then a proper **VCC** supply has to be held at least until the end of the modules' internal power off sequence, which occurs when the generic digital interfaces supply output (**V_INT**) is switched off by the module.

2.2.1.11 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- **VCC** connection must be as wide as possible and as short as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between **VCC** track and other signal routing.
- Coupling between **VCC** and audio lines (especially microphone inputs) must be avoided, because the typical GSM burst has a periodic nature of approx. 217 Hz, which lies in the audible audio range.
- The tank bypass capacitor with low ESR for current spikes smoothing described in section 2.2.1.6 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize the **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and cellular module tank capacitor.
- The bypass capacitors in the pF range described in section 2.2.1.6 should be placed as close as possible to the **VCC** pins. This is highly recommended if the application device integrates an internal antenna.
- Since **VCC** is directly connected to RF Power Amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the LARA-R2 series modules in the worst case.
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the cellular module, preferably closer to the DC source (otherwise protection functionality may be compromised).

2.2.1.12 Guidelines for grounding layout design

Good connection of the module **GND** pins with application board solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

- Connect each **GND** pin with application board solid GND layer. It is strongly recommended that each **GND** pin surrounding **VCC** pins have one or more dedicated via down to the application board solid ground layer.
- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- It is recommended to implement one layer of the application board as ground plane as wide as possible.
- If the application board is a multilayer PCB, then all the board layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board. Use as many vias as possible to connect the ground planes
- Provide a dense line of vias at the edges of each ground area, in particular along RF and high speed lines
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.
- Good grounding of **GND** pins also ensures thermal heat sink. This is critical during call connection, when the real network commands the module to transmit at maximum power: proper grounding helps prevent module overheating.

2.2.2 RTC supply (V_BCKP)

2.2.2.1 Guidelines for V_BCKP circuit design

LARA-R2 series modules provide the **V_BCKP** RTC supply input/output, which can be mainly used to:

- Provide RTC back-up when **VCC** supply is removed

If RTC timing is required to run for a time interval of T [s] when **VCC** supply is removed, place a capacitor with a nominal capacitance of C [µF] at the **V_BCKP** pin. Choose the capacitor using the following formula:

C [µF] = (Current_Consumption [µA] x T [s]) / Voltage_Drop [V]

= 2.5 x T [s]

For example, a 100 µF capacitor can be placed at **V_BCKP** to provide RTC backup holding the **V_BCKP** voltage within its valid range for around 40 s at 25 °C, after the **VCC** supply is removed. If a longer buffering time is required, a 70 mF super-capacitor can be placed at **V_BCKP**, with a 4.7 kΩ series resistor to hold the **V_BCKP** voltage within its valid range for approximately 8 hours at 25 °C, after the **VCC** supply is removed. The purpose of the series resistor is to limit the capacitor charging current due to the large capacitor specifications, and also to let a fast rise time of the voltage value at the **V_BCKP** pin after **VCC** supply has been provided. These capacitors allow the time reference to run during battery disconnection.

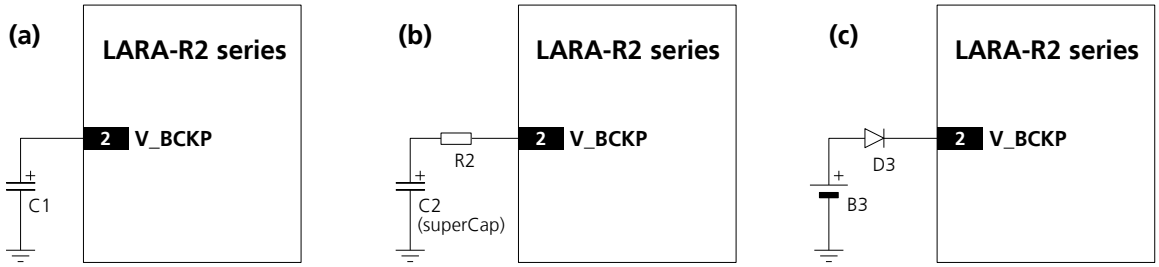


Figure 36: Real time clock supply (V_BCKP) application circuits: (a) using a 100 µF capacitor to let the RTC run for ~1 minute after VCC removal; (b) using a 70 mF capacitor to let RTC run for ~10 hours after VCC removal; (c) using a non-rechargeable battery

Reference	Description	Part Number - Manufacturer
C1	100 µF Tantalum Capacitor	GRM43SR60J107M - Murata
R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
C2	70 mF Capacitor	XH414H-IV01E - Seiko Instruments

Table 28: Example of components for V_BCKP buffering

If longer buffering time is required to allow the RTC time reference to run during a disconnection of the **VCC** supply, then an external battery can be connected to **V_BCKP** pin. The battery should be able to provide a proper nominal voltage and must never exceed the maximum operating voltage for **V_BCKP** (specified in the Input characteristics of Supply/Power pins table in the LARA-R2 series Data Sheet [1]). The connection of the battery to **V_BCKP** should be done with a suitable series resistor for a rechargeable battery, or with an appropriate series diode for a non-rechargeable battery. The purpose of the series resistor is to limit the battery charging current due to the battery specifications, and also to allow a fast rise time of the voltage value at the **V_BCKP** pin after the **VCC** supply has been provided. The purpose of the series diode is to avoid a current flow from the module **V_BCKP** pin to the non-rechargeable battery.

☞ If the RTC timing is not required when the **VCC** supply is removed, it is not needed to connect the **V_BCKP** pin to an external capacitor or battery. In this case the date and time are not updated when **VCC** is disconnected. If **VCC** is always supplied, then the internal regulator is supplied from the main supply and there is no need for an external component on **V_BCKP**.

Combining a LARA-R2 series cellular module with a u-blox GNSS positioning receiver, the positioning receiver **VCC** supply is controlled by the cellular module by means of the "GNSS supply enable" function provided by the **GPIO2** of the cellular module. In this case the **V_BCKP** supply output of the cellular module can be connected to the **V_BCKP** backup supply input pin of the GNSS receiver to provide the supply for the positioning real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS receiver is disabled. This enables the u-blox GNSS receiver to recover from a power breakdown with either a hot start or a warm start (depending on the duration of the positioning **VCC** outage) and to maintain the configuration settings saved in the backup RAM. Refer to section 2.6.4 for more details regarding the application circuit with a u-blox GNSS receiver.

☞ The internal regulator for **V_BCKP** is optimized for low leakage current and very light loads. Do not apply loads which might exceed the limit for maximum available current from **V_BCKP** supply, as this can cause malfunctions in the module. LARA-R2 series Data Sheet [1] describes the detailed electrical characteristics.

V_BCKP supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ ESD sensitivity rating of the **V_BCKP** supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible back-up battery connector is directly connected to **V_BCKP** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

2.2.2.2 Guidelines for V_BCKP layout design

RTC supply (**V_BCKP**) requires careful layout: avoid injecting noise on this voltage domain as it may affect the stability of the 32 kHz oscillator.

2.2.3 Interface supply (V_INT)

2.2.3.1 Guidelines for V_INT circuit design

LARA-R2 series provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on (see sections 1.6.1, 1.6.2 for more details)
- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply voltage translators to connect digital interfaces of the module to a 3.0 V device (see section 2.6.1)
- Pull-up DDC (I^2C) interface signals (see section 2.6.4 for more details)
- Supply a 1.8 V u-blox 6 or subsequent GNSS receiver (see section 2.6.4 for more details)
- Supply an external device, as an external 1.8 V audio codec (see section 2.7.1 for more details)

V_INT supply output pin provides internal short circuit protection to limit start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

☞ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply (see the LARA-R2 series Data Sheet [1]) as this can cause malfunctions in internal circuitry.

☞ Since the **V_INT** supply is generated by an internal switching step-down regulator, the **V_INT** voltage ripple can range as specified in the LARA-R2 series Data Sheet [1]: it is not recommended to supply sensitive analog circuitry without adequate filtering for digital noise.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to the accessible point.

☞ It is recommended to provide direct access to the **V_INT** pin on the application board by means of an accessible test point directly connected to the **V_INT** pin.

2.2.3.2 Guidelines for V_INT layout design

V_INT supply output is generated by an integrated switching step-down converter, used internally to supply the generic digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

LARA-R2 series modules' **PWR_ON** input is equipped with an internal active pull-up resistor to the **VCC** module supply as described in Figure 37: an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 37 and Table 29.

ESD sensitivity rating of the **PWR_ON** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **PWR_ON** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as the pin is equipped with an internal active pull-up resistor to the **V_BCKP** supply, as described in Figure 37.

A compatible push-pull output of an application processor can also be used. In any case, take care to set the proper level in all the possible scenarios to avoid an inappropriate module switch-on.

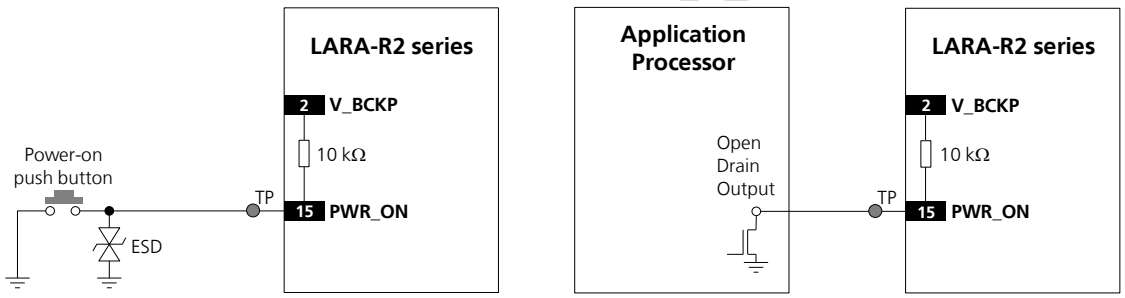


Figure 37: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	CT0402S14AHSG - EPCOS	Varistor array for ESD protection

Table 29: Example of pull-up resistor and ESD protection for the PWR_ON application circuit

It is recommended to provide direct access to the **PWR_ON** pin on the application board by means of accessible testpoint directly connected to the **PWR_ON** pin.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout since it is the sensitive input available to switch on the LARA-R2 series modules. It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious power-on request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

LARA-R2 series **RESET_N** is equipped with an internal pull-up to the **V_BCKP** supply as described in Figure 38. An external pull-up resistor is not required.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to accessible point on the line connected to this pin, as described in Figure 38 and Table 30.

☞ ESD sensitivity rating of the **RESET_N** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **RESET_N** pin. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible point.

An open drain output is suitable to drive the **RESET_N** input from an application processor as it is equipped with an internal pull-up to **V_BCKP** supply, as described in Figure 38.

A compatible push-pull output of an application processor can also be used. In any case, take care to set the proper level in all the possible scenarios to avoid an inappropriate module reset, switch-on or switch-off.

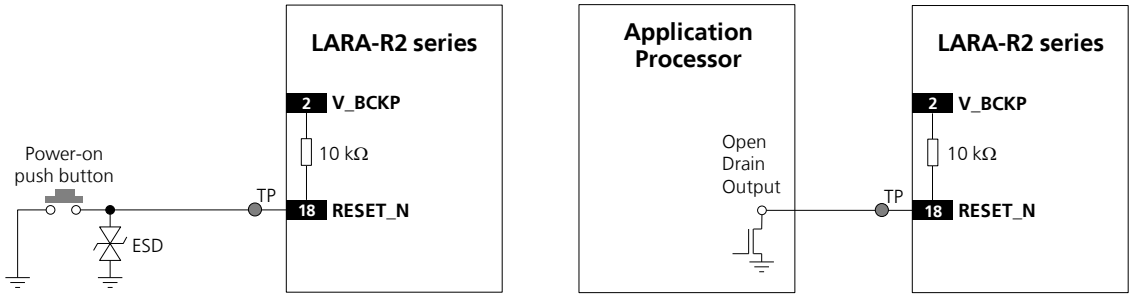


Figure 38: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Remarks
ESD	Varistor for ESD protection	CT0402S14AHSG - EPCOS

Table 30: Example of ESD protection component for the RESET_N application circuit

☞ If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by means of accessible testpoint directly connected to the **RESET_N** pin.

2.3.2.2 Guidelines for RESET_N layout design

The reset circuit (**RESET_N**) requires careful layout due to the pin function: ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious reset request. It is recommended to keep the connection line to **RESET_N** as short as possible.

2.3.3 Module / host configuration selection

2.3.3.1 Guidelines for HOST_SELECT circuit design

☞ Selection of module / host configuration over **HOST_SELECT** is not supported by "02" product versions.

LARA-R2 series modules include one pin (**HOST_SELECT**) to select the module / host application processor configuration: the pin is available to select, enable, connect, disconnect and subsequently re-connect the HSIC (USB High-Speed Inter-Chip) interface.

LARA-R2 series Data Sheet [1] describes the detailed electrical characteristics of the **HOST_SELECT** pin.

☞ Further guidelines for **HOST_SELECT** pin circuit design will be described in detail in a successive release of the System Integration Manual.

☞ Do not apply voltage to **HOST_SELECT** pin before the switch-on of its supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module. If the external signal connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.

☞ ESD sensitivity rating of the **HOST_SELECT** pin is 1 kV (HBM as per JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points

☞ If the **HOST_SELECT** pin is not used, they can be left unconnected on the application board.

2.3.3.2 Guidelines for HOST_SELECT layout design

The pin for the selection of the module / host application processor configuration (**HOST_SELECT**) is generally not critical for layout.

2.4 Antenna interface

LARA-R2 series modules provide two RF interfaces for connecting the external antennas:

- The **ANT1** pin represents the primary RF input/output for LTE/3G/2G RF signals transmission and reception.
- The **ANT2** pin represents the secondary RF input for LTE Rx diversity RF signals reception.

Both the **ANT1** and the **ANT2** pins have a nominal characteristic impedance of 50 Ω and must be connected to the related antenna through a 50 Ω transmission line to allow proper transmission / reception of RF signals.

☞ Two antennas (one connected to **ANT1** pin and one connected to **ANT2** pin) must be used to support the LTE Rx diversity radio technology. This is a required feature for LTE category 1 User Equipments (up to 10.2 Mb/s Down-Link data rate) according to 3GPP specifications.

2.4.1 Antenna RF interface (ANT1 / ANT2)

2.4.1.1 General guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antennas from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the RF compliance of the device integrating LARA-R2 series modules with all the applicable required certification schemes depends on antennas radiating performance.

Cellular antennas are typically available in the types of linear monopole or PCB antennas such as patches or ceramic SMT elements.

- External antennas (e.g. linear monopole)
  - External antennas basically do not imply physical restriction to the design of the PCB where the LARA-R2 series module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ω RF connector provides proper PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
  - If antenna detection functionality is required, select an antenna assembly provided with a proper built-in diagnostic circuit with a resistor connected to ground: see guidelines in section 2.4.2.
- Integrated antennas (e.g. patch-like antennas):
  - Internal integrated antennas imply physical restriction to the design of the PCB:

    Integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced down to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that has to be radiated, given that the orientation of the ground plane relative to the antenna element must be considered.

    The isolation between the primary and the secondary antennas has to be as high as possible and the correlation between the 3D radiation patterns of the two antennas has to be as low as possible. In general, a separation of at least a quarter wavelength between the two antennas is required to achieve a good isolation and low pattern correlation.

    As numerical example, the physical restriction to the PCB design can be considered as following:

    Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm

- Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
- It is recommended to select a pair of custom antennas designed by an antennas' manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry
- Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application

In both of cases, selecting external or internal antennas, these recommendations should be observed:

- Select antennas providing optimal return loss (or V.S.W.R.) figure over all the operating frequencies.
- Select antennas providing optimal efficiency figure over all the operating frequencies.
- Select antennas providing similar efficiency for both the primary (**ANT1**) and the secondary (**ANT2**) antenna.
- Select antennas providing appropriate gain figure (i.e. combined antenna directivity and efficiency figure) so that the electromagnetic field radiation intensity do not exceed the regulatory limits specified in some countries (e.g. by FCC in the United States, as reported in the section 4.2.2).
- Select antennas capable to provide low Envelope Correlation Coefficient between the primary (**ANT1**) and the secondary (**ANT2**) antenna: the 3D antenna radiation patterns should have lobes in different directions.

2.4.1.2 Guidelines for antenna RF interface design

Guidelines for ANT1 / ANT2 pins RF connection design

Proper transition between **ANT1** / **ANT2** pads and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT1** / **ANT2** pads:

- On a multilayer board, the whole layer stack below the RF connection should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT1** / **ANT2** pads, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 39
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT1** / **ANT2** pads if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 39

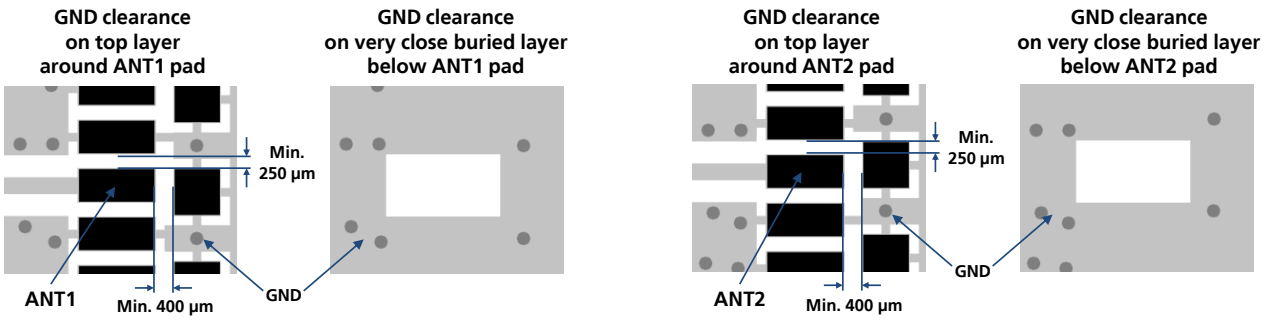


Figure 39: GND keep-out area on top layer around ANT1 / ANT2 pads and on very close buried layer below ANT1 / ANT2 pads

Guidelines for RF transmission line design

Any RF transmission line, such as the ones from the **ANT1** and **ANT2** pads up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 40 and Figure 41 provide two examples of proper 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

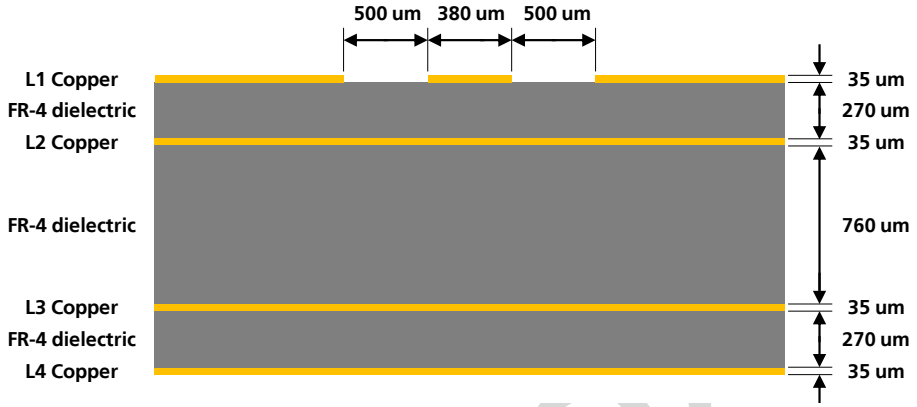


Figure 40: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

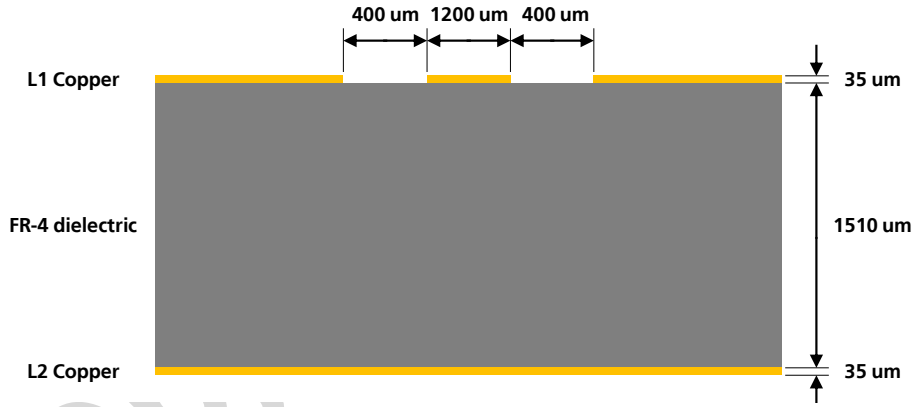


Figure 41: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB layup, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like AppCAD from Agilent (www.agilent.com) or TXLine from Applied Wave Research (www.mwoffice.com), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 40 and Figure 41)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 40, 1510 µm in Figure 41)

- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 40 and Figure 41)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 40, 400 µm in Figure 41)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for the transmission line design:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB.
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission line, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground.
- The transmission line width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND.
- Add GND vias around transmission line, as described in Figure 42.
- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough on the adjacent metal layer, as described in Figure 42.
- Route RF transmission line far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as analog audio lines).
- Avoid stubs on the transmission line.
- Avoid signal routing in parallel to transmission line or crossing the transmission line on buried metal layer.
- Do not route microstrip line below discrete component or other mechanics placed on top layer.

An example of proper RF circuit design is reported in Figure 42. In this case, the **ANT1** and **ANT2** pins are directly connected to SMA connectors by means of proper 50 Ω transmission lines, designed with proper layout.

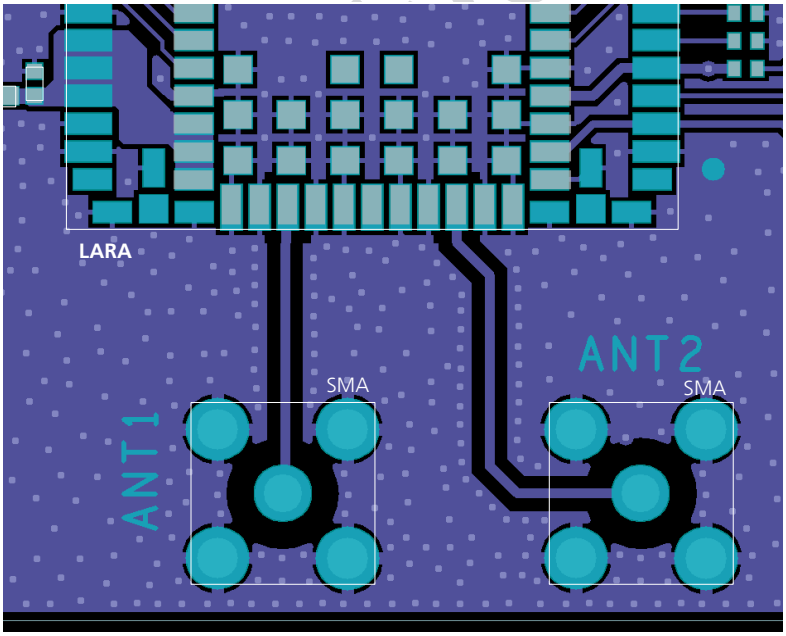


Figure 42: Example of circuit and layout for antenna RF circuits on application board

Guidelines for RF termination design

RF terminations must provide a characteristic impedance of 50 Ω as well as the RF transmission lines up to the RF terminations themselves, to match the characteristic impedance of the **ANT1** / **ANT2** ports of the modules.

However, real antennas do not have perfect 50 Ω load on all the supported frequency bands. Therefore, to reduce as much as possible performance degradation due to antennas mismatch, RF terminations must provide optimal return loss (or V.S.W.R.) figure over all the operating frequencies, as summarized in Table 7 and Table 8.

If external antennas are used, the antenna connectors represent the RF termination on the PCB:

- Use suitable 50 Ω connectors providing proper PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
  - SMA Pin-Through-Hole connectors require GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to annular pads of the four GND posts, as shown in Figure 42.
  - U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads.
- Cut out the GND layer under RF connectors and close to buried vias, to remove stray capacitance and thus keep the RF line 50 Ω, e.g. the active pad of UFL connectors needs to have a GND keep-out (i.e. clearance, a void area) at least on first inner layer to reduce parasitic capacitance to ground.

If integrated antennas are used, the RF terminations are represented by the integrated antennas themselves. The following guidelines should be followed:

- Use antennas designed by an antenna manufacturer, providing the best possible return loss (or V.S.W.R.).
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that has to be radiated. As numerical example,

  Frequency = 750 MHz → Wavelength = 40 cm → Minimum GND plane size = 10 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, antennas may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for the antenna matching relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place antennas within closed metal case.
- Do not place the antennas in close vicinity to end user since the emitted radiation in human tissue is limited by regulatory requirements.
- Place the antennas far from sensitive analog systems or employ countermeasures to reduce EMC issues.
- Take care of interaction between co-located RF systems since the cellular transmitted power may interact or disturb the performance of companion systems.
- Place the two LTE antennas providing low Envelope Correlation Coefficient (ECC) between primary (**ANT1**) and secondary (**ANT2**) antenna: the antenna 3D radiation patterns should have lobes in different directions. The ECC between primary and secondary antenna needs to be enough low to comply with the radiated performance requirements specified by related certification schemes, as indicated in Table 9.
- Place the two LTE antennas providing enough high isolation (see Table 9) between primary (**ANT1**) and secondary (**ANT2**) antenna. The isolation depends on the distance between antennas (separation of at least a quarter wavelength required for good isolation), antenna type (using antennas with different polarization improves isolation), antenna 3D radiation patterns (uncorrelated patterns improve isolation).

Examples of antennas

Table 31 lists some examples of possible internal on-board surface-mount antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	PA.710.A	Warrior	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PA.711.A	Warrior II	GSM / WCDMA / LTE SMD Antenna Pairs with the Taoglas PA.710.A Warrior for LTE MIMO applications 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 40.0 x 6.0 x 5.0 mm
Taoglas	PCS.06.A	Havok	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2500..2690 MHz 42.0 x 10.0 x 3.0 mm
Antenova	SR4L002	Lucida	GSM / WCDMA / LTE SMD Antenna 698..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2490..2690 MHz 35.0 x 8.5 x 3.2 mm

Table 31: Examples of internal surface-mount antennas

Table 32 lists some examples of possible internal off-board PCB-type antennas with cable and connector.

Manufacturer	Part Number	Product Name	Description
Taoglas	FXUB63.07.0150C		GSM / WCDMA / LTE PCB Antenna with cable and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 96.0 x 21.0 mm
Taoglas	FXUB66.07.0150C	Maximus	GSM / WCDMA / LTE PCB Antenna with cable and U.FL 698..960 MHz, 1390..1435 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz, 3400..3600 MHz, 4800..6000 MHz 120.2 x 50.4 mm
Taoglas	FXUB70.A.07.C.001		GSM / WCDMA / LTE PCB MIMO Antenna with cables and U.FL 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2690 MHz 182.2 x 21.2 mm
Ethertronics	5001537	Prestta	GSM / WCDMA / LTE PCB Antenna with cable 704..960 MHz, 1710..2170 MHz, 2300..2400 MHz, 2500..2690 MHz 80.0 x 18.0 mm
EAD	FSQS35241-UF-10	SQ7	GSM / WCDMA / LTE PCB Antenna with cable and U.FL 690..960 MHz, 1710..2170 MHz, 2500..2700 MHz 110.0 x 21.0 mm

Table 32: Examples of internal antennas with cable and connector

Table 33 lists some examples of possible external antennas.

Manufacturer	Part Number	Product Name	Description
Taoglas	GSA.8827.A.101111	Phoenix	GSM / WCDMA / LTE adhesive-mount antenna with cable and SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2490..2690 MHz 105 x 30 x 7.7 mm
Taoglas	TG.30.8112		GSM / WCDMA / LTE swivel dipole antenna with SMA(M) 698..960 MHz, 1575.42 MHz, 1710..2170 MHz, 2400..2700 MHz 148.6 x 49 x 10 mm
Taoglas	MA241.BI.001	Genesis	GSM / WCDMA / LTE MIMO 2in1 adhesive-mount combination antenna waterproof IP67 rated with cable and SMA(M) 698..960 MHz, 1710..2170 MHz, 2400..2700 MHz 205.8 x 58 x 12.4 mm
Laird Tech.	TRA6927M3PW-001		GSM / WCDMA / LTE screw-mount antenna with N-type(F) 698..960 MHz, 1710..2170 MHz, 2300..2700 MHz 83.8 x Ø 36.5 mm
Laird Tech.	CMS69273		GSM / WCDMA / LTE ceiling-mount antenna with cable and N-type(F) 698..960 MHz, 1575.42 MHz, 1710..2700 MHz 86 x Ø 199 mm
Laird Tech.	OC69271-FNM		GSM / WCDMA / LTE pole-mount antenna with N-type(M) 698..960 MHz, 1710..2690 MHz 248 x Ø 24.5 mm
Laird Tech.	CMD69273-30NM		GSM / WCDMA / LTE ceiling-mount MIMO antenna with cables & N-type(M) 698..960 MHz, 1710..2700 MHz 43.5 x Ø 218.7 mm
Pulse Electronics	WA700/2700SMA		GSM / WCDMA / LTE clip-mount MIMO antenna with cables and SMA(M) 698..960 MHz,1710..2700 MHz 149 x 127 x 5.1 mm

Table 33: Examples of external antennas

2.4.2 Antenna detection interface (ANT_DET)

2.4.2.1 Guidelines for ANT_DET circuit design

Figure 43 and Table 34 describe the recommended schematic / components for the antennas detection circuit that must be provided on the application board and for the diagnostic circuit that must be provided on the antennas' assembly to achieve primary and secondary antenna detection functionality.

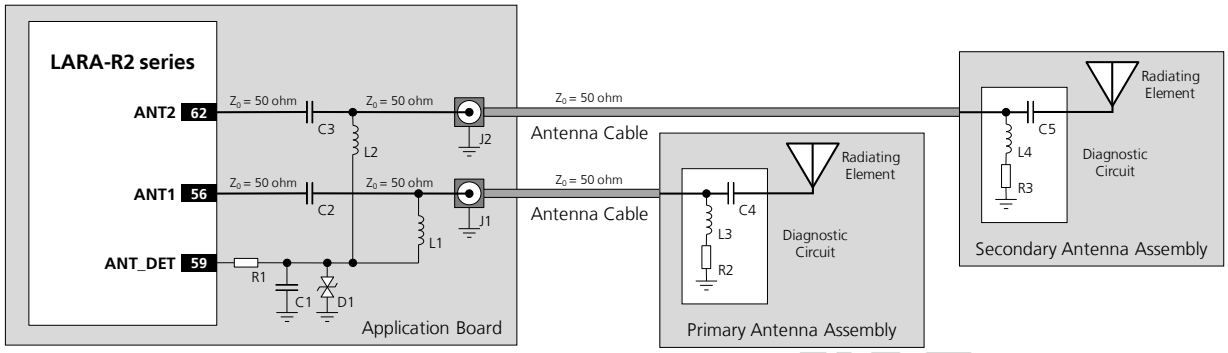


Figure 43: Suggested schematic for antenna detection circuit on application board and diagnostic circuit on antennas assembly

Reference	Description	Part Number - Manufacturer
C1	27 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H270J - Murata
C2, C3	33 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H330J - Murata
D1	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
L1, L2	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R1	10 kΩ Resistor 0402 1% 0.063 W	RK73H1ETTP1002F - KOA Speer
J1, J2	SMA Connector 50 Ω Through Hole Jack	SMA6251A1-3GT50G-50 - Amphenol
C4, C5	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220J - Murata
L3, L4	68 nH Multilayer Inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 - Murata
R2, R3	15 kΩ Resistor for Diagnostic	Various Manufacturers

Table 34: Suggested components for antenna detection circuit on application board and diagnostic circuit on antennas assembly

The antenna detection circuit and diagnostic circuit suggested in Figure 43 and Table 34 are explained here:

- When antenna detection is forced by AT+UANTR command, **ANT_DET** generates a DC current measuring the resistance (R2 // R3) from antenna connectors (J1, J2) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT1** / **ANT2** pins (C2, C3) and at the antenna radiating element (C4, C5) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1, L2) and in series at the diagnostic resistor (L3, L4), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Additional components (R1, C1 and D1 in Figure 43) are needed at the **ANT_DET** pin as ESD protection
- The **ANT1** / **ANT2** pins must be connected to the antenna connector by means of a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 43, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no means to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is properly connected.
- Values close to the measurement range maximum limit (approximately 50 kΩ) or an open-circuit "over range" report (see u-blox AT Commands Manual [2]) means that that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit (1 kΩ) highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an improper connection, damaged antenna or wrong value of antenna load resistor for diagnostic.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

☞ If the primary / secondary antenna detection function is not required by the customer application, the **ANT_DET** pin can be left not connected and the **ANT1** / **ANT2** pins can be directly connected to the related antenna connector by means of a 50 Ω transmission line as described in Figure 42.

2.4.2.2 Guidelines for ANT_DET layout design

The recommended layout for the primary antenna detection circuit to be provided on the application board to achieve the primary antenna detection functionality, implementing the recommended schematic described in Figure 43 and Table 34, is explained here:

- The **ANT1** / **ANT2** pins have to be connected to the antenna connector by means of a 50 Ω transmission line, implementing the design guidelines described in section 2.4.1 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT1** / **ANT2** pins (C2, C3) has to be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin has to be connected to the 50 Ω transmission line by means of a sense line.
- Choke inductors in series at the **ANT_DET** pin (L1, L2) have to be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1 and D1) on the **ANT_DET** line have to be placed as ESD protection.

2.5 SIM interface

2.5.1.1 Guidelines for SIM circuit design

Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC) which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the cellular network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP (Programming supply) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 6 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Solderable UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by ETSI TS 102 671 as:

- Case Pin 8 = UICC Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case Pin 7 = UICC Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case Pin 6 = UICC Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case Pin 5 = UICC Contact C4 = AUX1 (Aux.contact) → It must be left not connected
- Case Pin 1 = UICC Contact C5 = GND (Ground) → It must be connected to **GND**
- Case Pin 2 = UICC Contact C6 = VPP (Progr. supply) → It can be left not connected
- Case Pin 3 = UICC Contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case Pin 4 = UICC Contact C8 = AUX2 (Aux. contact) → It must be left not connected

A solderable SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 6 contacts are required and must be connected to the module SIM card interface as described above.

Solderable SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder has to be connected to the SIM card interface of LARA-R2 series modules as described in Figure 44, where the optional SIM detection feature is not implemented.

Follow these guidelines connecting the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: ESD sensitivity rating of the SIM interface pins is 1 kV (HBM), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each signal of the SIM interface (**SIM_CLK**, **SIM_IO**, **SIM_RST**), to match the SIM interface specifications requirements (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines).

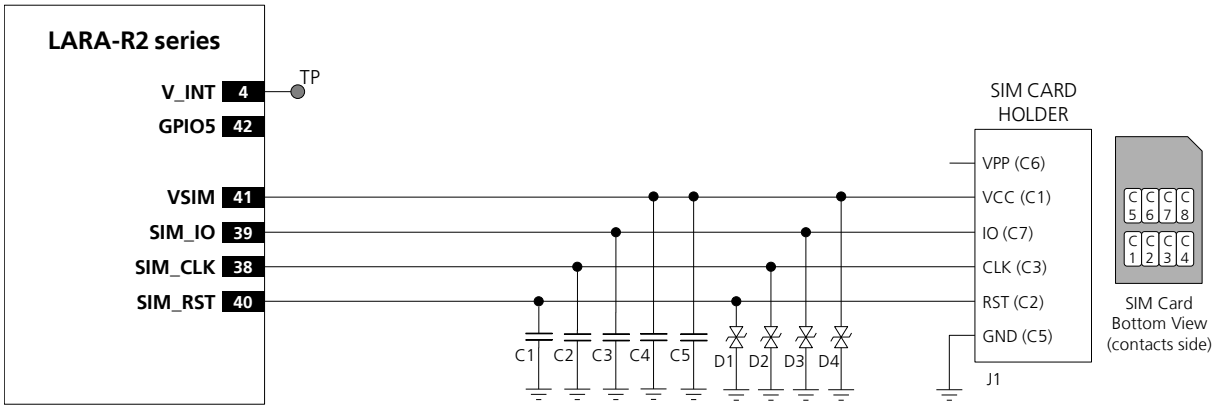


Figure 44: Application circuit for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1, D2, D3, D4	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
J1	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol

Table 35: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

Guidelines for single SIM chip connection

A solderable SIM chip (M2M UICC Form Factor) has to be connected the SIM card interface of LARA-R2 series modules as described in Figure 45.

Follow these guidelines connecting the module to a solderable SIM chip without SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**) close to the related pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Limit capacitance and series resistance on each signal of the SIM interface (**SIM_CLK**, **SIM_IO**, **SIM_RST**), to match the SIM specifications requirements (27.7 ns is the maximum allowed rise time on the **SIM_CLK** line, 1.0 µs is the maximum allowed rise time on the **SIM_IO** and **SIM_RST** lines).

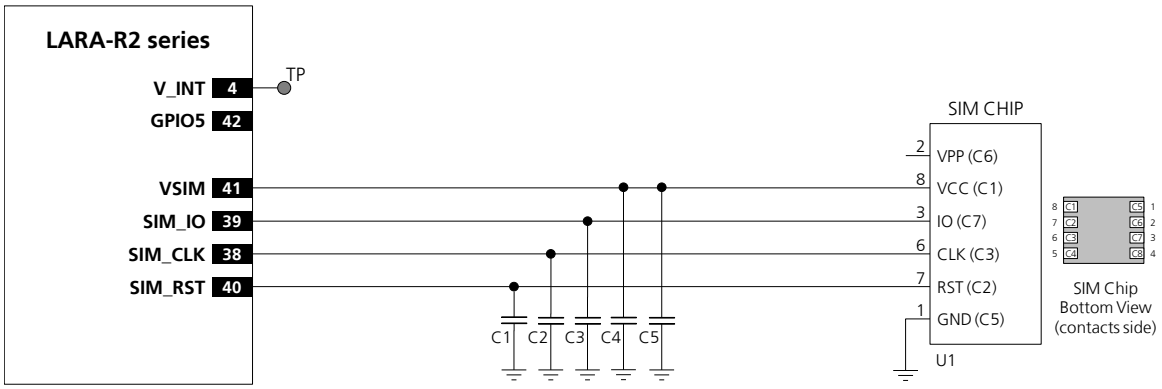


Figure 45: Application circuit for the connection to a single solderable SIM chip, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
U1	SIM chip (M2M UICC Form Factor)	Various Manufacturers

Table 36: Example of components for the connection to a single solderable SIM chip, with SIM detection not implemented

Guidelines for single SIM card connection with detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of LARA-R2 series modules as described in Figure 46, where the optional SIM card detection feature is implemented.

Follow these guidelines connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contacts C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW2 pin as described in Figure 46) to the **GPIO5** input pin of the module.
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (e.g. the SW1 pin as described in Figure 46) to the **V_INT** 1.8 V supply output of the module by means of a strong (e.g. 1 kΩ) pull-up resistor, as the R1 resistor in Figure 46.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector: ESD sensitivity rating of SIM interface pins is 1 kV (HBM according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible.
- Limit capacitance and series resistance on each SIM signal to match the SIM specifications requirements (27.7 ns = max allowed rise time on **SIM_CLK**, 1.0 µs = max allowed rise time on **SIM_IO** and **SIM_RST**).

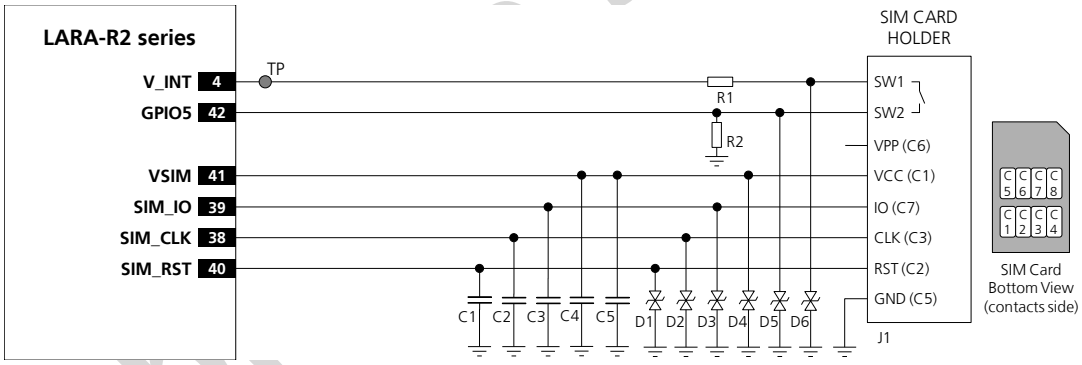


Figure 46: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	47 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H470JA01 - Murata
C5	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D6	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	1 kΩ Resistor 0402 5% 0.1 W	RC0402JR-071KL - Yageo Phycomp
R2	470 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07470KL- Yageo Phycomp
J1	SIM Card Holder 6 + 2 positions, with card presence switch	Various Manufacturers, CCM03-3013LFT R102 - C&K Components

Table 37: Example of components for the connection to a single removable SIM card, with SIM detection implemented

Guidelines for dual SIM card / chip connection

Two SIM card / chip can be connected to the SIM interface of LARA-R2 series modules as described in Figure 47.

LARA-R2 series modules do not support the usage of two SIM at the same time, but two SIM can be populated on the application board, providing a proper switch to connect only the first or only the second SIM at a time to the SIM interface of the modules, as described in Figure 47.

LARA-R2 series modules support SIM hot insertion / removal on the **GPIO5** pin, to enable / disable SIM interface upon detection of external SIM card physical insertion / removal: if the feature is enabled using the specific AT commands (see sections 1.8.2 and 1.12, and u-blox AT Commands Manual [2], +UGPIOC, +UDCONF=50 commands), the switch from first SIM to the second SIM can be properly done when a Low logic level is present on the **GPIO5** pin ("SIM not inserted" = SIM interface not enabled), without the necessity of a module re-boot, so that the SIM interface will be re-enabled by the module to use the second SIM when a high logic level is re-applied on the **GPIO5** pin.

In the application circuit example represented in Figure 47, the application processor will drive the SIM switch using its own GPIO to properly select the SIM that is used by the module. Another GPIO may be used to handle the SIM hot insertion / removal function of LARA-R2 series modules, which can also be handled by other external circuits or by the cellular module GPIO according to the application requirements.

The dual SIM connection circuit described in Figure 47 can be implemented for SIM chips as well, providing proper connection between SIM switch and SIM chip as described in Figure 45.

If it is required to switch between more than 2 SIM, a circuit similar to the one described in Figure 47 can be implemented: in case of 4 SIM circuit, using proper 4-throw switch instead of the suggested 2-throw switches.

Follow these guidelines connecting the module to two SIM connectors:

- Use a proper low on resistance (i.e. few ohms) and low on capacitance (i.e. few pF) 2-throw analog switch (e.g. Fairchild FSA2567) as SIM switch to ensure high-speed data transfer according to SIM requirements.
- Connect the contacts C1 (VCC) of the two UICC / SIM to the **VSIM** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C7 (I/O) of the two UICC / SIM to the **SIM_IO** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C3 (CLK) of the two UICC / SIM to the **SIM_CLK** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C2 (RST) of the two UICC / SIM to the **SIM_RST** pin of the module by means of a proper 2-throw analog switch (e.g. Fairchild FSA2567).
- Connect the contact C5 (GND) of the two UICC / SIM to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the two SIM connectors, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GRM1555C1H470J) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the two SIM connectors, to prevent RF coupling especially in case the RF antenna is placed closer than 10 - 30 cm from the SIM card holders.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the two SIM connectors, according to the EMC/ESD requirements of the custom application.
- Limit capacitance and series resistance on each SIM signal to match the SIM specifications requirements (27.7 ns = max allowed rise time on **SIM_CLK**, 1.0 µs = max allowed rise time on **SIM_IO** and **SIM_RST**).

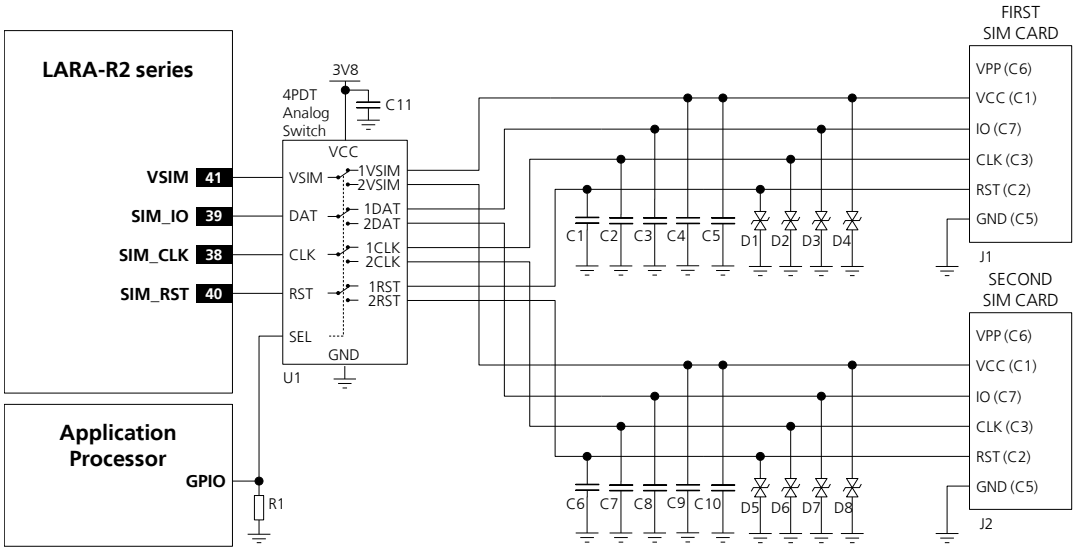


Figure 47: Application circuit for the connection to two removable SIM cards, with SIM detection not implemented

Reference	Description	Part Number - Manufacturer
C1 – C4, C6 – C9	33 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H330JZ01 - Murata
C5, C10, C11	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata
D1 – D8	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics
R1	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL- Yageo Phycomp
J1, J2	SIM Card Holder 6 positions, without card presence switch	Various Manufacturers, C707 10M006 136 2 - Amphenol
U1	4PDT Analog Switch, with Low On-Capacitance and Low On-Resistance	FSA2567 - Fairchild Semiconductor

Table 38: Example of components for the connection to two removable SIM cards, with SIM detection not implemented

2.5.1.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the LARA-R2 series modules or in close proximity to the RF antenna: these two cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface: keep the traces short and avoid coupling with RF line or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of cellular receiver channels whose carrier frequency is coincidental with harmonic frequencies: placing the RF bypass capacitors suggested in Figure 46 near the SIM connector will mitigate the problem.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges: add adequate ESD protection as suggested in Figure 46 to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications: the connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Data communication interfaces

2.6.1 UART interface

2.6.1.1 Guidelines for UART circuit design

Providing the full RS-232 functionality (using the complete V.24 link)

If RS-232 compatible signal levels are needed, two different external voltage translators can be used to provide full RS-232 (9 lines) functionality: e.g. using the Texas Instruments SN74AVC8T245PW for the translation from 1.8 V to 3.3 V, and the Maxim MAX3237E for the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V Application Processor (DTE) is used and complete RS-232 functionality is required, then the complete 1.8 V UART interface of the module (DCE) should be connected to a 1.8 V DTE, as described in Figure 48.

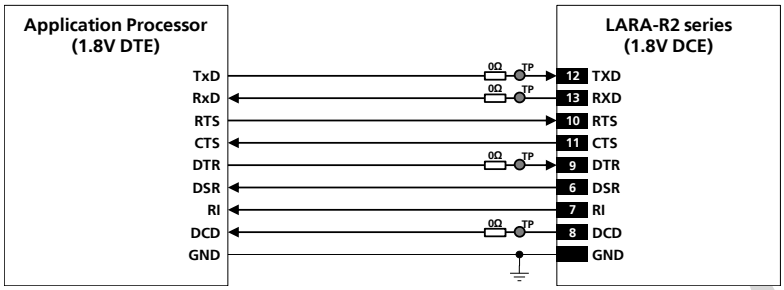


Figure 48: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 49.

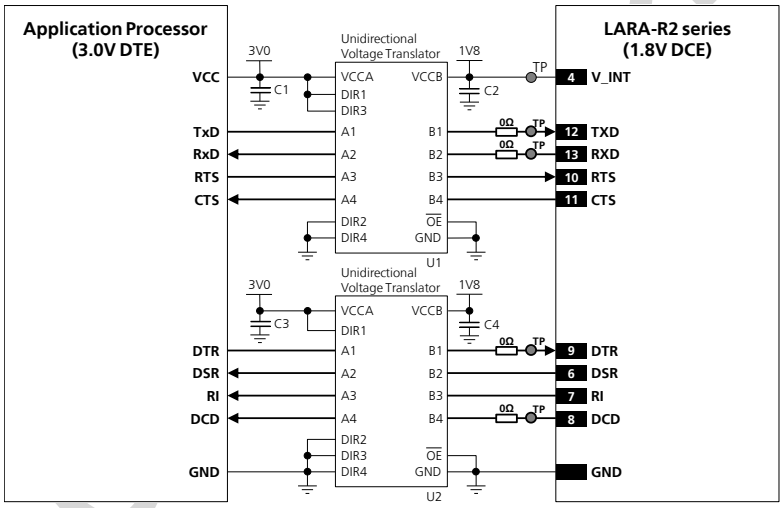


Figure 49: UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1, U2	Unidirectional Voltage Translator	SN74AVC4T774[16] - Texas Instruments

Table 39: Component for UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

[16] Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing the TXD, RXD, RTS, CTS and DTR lines only (not using the complete V.24 link)

If the functionality of the **DSR**, **DCD** and **RI** lines is not required, or the lines are not available:

- Leave **DSR**, **DCD** and **RI** lines of the module floating, with a test-point on **DCD**

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

Figure 50 describes the circuit that should be implemented as if a 1.8 V Application Processor (DTE) is used, given that the DTE will behave properly regardless **DSR** input setting.

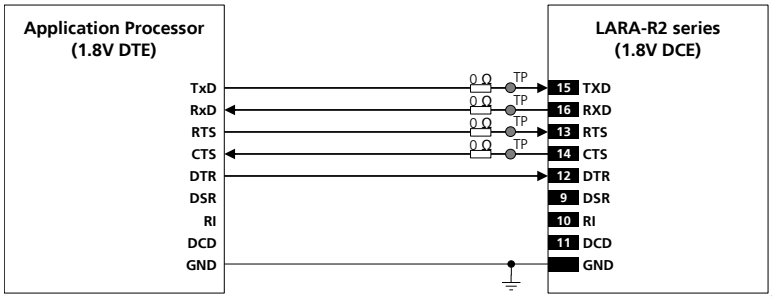


Figure 50: UART interface application circuit with partial V.24 link (6-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 51, given that the DTE will behave properly regardless **DSR** input setting.

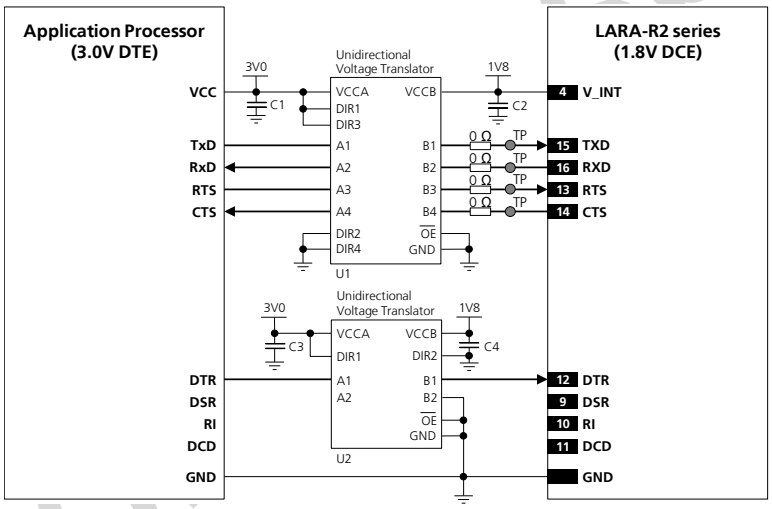


Figure 51: UART interface application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2, C3, C4	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774[17] - Texas Instruments
U2	Unidirectional Voltage Translator	SN74AVC2T245[17] - Texas Instruments

Table 40: Component for UART application circuit with partial V.24 link (6-wire) in DTE/DCE serial communication (3.0 V DTE)

[17] Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing the TXD, RXD, RTS and CTS lines only (not using the complete V.24 link)

- Connect the module **DTR** input to GND using a 0 Ω series resistor, since it may be useful to set **DTR** active if not specifically handled (see u-blox AT Commands Manual [2], &D, S0, +CSGT, +CNMI AT commands)
- Leave **DSR**, **DCD** and **RI** lines of the module floating, with a test-point on **DCD**

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor is used, the circuit should be implemented as described in Figure 52.

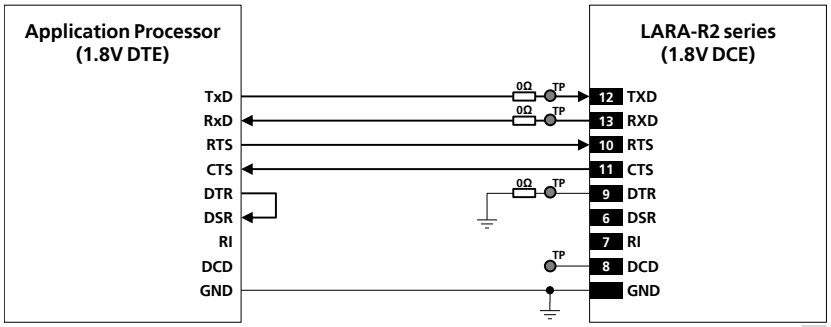


Figure 52: UART interface application circuit with partial V.24 link (5-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 53.

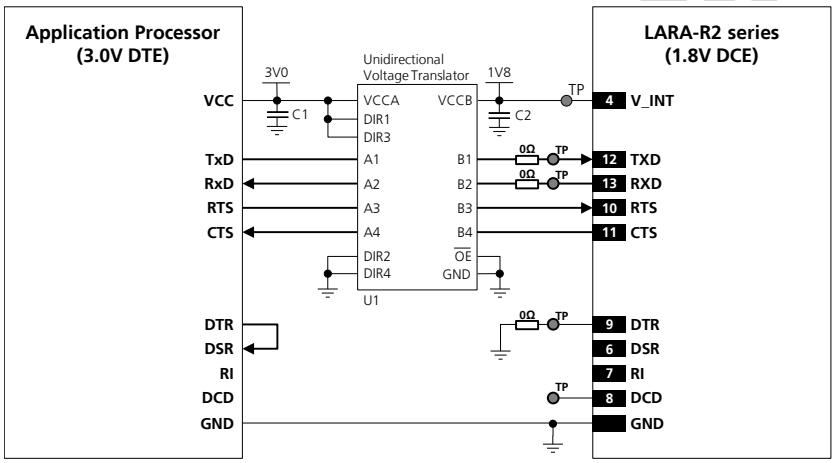


Figure 53: UART interface application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC4T774[18] - Texas Instruments

Table 41: Component for UART application circuit with partial V.24 link (5-wire) in DTE/DCE serial communication (3.0 V DTE)

[18] Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing the TXD and RXD lines only (not using the complete V24 link)

If the functionality of the **CTS**, **RTS**, **DSR**, **DCD**, **RI** and **DTR** lines is not required in the application, or the lines are not available:

- Connect the module **RTS** input line to GND or to the **CTS** output line of the module: since the module requires **RTS** active (low electrical level) if HW flow-control is enabled (AT&K3, which is the default setting).
- Connect the module **DTR** input to GND using a 0 Ω series resistor, since it may be useful to set **DTR** active if not specifically handled (see u-blox AT Commands Manual [2], &D, S0, +CSGT, +CNMI AT commands)
- Leave **DSR**, **DCD** and **RI** lines of the module floating, with a test-point on **DCD**

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V Application Processor (DTE) is used, the circuit that should be implemented as described in Figure 54:

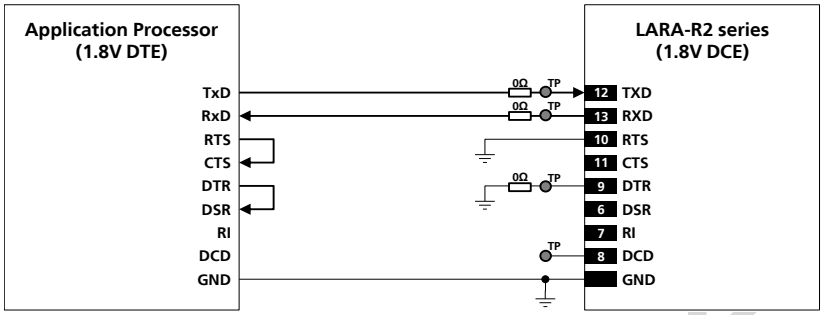


Figure 54: UART interface application circuit with partial V.24 link (3-wire) in the DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V Application Processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by means of appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 55.

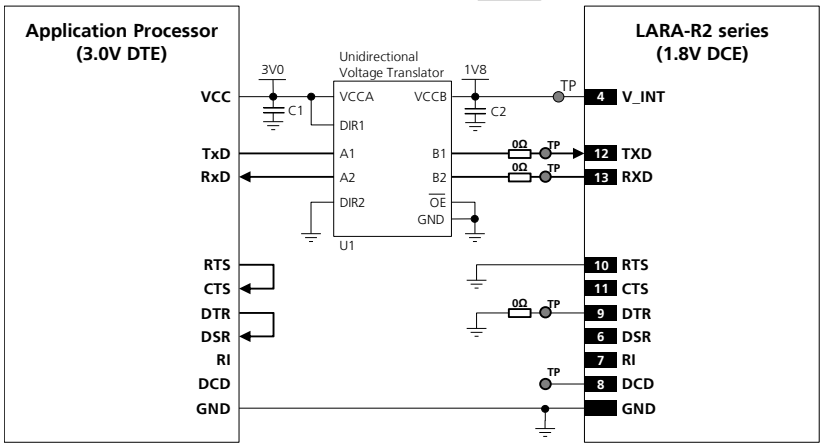


Figure 55: UART interface application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part Number - Manufacturer
C1, C2	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
U1	Unidirectional Voltage Translator	SN74AVC2T245[19] - Texas Instruments

Table 42: Component for UART application circuit with partial V.24 link (3-wire) in DTE/DCE serial communication (3.0 V DTE)

[19] Voltage translator providing partial power down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply

Additional considerations

If a 3.0 V Application Processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the apposite 1.8 V input of the module (DCE) can be implemented, as an alternative low-cost solution, by means of an appropriate voltage divider. Consider the value of the pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values and mind that any DTE signal connected to the module has to be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the apposite 3.0 V input of the Application Processor (DTE) can be implemented by means of an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

☞ If power saving is enabled the application circuit with the **TXD** and **RXD** lines only is not recommended. During command mode the DTE must send to the module a wake-up character or a dummy "AT" before each command line (see section 1.9.1.4 for the complete description), but during data mode the wake-up character or the dummy "AT" would affect the data communication.

☞ Do not apply voltage to any UART interface pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.

☞ ESD sensitivity rating of UART interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

☞ If the UART interface pins are not used, they can be left unconnected on the application board, but it is recommended providing accessible test points directly connected to the **TXD**, **RXD**, **DTR** and **DCD** pins for diagnostic purpose, in particular providing a 0 Ω series jumper on each line to detach each UART pin of the module from the DTE application processor.

2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 USB interface

2.6.2.1 Guidelines for USB circuit design

The **USB_D+** and **USB_D-** lines carry the USB serial data and signaling. The lines are used in single ended mode for full speed signaling handshake, as well as in differential mode for high speed signaling and data transfer.

USB pull-up or pull-down resistors and external series resistors on **USB_D+** and **USB_D-** lines as required by the USB 2.0 specification [9] are part of the module USB pins driver and do not need to be externally provided.

The USB interface of the module is enabled only if a valid voltage is detected by the **VUSB_DET** input (see the LARA-R2 series Data Sheet [1]). Neither the USB interface, nor the whole module is supplied by the **VUSB_DET** input: the **VUSB_DET** senses the USB supply voltage and absorbs few microamperes.

Routing the USB pins to a connector, they will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device with very low capacitance should be provided close to accessible point on the line connected to this pin, as described in Figure 56 and Table 43.

☞ The USB interface pins ESD sensitivity rating is 1 kV (Human Body Model according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. Tyco Electronics PESD0402-140 ESD protection device) on the lines connected to these pins, close to accessible points.

The USB pins of the modules can be directly connected to the USB host application processor without additional ESD protections if they are not externally accessible or according to EMC/ESD requirements.

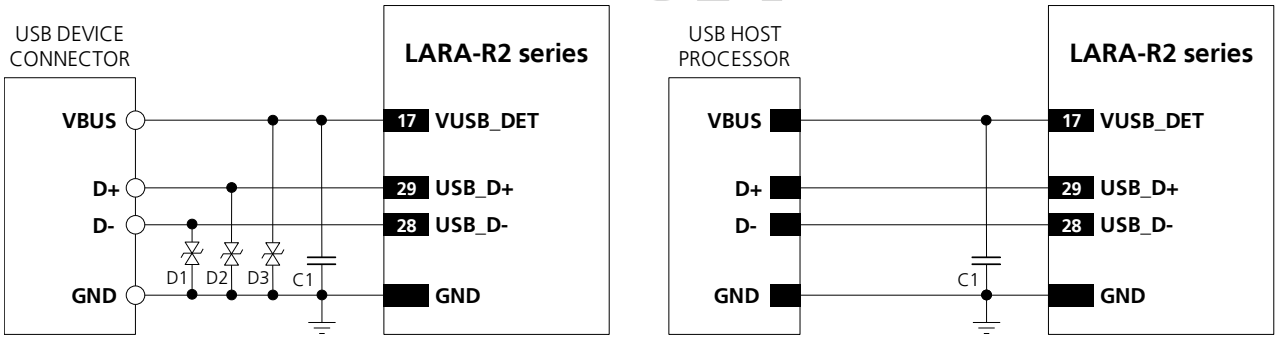


Figure 56: USB Interface application circuits

Reference	Description	Part Number - Manufacturer
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R61A104KA01 - Murata
D1, D2, D3	Very Low Capacitance ESD Protection	PESD0402-140 - Tyco Electronics

Table 43: Component for USB application circuits

☞ If the USB interface pins are not used, they can be left unconnected on the application board, but it is recommended providing accessible test points directly connected to **VUSB_DET**, **USB_D+**, **USB_D-** pins.

2.6.2.2 Guidelines for USB layout design

The **USB_D+** / **USB_D-** lines require accurate layout design to achieve reliable signaling at the high speed data rate (up to 480 Mb/s) supported by the USB serial interface.

The characteristic impedance of the **USB_D+** / **USB_D-** lines is specified by the Universal Serial Bus Revision 2.0 specification [9]. The most important parameter is the differential characteristic impedance applicable for the odd-mode electromagnetic field, which should be as close as possible to 90 Ω differential. Signal integrity may be degraded if PCB layout is not optimal, especially when the USB signaling lines are very long.

Use the following general routing guidelines to minimize signal quality problems:

- Route **USB_D+** / **USB_D-** lines as a differential pair.
- Route **USB_D+** / **USB_D-** lines as short as possible.
- Ensure the differential characteristic impedance (Z_0) is as close as possible to 90 Ω.
- Ensure the common mode characteristic impedance (Z_{CM}) is as close as possible to 30 Ω.
- Consider design rules for **USB_D+** / **USB_D-** similar to RF transmission lines, being them coupled differential micro-strip or buried stripline: avoid any stubs, abrupt change of layout, and route on clear PCB area.
- Avoid coupling with any RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Figure 57 and Figure 58 provide two examples of coplanar waveguide designs with differential characteristic impedance close to 90 Ω and common mode characteristic impedance close to 30 Ω. The first transmission line can be implemented in case of 4-layer PCB stack-up herein described, the second transmission line can be implemented in case of 2-layer PCB stack-up herein described.

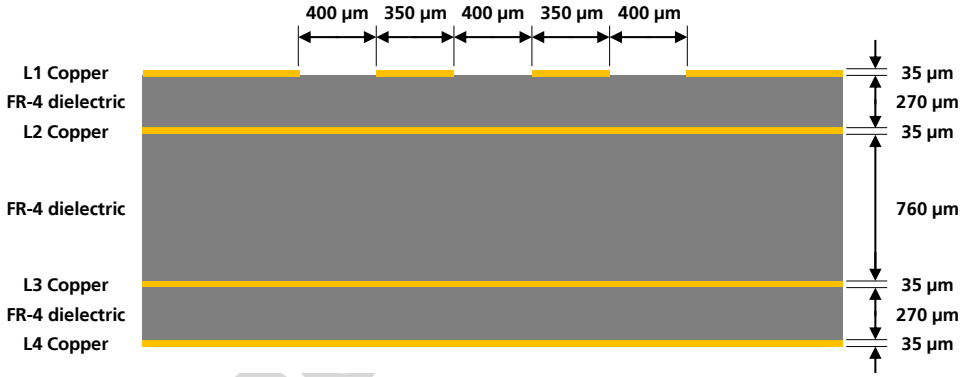


Figure 57: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 4-layer board layup

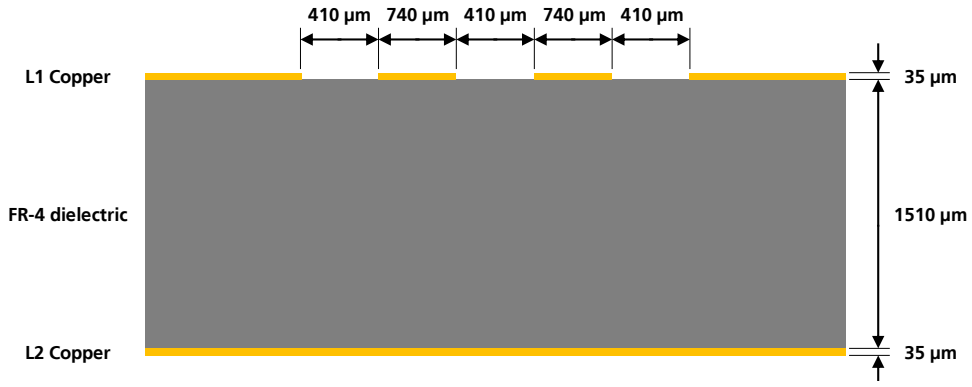


Figure 58: Example of USB line design, with Z_0 close to 90 Ω and Z_{CM} close to 30 Ω, for the described 2-layer board layup

2.6.3 HSIC interface

2.6.3.1 Guidelines for HSIC circuit design

☞ The HSIC interface is not supported by "02" modules product versions except for diagnostic purpose.

LARA-R2 series modules include a USB High-Speed Inter-Chip compliant interface with maximum 480 Mb/s data rate according to the High-Speed Inter-Chip USB Electrical Specification Version 1.0 [10] and USB Specification Revision 2.0 [9]. The module itself acts as a device and can be connected to any compatible host.

The HSIC interface consists of a bi-directional DDR data line (**HSIC_DATA**) for transmitting and receiving data synchronously with the bi-directional strobe line (**HSIC_STRB**), intended to be directly connected to the Data and Strobe pins of the compatible USB High-Speed Inter-Chip host mounted on the same PCB of the LARA-R2 series module, without using connectors / cables, as described in Figure 59.

The modules include also the **HOST_SELECT** pin to select the module / host application processor configuration: the pin is available to select, enable, connect, disconnect and subsequently re-connect the HSIC interface.

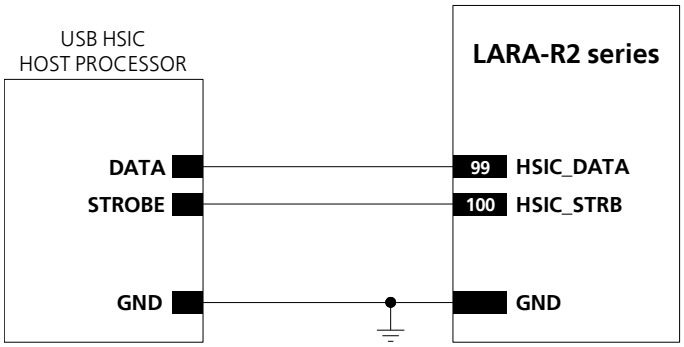


Figure 59: HSIC interface application circuit

☞ Further guidelines for HSIC interface circuit design will be described in detail in a successive release of the System Integration Manual.

☞ ESD sensitivity rating of HSIC interface pins is 1 kV (HBM as per JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points

☞ If the HSIC interface pins are not used, they can be left unconnected on the application board, but it is recommended providing accessible test points directly connected to **HSIC_DATA** and **HSIC_STRB** pins.

2.6.3.2 Guidelines for HSIC layout design

HSIC lines require accurate layout design to achieve reliable signaling at high speed data rate (up to 480 Mb/s), as supported by the HSIC serial interface: signal integrity may be degraded if PCB layout is not optimal, especially when the HSIC lines are very long.

The characteristic impedance of the **HSIC_DATA** and **HSIC_STRB** lines has to be as close as possible to 50 Ω, as specified by the High-Speed Inter-Chip USB Electrical Specification Version 1.0 [10].

Use the following general routing guidelines to minimize signal quality problems:

- Route **HSIC_DATA** and **HSIC_STRB** lines as short as possible.
- HSIC interface is only recommended for intra-board interconnect. The connection should be point-to-point. Connectors and cables are not recommended.
- **HSIC_DATA** and **HSIC_STRB** lines must be matched in length to within 10 mils.
- Ensure the characteristic impedance of **HSIC_DATA** and **HSIC_STRB** lines is as close as possible to 50 Ω.
- **HSIC_DATA** and **HSIC_STRB** signals are not differential signals and should not be routed as such.
- Consider design rules for **HSIC_DATA** and **HSIC_STRB** lines similar to RF transmission lines, routing them as micro-strips (conducting strips separated from ground plane by dielectric material) or striplines (flat strips of metal sandwiched between two parallel ground planes within a dielectric material).
- Avoid any stubs, abrupt change of layout, and route on clear PCB area.
- Avoid coupling with any RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Figure 40 and Figure 41 provide two examples of proper 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

If the two examples do not match the application PCB layup, the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like AppCAD from Agilent (www.agilent.com) or TXLine from Applied Wave Research (www.mwoffice.com), taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the width of the transmission line must be chosen depending on:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 40 and Figure 41)
- the thickness of the dielectric material between the top layer (where the transmission line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 40, 1510 µm in Figure 41)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 40 and Figure 41)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 40, 400 µm in Figure 41)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the track width of the micro strip, use the "Coplanar Waveguide" model for the 50 Ω calculation.

2.6.4 DDC (I²C) interface

2.6.4.1 Guidelines for DDC (I²C) circuit design

General considerations

☞ Communication with u-blox GNSS receivers over DDC (I²C) is not supported by "02" product versions.

The DDC I²C-bus master interface can be used to communicate with u-blox GNSS receivers and other external I²C-bus slaves as an audio codec. Beside the general considerations reported below, see:

- the following parts of this section for specific guidelines for the connection to u-blox GNSS receivers.
- the section 2.7.1 for an application circuit example with an external audio codec I²C-bus slave.

To be compliant to the I²C-bus specifications, the module bus interface pins are open drain output and pull up resistors must be mounted externally. Resistor values must conform to I²C bus specifications [11]: for example, 4.7 kΩ resistors can be commonly used. Pull-ups must be connected to a supply voltage of 1.8 V (typical), since this is the voltage domain of the DDC pins which are not tolerant to higher voltage values (e.g. 3.0 V).

☞ Connect the DDC (I²C) pull-ups to the **V_INT** 1.8 V supply source, or another 1.8 V supply source enabled after **V_INT** (e.g., as the GNSS 1.8 V supply present in Figure 60 application circuit), as any external signal connected to the DDC (I²C) interface must not be set high before the switch-on of the **V_INT** supply of the DDC (I²C) pins, to avoid latch-up of circuits and let a proper boot of the module.

The signal shape is defined by the values of the pull-up resistors and the bus capacitance. Long wires on the bus increase the capacitance. If the bus capacitance is increased, use pull-up resistors with nominal resistance value lower than 4.7 kΩ, to match the I²C bus specifications [11] regarding rise and fall times of the signals.

☞ Capacitance and series resistance must be limited on the bus to match the I²C specifications (1.0 µs is the maximum allowed rise time on the **SCL** and **SDA** lines): route connections as short as possible.

☞ ESD sensitivity rating of the DDC (I²C) pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

☞ If the pins are not used as DDC bus interface, they can be left unconnected.

Connection with u-blox 1.8 V GNSS receivers

Figure 60 shows an application circuit for connecting the cellular module to a u-blox 1.8 V GNSS receiver:

- The **SDA** and **SCL** pins of the cellular module are directly connected to the related pins of the u-blox 1.8 V GNSS receiver, with appropriate pull-up resistors connected to the 1.8 V GNSS supply enabled after the **V_INT** supply of the I^2C pins of the cellular module.
- The **GPIO2** pin is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 1.8 V GNSS receiver providing the "GNSS supply enable" function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the cellular module is switched off or in the reset state.
- The **GPIO3** and **GPIO4** pins are directly connected respectively to **TXD1** and **EXTINT0** pins of the u-blox 1.8 V GNSS receiver providing "GNSS Tx data ready" and "GNSS RTC sharing" functions.
- The **V_BCKP** supply output of the cellular module is connected to the **V_BCKP** backup supply input pin of the GNSS receiver to provide the supply for the GNSS real time clock and backup RAM when the **VCC** supply of the cellular module is within its operating range and the **VCC** supply of the GNSS receiver is disabled. This enables the u-blox GNSS receiver to recover from a power breakdown with either a hot start or a warm start (depending on the actual duration of the GNSS **VCC** outage) and to maintain the configuration settings saved in the backup RAM.

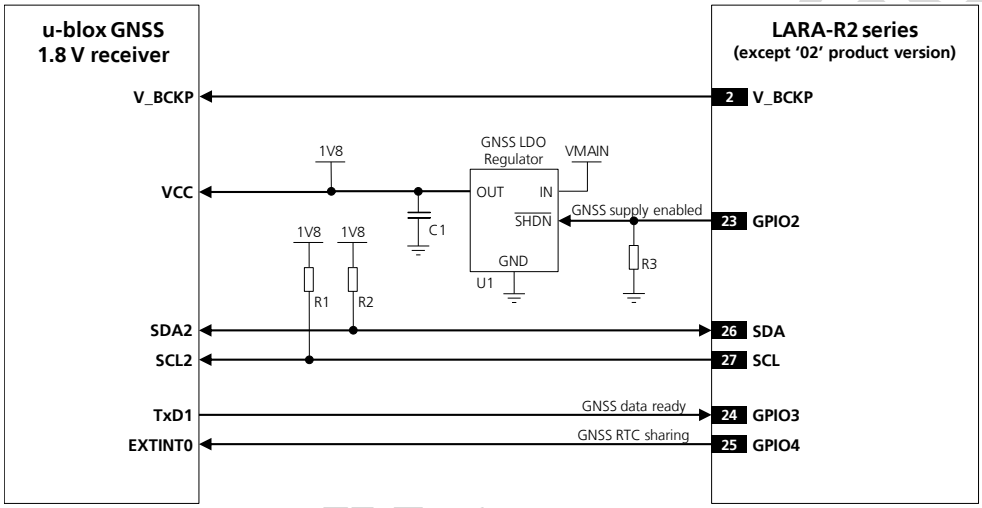


Figure 60: Application circuit for connecting LARA-R2 series modules to u-blox 1.8 V GNSS receivers

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
U1	Voltage Regulator for GNSS receiver	See GNSS receiver Hardware Integration Manual

Table 44: Components for connecting LARA-R2 series modules to u-blox 1.8 V GNSS receivers

Figure 61 illustrates an alternative solution as supply for u-blox 1.8 V GNSS receivers: the **V_INT** 1.8 V regulated supply output of the cellular module can be used to supply a u-blox 1.8 V GNSS receiver of the u-blox 6 generation (or any newer u-blox GNSS receiver generation) instead of using an external voltage regulator as shown in the previous Figure 60. The **V_INT** supply is able to support the maximum current consumption of these positioning receivers.

The internal switching step-down regulator that generates the **V_INT** supply is set to 1.8 V (typical) when the cellular module is switched on and it is disabled when the module is switched off.

The supply of the u-blox 1.8 V GNSS receiver can be switched off using an external p-channel MOSFET controlled by the **GPIO2** pin by means of a proper inverting transistor as shown in Figure 61, implementing the "GNSS supply enable" function. If this feature is not required, the **V_INT** supply output can be directly connected to the u-blox 1.8 V GNSS receiver, so that it will be switched on when **V_INT** output is enabled.

According to the **V_INT** supply output voltage ripple characteristic specified in LARA-R2 series Data Sheet [1]:

- Additional filtering may be needed to properly supply an external LNA, depending on the characteristics of the used LNA, adding a series ferrite bead and a bypass capacitor (e.g. the Murata BLM15HD182SN1 ferrite bead and the Murata GRM1555C1H220J 22 pF capacitor) at the input of the external LNA supply line.

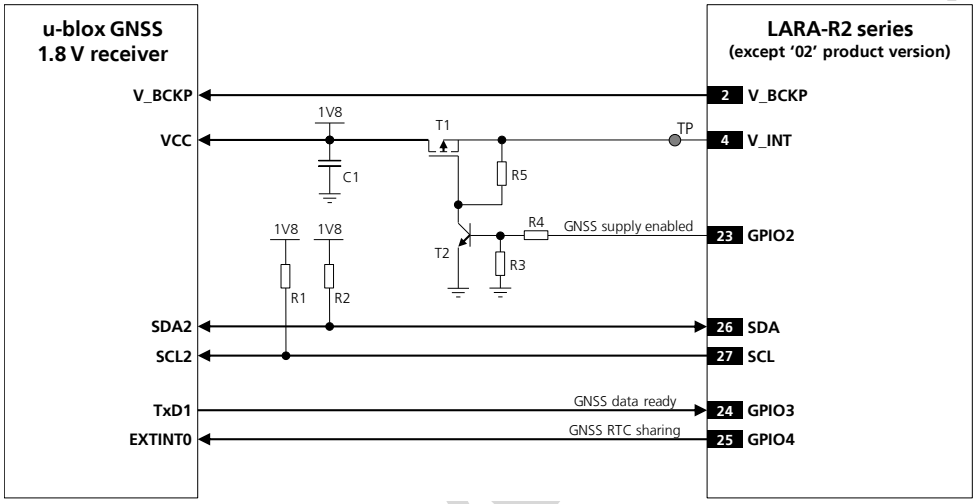


Figure 61: Application circuit for connecting LARA-R2 series modules to u-blox 1.8 V GNSS receivers using V_INT as supply

Reference	Description	Part Number - Manufacturer
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
R4	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R5	100 kΩ Resistor 0402 5% 0.1 W	RC0402JR-07100KL - Yageo Phycomp
T1	P-Channel MOSFET Low On-Resistance	IRLML6401 - International Rectifier or NTZS3151P - ON Semi
T2	NPN BJT Transistor	BC847 - Infineon
C1	100 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C104KA01 - Murata

Table 45: Components for connecting LARA-R2 series modules to u-blox 1.8 V GNSS receivers using V_INT as supply

For additional guidelines regarding the design of applications with u-blox 1.8 V GNSS receivers see the GNSS Implementation Application Note [22] and to the Hardware Integration Manual of the u-blox GNSS receivers.

Connection with u-blox 3.0 V GNSS receivers

Figure 62 shows an application circuit for connecting the cellular module to a u-blox 3.0 V GNSS receiver:

- As the **SDA** and **SCL** pins of the cellular module are not tolerant up to 3.0 V, the connection to the related I^2C pins of the u-blox 3.0 V GNSS receiver must be provided using a proper I^2C-bus Bidirectional Voltage Translator (e.g. TI TCA9406, which additionally provides the partial power down feature so that the GNSS 3.0 V supply can be ramped up before the **V_INT** 1.8 V cellular supply), with proper pull-up resistors.
- The **GPIO2** is connected to the active-high enable pin of the voltage regulator that supplies the u-blox 3.0 V GNSS receiver providing the "GNSS supply enable" function. A pull-down resistor is provided to avoid a switch on of the positioning receiver when the cellular module is switched off or in the reset state.
- As the **GPIO3** and **GPIO4** pins of the cellular module are not tolerant up to 3.0 V, the connection to the related pins of the u-blox 3.0 V GNSS receiver must be provided using a proper Unidirectional General Purpose Voltage Translator (e.g. TI SN74AVC2T245, which additionally provides the partial power down feature so that the 3.0 V GNSS supply can be also ramped up before the **V_INT** 1.8 V cellular supply).
- The **V_BCKP** supply output of the cellular module can be directly connected to the **V_BCKP** backup supply input pin of the GNSS receiver as in the application circuit for a u-blox 1.8 V GNSS receiver.

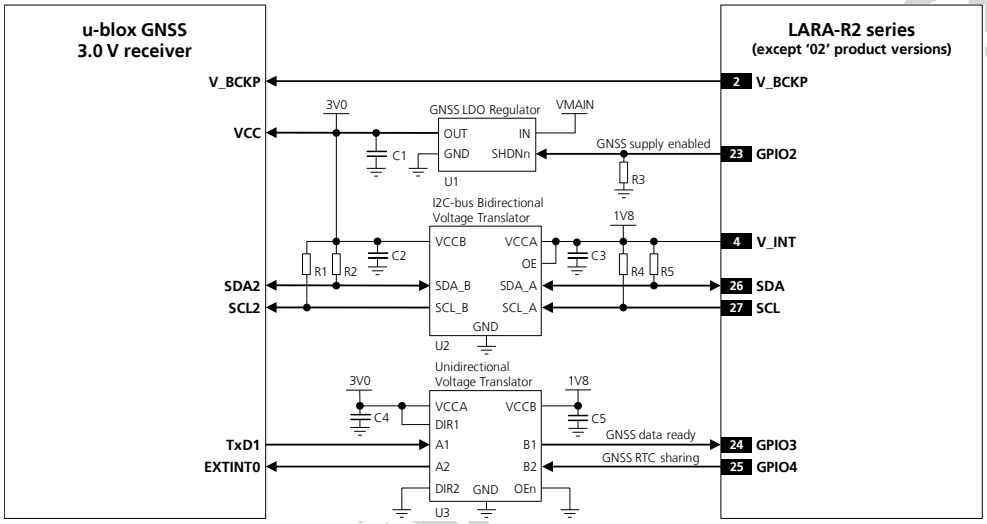


Figure 62: Application circuit for connecting LARA-R2 series modules to u-blox 3.0 V GNSS receivers

Reference	Description	Part Number - Manufacturer
R1, R2, R4, R5	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	47 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0747KL - Yageo Phycomp
C2, C3, C4, C5	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 - Murata
U1, C1	Voltage Regulator for GNSS receiver and related output bypass capacitor	See GNSS receiver Hardware Integration Manual
U2	I2C-bus Bidirectional Voltage Translator	TCA9406DCUR - Texas Instruments
U3	Generic Unidirectional Voltage Translator	SN74AVC2T245 - Texas Instruments

Table 46: Components for connecting LARA-R2 series modules to u-blox 3.0 V GNSS receivers

For additional guidelines regarding the design of applications with u-blox 3.0 V GNSS receivers see the GNSS Implementation Application Note [22] and to the Hardware Integration Manual of the u-blox GNSS receivers.

2.6.4.2 Guidelines for DDC (I^2C) layout design

The DDC (I^2C) serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.5 SDIO interface

2.6.5.1 Guidelines for SDIO circuit design

☞ The functionality of the SDIO Secure Digital Input Output interface pins is not supported by LARA-R2 series modules "02" product versions: the pins should not be driven by any external device.

LARA-R2 series modules include a 4-bit Secure Digital Input Output interface (**SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK**, **SDIO_CMD**) designed to communicate with an external u-blox short range Wi-Fi module.

Combining a u-blox cellular module with a u-blox short range communication module gives designers full access to the Wi-Fi module directly via the cellular module, so that a second interface connected to the Wi-Fi module is not necessary. AT commands via the AT interfaces of the cellular module allows full control of the Wi-Fi module from any host processor, because Wi-Fi control messages are relayed to the Wi-Fi module via the dedicated SDIO interface.

☞ Further guidelines for SDIO interface circuit design will be described in detail in a successive release of the System Integration Manual.

☞ Do not apply voltage to any SDIO interface pin before the switch-on of SDIO interface supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module.

☞ ESD sensitivity rating of SDIO interface pins is 1 kV (HMB according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance ESD protection (e.g. Tyco Electronics PESD0402-140 ESD), close to accessible points.

☞ If the SDIO interface pins are not used, they can be left unconnected on the application board.

2.6.5.2 Guidelines for SDIO layout design

The SDIO serial interface requires the same consideration regarding electro-magnetic interference as any other high speed digital interface.

Keep the traces short, avoid stubs and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

Consider the usage of low value series damping resistors to avoid reflections and other losses in signal integrity, which may create ringing and loss of a square wave shape.

2.7 Audio interface

☞ Audio is not supported by LARA-R204 module "02" product version.

2.7.1 Digital audio interface

2.7.1.1 Guidelines for digital audio circuit design

I²S digital audio interface can be connected to an external digital audio device for voice applications.

Any external digital audio device compliant with the configuration of the digital audio interface of the LARA-R2 series cellular module can be used, given that the external digital audio device must provide:

- The opposite role: slave or master role, as LARA-R2 series modules may act as master or slave
- The same mode and frame format: PCM / short synch mode or Normal I²S / long synch mode with
  - data in 2's complement notation
  - MSB transmitted first
  - data word length = 16-bit (16 clock cycles)
  - frame length = synch signal period:
    - 17-bit or 18-bit in PCM / short alignment mode (16 + 1 or 16 + 2 clock cycles, with the Word Alignment / Synchronization signal set high for 1 clock cycle or 2 clock cycles)
    - 32-bit in Normal I²S mode / long alignment mode (16 x 2 clock cycles)
- The same sample rate, i.e. synch signal frequency, configurable by AT+UI2S <I2S_sample_rate> parameter
  - 8 kHz
  - 11.025 kHz
  - 12 kHz
  - 16 kHz
  - 22.05 kHz
  - 24 kHz
  - 32 kHz
  - 44.1 kHz
  - 48 kHz
- The same serial clock frequency:
  - 17 x <I2S_sample_rate> or 18 x <I2S_sample_rate> in PCM / short alignment mode, or
  - 16 x 2 x <I2S_sample_rate> in Normal I²S mode / long alignment mode
- Compatible voltage levels (1.80 V typ.), otherwise it is recommended to connect the 1.8 V digital audio interface of the module to the external 3.0 V (or similar) digital audio device by means of appropriate unidirectional voltage translators (e.g. TI SN74AVC4T774 or SN74AVC2T245, providing partial power down feature so that the digital audio device 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply), using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side

For the appropriate selection of a compliant external digital audio device, see section 1.10.1 and see the +UI2S AT command description in the u-blox AT Commands Manual [2] for further details regarding the capabilities and the possible settings of I²S digital audio interface of LARA-R2 series modules.

An appropriate specific application circuit has to be implemented and configured according to the particular external digital audio device or audio codec used and according to the application requirements.

Examples of manufacturers offering compatible audio codec parts are the following:

- Maxim Integrated (as the MAX9860, MAX9867, MAX9880A audio codecs)
- Texas Instruments / National Semiconductor
- Cirrus Logic / Wolfson Microelectronics
- Nuvoton Technology
- Asahi Kasei Microdevices
- Realtek Semiconductor

Figure 63 and Table 47 describe an application circuit for the I²S digital audio interface providing basic voice capability using an external audio voice codec, in particular the Maxim MAX9860 audio codec.

- DAC and ADC integrated in the external audio codec respectively converts an incoming digital data stream to analog audio output through a mono amplifier and converts the microphone input signal to the digital bit stream over the digital audio interface,
- A digital side-tone mixer integrated in the external audio codec provides loopback of the microphones/ADC signal to the DAC/headphone output.
- The module's I²S interface (I²S master) is connected to the related pins of the external audio codec (I²S slave).
- The **GPIO6** of the LARA-R2 series module (that provides a suitable digital output clock) is connected to the clock input of the external audio codec to provide clock reference.
- The external audio codec is controlled by the LARA-R2 series module using the DDC (I²C) interface, which can concurrently communicate with other I²C devices and control an external audio codec.
- The **V_INT** output supplies the external audio codec, defining proper digital interfaces voltage level.
- Additional components are provided for EMC and ESD immunity conformity: a 10 nF bypass capacitor and a series chip ferrite bead noise/EMI suppression filter provided on each microphone line input and speaker line output of the external codec as described in Figure 63 and Table 47. The necessity of these or other additional parts for EMC improvement may depend on the specific application board design.

Specific AT commands are available to configure the Maxim MAX9860 audio codec: for more details see the u-blox AT Commands Manual [2], +UEXTDCONF AT command.

As various external audio codecs other than the one described in Figure 63 and Table 47 can be used to provide voice capability, the appropriate specific application circuit has to be implemented and configured according to the particular external digital audio device or audio codec used and according to the application requirements.

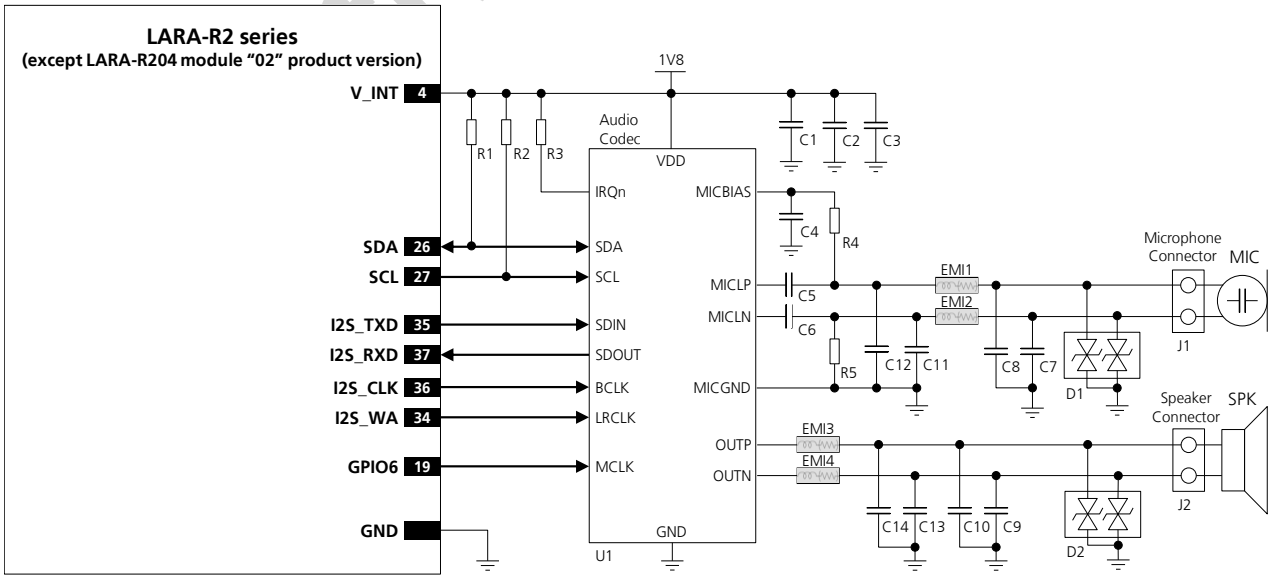


Figure 63: I²S interface application circuit with an external audio codec to provide voice capability

Reference	Description	Part Number – Manufacturer
C1	100 nF Capacitor Ceramic X5R 0402 10% 10V	GRM155R71C104KA01 – Murata
C2, C4, C5, C6	1 µF Capacitor Ceramic X5R 0402 10% 6.3 V	GRM155R60J105KE19 – Murata
C3	10 µF Capacitor Ceramic X5R 0603 20% 6.3 V	GRM188R60J106ME47 – Murata
C7, C8, C9, C10	27 pF Capacitor Ceramic COG 0402 5% 25 V	GRM1555C1H270JZ01 – Murata
C11, C12, C13, C14	10 nF Capacitor Ceramic X5R 0402 10% 50V	GRM155R71C103KA88 – Murata
D1, D2	Low Capacitance ESD Protection	USB0002RP or USB0002DP – AVX
EMI1, EMI2, EMI3, EMI4	Chip Ferrite Bead Noise/EMI Suppression Filter 1800 Ohm at 100 MHz, 2700 Ohm at 1 GHz	BLM15HD182SN1 – Murata
J1	Microphone Connector	Various manufacturers
J2	Speaker Connector	Various manufacturers
MIC	2.2 kΩ Electret Microphone	Various manufacturers
R1, R2	4.7 kΩ Resistor 0402 5% 0.1 W	RC0402JR-074K7L - Yageo Phycomp
R3	10 kΩ Resistor 0402 5% 0.1 W	RC0402JR-0710KL - Yageo Phycomp
R4, R5	2.2 kΩ Resistor 0402 5% 0.1 W	RC0402JR-072K2L – Yageo Phycomp
SPK	32 Ω Speaker	Various manufacturers
U1	16-Bit Mono Audio Voice Codec	MAX9860ETG+ - Maxim

Table 47: Example of components for audio voice codec application circuit

☞ Do not apply voltage to any I²S pin before the switch-on of I²S supply source (**V_INT**), to avoid latch-up of circuits and allow a proper boot of the module. If the external signals connected to the cellular module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, or TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.

☞ ESD sensitivity rating of I²S interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a general purpose ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

☞ If the I²S digital audio pins are not used, they can be left unconnected on the application board.

2.7.1.2 Guidelines for digital audio layout design

I²S interface and clock output lines require the same consideration regarding electro-magnetic interference as any other high speed digital interface. Keep the traces short and avoid coupling with RF lines / parts or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.7.1.3 Guidelines for analog audio layout design

Accurate design of the analog audio circuit is very important to obtain clear and high quality audio. The GSM signal burst has a repetition rate of 217 Hz that lies in the audible range. A careful layout is required to reduce the risk of noise from audio lines due to both **VCC** burst noise coupling and RF detection.

General guidelines for the uplink path (microphone), which is commonly the most sensitive, are the following:

- Avoid coupling of any noisy signal to microphone lines: it is strongly recommended to route microphone lines away from module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Avoid coupling between microphone and speaker / receiver lines.
- Optimize the mechanical design of the application device, the position, orientation and mechanical fixing (for example, using rubber gaskets) of microphone and speaker parts in order to avoid echo interference between uplink path and downlink path.

- Keep ground separation from microphone lines to other noisy signals. Use an intermediate ground layer or vias wall for coplanar signals.
- In case of external audio device providing differential microphone input, route microphone signal lines as a differential pair embedded in ground to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place bypass capacitor for RF very close to active microphone. The preferred microphone should be designed for GSM applications which typically have internal built-in bypass capacitor for RF very close to active device. If the integrated FET detects the RF burst, the resulting DC level will be in the pass-band of the audio circuitry and cannot be filtered by any other device.

General guidelines for the downlink path (speaker / receiver) are the following:

- The physical width of the audio output lines on the application board must be wide enough to minimize series resistance since the lines are connected to low impedance speaker transducer.
- Avoid coupling of any noisy signal to speaker lines: it is recommended to route speaker lines away from module **VCC** supply line, any switching regulator line, RF antenna lines, digital lines and any other possible noise source.
- Avoid coupling between speaker / receiver and microphone lines.
- Optimize the mechanical design of the application device, the position, orientation and mechanical fixing (for example, using rubber gaskets) of speaker and microphone parts in order to avoid echo interference between downlink path and uplink path.
- In case of external audio device providing differential speaker / receiver output, route speaker signal lines as a differential pair embedded in ground up to reduce differential noise pick-up. The balanced configuration will help reject the common mode noise.
- Cross other signals lines on adjacent layers with 90° crossing.
- Place bypass capacitor for RF close to the speaker.

2.8 General Purpose Input/Output (GPIO)

2.8.1.1 Guidelines for GPIO circuit design

A typical usage of LARA-R2 series modules' GPIOs can be the following:

- Network indication provided over **GPIO1** pin (see Figure 64 / Table 48 below)
- GNSS supply enable function provided by the **GPIO2** pin (see section 2.6.4)
- GNSS Tx data ready function provided by the **GPIO3** pin (see section 2.6.4)
- GNSS RTC sharing function provided by the **GPIO4** pin (see section 2.6.4)
- SIM card detection provided over **GPIO5** pin (see Figure 46 / Table 37 in section 2.5)

Figure 64: Application circuit for network indication provided over GPIO1

Reference	Description	Part Number - Manufacturer
R1	10 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	47 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	820 Ω Resistor 0402 5% 0.1 W	Various manufacturers
DL1	LED Red SMT 0603	LTST-C190KRKT - Lite-on Technology Corporation
T1	NPN BJT Transistor	BC847 - Infineon

Table 48: Components for network indication application circuit

☞ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of LARA-R2 series modules.

☞ Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply (**V_INT**), to avoid latch-up of circuits and allow a proper module boot. If the external signals connected to the module cannot be tri-stated or set low, insert a multi channel digital switch (e.g. TI SN74CB3Q16244, TS5A3159, TS5A63157) between the two-circuit connections and set to high impedance before **V_INT** switch-on.

☞ ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor array) close to accessible points.

☞ If the GPIO pins are not used, they can be left unconnected on the application board.

2.8.1.2 Guidelines for GPIO layout design

The general purpose input/output pins are generally not critical for layout.

2.9 Reserved pins (RSVD)

LARA-R2 series modules have pins reserved for future use, marked as **RSVD**. All the **RSVD** pins are to be left unconnected on the application board except the following **RSVD** pin, as described in Figure 65:

- the **RSVD** pin number **33** that must be externally connected to ground

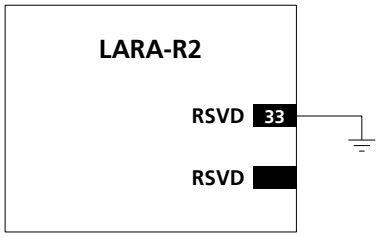


Figure 65: Application circuit for the reserved pins (RSVD)

2.10 Module placement

Optimize placement for minimum length of RF line and closer path from DC source for **VCC**.

Make sure that the module, RF and analog parts / circuits are clearly separated from any possible source of radiated energy, including digital circuits that can radiate some digital frequency harmonics, which can produce Electro-Magnetic Interference affecting module, RF and analog parts / circuits' performance or implement proper countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Make sure that the module, RF and analog parts / circuits, high speed digital circuits are clearly separated from any sensitive part / circuit which may be affected by Electro-Magnetic Interference or employ countermeasures to avoid any possible Electro-Magnetic Compatibility issue.

Provide enough clearance between the module and any external part.

☞ The heat dissipation during continuous transmission at maximum power can significantly raise the temperature of the application base-board below the LARA-R2 series modules: avoid placing temperature sensitive devices close to the module.

2.11 Module footprint and paste mask

Figure 66 and Table 49 describe the suggested footprint (i.e. copper mask) and paste mask layout for LARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder Mask Defined (NSMD) pad type is recommended over the Solder Mask Defined (SMD) pad type, implementing the solder mask opening 50 µm larger per side than the corresponding copper pad.

The recommended solder paste thickness is 150 µm, according to application production process requirements.

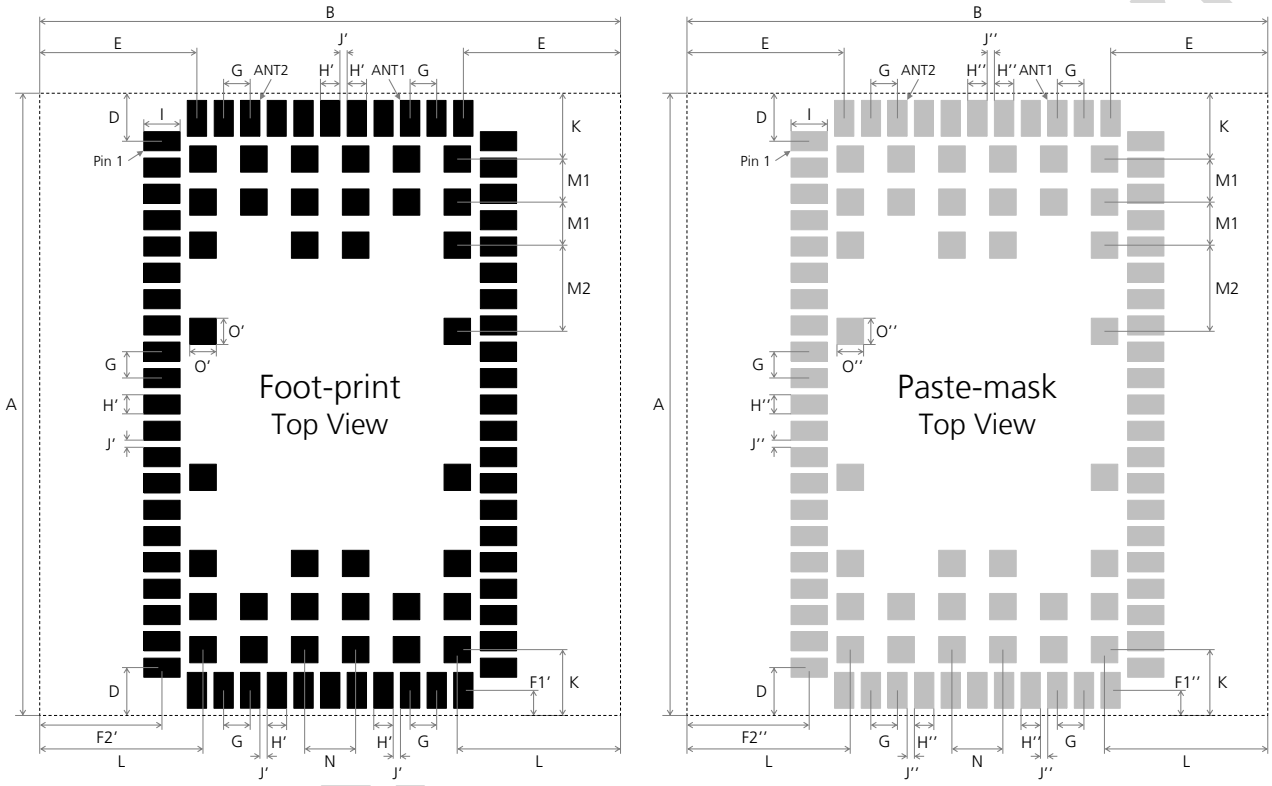


Figure 66: LARA-R2 series modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	F2''	5.00 mm	K	2.75 mm
B	24.0 mm	G	1.10 mm	L	6.75 mm
C	2.60 mm	H'	0.80 mm	M1	1.80 mm
D	2.00 mm	H''	0.75 mm	M2	3.60 mm
E	6.50 mm	I'	1.50 mm	N	2.10 mm
F1'	1.05 mm	I''	1.55 mm	O'	1.10 mm
F1''	1.00 mm	J'	0.30 mm	O''	1.05 mm
F2'	5.05 mm	J''	0.35 mm		

Table 49: LARA-R2 series modules suggested footprint and paste mask dimensions

☞ These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering etc.) of the customer.

2.12 Thermal guidelines

☞ Modules' operating temperature range is specified in LARA-R2 series Data Sheet [1].

The most critical condition concerning module thermal performance is the uplink transmission at maximum power (data upload in connected-mode), when the baseband processor runs at full speed, radio circuits are all active and the RF power amplifier is driven to higher output RF power. This scenario is not often encountered in real networks (for example, see the Terminal Tx Power distribution for WCDMA, taken from operation on a live network, described in the GSMA TS.09 Battery Life Measurement and Current Consumption Technique [16]); however the application should be correctly designed to cope with it.

During transmission at maximum RF power the LARA-R2 series modules generate thermal power that may exceed 2 W: this is an indicative value since the exact generated power strictly depends on operating condition such as the actual antenna return loss, the number of allocated TX resource blocks, the transmitting frequency band, etc. The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The spreading of the Module-to-Ambient thermal resistance ($R_{th,M-A}$) depends on the module operating condition. The overall temperature distribution is influenced by the configuration of the active components during the specific mode of operation and their different thermal resistance toward the case interface.

☞ The Module-to-Ambient thermal resistance value and the relative increase of module temperature will differ according to the specific mechanical deployments of the module, e.g. application PCB with different dimensions and characteristics, mechanical shells enclosure, or forced air flow.

The increase of the thermal dissipation, i.e. the reduction of the Module-to-Ambient thermal resistance, will decrease the temperature of the modules' internal circuitry for a given operating ambient temperature. This improves the device long-term reliability in particular for applications operating at high ambient temperature.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Connect each **GND** pin with solid ground layer of the application board and connect each ground area of the multilayer application board with complete thermal via stacked down to main ground layer.
- Provide a ground plane as wide as possible on the application board.
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the application device.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.

Further hardware techniques that may be considered to improve the heat dissipation in the application:

- Force ventilation air-flow within mechanical enclosure.
- Provide a heat sink component attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads of the LARA-R2 series LGA modules and dissipated over the backside of the application board.

For example, the Module-to-Ambient thermal resistance ($R_{th,M-A}$) is strongly reduced with forced air ventilation and a heat-sink installed on the back of the application board, decreasing the module temperature variation.

Beside the reduction of the Module-to-Ambient thermal resistance implemented by proper application hardware design, the increase of module temperature can be moderated by proper application software implementation:

- Enable power saving configuration using the AT+UPSV command (see section 1.14.16).
- Enable module connected-mode for a given time period and then disable it for a time period enough long to properly mitigate temperature increase.

2.13 ESD guidelines

The sections 2.13.1 and 2.13.2 are related to EMC / ESD immunity. The modules are ESD sensitive devices and the ESD sensitivity for each pin (as Human Body Model according to JESD22-A114F) is specified in LARA-R2 series Data Sheet [1]. Special precautions are required when handling: see section 3.2 for handling guidelines.

2.13.1 ESD immunity test overview

The immunity of devices integrating LARA-R2 series modules to Electro-Static Discharge (ESD) is part of the Electro-Magnetic Compatibility (EMC) conformity, which is required for products bearing the CE marking, compliant with the R&TTE Directive (99/5/EC), the EMC Directive (89/336/EEC) and the Low Voltage Directive (73/23/EEC) issued by the Commission of the European Community.

Compliance with these directives implies conformity to the following European Norms for device ESD immunity: ESD testing standard CENELEC EN 61000-4-2 [17] and the radio equipment standards ETSI EN 301 489-1 [18], ETSI EN 301 489-7 [19], ETSI EN 301 489-24 [20], which requirements are summarized in Table 50.

The ESD immunity test is performed at the enclosure port, defined by ETSI EN 301 489-1 [18] as the physical boundary through which the electromagnetic field radiates. If the device implements an integral antenna, the enclosure port is defined as all insulating and conductive surfaces housing the device. If the device implements a removable antenna, the antenna port can be separated from the enclosure port. The antenna port includes the antenna element and its interconnecting cable surfaces.

The applicability of the ESD immunity test to the whole device depends on the device classification as defined by ETSI EN 301 489-1 [18]. Applicability of the ESD immunity test to the relative device ports or the relative interconnecting cables to auxiliary equipments, depends on device accessible interfaces and manufacturer requirements, as defined by ETSI EN 301 489-1 [18].

Contact discharges are performed at conductive surfaces, while air discharges are performed at insulating surfaces. Indirect contact discharges are performed on the measurement setup horizontal and vertical coupling planes as defined in CENELEC EN 61000-4-2 [17].

☞ For the definition of integral antenna, removable antenna, antenna port, device classification see ETSI EN 301 489-1 [18], whereas for contact and air discharges definitions see CENELEC EN 61000-4-2 [17]

Application	Category	Immunity Level
All exposed surfaces of the radio equipment and ancillary equipment in a representative configuration	Contact Discharge	4 kV
	Air Discharge	8 kV

Table 50: EMC / ESD immunity requirements as defined by CENELEC EN 61000-4-2, ETSI EN 301 489-1, 301 489-7, 301 489-24

2.14 Schematic for LARA-R2 series module integration

Figure 67 is an example of a schematic diagram where a LARA-R2 series cellular module "02" product version is integrated into an application board, using all the available interfaces and functions of the module.

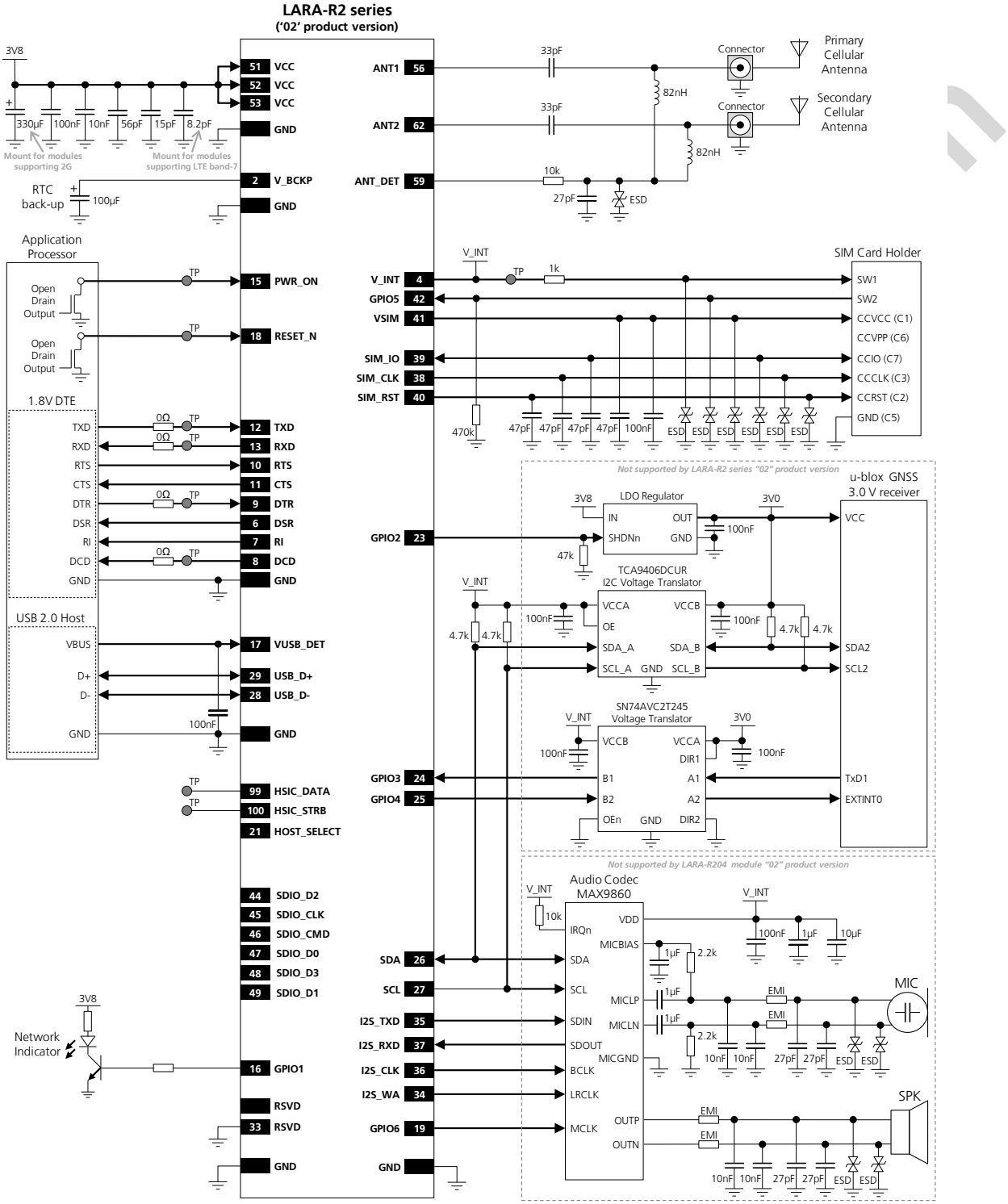


Figure 67: Example of schematic diagram to integrate a LARA-R2 module "02" product version using all available interfaces

2.15 Design-in checklist

This section provides a design-in checklist.

2.15.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting both the highest peak and the highest averaged current consumption values in connected-mode, as specified in the LARA-R2 series Data Sheet [1].
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Provide accessible test points directly connected to the following pins of the LARA-R2 series modules: **V_INT**, **PWR_ON** and **RESET_N** for diagnostic purpose.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, as the modules' signal names follow ITU-T V.24 Recommendation [5].
- ☑ Provide accessible test points directly connected to all the UART pins of the LARA-R2 series modules (**TXD**, **RXD**, **DTR**, **DCD**) for diagnostic purpose, in particular providing a 0 Ω series jumper on each line to detach each UART pin of the module from the DTE application processor.
- ☑ Capacitance and series resistance must be limited on each high speed line of the USB interface.
- ☑ If the USB is not used, provide accessible test points directly connected to the USB interface (**VUSB_DET**, **USB_D+** and **USB_D-** pins).
- ☑ Capacitance and series resistance must be limited on each high speed line of the HSIC interface.
- ☑ Consider providing appropriate low value series damping resistors on SDIO lines to avoid reflections.
- ☑ Add a proper pull-up resistor (e.g. 4.7 kΩ) to **V_INT** or another proper 1.8 V supply on each DDC (I^2C) interface line, if the interface is used.
- ☑ Check the digital audio interface specifications to connect a proper external audio device.
- ☑ Capacitance and series resistance must be limited on master clock output line and each I^2S interface line
- ☑ Consider passive filtering parts on each used analog audio line.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide proper precautions for ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of LARA-R2 series modules before the switch-on of the generic digital interface supply source (**V_INT**).
- ☑ All unused pins of LARA-R2 series modules can be left unconnected except the **RSVD** pin number **33**, which must be connected to GND.

2.15.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT1** and the **ANT2** ports (antenna RF interfaces).
- ☑ Ensure no coupling occurs between the RF interface and noisy or sensitive signals (primarily analog audio input/output signals, SIM signals, high-speed digital lines such as SDIO, USB and other data lines).
- ☑ Optimize placement for minimum length of RF line.
- ☑ Check the footprint and paste mask designed for LARA-R2 series module as illustrated in section 2.11.
- ☑ **VCC** line should be wide and as short as possible.
- ☑ Route **VCC** supply line away from RF lines / parts and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picoFarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Ensure an optimal grounding connecting each **GND** pin with application board solid ground layer.
- ☑ Use as many vias as possible to connect the ground planes on multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along RF and high speed lines.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.
- ☑ HSIC traces has to be designed as 50 Ω nominal characteristic impedance transmission lines
- ☑ Keep the SDIO traces short, avoid stubs, avoid coupling with any RF line / part and consider low value series damping resistors to avoid reflections and other losses in signal integrity.
- ☑ Ensure appropriate RF precautions for the Wi-Fi and Cellular technologies coexistence
- ☑ Ensure appropriate RF precautions for the GNSS and Cellular technologies coexistence as described in the GNSS Implementation Application Note [22].
- ☑ Route analog audio signals away from noisy sources (primarily RF interface, **VCC**, switching supplies).
- ☑ The audio outputs lines on the application board must be wide enough to minimize series resistance

2.15.3 Antenna checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement, as reported in sections 4.2.2 and/or 4.3.1 for products marked with the FCC and/or IC.
- ☑ Ensure high and similar efficiency for both the primary (**ANT1**) and the secondary (**ANT2**) antenna.
- ☑ Ensure high isolation between the primary (**ANT1**) and the secondary (**ANT2**) antenna.
- ☑ Ensure low Envelope Correlation Coefficient between the primary (**ANT1**) and the secondary (**ANT2**) antenna: the 3D antenna radiation patterns should have radiation lobes in different directions.
- ☑ Ensure high isolation between the cellular antennas and any other antenna or transmitter.

3 Handling and soldering

☞ No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage and moisture preconditioning

For information pertaining to LARA-R2 series reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the LARA-R2 series Data Sheet [1] and the u-blox Package Information Guide [25].

3.2 Handling

The LARA-R2 series modules are Electro-Static Discharge (ESD) sensitive devices.

⚠ **Ensure ESD precautions are implemented during handling of the module.**

Electrostatic discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of LARA-R2 series modules (as Human Body Model according to JESD22-A114F) is specified in the LARA-R2 series Data Sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from International Electrotechnical Commission (IEC) or American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be taken into account whenever handling the LARA-R2 series modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron,…).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in non ESD protected work area, implement proper ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD safe soldering iron.

For more robust designs, employ additional ESD protection measures on the application device integrating the LARA-R2 series modules, as described in section 2.13.3.

3.3 Soldering

3.3.1 Soldering paste

Use of "No Clean" soldering paste is strongly recommended, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering Paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% Tin / 3.9% Silver / 0.6% Copper)
	95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% Tin / 4.0% Silver / 0.5% Copper)
Melting Temperature:	217 °C
Stencil Thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.11

☞ The quality of the solder joints on the connectors ('half vias') should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the "IPC-7530 Guidelines for temperature profiling for mass soldering (reflow and wave) processes, published 2001".

Reflow profiles are to be selected according to the following recommendations.

⚠ **Failure to observe these recommendations can result in severe damage to the device!**

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s — If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 to 120 s — If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End Temperature: 150 to 200 °C — If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of 217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above 217 °C liquidus temperature: 40 to 60 s
- Peak reflow temperature: 245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects (solder becomes more brittle) of the solder and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

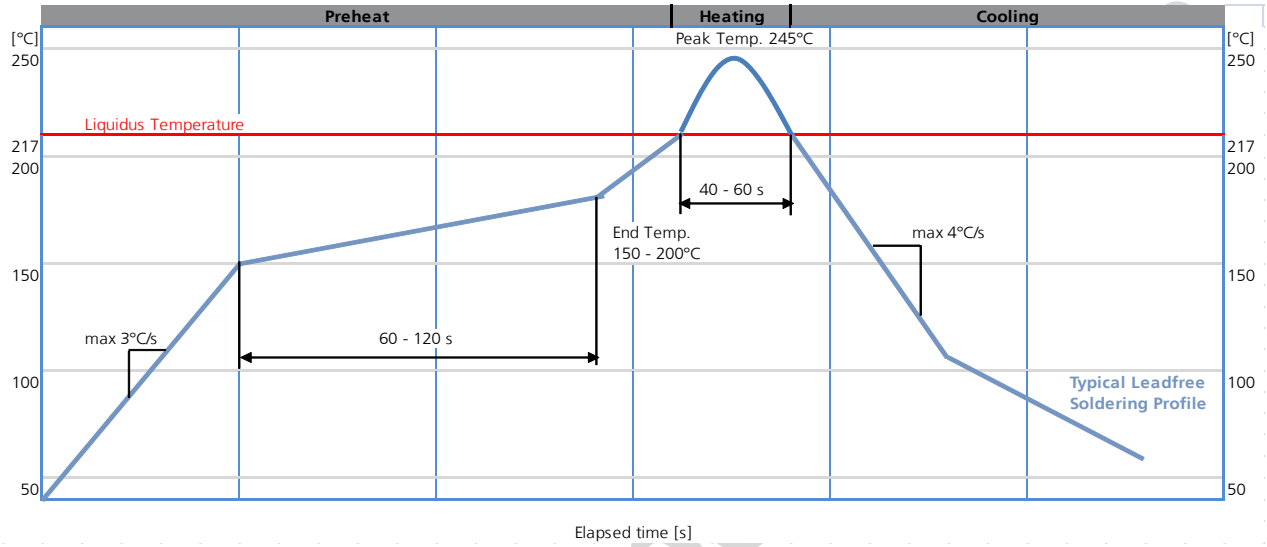


Figure 68: Recommended soldering profile

LARA-R2 series modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the LARA-R2 series modules, inspect the modules optically to verify that the module is properly aligned and centered.

3.3.4 Cleaning

Cleaning the soldered modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the two housings, areas that are not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results use a "no clean" soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Only a single reflow soldering process is encouraged for boards with a LARA-R2 series module populated on it.

3.3.6 Wave soldering

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. Only a single wave soldering process is encouraged for boards populated with LARA-R2 series modules.

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the RF properties of the LARA-R2 series modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal Coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the LARA-R2 series modules before implementing this in the production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interferences and noise.

☞ u-blox gives no warranty for damages to the LARA-R2 series modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

LARA-R2 series modules contain components which are sensitive to Ultrasonic Waves. Use of any Ultrasonic Processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty against damages to the LARA-R2 series modules caused by any Ultrasonic Processes.

4 Approvals

☞ For the complete list and specific details regarding the certification schemes approvals, see LARA-R2 series Data Sheet [1], or please contact the u-blox office or sales representative nearest you.

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called "certification schemes" that can be divided into three distinct categories:

- Regulatory certification
  - Country specific approval required by local government in most regions and countries, as:
    - CE (Conformité Européenne) marking for European Union
    - FCC (Federal Communications Commission) approval for United States
- Industry certification
  - Telecom industry specific approval verifying the interoperability between devices and networks:
    - GCF (Global Certification Forum), partnership between device manufacturers and network operators to ensure and verify global interoperability between devices and networks
    - PTCRB (PCS Type Certification Review Board), created by United States network operators to ensure and verify interoperability between devices and North America networks
- Operator certification
  - Operator specific approval required by some mobile network operator, as:
    - Verizon Wireless network operator in United States

Even if the LARA-R2 series modules are approved under all major certification schemes, the application device that integrates the modules must be approved under all the certification schemes required by the specific application device to be deployed in the market.

The required certification scheme approvals and relative testing specifications differ depending on the country or the region where the device that integrates LARA-R2 series modules must be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device must operate.

☞ The certification of the application device that integrates a LARA-R2 series module and the compliance of the application device with all the applicable certification schemes, directives and standards are the sole responsibility of the application device manufacturer.

LARA-R2 series modules are certified according to capabilities and options stated in the Protocol Implementation Conformance Statement document (PICS) of the module. The PICS, according to 3GPP Technical Specifications 51.010-2 [12], 36.521-2 [14] and 36.523-2 [15], is a statement of device capabilities and options.

☞ The PICS document of the application device integrating a LARA-R2 series module must be updated from the module PICS statement if any feature stated as supported by the module in its PICS document is not implemented or disabled in the application device. For more details regarding the AT commands settings that affect the PICS, see the u-blox AT Commands Manual [2].

☞ Check the specific settings required for mobile network operators approvals as they may differ from the AT commands settings defined in the module as integrated in the application device.

4.2 US Federal Communications Commission notice

United States Federal Communications Commission (FCC) IDs:

- u-blox LARA-R204 cellular modules: XPY1EIQN2NN

4.2.1 Safety warnings review the structure

- Equipment for building-in. The requirements for fire enclosure must be evaluated in the end product
- The clearance and creepage current distances required by the end product must be withheld when the module is installed
- The cooling of the end product shall not negatively be influenced by the installation of the module
- Excessive sound pressure from earphones and headphones can cause hearing loss
- No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed

4.2.2 Declaration of conformity

This device complies with Part 15 of the FCC rules and with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions:

- this device may not cause harmful interference
- this device must accept any interference received, including interference that may cause undesired operation

Radiofrequency radiation exposure Information: this equipment complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC procedures and as authorized in the module certification filing.

The gain of the system antenna(s) used for the LARA-R2 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 7.6 dBi (1700 MHz , i.e. LTE FDD-4) and 10.2 dBi (700 MHz, i.e. LTE FDD-13) for mobile and fixed or mobile operating configurations.

4.2.3 Modifications

The FCC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the LARA-R2 series modules are authorized to use the FCC Grants of the LARA-R2 series modules for their own final products according to the conditions referenced in the certificates.

The FCC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains FCC ID: XPY1EIQN2NN" resp.

IMPORTANT: Manufacturers of portable applications incorporating the LARA-R2 series modules are required to have their final product certified and apply for their own FCC Grant related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Additional Note: as per 47CFR15.105 this equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- **Reorient or relocate the receiving antenna**
- **Increase the separation between the equipment and receiver**
- **Connect the equipment into an outlet on a circuit different from that to which the receiver is connected**
- **Consultant the dealer or an experienced radio/TV technician for help**

4.3 Industry Canada notice

Industry Canada (IC) Certification Numbers:

- u-blox LARA-R204 cellular modules: 8595A-1EIQN2NN

4.3.1 Declaration of Conformity

Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The gain of the system antenna(s) used for the LARA-R2 series modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed 7.6 dBi (1700 MHz , i.e. LTE FDD-4) and 7.0 dBi (700 MHz, i.e. LTE FDD-13) for mobile and fixed or mobile operating configurations.

4.3.2 Modifications

The IC requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Manufacturers of mobile or fixed devices incorporating the LARA-R2 series modules are authorized to use the Industry Canada Certificates of the LARA-R2 series modules for their own final products according to the conditions referenced in the certificates.

The IC Label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

"Contains IC: 8595A-1EIQN2NN " resp.

Canada, Industry Canada (IC) Notices

This Class B digital apparatus complies with Canadian CAN ICES-3(B) / NMB-3(B) and RSS-210.

Operation is subject to the following two conditions:

- **this device may not cause interference**
- **this device must accept any interference, including interference that may cause undesired operation of the device**

Radio Frequency (RF) Exposure Information

The radiated output power of the u-blox Cellular Module is below the Industry Canada (IC) radio frequency exposure limits. The u-blox Cellular Module should be used in such a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the IC RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).

This device has been certified for use in Canada. Status of the listing in the Industry Canada's REL (Radio Equipment List) can be found at the following web address:

http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=eng

Additional Canadian information on RF exposure also can be found at the following web address: http://www.ic.gc.ca/eic/site/smt-gst.nsf/eng/sf08792.html

IMPORTANT: Manufacturers of portable applications incorporating the LARA-R2 series modules are required to have their final product certified and apply for their own Industry Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Canada, avis d'Industrie Canada (IC)

Cet appareil numérique de classe B est conforme aux normes canadiennes CAN ICES-3(B) / NMB-3(B) et CNR-210.

Son fonctionnement est soumis aux deux conditions suivantes:

- **cet appareil ne doit pas causer d'interférence**
- **cet appareil doit accepter toute interférence, notamment les interférences qui peuvent affecter son fonctionnement**

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans fil u-blox Cellular Module est inférieure à la limite d'exposition aux fréquences radio d'Industrie Canada (IC). Utilisez l'appareil de sans fil u-blox Cellular Module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (REL - Radio Equipment List) d'Industrie Canada rendez-vous sur:

http://www.ic.gc.ca/app/sitt/reltel/srch/nwRdSrch.do?lang=fra

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur: http://www.ic.gc.ca/eic/site/smt-gst.nsf/fra/sf08792.html

IMPORTANT: les fabricants d'applications portables contenant les modules LARA-R2 series doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat Industrie Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

4.4 R&TTED / RED and European Conformance CE mark

LARA-R211 modules have been evaluated against the essential requirements of the 1999/5/EC Directive.

In order to satisfy the essential requirements of the 1999/5/EC Directive, the modules are compliant with the following standards:

- Radio Frequency spectrum use (R&TTE art. 3.2):
  - EN 301 511
  - EN 301 908-1
  - EN 301 908-2
  - EN 301 908-13
- Electromagnetic Compatibility (R&TTE art. 3.1b):
  - EN 301 489-1
  - EN 301 489-7
  - EN 301 489-24
- Health and Safety (R&TTE art. 3.1a)
  - EN 60950-1:2006 + A11:2009 + A1:2010 + A12:2011 + A2:2013
  - EN 62311:2008

Radiofrequency radiation exposure Information: this equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The conformity assessment procedure for the modules, referred to in Article 10 and detailed in Annex IV of Directive 1999/5/EC, has been followed with the involvement of the following Notified Body number: 1588

Thus, the following marking is included in the product:

CE 1588

5 Product testing

5.1 u-blox in-series production test

u-blox focuses on high quality for its products. All units produced are fully tested automatically in production line. Stringent quality control process has been implemented in the production line. Defective units are analyzed in detail to improve the production quality.

This is achieved with automatic test equipment (ATE) in production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. Figure 69 illustrates typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests.

- Digital self-test (firmware download, Flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands (such as receiver S/N verification, frequency tuning of reference clock, calibration of transmitter and receiver power levels, etc.)
- Verification of RF characteristics after calibration (i.e. modulation accuracy, power levels, spectrum, etc. are checked to ensure they are all within tolerances when calibration parameters are applied)

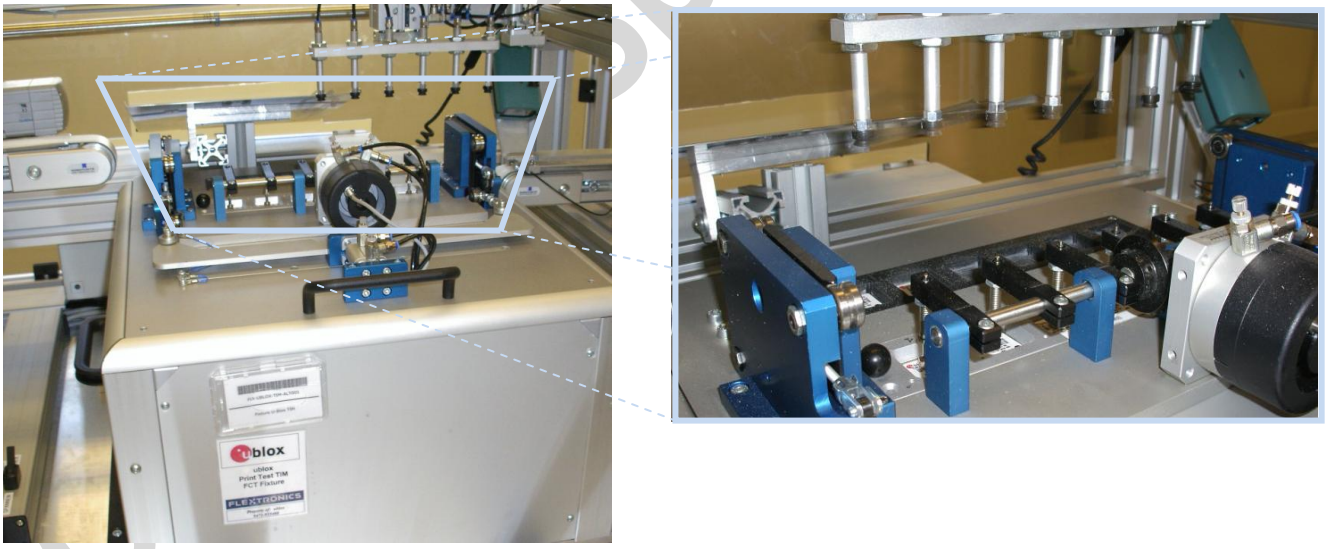


Figure 69: Automatic test equipment for module tests

5.2 Test parameters for OEM manufacturer

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

An OEM manufacturer should focus on:

- Module assembly on the device; it should be verified that:
  - Soldering and handling process did not damaged the module components
  - All module pins are well soldered on device board
  - There are no short circuits between pins
- Component assembly on the device; it should be verified that:
  - Communication with host controller can be established
  - The interfaces between module and device are working
  - Overall RF performance test of the device including antenna

Dedicated tests can be implemented to check the device. For example, the measurement of module current consumption when set in a specified status can detect a short circuit if compared with a "Golden Device" result.

In addition, module AT commands can be used to perform functional tests on digital interfaces (communication with host controller, check SIM interface, GPIOs, etc.), on audio interfaces (audio loop for test purposes can be enabled by the AT+UPAR=2 command as described in the u-blox AT Commands Manual [2]), and to perform RF performance tests (see the following section 5.2.2 for details).

5.2.1 "Go/No go" tests for integrated devices

A "Go/No go" test is typically to compare the signal quality with a "Golden Device" in a location with excellent network coverage and known signal quality. This test should be performed after data connection has been established. AT+CSQ is the typical AT command used to check signal quality in term of RSSI. See the u-blox AT Commands Manual [2] for detail usage of the AT command.

☞ These kinds of test may be useful as a "go/no go" test but not for RF performance measurements.

This test is suitable to check the functionality of communication with host controller, SIM card as well as power supply. It is also a means to verify if components at antenna interface are well soldered.

5.2.2 Functional tests providing RF operation

The overall RF functional test of the device including the antenna can be performed with basic instruments such as a spectrum analyzer (or an RF power meter) and a signal generator with the assistance of AT+UTEST command over AT command user interface.

The AT+UTEST command provides a simple interface to set the module to Rx or Tx test modes ignoring the cellular signaling protocol. The command can set the module into:

- transmitting mode in a specified channel and power level in all supported modulation schemes and bands
- receiving mode in a specified channel to returns the measured power level in all supported bands

☞ See the u-blox AT Commands Manual [2] and the End user test Application Note [24], for the AT+UTEST command syntax description and examples of use.

This feature allows the measurement of the transmitter and receiver power levels to check component assembly related to the module antenna interface and to check other device interfaces from which depends the RF performance.

To avoid module damage during transmitter test, a proper antenna according to module specifications or a 50 Ω termination must be connected to ANT1 port.

To avoid module damage during receiver test the maximum power level received at ANT1 and ANT2 ports must meet module specifications.

The AT+UTEST command sets the module to emit RF power ignoring cellular signaling protocol. This emission can generate interference that can be prohibited by law in some countries. The use of this feature is intended for testing purpose in controlled environments by qualified user and must not be used during the normal module operation. Follow instructions suggested in u-blox documentation. u-blox assumes no responsibilities for the inappropriate use of this feature.

Figure 70 illustrates a typical test setup for such RF functional test.

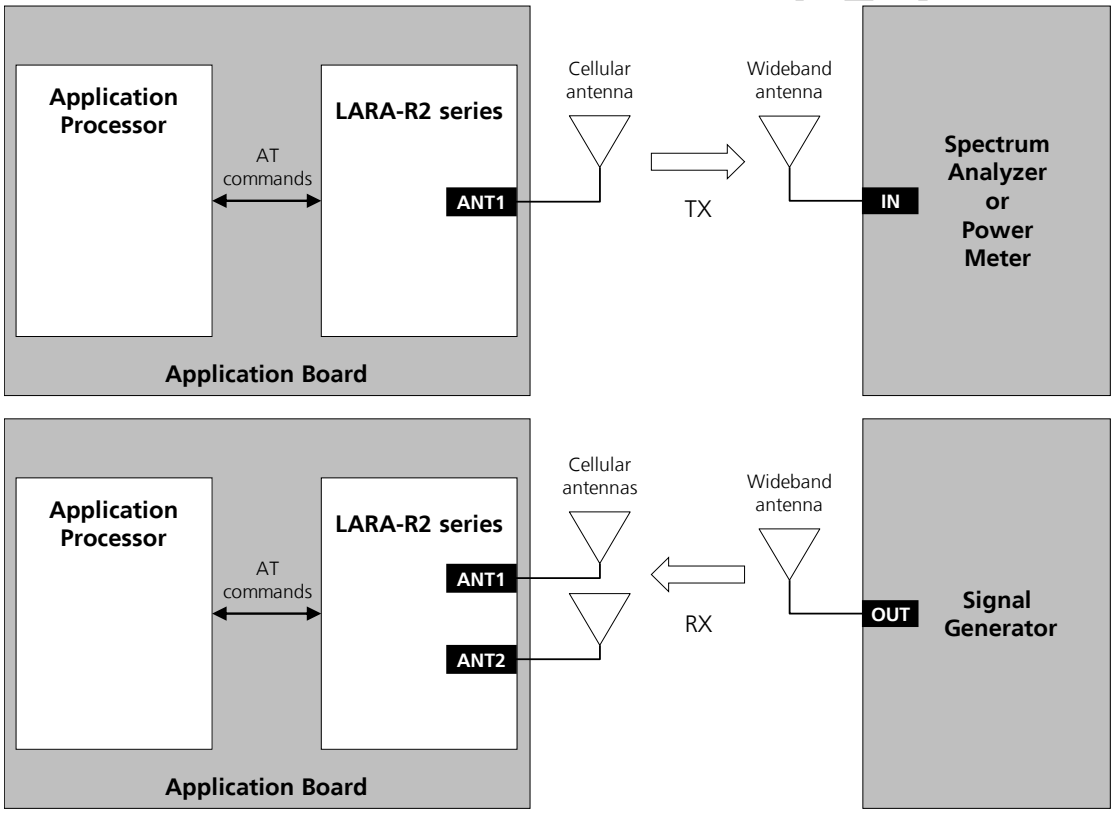


Figure 70: Setup with spectrum analyzer or power meter and signal generator for radiated measurements

Appendix

A Migration between SARA-U2 and LARA-R2

A.1 Overview

Migrating between u-blox SARA-U2 series 3G / 2G cellular modules and LARA-R2 series LTE Cat 1 / 2G cellular modules is a straightforward procedure that allows customers to take maximum advantage of their hardware and software investments.

The SARA cellular modules (26.0 x 16.0 mm, 96-pin LGA) have a different form factor than the LARA cellular modules (26.0 x 24.0 mm, 100-pin LGA), but the footprint of SARA and LARA modules has been developed to ensure layout compatibility as described in Figure 71, so that the modules can be alternatively mounted on the same single common application board.

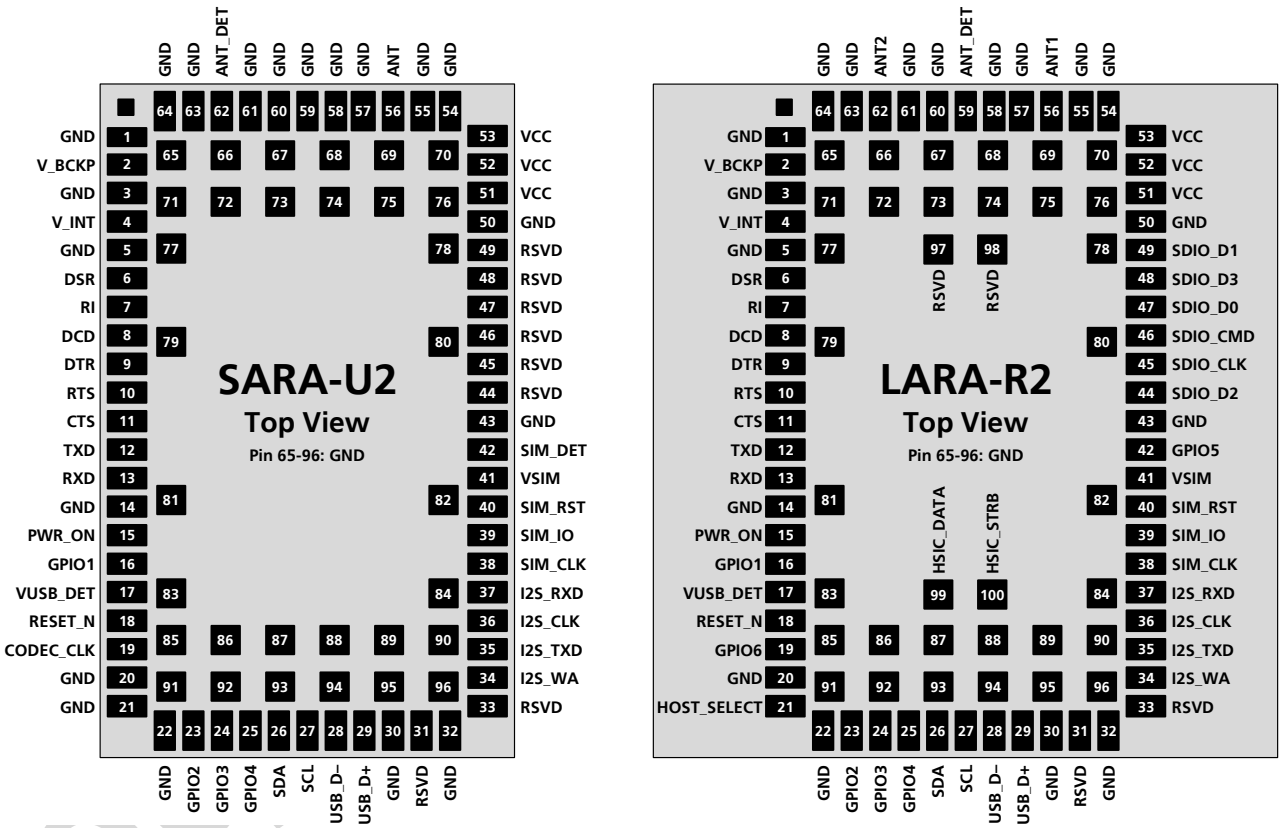


Figure 71: SARA-U2 and LARA-R2 series modules pin layout and pin assignment

SARA-U2 and LARA-R2 series modules are basically pin-to-pin compatible, given that LARA-R2 series modules provide further additional functions and interfaces, as shown in Figure 71:

- Secondary antenna
- SDIO interface
- HSIC interface
- HOST_SELECT function

SARA and LARA modules are also form-factor compatible with u-blox LISA and TOBY cellular module families: although SARA, LARA, LISA (33.2 x 22.4 mm, 76-pin LCC) and TOBY (35.6 x 24.8 mm, 152-pin LGA) modules each have different form factors, the footprints of all the SARA, LARA, LISA and TOBY modules have been developed to ensure layout compatibility.

With the u-blox "nested design" solution, any SARA, LARA, LISA or TOBY module can be alternatively mounted on the same space of a single "nested" application board as described in Figure 72, enabling straightforward development of products supporting different cellular radio access technologies.

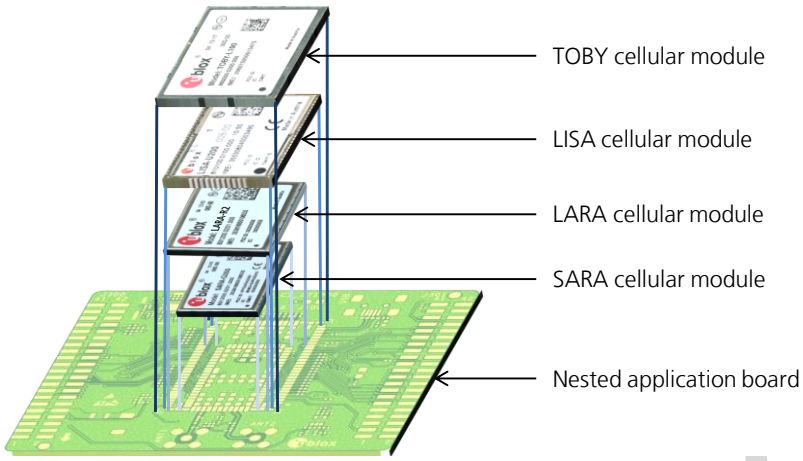
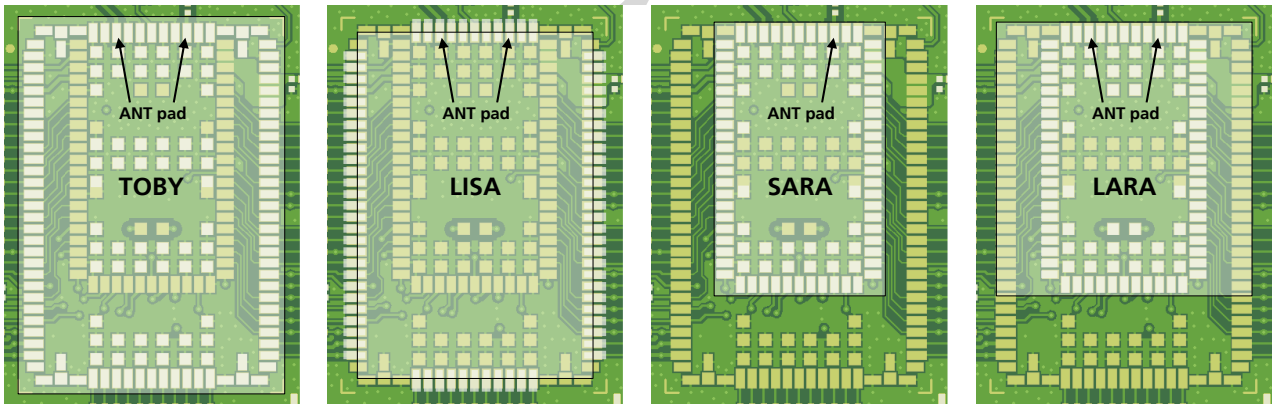


Figure 72: Nested design concept description: SARA, LARA, LISA and TOBY modules alternatively mounted on the same PCB

A different top-side stencil (paste mask) is needed for each form factor (SARA, LARA, LISA and TOBY) to be alternatively mounted on the same space of a single "nested" application board, as described in Figure 73.



TOBY mounting option with TOBY paste mask

LISA mounting option with LISA paste mask

SARA mounting option with SARA paste mask

LARA mounting option with LARA paste mask

Figure 73: Top-side stencil (paste mask) designs to alternatively mount SARA, LARA, LISA and TOBY modules on the same PCB

Detailed guidelines to implement a nested application board, comprehensive description of the u-blox reference nested design and detailed comparison between u-blox SARA, LARA, LISA and TOBY modules are provided in the Nested Design Application Note [26].

Table 51 summarizes the interfaces provided by SARA-U2 and LARA-R2 series modules: all the interfaces provided by different modules are electrically compatible, so that the same compatible external circuit can be implemented on the application board.

Module	RF / Radio Access Technology								Power			System			SIM		Serial					Audio		Other					
	LTE category	LTE bands	HSDPA category	HSUPA category	3G bands	Multi-slot class	2G bands	Rx diversity	Antenna Detection	VCC module supply in	V_BCKP	V_INT 1.8 V supply out	PWR_ON	RESET_N	Host select	SIM 1.8 V / 3.0 V	SIM detection	UART 1.8 V	USB 2.0	HSIC	SDIO 1.8 V	DDC (I^2C) 1.8 V	Analog audio	Digital audio	GPIOs 1.8 V	Network indication	Clock output	GNSS control	Wi-Fi control
SARA-U201			8	6	1,2,5 8,19	12	Quad		●	●	●	●	●	●		●	●	●	●			●		●		●	●	●	
SARA-U260			8	6	2,5	12	850 1900		●	●	●	●	●	●		●	●	●	●			●		●		●	●	●	
SARA-U270			8	6	1,8	12	900 1800		●	●	●	●	●	●		●	●	●	●			●		●		●	●	●	
SARA-U280			8	6	2,5				●	●	●	●	●	●		●	●	●	●			●		●		●	●	●	
LARA-R204	1	4,13						●	●	●	●	●	●	●	■	●	●	●	●	■	■	●		■		●	●	●	■	■
LARA-R211	1	3,7,20				12	900 1800	●	●	●	●	●	●	●	■	●	●	●	●	■	■	●		●		●	●	●	■	■

● = supported by all product versions ■ = supported by all product versions except version '02'

Table 51: Summary of SARA-U2 and LARA-R2 series modules interfaces

Figure 74 summarizes the LTE, 3G and 2G operating frequency bands of SARA-U2 and LARA-R2 series modules.

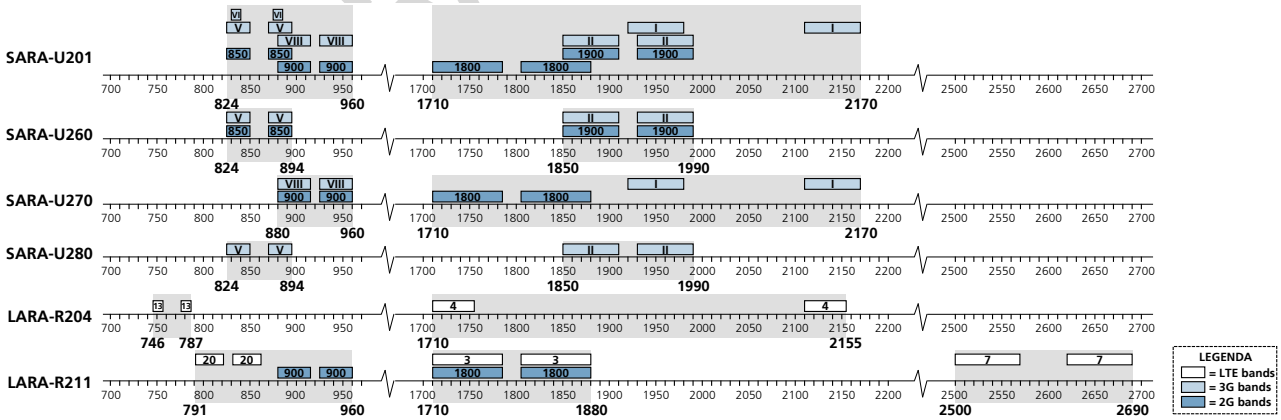


Figure 74: Summary of SARA-U2 and LARA-R2 series modules operating frequency bands

A.2 Pin-out comparison between SARA-U2 and LARA-R2

	SARA-U2		LARA-R2		
Pin No	**Pin Name**	**Description**	**Pin Name**	**Description**	**Remarks for migration**
1	GND	Ground	GND	Ground	
2	V_BCKP	RTC Supply I/O Output characteristics: 1.8 V typ, 3 mA max Input op. range: 1.0 V – 1.9 V	V_BCKP	RTC Supply I/O Output characteristics: 1.8 V typ, 3 mA max Input op. range: 1.0 V – 1.9 V	No functional difference
3	GND	Ground	GND	Ground	
4	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 50 mA max	V_INT	Interfaces Supply Out Output characteristics: 1.8 V typ, 50 mA max	No functional difference
5	GND	Ground	GND	Ground	
6	DSR	UART DSR Output 1.8 V, Driver strength: 1 mA	DSR	UART DSR Output 1.8 V, Driver strength: 6 mA	No functional difference
7	RI	UART RI Output 1.8 V, Driver strength: 2 mA	RI	UART RI Output 1.8 V, Driver strength: 6 mA	No functional difference
8	DCD	UART DCD Output 1.8 V, Driver strength: 2 mA	DCD	UART DCD Output 1.8 V, Driver strength: 6 mA	No functional difference
9	DTR	UART DTR Input 1.8 V, Internal pull-up: ~14 k	DTR	UART DTR Input 1.8 V, Internal pull-up: ~7.5 k	No functional difference
10	RTS	UART RTS Input 1.8 V, Internal pull-up: ~8 k	RTS	UART RTS Input 1.8 V, Internal pull-up: ~7.5 k	No functional difference
11	CTS	UART CTS Output 1.8 V, Driver strength: 6 mA	CTS	UART CTS Output 1.8 V, Driver strength: 6 mA	No functional difference
12	TXD	UART Data Input 1.8 V, Internal pull-up: ~8 k	TXD	UART Data Input 1.8 V, Internal pull-up: ~7.5 k	No functional difference
13	RXD	UART Data Output 1.8 V, Driver strength: 6 mA	RXD	UART Data Output 1.8 V, Driver strength: 6 mA	No functional difference
14	GND	Ground	GND	Ground	
15	PWR_ON	Power-on Input No internal pull-up L-level: -0.30 V – 0.65 V H-level: 1.50 V – 4.40 V ON L-level pulse time: 50 µs min / 80 µs max OFF L-level pulse time: 1 s min	PWR_ON	Power-on Input 10 kΩ internal pull-up to V_BCKP L-level: –0.30 V … 0.54 V H-level: 1.26 V … 2.10 V ON L-level pulse time: 50 µs min OFF L-level pulse time: Not supported	External → Internal pull-up Sligtlhy different input levels Switch-off over this pin is not supported by LARA-R2 series
16	GPIO1	1.8 V GPIO Driver strength: 6 mA	GPIO1	1.8 V GPIO Driver strength: 6 mA	No functional difference
17	VUSB_DET	USB Detect Input 5 V, Supply detection	VUSB_DET	USB Detect Input 5 V, Supply detection	No functional difference
18	RESET_N	Reset signal 10 kΩ internal pull-up L-level: -0.30 V – 0.51 V H-level: 1.32 V – 2.01 V Reset L-level pulse time: 50 ms min	RESET_N	Reset signal 10 kΩ internal pull-up L-level: -0.30 V – 0.51 V H-level: 1.32 V – 2.01 V Reset L-level pulse time: 50 ms min	No functional difference
19	CODEC_CLK	1.8 V Clock Output Driver strength: 4 mA	GPIO6	1.8 V Clock Output Driver strength: 6 mA	No functional difference
20	GND	Ground	GND	Ground	
21	GND	Ground	HOST_SELECT	1.8 V pin for module / host configuration selection[20]	GND → HOST_SELECT
22	GND	Ground	GND	Ground	
23	GPIO2	1.8 V GPIO Driver strength: 1 mA	GPIO2	1.8 V GPIO Driver strength: 6 mA	No functional difference
24	GPIO3	1.8 V GPIO Driver strength: 6 mA	GPIO3	1.8 V GPIO Driver strength: 6 mA	No functional difference
25	GPIO4	1.8 V GPIO Driver strength: 6 mA	GPIO4	1.8 V GPIO Driver strength: 6 mA	No functional difference

[20] Not supported by "02" product versions

	SARA-U2		LARA-R2		
Pin No	**Pin Name**	**Description**	**Pin Name**	**Description**	**Remarks for migration**
26	SDA	I²C Data I/O 1.8 V, open drain Driver strength: 1 mA	SDA	I²C Data I/O 1.8 V, open drain Driver strength: 1 mA	No functional difference
27	SCL	I²C Clock Output 1.8 V, open drain Driver strength: 1 mA	SCL	I²C Clock Output 1.8 V, open drain Driver strength: 1 mA	No functional difference
28	USB_D-	USB Data I/O (D-) High-Speed USB 2.0	USB_D-	USB Data I/O (D-) High-Speed USB 2.0	No functional difference
29	USB_D+	USB Data I/O (D+) High-Speed USB 2.0	USB_D+	USB Data I/O (D+) High-Speed USB 2.0	No functional difference
30	GND	Ground	GND	Ground	
31	RSVD	Reserved	RSVD	Reserved	No functional difference
32	GND	Ground	GND	Ground	
33	RSVD	Reserved To be externally connected to GND	RSVD	Reserved To be externally connected to GND	No functional difference
34	I2S_WA	I²S Word Alignment I/O, or GPIO 1.8 V, Driver strength: 2 mA	I2S_WA	I²S Word Alignment I/O[21], or GPIO 1.8 V, Driver strength: 6 mA	No functional difference
35	I2S_TXD	I²S Data Output, or GPIO 1.8 V, Driver strength: 2 mA	I2S_TXD	I²S Data Output[21], or GPIO 1.8 V, Driver strength: 6 mA	No functional difference
36	I2S_CLK	I²S Clock I/O, or GPIO 1.8 V, Driver strength: 2 mA	I2S_CLK	I²S Clock I/O[21], or GPIO 1.8 V, Driver strength: 6 mA	No functional difference
37	I2S_RXD	I²S Data Input, or GPIO 1.8 V, Inner pull-down: ~9 k	I2S_RXD	I²S Data Input[21], or GPIO 1.8 V, Inner pull-down: ~7.5 k	No functional difference
38	SIM_CLK	SIM Clock Output	SIM_CLK	SIM Clock Output	No functional difference
39	SIM_IO	SIM Data I/O	SIM_IO	SIM Data I/O	No functional difference
40	SIM_RST	SIM Reset Output	SIM_RST	SIM Reset Output	No functional difference
41	VSIM	SIM Supply Output	VSIM	SIM Supply Output	No functional difference
42	SIM_DET	1.8V SIM Detection	SIM_DET	1.8 V GPIO settable as SIM Detection	No functional difference
43	GND	Ground	GND	Ground	
44	RSVD	Reserved	SDIO_D2	1.8 V, SDIO serial data [2][22]	RSVD → SDIO
45	RSVD	Reserved	SDIO_CLK	1.8 V, SDIO serial clock[22]	RSVD → SDIO
46	RSVD	Reserved	SDIO_CMD	1.8 V, SDIO command[22]	RSVD → SDIO
47	RSVD	Reserved	SDIO_D0	1.8 V, SDIO serial data [0][22]	RSVD → SDIO
48	RSVD	Reserved	SDIO_D3	1.8 V, SDIO serial data [3][22]	RSVD → SDIO
49	RSVD	Reserved	SDIO_D1	1.8 V, SDIO serial data [1][22]	RSVD → SDIO
50	GND	Ground	GND	Ground	
51-53	VCC	Module Supply Input Normal range: 3.3 V – 4.4 V Extended range: 3.1 V – 4.5 V	VCC	Module Supply Input Normal range: 3.3 V – 4.4 V Extended range: 3.0 V – 4.5 V	No functional difference Larger range for LARA-R2
54-55	GND	Ground	GND	Ground	
56	ANT	RF Antenna Input/Output	ANT1	RF Antenna Input/Output (primary)	No functional difference
57-58	GND	Ground	GND	Ground	
59	GND	Ground	ANT_DET	Antenna Detection Input	GND → ANT_DET
60-61	GND	Ground	GND	Ground	
62	ANT_DET	Antenna Detection Input	ANT2	RF Antenna Input (secondary)	ANT_DET → ANT2
63-96	GND	Ground	GND	Ground	
97-98	-	Not Available	RSVD	Reserved	No functional difference
99	-	Not Available	HSIC_DATA	HSIC USB data line[22]	Not Available → HSIC
100	-	Not Available	HSIC_STRB	HSIC USB strobe line[22]	Not Available → HSIC

Table 52: SARA-U2 and LARA-R2 series modules pin assignment with remarks for migration

For further details regarding the characteristics, capabilities, usage or settings applicable for each interface of the SARA-U2 and LARA-R2 series modules, see LARA-R2 series Data Sheet [1], SARA-U2 series Data Sheet [27], SARA-G3 / SARA-U2 series System Integration Manual [28], u-blox AT Commands Manual [2] and Nested Design Application Note [26].

[21] Not supported by LARA-R204 module "02" product version.
[22] Not supported by "02" product versions.

A.3 Schematic for SARA-U2 and LARA-R2 integration

Figure 75 shows an example of schematic diagram where a SARA-U2 or a LARA-R2 series module can be integrated into the same application board, using all the available interfaces and functions of the modules. The different mounting options for the external parts are herein remarked according to the functions supported by each module.

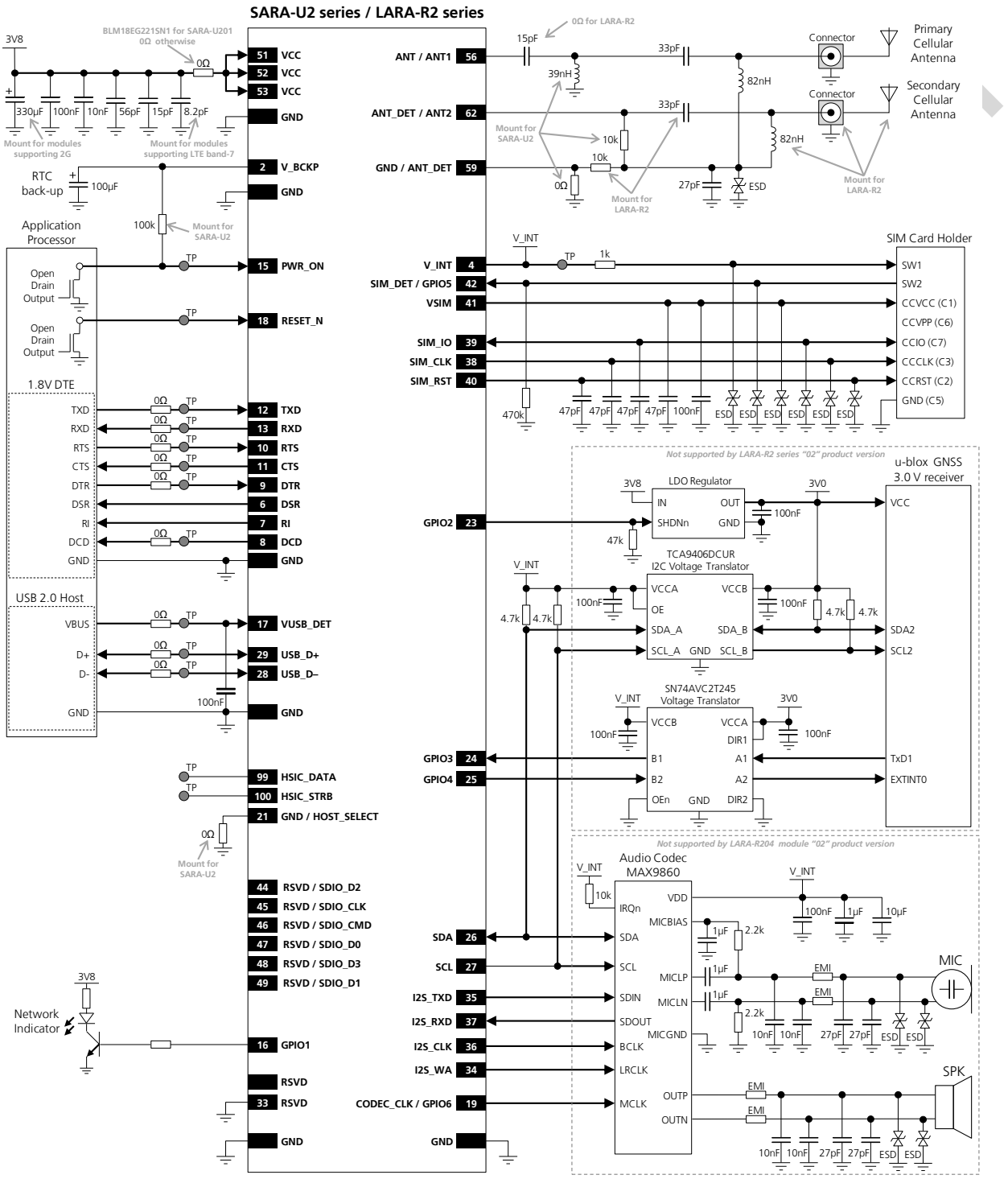


Figure 75: Example of complete schematic diagram to integrate SARA-U2 and LARA-R2 modules on the same application board

B Glossary

3GPP	3rd Generation Partnership Project
8-PSK	8 Phase-Shift Keying modulation
16QAM	16-state Quadrature Amplitude Modulation
ACM	Abstract Control Model
ADC	Analog to Digital Converter
AP	Application Processor
ASIC	Application-Specific Integrated Circuit
AT	AT Command Interpreter Software Subsystem, or attention
BAW	Bulk Acoustic Wave
CDC	Communication Device Class
CSFB	Circuit Switched Fall-Back
DC	Direct Current
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSP	Digital Signal Processing
DTE	Data Terminal Equipment
EDGE	Enhanced Data rates for GSM Evolution
EMC	Electro-magnetic Compatibility
EMI	Electro-magnetic Interference
ESD	Electro-static Discharge
ESR	Equivalent Series Resistance
FEM	Front End Module
FOAT	Firmware Over AT commands
FOTA	Firmware Over The Air
FTP	File Transfer Protocol
FW	Firmware
GMSK	Gaussian Minimum Shift Keying modulation
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global System for Mobile Communication
HBM	Human Body Model
HSIC	High Speed Inter Chip
HSDPA	High Speed Downlink Packet Access
HSUPA	High Speed Uplink Packet Access
HTTP	HyperText Transfer Protocol
HW	Hardware
I/Q	In phase and Quadrature
I^2C	Inter-Integrated Circuit interface
I^2S	Inter IC Sound interface
IP	Internet Protocol

LCC	Leadless Chip Carrier
LDO	Low-Dropout
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPDDR	Low Power Double Data Rate synchronous dynamic RAM memory
LTE	Long Term Evolution
MCS	Modulation Coding Scheme
N/A	Not Applicable
NCM	Network Control Model
OEM	Original Equipment Manufacturer device: an application device integrating a u-blox cellular module
OTA	Over The Air
PA	Power Amplifier
PCM	Pulse Code Modulation
PFM	Pulse Frequency Modulation
PMU	Power Management Unit
PWM	Pulse Width Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RSE	Radiated Spurious Emission
RTC	Real Time Clock
SAW	Surface Acoustic Wave
SDIO	Secure Digital Input Output
SDN / IN / PCN	Sample Delivery Note / Information Note / Product Change Notification
SIM	Subscriber Identification Module
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SRF	Self Resonant Frequency
TBD	To Be Defined
TCP	Transmission Control Protocol
TDMA	Time Division Multiple Access
TIS	Total Isotropic Sensitivity
TP	Test-Point
TRP	Total Radiated Power
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-Link (Transmission)
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
UTRA	UMTS Terrestrial Radio Access
VCO	Voltage Controlled Oscillator
VoLTE	Voice over LTE
VSWR	Voltage Standing Wave Ratio
Wi-Fi	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WLAN	Wireless Local Area Network (IEEE 802.11 short range radio technology)
WWAN	Wireless Wide Area Network (GSM / UMTS / LTE cellular radio technology)

Related documents

[1] u-blox LARA-R2 series Data Sheet, Docu No UBX-16005783

[2] u-blox AT Commands Manual, Docu No UBX-13002752

[3] u-blox EVK-R2xx User Guide, Docu No UBX-16016088

[4] u-blox Windows Embedded OS USB Driver Installation Application Note, Docu No UBX-14003263

[5] ITU-T Recommendation V.24 - 02-2000 - List of definitions for interchange circuits between the Data Terminal Equipment (DTE) and the Data Circuit-terminating Equipment (DCE). http://www.itu.int/rec/T-REC-V.24-200002-I/en

[6] 3GPP TS 27.007 – AT command set for User Equipment (UE) (Release 1999)

[7] 3GPP TS 27.005 – Use of Data Terminal Equipment – Data Circuit terminating; Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS) (Release 1999)

[8] 3GPP TS 27.010 – Terminal Equipment to User Equipment (TE-UE) multiplexer protocol (Release 1999)

[9] Universal Serial Bus Revision 2.0 specification, http://www.usb.org/developers/docs/usb20_docs/

[10] High-Speed Inter-Chip USB Specification, Ver. 1.0, http://www.usb.org/developers/docs/usb20_docs/

[11] I2C-bus specification and user manual - Rev. 5 - 9 October 2012 - NXP Semiconductors, http://www.nxp.com/documents/user_manual/UM10204.pdf

[12] 3GPP TS 51.010-2 – Technical Specification Group GSM/EDGE Radio Access Network; Mobile Station (MS) conformance specification; Part 2: Protocol Implementation Conformance Statement (PICS)

[13] 3GPP TS 36.521-1 - Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing

[14] 3GPP TS 36.521-2 - Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)

[15] 3GPP TS 36.523-2 - Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)

[16] GSM Association TS.09 - Battery Life Measurement and Current Consumption Technique http://www.gsma.com/newsroom/wp-content/uploads//TS.09_v8.0.pdf

[17] CENELEC EN 61000-4-2 (2001) – Electromagnetic compatibility (EMC); Part 4-2: Testing and measurement techniques; Electrostatic discharge immunity test

[18] ETSI EN 301 489-1 V1.8.1 – Electromagnetic compatibility and Radio spectrum Matters; EMC standard for radio equipment and services; Part 1: Common technical requirements

[19] ETSI EN 301 489-7 V1.3.1 – Electromagnetic compatibility and Radio spectrum Matters; EMC standard for radio equipment and services; Part 7: Specific conditions for mobile and portable radio and ancillary equipment of digital cellular radio telecommunications systems (GSM and DCS)

[20] ETSI EN 301 489-24 V1.4.1 – Electromagnetic compatibility and Radio spectrum Matters; EMC standard for radio equipment and services; Part 24: Specific conditions for IMT-2000 CDMA Direct Spread (UTRA) for Mobile and portable (UE) radio and ancillary equipment

[21] u-blox Multiplexer Implementation Application Note, Docu No UBX-13001887

[22] u-blox GNSS Implementation Application Note, Docu No UBX-13001849

[23] u-blox Firmware Update Application Note, Docu No UBX-13001845

[24] u-blox End user test Application Note, Docu No UBX-13001922

[25] u-blox Package Information Guide, Docu No UBX-14001652

[26] u-blox Nested Design Application Note, Docu No UBX-16007243

[27] u-blox SARA-U2 series Data Sheet, Docu No UBX-13005287

[28] u-blox SARA-G3 and SARA-U2 series System Integration Manual, Docu No UBX-13000995

Some of the above documents can be downloaded from u-blox web-site (http://www.u-blox.com).

Revision history

Revision	Date	Name	Status / Comments
R01	20-Sep-2016	sses	Initial release

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