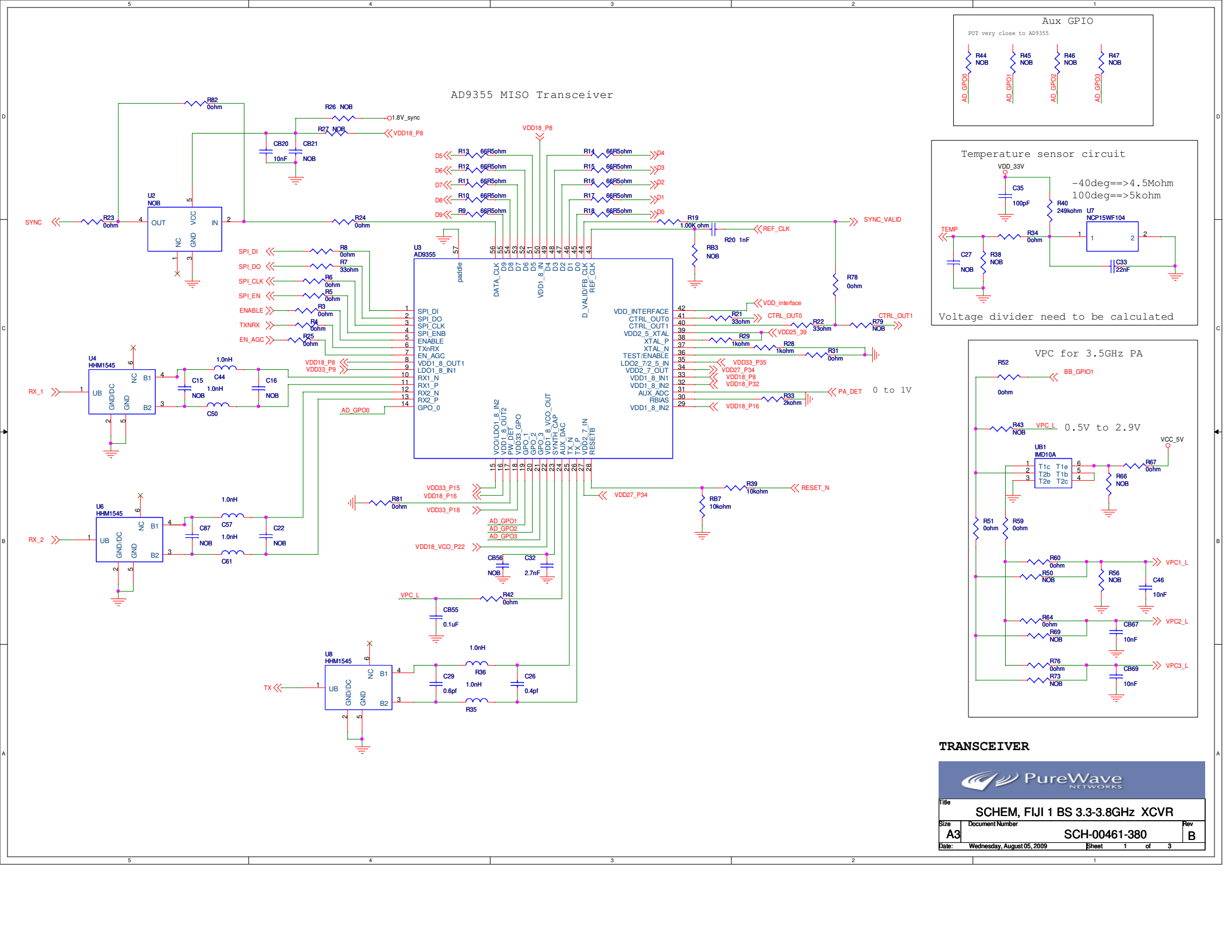
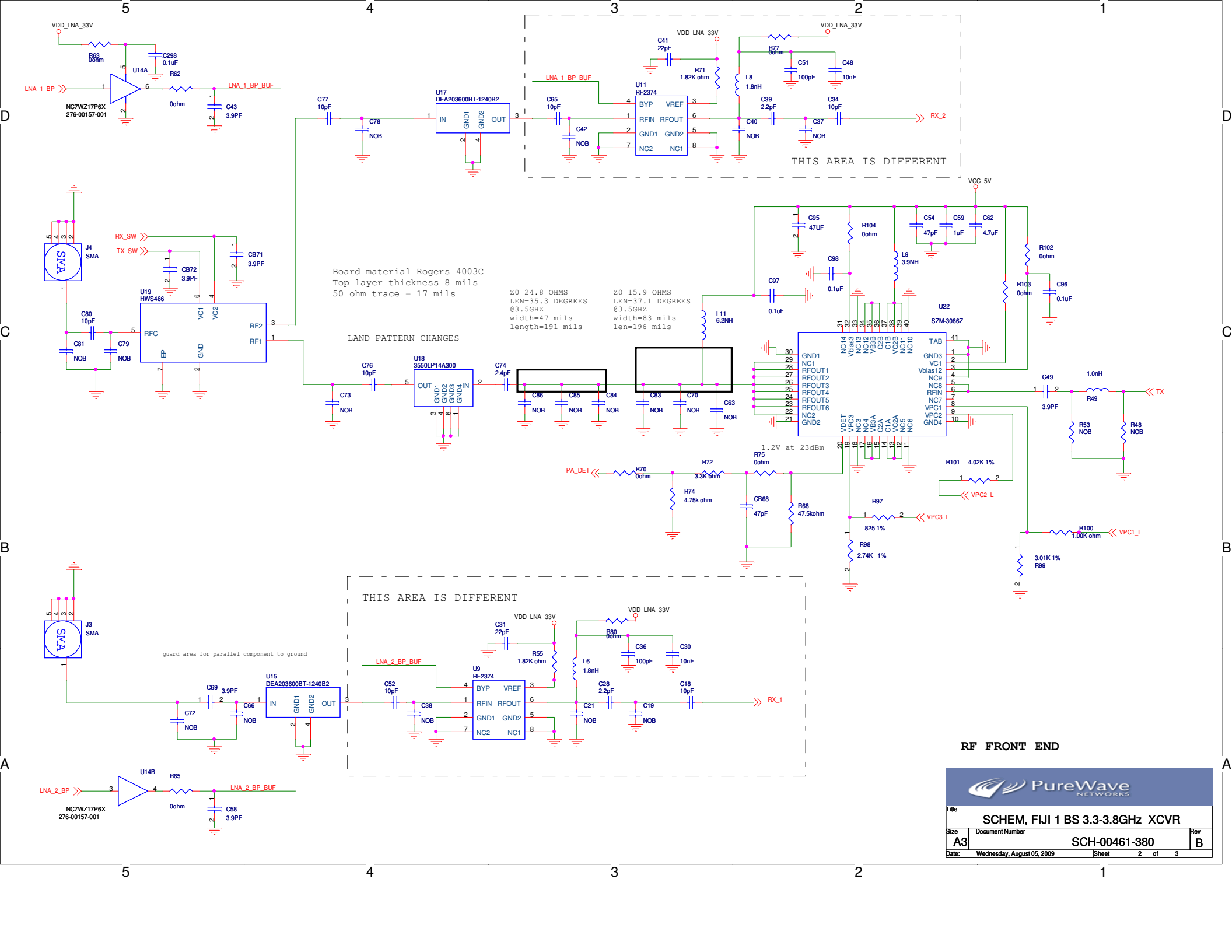
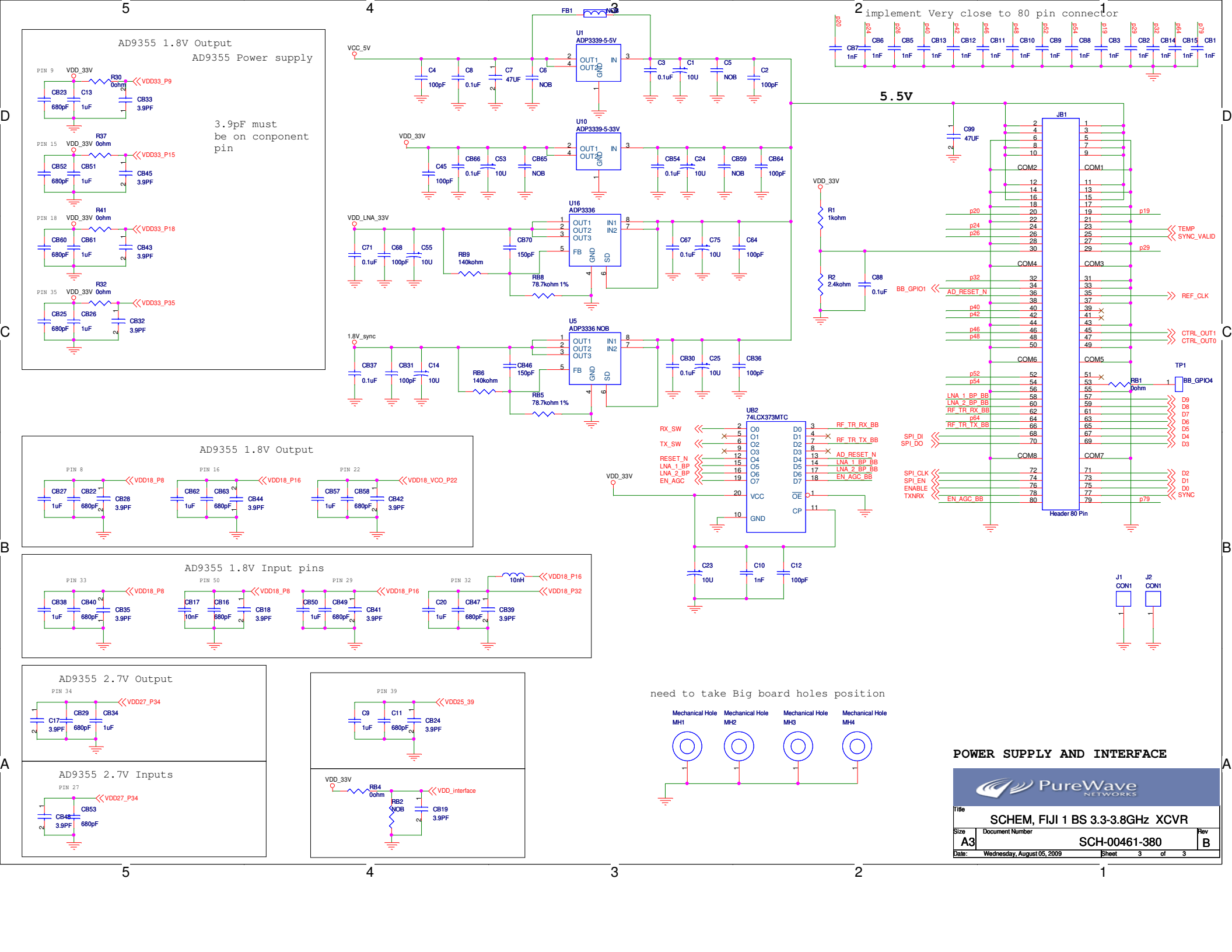


TRANSCEIVER

PureWave NETWORKS

Title	SCHEM, FIJI 1 BS 3.3-3.8GHz XCVR	
Size: A3	Document Number: SCH-00461-380	Rev: B
Date: Wednesday, August 05, 2009	Sheet 1 of 3	


VDD_LNA_33V
R63 0ohm
C298 0.1uF
U14A
R62
LNA_1_BP
LNA_1_BP_BUF
NC7WZ17P6X
276-00157-001
0ohm
C43 3.9PF
C77 10pF
C78 NOB
U17
DEA203600BT-1240B2
IN
GND1
GND2
OUT
C41 22pF
R71 1.82K ohm
C65 10pF
C42 NOB
U11
RF2374
BYP
VREF
RFIN
RFOUT
GND1
GND2
NC2
NC1
R77 0ohm
L8 1.8nH
C51 100pF
C48 10nF
C39 2.2pF
C40 NOB
C37 NOB
C34 10pF
RX_2
THIS AREA IS DIFFERENT
J4
SMA
RX_SW
TX_SW
CB71 3.9PF
CB72 3.9PF
U19
HWS466
VC1
VC2
RFC
RF2
RF1
EP
GND
C80 10pF
C81 NOB
C79 NOB
Board material Rogers 4003C
Top layer thickness 8 mils
50 ohm trace = 17 mils
Z0=24.8 OHMS
LEN=35.3 DEGREES
@3.5GHZ
width=47 mils
length=191 mils
Z0=15.9 OHMS
LEN=37.1 DEGREES
@3.5GHZ
width=83 mils
len=196 mils
LAND PATTERN CHANGES
C76 10pF
C73 NOB
U18
3550LP14A300
OUT
GND1
GND2
GND3
GND4
IN
C74 2.4pF
C86 NOB
C85 NOB
C84 NOB
C83 NOB
C70 NOB
C63 NOB
L11 6.2NH
VCC_5V
C95 47UF
C97 0.1uF
C98 0.1uF
R104 0ohm
L9 3.9NH
C54 47pF
C59 1uF
C62 4.7uF
R102 0ohm
R103 0ohm
C96 0.1uF
U22
SZM-3066Z
GND1
NC1
RFOUT1
RFOUT2
RFOUT3
RFOUT4
RFOUT5
RFOUT6
NC2
GND2
NC14
Vbias3
NC13
NC12
VB3
C2B
C1B
VC2B
NC11
NC10
TAB
GND3
VC1
Vbias12
NC9
NC8
RFIN
NC7
VPC1
VPC2
GND4
VDET
VPC3
NC3
VB4
C2A
C1A
VC2A
NC5
NC6
C49 3.9PF
1.0nH
R49
TX
R53 NOB
R48 NOB
1.2V at 23dBm
PA_DET
R70 0ohm
R72 3.3K ohm
R75 0ohm
R74 4.75k ohm
CB68 47pF
R68 47.5kohm
R101 4.02K 1%
VPC2_L
R97
825 1%
VPC3_L
R98 2.74K 1%
R100 1.00K ohm
VPC1_L
3.01K 1% R99
J3
SMA
guard area for parallel component to ground
C69 3.9PF
C72 NOB
C66 NOB
U15
DEA203600BT-1240B2
C31 22pF
R55 1.82K ohm
LNA_2_BP_BUF
C52 10pF
C38 NOB
U9
RF2374
L6 1.8nH
R80 0ohm
C36 100pF
C30 10nF
C28 2.2pF
C21 NOB
C19 NOB
C18 10pF
RX_1
THIS AREA IS DIFFERENT
U14B
R65
LNA_2_BP
LNA_2_BP_BUF
NC7WZ17P6X
276-00157-001
0ohm
C58 3.9PF
RF FRONT END
PureWave NETWORKS
Title
SCHEM, FIJI 1 BS 3.3-3.8GHz XCVR
Size A3
Document Number SCH-00461-380
Rev B
Date: Wednesday, August 05, 2009
Sheet 2 of 3


AD9355 1.8V Output
AD9355 Power supply
3.9pF must be on conponent pin
AD9355 1.8V Output
AD9355 1.8V Input pins
AD9355 2.7V Output
AD9355 2.7V Inputs
implement Very close to 80 pin connector
5.5V
need to take Big board holes position
Mechanical Hole MH1
Mechanical Hole MH2
Mechanical Hole MH3
Mechanical Hole MH4
Header 80 Pin
POWER SUPPLY AND INTERFACE
PureWave NETWORKS
SCHEM, FIJI 1 BS 3.3-3.8GHz XCVR
SCH-00461-380
Wednesday, August 05, 2009

Ext. Power IN

J1
CONN_PWR_2X2_H
D2
SS10P4
D1
SS10P4
VCC_12
DGND

D7 LED
R231 1000
D6 LED
R230 392
D5 LED
R217 150
VCC_5
VDD_33
VDD_18
VDD_13
TP1
TP7

STATUS

R218 332 1% 1003283
R219 332 1% 1003283
D3 LED
D4 LED
<6> GPIO_PA13
<6> GPIO_PB1

FB1 Ferrite 1002401
C1 0.1uF 1003323
CHASSIS

5V USB

Q2 NTGS4111PT1G 1002763
VCC_5
VBUS
C13 0.1uF 1002396
R12 10.0K 1001336 1%
R13 10.0K 1001336 1%
C12 1.0uF
VDD_33
Q3 N-CH 2N7002-7-F 1001604
C14 0.1uF NL

U5 FPMR12T
Vout TRIM GND Vin ON/OFF
FB3 8A
C25 10uF
C26 1.0uF
R216 1.47K
C2 47uF
C3 47uF

U6 FPMR12T
FB4 8A
C27 10uF
C28 1.0uF
R215 3.09K
C7 47uF
C6 47uF

R23 4750
R24 953
C34 1.0uF
R25 4750
R26 4750
C37 1.0uF

MONITORING

R212 402
R213 499
U9
IN0 IN1 IN2 IN3 IN4 IN5 IN6 IN7
VA VD AGND DGND
SCLK DIN DOUT CS
ADC108S022
VREF_41
C33 0.1uF 1002396
C32 1.0uF
U8 LM4040
R22 909
C293 0.1uF 1002396
C39 1.0uF
FB2 BLM15AG601SN1D
AGND

U11
GND NC GND(2) VCC VOUT
STLM20
C292 0.1uF 1002396
R28 200
C38 1.0uF
THERM0 <8>

<8,13> uP_SPI_CLK
<8,13> uP_SPI_MOSI
<8,13> uP_SPI_MISO
<7,8> uP_SPI_nCS0

J6 103186-1

REDUNDANT PS

U2
PVIN1 PVIN2 PVIN3 AVIN EN NC1 NC2 NC3 SW1 SW2 FB SS EXP AGND PGND1 PGND2 PGND3
LM2854
L1 2uH 5.4A
R204 86.6K
R202 1100
C281 100pF
R203 69.8K
C18 100uF 10V 1005201
C17 22uF 1003577
C15 10uF
C19 1500pF

DDR 1.8 @ 4A

U7 FPMR12T
FB5 8A
C29 10uF
C30 1.0uF
R214 18.2K
C5 47uF
C4 47uF

R21 34.8K
R20 12.1K
Q1
Q4
220-00012-001 MMBT3904
R19 10.0K
C31 4.7uF
R18 20.0K

RESET

S1 SW PUSHBUTTON-SPST-2
R15 22.1
C22 33pF 1002765
uP_nPORESET <4,8,11>

M HOLE1 MH8
M HOLE1 MH7
M HOLE1 MH2
M HOLE1 MH4
M HOLE1 MH3
M HOLE1 MH1
M HOLE1 MH6
M HOLE1 MH5
0.0 R201
0.0 R14
0.0 R17
0.0 R1
0.0 R194
0.0 R155
CHASSIS

Title: PMACNP - POWER
Size: B
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Date: Friday, June 05, 2009
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LAYOUT NOTE: PLACE R1 NEAR U1

LAYOUT NOTE: PLACE R2 NEAR U2

LAYOUT NOTE: PLACE R5 NEAR U3

LAYOUT NOTE: PLACE R6 NEAR U4

LAYOUT NOTE: EQUALLY SPLIT THESE CAPS AND PLACE NEAR U1, U2, U3, U4, AND U47 POWER PINS, OPPOSITE SIDE OF PCB IS PREFERRED

LAYOUT NOTE: PLACE ONE DECOUPLING CAPACITOR ON EACH VREF PIN OF U1, U2, U3, AND U4

U24 / U25 / U27 / U28
512Mb
MT47H64M16HR-3 IT:E
1006545

R205 / R206 / R210 / R211
0.0
NL

R42 / R38 / R34 / R31
100 1%
1003249

C87 / C79 / C57 / C46
2.2pF

C16
22uF
1003577

C21
22uF
1003577

C20
100uF
10V
1005201

C41 C43 C45 C47 C42
C55 C59 C291 C290 C51
C70 C289 C287 C69 C67
C72 C76 C286 C73 C81
C83 C285 C82 C88 C85
C54 C65 C44 C75
0.01uF
1001329

R29
4750
1%
1002429

R30
4750
1%
1002429

C40
4.7uF

Title	PMACNP - DDR2 MEMORY
Size C	Document Number SCH-00346-001 Rev B
Date: Friday, June 05, 2009	Sheet 2 of 13

U30E
MPC8360
1006699

MEMC1_MECC7 AN18 uP_MECC7
MEMC1_MECC6 AM22 uP_MECC6
MEMC1_MECC5 AM23 uP_MECC5
MEMC1_MECC4 AM24 uP_MECC4
MEMC1_MECC3 AN19 uP_MECC3
MEMC1_MECC2 AM19 uP_MECC2
MEMC1_MECC1 AN22 uP_MECC1
MEMC1_MECC0 AP24 uP_MECC0
MEMC1_MDQS8 AP26 uP_DQS8
MEMC1_MDM8 AP27 uP_DM8

MEMC1_MDQ63/MEMC2_MDQ31 AH3 uP_SDQ63
MEMC1_MDQ62/MEMC2_MDQ30 AK4 uP_SDQ62
MEMC1_MDQ61/MEMC2_MDQ29 AH4 uP_SDQ61
MEMC1_MDQ60/MEMC2_MDQ28 AJ3 uP_SDQ60
MEMC1_MDQ59/MEMC2_MDQ27 AJ2 uP_SDQ59
MEMC1_MDQ58/MEMC2_MDQ26 AK3 uP_SDQ58
MEMC1_MDQ57/MEMC2_MDQ25 AH5 uP_SDQ57
MEMC1_MDQ56/MEMC2_MDQ24 AL2 uP_SDQ56
MEMC1_MDQS7/MEMC2_MDQS3 AJ5 uP_DQS7 <2>
MEMC1_MDM7/MEMC2_MDM3 AJ6 uP_DM7 <2>

MEMC1_MDQ55/MEMC2_MDQ23 AM2 uP_SDQ55
MEMC1_MDQ54/MEMC2_MDQ22 AN4 uP_SDQ54
MEMC1_MDQ53/MEMC2_MDQ21 AL5 uP_SDQ53
MEMC1_MDQ52/MEMC2_MDQ20 AN5 uP_SDQ52
MEMC1_MDQ51/MEMC2_MDQ19 AN3 uP_SDQ51
MEMC1_MDQ50/MEMC2_MDQ18 AP3 uP_SDQ50
MEMC1_MDQ49/MEMC2_MDQ17 AM5 uP_SDQ49
MEMC1_MDQ48/MEMC2_MDQ16 AP4 uP_SDQ48
MEMC1_MDQS6/MEMC2_MDQS2 AL4 uP_DQS6 <2>
MEMC1_MDM6/MEMC2_MDM2 AM3 uP_DM6 <2>

MEMC1_MDQ47/MEMC2_MDQ15 AT3 uP_SDQ47
MEMC1_MDQ46/MEMC2_MDQ14 AR5 uP_SDQ46
MEMC1_MDQ45/MEMC2_MDQ13 AT5 uP_SDQ45
MEMC1_MDQ44/MEMC2_MDQ12 AT6 uP_SDQ44
MEMC1_MDQ43/MEMC2_MDQ11 AR3 uP_SDQ43
MEMC1_MDQ42/MEMC2_MDQ10 AR4 uP_SDQ42
MEMC1_MDQ41/MEMC2_MDQ9 AP6 uP_SDQ41
MEMC1_MDQ40/MEMC2_MDQ8 AU6 uP_SDQ40
MEMC1_MDQS5/MEMC2_MDQS1 AU3 uP_DQS5 <2>
MEMC1_MDM5/MEMC2_MDM1 AU4 uP_DM5 <2>

MEMC1_MDQ39/MEMC2_MDQ7 AP7 uP_SDQ39
MEMC1_MDQ38/MEMC2_MDQ6 AT7 uP_SDQ38
MEMC1_MDQ37/MEMC2_MDQ5 AN9 uP_SDQ37
MEMC1_MDQ36/MEMC2_MDQ4 AP9 uP_SDQ36
MEMC1_MDQ35/MEMC2_MDQ3 AM6 uP_SDQ35
MEMC1_MDQ34/MEMC2_MDQ2 AM8 uP_SDQ34
MEMC1_MDQ33/MEMC2_MDQ1 AN7 uP_SDQ33
MEMC1_MDQ32/MEMC2_MDQ0 AN8 uP_SDQ32
MEMC1_MDQS4/MEMC2_MDQS0 AT8 uP_DQS4 <2>
MEMC1_MDM4/MEMC2_MDM0 AT9 uP_DM4 <2>

MEMC1_MDQ31 AR29 uP_SDQ31
MEMC1_MDQ30 AN27 uP_SDQ30
MEMC1_MDQ29 AP29 uP_SDQ29
MEMC1_MDQ28 AN29 uP_SDQ28
MEMC1_MDQ27 AT32 uP_SDQ27
MEMC1_MDQ26 AR30 uP_SDQ26
MEMC1_MDQ25 AM27 uP_SDQ25
MEMC1_MDQ24 AP31 uP_SDQ24
MEMC1_MDQS3 AM26 uP_DQS3 <2>
MEMC1_MDM3 AN28 uP_DM3 <2>

MEMC1_MDQ23 AM30 uP_SDQ23
MEMC1_MDQ22 AM33 uP_SDQ22
MEMC1_MDQ21 AM34 uP_SDQ21
MEMC1_MDQ20 AN33 uP_SDQ20
MEMC1_MDQ19 AM31 uP_SDQ19
MEMC1_MDQ18 AP32 uP_SDQ18
MEMC1_MDQ17 AR32 uP_SDQ17
MEMC1_MDQ16 AP34 uP_SDQ16
MEMC1_MDQS2 AN31 uP_DQS2 <2>
MEMC1_MDM2 AP33 uP_DM2 <2>

MEMC1_MDQ15 AT35 uP_SDQ15
MEMC1_MDQ14 AR36 uP_SDQ14
MEMC1_MDQ13 AP36 uP_SDQ13
MEMC1_MDQ12 AR37 uP_SDQ12
MEMC1_MDQ11 AT34 uP_SDQ11
MEMC1_MDQ10 AR34 uP_SDQ10
MEMC1_MDQ9 AN35 uP_SDQ9
MEMC1_MDQ8 AN37 uP_SDQ8
MEMC1_MDQS1 AP35 uP_DQS1 <2>
MEMC1_MDM1 AN34 uP_DM1 <2>

MEMC1_MDQ7 AM36 uP_SDQ7
MEMC1_MDQ6 AK32 uP_SDQ6
MEMC1_MDQ5 AK34 uP_SDQ5
MEMC1_MDQ4 AJ33 uP_SDQ4
MEMC1_MDQ3 AL35 uP_SDQ3
MEMC1_MDQ2 AL33 uP_SDQ2
MEMC1_MDQ1 AK33 uP_SDQ1
MEMC1_MDQ0 AJ34 uP_SDQ0
MEMC1_MDQS0 AK35 uP_DQS0 <2>
MEMC1_MDM0 AL36 uP_DM0 <2>

MEMC1_MBA2 AT30 uP_SDBA2 <2>
MEMC1_MBA1 AU30 uP_SDBA1 <2>
MEMC1_MBA0 AU29 uP_SDBA0 <2>
MEMC1_MA14 AR18 uP_SDA14
MEMC1_MA13 AU20 uP_SDA13
MEMC1_MA12 AR22 uP_SDA12
MEMC1_MA11 AU23 uP_SDA11
MEMC1_MA10 AR28 uP_SDA10
MEMC1_MA9 AR23 uP_SDA9
MEMC1_MA8 AU24 uP_SDA8
MEMC1_MA7 AR26 uP_SDA7
MEMC1_MA6 AT23 uP_SDA6
MEMC1_MA5 AU26 uP_SDA5
MEMC1_MA4 AU25 uP_SDA4
MEMC1_MA3 AT21 uP_SDA3
MEMC1_MA2 AP21 uP_SDA2
MEMC1_MA1 AR22 uP_SDA1
MEMC1_MA0 AU21 uP_SDA0
uP_SDA[0:14] <2>

MEMC2_MCS1/MEMC1_MCS3 AU7
MEMC2_MCS0/MEMC1_MCS2 AU8
MEMC1_MCS1 AT27
MEMC1_MCS0 AU27 uP_nSDCS0 <2>

MEMC1_MCAS AT24 uP_nCAS <2>
MEMC1_MRAS AT29 uP_nRAS <2>
MEMC1_MWE AT26 uP_nSDWE <2>

MEMC2_MCK1/MEMC1_MCK3 AR2 uP_SDCK3+_R R33 10.0 1001339 1% uP_SDCK3+ <2>
MEMC2_MCK1/MEMC1_MCK3 AT2 uP_SDCK3-_R R32 10.0 1001339 1% uP_SDCK3- <2>
MEMC2_MCK0/MEMC1_MCK2 AN1 uP_SDCK2+_R R92 10.0 1001339 1% uP_SDCK2+ <2>
MEMC2_MCK0/MEMC1_MCK2 AP2 uP_SDCK2-_R R91 10.0 1001339 1% uP_SDCK2- <2>
MEMC1_MCK1 AT37 uP_SDCK1+_R R40 10.0 1001339 1% uP_SDCK1+ <2>
MEMC1_MCK1 AT36 uP_SDCK1-_R R41 10.0 1001339 1% uP_SDCK1- <2>
MEMC1_MCK0 AK37 uP_SDCK0+_R R101 10.0 1001339 1% uP_SDCK0+ <2>
MEMC1_MCK0 AL37 uP_SDCK0-_R R100 10.0 1001339 1% uP_SDCK0- <2>
MEMC1_MCKE1 AL32
MEMC1_MCKE0 AL32 uP_CKE0 <2>
MVREF2 AU32
MVREF1 AN20 VREF_09
SPARE3 AH32
TEST_SEL AU34 DGND

MEMC2_MECC0 AN16
MEMC2_MECC1 AP18
MEMC2_MECC2 AM16
MEMC2_MECC3 AM17
MEMC2_MECC4 AN17
MEMC2_MECC5 AP13
MEMC2_MECC6 AP15
MEMC2_MECC7 AN13
MEMC2_MDQS8/MEMC1_MCK5 AL1
MEMC2_MDM8/MEMC1_MCK4 AN24
MEMC2_MCKE0/MEMC1_MCK4 AN25
MEMC2_MCKE1/MEMC1_MCK5 AK1

R36 10.0 1% 1001339 uP_SDCK4- uP_SDCK4-_R
R37 10.0 1% 1001339 uP_SDCK4+ uP_SDCK4+_R

MEMC2_MBA2 AU13
MEMC2_MBA1 AU15
MEMC2_MBA0 AU12
MEMC2_MA0 AT12
MEMC2_MA1 AP11
MEMC2_MA2 AT13
MEMC2_MA3 AT14
MEMC2_MA4 AR13
MEMC2_MA5 AR15
MEMC2_MA6 AR16
MEMC2_MA7 AT16
MEMC2_MA8 AT18
MEMC2_MA9 AT17
MEMC2_MA10 AP10
MEMC2_MA11 AR20
MEMC2_MA12 AR17
MEMC2_MA13 AR14
MEMC2_MA14 AR11

VDD_18
R39 18.2 1% 1006531
MEMC2_MCAS AU11
MEMC2_MRAS AT11
MEMC2_MWE AU10
MDIC0 AH6
MDIC1 AP30
R93 18.2 1% 1006531 DGND
<2> uP_MODT0
MEMC1_MODT0 AG33
MEMC1_MODT1 AJ36
MEMC1_MODT2/MEMC2_MODT0 AT1
MEMC1_MODT3/MEMC2_MODT1 AK2
SPARE5 AP1
SPARE4 AU18 DGND

LAYOUT NOTE: PLACE R266 NEAR U47

VDD_18
VREF_09
R207 100 1% 1003249
C288 2.2pF
uP_SDCK4+
uP_SDCK4-
<2> uP_CKE0
J8 CK
K8 CK
K2 CKE

U26
512Mb
MT47H64M16HR-3 IT:E
1006545

VDD_18
<2> uP_nSDCS0 L8 CS
<2> uP_nSDWE K3 WE
<2> uP_nRAS K7 RAS
<2> uP_nCAS L7 CAS
R209 10.0K 1% 1001336
R208 10.0K 1% 1001336
B7 UDQS
uP_DQS8 A8 UDQS/NU
F7 LDQS
E8 LDQS/NU
B3 UDM
uP_DM8 F3 LDM
<2> uP_MODT0 K9 ODT
A2 NC
E2 NC
VSS A3 VSS E3 VSS E4 VSS N1 VSS P3
VSSQ A7 VSSQ B2 VSSQ B8 VSSQ D2 VSSQ D8 VSSQ E7 VSSQ F2 VSSQ F8 VSSQ H2 VSSQ H8 VSSDL J7
DGND

DQ15 B9
DQ14 B1
DQ13 D9
DQ12 D1
DQ11 D3
DQ10 D7
DQ9 C2
DQ8 C8
DQ7 F9 uP_MECC4
DQ6 E1 uP_MECC2
DQ5 H9 uP_MECC5
DQ4 H1 uP_MECC7
DQ3 H3 uP_MECC3
DQ2 H7 uP_MECC6
DQ1 G2 uP_MECC1
DQ0 G8 uP_MECC0

BA2 L1 uP_SDBA2 <2>
BA1 L3 uP_SDBA1 <2>
BA0 L2 uP_SDBA0 <2>

R35 0.0 NL
A15 R7
A14 R3 uP_SDA14_R4 uP_SDA14
A13 R8 uP_SDA13
A12 R2 uP_SDA12
A11 P7 uP_SDA11
A10 M2 uP_SDA10
A9 P3 uP_SDA9
A8 P8 uP_SDA8
A7 P2 uP_SDA7
A6 N7 uP_SDA6
A5 N3 uP_SDA5
A4 N8 uP_SDA4
A3 N2 uP_SDA3
A2 M7 uP_SDA2
A1 M3 uP_SDA1
A0 M8 uP_SDA0
uP_SDA[0:14] <2>

LAYOUT NOTE: A TREE ROUTING TOPOLOGY SHOULD BE USED FOR ALL SHARED DDR2 SIGNALS. REFER TO MICRON'S TN-47-20

LAYOUT NOTE: PLACE ONE DECOUPLING CAPACITOR ON EACH VREF PIN OF U5 AND U47

VREF_09
C84 0.01uF 1001329
C78 0.01uF 1001329
C129 0.01uF 1001329
DGND

Title: PMACNP - DDR2 INTERFACE
Size: C
Document Number: SCH-00346-001
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U30D
MPC8360
1006699

LAD0 N32 uP_LAD0
LAD1 N33 uP_LAD1
LAD2 N35 uP_LAD2
LAD3 N36 uP_LAD3
LAD4 P37 uP_LAD4
LAD5 P32 uP_LAD5
LAD6 P34 uP_LAD6
LAD7 R36 uP_LAD7
LAD8 R35 uP_LAD8
LAD9 R34 uP_LAD9
LAD10 R33 uP_LAD10
LAD11 T37 uP_LAD11
LAD12 T35 uP_LAD12
LAD13 T34 uP_LAD13
LAD14 T33 uP_LAD14
LAD15 U37 uP_LAD15
LAD16 T32 uP_LAD16
LAD17 U36 uP_LAD17
LAD18 U34 uP_LAD18
LAD19 V36 uP_LAD19
LAD20 V35 uP_LAD20
LAD21 W37 uP_LAD21
LAD22 W35 uP_LAD22
LAD23 V33 uP_LAD23
LAD24 V32 uP_LAD24
LAD25 W34 uP_LAD25
LAD26 Y36 uP_LAD26
LAD27 W32 uP_LAD27
LAD28 AA37 uP_LAD28
LAD29 Y33 uP_LAD29
LAD30 AA35 uP_LAD30
LAD31 AA34 uP_LAD31
LDP0/CKSTOP_OUT_B AB37
LDP1/CKSTOP_IN_B AB36
LDP2/LCS_B6 AB35
LDP3/LCS_B7 AA33
LA27 AC37 uP_LA27
LA28 AA32 uP_LA28
LA29 AC36 uP_LA29
LA30 AC34 uP_LA30
LA31 AD36 uP_LA31
LALE M37 uP_LALE
LCS0 AD33 uP_nLCS0
LCS1 AG37 uP_nLCS1
LCS2 AE34 uP_nLCS2
LCS3 AE33 uP_nLCS3
LCS4 AD32 uP_nLCS4
LCS5 AH37 uP_nLCS5
LWE0 AG35 uP_nLWE0
LWE1 AG34
LWE2 AH36
LWE3 AE32
LBCTL AD35
LSDA10_LGPL0/CFG_RESET_SOURCE[0] AB32
LSDWE/LGPL1/CFG_RESET_SOURCE[1] AE37
LSDRAS/LGPL2_LOE_B/RST_LOE_B AC33
LSDCAS/LGPL3/CFG_RESET_SOURCE[2] AD34
LGTA/LGPL4/LUPWAIT_LPBSE AE35
LGPL5/CFG_CLKIN_DIV AF36
LCKE G36
LCLK0 J33
LCLK1/LCS_B6 J34
LCLK2/LCS7/CORE_CLK_OUT/CE_CLK_OUT G37
LSYNC_OUT F34
LSYNC_IN G35

uP_LAD[31:0]

TP2 TP3 TP4 TP5 TP6 TP8 TP9

RN3 10K: uP_LAD27 uP_LAD28 uP_LAD29 uP_LAD30 uP_LAD31
R59 4750 1% NL
R60 4750 1% 1002996
R99 4750 1% 1002996
uP_LDP1 uP_LDP0 uP_LALE uP_LCLK
R148 22.1 1001374 1%
R150 22.1 1001374 1%
R151 0.0 NL
1001374

RN1 10K: uP_nLCS0 uP_nLCS1 uP_nLCS2 uP_nLCS3 uP_nLCS4 uP_nLCS5

R50 4750 1% 1002996
R48 4750 1% NL
R45 4750 1% NL
R53 4750 1% NL
R49 1000 1% 1001337
R51 1000 1% NL
R47 1000 1% 1001337
R46 1000 1% 1001337
R52 1000 1% 1001337
uP_LGPL0 uP_LGPL1 uP_LGPL2 uP_LGPL3 uP_LGPL4 uP_LGPL5

LAYOUT NOTE: R38 SHOULD BE CLOSE TO LSYNC_OUT

DLL Bypass Mode

VDD_33 VDD_18 DGND

R54 0.0 1001368
R55 0.0 NL
C89 0.1uF 1002396
C169 0.1uF 1002396

uP_LLAD6 R56 0.0 NL

U29
PC28F256P30T85
1006905

VCC VCC VCCQ RFU_J3/VCCQ_P30/33 RFU_J3/VCCQ_P30/33
NC/A25_on_512b NC/A24_on_256b NC/A23_on_128b
A22 A21 A20 A19 A18 A17 A16 A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0_J3/RFU_P30/33
uP_LLAD7 uP_LLAD8 uP_LLAD9 uP_LLAD10 uP_LLAD11 uP_LLAD12 uP_LLAD13 uP_LLAD14 uP_LLAD15 uP_LLAD16 uP_LLAD17 uP_LLAD18 uP_LLAD19 uP_LLAD20 uP_LLAD21 uP_LLAD22 uP_LLAD23 uP_LLAD24 uP_LLAD25 uP_LLAD26 uP_LA27 uP_LA28 uP_LA29 uP_LA30
CE0 CE1_J3/RFU_P30/33 CE2_J3/RFU_P30/33 RP# BYTE#_J3/RFU_P30/33 WE# OE# STS_J3/RFU_P30/33 VPEN RFU_J3/WP#_P30/33 RFU_J3/CLK_P30/33 RFU_J3/ADV#_P30/33 RFU_J3/WAIT_P30/33
DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
VSS VSS VSS RFU_J3/VSS_P30/33

R111 10.0K 1% NL
R44 10.0K 1% NL
R58 10.0K 1% 1001336
R43 10.0K 1% 1001336
R57 0.0 1001368 uP_nLCS0
uP_nPORESET <1,8,11>
R102 0.0 1001368 uP_nLWE0
R110 0.0 1001368 uP_LGPL2

R106 0.0 NL uP_LA27
R108 0.0 NL uP_LA28
R103 0.0 NL uP_nLWE0
R234 0.0 1001368 <7> NAND_RYnBY
R109 0.0 1001368 uP_LGPL2
R233 0.0 1001368 uP_nLCS1
R104 0.0 1001368 uP_LGPL1
R105 0.0 1001368 uP_LGPL3
R107 0.0 1001368 uP_LGPL0

R235 10.0K 1% 1001336
R232 10.0K 1% 1001336

U14
NAND08GW3B2CN6E
1002768
NANDxxxW3A0
RY/BY RE CE CLE ALE WE WP I/O1 I/O2 I/O3 I/O4 I/O5 I/O6 I/O7 I/O8
NC GND VCC VSS

LAYOUT NOTE: EQUALLY SPLIT THESE CAPS AND PLACE NEAR U6, U7, U8 AND U29 POWER PINS

C168 C166 C294 C283 0.1uF 1002396
C284 C282 C227 C167 0.1uF 1002396
C165 22uF 1003577

FREE: uP_nLCS[2..0]

LATCHES

U13
SN74LVTH162373
1006675
VCC GND #1OE #2OE 1LE 2LE 1D1 1D2 1D3 1D4 1D5 1D6 1D7 1D8 2D1 2D2 2D3 2D4 2D5 2D6 2D7 2D8 1Q1 1Q2 1Q3 1Q4 1Q5 1Q6 1Q7 1Q8 2Q1 2Q2 2Q3 2Q4 2Q5 2Q6 2Q7 2Q8
LATCH_nOE uP_LALE uP_LLAD[26:6] R61 10.0K 1% 1001336

U15
SN74AHC373PWR
1005199
OE LE VCC 1D 2D 3D 4D 5D 6D 7D 8D GND 1Q 2Q 3Q 4Q 5Q 6Q 7Q 8Q
RN5 22 1002428
R226 22.1 1001374

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LAYOUT NOTE: PLACE C36, C38, AND C39 NEAR U12 POWER PINS

LAYOUT NOTE: PLACE R40, R42, R44 NEAR U12

LAYOUT NOTE: PLACE R218, C316, C317, AND Y4 NEAR U12

LAYOUT NOTE: TRD+/- PAIRS MUST BE DIFFERENTIALLY ROUTED WITH 100 OHM IMPEDANCE

LAYOUT NOTE: PLACE C37, C40, AND C41 NEAR U13 POWER PINS

LAYOUT NOTE: PLACE R41, R43, R45 NEAR U13

LAYOUT NOTE: PLACE R218, C318, C319, AND Y5 NEAR U13

LAYOUT NOTE: TRD+/- PAIRS MUST BE DIFFERENTIALLY ROUTED WITH 100 OHM IMPEDANCE

U22 BCM5481UA2 1006547

U23 BCM5481UA2 1006547

U21 PI49FCT3803

Y3 25.0000MHz 1006862

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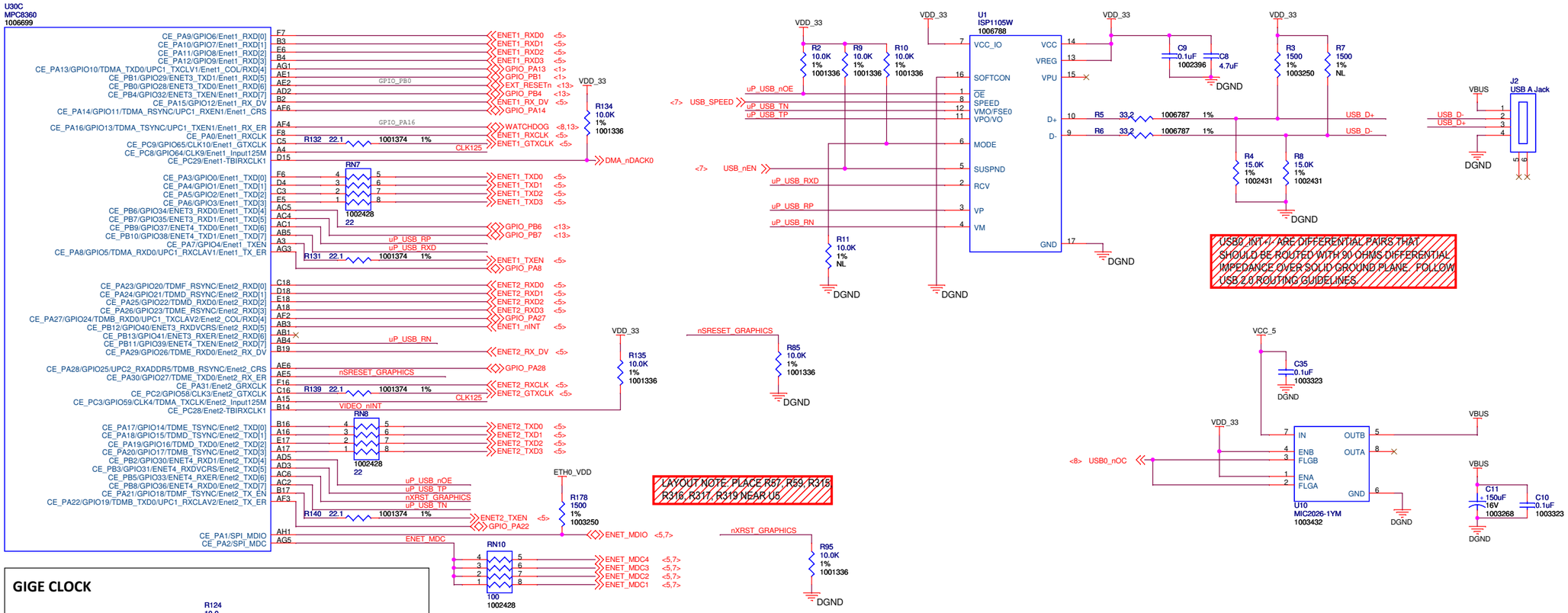

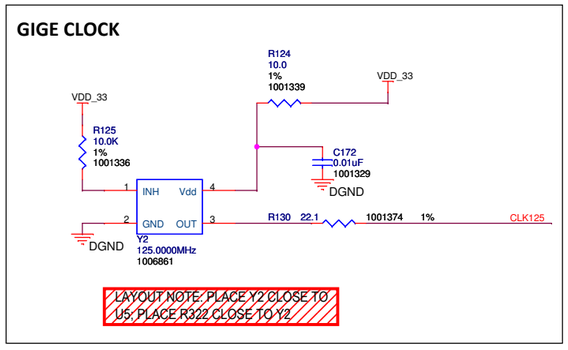

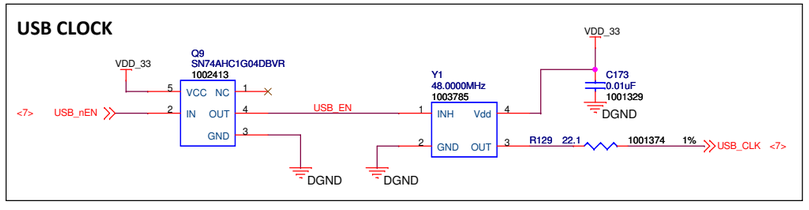

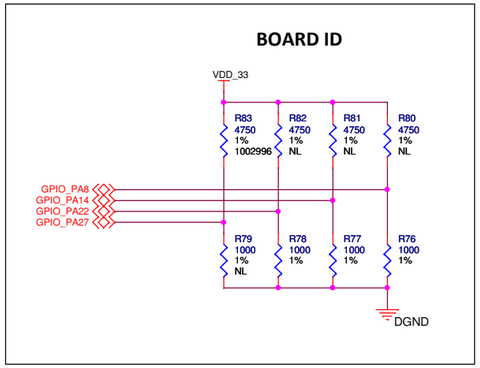

Deleted R84, Added RN10, broke ENET_MDC into 4 seperate nets

Title	PMACNP - ETHERNET INTERFACE/USB		
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LAYOUT NOTE: PLACE C75, C76, C77 AND C78 NEAR U17 POWER PINS

LAYOUT NOTE: PLACE R223, C320, C321, AND Y6 NEAR U17

NOTE: REFER TO MANUFACTURES DATA SHEET FOR CHARACTERISTIC IMPEDENCE AND RECOMMENDED ROUTING STRATEGIES FOR ETHERNET DIFFERENTIAL PAIRS

NOTE: ROUTE ENET_TX+/- SIGNALS AS DIFFERENTIAL PAIRS, ROUTE ENET_RX+/- AS DIFFERENTIAL PAIRS

LAYOUT NOTE: PLACE C83, C84, C85 AND C86 NEAR U18 POWER PINS

LAYOUT NOTE: PLACE R224, C322, C323, AND Y7 NEAR U18

U19
DP83848IVV NOPB
1003254

U18
DP83848IVV NOPB
1003254

U30B
MPC8360
1006699

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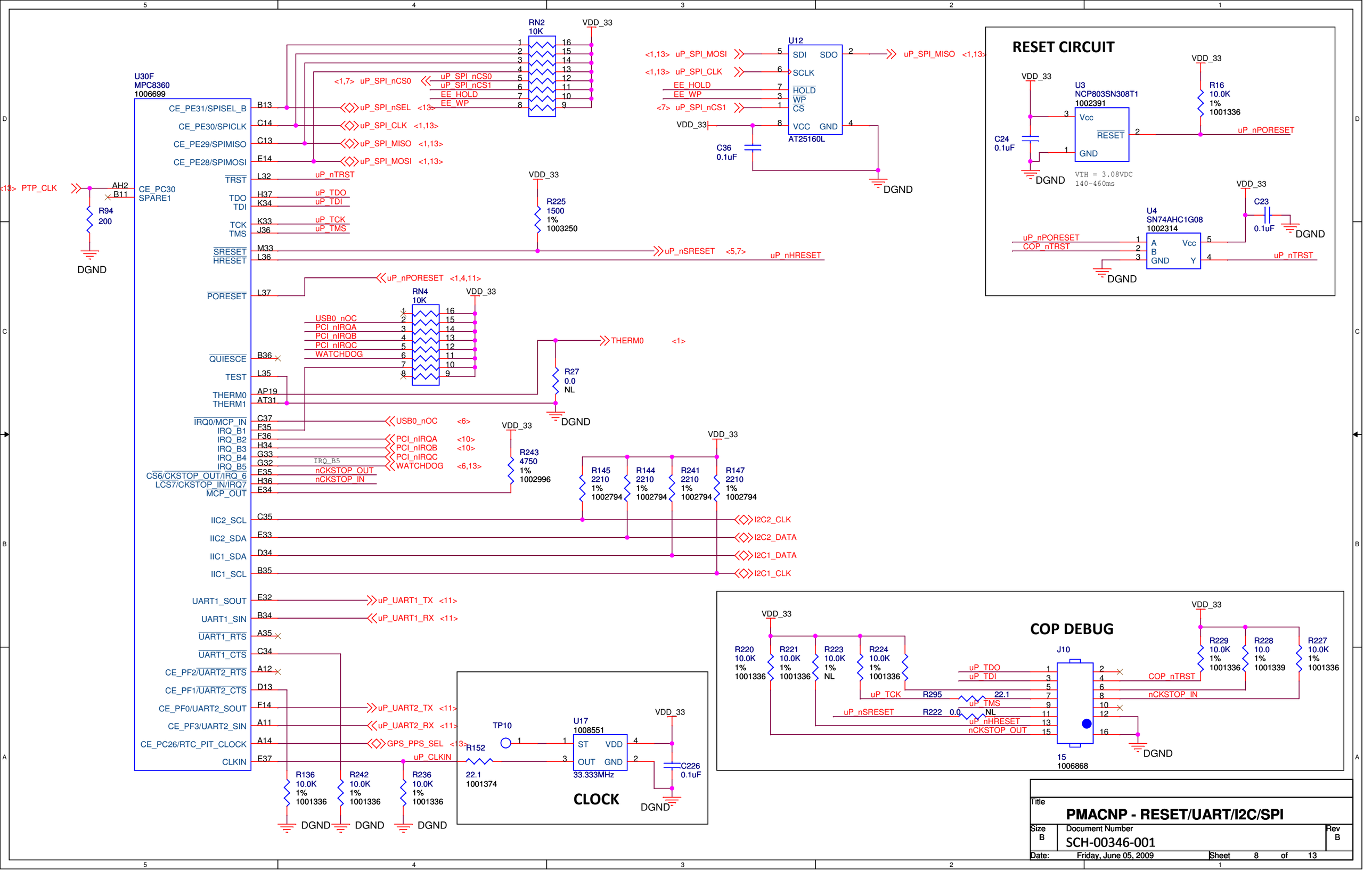
RESET CIRCUIT
U30F
MPC8360
1006699
RN2
10K
VDD_33
U12
AT25160L
U3
NCP803SN308T1
1002391
R16
10.0K
1%
1001336
C24
0.1uF
VTH = 3.08VDC
140-460ms
U4
SN74AHC1G08
1002314
C23
0.1uF
R94
200
R225
1500
1%
1003250
RN4
10K
R27
0.0
NL
R243
4750
1%
1002996
R145
R144
R241
R147
2210
1%
1002794
C36
0.1uF
R136
R242
R236
10.0K
1%
1001336
TP10
R152
22.1
1001374
U17
1008551
33.333MHz
CLOCK
C226
0.1uF
COP DEBUG
J10
15
1006868
R220
R221
R223
R224
R229
R228
R227
10.0K
10.0
1%
1001339
R295
22.1
R222
0.0
NL
Title
PMACNP - RESET/UART/I2C/SPI
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B
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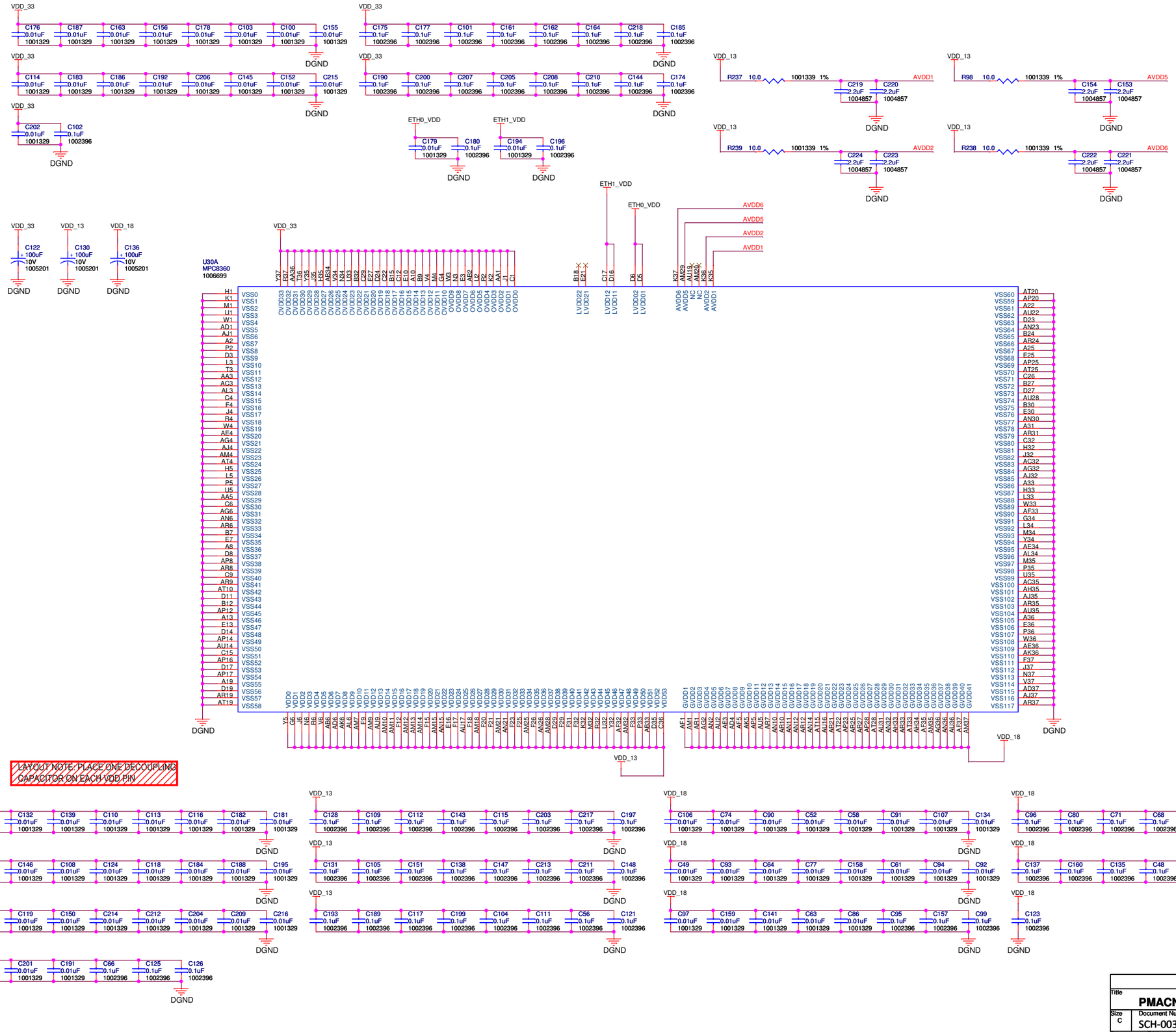
VDD_33
C176 0.01uF 1001329
C187 0.01uF 1001329
C163 0.01uF 1001329
C156 0.01uF 1001329
C178 0.01uF 1001329
C103 0.01uF 1001329
C100 0.01uF 1001329
C155 0.01uF 1001329
DGND
C175 0.1uF 1002396
C177 0.1uF 1002396
C101 0.1uF 1002396
C161 0.1uF 1002396
C162 0.1uF 1002396
C164 0.1uF 1002396
C218 0.1uF 1002396
C185 0.1uF 1002396
C114 0.01uF 1001329
C183 0.01uF 1001329
C186 0.01uF 1001329
C192 0.01uF 1001329
C206 0.01uF 1001329
C145 0.01uF 1001329
C152 0.01uF 1001329
C215 0.01uF 1001329
C190 0.1uF 1002396
C200 0.1uF 1002396
C207 0.1uF 1002396
C205 0.1uF 1002396
C208 0.1uF 1002396
C210 0.1uF 1002396
C144 0.1uF 1002396
C174 0.1uF 1002396
C202 0.01uF 1001329
C102 0.1uF 1002396
ETH0_VDD
C179 0.01uF 1001329
C180 0.1uF 1002396
ETH1_VDD
C194 0.01uF 1001329
C196 0.1uF 1002396
VDD_13
R237 10.0 1001339 1%
C219 2.2uF 1004857
C220 2.2uF 1004857
AVDD1
R98 10.0 1001339 1%
C154 2.2uF 1004857
C153 2.2uF 1004857
AVDD5
R239 10.0 1001339 1%
C224 2.2uF 1004857
C223 2.2uF 1004857
AVDD2
R238 10.0 1001339 1%
C222 2.2uF 1004857
C221 2.2uF 1004857
AVDD6
VDD_18
C122 100uF 10V 1005201
C130 100uF 10V 1005201
C136 100uF 10V 1005201
U30A
MPC8360
1006699
H1 VSS0
K1 VSS1
M1 VSS2
U1 VSS3
W1 VSS4
AD1 VSS5
AJ1 VSS6
A2 VSS7
P2 VSS8
D3 VSS9
L3 VSS10
T3 VSS11
AA3 VSS12
AC3 VSS13
AL3 VSS14
C4 VSS15
F4 VSS16
J4 VSS17
R4 VSS18
W4 VSS19
AE4 VSS20
AG4 VSS21
AJ4 VSS22
AM4 VSS23
AT4 VSS24
H5 VSS25
L5 VSS26
P5 VSS27
U5 VSS28
AA5 VSS29
C6 VSS30
AG6 VSS31
AN6 VSS32
AR6 VSS33
B7 VSS34
E7 VSS35
A8 VSS36
D8 VSS37
AP8 VSS38
AR8 VSS39
C9 VSS40
AR9 VSS41
AT10 VSS42
D11 VSS43
B12 VSS44
AP12 VSS45
A13 VSS46
E13 VSS47
D14 VSS48
AP14 VSS49
AU14 VSS50
C15 VSS51
AP16 VSS52
D17 VSS53
AP17 VSS54
A19 VSS55
D19 VSS56
AR19 VSS57
AT19 VSS58
V37 OVDD33
R37 OVDD32
AA36 OVDD31
T36 OVDD30
V35 OVDD29
H35 OVDD28
AB35 OVDD27
V34 OVDD26
N34 OVDD25
U33 OVDD24
B32 OVDD23
C29 OVDD22
E27 OVDD21
D24 OVDD20
C23 OVDD19
B15 OVDD18
C12 OVDD17
E10 OVDD16
A10 OVDD15
B9 OVDD14
V4 OVDD13
M4 OVDD12
W3 OVDD11
N3 OVDD10
E3 OVDD9
AB2 OVDD8
U2 OVDD7
P2 OVDD6
K2 OVDD5
AA1 OVDD4
J1 OVDD3
G1 OVDD2
OVDD1
OVDD0
B18 LVDD22
E21 LVDD21
C17 LVDD12
D16 LVDD11
D6 LVDD02
D5 LVDD01
K37 AVDD6
AM29 AVDD5
AU19 NC
AM25 NC
K35 NC
K35 AVDD2
AVDD1
VSS60 AT20
VSS59 AP20
VSS61 A22
VSS62 AU22
VSS63 D23
VSS64 AN23
VSS65 B24
VSS66 AR24
VSS67 A25
VSS68 E25
VSS69 AP25
VSS70 AT25
VSS71 G26
VSS72 B27
VSS73 D27
VSS74 AU28
VSS75 B30
VSS76 E30
VSS77 AN30
VSS78 A31
VSS79 AR31
VSS80 C32
VSS81 H32
VSS82 J32
VSS83 AC32
VSS84 AG32
VSS85 AJ32
VSS86 A33
VSS87 H33
VSS88 L33
VSS89 W33
VSS90 AF33
VSS91 G34
VSS92 L34
VSS93 M34
VSS94 Y34
VSS95 AE34
VSS96 AL34
VSS97 M35
VSS98 P35
VSS99 U35
VSS100 AC35
VSS101 AH35
VSS102 AJ35
VSS103 AR35
VSS104 AU35
VSS105 A36
VSS106 E36
VSS107 P36
VSS108 W36
VSS109 AE36
VSS110 AK36
VSS111 F37
VSS112 J37
VSS113 N37
VSS114 V37
VSS115 AD37
VSS116 AJ37
VSS117 AR37
VDD0 Y5
G6 VDD1
J6 VDD2
N6 VDD3
R6 VDD4
U6 VDD5
AB6 VDD6
AD6 VDD7
AK6 VDD8
AL6 VDD9
AM7 VDD10
F9 VDD11
AM9 VDD12
AM10 VDD13
AM11 VDD14
F12 VDD15
AM12 VDD16
AM13 VDD17
AM14 VDD18
F15 VDD19
AM15 VDD20
AM16 VDD21
F16 VDD22
AU17 VDD23
F17 VDD24
F18 VDD25
AM18 VDD26
F20 VDD27
P21 VDD28
AM21 VDD29
AM23 VDD30
F25 VDD31
AM25 VDD32
F26 VDD33
AM26 VDD34
AM28 VDD35
D29 VDD36
F29 VDD37
F31 VDD38
F32 VDD39
K32 VDD40
M32 VDD41
R32 VDD42
U32 VDD43
V32 VDD44
AF32 VDD45
AM32 VDD46
F33 VDD47
P33 VDD48
AB33 VDD49
D35 VDD50
C36 VDD51
VDD52
VDD53
AF1 GVDD1
AM1 GVDD2
AE1 GVDD3
AC1 GVDD4
AU2 GVDD5
AN2 GVDD6
AE3 GVDD7
AJ4 GVDD8
AE5 GVDD9
AK5 GVDD10
AU5 GVDD11
AT7 GVDD12
AN10 GVDD13
AB10 GVDD14
AN11 GVDD15
AN12 GVDD16
AN14 GVDD17
AT15 GVDD18
AU16 GVDD19
AT17 GVDD20
AT22 GVDD21
AF23 GVDD22
AT24 GVDD23
AB25 GVDD24
AF25 GVDD25
AP26 GVDD26
AT28 GVDD27
AU29 GVDD28
AU31 GVDD29
AN32 GVDD30
AK32 GVDD31
AB33 GVDD32
AT33 GVDD33
AH34 GVDD34
AC35 GVDD35
AG36 GVDD36
AK36 GVDD37
AN36 GVDD38
AU38 GVDD39
AJ37 GVDD40
AM37 GVDD41
LAYOUT NOTE: PLACE ONE DECOUPLING CAPACITOR ON EACH VDD PIN
C127 0.01uF 1001329
C132 0.01uF 1001329
C139 0.01uF 1001329
C110 0.01uF 1001329
C113 0.01uF 1001329
C116 0.01uF 1001329
C182 0.01uF 1001329
C181 0.01uF 1001329
C128 0.1uF 1002396
C109 0.1uF 1002396
C112 0.1uF 1002396
C143 0.1uF 1002396
C115 0.1uF 1002396
C203 0.1uF 1002396
C217 0.1uF 1002396
C197 0.1uF 1002396
C106 0.01uF 1001329
C74 0.01uF 1001329
C90 0.01uF 1001329
C52 0.01uF 1001329
C58 0.01uF 1001329
C91 0.01uF 1001329
C107 0.01uF 1001329
C134 0.01uF 1001329
C96 0.1uF 1002396
C80 0.1uF 1002396
C71 0.1uF 1002396
C68 0.1uF 1002396
C98 0.1uF 1002396
C133 0.1uF 1002396
C53 0.1uF 1002396
C50 0.1uF 1002396
C142 0.01uF 1001329
C146 0.01uF 1001329
C108 0.01uF 1001329
C124 0.01uF 1001329
C118 0.01uF 1001329
C184 0.01uF 1001329
C188 0.01uF 1001329
C195 0.01uF 1001329
C131 0.1uF 1002396
C105 0.1uF 1002396
C151 0.1uF 1002396
C138 0.1uF 1002396
C147 0.1uF 1002396
C213 0.1uF 1002396
C211 0.1uF 1002396
C148 0.1uF 1002396
C49 0.01uF 1001329
C93 0.01uF 1001329
C64 0.01uF 1001329
C77 0.01uF 1001329
C158 0.01uF 1001329
C61 0.01uF 1001329
C94 0.01uF 1001329
C92 0.01uF 1001329
C137 0.1uF 1002396
C160 0.1uF 1002396
C135 0.1uF 1002396
C48 0.1uF 1002396
C60 0.1uF 1002396
C140 0.1uF 1002396
C62 0.1uF 1002396
C120 0.1uF 1002396
C149 0.01uF 1001329
C119 0.01uF 1001329
C150 0.01uF 1001329
C214 0.01uF 1001329
C212 0.01uF 1001329
C204 0.01uF 1001329
C209 0.01uF 1001329
C216 0.01uF 1001329
C193 0.1uF 1002396
C189 0.1uF 1002396
C117 0.1uF 1002396
C199 0.1uF 1002396
C104 0.1uF 1002396
C111 0.1uF 1002396
C56 0.1uF 1002396
C121 0.1uF 1002396
C97 0.01uF 1001329
C159 0.01uF 1001329
C141 0.01uF 1001329
C63 0.01uF 1001329
C86 0.01uF 1001329
C95 0.1uF 1002396
C157 0.1uF 1002396
C99 0.01uF 1002396
C123 0.1uF 1002396
C198 0.01uF 1001329
C201 0.01uF 1001329
C191 0.01uF 1001329
C66 0.1uF 1002396
C125 0.1uF 1002396
C126 0.1uF 1002396
DGND
Title
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U30G
MPC8360
1006699

PCI_AD[31..0]

PG31/UPC2_RxEN_B[2]/PCI_AD31 D20 PCI_AD31
PG30/UPC2_TxEN_B[1]/PCI_AD30 D21 PCI_AD30
PG29/UPC2_TxDATA[6]/PCI_AD29 A24 PCI_AD29
PG28/UPC2_TxDATA[7]/PCI_AD28 B23 PCI_AD28
PG27/UPC2_TxDATA[8]/PCI_AD27 C23 PCI_AD27
PG26/UPC2_TxDATA[9]/PCI_AD26 E23 PCI_AD26
PG25/UPC2_TxDATA[10]/PCI_AD25 A26 PCI_AD25
PG24/UPC2_RxCLAV[2]/PCI_AD24 B21 PCI_AD24
PG23/UPC2_TxDATA[12]/PCI_AD23 C24 PCI_AD23
PG22/UPC2_TxDATA[13]/PCI_AD22 C25 PCI_AD22
PG21/UPC2_TxDATA[14]/PCI_AD21 D25 PCI_AD21
PG20/UPC2_TxDATA[15]/PCI_AD20 B25 PCI_AD20
PG19/UPC2_M_TxCLAV[0]/PCI_AD19 E24 PCI_AD19
PG18/UPC2_M_TxEN_B[0]/PCI_AD18 F24 PCI_AD18
PG17/UPC2_TxSOC/PCI_AD17 A27 PCI_AD17
PG16/UPC2_TxPRTY/PCI_AD16 A28 PCI_AD16
PG15/UPC2_RxPRTY/PCI_AD15 F27 PCI_AD15
PG14/UPC2_TxDATA[4]/PCI_AD14 A30 PCI_AD14
PG13/UPC2_TxCLAV[1]/PCI_AD13 C30 PCI_AD13
PG12/UPC2_TxCLAV[2]/PCI_AD12 D30 PCI_AD12
PG11/UPC2_RxCLAV[1]/PCI_AD11 E29 PCI_AD11
PG10/UPC2_TxDATA[5]/PCI_AD10 B31 PCI_AD10
PG9/UPC2_TxDATA[11]/PCI_AD9 C31 PCI_AD9
PG8/UPC2_RxDATA[2]/PCI_AD8 D31 PCI_AD8
PG7/UPC2_M_TxADDR[4]/PCI_AD7 D32 PCI_AD7
PG6/UPC2_RxDATA[7]/PCI_AD6 A32 PCI_AD6
PG5/UPC2_M_TxADDR[2]/PCI_AD5 C33 PCI_AD5
PG4/UPC2_M_TxADDR[1]/PCI_AD4 B33 PCI_AD4
PG3/UPC2_M_TxADDR[0]/PCI_AD3 F30 PCI_AD3
PG2/UPC2_RxDATA[3]/PCI_AD2 E31 PCI_AD2
PG1/UPC2_RxDATA[4]/PCI_AD1 A34 PCI_AD1
PG0/UPC2_RxDATA[8]/PCI_AD0 D33 PCI_AD0
PF17/UPC2_RxDATA[12]/PCI_IDSEL F22 R245 0.0 1001368 1% R142 0.0 NL 1% PCI_AD24

PF10/UPC2_TxDATA[0]/PCI_C_BE3 E22 PCI_C/nBE3
PF9/UPC2_TxDATA[1]/PCI_C_BE2 B26 PCI_C/nBE2
PF8/UPC2_TxDATA[2]/PCI_C_BE1 E28 PCI_C/nBE1
PF7/UPC2_TxDATA[3]/PCI_C_BE0 F28 PCI_C/nBE0

PF25/UPC2_RxEN_B[1]/PCI_GNT[2] C20 PCI_nGNT2
PF24/UPC2_M_RxADDR[4]/PCI_GNT[1] B20 PCI_nGNT1
PF23/UPC2_M_RxADDR[3]/PCI_GNT[0] E20 PCI_nGNT0

PF22/UPC2_M_TxADDR[3]/PCI_REQ[2] C21 PCI_nREQ2
PF21/UPC2_M_RxADDR[2]/PCI_REQ[1] A21 PCI_nREQ1
PF20/UPC2_TxEN_B[2]/PCI_REQ[0] F19 PCI_nREQ0

PF12/UPC2_M_RxEN_B[0]/PCI_FRAME D26 PCI_nFRAME
PF16/UPC2_RxDATA[13]/PCI_DEVSEL E26 PCI_nDEVSEL
PF14/UPC2_RxDATA[15]/PCI_IRDY C28 PCI_nIRDY
PF13/UPC2_M_RxCLAV[0]/PCI_TRDY C27 PCI_nTRDY
PF19/UPC2_RxDATA[10]/PCI_PERR A29 PCI_nPERR
PF18/UPC2_RxDATA[11]/PCI_SERR B29 PCI_nSERR
PF11/UPC2_RxSOC/PCI_PAR D28 PCI_PAR
PF15/UPC2_RxDATA[14]/PCI_STOP B28 PCI_nSTOP
PF5/UPC2_M_RxADDR[0]/INTA A20 R153 0.0 NL PCI_nIRQA <8>

PF6/UPC2_M_RxADDR[1]/PCI_RSTO E19 R137 0.0 1001368 1% PCI_nRESET

VDD_33
R154 10.0K 1% 1001336
R253 10.0K 1% NL

DESIGN NOTE: NP for PCI device operation

PF28/UPC2_RxCLAV[3]/PCI_CLK[2] A23
PF27/UPC2_TxEN_B[3]/PCI_CLK[1] D22
CE_PF26/PCI_CLK0 B22 R143 22.1 1001374 PCI_CLK
PCI_MODE D36 PCI_MODE

PF29/UPC2_TxCLAV[3]/PCI_SYNC_OUT D37 R149 22.1 1001374

PCI_SYNC_IN M36

PF4/UPC2_RxDATA[6]/PCI_M66EN B37 PCI_M66EN

LAYOUT NOTE: PCI_SYNC MUST BE ROUTED EQUIVALENT TO PCI_CLK. EXTRA TRACE SHOULD BE ROUTED TO ACCOUNT FOR BASEBOARD TRACE LENGTH.

PCI_AD0 96 AD[00]
PCI_AD1 99 AD[01]
PCI_AD2 94 AD[02]
PCI_AD3 95 AD[03]
PCI_AD4 92 AD[04]
PCI_AD5 91 AD[05]
PCI_AD6 90 AD[06]
PCI_AD7 87 AD[07]
PCI_AD8 85 AD[08]
PCI_AD9 84 AD[09]
PCI_AD10 81 AD[10]
PCI_AD11 80 AD[11]
PCI_AD12 79 AD[12]
PCI_AD13 78 AD[13]
PCI_AD14 75 AD[14]
PCI_AD15 76 AD[15]
PCI_AD16 60 AD[16]
PCI_AD17 57 AD[17]
PCI_AD18 58 AD[18]
PCI_AD19 53 AD[19]
PCI_AD20 54 AD[20]
PCI_AD21 51 AD[21]
PCI_AD22 52 AD[22]
PCI_AD23 47 AD[23]
PCI_AD24 46 AD[24]
PCI_AD25 41 AD[25]
PCI_AD26 44 AD[26]
PCI_AD27 39 AD[27]
PCI_AD28 42 AD[28]
PCI_AD29 35 AD[29]
PCI_AD30 38 AD[30]
PCI_AD31 33 AD[31]

PCI_C/nBE3 45 C/BE[3]#
PCI_C/nBE2 59 C/BE[2]#
PCI_C/nBE1 73 C/BE[1]#
PCI_C/nBE0 86 C/BE[0]#

PCI_PAR 56 PAR
PCI_nFRAME 64 FRAME#
PCI_nTRDY 66 TRDY#
PCI_nIRDY 61 IRDY#
PCI_nSTOP 68 STOP#
PCI_nDEVSEL 72 DEVSEL#
PCI_nPERR 71 PERR#
PCI_nSERR 67 SERR#
PCI_M66EN 104 M66EN
PCI_AD20 R251 33.2 1003119 48 IDSEL

PCI_nREQ0 29 REQ#
PCI_nGNT0 30 GNT#

<8> PCI_nIRQA 20 INTA#
<8> PCI_nIRQB 17 INTB#
PCI_CLK 25 CLK
PCI_nRESET 26 RST#

C300 10pF NL

121 RSVD
22 RSVD_3
36 RSVD_4
43 RSVD_5
93 RSVD_6
112 RSVD_7
21 RSVD_2
16 RSVD_1

J16
6318228-1
1006898
124

MPCIACT# 122 R288 10.0K 1% 1001336 VDD_33
CLKRUN# 65
PME# 34

AC_SYNC 103 R291 10.0K 1% 1001336
AC_SDATA_IN 105 R292 10.0K 1% 1001336
AC_BIT_CLK 107 R290 10.0K 1% 1001336 VDD_33
AC_CODEC_ID0# 108 R293 10.0K 1% 1001336 VDD_33
AC_CODEC_ID1# 109 R286 10.0K 1% 1001336
AC_SDATA_OUT 106 R287 10.0K 1% 1001336
AC_RESET# 110

MOD_AUDIO_MON 111
SYS_AUDIO_IN 116
SYS_AUDIO_OUT 115
SYS_AUDIO_IN_GND 118
SYS_AUDIO_OUT_GND 117
AUDIO_GND 113
AUDIO_GND 120
AUDIO_GND 119

8PMJ-1 4
8PMJ-2 6
8PMJ-3 3
8PMJ-4 8
8PMJ-5 10
8PMJ-6 5
8PMJ-7 7
8PMJ-8 9

TIP 1
RING 2

LED2_YELP 12
LED2_YELN 14
LED1_GRNP 11
LED1_GRNN 13

RSVD_WIP_1 100 R294 0.0 NL
RSVD_WIP_2 98 VCC_5
VCC5VA 123
5V 18
5V 97

3.3V 19
3.3V 28
3.3V 31
3.3V 63
3.3V 40
3.3V 70
3.3V 88
3.3V 89
VDD_33
R252 0.0 NL
3.3VAUX 124
3.3VAUX 24

GND 23
GND 27
GND 32
GND 37
GND 49
GND 50
GND 55
GND 62
GND 69
GND 74
GND 77
GND 82
GND 83
GND 101
GND 102
GND 114

CHSGND 15

DGND
CHASSIS

LAYOUT NOTE: PLACE DECOUPLING CAPACITORS NEAR POWER PINS ON J9

VDD_33
C297 0.1uF 1003323
C298 0.1uF 1003323
C318 0.1uF 1003323
C295 0.1uF 1003323
C319 0.1uF 1003323
C299 0.1uF 1003323
DGND

VCC_5
C320 0.1uF 1003323
C296 0.1uF 1003323
DGND

VDD_33
C225 100uF 16V 1002485
DGND

VCC_5
C280 100uF 16V 1002485
DGND

3.3V MiniPCI Type IIIA 124 pin slot, 33 or 66 MHz (50.95mm length)

VDD_33
R289 8250 1% 1006854 PCI_M66EN
R254 8250 1% 1006854 PCI_nFRAME
R250 8250 1% 1006854 PCI_nTRDY
R262 8250 1% 1006854 PCI_nIRDY
R256 8250 1% 1006854 PCI_nDEVSEL
R255 8250 1% 1006854 PCI_nSTOP
R258 8250 1% 1006854 PCI_nSERR
R259 8250 1% 1006854 PCI_nPERR
R285 8250 1% 1006854 PCI_C/nBE0
R263 8250 1% 1006854 PCI_C/nBE1
R257 8250 1% 1006854 PCI_C/nBE2
R261 8250 1% 1006854 PCI_C/nBE3

VDD_33
R260 8250 1% 1006854 PCI_nREQ0
R138 8250 1% 1006854 PCI_nREQ1
R141 8250 1% 1006854 PCI_nREQ2
R249 8250 1% NL PCI_nGNT0
R246 8250 1% NL PCI_nGNT1
R247 8250 1% NL PCI_nGNT2

VDD_33
R240 10.0K 1% 1001336
PCI_MODE
R146 0.0 1% NL
DGND

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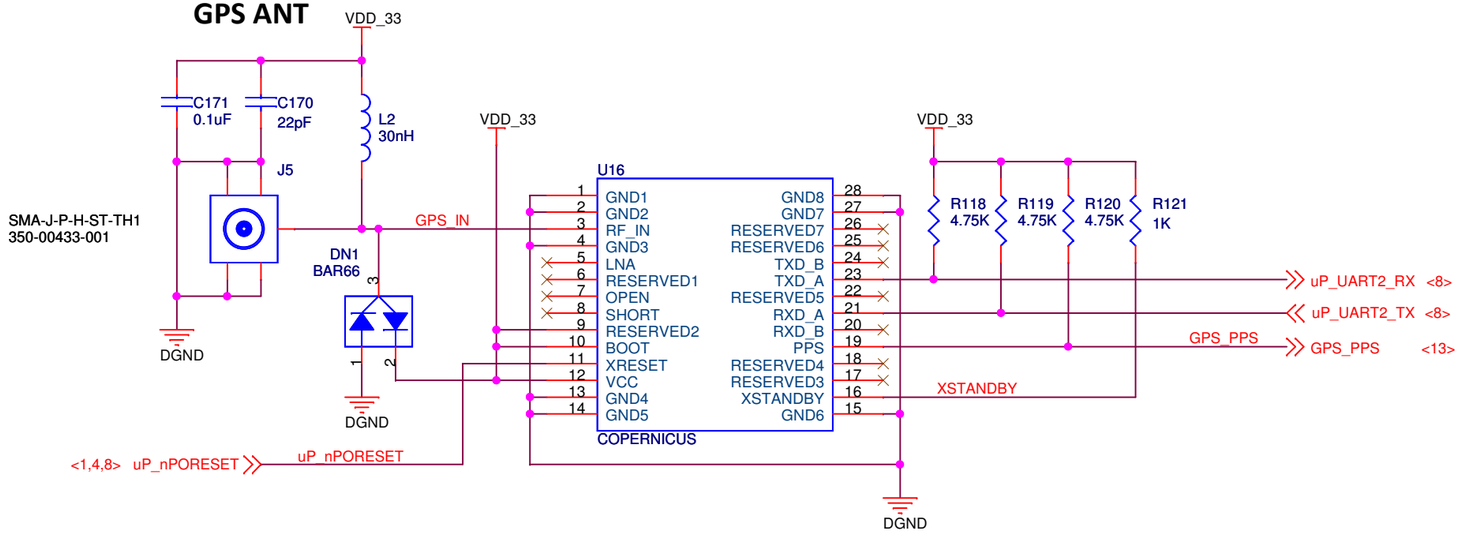
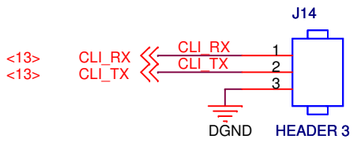
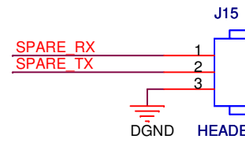
GPS ANT

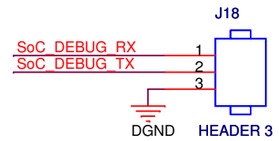




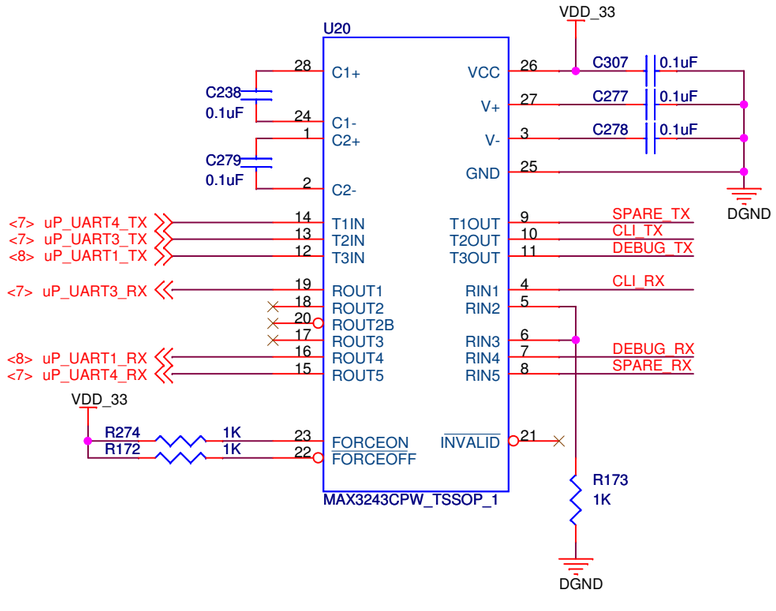
SoC CLI to MPC8360

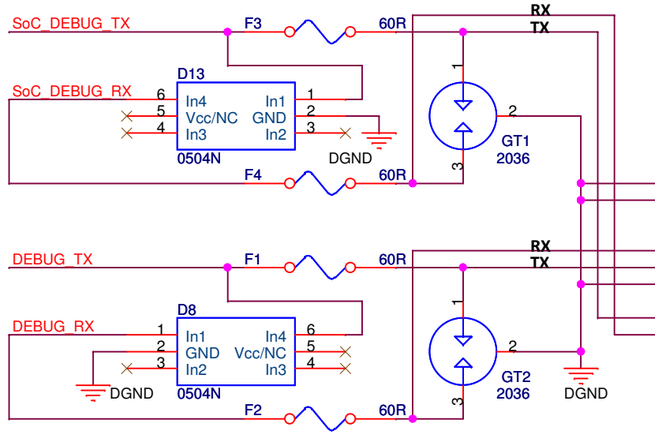


SPARE RS-232

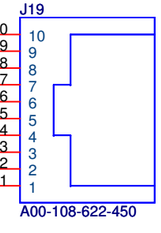


SoC CLI to Debug Port





RS-232 EIA/TIA-561 RJ45 Pinout



Combined CLI Debug Port

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GIGABIT ETHERNET

LAYOUT NOTE: ENETnx+/- ARE DIFFERENTIAL PAIRS THAT SHOULD BE ROUTED WITH 100 OHMS DIFFERENTIAL IMPEDENCE

ENET1_CT

J20
JXK0-0185NL

<5> ENET1_TRD0+ — 11 MD1+
12 CT1
<5> ENET1_TRD0- — 10 MD1-
<5> ENET1_TRD1+ — 4 MD2+
6 CT2
<5> ENET1_TRD1- — 5 MD2-
<5> ENET1_TRD2+ — 3 MD3+
1 CT3
<5> ENET1_TRD2- — 2 MD3-
<5> ENET1_TRD3+ — 8 MD4+
7 CT4
<5> ENET1_TRD3- — 9 MD4-
13 EGND1
14 EGND2
HOLE1 15
HOLE2 16

A+ 1
A- 2
B+ 3
C+ 4
C- 5
B- 6
D+ 7
D- 8

CHASSIS

ENET2_CT

J21
JXK0-0185NL

<5> ENET2_TRD0+ — 11 MD1+
12 CT1
<5> ENET2_TRD0- — 10 MD1-
<5> ENET2_TRD1+ — 4 MD2+
6 CT2
<5> ENET2_TRD1- — 5 MD2-
<5> ENET2_TRD2+ — 3 MD3+
1 CT3
<5> ENET2_TRD2- — 2 MD3-
<5> ENET2_TRD3+ — 8 MD4+
7 CT4
<5> ENET2_TRD3- — 9 MD4-
13 EGND1
14 EGND2
HOLE1 15
HOLE2 16

A+ 1
A- 2
B+ 3
C+ 4
C- 5
B- 6
D+ 7
D- 8

CHASSIS

VDD_33

<5> ENET1_LED3 — R195 332 — 1003283 — D14 LED — Green / ACT
<5> ENET1_LED1 — R197 332 — 1003283 — D16 LED — Yellow / ANEN
<5> ENET1_LED2 — R196 332 — 1003283 — D15 LED — Yellow / FDX

VDD_33

<5> ENET2_LED3 — R198 332 — 1003283 — D17 LED — Green / ACT
<5> ENET2_LED1 — R200 332 — 1003283 — D19 LED — Yellow / ANEN
<5> ENET2_LED2 — R199 332 — 1003283 — D18 LED — Yellow / FDX

VDD_33

J11
103186-1

GigE ACT Chassis LED

R112
332

Q7
N-CH
2N7002-7-F
1001604

R116
10.0K

DGND

VDD_33

J12
103186-1

Power OK Chassis LED

R113
332

DGND

10/100 ETHERNET

ENET3_CTREF

J17A
SI-30107-F
1006999

<7> ENET3_TD+ — T1 TX+
T2 CT
<7> ENET3_TD- — T3 TX-
<7> ENET3_RD+ — T4 RX+
T5 CT
<7> ENET3_RD- — T6 RX-
T7 NC
T8 GND

MT3 17
MT4 18
MT5 19
MT6 20
MT7 21

CHASSIS

CHASSIS

VDD_33

R156
0.0
1001368
ENET3_CTREF

R164
0.0
1001368
ENET4_CTREF

ENET4_CTREF

J17B
SI-30107-F
1006999

<7> ENET4_TD+ — B1 TX+
B2 CT
<7> ENET4_TD- — B3 TX-
<7> ENET4_RD+ — B4 RX+
B5 CT
<7> ENET4_RD- — B6 RX-
B7 NC
B8 GND

CHASSIS

C276
220pF

FB6
Ferrite
1002401

DGND

CHASSIS

VDD_33

<7> ENET3_nLINK — R193 332 — 1003283 — D12 LED — Green / Link
<7> ENET3_nACT — R192 332 — 1003283 — D11 LED — Green / ACT
<7> ENET4_nLINK — R191 332 — 1003283 — D10 LED — Green / Link
<7> ENET4_nACT — R190 332 — 1003283 — D9 LED — Green / ACT

VDD_33

R114
332

R115
332

R117
10.0K

J13
103186-1

Q6
N-CH
2N7002-7-F
1001604

GPIO_PD25 <7>

Q5
N-CH
2N7002-7-F
1001604

Q8
NC VCC
OUT IN
GND
SN74AHC1G04DBVR
1002413

DGND

Status Chassis LED

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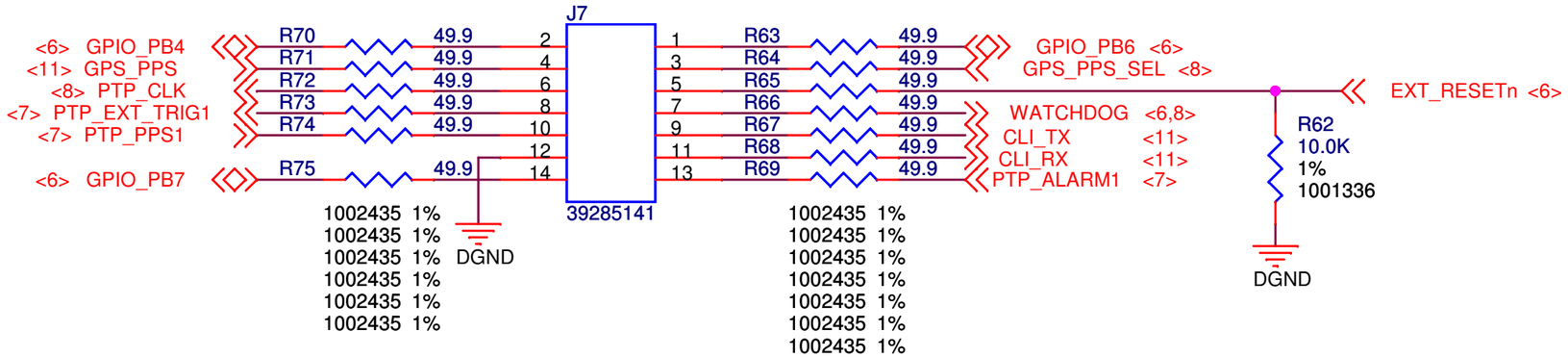
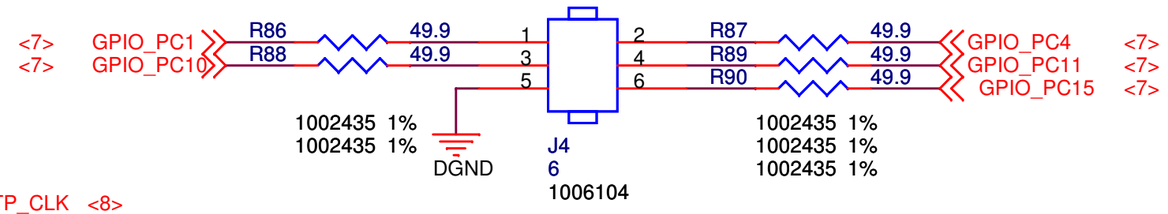
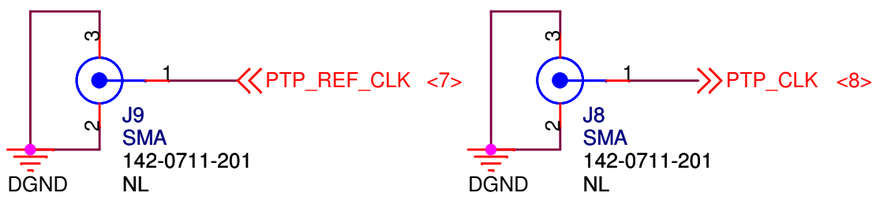
DAN <-> MPC



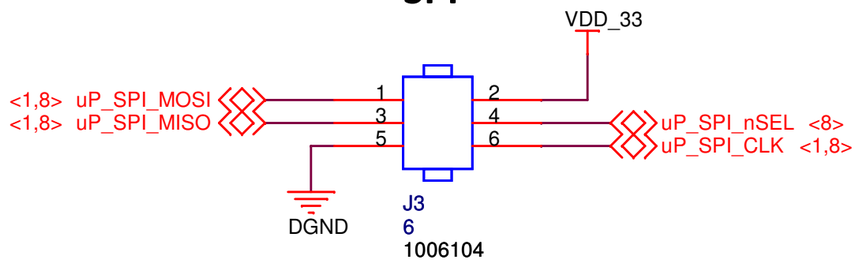
GPIO



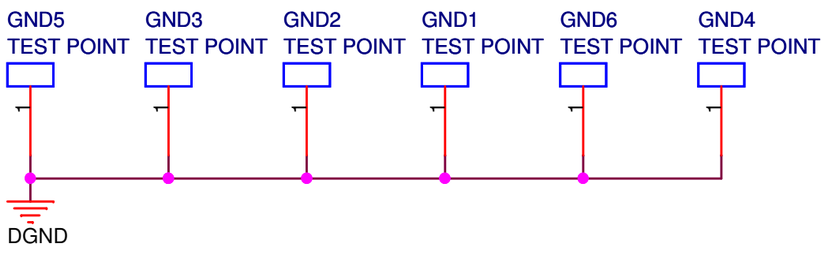
IEEE1588



SPI



GND



Title: **PMACNP - MISC CONNECTORS**		
Size: A	Document Number: SCH-00346-001	Rev: B
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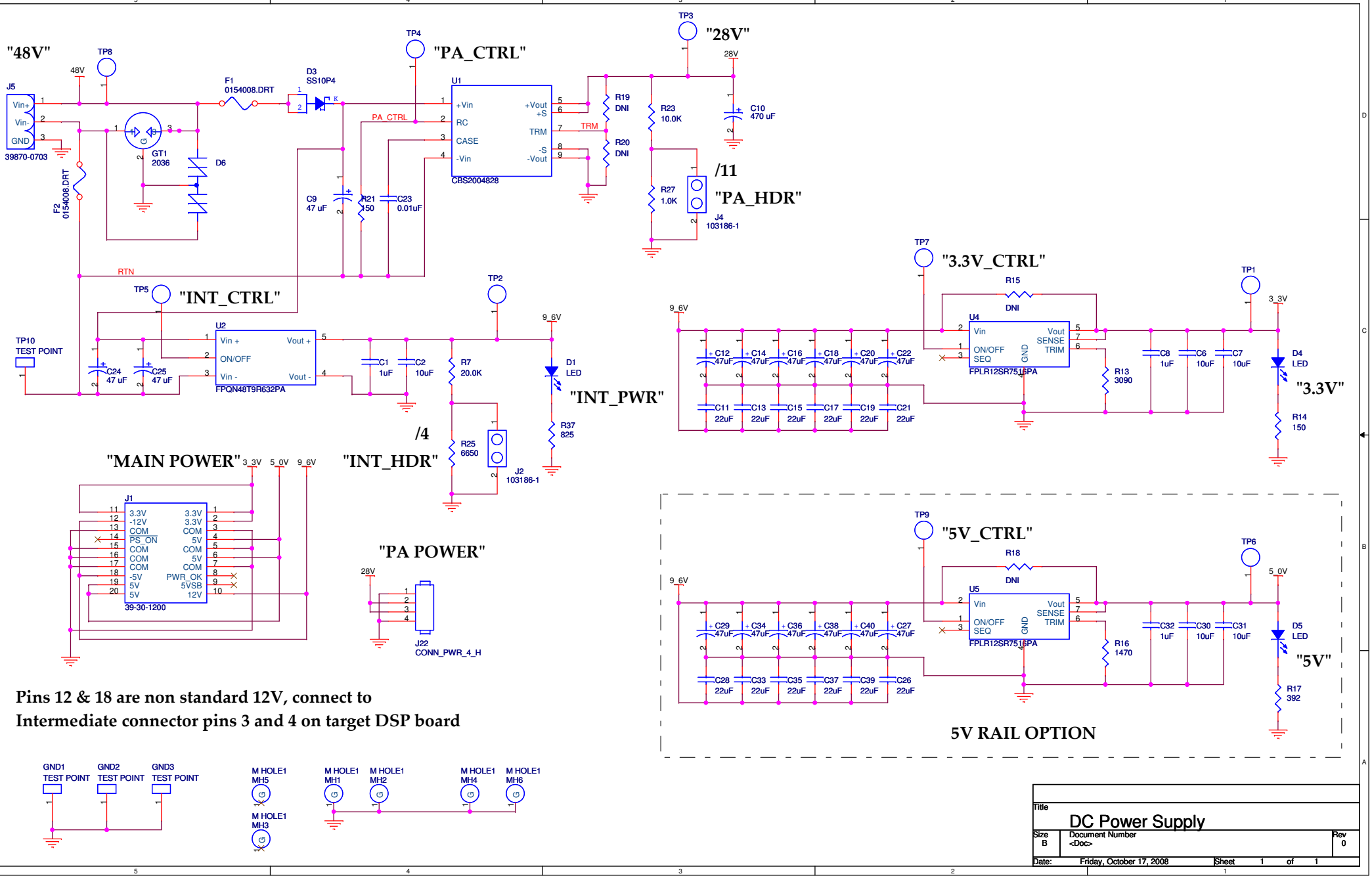

Title	DC Power Supply	
Size B	Document Number <Doc>	Rev 0
Date: Friday, October 17, 2008	Sheet 1 of 1	