SG885G-WF

Hardware Design

Smart Module Series

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-11-30	Clifton HE/Jalon PAN/ Rid WANG	Creation of the document
0.1	2023-11-30	Clifton HE/Jalon PAN/ Rid WANG	Draft

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1 Introduction

This document describes the SG885G-WF features, performance, and air interfaces and hardware interfaces connected to your applications. The document provides a quick insight into interface specifications, RF performance, electrical and mechanical specifications, and other module information, as well.

1.1. Special Marks

Table 1: Special Marks

Marks	Definitions
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, argument, and so on, it indicates that the function, feature, interface, pin, AT command, argument, and so on, is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

2 Product Overview

The module is a Smart LTE module based on Android operating system, and provides industrial-grade performance. It is an SMD module with compact packaging and it supports built-in high performance Adreno™ GPU 740 graphics processing unit, multiple audio and video codecs, and multiple audio and video input/output interfaces as well as abundant GPIO interfaces.

Table 2: Basic Information

SG885G-WF	
Packaging type	LGA
Pin counts	546
Dimensions	(51.0 ±0.2) mm × (49.0 ±0.2) mm × (4.25 ±0.2) mm
Weight	Approx. 18.6 g

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

	SG885G-WF
Wi-Fi 2.4 GHz	2412–2462 MHz
Wi-Fi 5 GHz	5180–5825 MHz
Wi-Fi 5.9 GHz & 6 GHz & 7 GHz	5850–7125 MHz
Bluetooth 5.3	2402–2480 MHz

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Application Processor	● 8-core Kryo™ CPU ● 1 × Kryo Prime Core, Fmax at 3.2 GHz ● ● 3 × Kryo Silver Core, Fmax at 2.0 GHz
Modem DSP	Hexagon™ DSP with 4 × Hexagon Vector eXtensions (HVX) and 1 × Hexagon Matrix eXtensions (HMX)
GPU	Adreno™ 740 GPU
Memory	● ● 8 GB LPDDR5X + 128 GB UFS4.0 (optional)
Operating System	Android 13 *
Supply Voltage	● 3.55–4.4 V ● Typ.: 3.8 V
USB Interface	● Complies with USB 2.0 and 3.1 Gen 2 specifications ● Data rate: up to 480 Mbps on USB2.0 and 10 Gbps on USB 3.1 Gen 2 ● USB OTG: – Master and slave modes: supported – Type-C: supported – USB Hub expansion: supported ● Use: AT command communication, data transmission, software debugging, firmware upgrade over USB ● DisplayPort v1.4 over Type-C with MST
SD Card Interface	● Complies with SD 3.0 protocol ● 1.8 V SD card ● SD card hot-plug
UART	● Up to 1 group of UART. – Debug UART: 2-wire UART, used for debugging
SPI	● Up to 4 groups of SPI ● Master mode only
I2C Interfaces	● Up to 12 groups of I2C interfaces: – 6 dedicated I2C interfaces, used for camera – 2 dedicated I2C interfaces, used for TP – 2 dedicated I2C interfaces, used for NFC and APPS – 2 generic I2C interfaces, used for sensor
I2S Interfaces	● Up to 2 groups of I2S interfaces: – 2 I2S interfaces are configured by default

Analog Audio Interfaces	● Digital M ● SWR
Audio Codec	GSM-FR, GSM-EFR, GSM-HR, AMR-NB, AMR-WB, EVS-NB, EVS-WB, EVS-SWB, MP3, AAC, AAC+, AMR and PCM
ADC Interfaces	● 2 generic ADC interfaces ● Resolution: up to 14-bit
LCM Interfaces	● 2 groups of 4-lane MIPI_DSI ● Data rate: up to 2.5 Gbps/lane ● Supports up to 5120 × 2880 @ 60 fps
Camera Interfaces	● 6 groups of 4-lane MIPI_CSI ● Data rate: up to 2.5 Gbps/lane
Video Codec	● Encoding: 4K @ 120 fps; 8K @ 30 fps ● Decoding: 4K @ 240 fps；8K @ 60 fps ● Native encode supports for H.265 Main 10, H.265 Main, H.264 high formats ● Native decode supports for H.265 Main 10, H.265 Main, H.264 High, and VP9 profile 2
RGMII Interface [1]	1 group of RGMII
SGMII&USXGMII Interfaces [1]	2 groups of SGMII&USXGMII
PCIe Interfaces [1]	● 3 groups of PCIe – PCIe 1：2-lane Gen 4 – PCIe 2：2-lane Gen 3 – PCIe 3：1-lane Gen 3
Antenna Interfaces	● Wi-Fi & Bluetooth antenna interfaces (ANT_WIFI/BT) ● 50 Ω characteristic impedance
WLAN Features	● Operating modes: AP and STA ● Operating frequency: 2.4 GHz, 5 GHz, 6 GHz and 7 GHz ● ●
Bluetooth Features	● *Bluetooth Core Specification Version 5.3* ● Bluetooth Classic & Bluetooth Low Energy (BLE)
Real Time Clock	The module supports RTC function
Temperature Ranges	● Normal operating temperature [2]: -30 to +75 °C ● Storage temperature: -40 to +90 °C
Firmware Upgrade	● USB 2.0 interface ● DFOTA
RoHS	All hardware components are fully Complies with EU RoHS directive

[1] PCIe 2, PCIe 3, and Ethernet functions cannot be used simultaneously with PCIe 1.
[2] Within this range, the module's indicators comply with 3GPP specification requirements.

2.3. Functional Diagram

The functional diagram illustrates the following major functional parts:

- Power management
- Baseband part
- LPDDR5X + UFS flash
- Radio frequency part
- Peripheral interfaces

Figure 1: Functional Diagram

2.4. Pin Assignment

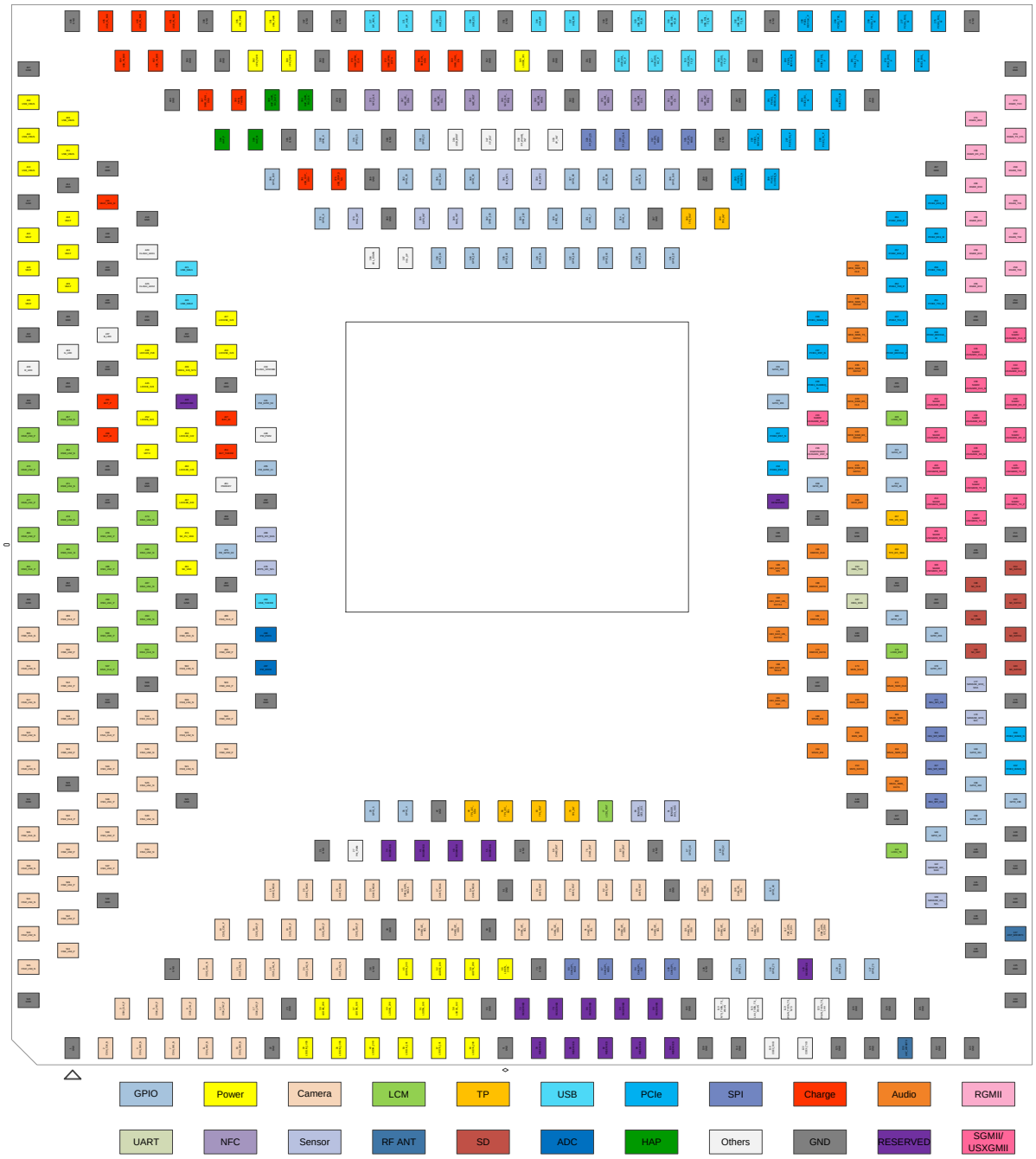


Figure 2: Pins Assignment (Top View)

NOTE

Keep all RESERVED pins and unused pins unconnected.

2.5. Pin Description

Table 5: Parameters Definition

Parameters	Descriptions
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output

DC characteristics include power domain and rated current in the table below.

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	418, 422, 423, 428, 429, 435	PIO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It must be provided with sufficient current up to 6.0 A.
LDO1B_1V8	445	PO	1.8 V output power for sensor	Vnom = 1.8 V	It is recommended to use a TVS to increase voltage surge withstand capability.

LDO2B_3V0	452	PO	3.0 V output power for sensor	Vnom = 3.0 V $I_O$max = 100 mA	Add a 1.0–4.7 μF bypass capacitor if used.
LDO5B_3V1	345	PO	3.1 V output power for USB DisplayPort's pull-up circuits	Vnom = 3.1 V $I_O$max = 150 mA	If unused, keep this pin unconnected.
LDO11B_1V2	453	PO	1.2 V output power	Vnom = 1.2 V $I_O$max = 400 mA	Add a 2.2 μF bypass capacitor if used.
LDO12B_1V8	460	PO	1.8 V output power for LCD and TP VDDIO	Vnom = 1.8 V	If unused, keep this pin unconnected.
LDO13B_3V0	467	PO	3.0 V output power for LCD	Vnom = 3.0 V $I_O$max = 150 mA	Reserve a 1.0 μF bypass capacitor if used.
LDO14B_2V8	438	PO	2.8 V output power for TP VDD	Vnom = 2.8 V	If unused, keep this pin unconnected.
LDO15B_1V8	427, 433	PO	1.8 V output power for I/O's pull-up circuits and level-shifting circuit	Vnom = 1.8 V $I_O$max = 20 mA	Add a 1.0–4.7 μF bypass capacitor if used.
LDO2G_1V2	58	PO	1.2 V output	Vnom = 1.2 V	If unused, keep this pin unconnected.
VREG_1V8_SYS	439	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 20 mA	
VPH_PWR	388, 391, 392, 395	PO	Power supply for peripherals	Vnom = VBAT	
VRTC*	459	PIO	Power supply for RTC	Vmin = 2.5 V Vnom = 3.0 V Vmax = 3.25 V	
GND	1, 6, 21, 22, 23, 38, 39, 42, 60, 61, 62, 65, 71, 73, 90, 96, 105, 106, 109, 114, 125, 126, 128, 129, 131, 132, 133, 134, 135, 136, 138, 140, 141, 144, 145, 147, 148, 149, 167, 176, 180, 192, 193, 196, 201, 202, 205, 211, 235, 240, 250, 254, 267, 273, 274, 279, 295, 296, 297, 298, 299, 307, 330, 331, 332, 338, 351, 352,				

	363, 368, 369, 379, 382, 383, 385, 387, 396, 398, 399, 400, 406, 407, 412, 414, 416, 417, 419, 424, 430, 431, 432, 436, 440, 442, 444, 450, 456, 462, 465, 466, 468, 472, 482, 488, 492, 498, 504, 508, 513, 526, 528, 531, 540, 546				
RGB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
R_LED	449	AO	Current source for red LED		
G_LED	443	AO	Current source for green LED		
B_LED	437	AO	Current source for blue LED		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	408, 409, 410, 411, 413	PIO	Charging power input; Power supply for OTG device; USB/adaptor insertion detection	$V_I$max = 21.5 V Vmin = 3.7 V Vnom = 5.0 V $I_I$max = 5 A $I_O$max = 3 A	
USB_DP	344	AIO	USB 2.0 differential data (+)		90 Ω differential impedance; USB 2.0 standard compliant
USB_DM	337	AIO	USB 2.0 differential data (-)		
USB_SS0_RX_P	317	AI	USB 3.1 channel 0 SuperSpeed receive (+)		
USB_SS0_RX_M	316	AI	USB 3.1 channel 0 SuperSpeed receive (-)		
USB_SS0_TX_P	303	AO	USB 3.1 channel 0 SuperSpeed transmit (+)		90 Ω differential impedance; USB 3.1 Gen 2 standard compliant
USB_SS0_TX_M	302	AO	USB 3.1 channel 0 SuperSpeed transmit (-)		
USB_SS1_RX_P	324	AI	USB 3.1 channel 1 SuperSpeed receive (+)		
USB_SS1_RX_M	323	AI	USB 3.1 channel 1 SuperSpeed receive		

			(-)		
USB_SS1_TX_M	309	AO	USB 3.1 channel 1 SuperSpeed transmit (-)		
USB_SS1_TX_P	310	AO	USB 3.1 channel 1 SuperSpeed transmit (+)		
USB_CC1	358	AI	USB Type-C configuration channel 1		
USB_CC2	365	AI	USB Type-C configuration channel 2		
USB_THERM	483	AI	USB temperature detect		
DP_AUX_P	371	AIO	DisplayPort auxiliary channel (+)		
DP_AUX_N	377	AIO	DisplayPort auxiliary channel (-)		
USB_SBU1	421	DI	USB Type-C side band use 1		
USB_SBU2	426	DI	USB Type-C side band use 2		
Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WSA0_EN	160	DO	WSA0 enable	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
WSA1_EN	154	DO	WSA1 enable		
WSA0_SWR_CLK	172	DO	WSA0 SoundWire clock		
WSA1_SWR_CLK	158	DO	WSA1 SoundWire clock		
WSA0_SWR_DATA	165	DIO	WSA0 SoundWire data		
WSA1_SWR_DATA	152	DIO	WSA1 SoundWire data		
WCD_RST	208	DO	WCD reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
WCD_SWR_TX_CLK	253	DO	WCD SoundWire transmit clock		
WCD_SWR_TX_DATA0	248	DIO	WCD SoundWire transmit data 0		

WCD_SWR_TX_DATA1	242	DIO	WCD SoundWire transmit data 1		
WCD_SWR_TX_DATA2	236	DIO	WCD SoundWire transmit data 2		
WCD_SWR_RX_CLK	229	DO	WCD SoundWire receive clock		
WCD_SWR_RX_DATA0	222	DIO	WCD SoundWire receive data 0		
WCD_SWR_RX_DATA1	215	DIO	WCD SoundWire receive data 1		
DMIC23_CLK	181	DO	Digital microphone 23 clock		
DMIC23_DATA	174	DI	Digital microphone 23 data	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
DMIC01_CLK	195	DO	Digital microphone 01 clock		
DMIC01_DATA	188	DI	Digital microphone 01 data		
I2S Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
HIFI_DAC_I2S_DATA0	175	DIO	HIFI DAC I2S data channel 0		
HIFI_DAC_I2S_DATA1	182	DIO	HIFI DAC I2S data channel 1		
HIFI_DAC_I2S_MCLK	168	DO	HIFI DAC I2S master clock		
HIFI_DAC_I2S_CLK	161	DO	HIFI DAC I2S clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
HIFI_DAC_I2S_WS	189	DO	HIFI DAC I2S word select		
MI2S_DATA0	166	DIO	I2S data channel 0		
MI2S_DATA1	153	DIO	I2S data channel 1		
MI2S_SCLK	173	DO	I2S bit clock		
MI2S_WS	159	DO	I2S word select		
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	198	DO	SD card clock	V_{OL}max = 0.225 V V_{OH}min = 1.53 V	

SD_CMD	191	DIO	SD card command	V_{OL}max = 0.225 V V_{OH}min = 1.53 V V_{IL}max = 0.63 V V_{IH}min = 1.125 V	
SD_DATA0	183	DIO	SDIO data bit 0		
SD_DATA1	190	DIO	SDIO data bit 1		
SD_DATA2	197	DIO	SDIO data bit 2		
SD_DATA3	204	DIO	SDIO data bit 3		
SD_DET	184	DI	SD card hot-plug detect	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	
SD_VDD	481	PO	SD card power supply	Vnom = 1.8 V	Add a 1.0–4.7 μF bypass capacitor if used. If unused, keep this pin open
SD_PU_VDD	474	PO	1.8 V output power for SD card pull-up circuits	Vnom = 1.8 V	Reserve a 1.0–2.2 μF bypass capacitor if used. If unused, keep this pin open
PCIe Interfaces [3]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE1_REFCLK_P	289	AO	PCIe1 reference clock (+)		100 Ω differential impedance.
PCIE1_REFCLK_M	290	AO	PCIe1 reference clock (-)		
PCIE1_TX0_P	285	AO	PCIe1 transmit 0 (+)		
PCIE1_TX0_M	284	AO	PCIe1 transmit 0 (-)		
PCIE1_RX0_P	278	AI	PCIe1 receive 0 (+)		
PCIE1_RX0_M	277	AI	PCIe1 receive 0 (-)		
PCIE1_TX1_P	281	AO	PCIe1 transmit 1 (+)		
PCIE1_TX1_M	280	AO	PCIe1 transmit 1 (-)		
PCIE1_RX1_P	276	AI	PCIe1 receive 1 (+)		

[3] PCIe 2, PCIe 3, and Ethernet functions cannot be used simultaneously with PCIe 1.

PCIE1_RX1_M	275	AI	PCIe1 receive 1 (-)		
PCIE1_WAKE_N	243	DI	PCIe1 wake up	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
PCIE1_RST_N	237	DO	PCIe1 reset		
PCIE1_CLKREQ_N	230	DI	PCIe1 clock request		
PCIE2_REFCLK_P	241	AO	PCIe2 reference clock (+)		100 Ω differential impedance.
PCIE2_REFCLK_M	246	AO	PCIe2 reference clock (-)		
PCIE2_TX0_P	252	AO	PCIe2 transmit 0 (+)		
PCIE2_TX0_M	256	AO	PCIe2 transmit 0 (-)		
PCIE2_RX0_P	261	AI	PCIe2 receive 0 (+)		
PCIE2_RX0_M	264	AI	PCIe2 receive 0 (-)		
PCIE2_TX1_P	247	AO	PCIe2 transmit 1 (+)		
PCIE2_TX1_M	251	AO	PCIe2 transmit 1 (-)		
PCIE2_RX1_P	257	AI	PCIe2 receive 1 (+)		
PCIE2_RX1_M	260	AI	PCIe2 receive 1 (-)		
PCIE2_WAKE_N	169	DI	PCIe2 wake up	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
PCIE2_RST_N	217	DO	PCIe2 reset		
PCIE2_CLKREQ_N	288	DI	PCIe2 clock request		
PCIE3_REFCLK_P	292	AO	PCIe3 reference clock (+)		100 Ω differential impedance
PCIE3_REFCLK_M	291	AO	PCIe3 reference clock (-)		
PCIE3_TX_P	283	AO	PCIe3 transmit (+)		
PCIE3_TX_M	282	AO	PCIe3 transmit (-)		
PCIE3_RX_P	287	AI	PCIe3 receive (+)		
PCIE3_RX_M	286	AI	PCIe3 receive (-)		
PCIE3_WAKE_N	169	DI	PCIe2 wake up	V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
PCIE3_RST_N	210	DO	PCIe3 reset		

PCIE3_CLKREQ_N	293	DI	PCIe3 clock request		
Touch Panel Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP0_RST	300	DO	TP0 reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
TP0_INT	294	DI	TP0 interrupt		
TP0_I2C_SDA	200	OD	TP0 I2C data		
TP0_I2C_SCL	207	OD	TP0 I2C clock		
TP1_RST	63	DO	TP1 reset		
TP1_INT	70	DI	TP1 interrupt		
TP1_I2C_SDA	49	OD	TP1 I2C data		
TP1_I2C_SCL	56	OD	TP1 I2C clock		
LCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD0_RST	179	DO	LCD0 reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
LCD0_TE	228	DI	LCD0 tearing effect		
DSI0_CLK_P	491	AO	LCD0 MIPI clock (+)		85 Ω differential impedance
DSI0_CLK_N	485	AO	LCD0 MIPI clock (-)		
DSI0_LN0_P	484	AO	LCD0 MIPI lane 0 data (+)		
DSI0_LN0_N	478	AO	LCD0 MIPI lane 0 data (-)		
DSI0_LN1_P	477	AO	LCD0 MIPI lane 1 data (+)		
DSI0_LN1_N	471	AO	LCD0 MIPI lane 1 data (-)		
DSI0_LN2_P	470	AO	LCD0 MIPI lane 2 data (+)		
DSI0_LN2_N	464	AO	LCD0 MIPI lane 2 data (-)		
DSI0_LN3_P	463	AO	LCD0 MIPI lane 3 data (+)		
DSI0_LN3_N	457	AO	LCD0 MIPI lane 3		

			data (-)		
LCD1_RST	77	DO	LCD1 reset	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
LCD1_TE	143	DI	LCD1 tearing effect		
DSI1_CLK_P	507	AO	LCD1 MIPI clock (+)		85 Ω differential impedance
DSI1_CLK_N	501	AO	LCD1 MIPI clock (-)		
DSI1_LN0_P	500	AO	LCD1 MIPI lane 0 data (+)		
DSI1_LN0_N	494	AO	LCD1 MIPI lane 0 data (-)		
DSI1_LN1_P	493	AO	LCD1 MIPI lane 1 data (+)		
DSI1_LN1_N	487	AO	LCD1 MIPI lane 1 data (-)		
DSI1_LN2_P	486	AO	LCD1 MIPI lane 2 data (+)		
DSI1_LN2_N	480	AO	LCD1 MIPI lane 2 data (-)		
DSI1_LN3_P	479	AO	LCD1 MIPI lane 3 data (+)		
DSI1_LN3_N	473	AO	LCD1 MIPI lane 3 data (-)		
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_P	499	AI	MIPI CSI0 clock (+)		85 Ω differential impedance
CSI0_CLK_N	505	AI	MIPI CSI0 clock (-)		
CSI0_LN0_P	506	AI	MIPI CSI0 lane 0 data (+)		
CSI0_LN0_N	511	AI	MIPI CSI0 lane 0 data (-)		
CSI0_LN1_P	512	AI	MIPI CSI0 lane 1 data (+)		
CSI0_LN1_N	517	AI	MIPI CSI0 lane 1 data (-)		
CSI0_LN2_P	518	AI	MIPI CSI0 lane 2 data (+)		
CSI0_LN2_N	522	AI	MIPI CSI0 lane 2 data (-)		

CSI0_LN3_P	523	AI	MIPI CSI0 lane 3 data (+)
CSI0_LN3_N	527	AI	MIPI CSI0 lane 3 data (-)
CSI1_CLK_P	519	AI	MIPI CSI1 clock (+)
CSI1_CLK_N	514	AI	MIPI CSI1 clock (-)
CSI1_LN0_P	524	AI	MIPI CSI1 lane 0 data (+)
CSI1_LN0_N	520	AI	MIPI CSI1 lane 0 data (-)
CSI1_LN1_P	529	AI	MIPI CSI1 lane 1 data (+)
CSI1_LN1_N	525	AI	MIPI CSI1 lane 1 data (-)
CSI1_LN2_P	533	AI	MIPI CSI1 lane 2 data (+)
CSI1_LN2_N	530	AI	MIPI CSI1 lane 2 data (-)
CSI1_LN3_P	537	AI	MIPI CSI1 lane 3 data (+)
CSI1_LN3_N	534	AI	MIPI CSI1 lane 3 data (-)
CSI2_CLK_P	532	AI	MIPI CSI2 clock (+)
CSI2_CLK_N	535	AI	MIPI CSI2 clock (-)
CSI2_LN0_P	536	AI	MIPI CSI2 lane 0 data (+)
CSI2_LN0_N	538	AI	MIPI CSI2 lane 0 data (-)
CSI2_LN1_P	539	AI	MIPI CSI2 lane 1 data (+)
CSI2_LN1_N	541	AI	MIPI CSI2 lane 1 data (-)
CSI2_LN2_P	542	AI	MIPI CSI2 lane 2 data (+)
CSI2_LN2_N	543	AI	MIPI CSI2 lane 2 data (-)
CSI2_LN3_P	544	AI	MIPI CSI2 lane 3 data (+)
CSI2_LN3_N	545	AI	MIPI CSI2 lane 3 data (-)

CSI3_CLK_P	489	AI	MIPI CSI3 clock (+)
CSI3_CLK_N	495	AI	MIPI CSI3 clock (-)
CSI3_LN0_P	496	AI	MIPI CSI3 lane 0 data (+)
CSI3_LN0_N	502	AI	MIPI CSI3 lane 0 data (-)
CSI3_LN1_P	503	AI	MIPI CSI3 lane 1 data (+)
CSI3_LN1_N	509	AI	MIPI CSI3 lane 1 data (-)
CSI3_LN2_P	510	AI	MIPI CSI3 lane 2 data (+)
CSI3_LN2_N	515	AI	MIPI CSI3 lane 2 data (-)
CSI3_LN3_P	516	AI	MIPI CSI3 lane 3 data (+)
CSI3_LN3_N	521	AI	MIPI CSI3 lane 3 data (-)
CSI4_CLK_P	3	AI	MIPI CSI4 clock (+)
CSI4_CLK_N	2	AI	MIPI CSI4 clock (-)
CSI4_LN0_P	5	AI	MIPI CSI4 lane 0 data (+)
CSI4_LN0_N	4	AI	MIPI CSI4 lane 0 data (-)
CSI4_LN1_P	8	AI	MIPI CSI4 lane 1 data (+)
CSI4_LN1_N	7	AI	MIPI CSI4 lane 1 data (-)
CSI4_LN2_P	12	AI	MIPI CSI4 lane 2 data (+)
CSI4_LN2_N	11	AI	MIPI CSI4 lane 2 data (-)
CSI4_LN3_P	17	AI	MIPI CSI4 lane 3 data (+)
CSI4_LN3_N	16	AI	MIPI CSI4 lane 3 data (-)
CSI5_CLK_P	10	AI	MIPI CSI5 clock (+)
CSI5_CLK_N	9	AI	MIPI CSI5 clock (-)
CSI5_LN0_P	14	AI	MIPI CSI5 lane 0 data (+)

CSI5_LN0_N	13	AI	MIPI CSI5 lane 0 data (-)		
CSI5_LN1_P	19	AI	MIPI CSI5 lane 1 data (+)		
CSI5_LN1_N	18	AI	MIPI CSI5 lane 1 data (-)		
CSI5_LN2_P	25	AI	MIPI CSI5 lane 2 data (+)		
CSI5_LN2_N	24	AI	MIPI CSI5 lane 2 data (-)		
CSI5_LN3_P	32	AI	MIPI CSI5 lane 3 data (+)		
CSI5_LN3_N	31	AI	MIPI CSI5 lane 3 data (-)		
CAM0_MCLK	15	DO	Master clock of camera 0		
CAM1_MCLK	20	DO	Master clock of camera 1		
CAM2_MCLK	26	DO	Master clock of camera 2		
CAM3_MCLK	33	DO	Master clock of camera 3		
CAM4_AON_MCLK	40	DO	Always on master clock of camera 4		
CAM5_MCLK	47	DO	Master clock of camera 5		
CAM6_MCLK	54	DO	Master clock of camera 6	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
CAM0_RST	69	DO	Reset of camera 0		
CAM1_RST	76	DO	Reset of camera 1		
CAM2_RST	83	DO	Reset of camera 2		
CAM3_RST	68	DO	Reset of camera 3		
CAM4_RST	75	DO	Reset of camera 4		
CAM5_RST	82	DO	Reset of camera 5		
CAM6_RST	89	DO	Reset of camera 6		
CAM0_I2C_SDA	53	OD	I2C data of CAM0		
CAM0_I2C_SCL	46	OD	I2C clock of CAM0		

CAM1_I2C_SDA	74	OD	I2C data of CAM1	
CAM1_I2C_SCL	67	OD	I2C clock of CAM1	
CAM2_I2C_SDA	88	OD	I2C data of CAM2	
CAM2_I2C_SCL	81	OD	I2C clock of CAM2	
CAM3_I2C_SDA	101	OD	I2C data of CAM3	
CAM3_I2C_SCL	95	OD	I2C clock of CAM3	
CAM4_I2C_SDA	112	OD	I2C data of CAM4	
CAM4_I2C_SCL	107	OD	I2C clock of CAM4	
AON_CAM_I2C_SDA	121	OD	Always on I2C data of camera	
AON_CAM_I2C_SCL	117	OD	Always on I2C clock of camera	
CAM_I3C_SDA	102	OD	I3C data of CAM	
CAM_I3C_SCL	108	OD	I3C data of CAM	
LDO1M_1V05	29	PO	1.05 V output power for always on camera DVDD	Vnom = 1.05 V $I_O$max = 1200 mA
LDO2M_1V05	36	PO	1.05 V output power for camera DVDD	Vnom = 1.05 V $I_O$max = 1200 mA
LDO3M_2V8	43	PO	2.8 V output power for camera AVDD	Vnom = 2.8 V $I_O$max = 300 mA
LDO4M_2V8	30	PO	2.8 V output power for camera AVDD	Vnom = 2.8 V $I_O$max = 300 mA
LDO5M_1V8	37	PO	1.8 V output power for camera AVDD	Vnom = 1.8 V $I_O$max = 600 mA
LDO6M_1V8	52	PO	1.8 V output power for always on camera AVDD	Vnom = 1.8 V $I_O$max = 300 mA
LDO7M_2V8	59	PO	2.8 V output power for camera AVDD	Vnom = 2.8 V $I_O$max = 600 mA
LDO1N_1V1	50	PO	1.1 V output power for camera DVDD	Vnom = 1.1 V $I_O$max = 1200 mA
LDO2N_1V1	57	PO	1.1 V output power for camera DVDD	Vnom = 1.1 V $I_O$max = 1200 mA
LDO3N_2V8	64	PO	2.8 V output power for camera AVDD	Vnom = 2.8 V $I_O$max = 300 mA
LDO4N_2V8	44	PO	2.8 V output power	Vnom = 2.8 V

			for camera AVDD	$I_O$max = 300 mA	
LDO5N_1V8	51	PO	1.8 V output power for camera DOVDD	Vnom = 1.8 V $I_O$max = 600 mA	
LDO6N_3V3	45	PO	3.3 V output power for TOF Camera	Vnom = 3.3 V $I_O$max = 300 mA	
LDO7N_2V96	66	PO	2.96 V output power for camera AFVDD	Vnom = 2.96 V $I_O$max = 600 mA	
Flash & Torch Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH_LED1	420	AO	Flash/torch driver output 1		
FLASH_LED2	425	AO	Flash/torch driver output 2		
FLASH_STROBE	434	DI	Flash LED strobe		If unused, keep it unconnected.
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	461	DI	Turn on/off the module		
VOL_UP	357	DI	Volume up		
VOL_DOWN	364	DI	Volume down		
UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	194	DO	Debug UART transmit	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
DBG_RXD	187	DI	Debug UART receive		
Sensor Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C0_SDA	177	OD	I2C0 data for external sensor	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
SENSOR_I2C0_SCL	170	OD	I2C0 clock for external sensor		
SENSOR_I2C1_SDA	91	OD	I2C1 data for external sensor		
SENSOR_I2C1_SCL	84	OD	I2C1 clock for external sensor		

SENSOR_I3C_SDA	142	OD	I3C data for external sensor		
SENSOR_I3C_SCL	139	OD	I3C clock for external sensor		
MAG_INT	349	DI	Magnetic sensor interrupt		
HALL_INT	370	DI	Hall sensor interrupt		
ALPS_INT	356	DI	Ambient light/proximity sensor interrupt		
IMU_INT1	341	DI	IMU interrupt 1		
IMU_INT2	334	DI	IMU interrupt 2		
APPS_I2C_SDA	469	OD	I2C data for APPS		
APPS_I2C_SCL	476	OD	I2C clock for APPS		
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
IMU_SPI_CLK	151	DO	IMU SPI clock		
IMU_SPI_CS	171	DO	IMU SPI chip select		
IMU_SPI_MISO	164	DI	IMU SPI master-in slave-out		
IMU_SPI_MOSI	157	DO	IMU SPI master-out slave-in		
CAM_SPI_CLK	94	DO	CAM SPI0 clock		
CAM_SPI_CS	100	DO	CAM SPI0 chip select	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
CAM_SPI_MISO	80	DI	CAM SPI0 master-in slave-out		
CAM_SPI_MOSI	87	DO	CAM SPI0 master-out slave-in		
FP_SPI_CLK	319	DO	FP SPI clock		
FP_SPI_CS	326	DO	FP SPI chip select		
FP_SPI_MISO	305	DI	FP SPI master-in slave-out		
FP_SPI_MOSI	312	DO	FP SPI master-out slave-in		
RF Antenna Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ANT_WIFI/BT0	130	AIO	Wi-Fi/Bluetooth antenna interface 0		50 Ω impedance
ANT_WIFI/BT1	137	AIO	Wi-Fi/Bluetooth antenna interface 1		
WLAN/Bluetooth Application Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
COEX_RXD	118	DI	2.4 GHz WWAN & Wi-Fi/Bluetooth coexistence receive		
COEX_TXD	122	DO	2.4 GHz WWAN & Wi-Fi/Bluetooth coexistence transmit		
N79_TXEN_TO_WLAN	110	DI	Notify N79 transmission from SDR transceiver to WLAN		
LAA_TXEN_TO_WLAN	115	DI	Notify LAA transmission from SDR transceiver to WLAN		
WLAN_TXEN_TO_N79	119	DO	Notify WLAN transmission from WLAN to SDR transceiver		
WLAN_TXEN_TO_LAA	123	DO	Notify WLAN transmission from WLAN to SDR transceiver		
NFC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NFC_SPI_CLK	318	DO	NFC SPI0 clock	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
NFC_SPI_CS	311	DO	NFC SPI0 chip select		
NFC_SPI_MISO	339	DI	NFC SPI0 master-in slave-out		
NFC_SPI_MOSI	325	DO	NFC SPI0 master-out slave-in		
NFC_I2C_SCL	360	OD	NFC I2C0 clock		

NFC_I2C_SDA	367	OD	NFC I2C0 data		
NFC_RST	353	DO	NFC reset		
NFC_CLK_REQ	346	DI	NFC clock request		
NFC_INT_REQ	304	DI	NFC interrupt request		
NFC_IN	373	DO	NFC output		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PM_ADC0	497	AI	General-purpose ADC interface		
PM_ADC1	490	AI	General-purpose ADC interface		
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_P	451	AI	Battery voltage detect (+)		Must be connected.
BAT_M	458	AI	Battery voltage detect (-)		Must be connected.
VBAT_SNS_M	415	AI	Sensed battery voltage for charger circuits (-)		Must be connected.
BAT_THERM	454	AI	Battery temperature detect		Must be pulled down to ground with a 100 kΩ resistor.
BAT_ID	447	AI	Battery type detect		
SMB_THERM	393	AI	SMB1394 parallel charging temperature detect		Parallel charging is not supported by default. If parallel charging is not needed, keep these pins unconnected.
SMB_CHG_EN	359	DO	SMB1394 parallel charging enable		
USB_IN_MID	401, 402, 403, 404, 405	PI	Power intput for parallel charging		
SMB_SPMI_DATA	372	DIO	SMB1394 SPMI data		

SMB_SPMI_CLK	378	DO	SMB1394 SPMI clock		
SMB_ICHG_SNS	397	AI	SMB1394 input to PMIC charger charge current limit control loop		
SMB_IIN_SNS	366	AI	SMB1394 input to PMIC charger input current limit control loop		
USB_OVP_SNS	375	AI	USB OVP input remove sense		
USB_OVP_DRV	381	AO	USB OVP FET gate drive		
Vibration Motor Driver Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
HAP_P	394	AO	Haptics driver output (+)		
HAP_M	390	AO	Haptics driver output (-)		
HAP_SWR_RX_CLK	384	DO	Haptics SoundWire receive clock		
HAP_SWR_RX_DATA	389	DIO	Haptics SoundWire receive data		
SGMII/USXGMII Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SGMII/USXGMII0_CLK_M	239	AO	SGMII/USXGMII clock 0 (-)		
SGMII/USXGMII0_CLK_P	244	AO	SGMII/USXGMII clock 0 (+)		
SGMII/USXGMII0_RX_M	233	AI	SGMII/USXGMII receive 0 (-)		
SGMII/USXGMII0_RX_P	238	AI	SGMII/USXGMII receive 0 (+)		
SGMII/USXGMII0_TX_M	219	AO	SGMII/USXGMII transmit 0 (-)		
SGMII/USXGMII0_TX_P	225	AO	SGMII/USXGMII transmit 0 (+)		
SGMII/USXGMII0_INT_N	206	DI	SGMII/USXGMII interrupt 0	V_{OL}max = 0.4 V V_{OH}min = 1.3 V V_{IL}max = 0.54 V	1.8 V power domain.
SGMII/USXGMII0_	234	DO	SGMII/USXGMII		

MDC			management data clock 0	V_{IH}min = 1.26 V	
SGMII/USXGMII0_MDIO	220	DIO	SGMII/USXGMII management data input/output 0		
SGMII/USXGMII0_RST_N	223	DO	Reset output for external PHY0		
SGMII/USXGMII1_CLK_M	245	AO	SGMII/USXGMII clock 1 (-)		
SGMII/USXGMII1_CLK_P	249	AO	SGMII/USXGMII clock 1 (+)		
SGMII/USXGMII1_RX_M	226	AI	SGMII/USXGMII receive 1 (-)		
SGMII/USXGMII1_RX_P	232	AI	SGMII/USXGMII receive 1 (+)		
SGMII/USXGMII1_TX_M	212	AO	SGMII/USXGMII transmit 1 (-)		
SGMII/USXGMII1_TX_P	218	AO	SGMII/USXGMII transmit 1 (+)		
SGMII/USXGMII1_INT_N	199	DI	SGMII/USXGMII interrupt 1		
SGMII/USXGMII1_MDC	227	DO	SGMII/USXGMII management data clock 1	V_{OL}max = 0.4 V V_{OH}min = 1.3 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V	1.8 V power domain.
SGMII/USXGMII1_MDIO	213	DIO	SGMII/USXGMII management data input/output 1		
RGMII Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII_RX0	266	DI	RGMII receive data bit 0		
RGMII_RX1	263	DI	RGMII receive data bit 1		
RGMII_RX2	259	DI	RGMII receive data bit 2		
RGMII_RX3	255	DI	RGMII receive data bit 3		
RGMII_RXC	271	DI	RGMII receive clock		
RGMII_RX_CTL	269	DI	RGMII receive control		
RGMII_TX0	268	DO	RGMII transmit data bit 0		

RGMII_TX1	265	DO	RGMII transmit data bit 1		
RGMII_TX2	262	DO	RGMII transmit data bit 2		
RGMII_TX3	258	DO	RGMII transmit data bit 3		
RGMII_TXC	272	DO	RGMII transmit clock		
RGMII_TX_CTL	270	DO	RGMII transmit control		
RGMII/SGMII/USXGMII1_RST_N	216	DO	Reset output for external PHY	V_{OL}max = 0.4 V V_{OH}min = 1.3 V	1.8 V power domain.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PMK_PWM	27	DO	PWM output		VREG_1V8_SYS power domain.
PM_PWM	448	DO	PWM output		VREG_1V8_SYS power domain.
CBL_PWR_N	34	DI	Cable power-on; Initiates power on when grounded		If unused, keep it open.
USB_BOOT	354	DI	Force the module into download mode		1.8 V power domain. A test point is recommended to be reserved.
FP_INT	333	DI	FP interrupt	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
FP_WUHB_INT	340	DI	FP wake-up host board interrupt		
FP_RST	347	DI	FP reset		
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_4	35	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
GPIO_5	28	DIO	General-purpose input/output		
GPIO_6	314	DIO	General-purpose input/output		

GPIO_7	321	DIO	General-purpose input/output
GPIO_8	376	DIO	General-purpose input/output
GPIO_9	380	DIO	General-purpose input/output
GPIO_12	146	DIO	General-purpose input/output
GPIO_15	374	DIO	General-purpose input/output
GPIO_18	348	DIO	General-purpose input/output
GPIO_19	328	DIO	General-purpose input/output
GPIO_22	361	DIO	General-purpose input/output
GPIO_23	362	DIO	General-purpose input/output
GPIO_46	214	DIO	General-purpose input/output
GPIO_47	221	DIO	General-purpose input/output
GPIO_48	97	DIO	General-purpose input/output
GPIO_49	113	DIO	General-purpose input/output
GPIO_62	103	DIO	General-purpose input/output
GPIO_68	124	DIO	General-purpose input/output
GPIO_70	127	DIO	General-purpose input/output
GPIO_71	111	DIO	General-purpose input/output
GPIO_73	116	DIO	General-purpose input/output
GPIO_88	209	DIO	General-purpose input/output
GPIO_89	327	DIO	General-purpose input/output
GPIO_90	320	DIO	General-purpose input/output
GPIO_91	313	DIO	General-purpose input/output

GPIO_137	186	DIO	General-purpose input/output		
GPIO_142	336	DIO	General-purpose input/output		
GPIO_143	315	DIO	General-purpose input/output		
GPIO_144	322	DIO	General-purpose input/output		
GPIO_146	306	DIO	General-purpose input/output		
GPIO_147	343	DIO	General-purpose input/output		
GPIO_150	156	DIO	General-purpose input/output		
GPIO_151	163	DIO	General-purpose input/output		
GPIO_152	335	DIO	General-purpose input/output		
GPIO_153	342	DIO	General-purpose input/output		
GPIO_154	329	DIO	General-purpose input/output		
GPIO_155	224	DIO	General-purpose input/output		
GPIO_156	231	DIO	General-purpose input/output		
GPIO_157	301	DIO	General-purpose input/output		
GPIO_159	308	DIO	General-purpose input/output		
GPIO_160	386	DIO	General-purpose input/output		
GPIO_162	355	DIO	General-purpose input/output		
GPIO_163	350	DIO	General-purpose input/output		
GPIO_177	150	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	LDO15B_1V8 power domain.
GPIO_198	155	DIO	General-purpose input/output		
GPIO_206	185	DIO	General-purpose input/output	V_{OL}max = 0.45 V V_{OH}min = 1.35 V V_{IL}max = 0.63 V V_{IH}min = 1.17 V	1.8 V power domain.
GPIO_207	178	DIO	General-purpose input/output		

PM_GPIO_03	475	DIO	General-purpose input/output of PM	VREG_1V8_SYS power domain.
PM_GPIO_04	441	DIO	General-purpose input/output of PM	
PM_GPIO_11	455	DIO	General-purpose input/output of PM	
RESERVED				
Pin Name	**Pin No.**			
RESERVED	72,78,79,85,93,98,86,92,99,104,41,48,55, 120, 203,			

2.6. EVB Kit

Quectel supplies an evaluation board with accessories to develop and test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Interface

The module provides 6 VBAT pins dedicated to connecting with the external power supply. The power supply range of the module is 3.55–4.4 V, and the recommended value is 3.8 V.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Comment
VBAT	418, 422, 423, 428, 429, 435	PIO	Power supply for the module	
GND	1, 6, 21, 22, 23, 38, 39, 42, 60, 61, 62, 65, 71, 73, 90, 96, 105, 106, 109, 114, 125, 126, 128, 129, 131, 132, 133, 134, 135, 136, 138, 140, 141, 144, 145, 147, 148, 149, 167, 176, 180, 192, 193, 196, 201, 202, 205, 211, 235, 240, 250, 254, 267, 273, 274, 279, 295, 296, 297, 298, 299, 307, 330, 331, 332, 338, 351, 352, 363, 368, 369, 379, 382, 383, 385, 387, 396, 398, 399, 400, 406, 407, 412, 414, 416, 417, 419, 424, 430, 431, 432, 436, 440, 442, 444, 450, 456, 462, 465, 466, 468, 472, 482, 488, 492, 498, 504, 508, 513, 526, 528, 531, 540, 546			

3.1.2. Reference Design for Power Supply

The power source is critical to the module's performance. The power supply of the module should be able to provide sufficient current of 6 A at least. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for +12 V input power supply:

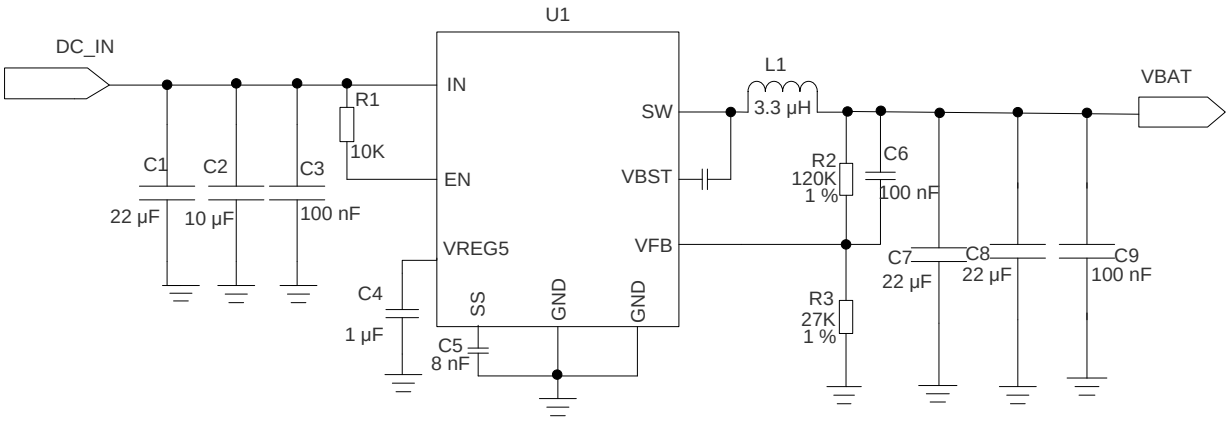


Figure 3: Reference Design of Power Input

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY, then you can cut off the power supply.

3.1.3. Requirements for Voltage Stability

The recommended power supply voltage of the module is 3.55 to 4.4 V. The power supply performance, such as load capacity, voltage ripple will directly influence the module's performance and stability. Under ultimate conditions, the module may have a transient peak current up to 6 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.55 V, the module will turn off automatically. Therefore, ensure the input voltage never drops below 3.55 V.

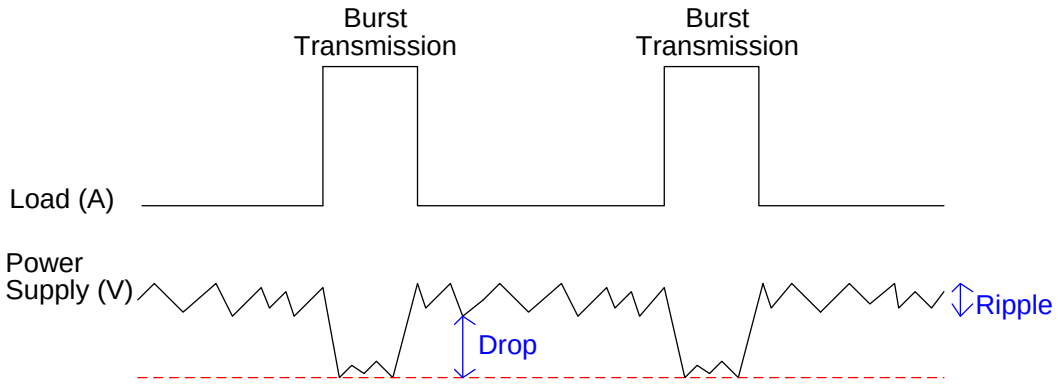


Figure 4: Power Supply Limits During Burst Transmission

To prevent the voltage from dropping below 3.55 V, it is recommended to connect a 100 µF bypass capacitor with low ESR as well as 10 µF, 100 nF, 33 pF and 10 pF filter capacitors in parallel near the VBAT pins of the module. It is also recommended that the PCB traces of VBAT should be as short as possible and wide enough to reduce the equivalent impedance of the VBAT traces and ensure that there will be no large voltage drop under high current at the maximum transmission power. The width of VBAT trace should be at least 3 mm. As per design rules, the longer the VBAT trace is, the wider it should be. Additionally, the ground plane of the power supply part should be as complete as possible.

To suppress the impact of power fluctuations and ensure the stability of the output power supply, it is suggested to add a TVS of at least 2000 W and place it as close to the VBAT pins as possible to enhance surge protection. The following figure shows a reference circuit:

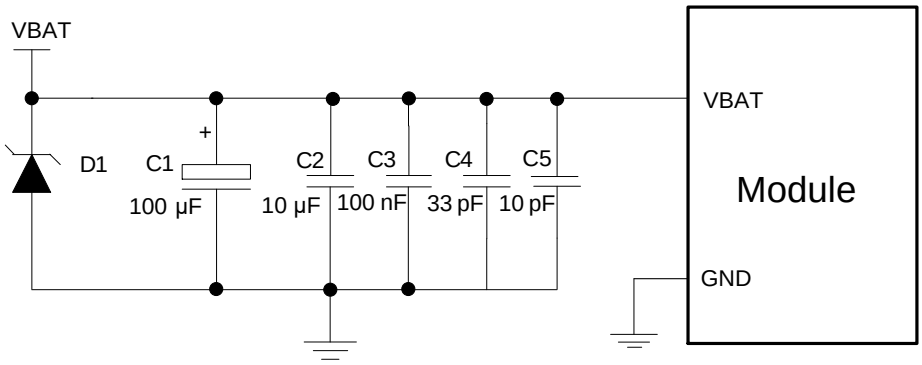


Figure 5: Reference Design of Power Supply

3.1.4. Battery Charge and Management

The module supports fully programmable switch-mode Li-ion battery charging. It can charge single-cell Li-ion and Li-polymer batteries. The switch-mode charging supports Quick Charge 2.0, 3.0 and 4.0. Its' maximum charging current is up to 3 A. The battery charger of the module supports trickle charging, pre-charge, constant current charging and constant voltage charging.

- **Trickle charging:** when the battery voltage is below 2.1 V, a 75-mA trickle charging current is applied to the battery.
- **Pre-charge:** when the battery voltage is between 2.1 V and the pre-charge cut-off voltage, the system switches to pre-charge. Charging current software programmable range is from 100 mA to 450 mA.
- **Constant current charging:** when the battery voltage is increased between the pre-charge cut-off voltage and constant current charging cut-off voltage, the system switches to constant current charging.
- **Constant voltage charging:** when the battery voltage reaches the constant current charging cut-off voltage, the system switches to constant voltage charging and the charging current decreases gradually. When the charging current reduces to about 100 mA, charging is completed.

Table 8: Pin Description of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
BAT_P	451	AI	Battery voltage detect (+)	
BAT_M	458	AI	Battery voltage detect (-)	
VBAT_SNS_M	415	AI	Sensed battery voltage for charger circuits (-)	
BAT_THERM	454	AI	Battery temperature detect	
BAT_ID	447	AI	Battery type detect	
SMB_THERM	393	AI	SMB1394 parallel charging temperature detect	
SMB _CHG_EN	359	DO	SMB1394 parallel charging enable	
USB_IN_MID	401, 402, 403, 404, 405	PI	Power input for SMB1394 parallel charging	
SMB_SPMI_DATA	372	DIO	SMB1394 SPMI data	
SMB_SPMI_CLK	378	DO	SMB1394 SPMI clock	
SMB_ICHG_SNS	397	AI	SMB1394 input to PMIC charger charge current limit control loop	
SMB_IIN_SNS	366	AI	SMB1394 input to PMIC charger input current limit control loop	
USB_OVP_SNS	375	AI	USB OVP input remove sense	

The module supports battery temperature detection with the condition that the battery integrates a thermistor (100 kΩ ±1 % NTC thermistor with a B-constant of 4050 K by default) and the thermistor is connected to BAT_THERM. If BAT_THERM is not connected, there will be malfunctioning, like battery charging failure, battery level display error.

A reference design for the battery charging circuit is shown below:

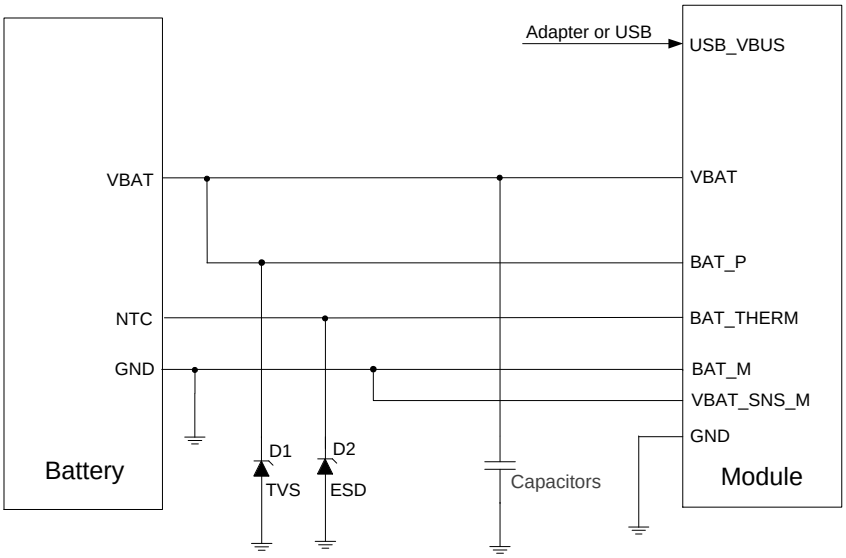


Figure 6: Reference Design of Charging Interface

Mobile devices are all powered by batteries. When different batteries are utilized, the charging and discharging curve must be modified correspondingly to achieve the best effect.

If the thermistor is not available in the battery or an adapter is utilized for powering the module, you must connect BAT_THERM to GND via a 100 kΩ resistor. Otherwise, the system may misjudge that the battery temperature is abnormal, which will cause battery charging failure.

BAT_P and BAT_M must be connected, and VBAT_SNS_M pin must be connected. Otherwise, the module will have abnormalities in voltage detection, as well as associated module power on/off and battery charging and discharging issues.

3.2. Turn On

3.2.1. Turn On with PWRKEY

Table 9: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	461	DI	Turn on/off the module	PWRKEY pin is pulled to 1.8 V internally.

When powering up the VBAT, it can be turned on by driving PWRKEY low for at least 1.6 s. It is recommended to use an open drain/collector driver to control the PWRKEY. PWRKEY is pulled up to VBAT internally.

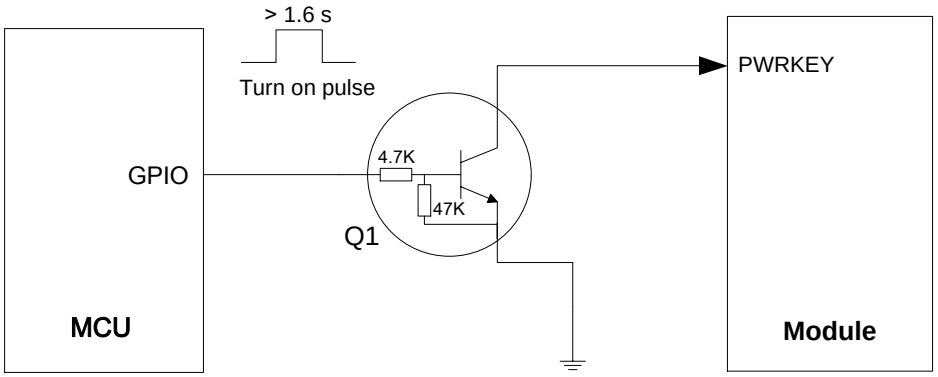


Figure 7: Reference Design of Turn On with Driving Circuit

Another way to control the PWRKEY is using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from finger. Therefore, you should place a TVS near the keystroke for ESD protection. Additionally, a 1 kΩ resistor is connected in series to PWRKEY for ESD protection.

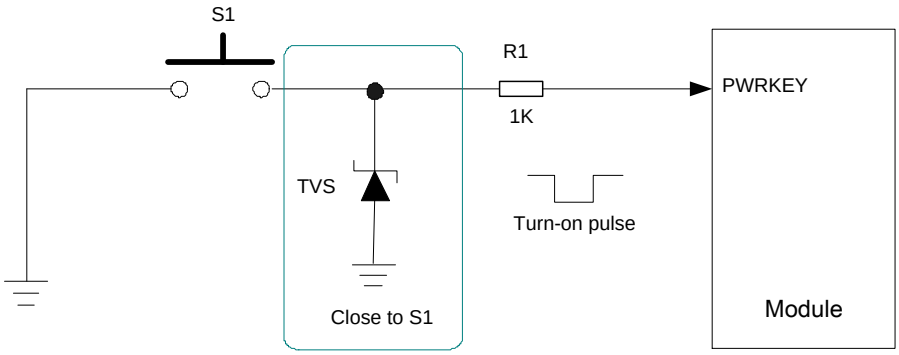


Figure 8: Reference Design of Turn On with Keystroke

3.2.2. Turn On Automatically with CBL_PWR_N

Table 10: Pin Definition of CBL_PWR_N

Pin Name	Pin No.	I/O	Description
CBL_PWR_N	34	DI	Cable power-on; Initiates power on when grounded

The module can be turned on automatically by driving CBL_PWR_N pin to GND via a 1 kΩ resistor. CBL_PWR_N pin is pulled up internally. A simple reference circuit is illustrated in the following figure.

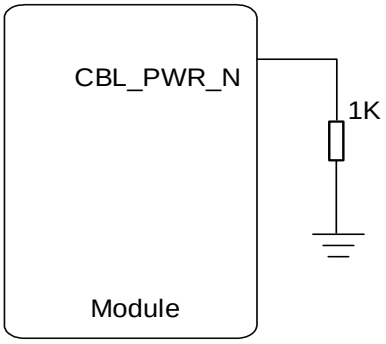


Figure 9: Reference Circuit of Automatic Turn-on

NOTE

If the module turns on automatically through CBL_PWR_N pin, it cannot be turned off manually. In such case, it can be turned off only by cutting off the power supply of system.

The power-up timing is illustrated in the following figure.

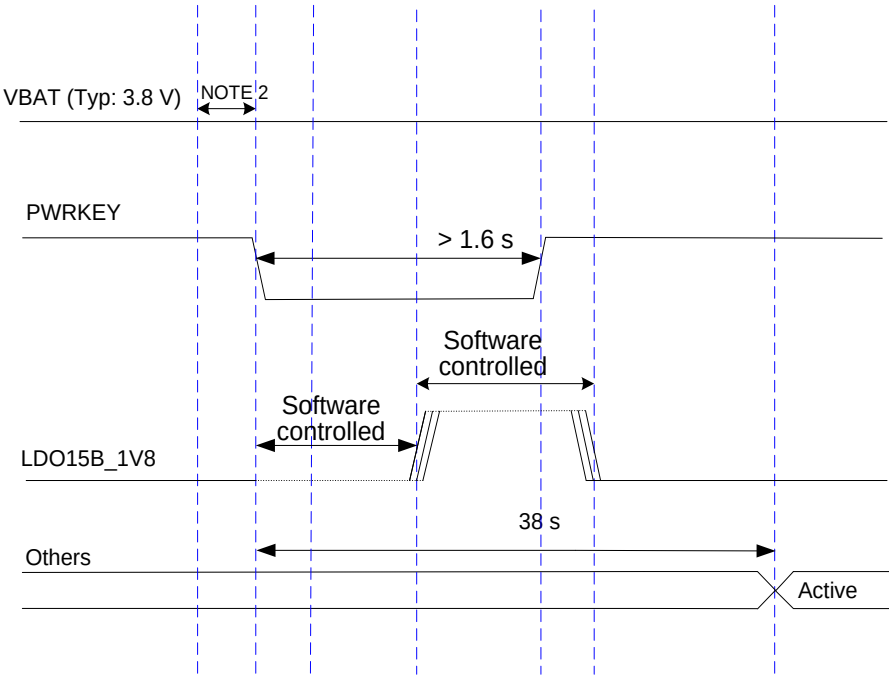


Figure 10: Timing of Turn On with PWRKEY

NOTE

1. When the module is powered up for the first time, its turn on timing may be different from that shown in the figure above.
2. Ensure the voltage of VBAT is stable before driving the PWRKEY low. It is recommended to drive PWRKEY low after VBAT reaches 3.8 V and remains stable for 30 ms. PWRKEY cannot be driven low all the time.

3.3. Restart/Turn Off

The module can be turned off by driving the PWRKEY low for at least 1 second. Set the PWRKEY low for at least 1 second, and then choose to turn off or to restart the module when the prompt window comes up. The other way to execute the forced restart is to drive the PWRKEY low for a long time (for at least 8 seconds).

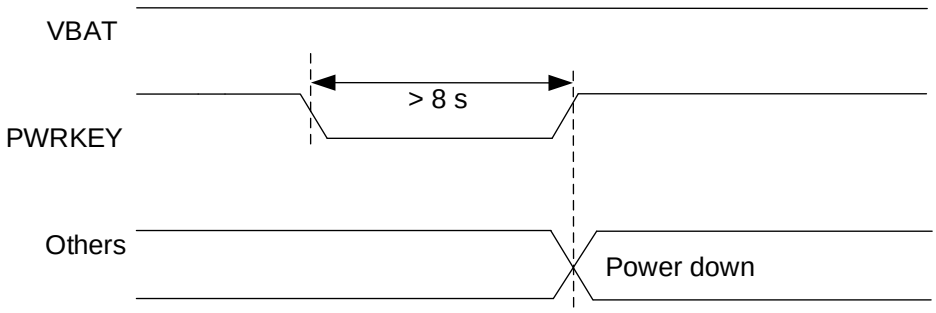


Figure 11: Timing of Restart

3.4. VRTC

The RTC of the module can be powered by an external power supply pin VRTC. When VBAT is disconnected and you need to reserve RTC function, then VRTC cannot be kept unconnected. The RTC can be powered by an external power source when the module is powered down and there is no power supply for the VBAT. The power source can be an external battery or capacitor according to application demands. The following are some reference circuit designs when an external battery or capacitor is utilized for powering RTC.

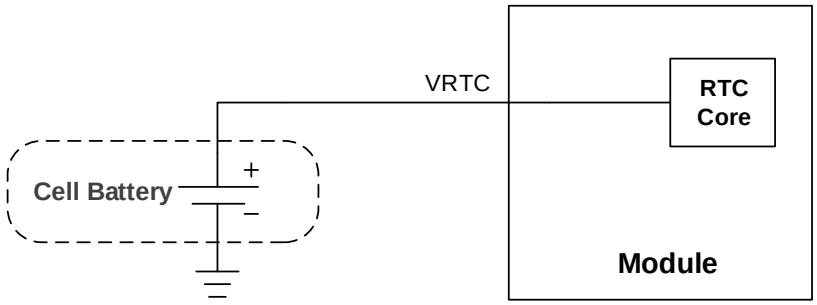


Figure 12: RTC Powered by Rechargeable Cell Battery

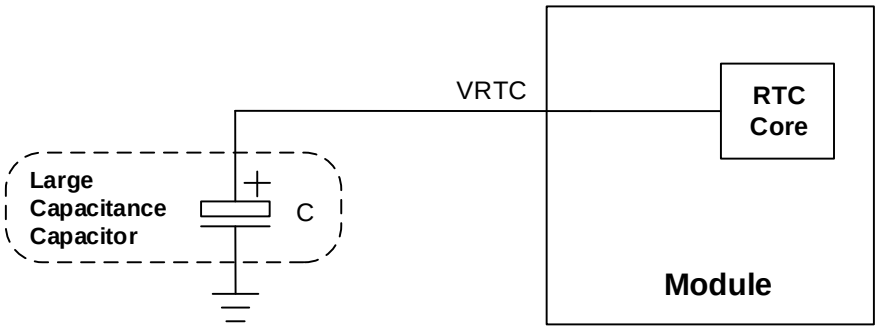


Figure 13: RTC Powered by Large Capacitance Capacitor

If RTC fails, the module can synchronize time over the network after being powering up.

- The recommended input voltage range for VRTC is 2.5–3.25 V and the recommended typical value is 3.0 V. The average power consumption is 7 μA when VBAT is disconnected.
- If a rechargeable button battery is used, ESR of the battery should be less than 1 kΩ. It is recommended to use MS621FE-FL11E of SEIKO.

3.5. Power Output

The module supports multiple regulated voltage output for peripheral circuits. In practical application, it is recommended to use a 10-pF and a 33-pF capacitor in parallel to suppress high-frequency noise.

Table 11: Power Information

Pin Name	Default Voltage (V)	Drive Current (mA)	Standby
LDO1B_1V8	1.8	TBD	

LDO2B_3V0	3.0	100	
LDO5B_3V1	3.1	150	
LDO11B_1V2	1.2	400	
LDO12B_1V8	1.8	TBD	
LDO13B_3V0	3.0	150	
LDO14B_2V8	2.8	TBD	
LDO15B_1V8	1.8	20	Keeps ON
LDO2G_1V2	1.2	TBD	
VREG_1V8_SYS	1.8	20	
VPH_PWR	VBAT	2000	Keeps ON

4 Application Interfaces

4.1. USB Interface

The module provides one USB interface which complies with USB 3.1 Gen 2 and USB 2.0 specifications and supports USB OTG. It supports USB Type-C interface and DisplayPort mode. It also supports SuperSpeed mode (10 Gbps) for USB 3.1 Gen 2, high-speed (480 Mbps) and full-speed (12 Mbps) modes for USB 2.0. The USB interface is used for AT command transmission, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB.

4.1.1. Type-C Interface

4.1.1.1. Type-C Mode

Table 12: Pin Description of USB Type-C Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	408, 409, 410, 411, 413	PIO	Charging power input; Power supply for OTG device; USB/adaptor insertion detection	
USB_DP	344	AIO	USB 2.0 differential data (+)	90 Ω differential impedance. USB 2.0 standard compliant.
USB_DM	337	AIO	USB 2.0 differential data (-)	
USB_SS0_RX_P	317	AI	USB 3.1 channel 0 SuperSpeed receive (+)	90 Ω differential impedance. USB 3.1 standard compliant.
USB_SS0_RX_M	316	AI	USB 3.1 channel 0 SuperSpeed receive (-)	
USB_SS0_TX_P	303	AO	USB 3.1 channel 0 SuperSpeed transmit (+)	
USB_SS0_TX_M	302	AO	USB 3.1 channel 0 SuperSpeed transmit (-)	
USB_SS1_RX_P	324	AI	USB 3.1 channel 1 SuperSpeed receive (+)	

USB_SS1_RX_M	323	AI	USB 3.1 channel 1 SuperSpeed receive (-)
USB_SS1_TX_P	310	AO	USB 3.1 channel 1 SuperSpeed transmit (+)
USB_SS1_TX_M	309	AO	USB 3.1 channel 1 SuperSpeed transmit (-)
USB_CC1	358	AI	USB Type-C configuration channel 1
USB_CC2	365	AI	USB Type-C configuration channel 2
USB_THERM	483	AI	USB temperature detect
DP_AUX_P	371	AIO	DisplayPort auxiliary channel (+)
DP_AUX_N	377	AIO	DisplayPort auxiliary channel (-)
USB_SBU1	421	AI	USB Type-C SBU 1
USB_SBU2	426	AI	USB Type-C SBU 2

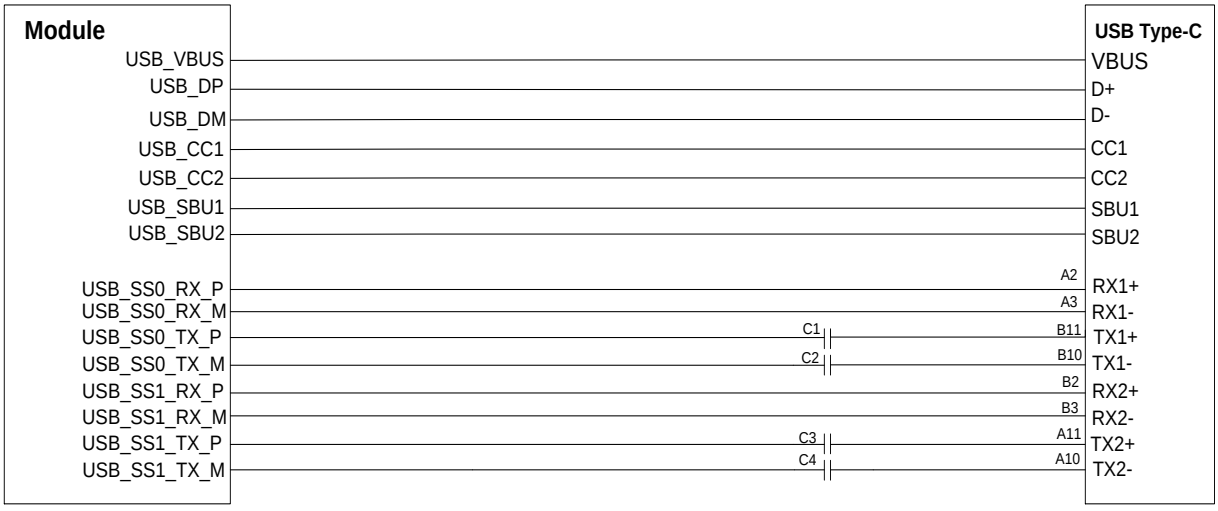


Figure 14: Reference Design of USB Type-C Mode

4.1.1.2. DisplayPort Mode

The module supports 4-lane DisplayPort mode up to 4K @ 60 fps over Type-C.

Table 13: USB Type-C & DisplayPort Mode Configuration

Pin Name	USB Type-C Mode	DisplayPort Mode
USB_SS0_RX_P/M	USB_SS0_RX_P/M	DP_LANE0_P/M
USB_SS0_TX_P/M	USB_SS0_TX_P/M	DP_LANE1_P/M
USB_SS1_RX_P/M	USB_SS1_RX_P/M	DP_LANE3_P/M
USB_SS1_TX_P/M	USB_SS1_TX_P/M	DP_LANE2_P/M
DP_AUX_P/M	SBU1/2	DP_AUX_P/N
USB_DP/M	USB_DP/M	USB_DP/M
USB_CC1/CC2	USB_CC1/CC2	HOTPLUG_DET/VCONN
USB_VBUS	USB_VBUS	USB_VBUS
GPIO_68	-	SBU_SW_OE
GPIO_70	-	SBU_SW_SEL
GND	GND	GND

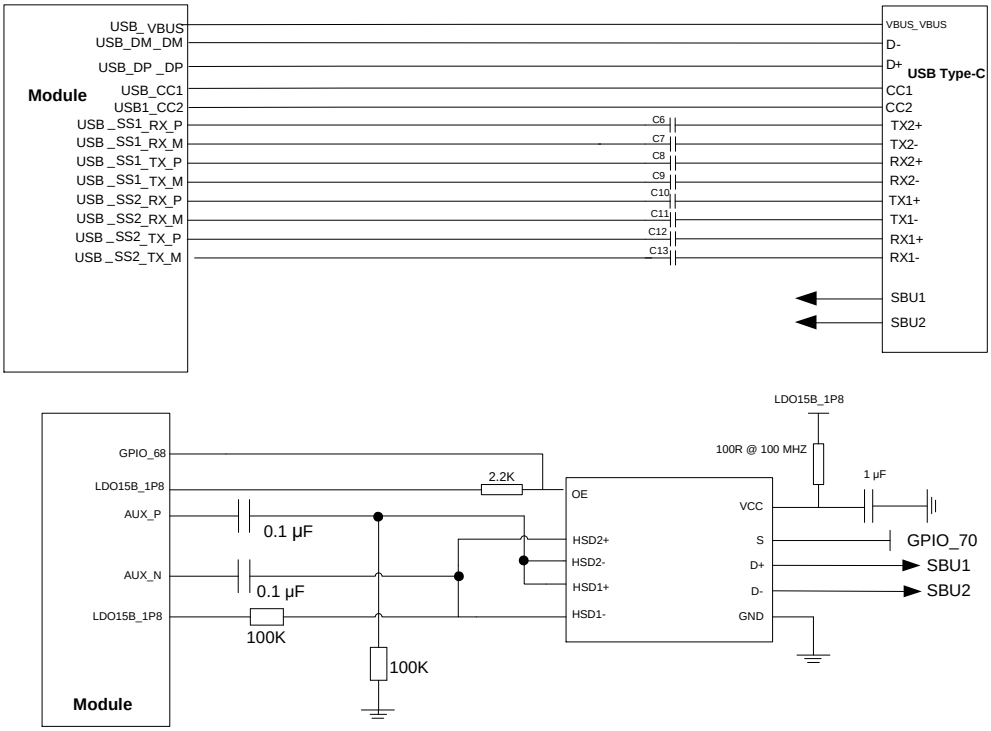


Figure 15: Reference Design of DisplayPort Mode

4.1.2. USB Interfaces Design Considerations

Table 14: USB Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Signal	Length	Length Matching
337	USB_DM	26.71	0.13
344	USB_DP	26.84	
317	USB_SS0_RX_P	24.36	0.08
316	USB_SS0_RX_M	24.28	
303	USB_SS0_TX_P	22.67	0.05
302	USB_SS0_TX_M	22.72	
324	USB_SS1_RX_P	18.43	0.01
323	USB_SS1_RX_M	18.44	
309	USB_SS1_TX_P	21.60	0.31
310	USB_SS1_TX_M	21.91	
371	DP_AUX_P	36.93	0.12
377	DP_AUX_N	37.05	

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC.
- The reference ground plane under the USB signal traces must be continuous without any cuts or vias to ensure impedance continuity.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, stray capacitance should be less than 2 pF for USB 2.0, and less than 0.5 pF for USB 3.1 Gen 2.
- Do not route USB 3.1 Gen 2 signal traces under RF signal traces. Crossing or being parallel with RF signal traces is forbidden.

- For USB 3.1 Gen 2 signal traces, ntra-pair length matching (P/M) should be less than 0.7 mm, while the inter-pair length matching (Tx/Rx) should be less than 10 mm.
- For USB 3.1 Gen 2, the clearance between Rx and Tx signal traces should be three times the signal trace width. The clearance between USB 3.1 Gen 2 signal traces and other signal traces should be four times the signal trace width.
- For USB 2.0 signal traces, the total trace length of each signal should be less than 90 mm, the differential data pair matching (P/M) should be less than 2 mm.
- For USB 2.0, the clearance between DP and DM signal traces should be three times the signal trace width and the clearance between USB 2.0 signal traces and other signal traces should be four times the signal trace width.
- For DisplayPort, the length matching between DP_AUX_N and DP_AUX_P should be less than 7 mm.

4.2. USB_BOOT

The module provides a USB_BOOT for forced download. Pulling up USB_BOOT to LAO15B_1V8 before turning on the module, and then the module will enter forced download mode. This is an emergency option when failures such as abnormal start-up or running occur. For firmware upgrade and software debugging in the future, reserve the following reference design.

Table 15: Pin Description of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	354	DI	Force the module into download mode	A test point is recommended to be reserved.

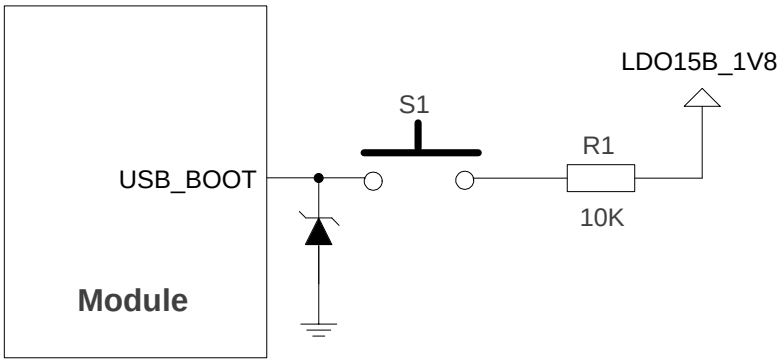


Figure 16: Reference Design of USB_BOOT

4.3. SD Card Interface

SD card interface of the module complies with SD 3.0 specifications:

Table 16: Pin Description of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	198	DO	SD card clock	
SD_CMD	191	DIO	SD card command	
SD_DATA0	183	DIO	SDIO data bit 0	
SD_DATA1	190	DIO	SDIO data bit 1	
SD_DATA2	197	DIO	SDIO data bit 2	
SD_DATA3	204	DIO	SDIO data bit 3	
SD_DET	184	DI	SD card hot-plug detect	
SD_VDD	481	PO	SD card power supply	
SD_PU_VDD	474	PO	1.8 V output power for SD card pull-up circuits	

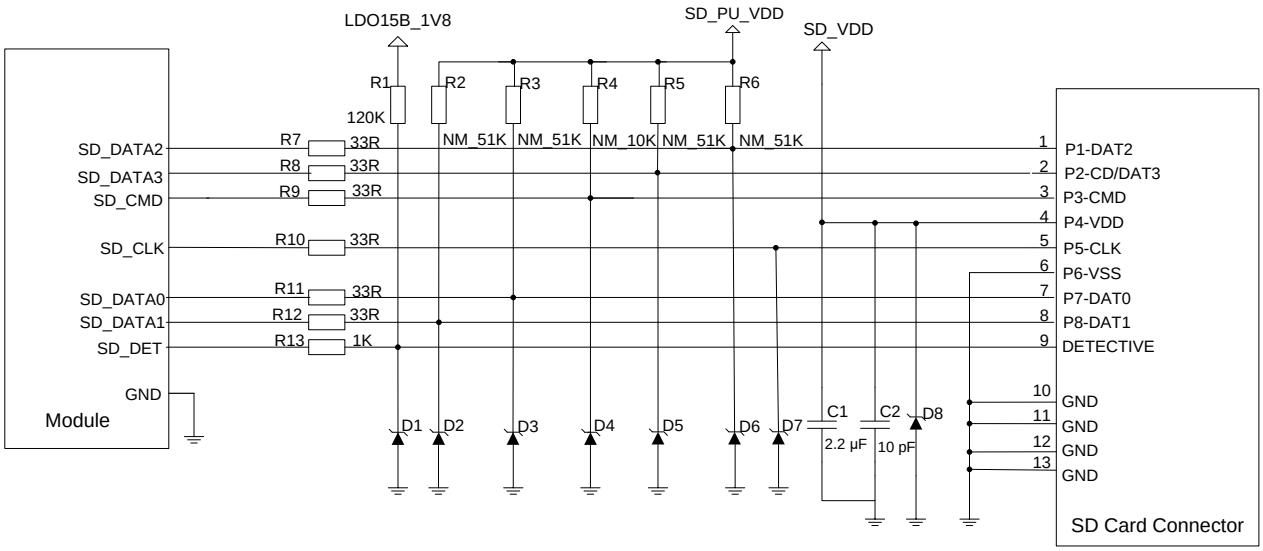


Figure 17: Reference Design of SD Card Interface

SD_VDD is a peripheral driver power supply for SD card. Because of the high drive current, it is recommended to keep the trace width as at least 0.6 mm. To ensure the stability of drive power, you should add a 4.7-μF and a 33-pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK and SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of these traces as 50 Ω, shield them and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB and keep their lengths the same. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 50 Ω ±10 %, and add ground shielding.
- Trace length matching between SD_CLK and SD_CMD/SD_DATA should be less than 2 mm for SDR104 mode.
- Trace length requirements: less than 50 mm for traces of SDR104 mode.
- Clearance between signal traces should be 1.5 times the trace width.
- The capacitive reactance of SD_DATA[0:3], SD_CLK and SD_CMD traces should be less than 8 pF.

Table 17: SD Card Interface Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length (mm)
198	SD_CLK	36.80
191	SD_CMD	36.32
183	SD_DATA0	36.34
190	SD_DATA1	36.48
197	SD_DATA2	36.15
204	SD_DATA3	36.31

4.4. UART

The module supports a group of UART.

Debug UART: 2-wire UART, used for debugging only.

Table 18: Pin Description of UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	194	DO	Debug UART transmit	Test points must be reserved.
DBG_RXD	187	DI	Debug UART receive	

Debug UART is a 2-wire UART with 1.8 V power domain. You can use a level-shifting chip between the module and host's UART if the host is equipped with a 3.3 V UART:

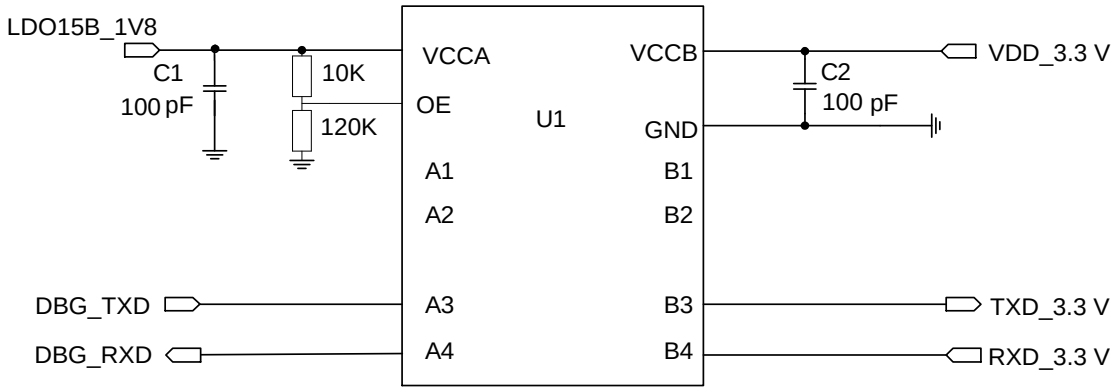


Figure 18: Reference Design of UART with Level-shifting Chip (for Debug UART)

The following circuit shows a reference design for the communication between the module and a PC with a standard RS-232 level-shifting chip:

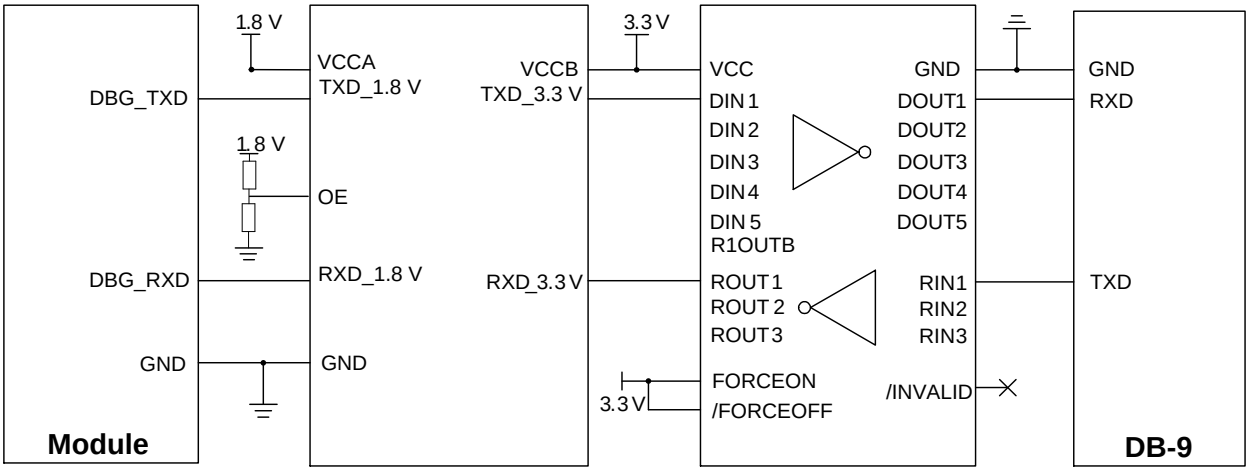


Figure 19: Reference Design of UART with RS-232 Level-shifting Chip (for Debug UART)

4.5. SPI

The module provides 4 groups of SPI. These interfaces only support the master mode, which can be used for fingerprint recognition, sensor, camera and so on.

Table 19: Pin Description of SPI

Pin Name	Pin No.	I/O	Description	Comment
IMU_SPI_CLK	151	DO	IMU SPI clock	
IMU_SPI_CS	171	DO	IMU SPI chip select	
IMU_SPI_MISO	164	DI	IMU SPI master-in slave-out	
IMU_SPI_MOSI	157	DO	IMU SPI master-out slave-in	
CAM_SPI_CLK	94	DO	CAM SPI clock	
CAM_SPI_CS	100	DO	CAM SPI chip select	
CAM_SPI_MISO	80	DI	CAM SPI master-in slave-out	
CAM_SPI_MOSI	87	DO	CAM SPI master-out slave-in	
FP_SPI_CLK	319	DO	FP SPI clock	
FP_SPI_CS	326	DO	FP SPI chip select	
FP_SPI_MISO	305	DI	FP SPI master-in slave-out	
FP_SPI_MOSI	312	DO	FP SPI master-out slave-in	
NFC_SPI_CLK	318	DO	NFC SPI0 clock	
NFC_SPI_CS	311	DO	NFC SPI0 chip select	
NFC_SPI_MISO	339	DI	NFC SPI0 master-in slave-out	
NFC_SPI_MOSI	325	DI	NFC SPI0 master-out slave-in	

4.6. I2C Interfaces

The module supports up to 12 groups of I2C interfaces. 2 of them are generic I2C interfaces, 10 of them are dedicated I2C interfaces. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V.

Table 20: Pin Description of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CAM0_I2C_SDA	53	OD	I2C data of camera 0	
CAM0_I2C_SCL	46	OD	I2C clock of camera 0	
CAM1_I2C_SDA	74	OD	I2C data of camera 1	
CAM1_I2C_SCL	67	OD	I2C clock of camera 1	
CAM2_I2C_SDA	88	OD	I2C data of camera 2	
CAM2_I2C_SCL	81	OD	I2C clock of camera 2	
CAM3_I2C_SDA	101	OD	I2C data of camera 3	
CAM3_I2C_SCL	95	OD	I2C clock of camera 3	
CAM4_I2C_SDA	112	OD	I2C data of camera 4	
CAM4_I2C_SCL	107	OD	I2C clock of camera 4	
CAM_AON_I2C_SDA	121	OD	I2C data of always on camera	
CAM_AON_I2C_SCL	117	OD	I2C clock of always on camera	
TP0_I2C_SDA	200	OD	TP0 I2C data	
TP0_I2C_SCL	207	OD	TP0 I2C clock	
TP1_I2C_SDA	49	OD	TP1 I2C data	
TP1_I2C_SCL	56	OD	TP1 I2C clock	
SENSOR_I2C0_SDA	177	OD	I2C0 data for external sensor	
SENSOR_I2C0_SCL	170	OD	I2C0 clock for external sensor	
SENSOR_I2C1_SDA	91	OD	I2C1 data for external sensor	
SENSOR_I2C1_SCL	84	OD	I2C1 clock for external sensor	

APPS_I2C_SDA	469	OD	I2C data for APPS
APPS_I2C_SCL	476	OD	I2C clock for APPS
NFC_I2C_SCL	360	OD	NFC I2C clock
NFC_I2C_SDA	367	OD	NFC I2C data

4.7. I2S Interfaces

The module supports up to 2 groups of I2S interfaces. The reference power domain is 1.8 V.

Table 21: Pin Description of I2S Interfaces

Pin Name	Pin No.	I/O	Description	Comment
HIFI_DAC_I2S_DATA0	175	DIO	HIFI DAC I2S data channel 0	
HIFI_DAC_I2S_DATA1	182	DIO	HIFI DAC I2S data channel 1	
HIFI_DAC_I2S_MCLK	168	DO	HIFI DAC I2S master clock	
HIFI_DAC_I2S_CLK	161	DO	HIFI DAC I2S clock	
HIFI_DAC_I2S_WS	189	DO	HIFI DAC I2S word select	
MI2S_DATA0	166	DIO	MI2S data channel 0	
MI2S_DATA1	153	DIO	MI2S data channel 1	
MI2S_SCLK	173	DO	MI2S bit clock	
MI2S_WS	159	DO	MI2S word select	

4.8. Audio Interfaces

The module provides SoundWire and digital microphone interfaces. One SoundWire interface is dedicated to transmit data between the module and analog codec WCD9385. The other SoundWire interface is dedicated to transmit data between the module and audio amplifier WSA8845.

Table 22: Pin Description of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
WSA0_EN	160	DO	WSA0 enable	
WSA1_EN	154	DO	WSA1 enable	
WSA0_SWR_CLK	172	DO	WSA0 SoundWire clock	
WSA1_SWR_CLK	158	DO	WSA1 SoundWire clock	
WSA0_SWR_DATA	165	DIO	WSA0 SoundWire data	
WSA1_SWR_DATA	152	DIO	WSA1 SoundWire data	
WCD_RST	208	DO	WCD reset	
WCD_SWR_TX_CLK	253	DO	WCD SoundWire transmit clock	
WCD_SWR_TX_DATA0	248	DIO	WCD SoundWire transmit data 0	
WCD_SWR_TX_DATA1	242	DIO	WCD SoundWire transmit data 1	
WCD_SWR_TX_DATA2	236	DIO	WCD SoundWire transmit data 2	
WCD_SWR_RX_CLK	229	DO	WCD SoundWire receive clock	
WCD_SWR_RX_DATA0	222	DIO	WCD SoundWire receive data 0	
WCD_SWR_RX_DATA1	215	DIO	WCD SoundWire receive data 1	
DMIC23_CLK	181	DO	Digital microphone 23 clock	
DMIC23_DATA	174	DI	Digital microphone 23 data	
DMIC01_CLK	195	DO	Digital microphone 01 clock	
DMIC01_DATA	188	DI	Digital microphone 01 data	

4.9. ADC Interfaces

The module provides 2 ADC interfaces which support up to 14-bit resolution.

Table 23: Pin Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PM_ADC0	497	AI	General-purpose ADC interface	
PM_ADC0	490	AI	General-purpose ADC interface	

4.10. LCM Interfaces

The module provides 2 LCM interfaces, which is MIPI_DSI standard compliant. The interface supports 2 data lines for high-speed differential data transmission. The data rate can reach up to 2.5 Gbps per lane. The interface supports 8-lane display (5120 × 2880 @ 60 fps).

Table 24: Pin Description of LCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LCD0_RST	179	DO	LCD0 reset	
LCD0_TE	228	DI	LCD0 tearing effect	
DSI0_CLK_P	491	AO	LCD0 tearing effect	
DSI0_CLK_N	485	AO	LCD0 MIPI clock (+)	
DSI0_LN0_P	484	AO	LCD0 MIPI clock (-)	
DSI0_LN0_N	478	AO	LCD0 MIPI lane 0 data (+)	
DSI0_LN1_P	477	AO	LCD0 MIPI lane 0 data (-)	
DSI0_LN1_N	471	AO	LCD0 MIPI lane 1 data (+)	
DSI0_LN2_P	470	AO	LCD0 MIPI lane 1 data (-)	
DSI0_LN2_N	464	AO	LCD0 MIPI lane 2 data (+)	
DSI0_LN3_P	463	AO	LCD0 MIPI lane 2 data (-)	
DSI0_LN3_N	457	AO	LCD0 MIPI lane 3 data (+)	
LCD1_RST	77	DO	LCD1 reset	
LCD1_TE	143	DI	LCD1 tearing effect	

DSI1_CLK_P	507	AO	LCD1 MIPI clock (+)
DSI1_CLK_N	501	AO	LCD1 MIPI clock (-)
DSI1_LN0_P	500	AO	LCD1 MIPI lane 0 data (+)
DSI1_LN0_N	494	AO	LCD1 MIPI lane 0 data (-)
DSI1_LN1_P	493	AO	LCD1 MIPI lane 1 data (+)
DSI1_LN1_N	487	AO	LCD1 MIPI lane 1 data (-)
DSI1_LN2_P	486	AO	LCD1 MIPI lane 2 data (+)
DSI1_LN2_N	480	AO	LCD1 MIPI lane 2 data (-)
DSI1_LN3_P	479	AO	LCD1 MIPI lane 3 data (+)
DSI1_LN3_N	473	AO	LCD1 MIPI lane 3 data (-)

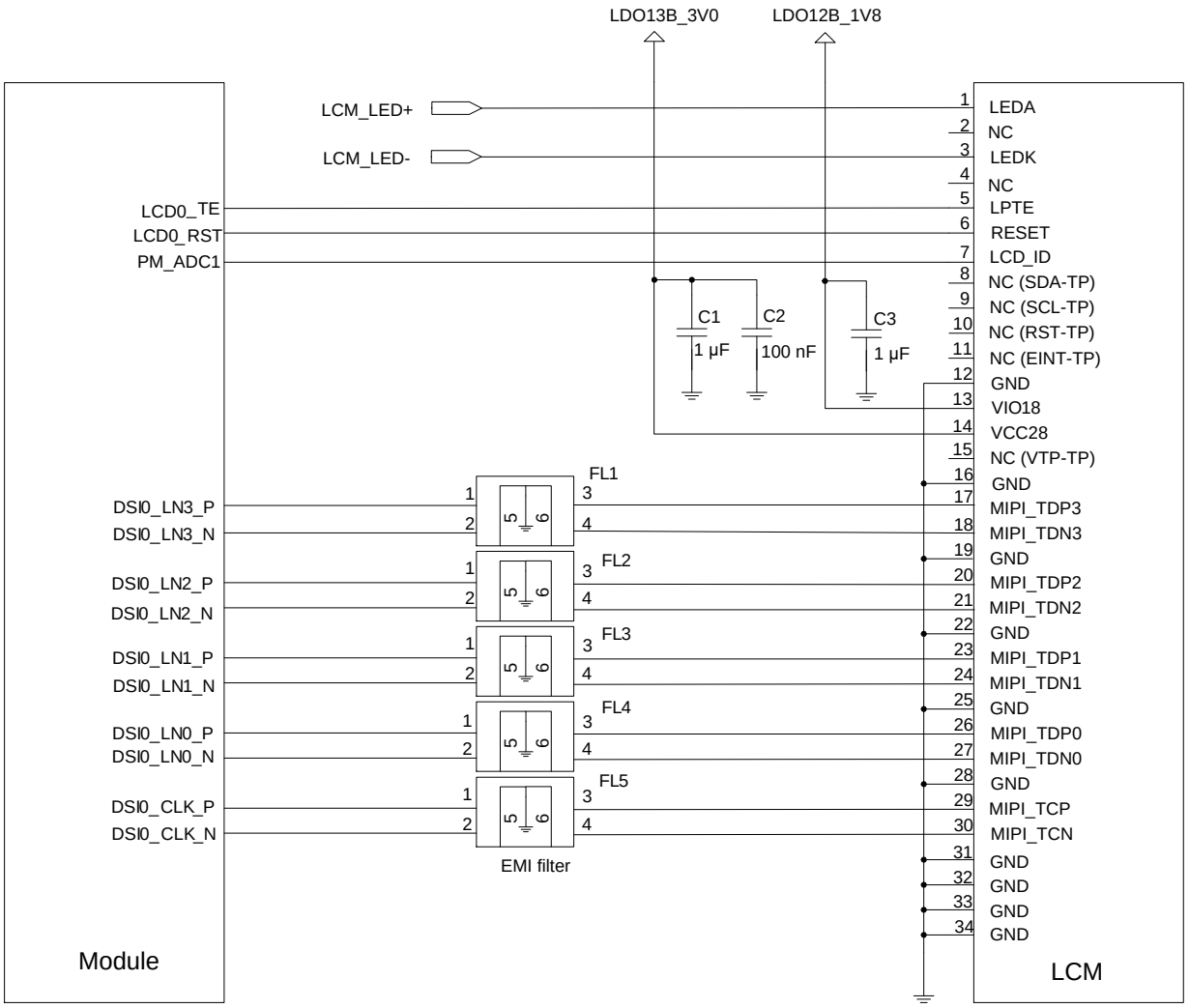


Figure 20: Reference Design of LCM0 Interface

NOTE

The reference design of LCM1 interface is similar to LCM0 interface.

MIPI are high-speed signal traces. It is recommended to add common-mode chokes in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that LCM factory burn an OTP register to distinguish different screens. You can also connect the LCD_ID of LCM to the GPIOs of the module to distinguish different screens by level detection. But note that the output voltage of LCD_ID should not exceed the voltage range of the GPIOs.

You can design an external backlight drive circuit for LCM according to actual requirement. PWM can be used for backlight brightness adjustment.

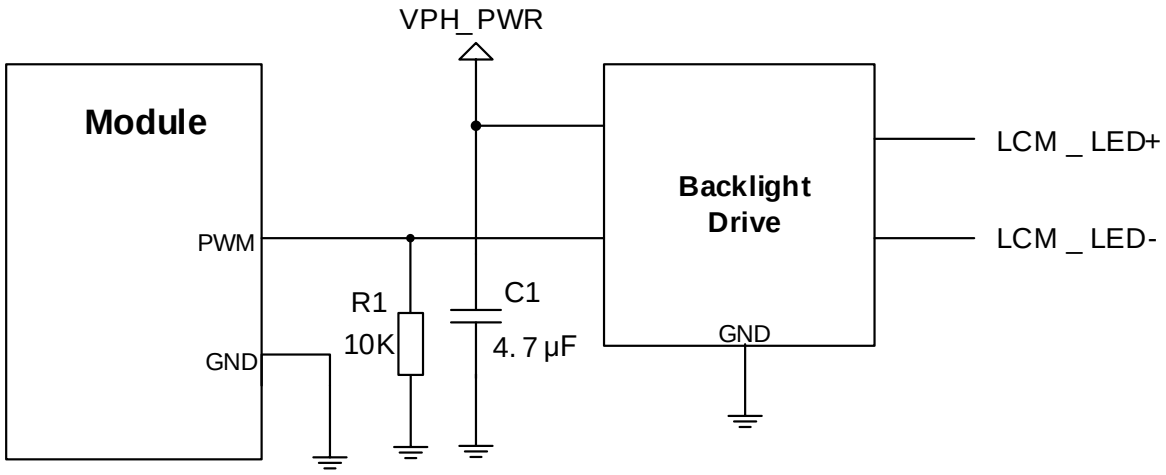


Figure 21: Reference Design of LCM Interface External Backlight Drive

4.11. Camera Interfaces

Based on MIPI_CSI standard, the module supports 6 cameras. The maximum data rate is up to 2.5 Gbps/lane.

Table 25: Pin Description of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CSI0_CLK_P	499	AI	MIPI CSI0 clock (+)	
CSI0_CLK_N	505	AI	MIPI CSI0 clock (-)	
CSI0_LN0_P	506	AI	MIPI CSI0 lane 0 data (+)	
CSI0_LN0_N	511	AI	MIPI CSI0 lane 0 data (-)	
CSI0_LN1_P	512	AI	MIPI CSI0 lane 1 data (+)	
CSI0_LN1_N	517	AI	MIPI CSI0 lane 1 data (-)	
CSI0_LN2_P	518	AI	MIPI CSI0 lane 2 data (+)	
CSI0_LN2_N	522	AI	MIPI CSI0 lane 2 data (-)	

CSI0_LN3_P	523	AI	MIPI CSI0 lane 3 data (+)
CSI0_LN3_N	527	AI	MIPI CSI0 lane 3 data (-)
CSI1_CLK_P	519	AI	MIPI CSI1 clock (+)
CSI1_CLK_N	514	AI	MIPI CSI1 clock (-)
CSI1_LN0_P	524	AI	MIPI CSI1 lane 0 data (+)
CSI1_LN0_N	520	AI	MIPI CSI1 lane 0 data (-)
CSI1_LN1_P	529	AI	MIPI CSI1 lane 1 data (+)
CSI1_LN1_N	525	AI	MIPI CSI1 lane 1 data (-)
CSI1_LN2_P	533	AI	MIPI CSI1 lane 2 data (+)
CSI1_LN2_N	530	AI	MIPI CSI1 lane 2 data (-)
CSI1_LN3_P	537	AI	MIPI CSI1 lane 3 data (+)
CSI1_LN3_N	534	AI	MIPI CSI1 lane 3 data (-)
CSI2_CLK_P	532	AI	MIPI CSI2 clock (+)
CSI2_CLK_N	535	AI	MIPI CSI2 clock (-)
CSI2_LN0_P	536	AI	MIPI CSI2 lane 0 data (+)
CSI2_LN0_N	538	AI	MIPI CSI2 lane 0 data (-)
CSI2_LN1_P	539	AI	MIPI CSI2 lane 1 data (+)
CSI2_LN1_N	541	AI	MIPI CSI2 lane 1 data (-)
CSI2_LN2_P	542	AI	MIPI CSI2 lane 2 data (+)
CSI2_LN2_N	543	AI	MIPI CSI2 lane 2 data (-)
CSI2_LN3_P	544	AI	MIPI CSI2 lane 3 data (+)
CSI2_LN3_N	545	AI	MIPI CSI2 lane 3 data (-)
CSI3_CLK_P	489	AI	MIPI CSI3 clock (+)
CSI3_CLK_N	495	AI	MIPI CSI3 clock (-)
CSI3_LN0_P	496	AI	MIPI CSI3 lane 0 data (+)

CSI3_LN0_N	502	AI	MIPI CSI3 lane 0 data (-)
CSI3_LN1_P	503	AI	MIPI CSI3 lane 1 data (+)
CSI3_LN1_N	509	AI	MIPI CSI3 lane 1 data (-)
CSI3_LN2_P	510	AI	MIPI CSI3 lane 2 data (+)
CSI3_LN2_N	515	AI	MIPI CSI3 lane 2 data (-)
CSI3_LN3_P	516	AI	MIPI CSI3 lane 3 data (+)
CSI3_LN3_N	521	AI	MIPI CSI3 lane 3 data (-)
CSI4_CLK_P	3	AI	MIPI CSI4 clock (+)
CSI4_CLK_N	2	AI	MIPI CSI4 clock (-)
CSI4_LN0_P	5	AI	MIPI CSI4 lane 0 data (+)
CSI4_LN0_N	4	AI	MIPI CSI4 lane 0 data (-)
CSI4_LN1_P	8	AI	MIPI CSI4 lane 1 data (+)
CSI4_LN1_N	7	AI	MIPI CSI4 lane 1 data (-)
CSI4_LN2_P	12	AI	MIPI CSI4 lane 2 data (+)
CSI4_LN2_N	11	AI	MIPI CSI4 lane 2 data (-)
CSI4_LN3_P	17	AI	MIPI CSI4 lane 3 data (+)
CSI4_LN3_N	16	AI	MIPI CSI4 lane 3 data (-)
CSI5_CLK_P	10	AI	MIPI CSI5 clock (+)
CSI5_CLK_N	9	AI	MIPI CSI5 clock (-)
CSI5_LN0_P	14	AI	MIPI CSI5 lane 0 data (+)
CSI5_LN0_N	13	AI	MIPI CSI5 lane 0 data (-)
CSI5_LN1_P	19	AI	MIPI CSI5 lane 1 data (+)
CSI5_LN1_N	18	AI	MIPI CSI5 lane 1 data (-)
CSI5_LN2_P	25	AI	MIPI CSI5 lane 2 data (+)
CSI5_LN2_N	24	AI	MIPI CSI5 lane 2 data (-)

CSI5_LN3_P	32	AI	MIPI CSI5 lane 3 data (+)
CSI5_LN3_N	31	AI	MIPI CSI5 lane 3 data (-)
CAM0_MCLK	15	DO	Master clock of camera 0
CAM1_MCLK	20	DO	Master clock of camera 1
CAM2_MCLK	26	DO	Master clock of camera 2
CAM3_MCLK	33	DO	Master clock of camera 3
CAM4_AON_MCLK	40	DO	Master clock of always on camera 4
CAM5_MCLK	47	DO	Master clock of camera 5
CAM6_MCLK	54	DO	Master clock of camera 6
CAM0_RST	69	DO	Reset of camera 0
CAM1_RST	76	DO	Reset of camera 1
CAM2_RST	83	DO	Reset of camera 2
CAM3_RST	68	DO	Reset of camera 3
CAM4_RST	75	DO	Reset of camera 4
CAM5_RST	82	DO	Reset of camera 5
CAM6_RST	89	DO	Reset of camera 6
CAM0_I2C_SDA	53	OD	I2C data of camera 0
CAM0_I2C_SCL	46	OD	I2C clock of camera 0
CAM1_I2C_SDA	74	OD	I2C data of camera 1
CAM1_I2C_SCL	67	OD	I2C clock of camera 1
CAM2_I2C_SDA	88	OD	I2C data of camera 2
CAM2_I2C_SCL	81	OD	I2C clock of camera 2
CAM3_I2C_SDA	101	OD	I2C data of camera 3
CAM3_I2C_SCL	95	OD	I2C clock of camera 3
CAM4_I2C_SDA	112	OD	I2C data of camera 4

CAM4_I2C_SCL	107	OD	I2C clock of camera 4
CAM_AON_I2C_SDA	121	OD	I2C data of always on camera
CAM_AON_I2C_SCL	117	OD	I2C clock of always on camera
CAM_I3C_SDA	102	OD	I3C data of camera
CAM_I3C_SCL	108	OD	I3C data of camera
VREG_L1M_1V05	29	PO	1.05 V output power for always on camera DVDD
VREG_L2M_1V05	36	PO	1.05 V output power for camera DVDD
VREG_L3M_2V8	43	PO	2.8 V output power for camera AVDD
VREG_L4M_2V8	30	PO	2.8 V output power for camera AVDD
VREG_L5M_1V8	37	PO	1.8 V output power for camera AVDD
VREG_L6M_1V8	52	PO	1.8 V output power for always on camera AVDD
VREG_L7M_2V8	59	PO	2.8 V output power for camera AVDD
VREG_L1N_1V1	50	PO	1.1 V output power for camera DVDD
VREG_L2N_1V1	57	PO	1.1 V output power for camera DVDD
VREG_L3N_2V8	64	PO	2.8 V output power for camera AVDD
VREG_L4N_2V8	44	PO	2.8 V output power for camera AVDD
VREG_L5N_1V8	51	PO	1.8 V output power for camera DOVDD
VREG_L6N_3V3	45	PO	3.3 V output power for TOF Camera
VREG_L7N_2V96	66	PO	2.96 V output power for camera AFVDD

The following is a reference design of camera 0 application:

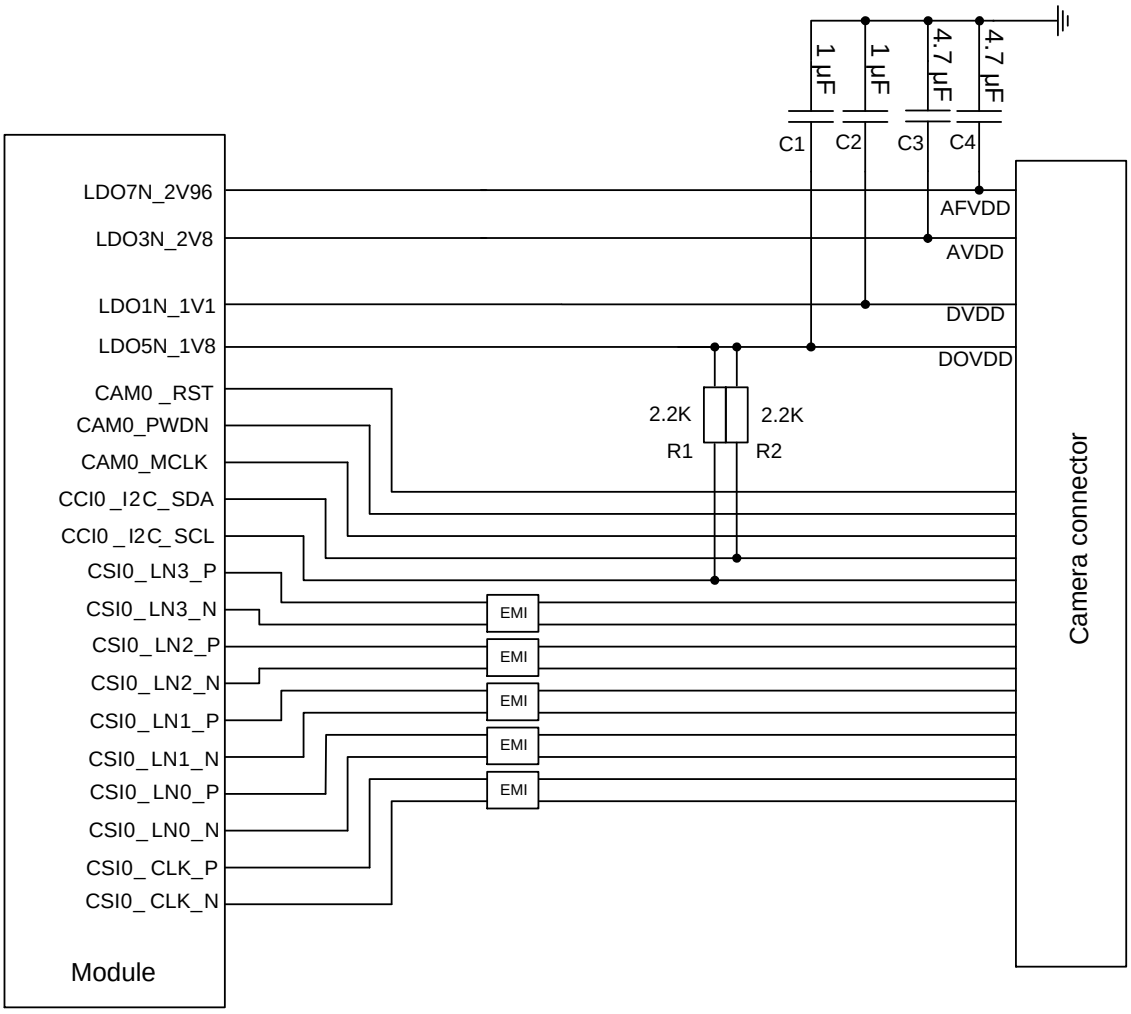


Figure 22: Reference Design of Camera 0 Application

NOTE

The reference design of CSI5, CSI4. CSI3, CSI2, CSI1 interface is similar to CSI0 interface.

4.11.1. MIPI Design Considerations

To ensure performance, the following principles should be complied with when designing LCM and camera interfaces:

- Special attention should be paid to the pin description of LCM and camera interfaces. Different video devices will have varied definitions for their corresponding connectors. Ensure that the devices and

the connectors are correctly connected.

- MIPI are high-speed signal traces, supporting maximum data rate up to 2.5 Gbps. The differential impedance should be controlled to 85 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB and do not cross it with other traces. For the same video device, keep all the MIPI traces be of the same length. To avoid crosstalk, a clearance of 1.5 times the trace width is recommended among MIPI signal traces. During impedance matching, do not connect MIPI signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a TVS of low capacitance for ESD protection and the recommended parasitic capacitance should be lower than 1 pF.
- Route MIPI traces according to the following requirements:
  a) The total trace length should be less than 150 mm with -6.5 dB total insertion loss and -3.5 dB cable insertion loss for 2.5 Gbps;
  b) Control the differential impedance to 85 Ω ±10 %;
  c) Control intra-lane length matching within 0.7 mm;
  d) Control inter-lane length matching within 1.4 mm.

Table 26: MIPI Trace Length Inside the Module (Unit: mm)

Pin No.	Pin Name	Length	Length Matching
485	DSI0_CLK_N	23.39	0.29
491	DSI0_CLK_P	23.10	
478	DSI0_LN0_N	22.98	0.20
484	DSI0_LN0_P	23.18	
471	DSI0_LN1_N	22.99	0.22
477	DSI0_LN1_P	23.21	
464	DSI0_LN2_N	23.05	0.05
470	DSI0_LN2_P	23.00	
457	DSI0_LN3_N	23.14	0.16
463	DSI0_LN3_P	23.30	
501	DSI1_CLK_N	18.07	0.26
507	DSI1_CLK_P	18.33	
494	DSI1_LN0_N	18.03	0.23
500	DSI1_LN0_P	18.26	

487	DSI1_LN1_N	18.04	0.27
493	DSI1_LN1_P	18.31	
480	DSI1_LN2_N	18.07	0.27
486	DSI1_LN2_P	18.34	
473	DSI1_LN3_N	18.27	0.24
479	DSI1_LN3_P	18.03	
505	CSI0_CLK_N	22.22	0.16
499	CSI0_CLK_P	22.38	
511	CSI0_LN0_N	22.23	0.01
506	CSI0_LN0_P	22.22	
517	CSI0_LN1_N	22.24	0.15
512	CSI0_LN1_P	22.39	
522	CSI0_LN2_N	22.22	0.18
518	CSI0_LN2_P	22.40	
527	CSI0_LN3_N	22.42	0.01
523	CSI0_LN3_P	22.41	
514	CSI1_CLK_N	23.10	0.22
519	CSI1_CLK_P	23.32	
520	CSI1_LN0_N	23.07	0.17
524	CSI1_LN0_P	23.24	
525	CSI1_LN1_N	23.16	0.11
529	CSI1_LN1_P	23.27	
530	CSI1_LN2_N	23.09	0.18
533	CSI1_LN2_P	23.27	
534	CSI1_LN3_N	23.27	0.01

537	CSI1_LN3_P	23.28	
535	CSI2_CLK_N	29.11	0.11
532	CSI2_CLK_P	29.22	
538	CSI2_LN0_N	29.28	0.15
536	CSI2_LN0_P	29.13	
541	CSI2_LN1_N	29.29	0.12
539	CSI2_LN1_P	29.17	
543	CSI2_LN2_N	29.38	0.24
542	CSI2_LN2_P	29.14	
545	CSI2_LN3_N	29.25	0.20
544	CSI2_LN3_P	29.05	
495	CSI3_CLK_N	17.28	0.11
489	CSI3_CLK_P	17.39	
502	CSI3_LN0_N	17.31	0.07
496	CSI3_LN0_P	17.24	
509	CSI3_LN1_N	17.34	0.14
503	CSI3_LN1_P	17.20	
515	CSI3_LN2_N	17.21	0
510	CSI3_LN2_P	17.21	
521	CSI3_LN3_N	17.42	0.17
516	CSI3_LN3_P	17.25	
2	CSI4_CLK_N	36.25	0.24
3	CSI4_CLK_P	36.01	
4	CSI4_LN0_N	36.20	0.17
5	CSI4_LN0_P	36.03	

7	CSI4_LN1_N	36.24	0.13
8	CSI4_LN1_P	36.11	
11	CSI4_LN2_N	36.24	0.20
12	CSI4_LN2_P	36.04	
16	CSI4_LN3_N	36.17	0.07
17	CSI4_LN3_P	36.24	
9	CSI5_CLK_N	24.33	0.05
10	CSI5_CLK_P	24.38	
13	CSI5_LN0_N	24.20	0.14
14	CSI5_LN0_P	24.34	
18	CSI5_LN1_N	24.20	0.22
19	CSI5_LN1_P	24.42	
24	CSI5_LN2_N	24.45	0.25
25	CSI5_LN2_P	24.20	
31	CSI5_LN3_N	24.14	0.03
32	CSI5_LN3_P	24.17	

Table 27: Mapping of CSI Data Rates and Trace Length (D-PHY)

Data Rates	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	76.2	-0.5	< 260
	152.4	-1.0	< 190
750 Mbps/lane	76.2	-0.7	< 210
	152.4	-1.15	< 155
1.0 Gbps/lane	76.2	-0.75	< 200
	152.4	-1.4	< 125

1.5 Gbps/lane	76.2	-0.9	< 145
	152.4	-1.8	< 60
2.1 Gbps/lane	76.2	-1.3	< 170
	152.4	-2.3	< 90
2.5 Gbps/lane	76.2	-2.1	< 210
	152.4	-3.5	< 150

Table 28: Mapping of DSI Data Rates and Trace Length (D-PHY)

Data Rates	Cable Length (mm)	Cable Insertion Loss (dB)	Trace Length (mm)
500 Mbps/lane	76.2	-0.8	< 280
	152.4	-1.4	< 210
750 Mbps/lane	76.2	-1.0	< 210
	152.4	-1.5	< 150
1.0 Gbps/lane	76.2	-1.1	< 200
	152.4	-1.7	< 100
1.5 Gbps/lane	76.2	-1.2	< 135
	152.4	-2.2	< 40
2.1 Gbps/lane	76.2	-1.6	< 150
	152.4	-2.8	< 80
2.5 Gbps/lane	76.2	-2.1	< 70
	152.4	-3.5	< 0

4.11.2. Flashlight Interfaces

The module supports 2 flash LED drivers. FLASH_LED1 and FLASH_LED2 are both with maximal output current up to 1.5 A per channel in flash mode and 300 mA in torch mode.

Table 29: Pin Definition of Flashlight Interfaces

Pin Name	Pin No.	I/O	Description	Comment
FLASH_LED1	420	AO	Flash/torch driver output 1	
FLASH_LED2	425	AO	Flash/torch driver output 2	
FLASH_STROBE	434	DI	Flash LED strobe	

A reference circuit design is shown below.

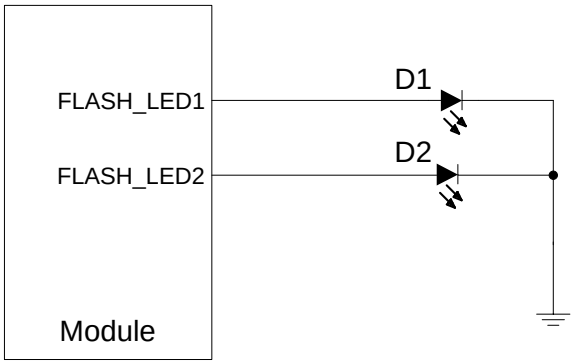


Figure 23: Reference Design for Flashlight Interfaces

4.12. Touch Panel Interfaces

The module provides 2 I2C interfaces for connection with Touch Panel (TP), and provides the corresponding power supply and interrupt pins.

Table 30: Pin Description of Touch Panel Interfaces

Pin Name	Pin No.	I/O	Description	Comment
TP0_RST	300	DO	TP0 reset	
TP0_INT	294	DI	TP0 interrupt	
TP0_I2C_SDA	200	OD	TP0 I2C data	
TP0_I2C_SCL	207	OD	TP0 I2C clock	
TP1_RST	63	DO	TP1 reset	

TP1_INT	70	DI	TP1 interrupt
TP1_I2C_SDA	49	OD	TP1 I2C data
TP1_I2C_SCL	56	OD	TP1 I2C clock

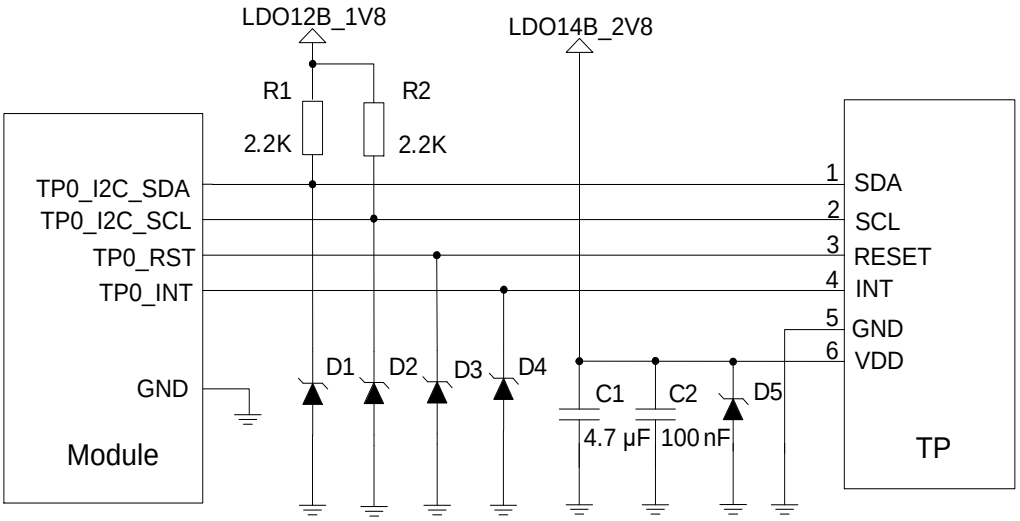


Figure 24: Reference Design of Touch Panel Interface

NOTE

The reference design of TP1 interface is similar to TP0 interface.

4.13. Motor Drive Interface

The module provides one motor drive interface:

Table 31: Pin Description of Motor Drive Interface

Pin Name	Pin No.	I/O	Description	Comment
HAP_P	394	AO	Haptics driver output (+)	
HAP_M	390	AO	Haptics driver output (-)	
HAP_SWR_RX_CLK	384	DO	Haptics SoundWire	

			receive clock
HAP_SWR_RX_DATA	389	DIO	Haptics SoundWire receive data

The motor is driven by a dedicated circuit, and a reference circuit is shown below:

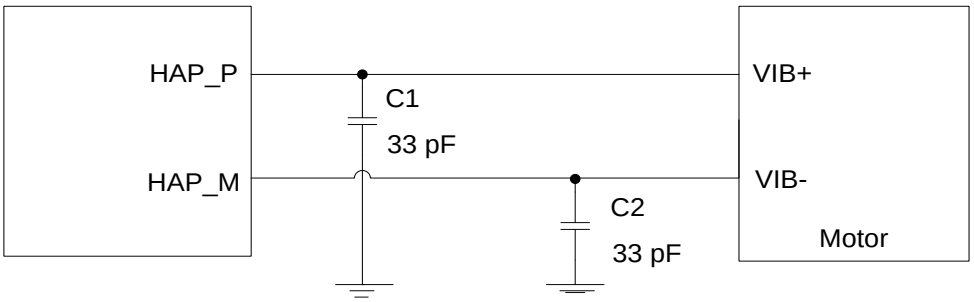


Figure 25: Reference Design of Motor Drive Interface

4.14. Sensor Interfaces

The module supports communication with sensors via I2C interfaces, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, light sensor, temperature sensor, pressure sensor.

Table 32: Pin Description of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C0_SDA	177	OD	I2C0 data for external sensor	
SENSOR_I2C0_SCL	170	OD	I2C0 clock for external sensor	
SENSOR_I2C1_SDA	91	OD	I2C1 data for external sensor	
SENSOR_I2C1_SCL	84	OD	I2C1 clock for external sensor	
SENSOR_I3C_SDA	142	OD	I3C data for external sensor	
SENSOR_I3C_SCL	139	OD	I3C clock for external sensor	

MAG_INT	349	DI	Magnetic sensor interrupt
HALL_INT	370	DI	Hall sensor interrupt
ALPS_INT	356	DI	Ambient light/proximity sensor interrupt
IMU_INT1	341	DI	IMU interrupt 1
IMU_INT2	334	DI	IMU interrupt 2

4.15. RGMII Interface

The module provides one RGMII interface, which can be connected with a PHY or MAC.

Table 33: Pin Description of RGMII Interface

Pin Name	Pin No.	I/O	Description	Comment
RGMII_RX0	266	DI	RGMII receive data bit 0	
RGMII_RX1	263	DI	RGMII receive data bit 1	
RGMII_RX2	259	DI	RGMII receive data bit 2	
RGMII_RX3	255	DI	RGMII receive data bit 3	
RGMII_RXC	271	DI	RGMII receive clock	
RGMII_RX_CTL	269	DI	RGMII receive control	
RGMII_TX0	268	DO	RGMII transmit data bit 0	
RGMII_TX1	265	DO	RGMII transmit data bit 1	
RGMII_TX2	262	DO	RGMII transmit data bit 2	
RGMII_TX3	258	DO	RGMII transmit data bit 3	
RGMII_TXC	272	DO	RGMII transmit clock	
RGMII_TX_CTL	270	DO	RGMII transmit control	
RGMII/SGMII /USXGMII1_RST_N	216	DO	Reset output for RGMI/SGMII/USXGMII1 PHY	

Table 34: RGMII Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)
266	RGMII_RX0	12.57
263	RGMII_RX1	13.05
259	RGMII_RX2	12.61
255	RGMII_RX3	12.40
271	RGMII_RXC	13.66
269	RGMII_RX_CTL	13.44
268	RGMII_TX0	15.49
265	RGMII_TX1	15.54
262	RGMII_TX2	15.51
258	RGMII_TX3	15.40
272	RGMII_TXC	15.61
270	RGMII_TX_CTL	15.47

4.16. SGMII&USXGMII Interfaces

The module includes two integrated Ethernet MAC with two SGMII/USXGMII management interfaces.

Table 35: Pin Description of SGMII&USXGMII Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SGMII/USXGMII0_CLK_M	239	DI	SGMII/USXGMII 0 clock (-)	
SGMII/USXGMII0_CLK_P	244	DI	SGMII/USXGMII 0 clock (+)	
SGMII/USXGMII0_RX_M	233	DI	SGMII/USXGMII 0 receive (-)	
SGMII/USXGMII0_RX_P	238	DI	SGMII/USXGMII 0 receive (+)	
SGMII/USXGMII0_TX_M	219	DO	SGMII/USXGMII 0 transmit (-)	

SGMII/USXGMII0_TX_P	225	DO	SGMII/USXGMII 0 transmit (+)
SGMII/USXGMII0_INT_N	206	DI	SGMII/USXGMII 0 interrupt
SGMII/USXGMII0_MDC	234	DO	SGMII/USXGMII 0 management data clock
SGMII/USXGMII0_MDIO	220	DIO	SGMII/USXGMII 0 management data input/output
SGMII/USXGMII0_RST_N	223	DO	Reset output for external PHY0
SGMII/USXGMII1_CLK_M	245	DI	SGMII/USXGMII 1 clock (-)
SGMII/USXGMII1_CLK_P	249	DI	SGMII/USXGMII 1 clock (+)
SGMII/USXGMII1_RX_M	226	DI	SGMII/USXGMII 1 receive (-)
SGMII/USXGMII1_RX_P	232	DI	SGMII/USXGMII 1 receive (+)
SGMII/USXGMII1_TX_M	212	DO	SGMII/USXGMII 1 transmit (-)
SGMII/USXGMII1_TX_P	218	DO	SGMII/USXGMII 1 transmit (+)
SGMII/USXGMII1_INT_N	199	DI	SGMII/USXGMII 1 interrupt
SGMII/USXGMII1_MDC	227	DO	SGMII/USXGMII 1 management data clock
SGMII/USXGMII1_MDIO	213	DIO	SGMII/USXGMII 1 management data input/output

Table 36: SGMII/USXGMII Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)	Length Difference (mm)
239	SGMII/USXGMII0_CLK_M	5.39	0.01
244	SGMII/USXGMII0_CLK_P	5.38	
233	SGMII/USXGMII0_RX_M	9.18	0.07
238	SGMII/USXGMII0_RX_P	9.11	
219	SGMII/USXGMII0_TX_M	10.46	0.09
225	SGMII/USXGMII0_TX_P	10.55	
245	SGMII/USXGMII1_CLK_M	10.36	0.01

249	SGMII/USXGMII1_CLK_P	10.35	
226	SGMII/USXGMII1_RX_M	9.99	0.09
232	SGMII/USXGMII1_RX_P	9.90	
212	SGMII/USXGMII1_TX_M	12.75	0.07
218	SGMII/USXGMII1_TX_P	12.82	

4.17. PCIe Interfaces

The module provides 3 integrated PCIe (Peripheral Component Interconnect Express) interfaces. PCIe 2, PCIe 3, and Ethernet functions cannot be used simultaneously with PCIe 1. The key features of the PCIe interfaces are mentioned below:

- *PCI Express Base Specification Revision 3.0* compliance.
- Data rate at 8 Gbps per lane.
- Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC.

Table 37: Pin Description of PCIe Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIE1_REFCLK_P	289	DO	PCIe1 reference clock (+)	
PCIE1_REFCLK_M	290	DO	PCIe1 reference clock (-)	
PCIE1_TX0_P	285	DO	PCIe1 transmit 0 (+)	
PCIE1_TX0_M	284	DO	PCIe1 transmit 0 (-)	
PCIE1_RX0_P	278	DI	PCIe1 receive 0 (+)	
PCIE1_RX0_M	277	DI	PCIe1 receive 0 (-)	
PCIE1_TX1_P	281	DO	PCIe1 transmit 1 (+)	
PCIE1_TX1_M	280	DO	PCIe1 transmit 1 (-)	
PCIE1_RX1_P	276	DI	PCIe1 receive 1 (+)	
PCIE1_RX1_M	275	DI	PCIe1 receive 1 (-)	

PCIE1_WAKE_N	243	DI	PCIe1 wake up
PCIE1_RST_N	237	DO	PCIe1 reset
PCIE1_CLKREQ_N	230	DI	PCIe1 clock request
PCIE2_REFCLK_P	241	DO	PCIe2 reference clock (+)
PCIE2_REFCLK_M	246	DO	PCIe2 reference clock (-)
PCIE2_TX0_P	252	DO	PCIe2 transmit 0 (+)
PCIE2_TX0_M	256	DO	PCIe2 transmit 0 (-)
PCIE2_RX0_P	261	DI	PCIe2 receive 0 (+)
PCIE2_RX0_M	264	DI	PCIe2 receive 0 (-)
PCIE2_TX1_P	247	DO	PCIe2 transmit 1 (+)
PCIE2_TX1_M	251	DO	PCIe2 transmit 1 (-)
PCIE2_RX1_P	257	DI	PCIe2 receive 1 (+)
PCIE2_RX1_M	260	DI	PCIe2 receive 1 (-)
PCIE2_WAKE_N	169	DI	PCIe2 wake up
PCIE2_RST_N	217	DO	PCIe2 reset
PCIE2_CLKREQ_N	288	DI	PCIe2 clock request
PCIE3_REFCLK_P	292	DO	PCIe3 reference clock (+)
PCIE3_REFCLK_M	291	DO	PCIe3 reference clock (-)
PCIE3_TX_P	283	DO	PCIe3 transmit (+)
PCIE3_TX_M	282	DO	PCIe3 transmit (-)
PCIE3_RX_P	287	DI	PCIe3 receive (+)
PCIE3_RX_M	286	DI	PCIe3 receive (-)
PCIE3_WAKE_N	162	DI	PCIe3 wake up
PCIE3_RST_N	210	DO	PCIe3 reset
PCIE3_CLKREQ_N	293	DI	PCIe3 clock request

Table 38: PCIe Trace Length Inside the Module

Pin No.	Pin Name	Length (mm)	Length Difference (mm)
289	PCIE1_REFCLK_P	46.63	0.60
290	PCIE1_REFCLK_M	46.04	
285	PCIE1_TX0_P	44.36	0
284	PCIE1_TX0_M	44.36	
278	PCIE1_TX1_P	49.43	0.29
277	PCIE1_TX1_M	49.14	
281	PCIE1_RX0_P	41.45	0.10
280	PCIE1_RX0_M	41.34	
276	PCIE1_RX1_P	39.41	0.14
275	PCIE1_RX1_M	39.55	
241	PCIE2_REFCLK_P	17.13	0.32
246	PCIE2_REFCLK_M	17.45	
252	PCIE2_TX0_P	12.04	0.22
256	PCIE2_TX0_M	12.26	
247	PCIE2_TX1_P	14.55	0.31
251	PCIE2_TX1_M	14.24	
261	PCIE2_RX0_P	11.02	0.25
264	PCIE2_RX0_M	10.77	
257	PCIE2_RX1_P	11.66	0.09
260	PCIE2_RX1_M	11.57	
292	PCIE3_REFCLK_P	28.31	0.25
291	PCIE3_REFCLK_M	28.56	
283	PCIE3_TX_P	18.93	0.45

282	PCIE3_TX_M	19.38	0.34
287	PCIE3_RX_P	28.22	
286	PCIE3_RX_M	28.56	

4.18. RGB Interfaces

The module provides 3 RGB interfaces, which are with maximal output current up to 12 mA.

Table 39: Pin Definition of RGB Interfaces

Pin Name	Pin No.	I/O	Description
R_LED	219	AO	Current source for red LED
G_LED	213	AO	Current source for green LED
B_LED	207	AO	Current source for blue LED

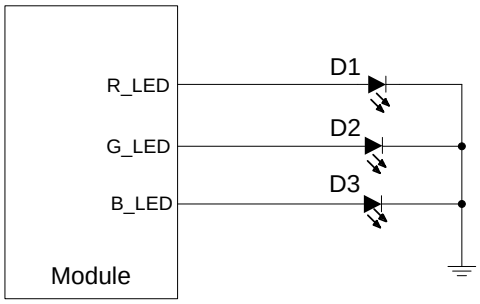


Figure 26: Reference Design for RGB Interfaces

4.19. GPIO

The module provides 50 GPIOs with the power domain of 1.8 V:

Table 40: Pin Description of GPIO

Pin Name	Pin No.	I/O	Description	Comment
GPIO_4	35	DIO	General-purpose input/output	
GPIO_5	28	DIO	General-purpose input/output	
GPIO_6	314	DIO	General-purpose input/output	
GPIO_7	321	DIO	General-purpose input/output	
GPIO_8	376	DIO	General-purpose input/output	
GPIO_9	380	DIO	General-purpose input/output	
GPIO_12	146	DIO	General-purpose input/output	
GPIO_15	374	DIO	General-purpose input/output	
GPIO_18	348	DIO	General-purpose input/output	
GPIO_19	328	DIO	General-purpose input/output	
GPIO_22	361	DIO	General-purpose input/output	
GPIO_23	362	DIO	General-purpose input/output	
GPIO_46	214	DIO	General-purpose input/output	
GPIO_47	221	DIO	General-purpose input/output	
GPIO_48	97	DIO	General-purpose input/output	
GPIO_49	113	DIO	General-purpose input/output	
GPIO_62	103	DIO	General-purpose input/output	
GPIO_68	124	DIO	General-purpose input/output	
GPIO_70	127	DIO	General-purpose input/output	
GPIO_71	111	DIO	General-purpose input/output	
GPIO_73	116	DIO	General-purpose input/output	
GPIO_88	209	DIO	General-purpose input/output	
GPIO_89	327	DIO	General-purpose input/output	

GPIO_90	320	DIO	General-purpose input/output
GPIO_91	313	DIO	General-purpose input/output
GPIO_137	186	DIO	General-purpose input/output
GPIO_142	336	DIO	General-purpose input/output
GPIO_143	315	DIO	General-purpose input/output
GPIO_144	322	DIO	General-purpose input/output
GPIO_146	306	DIO	General-purpose input/output
GPIO_147	343	DIO	General-purpose input/output
GPIO_150	156	DIO	General-purpose input/output
GPIO_151	163	DIO	General-purpose input/output
GPIO_152	335	DIO	General-purpose input/output
GPIO_153	342	DIO	General-purpose input/output
GPIO_154	329	DIO	General-purpose input/output
GPIO_155	224	DIO	General-purpose input/output
GPIO_156	231	DIO	General-purpose input/output
GPIO_157	301	DIO	General-purpose input/output
GPIO_159	308	DIO	General-purpose input/output
GPIO_160	386	DIO	General-purpose input/output
GPIO_162	355	DIO	General-purpose input/output
GPIO_163	350	DIO	General-purpose input/output
GPIO_177	150	DIO	General-purpose input/output
GPIO_198	155	DIO	General-purpose input/output
GPIO_206	185	DIO	General-purpose input/output
GPIO_207	178	DIO	General-purpose input/output
PM_GPIO_03	475	DIO	General-purpose input/output of PM

PM_GPIO_04	441	DIO	General-purpose input/output of PM
PM_GPIO_11	455	DIO	General-purpose input/output of PM

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to conduct a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Wi-Fi & Bluetooth

The module provides two shared antenna interfaces: ANT_WIFI/BT0 and ANT_WIFI/BT1 for Wi-Fi and Bluetooth functions. The impedance shall be kept as 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna or ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

Table 41: Pin Description of Wi-Fi & Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description
ANT_WIFI/BT0	130	AIO	Wi-Fi/Bluetooth antenna interface
ANT_WIFI/BT0	137	AIO	Wi-Fi/Bluetooth antenna interface

Table 42: Wi-Fi & Bluetooth Frequency (Unit: MHz)

Types	Frequency
Wi-Fi 802.11a/b/g/n/ac/ax/be	2412–2462 5150–5895 5925-7125
Bluetooth 5.3 LE	2402–2480

5.1.1. Wi-Fi Overview

The module supports for Wi-Fi 2 × 2 MU-MIMO, three-band 2.4 GHz, 5 GHz, 6 GHz and 7GHz functions. The module complies with the IEEE 802.11a/b/g/n/ac/ax/be standard and supports Dual Band Simultaneous (simultaneous) for dual MAC:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP and STA modes
- Support Wi-Fi Direct
- Support 2 × 2 Multi-User Multiple-Input Multiple-Output (MU-MIMO)
- Support tri-band 2.4 GHz, 5 GHz, 6 GHz and 7 GHz
- Support up to 4096 QAM modulation at each band
- Channel bandwidth up to 40 MHz at 2.4 GHz, up to 160 MHz at 5 GHz and up to 320 MHz at 6 GHz
- Dual Band Simultaneous (DBS) up to 2.4 GHz 2 × 2 40 MHz + 5 GHz 2 × 2 160 MHz/6 GHz 2 × 2 160 MHz
- High Band Simultaneous (HBS) up to 5 GHz/6 GHz 2 × 2 160 MHz + 5 GHz/6 GHz 2 × 2 160 MHz
- Up to 5.8 Gbps data rate (2 × 2 5 GHz 160 MHz + 2 × 2 6 GHz 160 MHz with 4K QAM modulation)
- MCS 0–MCS 7: HT20 and HT40
- MCS 0–MCS 7: HT20 and HT40
- MCS 0–MCS 8: VHT20
- MCS 0–MCS 9: VHT40 and VHT80
- MCS 0–MCS 11: HE20 and HE40 and HE80 and HE160
- MCS 0–MCS 13: EHT20 and EHT40 and EHT80 and EHT160 and EHT320

Table 43: Wi-Fi Transmitting Performance

Table 44: Wi-Fi Receiving Performance

Frequency	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-99 dbm
	802.11b	11 Mbps	-92 dbm
	802.11g	6 Mbps	-95 dbm
	802.11g	54 Mbps	-78 dbm
	802.11n HT20	MCS0	-92 dbm
	802.11n HT20	MCS7	-74 dbm

	802.11n HT40	MCS0	-90 dbm
	802.11n HT40	MCS7	-71 dbm
	802.11ax HE20	MCS0	-94 dbm
	802.11ax HE20	MCS11	-64 dbm
	802.11ax HE40	MCS0	-93 dbm
	802.11ax HE40	MCS11	-63 dbm
	802.11be HE20	MCS0	-94 dbm
	802.11be HE20	MCS11	-61 dbm
	802.11be HE40	MCS0	-91 dbm
	802.11be HE40	MCS11	-58 dbm
5 GHz	802.11a	6 Mbps	-90 dbm
	802.11a	54 Mbps	-73 dbm
	802.11n HT20	MCS0	-88 dbm
	802.11n HT20	MCS7	-69 dbm
	802.11n HT40	MCS0	-85 dbm
	802.11n HT40	MCS7	-66 dbm
	802.11ac VHT20	MCS0	-90 dbm
	802.11ac VHT20	MCS8	-66 dbm
	802.11ac VHT40	MCS0	-87 dbm
	802.11ac VHT40	MCS9	-61 dbm
	802.11ac VHT80	MCS0	-84 dbm
	802.11ac VHT80	MCS9	-58 dbm
	802.11ax HE20	MCS0	-89 dbm
	802.11ax HE20	MCS11	-61 dbm
	802.11ax HE40	MCS0	-88 dbm

	802.11ax HE40	MCS11	-58 dbm
	802.11ax HE80	MCS0	-86 dbm
	802.11ax HE80	MCS11	-52 dbm
	802.11ax HE160	MCS0	-83 dbm
	802.11ax HE160	MCS11	-54 dbm
	802.11be HE20	MCS0	-93 dbm
	802.11be HE20	MCS13	-54 dbm
	802.11be HE40	MCS0	-90 dbm
	802.11be HE40	MCS13	-53 dbm
	802.11be HE80	MCS0	-87 dbm
	802.11be HE80	MCS13	-49 dbm
	802.11be HE160	MCS0	-84 dbm
	802.11be HE160	MCS13	-46 dbm
6 GHz	802.11a	6 Mbps	-90 dbm
	802.11a	54 Mbps	-73 dbm
	802.11n HT20	MCS0	-88 dbm
	802.11n HT20	MCS7	-69 dbm
	802.11n HT40	MCS0	-85 dbm
	802.11n HT40	MCS7	-66 dbm
	802.11ac VHT20	MCS0	-90 dbm
	802.11ac VHT20	MCS8	-66 dbm
	802.11ac VHT40	MCS0	-87 dbm
	802.11ac VHT40	MCS9	-61 dbm
	802.11ac VHT80	MCS0	-84 dbm
	802.11ac VHT80	MCS9	-58 dbm

802.11ax HE20	MCS0	-89 dbm
802.11ax HE20	MCS11	-61 dbm
802.11ax HE40	MCS0	-88 dbm
802.11ax HE40	MCS11	-58 dbm
802.11ax HE80	MCS0	-86 dbm
802.11ax HE80	MCS11	-52 dbm
802.11ax HE160	MCS0	-83 dbm
802.11ax HE160	MCS11	-54 dbm
802.11be HE20	MCS0	-92 dbm
802.11be HE20	MCS13	-55 dbm
802.11be HE40	MCS0	-75 dbm
802.11be HE40	MCS13	-40 dbm
802.11be HE80	MCS0	-77 dbm
802.11be HE80	MCS13	-49 dbm
802.11be HE160	MCS0	-84 dbm
802.11be HE160	MCS13	-47 dbm
802.11be HE320	MCS0	-79 dbm
802.11be HE320	MCS13	-42 dbm

NOTE

The product complies with the IEEE specifications.

5.1.2. Bluetooth Overview

Models with built-in Bluetooth function provide Bluetooth antenna interfaces. The module supports Bluetooth 5.3 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulations. Supported characteristics include:

- Up to 7-lane wireless connections.

- Up to 3.5 Piconets simultaneously.
- One SCO or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 45: Bluetooth Data Rates and Versions

Versions	Data Rates (Mbit/s)	Maximum Application Throughput
1.2	1	> 80 kbit/s
2.0 + EDR	3	> 80 kbit/s
3.0 + HS	24	Refer to 3.0 + HS
4.0	24	Refer to 4.0 LE
5.1	TBD	Refer to 5.1 LE
5.2	TBD	Refer to 5.2 LE
5.3	TBD	Refer to 5.3 LE

Referenced specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016*

Table 46: Bluetooth Transmitting and Receiving Performance (Unit: dBm)

Receiving Performance			
Packet types	DH5	2-DH5	3-DH5
Receiving sensitivity	-96	-96	-89

5.1.3. Reference Design

A reference design of Wi-Fi & Bluetooth antenna interface is shown as below. C1 and C2 are not mounted by default. Only a 0 Ω resistor is mounted on R1.

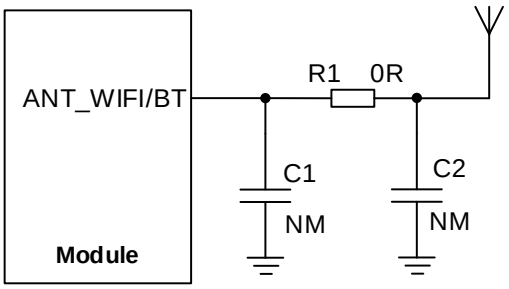


Figure 27: Reference Design of Wi-Fi & Bluetooth Antenna

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

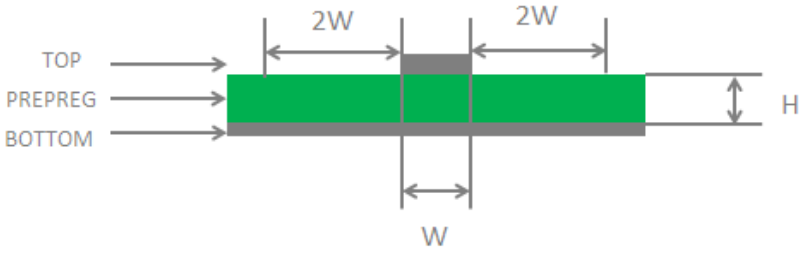


Figure 28: Microstrip Design on a 2-layer PCB

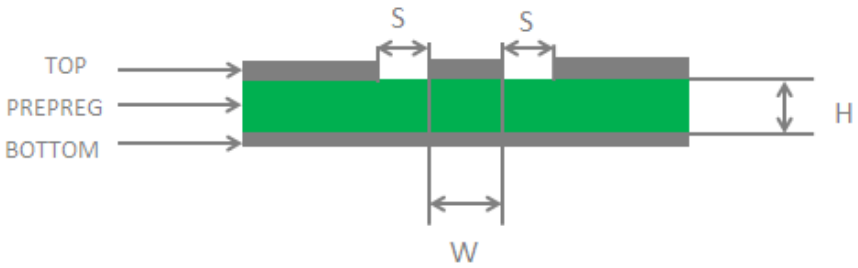


Figure 29: Coplanar Waveguide Design on a 2-layer PCB

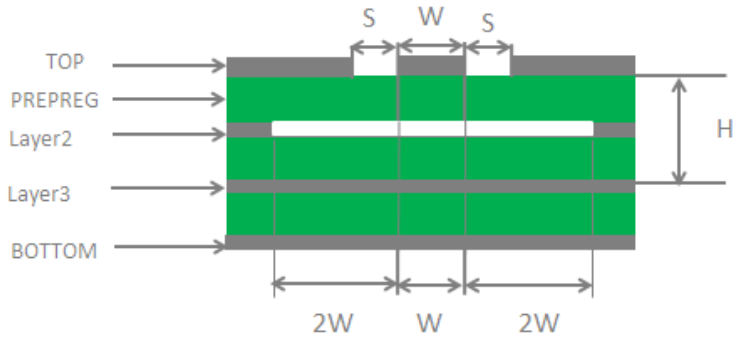


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

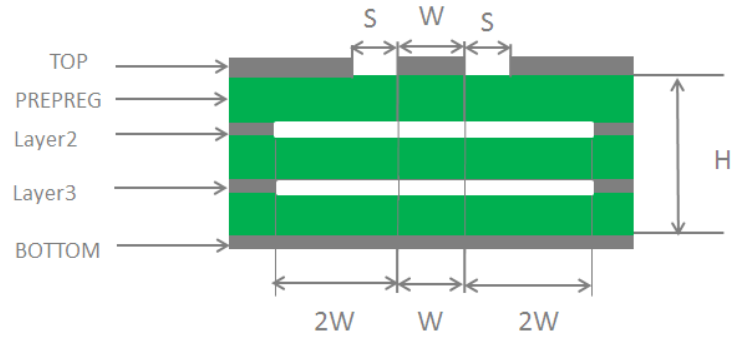


Figure 31: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [2]***.

5.3. Requirements for Antenna Design

Table 47: Requirements for Antenna Design

Antenna Types	Requirements
Wi-Fi & Bluetooth	VSWR: ≤ 2 Gain: 1 dBi Max input power: 50 W Input impedance: 50 Ω Vertical polarization Cable insertion loss: < 1 dB

5.4. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

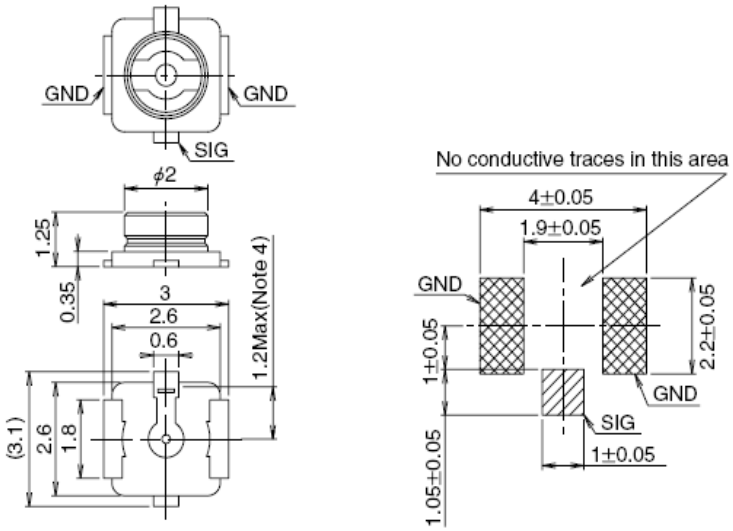


Figure 32: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

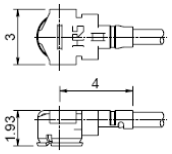
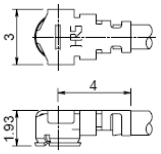
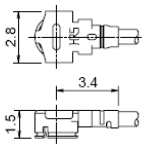
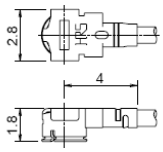
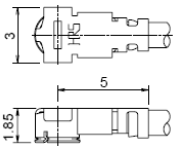
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 33: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

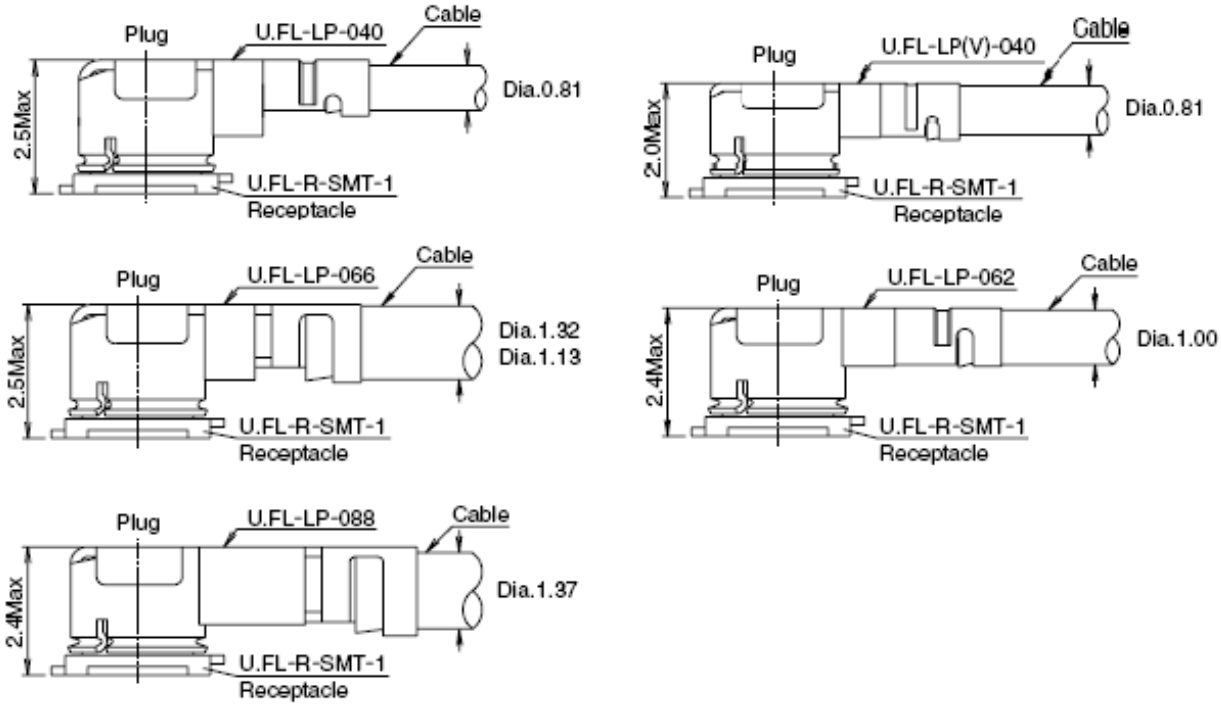


Figure 34: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 48: Absolute Maximum Ratings

Parameters	Min.	Max.	Units
Voltage at VBAT	-0.3	6	V
Voltage at USB_VBUS	-0.3	25	V
Voltage at digital pins	-0.3	2.09	V

6.2. Power Supply Ratings

Table 49: Module's Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Units
VBAT	Power supply for the module	The actual input voltages must stay between the minimum and maximum values.	3.55	3.8	4.4	V
USB_VBUS	Charging power input. Power supply for OTG device. USB/adaptor insertion detection	-	3.7	5.0	21.5	V

6.3. Power Consumption

Table 50: SG885G-WF Power Consumption

Modes	Conditions	Typ.	Units
OFF state	Power off	350	μA
Sleep state	Screen off	7	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact Quectel Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 51: 1.8 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.17	-
V_{IL}	Low-level input voltage	-	0.63
V_{OH}	High-level output voltage	1.35	-
V_{OL}	Low-level output voltage	-	0.45

Table 52: LDO15B_1V8 I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.17	-
V_{IL}	Low-level input voltage	-	0.63
V_{OH}	High-level output voltage	1.35	-

V_{OL}	Low-level output voltage	-	0.45

Table 53: SD Card 1.8 V I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	1.125	-
V_{IL}	Low-level input voltage	-	0.63
V_{OH}	High-level output voltage	1.53	-
V_{OL}	Low-level output voltage	-	0.225

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 54: ESD Characteristics (Temperature: 25–30 °C, Humidity: 45 ±5 %; Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT & GND	±8	±12
All antenna interfaces	±4	±8
Other interfaces	±0.5	±1

6.6. Operating and Storage Temperatures

Table 55: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature [4]	-30	+25	+75
Storage Temperature	-40	-	+90

[4] Within this range, the module's related indicators can meet 3GPP specifications.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

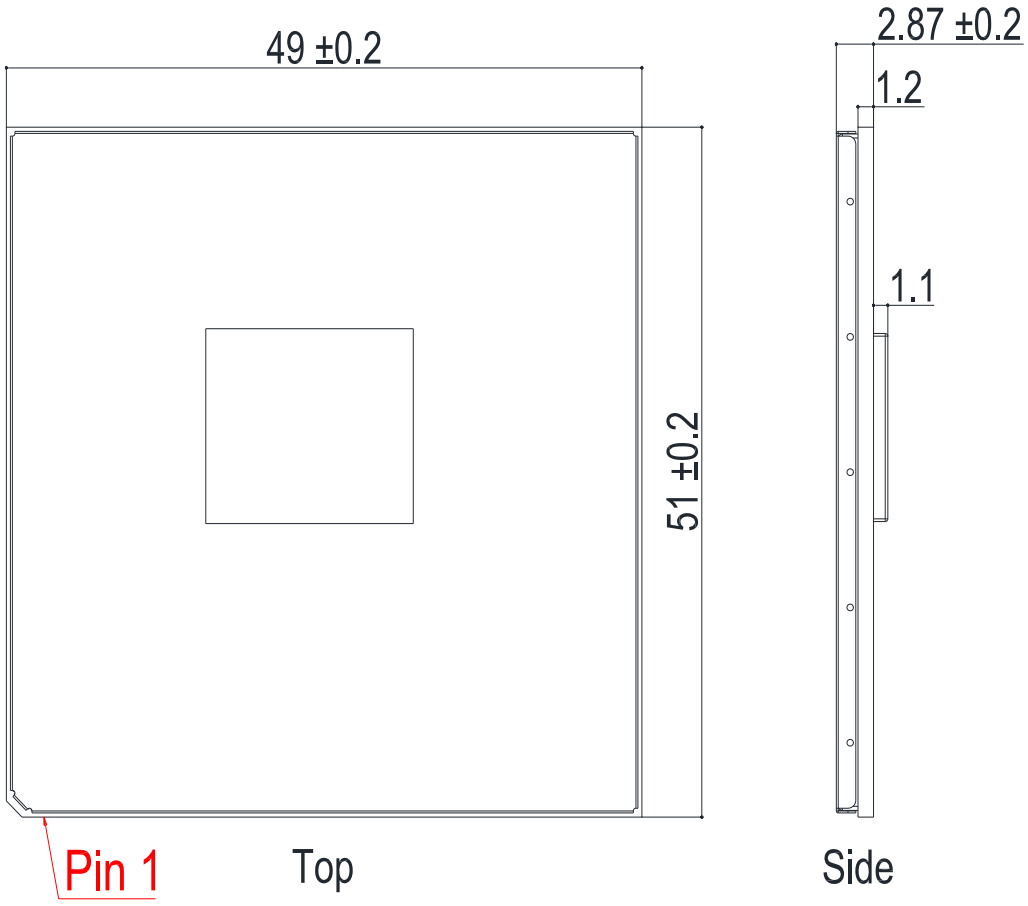


Figure 35: Top and Side Dimensions

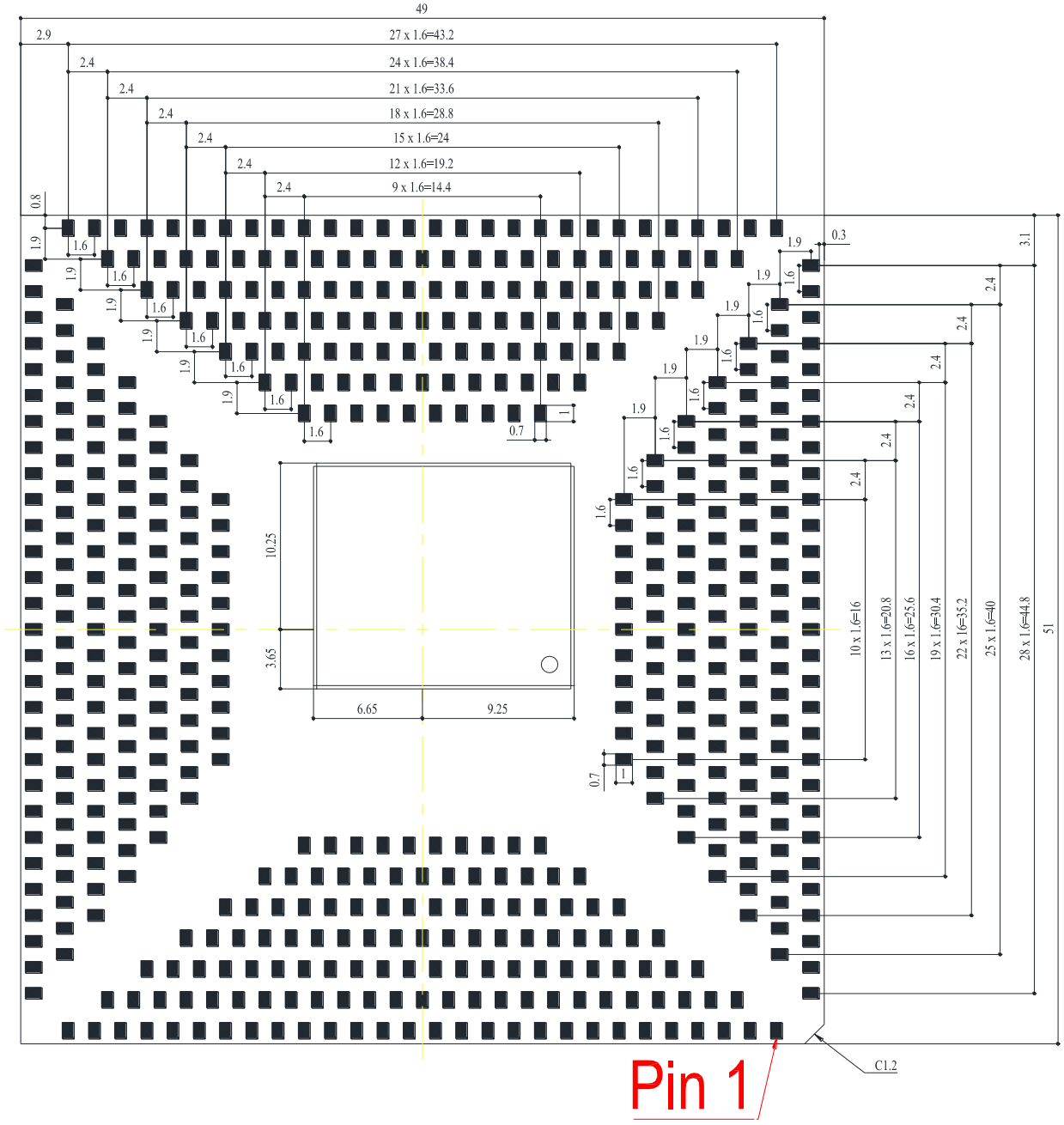


Figure 36: Bottom Dimension

NOTE

1. The package warpage level of the module refers to the *JEITA ED-7306* standard.
2. Reserve 0.7 mm distance from the hollow area on the bottom.

7.2. Recommended Footprint

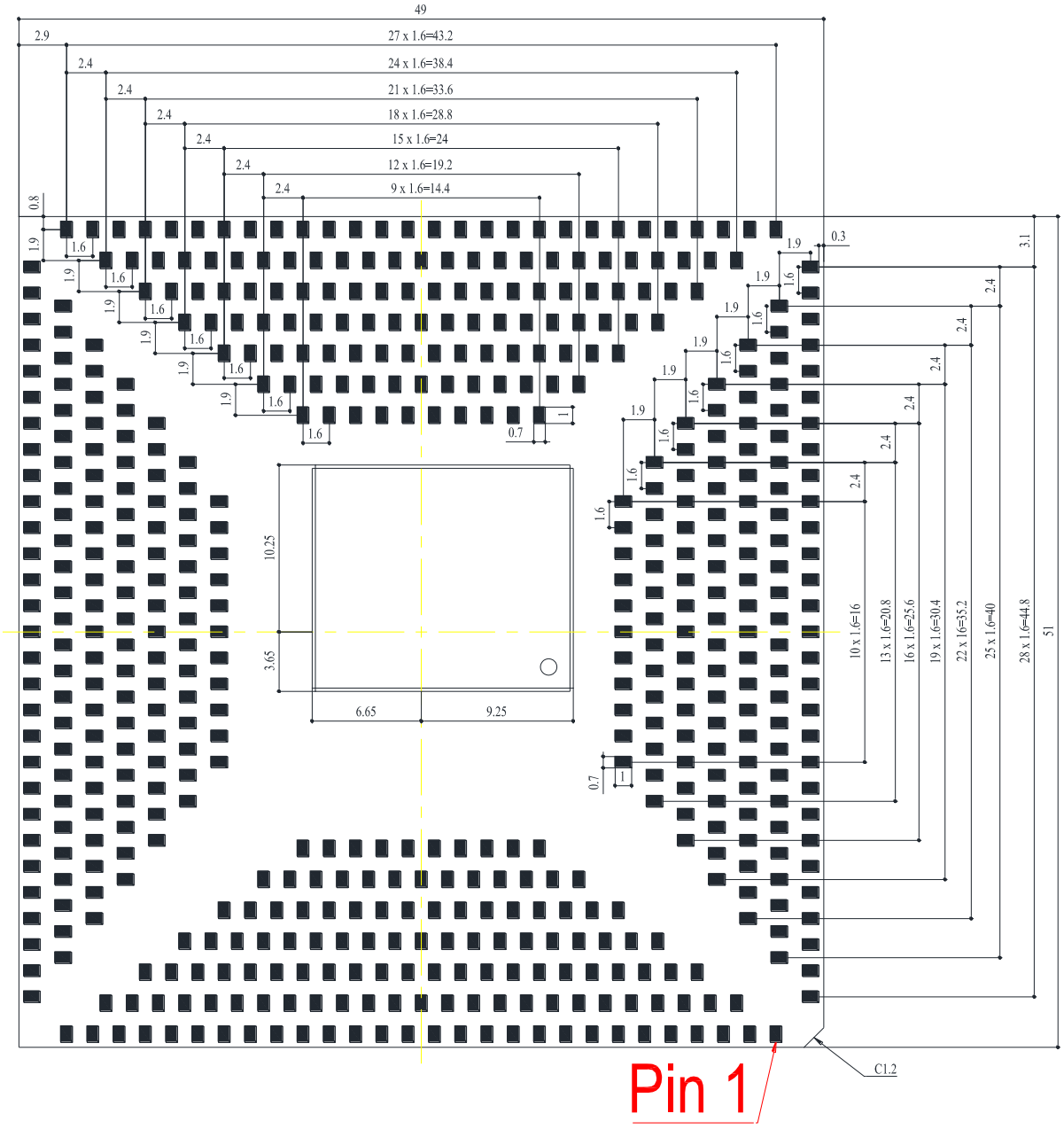


Figure 37: Recommended Footprint

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. Reserve 0.7 mm distance from the hollow area on the bottom.

7.3. Top and Bottom Views

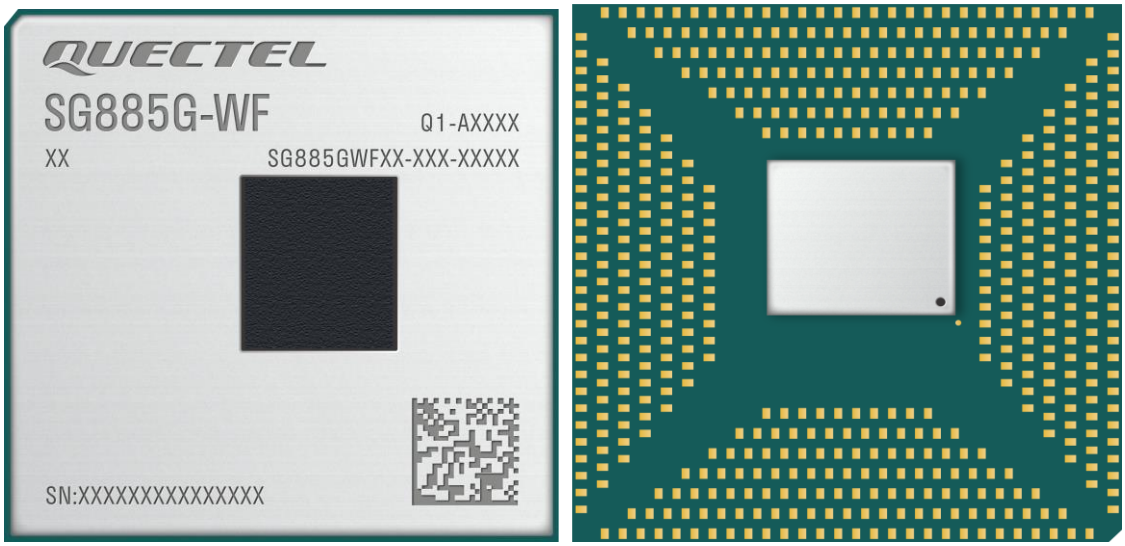


Figure 38: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended storage condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in recommended storage condition.

3. Floor life: 168 hours [5] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in recommended storage condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[5] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

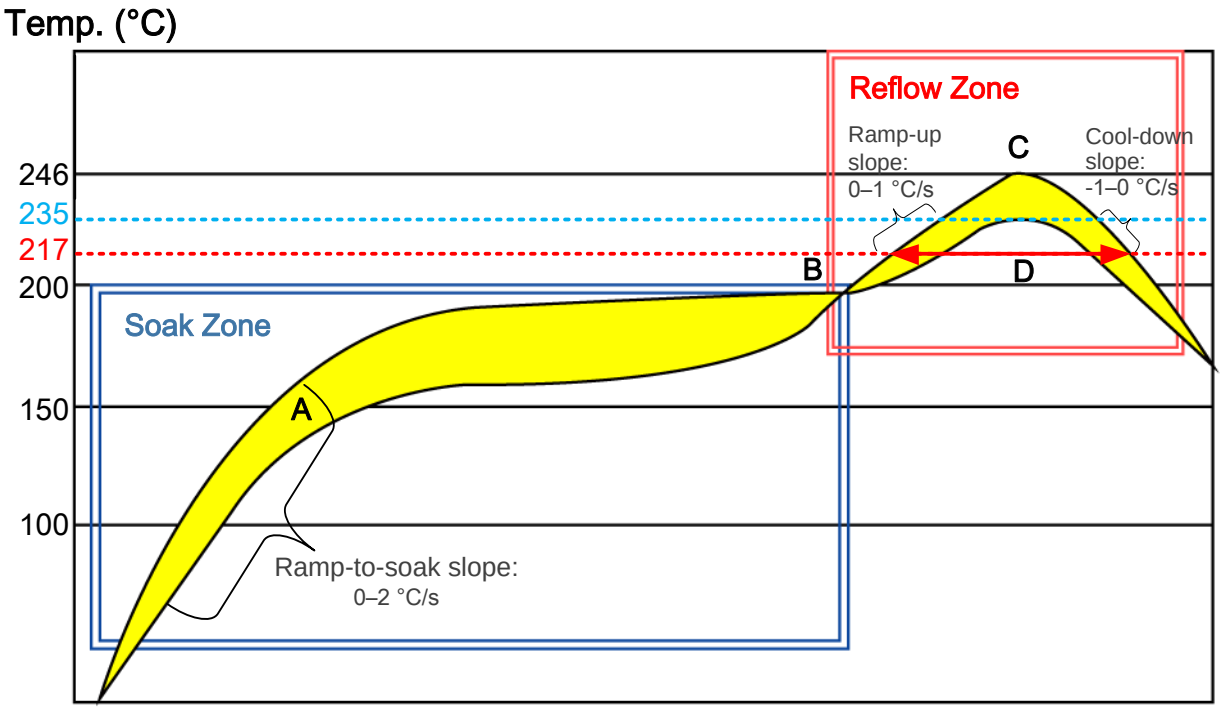


Figure 39: Recommended Reflow Soldering Thermal Profile

Table 56: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–2 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C Ramp-up Slope	0–1 °C/s
Reflow Time (D: over 217°C)	40–65 s
Max Temperature	235–246 °C
235–217 °C Cool-down Slope	-1–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, to avoid excessive temperature change, which may cause excessive thermal deformation of the metal shielding frame and cover, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste. If possible, please choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
3. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in ***document [3]***.

8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts injection tray packaging and details are as follow:

8.3.1. Injection Tray

Dimension details are as follow:

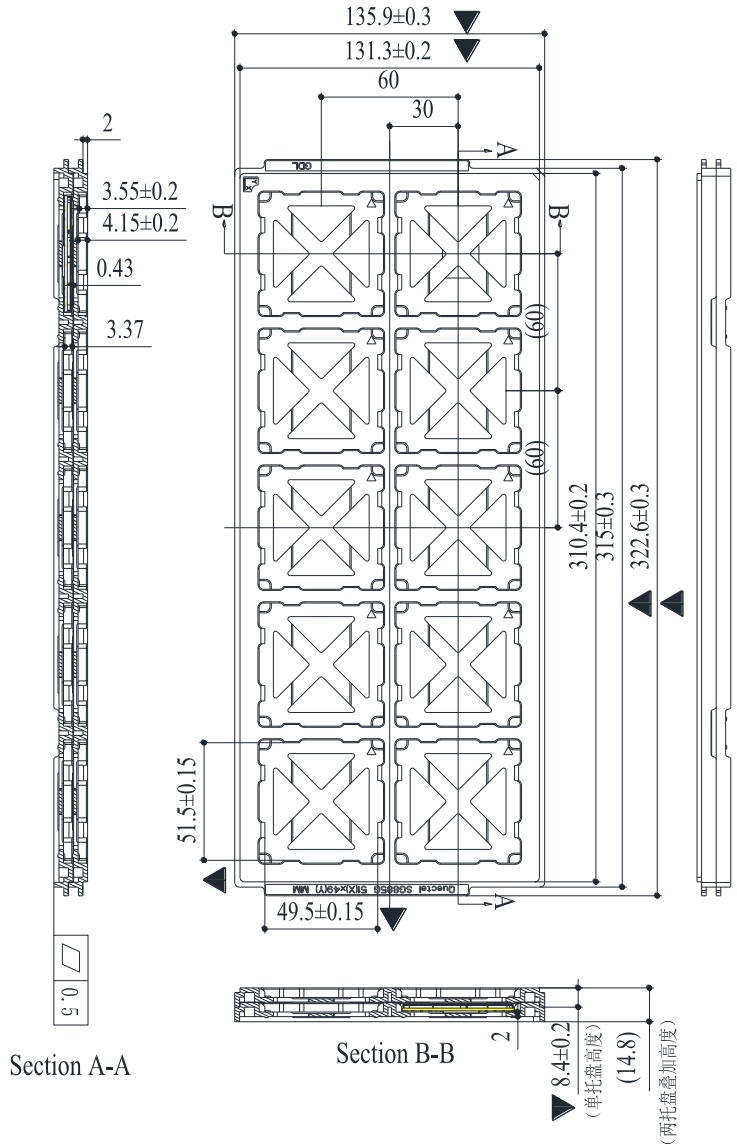
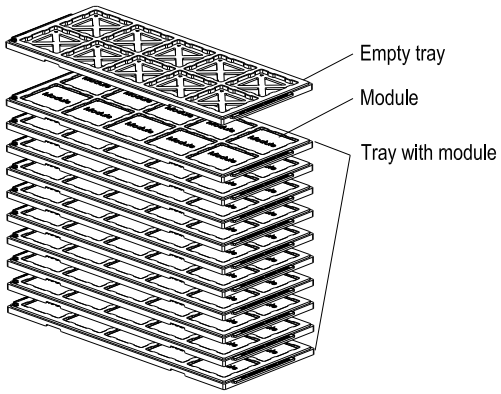
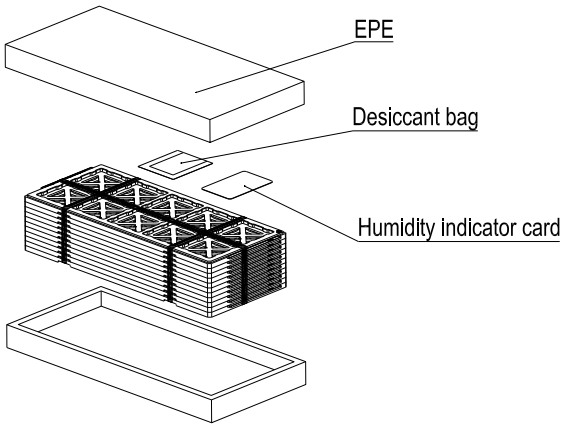


Figure 40: Injection Tray Dimension Drawing

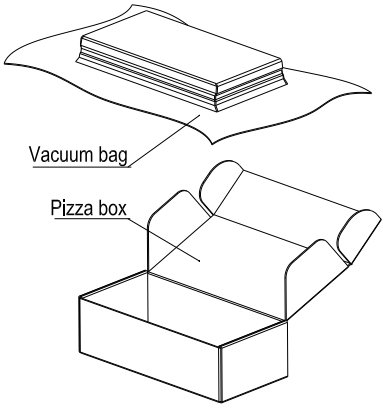
8.3.2. Packaging Process



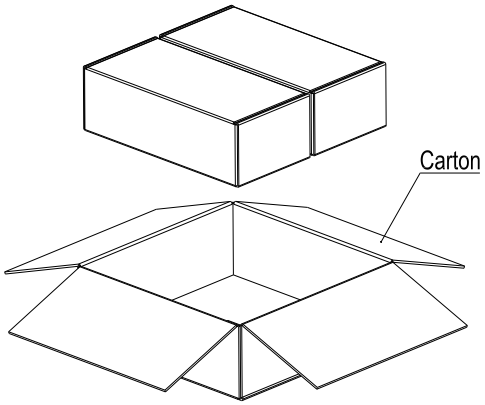
Each injection tray packs 10 modules. Stack 10 injection trays with modules together, and put 1 empty injection tray on the top.



Packing 11 injection trays together. Place 1 humidity indicator card and 1 desiccant bag on the top of injection tray, then put 2 EPE on the top and bottom of injection tray.



Put injection trays protected by EPE into vacuum bag, vacuumize it. Put the vacuum-packed injection trays into the pizza box. 1 pizza box can pack 100 modules.



Put 2 packaged pizza boxes into 1 carton box and then seal it. 1 carton box can pack 200 modules.

Figure 41: Packaging Process

9 Appendix References

Table 57: Related Documents

Document Name
[1] Quectel_Smart_EVB_G5_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_SMT_Application_Note

Table 58: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AON	Active Optical Network
AP	Application Processor
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data
CS2	Commercial Sample II
CTS	Clear To Send

DAI	Digital Audio Interface
DCE	Data Communications Equipment
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FEM	Front-End Module
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access

HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inorm	Normal Current
LAA	License Assisted Access
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated
NR	New Radio
NSA	Non-Stand Alone

PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SD	Secure Digital
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service

SoC	System on a Chip
SPI	Serial Peripheral Interface
STB	Set Top Box
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
$V_{IH}max$	Maximum High-level Input Voltage
$V_{IH}min$	Minimum High-level Input Voltage
$V_{IL}max$	Maximum Low-level Input Voltage
$V_{IL}min$	Minimum Low-level Input Voltage
$V_{I}max$	Absolute Maximum Input Voltage
$V_{I}min$	Absolute Minimum Input Voltage

V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network

10 Warning statements

The following notices is to guide host manufacturer integrating this module inside their final product with the FCC/ISED regulatory requirements.
When this module being integrated in any finished product(Host device) with 5.925-7.125GHz and 5.850-5.895GHz enabled, the following conditions must be met:
The operation of the host device is restricted to indoor use only. The host device must not have weatherized enclosure. The host device must use the integrated antennas. The host device must be powered by a wired connection and not by battery power. The host device must be labeled with "Contains FCC ID: XMR2023SG885GWF" alone with "Indoor Use Only".

10.1. FCC

1. Note EMI Considerations--Applicable
Note that a host manufacture is recommended to use D04 Module Integration Guide recommending as "best practice" RF design engineering testing and evaluation in case non-linear interactions generate additional non-compliant limits due to module placement to host components or properties.
For standalone mode, reference the guidance in D04 Module Integration Guide and for simultaneous mode7; see D02 Module Q&A Question 12, which permits the host manufacturer to confirm compliance.

10.1.1. Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.

2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

10.1.2. Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel（Contact: Jean Hu, E-mail: jean.hu@quectel.com）that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

10.1.3. End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2023SG885GWF”
“Contains IC: 10224A-023SG885GWF “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

10.1.4. Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

SG885G-WF: Dipole antenna		
Bluetooth	2402-2480	0.47
2.4G WIFI	2402-2462	0.47
5G WIFI U-NII-1	5150~5250 MHz	-0.67

5G WIFI U-NII-2A	5250~5350 MHz	-0.19
5G WIFI U-NII-2C	5470~5725 MHz	1.28
5G WIFI U-NII-3	5725~5850 MHz	1.1
6E	5850~5925MHz	3.48
6E	5925~6425MHz	3.76
6E	6425~6525MHz	3.62
6E	6525~6875MHz	2.66
6E	6875~7125MHz	2.2

note: The minimum Gain is 2.2dBi for CBP

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

10.1.5. Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

10.1.6. Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

10.1.7. List of applicable FCC rules

The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

a. FCC regulations restrict the operation of this device to indoor use only for 5.925-7.125GHz and 5.850-5.895GHz.

b. The operation of this device is prohibited on oil platforms, cars, trains, boats, and aircraft, except that operation of this device is permitted in large aircraft while flying above 10,000 feet in the 5.925-6.425 GHz band.

c. Operation of transmitters in the 5.925-7.125 GHz band is prohibited for control of or communications with
unmanned aircraft systems.

10.1.8. This device is intended only for OEM integrators under the following conditions:(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

10.1.9. Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

10.2. IC

10.2.1. Industry Canada Statement

a. 5850-5895MHz shall be indoor use only

5850-5895mhz sera usage d'intérieur seulement

b. 5925-7125MHz Operation shall be limited to indoor use only
l'opération sera limitée à l'usage d'intérieur seulement(5925-7125MHz)

c. Operation on oil platforms, automobiles, trains, maritime vessels and aircraft shall be prohibited except for on large aircraft flying above 3,048 m (10,000 ft).
l'exploitation sur les plates-formes pétrolières, les automobiles, les trains, les navires maritimes et les aéronefs doit être interdite, sauf à bord des gros aéronefs volant au-dessus de 3 048 m (10 000 pieds)

This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

10.2.2. Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

10.2.3. Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

10.2.4. RSS-247 Section 6.4 (5) (6) (for local area network devices, 5GHz)

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
The maximum antenna gain permitted for devices in the bands 5250–5350 MHz and 5470–5725 MHz shall comply with the e.i.r.p. limit; and

The maximum antenna gain permitted for devices in the band 5725–5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;
Le gain d'antenne maximal autorisé pour les dispositifs dans les bandes 5250-5350 MHz et 5470-5725 MHz doit être conforme à la norme e.r.p. limite; et
Le gain d'antenne maximal autorisé pour les appareils de la bande 5725-5825 MHz doit être conforme à la norme e.i.r.p. les limites spécifiées pour un fonctionnement point à point et non point à point, selon le cas.

10.2.5. This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

10.2.6. Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

10.2.7. IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

10.2.8. NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

10.2.9. End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-023SC696SWF”.

10.2.10. Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-023SG885GWF".

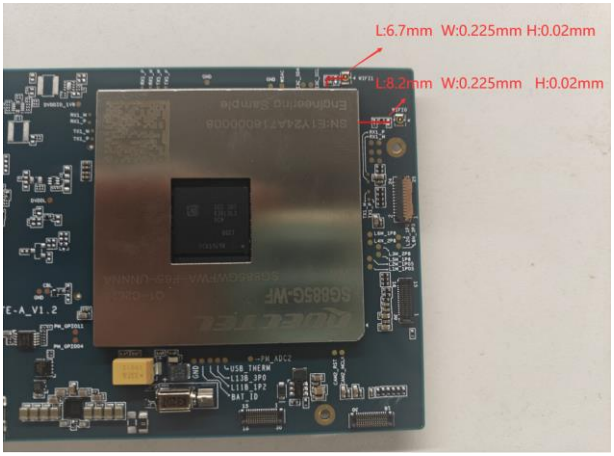
10.2.11. Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

10.2.12. Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

10.3. Trace design



10.4. Dielectric constant, and Impedance

No.	Design resistance	Impedance tolerance	Signal layer	Ground plane	type	Metric unit: micron (μm)		Management and control objectives	
						High frequency circuit design value			
						Line width	Line spacing	esistance valu	allowance
1	30Ω	10%	L1	L2	peculiarity	124		30Ω	±5Ω
2	50Ω	10%	L1	L2	peculiarity	79		50Ω	±5Ω
3	50Ω	10%	L1	L3	peculiarity	229		50Ω	±5Ω
4	85Ω	10%	L1	L2	difference	81	99	85Ω	±8.5Ω
5	90Ω	10%	L1	L2	difference	69	97	90Ω	±9Ω
6	100Ω	10%	L1	L2	difference	50	97	100Ω	±10Ω
7	30Ω	10%	L11	L12/L10	peculiarity	94		30Ω	±5Ω
8	50Ω	10%	L11	L12/L10	peculiarity	42		50Ω	±5Ω
9	85Ω	10%	L11	L12/L10	difference	53	82	85Ω	±8.5Ω
10	100Ω	10%	L11	L12/L10	difference	41	159	100Ω	±10Ω
11	30Ω	10%	L12	L13/L11	peculiarity	94		30Ω	±5Ω
12	50Ω	10%	L12	L13/L11	peculiarity	42		50Ω	±5Ω
13	85Ω	10%	L12	L13/L11	difference	53	82	85Ω	±8.5Ω
14	30Ω	10%	L13	L14/L12	peculiarity	94		30Ω	±5Ω
15	85Ω	10%	L13	L14/L12	difference	53	82	85Ω	±8.5Ω
16	100Ω	10%	L13	L14/L12	difference	41	159	100Ω	±10Ω
17	30Ω	10%	L3	L2/L4	peculiarity	94		30Ω	±5Ω
18	50Ω	10%	L3	L2/L4	peculiarity	42		50Ω	±5Ω
19	85Ω	10%	L3	L2/L4	difference	53	82	85Ω	±8.5Ω
20	90Ω	10%	L3	L2/L4	difference	49	96	90Ω	±9Ω
21	100Ω	10%	L3	L2/L4	difference	41	159	100Ω	±10Ω

22	30Ω	10%	L5	L4/L6	peculiarity	94		30Ω	±5Ω
23	50Ω	10%	L5	L4/L6	peculiarity	42		50Ω	±5Ω
24	85Ω	10%	L5	L4/L6	difference	54	81	85Ω	±8.5Ω
25	90Ω	10%	L5	L4/L6	difference	49	96	90Ω	±9Ω
26	100Ω	10%	L5	L4/L6	difference	42	159	100Ω	±10Ω
27	50Ω	10%	L7	L6/L8	peculiarity	76		50Ω	±5Ω
28	30Ω	10%	L9	L10/L8	peculiarity	94		30Ω	±5Ω
29	50Ω	10%	L9	L10/L8	peculiarity	44		50Ω	±5Ω
30	85Ω	10%	L9	L10/L8	difference	55	80	85Ω	±8.5Ω
31	90Ω	10%	L9	L10/L8	difference	50	90	90Ω	±9Ω
32	100Ω	10%	L9	L10/L8	difference	43	157	99Ω	±10Ω

stratum	Simulated thickness (finished thickness UM)	Stack diagram	Standard thickness	PP, CORE model	材料名	Material name	DF	Residual copper rate of each layer		TG	TD	Z-axis Expansion (50-260°C)	Composition utilization rate
								Make up	Single pcs				
	20	Image	20		PSR2000 CE811 TIBL3	4.1	0.02			≥230℃	≥430℃	1.30%	72.73%
L1	33		33	0.012				65.09%	72.75%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L2	20		20	0.012				76.34%	88.83%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L3	20		20	0.012				69.47%	79.20%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L4	20		20	0.012				78.74%	92.20%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L5	20		20	0.012				70.16%	80.02%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L6	19		19	0.012				77.56%	90.44%				
	53		53	#1067 RC71%	EM-526B	3.48	0.006						
L7	14		14					71.16%	81.10%				
	254		254	0.254mm H/H	EM-526	3.84	0.005						
L8	14		14					73.46%	84.39%				
	53		53	#1067 RC71%	EM-526B	3.48	0.006						
L9	19		19	0.012				71.54%	81.94%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L10	20		20	0.012				75.41%	87.51%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L11	20		20	0.012				72.94%	84.00%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L12	20		20	0.012				74.95%	86.86%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L13	20		20	0.012				74.73%	86.19%				
	51		51	#1067 RC71%	EM-526B	3.48	0.006						
L14	33		33	0.012				57.12%	61.46%				
	20		20		PSR2000 CE811 TIBL3	4.1	0.02						
		Gauge thickn	1.2±0.12mm										
Total	SR-SR	1202	Pt-Pt	1162									