QUECTEL

SG560D Series

Hardware Design

Smart Module Series

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Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

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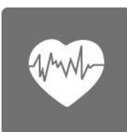
Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-05-13	Xiaomeng GUO/ Chris ZHANG	Creation of the document
1.0	2022-06-22	Xiaomeng GUO/ Chris ZHANG	First official release
1.1	2023-02-10	Waller GUO/ Jamie SHI/ Xiaomeng GUO	1. Added n3, n5, and n8 for SG560D-CN (Table 3, Table 6, Table 36, Table 38, Table 42 and Table 56). 2. Updated the video decode speed (Table 4). 3. Updated the NSA and SA maximum transmission rate of the 5G NR features (Table 4) 4. Updated the TBD data of the Rx sensitivity (Table 41 and Table 42). 5. Updated the TBD data of GNSS performance (Table 46). 6. Updated the GNSS antenna design requirement: changed from VSWR: < 2 to VSWR: ≤ 2 (Table 52). 7. Updated the TBD data of the power consumption (Table 55 and Table 56). 8. Updated the recommended reflow soldering thermal profile, the recommended thermal profile parameters and related notes (Chapter 8.2). 9. Updated the UART multiplexing relationship (Chapter 4.5 & 4.9).

2.0	2024-03-05	Cheney ZHANG/ Waller GUO/ Andy ZHANG/ Leon GONG	1. Updated the applicable modules to SG560D-CE, SG560D-EM, SG560D-NA and SG560D-WF. 2. Updated the reference circuit for GNSS passive antenna and GNSS active antenna (Figure 29 and Figure 30).

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1 Introduction

This document defines the SG560D series module and describes its air interfaces and hardware interfaces which are connected to your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

2 Product Overview

SG560D is a series of smart 5G module based on Android operating system, and provides industrial grade performance. It supports up to 4K video encoding/decoding, DMIC, built-in high performance Adreno™ 643 GPU, abundant GPIO interfaces as well as external audio codec. With these, the module is engineered to meet the demanding requirements in M2M applications. Related information and details are listed in the table below:

Table 2: Brief Introduction of the Module

SG560D Series	
Packaging	LGA
Pin Number	636
Dimensions	(42.5 ±0.2) mm × (56.5 ±0.2) mm × (2.95 ±0.2) mm
Weight	Approx. 17.5 g
Wireless Network Functions [1]	5G NR, LTE-FDD, LTE-TDD, DC-HSDPA, HSPA+, HSDPA, HSUPA, WCDMA, GSM and EDGE
Variants	SG560D-CE, SG560D-EM, SG560D-NA and SG560D-WF

[1] GSM/EDGE bands are only supported by SG560D-EM.

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	SG560D-CE	SG560D-EM	SG560D-NA	SG560D-WF
5G NR NSA	n41/n78/n79	n1/n3/n5/n7/n8/n20/n28/n38/n40/ n41/n77/n78/n79	n2/n5/n7/n12/n13/n14/n25/n26/ n30/n38/n41/n48/n66/n70/n71/n77/n78	-
5G NR SA	n1/n3/n5/n8/n28/n41/n78/ n79	n1/n3/n5/n7/n8/n20/n28/n38/n40/n41/ n78/n79	n2/n5/n7/n12/n13/n14/n25/n26/n29/ n30/n38/n41/n48/n66/n70/n71/n77/n78	-
LTE-FDD	B1/B3/B5/B8	B1/B2/B3/B4/B5/B7/B8/B12/B17/B18/ B19/B20/B26/B28/B32	B2/B4/B5/B7/B12/B13/B14/B17/B25/ B26/B29/B30/B66/B71	-
LTE-TDD	B34/B38/B39/B40/B41	B34/B38/B39/B40/B41/B42	B38/B41/B42/B43/B48/B46	-
WCDMA	B1/B5/B8	B1/B2/B4/B5/B6/B8/B19	-	-
GSM/EDGE	-	GSM850/EGSM900/DCS1800/ PCS1900	-	-
GNSS (optional)	GPS/GLONASS/BDS/ Galileo/NavIC/SBAS/QZSS; L1 + L5	GPS/GLONASS/BDS/Galileo/NavIC/ SBAS/QZSS; L1 + L5	GPS/GLONASS/BDS/Galileo/NavIC/ SBAS/QZSS; L1 + L5	-
Wi-Fi	802.11a/b/g/n/ac/ax	802.11a/b/g/n/ac/ax	802.11a/b/g/n/ac/ax	802.11a/b/g/n/ ac/ax
Bluetooth	Bluetooth 5.2 (BR/EDR + BLE)	Bluetooth 5.2 (BR/EDR + BLE)	Bluetooth 5.2 (BR/EDR + BLE)	Bluetooth 5.2 (BR/EDR + BLE)

2.2. Key Features

Table 4: Key Features

Parameter	Details
Application Processor	Customized octa-core 64-bit ARMv8-compliant Kryo 670 CPU with 2 MB L3 cache ● 1 × Kryo Gold Plus (high performance) core @ 2.7 GHz with 256 KB L2 cache ● 3 × Kryo Gold (high performance) cores @ 2.4 GHz with 256 KB L2 cache ● 4 × Kryo Silver (low power) cores @ 1.9 GHz with 128 KB L2 cache
Modem system	● 5G NR: 3GPP Rel-15 ● LTE: 3GPP Rel-15
GPU	Adreno™ 643, up to 812 MHz
Memory	**SG560D-CE/SG560D-EM/SG560D-NA:** 4 GB LPDDR4X + 64 GB UFS **SG560D-WF:** ● 4 GB LPDDR4X + 64 GB UFS (Default) ● 6 GB LPDDR4X + 128 GB UFS (Optional) ● 8 GB LPDDR4X + 128 GB UFS (Optional)
Operating System	Android 13
Power Supply	● Supply voltage: 3.55–4.4 V ● Typical supply voltage: 4.0 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
LCM Interface	● Supports one 4-lane MIPI DSI, up to 2.5 Gbps/lane ● FHD + (1200 × 2520) @ 144 fps based on MIPI standard ● Supports Wi-Fi miracast 4K @ 60 fps
Camera Interfaces	● Supports four 4-lane MIPI CSI, up to 2.5 Gbps/lane ● Supports up to 5 cameras ● 3 × ISP: up to 3 × 27 MP @ 24 fps or 3 × 22 MP @ 30 fps; 36 MP + 27 MP @ 24 fps or 36 MP + 22 MP @ 30 fps; 36 MP @ 30 fps
Video Codec [2]	● Video decoding: up to 4K @ 60 fps for H.264/H.265/VP9 ● Video encoding: up to 4K @ 30 fps for H.264/H.265 ● Video decoding and encoding: 1080P @ 60 fps decoding + 1080P @

[2] Audio codec and video codec listed in this table are dedicated for codec inside the CPU.

	60 fps encoding or 4K @ 30 fps decoding + 1080P @ 30 fps encoding
Audio Codec [2]	● EVRC, EVRC-B, EVRC-WB, G.711, G.729, PCM, EVS ● GSM-FR, GSM-EFR, GSM-HR ● AMR-NB, AMR-WB, QCELP
Audio Interfaces [3]	Three digital microphone inputs
(U)SIM Interfaces	● Two (U)SIM interfaces ● Supports 1.8/2.95 V (U)SIM card ● Supports Dual SIM Dual Standby by default
ADC Interfaces	● Six general-purpose ADC interfaces ● Supports up to 15-bit resolution
Real Time Clock	Supported
USB Interfaces	Supports two USB interfaces: USB0 and USB1 **USB0 function:** ● Compliant with USB 3.1 Gen 1 and USB 2.0 specifications, with transmission rates up to 5 Gbps on USB 3.1 and 480 Mbps on USB 2.0 ● Supports USB OTG ● Used for AT command communication, data transmission, software debugging, firmware upgrade and voice over USB **USB1 function:** ● Compliant with USB 2.0 specifications, with transmission rate up to 480 Mbps ● Only support host mode (external VBUS power supply is needed)
DisplayPort Interface	● Supports DisplayPort 1.4 function through USB0_SS1 and USB0_SS2 ● Supports up to 4K (3840 × 2160) @ 60 fps ● USB 3.1 and DisplayPort 1.4 can work concurrently
PCIe Interface	Supports 2-lane PCIe Gen 3, up to 8 Gbps
SD Card Interface	● Supports SD 3.0 protocol ● Supports 1.8/2.95 V SD card ● Supports SD card hot-plug
UART Interfaces [4]	Supports up to eleven UART interfaces, two of them are default configurations and nine of them can be multiplexed from other interfaces ● Default UART interfaces: UART and DBG_UART – UART: 4-wire UART interface, supports RTS and CTS hardware flow control, up to 4 Mbps – DBG_UART: 2-wire UART interface, dedicated for debugging ● For details about nine UART interfaces that can be multiplexed from other interfaces, see ***Table 23***

[3] An external codec should be added via I2S interface when audio output function is needed.
[4] For details about the multiplexing and conflict relationships of UART, I2C and SPI interfaces, see ***Table 23***.

SPI Interfaces [4]	Supports up to ten SPI interfaces, one of them is default configuration and nine of them can be multiplexed from other interfaces ● The default SPI supports master mode only ● For details about nine SPI interfaces that can be multiplexed from other interfaces, see ***Table 23***
I2C Interfaces [4]	Supports up to sixteen I2C interfaces ● Five of them are dedicated I2C interfaces used for camera and sensor peripherals ● Three of them are generic I2C interfaces that can be used for TP and NFC peripherals ● For details about eight I2C interfaces that can be multiplexed from other interfaces, see ***Table 23***
I2S Interfaces	Supports up to five I2S interfaces ● Two I2S interfaces are default configurations ● For details about three I2S interfaces that can be multiplexed from other interfaces, see ***Table 24***
Bluetooth Features	● Supports *Bluetooth Core Specification Version 5.2* ● Supports Bluetooth Classic & BLE
GNSS Features (optional)	● GPS/GLONASS/BDS/Galileo/NavIC/SBAS/QZSS ● L1 + L5
Antenna Interface	● ANT0, ANT1, ANT2, ANT3 and ANT4 ● ANT_GNSS ● ANT_WIFI/BT and ANT_WIFI_MIMO
Transmitting Power	● Class 4 (33 dBm ±2 dB) for EGSM900 & GSM850 ● Class 1 (30 dBm ±2 dB) for DCS1800 & PCS1900 ● Class E2 (27 dBm ±3 dB) for EGSM900 & GSM850 8-PSK ● Class E2 (26 dBm ±3 dB) for DCS1800 & PCS1900 8-PSK ● WCDMA bands: Class 3 (23 dBm ±2 dB) ● LTE HPUE [5] band (B41): Class 2 (26 dBm ±2 dB) ● Other LTE bands: Class 3 (23 dBm ±2 dB) ● 5G NR HPUE [5] bands (n41/n77/n78/n79): Class 2 (26 dBm +2/-3 dB) ● Other 5G NR bands: Class 3 (23 dBm ±2 dB)
5G NR Features	● Supports 3GPP Rel-15 FDD and TDD ● Supported modulation types: – Uplink: π/2-BPSK, QPSK, 16QAM, 64QAM and 256QAM – Downlink: QPSK, 16QAM, 64QAM and 256QAM ● Supports Multi-User MIMO – Uplink 2 × 2 MIMO [6]: **SG560D-EM:** n38/n40/n41/n77/n78/n79 **SG560D-NA:** n38/n41/n48/n77/n78 – Downlink 4 × 4 MIMO:

[5] HPUE only supports single carrier.
[6] Uplink 2 × 2 MIMO is supported only in 5G TDD SA mode.

	SG560D-CE: n1/n41/n78/n79 **SG560D-EM:** n1/n3/n7/n38/n40/n41/n77/n78/n79 **SG560D-NA:** n2/n7/n25/n30/n38/n41/n48/n66/n70/n77/n78 ● Supports SCS 15 kHz and 30 kHz [7] ● Supports SA and NSA operation modes ● Supports Option 3x, Option 3a, Option 3 and Option 2 ● Maximum transmission rate: **SG560D-CE:** – NSA: 2.5 Gbps (DL)/ 550 Mbps (UL) – SA: 2.1 Gbps (DL)/ 450 Mbps (UL) **SG560D-EM/SG560D-NA:** – NSA: 2.5 Gbps (DL)/ 550 Mbps (UL) – SA: 2.1 Gbps (DL)/ 900 Mbps (UL) ● SRS: **SG560D-CE:** – NSA: 1T4R (n41/n78/n79) – SA: 1T4R (n41/n78/n79) **SG560D-EM:** – NSA: 1T4R (n38/n40/n41/n77/n78/n79) – SA: 2T4R (n38/n40/n41/n77/n78/n79) **SG560D-NA:** – NSA: 1T4R (n38/n41/n48/n77/n78) – SA: 2T4R (n38/n41/n48/n77/n78)
LTE Features	● Support 3GPP Rel-15 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports Multi-User MIMO – Downlink 4 × 4 MIMO: **SG560D-CE:** B1/B41 **SG560D-EM:** B1/B3/B7/B38/B40/B41/B42 **SG560D-NA:** B2/B4/B7/B25/B30/B38/B66/B41/B42/B43/B48 ● Supports modulation types: – Uplink QPSK, 16QAM, 64QAM and 256QAM – Downlink QPSK, 16QAM, 64QAM and 256QAM ● Maximum transmission rate: 1.2 Gbps (DL)/ 200 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-9 ● Supports QPSK, 16QAM and 64QAM modulation ● DC-HSDPA: Max. 42 Mbps (DL) ● HSUPA: Max. 5.76 Mbps (UL) ● WCDMA: Max. 384 kbps (DL)/ 384 kbps (UL)
GSM Features [8]	● Class 4 (33 dBm ±2 dB) for EGSM900 & GSM850 ● Class 1 (30 dBm ±2 dB) for DCS1800 & PCS1900 ● Class E2 (27 dBm ±3 dB) for EGSM900 & GSM850 8-PSK

[7] 5G NR FDD bands only support 15 kHz SCS. 5G NR TDD bands only support 30 kHz SCS.
[8] GSM/EDGE bands are only supported by SG560D-EM.

	● Class E2 (26 dBm ±3 dB) for DCS1800 & PCS1900 8-PSK ● EDGE: Max. 296 kbps (DL)/ 236.8 kbps (UL) ● GPRS: Max. 107 kbps (DL)/ 85.6 kbps (UL)
WLAN Features	● Supports Wi-Fi 6E ● Supports AP and STA modes ● 2.4 GHz, 5 GHz and 6 GHz, supports 802.11a/b/g/n/ac/ax, up to 3.6 Gbps
Temperature Range	● Operating Temperature Range [9]: -35 °C to +75 °C ● Storage Temperature Range: -40 °C to +90 °C
Firmware Upgrade	Upgrade via USB or OTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power Management
- Battery Charge and Management
- Radio Frequency
- Baseband
- Memory (LPDDR4X + UFS flash)
- Peripheral Interface
  - USB Interfaces
  - (U)SIM Interfaces
  - SD Card Interface
  - GPIO Interfaces
  - UART Interfaces
  - I2C Interfaces
  - SPI Interface
  - I2S Interfaces
  - ADC Interfaces
  - LCM (MIPI) Interface
  - Touch Panel Interface
  - Camera (MIPI) Interfaces
  - Sensor Interfaces
  - Forced Download Interface
  - PCIe Interface
  - NFC Interface*

[9] Within operating temperature range, the module is 3GPP compliant.

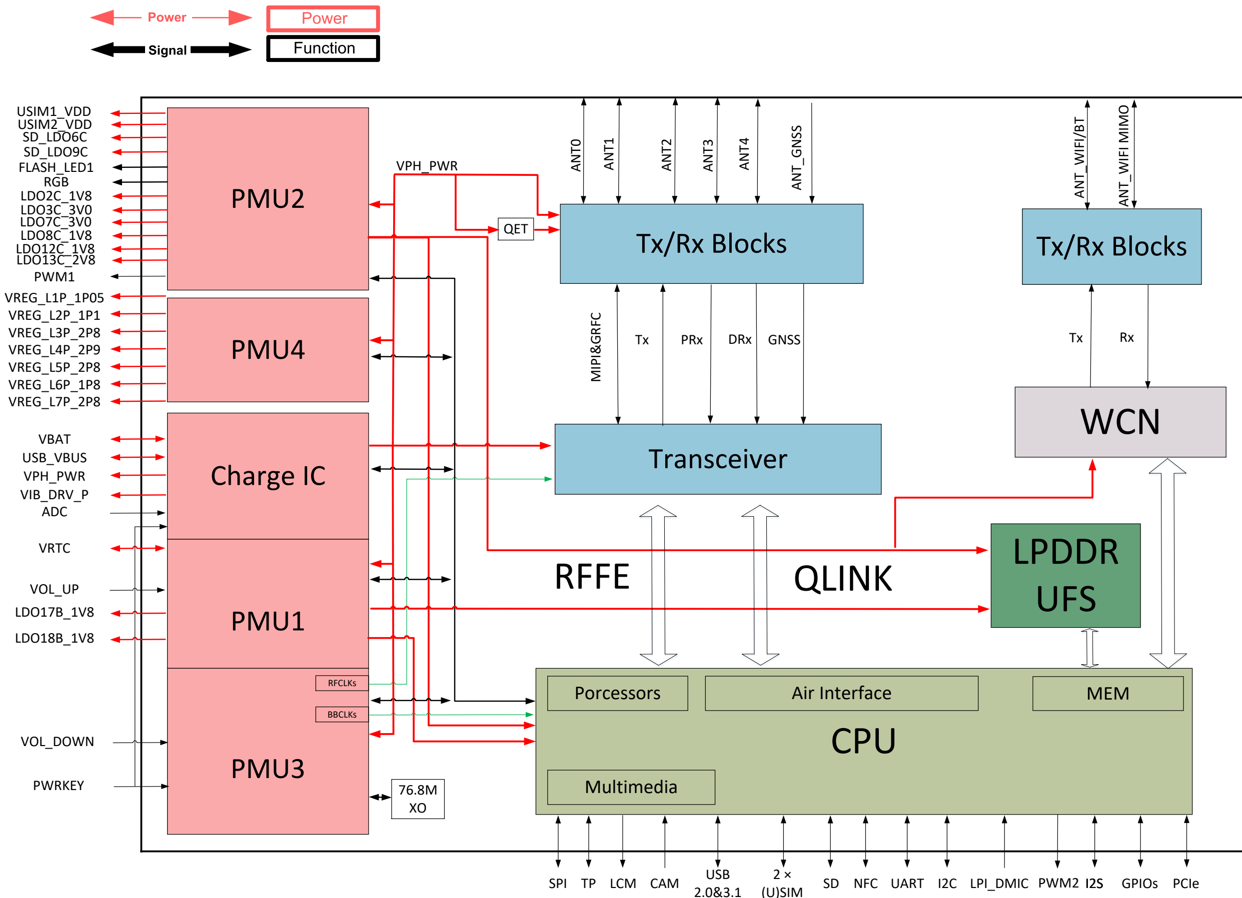


Figure 1: Functional Diagram

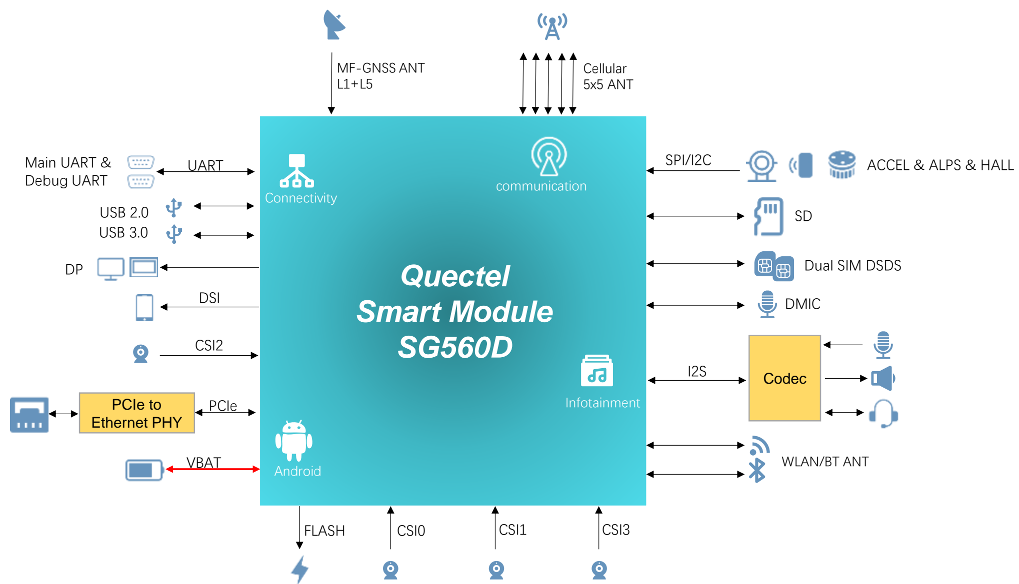


Figure 2: Application Block Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

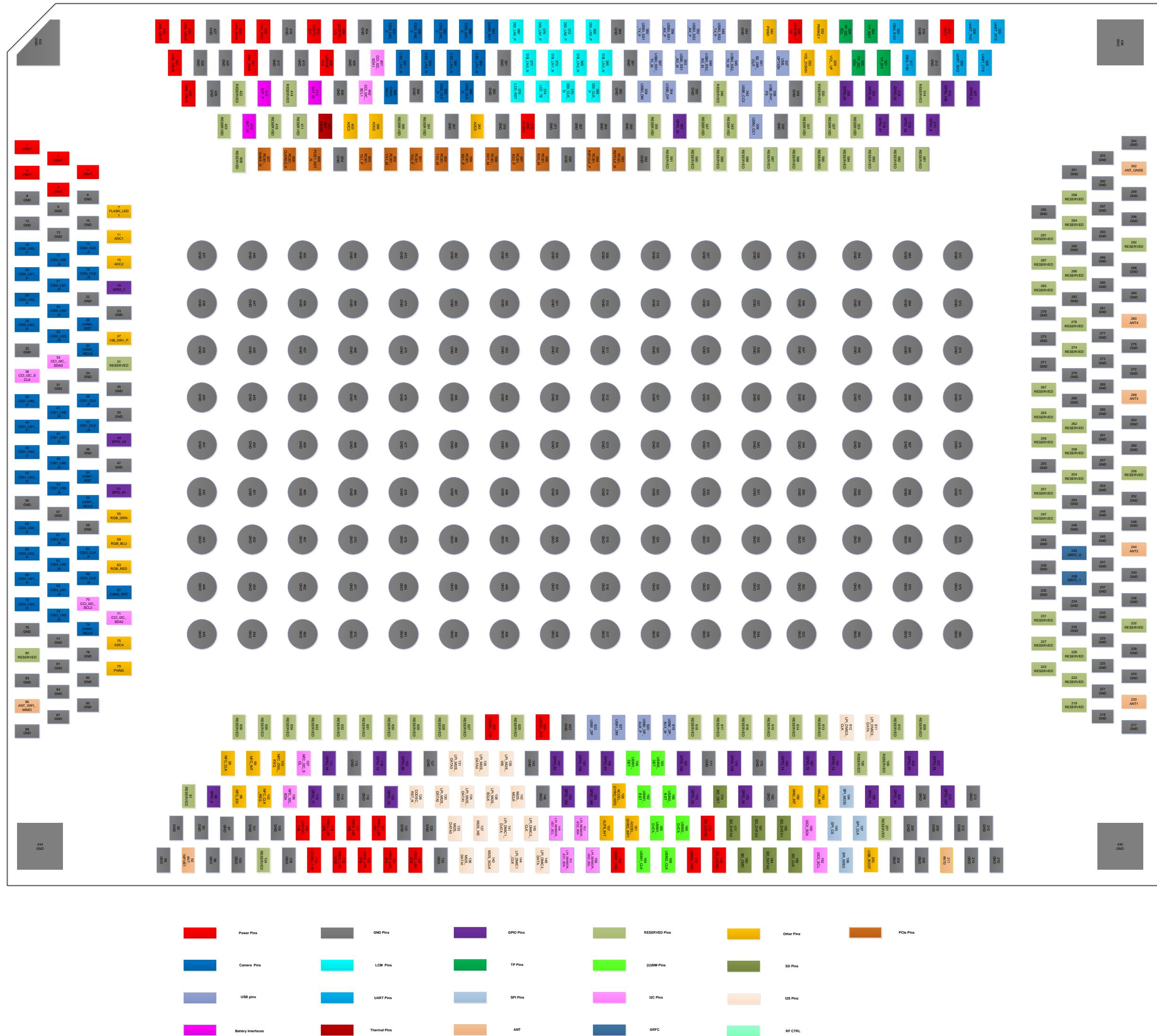


Figure 3: Pin Assignment

NOTE

1. Keep all RESERVED pins unconnected.
2. All GND pins should be connected to the ground unless otherwise specified.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
AO	Analog Output
DI	Digital Input
DIO	Digital Input/Output
DO	Digital Output
OD	Open Drain
PI	Power Input
PIO	Power Input/Output
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	1–5	PIO	Power supply for the module	Vmin = 3.55 V Vnom = 4.0 V Vmax = 4.4 V	It must be able to provide sufficient current up to 5.0 A. It is suggested to add a TVS diode for surge protection.
VPH_PWR	420, 421, 424	PO	Power supply for peripherals	Vnom = VBAT $I_O$max = 1500 mA	Keep on. 1.5 A in total.

LDO7C_3V0	412	PO	3.0 V output power for sensors and TP	Vnom = 3.0 V $I_O$max = 600 mA	When using it, it is recommended to add 1–4.7 μF bypass capacitors with a total capacitance not exceeding 18.8 μF.
LDO13C_2V8	409	PO	2.8 V output power for LCM	Vnom = 2.8 V $I_O$max = 150 mA	When using it, it is recommended to add 1–4 μF bypass capacitors with a total capacitance not exceeding 4 μF.
LDO18B_1V8	336	PO	1.8 V output power for I/O pull-up	Vnom = 1.8 V $I_O$max = 20 mA	Keep on. When using it, it is recommended to add 1–4.7 μF bypass capacitors with a total capacitance not exceeding 14.1 μF.
LDO17B_1V8	408	PO	1.8 V output for I/O power supply	Vnom = 1.8 V $I_O$max = 600 mA	When using it, it is recommended to add 1–4.7 μF bypass capacitors with a total capacitance not exceeding 18.8 μF.
LDO12C_1V8	109	PO	1.8 V output for I/O power supply of LCM	Vnom = 1.8 V $I_O$max = 150 mA	When using it, it is recommended to add 1–4 μF bypass capacitors with a total capacitance not exceeding 4 μF.
LDO8C_1V8	112	PO	1.8 V output power for sensors	Vnom = 1.8 V $I_O$max = 150 mA	When using it, it is recommended to add 1–4.7 μF bypass capacitors with a total capacitance not exceeding 18.8 μF.

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
LDO3C_3V0	624	PO	3.0 V output (reserved power)	Vnom = 3.0 V $I_O$max = 150 mA	When using them, it is recommended to add 1–4 μF bypass capacitors with a total capacitance not exceeding 4 μF.
LDO2C_1V8	626	PO	1.8 V output (reserved power)	Vnom = 1.8 V $I_O$max = 150 mA	
VRTC	312	PIO	Power supply for RTC	Vmin = 2.0 V Vnom = 3.0 V Vmax = 3.25 V	
GND	6, 8–10, 12, 13, 22, 23, 32, 34, 35, 37, 39, 46, 47, 56–58, 76–78, 81–85, 87–90, 93, 96, 97, 100, 101, 105, 108, 114, 115, 118, 125, 127, 129, 132, 143, 146, 171, 179, 182, 204–206, 208, 209, 212–218, 221, 224, 225, 228–230, 233–237, 239–241, 243, 245, 246, 248–250, 252, 253, 255, 257, 260, 261, 264–266, 269–273, 275–277, 279, 281, 282, 284, 285, 288–290, 293, 295–297, 299–301, 303, 304, 313, 316, 334, 335, 344, 350, 359, 361–364, 367, 371, 379, 381, 382, 387, 394, 404–406, 413, 416, 417, 425–428, 433–580, 592, 595, 604, 623				
Battery Detection					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_P	418	AI	Battery voltage detect (+)		Must be connected.
BAT_M	419	AI	Battery voltage detect (-)		
BAT_THERM	407	AI	Battery temperature detect		Internally pulled up. Supports 100 kΩ NTC thermistor by default. Connect it to 100 kΩ NTC thermistor. If unused, connect it to GND with a 100 kΩ resistor.
BAT_ID	410	AI	Battery ID detect		If unused, keep it unconnected.
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	332	DI	Turn on/off the module	1.8 V	
VOL_DOWN	333	DI	Volume down		

VOL_UP	329	DI	Volume up		
USB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	429–432	PIO	USB/charger insertion detection Charging power input Power output for OTG device	Vmax = 12.6 V Vmin = 3.7 V Vnom = 5.0 V	The maximum output current in OTG mode is 1.5 A. A test point must be reserved.
USB0_DP	354	AIO	USB0 2.0 differential data (+)		Requires differential impedance of 90 Ω. Complies with USB 2.0 specification. Supports OTG. Test points must be reserved.
USB0_DM	358	AIO	USB0 2.0 differential data (-)		
USB0_SS1_TX_P	360	AO	USB 3.1 channel 1 SuperSpeed transmit (+)		Requires differential impedance of 90 Ω. Complies with USB 3.1 Gen 1 specification.
USB0_SS1_TX_M	357	AO	USB 3.1 channel 1 SuperSpeed transmit (-)		
USB0_SS1_RX_P	356	AI	USB 3.1 channel 1 SuperSpeed receive (+)		
USB0_SS1_RX_M	353	AI	USB 3.1 channel 1 SuperSpeed receive (-)		
USB0_SS2_TX_P	348	AO	USB 3.1 channel 2 SuperSpeed transmit (+)		
USB0_SS2_TX_M	345	AO	USB 3.1 channel 2 SuperSpeed transmit (-)		
USB0_SS2_RX_P	352	AI	USB 3.1 channel 2 SuperSpeed receive (+)		

USB0_SS2_RX_M	349	AI	USB 3.1 channel 2 SuperSpeed receive (-)		
USB_VCONN	375	PI	Power supply for E-Mark cables	Vmax =4.5 V Vmin = 3.0 V	Externally connected to VPH_PWR or dedicated boost converter.
USB0_CC1	339	AI	USB Type-C detect 1		When Micro-USB mode is used, this pin can be used as USB_ID.
USB0_CC2	342	AI	USB Type-C detect 2		
USB_PHY_PS	338	DI	Configuration channel status detection		When USB Type-C mode is used, connect it to SS_DIR_OUT. When Micro-USB mode is used, this pin should be connected to the ground through a 1 kΩ resistor.
SS_DIR_OUT	341	DO	Configuration channel status output		
USB_OPTION	337	AI	Initial configuration for mode selection when powering up USB		When USB Type-C mode is used, keep it unconnected. When Micro-USB mode is used, it should be connected to ground.
USB1_DP	622	AIO	USB1 2.0 differential data (+)		Requires differential impedance of 90 Ω. Complies with USB 2.0 specification. Only supports host mode.
USB1_DM	621	AIO	USB1 2.0 differential data (-)		

					Test points must be reserved.
USB0_DP_AUX_P	620	AIO	Displayport auxiliary channel (+)		
USB0_DP_AUX_M	619	AIO	Displayport auxiliary channel (-)		
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE1_REFCLK_P	594	AIO	PCIe1 reference clock (+)		Requires differential impedance of 85 Ω.
PCIE1_REFCLK_M	593	AIO	PCIe1 reference clock (-)		
PCIE1_RX0_P	597	AI	PCIe1 recive 0 (+)		
PCIE1_RX0_M	596	AI	PCIe1 recive 0 (-)		
PCIE1_RX1_P	599	AI	PCIe1 recive 1 (+)		
PCIE1_RX1_M	598	AI	PCIe1 recive 1 (-)		
PCIE1_TX0_P	601	AO	PCIe1 transmit 0 (+)		
PCIE1_TX0_M	600	AO	PCIe1 transmit 0 (-)		
PCIE1_TX1_P	603	AO	PCIe1 transmit 1 (+)		
PCIE1_TX1_M	602	AO	PCIe1 transmit 1 (-)		
PCIE1_RST_N	605	DO	PCIe1 reset	1.8 V	
PCIE1_CLKREQ_N	606	DI	PCIe1 clock request		
PCIE1_WAKE_N	607	DI	PCIe1 wake up		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DSI_CLK_P	366	AO	LCD MIPI clock (+)		Requires differential impedance of 85 Ω.
DSI_CLK_N	370	AO	LCD MIPI clock (-)		
DSI_LN0_P	380	AO	LCD MIPI lane 0 data (+)		

DSI_LN0_N	377	AO	LCD MIPI lane 0 data (-)		
DSI_LN1_P	376	AO	LCD MIPI lane 1 data (+)		
DSI_LN1_N	373	AO	LCD MIPI lane 1 data (-)		
DSI_LN2_P	372	AO	LCD MIPI lane 2 data (+)		
DSI_LN2_N	369	AO	LCD MIPI lane 2 data (-)		
DSI_LN3_P	368	AO	LCD MIPI lane 3 data (+)		
DSI_LN3_N	365	AO	LCD MIPI lane 3 data (-)		
LCD_TE	374	DI	LCD tearing effect	1.8 V	
LCD_RST	378	DO	LCD reset		External pull-up is not required.
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_P	14	AI	MIPI CSI0 clock (+)		Requires differential impedance of 85 Ω.
CSI0_CLK_N	18	AI	MIPI CSI0 clock (-)		
CSI0_LN0_P	16	AI	MIPI CSI0 lane 0 data (+)		
CSI0_LN0_N	17	AI	MIPI CSI0 lane 0 data (-)		
CSI0_LN1_P	20	AI	MIPI CSI0 lane 1 data (+)		
CSI0_LN1_N	21	AI	MIPI CSI0 lane 1 data (-)		
CSI0_LN2_P	24	AI	MIPI CSI0 lane 2 data (+)		
CSI0_LN2_N	25	AI	MIPI CSI0 lane 2 data (-)		
CSI0_LN3_P	28	AI	MIPI CSI0 lane 3 data (+)		
CSI0_LN3_N	29	AI	MIPI CSI0 lane 3 data (-)		
CAM0_MCLK	30	DO	Master clock of camera 0	1.8 V	

CAM0_RST	26	DO	Reset of camera 0		
CSI1_CLK_P	38	AI	MIPI CS1 clock (+)		Requires differential impedance of 85 Ω.
CSI1_CLK_N	42	AI	MIPI CSI1 clock (-)		
CSI1_LN0_P	40	AI	MIPI CSI1 lane 0 data (+)		
CSI1_LN0_N	41	AI	MIPI CSI1 lane 0 data (-)		
CSI1_LN1_P	44	AI	MIPI CSI1 lane 1 data (+)		
CSI1_LN1_N	45	AI	MIPI CSI1 lane 1 data (-)		
CSI1_LN2_P	48	AI	MIPI CSI1 lane 2 data (+)		
CSI1_LN2_N	49	AI	MIPI CSI1 lane 2 data (-)		
CSI1_LN3_P	52	AI	MIPI CSI1 lane 3 data (+)		
CSI1_LN3_N	53	AI	MIPI CSI1 lane 3 data (-)		
CAM1_MCLK	54	DO	Master clock of camera 1	1.8 V	
CAM1_RST	50	DO	Reset of camera 1		
CSI2_CLK_P	390	AI	MIPI CSI2 clock (+)		Requires differential impedance of 85 Ω.
CSI2_CLK_N	386	AI	MIPI CSI2 clock (-)		
CSI2_LN0_P	392	AI	MIPI CSI2 lane 0 data (+)		
CSI2_LN0_N	389	AI	MIPI CSI2 lane 0 data (-)		
CSI2_LN1_P	388	AI	MIPI CSI2 lane 1 data (+)		
CSI2_LN1_N	385	AI	MIPI CSI2 lane 1 data (-)		
CSI2_LN2_P	396	AI	MIPI CSI2 lane 2 data (+)		
CSI2_LN2_N	393	AI	MIPI CSI2 lane 2 data (-)		
CSI2_LN3_P	400	AI	MIPI CSI2 lane 3 data (+)		

CSI2_LN3_N	397	AI	MIPI CSI2 lane 3 data (-)		
CAM2_MCLK	398	DO	Master clock of camera 2	1.8 V	
CAM2_RST	384	DO	Reset of camera 2		
CSI3_CLK_P	62	AI	MIPI CSI3 clock (+)		Requires differential impedance of 85 Ω.
CSI3_CLK_N	66	AI	MIPI CSI3 clock (-)		
CSI3_LN0_P	60	AI	MIPI CSI3 lane 0 data (+)		
CSI3_LN0_N	61	AI	MIPI CSI3 lane 0 data (-)		
CSI3_LN1_P	68	AI	MIPI CSI3 lane 1 data (+)		
CSI3_LN1_N	69	AI	MIPI CSI3 lane 1 data (-)		
CSI3_LN2_P	64	AI	MIPI CSI3 lane 2 data (+)		
CSI3_LN2_N	65	AI	MIPI CSI3 lane 2 data (-)		
CSI3_LN3_P	72	AI	MIPI CSI3 lane 3 data (+)		
CSI3_LN3_N	73	AI	MIPI CSI3 lane 3 data (-)		
CAM3_MCLK	74	DO	Master clock of camera 3	1.8 V	
CAM3_RST	67	DO	Reset of camera 3		
VREG_L1P_1P05	116	PO	DVDD for cameras 1 and 2	Vnom = 1.05 V $I_O$max = 600 mA	When using them, it is recommended to add bypass capacitors with a total capacitance not exceeding 45.3 μF.
VREG_L2P_1P1	121	PO	DVDD for cameras 0 and 3	Vnom = 1.1 V $I_O$max = 600 mA	
VREG_L3P_2P8	113	PO	AVDD for cameras 1 and 3	Vnom = 2.8 V $I_O$max = 300 mA	When using them, it is recommended to add bypass capacitors with a total capacitance not exceeding 19 μF.
VREG_L4P_2P9	124	PO	AVDD for camera 0	Vnom = 2.9 V $I_O$max = 300 mA	
VREG_L5P_2P8	128	PO	AFVDD for camera 0	Vnom = 2.8 V $I_O$max = 300 mA	

VREG_L6P_1P8	117	PO	DOVDD for cameras 0, 1, 2 and 3	Vnom = 1.8 V $I_{O}max$ = 300 mA	
VREG_L7P_2P8	120	PO	AVDD for camera 2	Vnom = 2.8 V $I_{O}max$ = 300 mA	
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	160	PO	(U)SIM1 card power supply	Vmin = 1.65 V Vmax = 3.05 V Imax = 150 mA	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by the module. When using it, it is recommended to add bypass capacitors with a total capacitance not exceeding 3 μF.
USIM1_DATA	165	DIO	(U)SIM1 card data	1.8/2.95 V	Pull it up to USIM1_VDD with an external 20 kΩ resistor.
USIM1_CLK	164	DO	(U)SIM1 card clock		
USIM1_RST	162	DO	(U)SIM1 card reset		
USIM1_DET	159	DI	(U)SIM1 card hot-plug detect	1.8 V	Active low. Pull it up to 1.8 V externally. If not used, keep it unconnected. Disabled by default, and can be enabled via software configuration.
USIM2_VDD	172	PO	(U)SIM2 card power supply	Vmin = 1.65 V Vmax = 3.05 V Imax = 150 mA	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by

					the module. When using it, it is recommended to add bypass capacitors with a total capacitance not exceeding 3 μF.
USIM2_DATA	169	DIO	(U)SIM2 card data	1.8/2.95 V	Pull it up to USIM2_VDD with an external 20 kΩ resistor.
USIM2_CLK	168	DO	(U)SIM2 card clock		
USIM2_RST	166	DO	(U)SIM2 card reset		
USIM2_DET	163	DI	(U)SIM2 card hot-plug detect	1.8 V	Active low. Pull it up to 1.8 V externally. If not used, keep it unconnected. Disabled by default, and can be enabled via software configuration.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	188	DO	SD card clock	1.8/2.95 V	Control characteristic impedance as 45 Ω.
SD_CMD	180	DIO	SD card command		
SD_DATA0	184	DIO	SDIO data bit 0		
SD_DATA1	185	DIO	SDIO data bit 1		
SD_DATA2	177	DIO	SDIO data bit 2		
SD_DATA3	181	DIO	SDIO data bit 3		
SD_DET	174	DI	SD card hot-plug detect	1.8 V	Active low by default. External 1.8 V pull-up is required.

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
SD_LDO9C	176	PO	Power supply for SD card	Vnom = 2.95 V I_{O}max = 600 mA	When using it, it is recommended to add 1–4.7 μF bypass capacitors with a total capacitance not exceeding 18.8 μF.
SD_LDO6C	173	PO	SD card pull-up power supply; 1.8/2.95 V output	Vnom = 1.8/2.95 V I_{O}max = 150 mA	Only for SD card pull-up. When using it, it is recommended to add 1–3 μF bypass capacitors with a total capacitance not exceeding 3 μF.
UART Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	317	DO	Debug UART transmit	1.8 V	Cannot be multiplexed into generic GPIOs. If not used, keep them unconnected. Test points must be reserved.
DBG_RXD	320	DI	Debug UART receive		
UART_TXD	308	DO	UART transmit		If not used, keep them unconnected.
UART_RXD	309	DI	UART receive		
UART_RTS	305	DO	Request to send signal from the module		
UART_CTS	306	DI	Clear to send signal to the module		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C0_SCL	192	OD	I2C serial clock	1.8 V	External 1.8 V pull-up is required. If not used, keep them unconnected. The sensor I2C
I2C0_SDA	189	OD	I2C serial data		
LPI_SENSOR_ I2C1_SDA	152	OD	I2C data 1 for external sensor		

LPI_SENSOR_I2C1_SCL	149	OD	I2C clock 1 for external sensor		interface only supports sensors of aDSP architecture.
LPI_SENSOR_I2C2_SDA	153	OD	I2C data 2 for external sensor		
LPI_SENSOR_I2C2_SCL	156	OD	I2C clock 2 for external sensor		
CCI_I2C_SDA2	71	OD	I2C data of cameras 2 and 3	1.8 V	External 1.8 V pull-up is required. If not used, keep them unconnected.
CCI_I2C_SCL2	70	OD	I2C clock of cameras 2 and 3		
CCI_I2C_SDA1	401	OD	I2C data of camera 1		
CCI_I2C_SCL1	402	OD	I2C clock of camera 1		
CCI_I2C_SDA0	33	OD	I2C data of camera 0		
CCI_I2C_SCL0	36	OD	I2C clock of camera 0		
I2S Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MI2S_MCLK	142	DO	I2S master clock	1.8 V	
MI2S_SCLK	140	DO	I2S serial clock		
MI2S_WS	137	DO	I2S word select		
MI2S_DATA0	133	DIO	I2S data channel 0		
MI2S_DATA1	136	DIO	I2S data channel 1		
LPI_MI2S_SCLK	138	DO	LPI I2S serial clock		
LPI_MI2S_WS	139	DO	LPI I2S word select		
LPI_MI2S_DATA0	135	DIO	LPI I2S data channel 0		
LPI_MI2S_DATA1	134	DIO	LPI I2S data channel 1		
LPI_MI2S_DATA2	130	DIO	LPI I2S data channel 2		
LPI_MI2S_DATA3	131	DIO	LPI I2S data channel 3		
CODEC_RST_N	126	DO	Audio codec reset		Do not pull it up during startup.

DMIC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LPI_DMIC1_CLK	144	DO	LPI digital MIC1 clock	1.8 V	
LPI_DMIC1_DATA	141	DI	LPI digital MIC1 data		
LPI_DMIC2_CLK	145	DO	LPI digital MIC2 clock		
LPI_DMIC2_DATA	148	DI	LPI digital MIC2 data		
LPI_DMIC3_CLK	612	DO	LPI digital MIC3 clock		
LPI_DMIC3_DATA	611	DI	LPI digital MIC3 data		
TP Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_RST	324	DO	TP reset	1.8 V	
TP_INT	321	DI	TP interrupt		
TP_I2C_SCL	328	OD	TP I2C clock		External 1.8 V pull-up is required. If not used, keep them unconnected.
TP_I2C_SDA	325	OD	TP I2C data		
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	197	DO	SPI clock	1.8 V	Supports master mode only.
SPI_CS	193	DO	SPI chip select		
SPI_MISO	196	DI	SPI master-in slave-out		
SPI_MOSI	194	DO	SPI master-out slave-in		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	399	AI	General-purpose ADC interface		Maximum input voltage 1.8 V.
ADC1	11	AI			

ADC2	15	AI			
ADC3	403	AI			
ADC4	75	AI			
ADC5	383	AI			
PWM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWM2	79	DO	PWM output 2	1.8 V	
PWM1	340	DO	PWM output 1	VPH_PWR	Backlight control.
RGB Interfaces					
Pin No.	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGB_BLU	59	AO	RGB light-blue	$I_{O}max$ = 12 mA	
RGB_GRN	55	AO	RGB light-green		
RGB_RED	63	AO	RGB light-red		
NFC Interface*					
Pin No.	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NFC_CLK	95	DO	NFC clock	1.8 V	
NFC_CLK_REQ	102	DI	NFC clock request		
NFC_DWL_REQ	103	DO	NFC download control request		
NFC_EN	98	DO	NFC enable		Internally pulled up by default.
NFC_INT	99	DI	NFC interrupt		
NFC_I2C_SDA	106	OD	NFC I2C data		External 1.8 V pull-up is required. If not used, keep them unconnected.
NFC_I2C_SCL	107	OD	NFC I2C clock		
Sensor Interrupt Interfaces					
Pin No.	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ACCEL_GYRO_INT1	161	DI	Acceleration/ gyroscope sensor interrupt 1	1.8 V	

ACCEL_GYRO_INT2	158	DI	Acceleration/ gyroscope sensor interrupt 2		
MAG_INT	186	DI	Geomagnetic sensor interrupt		
ALPS_INT	157	DI	Light/proximity sensor interrupt		
HALL_INT	190	DI	Hall sensor interrupt		
GPIO Interfaces					
Pin No.	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_6	94	DIO	General-purpose input/output	1.8 V	
GPIO_7	19	DIO			Wakeup.
GPIO_8	311	DIO			
GPIO_9	307	DIO			
GPIO_12	198	DIO			Wakeup.
GPIO_13	191	DIO			
GPIO_14	183	DIO			Do not pull it up during startup.
GPIO_15	187	DIO			Do not pull it up during startup. Wakeup.
GPIO_16	111	DIO			Wakeup.
GPIO_17	110	DIO			
GPIO_18	122	DIO			Wakeup.
GPIO_19	119	DIO			
GPIO_24	43	DIO			
GPIO_32	351	DIO			
GPIO_33	170	DIO			
GPIO_34	315	DIO			Wakeup.
GPIO_35	178	DIO			
GPIO_42	318	DIO			

GPIO_43	155	DIO			Wakeup. Do not pull up the GPIO_45 during startup.
GPIO_44	202	DIO			
GPIO_45	203	DIO			
GPIO_46	207	DIO			
GPIO_47	319	DIO			Wakeup.
GPIO_61	51	DIO			
GPIO_62	322	DIO			
GPIO_63	326	DIO			Do not pull it up during startup.
GPIO_68	123	DIO			Wakeup.
GPIO_93	147	DIO			Do not pull it up during startup. Wakeup.
GPIO_105	175	DIO			
GPIO_106	167	DIO			
GPIO_107	210	DIO			
GPIO_108	310	DIO			
GPIO_165	150	DIO			
GPIO_166	154	DIO			
GPIO_158	151	DIO			Wakeup.
RF Antenna Interface					
Pin No.	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT0	211	AIO	**SG560D-CE:** 5G NR: LB DRX & MHB TRX (n41 DRX) LTE: LB DRX & MHB TRX (B38/B41 DRX) WCDMA: LB DRX & MHB TRX		50 Ω impedance.
			SG560D-EM: 5G NR: LB DRX &		

			MHB TRX0 LTE: LB DRX & MHB TRX WCDMA: LB DRX & MHB TRX GSM: DCS1800/PCS1900 TRX	
			SG560D-NA: 5G NR: LB DRX & MHB TRX LTE: LB DRX & MHB TRX	
ANT1	220	AIO	**SG560D-CE:** 5G NR: n78/n79 TRX	
			SG560D-EM: 5G NR: n77/n78/n79 TRX0 LTE: B42 TRX	
			SG560D-NA: 5G NR: n77/n78 TRX0 LTE: B42/B43/B48 TRX & B46 PRX	
ANT2	244	AIO	**SG560D-CE:** 5G NR: n1 PRX MIMO & n78/n79 PRX MIMO & n41 DRX MIMO LTE: MHB PRX MIMO	
			SG560D-EM: 5G NR: MHB PRX MIMO & n77/n78/n79 PRX MIMO LTE: MHB PRX MIMO & B42 PRX MIMO & B32 PRX & LB + LB EN-DC PRX	

			SG560D-NA: 5G NR: MHB PRX MIMO & n77/n78 PRX MIMO LTE: MHB PRX MIMO & B46 DRX & B5 EN-DC PRX
ANT3	268	AIO	**SG560D-CE:** 5G NR: n1 DRX MIMO & n78/n79 DRX MIMO & n41 PRX MIMO LTE: MHB DRX MIMO
			SG560D-EM: 5G NR: MHB DRX MIMO & n77/n78/n79 DRX MIMO LTE: MHB DRX MIMO & B42 DRX MIMO & B32 DRX & LB + LB EN-DC DRX
			SG560D-NA: 5G NR: MHB DRX MIMO & n77/n78 DRX MIMO LTE: MHB DRX MIMO & B5 EN-DC DRX
ANT4	280	AIO	**SG560D-CE:** 5G NR: LB TRX & MHB DRX (n41 TRX) & n78/n79 DRX LTE: LB TRX & MHB DRX (B38/B41 TRX) WCDMA: LB TRX & MHB DRX

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
			SG560D-EM: 5G NR: LB TRX & MHB TX1 + DRX & n77/n78/n79 TX1 + DRX LTE: LB TRX & MHB DRX & B42 DRX WCDMA: LB TRX & MHB DRX GSM: GSM850/EGSM900 TRX		
			SG560D-NA: 5G NR: LB TRX & MHB TX1 + DRX & n77/n78 TX1 + DRX LTE: LB TRX & MHB DRX		
ANT_GNSS	302	AI	GNSS antenna interface		
ANT_WIFI/BT	92	AIO	Wi-Fi/Bluetooth antenna interface		
ANT_WIFI_MIMO	86	AIO	Wi-Fi MIMO antenna interface		
Antenna Tuner Control Interfaces					
GRFC_0	242	DIO	General RF Controller	1.8 V	Cannot be multiplexed into a generic GPIO.
GRFC_1	238	DIO			
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH_LED1	7	AO	Flash/torch driver output	$I_O$max = 850 mA	
VIB_DRV_P	27	PO	Vibration motor driver output control	Vmin = 1.50 V Vmax = 3.54 V	

USB_BOOT	200	DI	Force the module into download mode	$V_{IL}max$ = 0.63 V $V_{IH}min$ = 1.17 V	
Reserved Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	31, 80, 91, 104, 195, 199, 201, 219, 222, 223, 226, 227, 231, 232, 247, 251, 254, 256, 258, 259, 262, 263, 267, 274, 278, 283, 286, 287, 291, 292, 294, 298, 314, 323, 327, 330, 331, 343, 346, 347, 355, 391, 395, 411, 414, 415, 422, 423, 581–591, 608–610, 613–618, 625, 627–636				Keep them unconnected.

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (Smart 5G EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Pins

The module provides five VBAT pins, which are dedicated for connection to external power supply. The power supply range of the module is 3.55–4.4 V, and the recommended value is 4.0 V. VPH_PWR is used for powering peripherals.

Table 7: VBAT Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT	1–5	PIO	Power supply for the module	3.55	4.0	4.4	V

3.1.2. Battery Charge and Management

The module supports fully programmable switch-mode Li-ion battery charging. It can charge single-cell Li-ion and Li-polymer batteries. The switch-mode charging supports Quick Charge 2.0, 3.0 and 4.0, and the maximum charging current is 4.0 A. The battery charger of the module supports trickle charging, pre-charge, constant current charging and constant voltage charging modes.

- **Trickle charging:** when the battery voltage is below 2.1 V, a 75 mA trickle charging current is applied to the battery.
- **Pre-charge:** when the battery voltage is between 2.1 V and the pre-charge cut-off voltage (software progarmmable range: 2.7–3.4 V, default value: 3.0 V), the system enters pre-charge mode. The charging current is programmable between 100–450 mA, 300 mA by default.
- **Constant current mode (CC mode):** when the battery voltage increases between the pre-charge cut-off voltage and constant current charing cut-off voltage (software progarmmable range: 3.6–4.4 V, default value: 4.4 V), the system switches to CC mode. The charging current is programmable between 50–3000 mA. The default charging current is 500 mA for USB charging and 3 A for adapter.
- **Constant voltage mode (CV mode):** when the battery voltage reaches the final value 4.4 V, the system switches to CV mode and the charging current decreases gradually. When the charging current reduces to about 100 mA, charging is completed.

Table 8: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	429–432	PIO	USB/charger insertion detection; Charging power input; Power output for OTG device	The maximum output current in OTG mode is 1.5 A. A test point must be reserved.
VBAT	1–5	PIO	Power supply for the module	It must be able to provide sufficient current up to 5.0 A. It is suggested to use a TVS diode for surge protection.
BAT_P	418	AI	Battery voltage detect (+)	Must be connected.
BAT_M	419	AI	Battery voltage detect (-)	
BAT_THERM	407	AI	Battery temperature detect	Internally pulled up. Supports 100 kΩ NTC thermistor by default. Connect it to 100 kΩ NTC thermistor. If unused, connect it to GND with a 100 kΩ resistor.
BAT_ID	410	AI	Battery ID detect	If unused, keep itunconnected.

The module supports battery temperature detection in the condition that the battery integrates a thermistor (100 kΩ ±1 % NTC thermistor with a B-constant of 4250 kΩ ±1 % by default) and the thermistor is connected to BAT_THERM. If BAT_THERM is not connected, there will be malfunctions such as battery charging failure and battery level display error.

A reference design for the battery charging circuit is shown below.

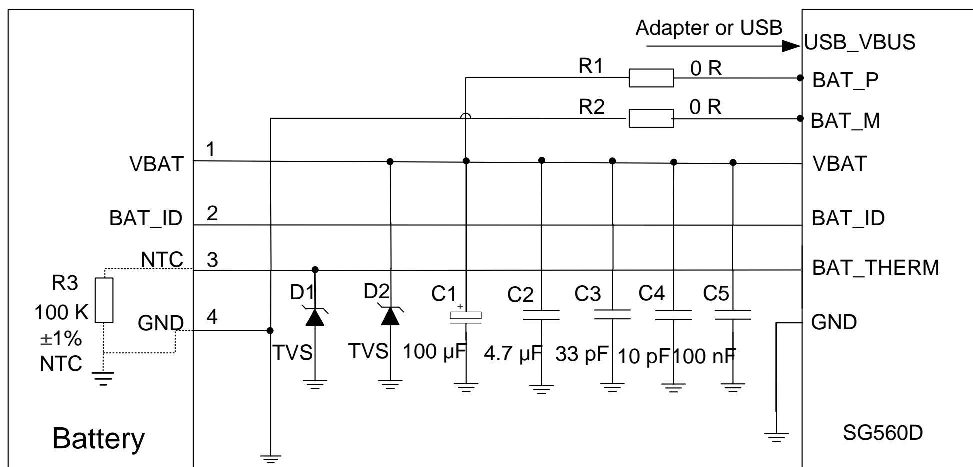


Figure 4: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. For different batteries, the charging and discharging curves must be modified correspondingly to achieve the best performance.

If the thermistor is not available in the battery, or the adapter is utilized for powering the module, then you must connect BAT_THERM to GND via a 100 kΩ resistor. Otherwise, the system may mistakenly judge that the battery temperature is abnormal, which will cause battery charging failure. BAT_P and BAT_M pins must be connected. Otherwise, the module will have abnormalities in voltage detection, as well as related turn-on/off and battery charging or discharging issues.

3.1.3. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 5 A at least. If the voltage difference between input and output is not too large, it is suggested that an LDO should be used for the module. If there is a large voltage difference between the input source and the desired output (VBAT), a buck converter is preferred to be used as the power supply.

The following figure illustrates a reference design for +5 V input power source.

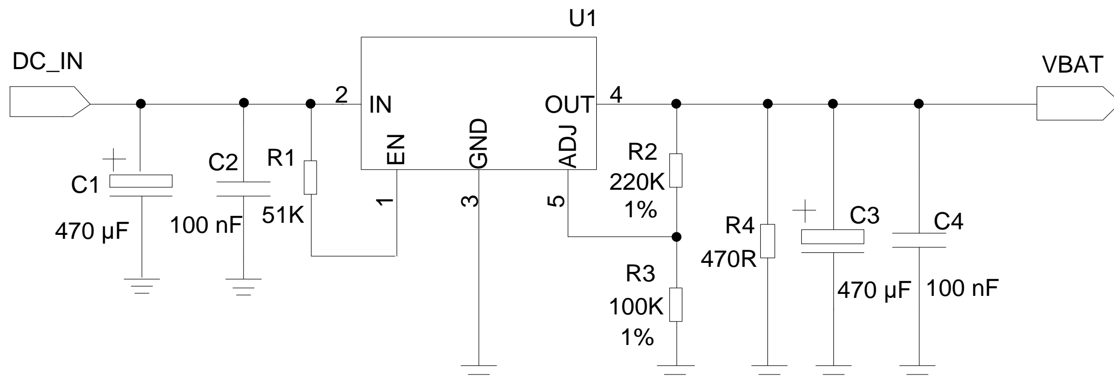


Figure 5: Reference Design for Power Supply

3.1.4. Requirements for Voltage Stability

The recommended power supply value of the module is 4 V. The power supply performance, such as load capacity, voltage ripple, directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current of up to 5 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.2 V, the module will be turned off automatically. Therefore, make sure the input voltage never drops below 3.2 V.

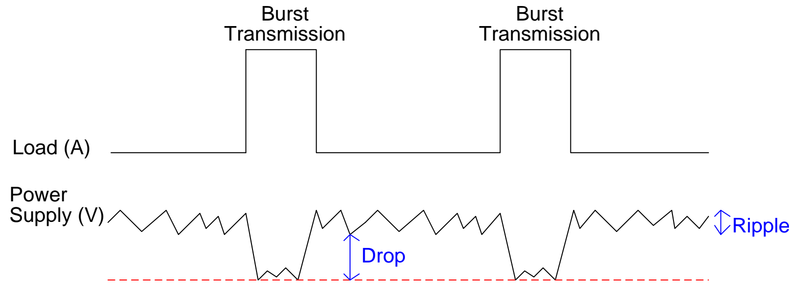


Figure 6: Power Supply Limits During Burst Transmission

To prevent the voltage from dropping below 3.2 V, it is recommended to connect a tantalum capacitor of about 100 μF with low ESR (ESR ≤ 0.7 Ω) and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array, and place these capacitors close to VBAT pins. Additionally, add a 4.7 μF capacitor in parallel. The width of VBAT trace should be not less than 5 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to get a stable power source, it is suggested to use a TVS diode and place it as close to the VBAT pin as possible to enhance surge protection. The following figure shows the structure of the power supply.

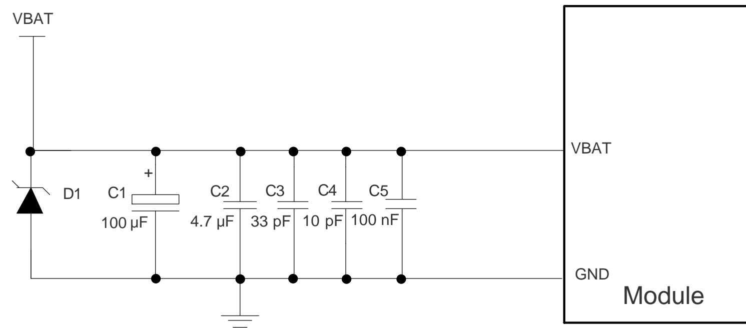


Figure 7: Structure of Power Supply

3.2. Turn On

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description
PWRKEY	332	DI	Turn on/off the module

The module can be turned on by driving the PWRKEY pin low for at least 1.6 s. PWRKEY is pulled up to 1.8 V internally.

It is recommended to use an open drain/collector driver to control PWRKEY. A simple reference circuit is illustrated in the following figure.

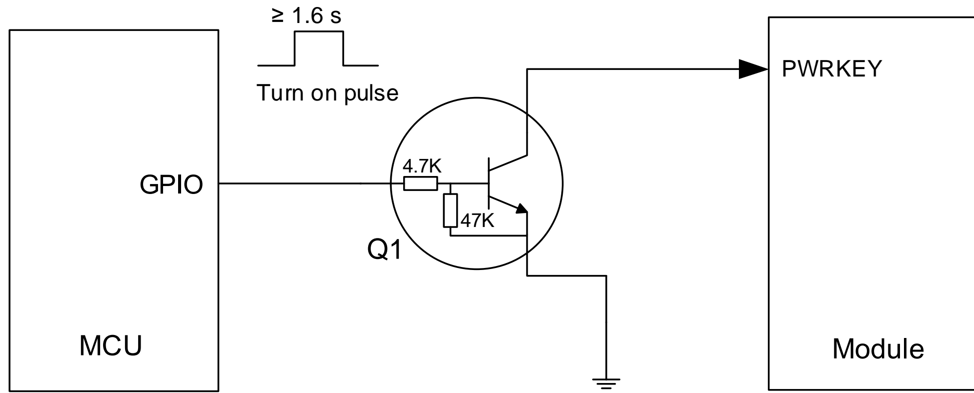


Figure 8: Turn On the Module Using Driving Circuit

Another way to control the PWRKEY pin is to use a push button directly. When you press the button, electrostatic strike may be generated from finger. Therefore, you must place a TVS component near the button for ESD protection. Additionally, a 1 kΩ resistor is connected in series to PWRKEY for ESD protection. A reference circuit is shown in the following figure.

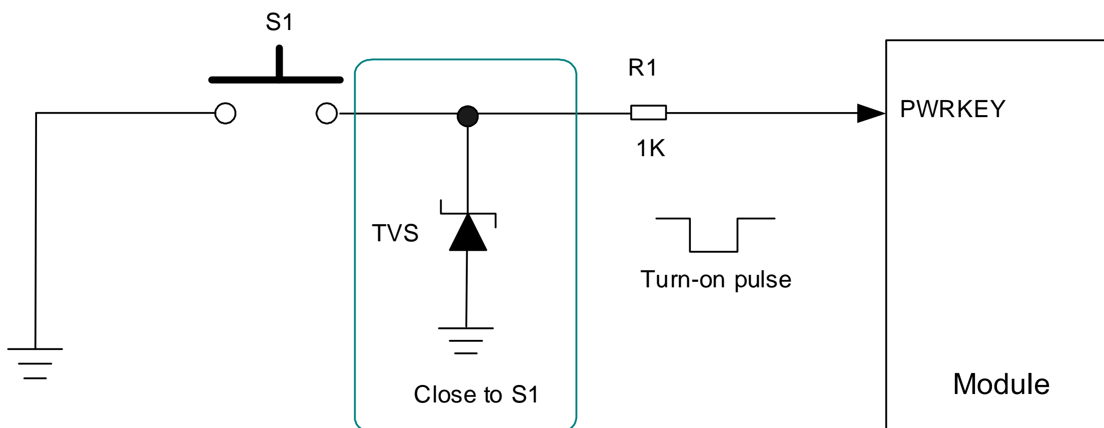


Figure 9: Turn On the Module Using Push Button

The timing of turning on the module is illustrated in the following figure.

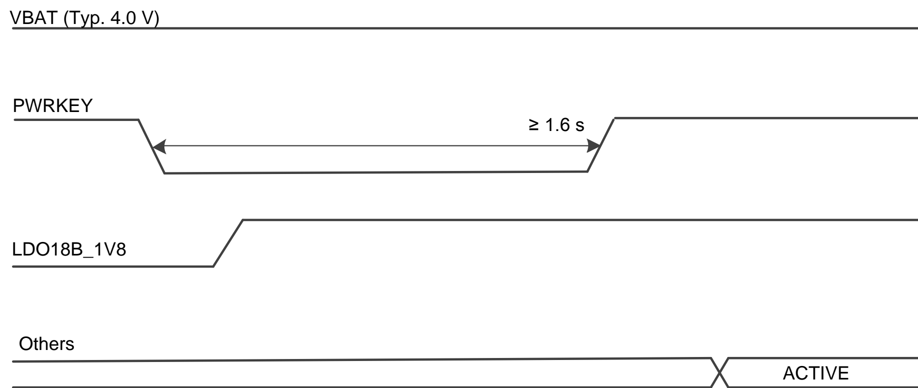


Figure 10: Turn-on Timing

NOTE

1. When the module is turned on for the first time, its turn-on timing may be different from that shown above.
2. Make sure that VBAT is stable before pulling down the PWRKEY pin. It is recommended to drive PWRKEY low after VBAT reaches 4.0 V and remains stable for 30 ms. PWRKEY pin cannot be pulled down all the time.

3.3. Turn Off/Restart

The module can be turned off by driving the PWRKEY pin low for at least 3 s. If the PWRKEY pin is driven low for at least 3 s, you can choose to turn off the module in the prompt window popped up.

It is also possible to restart the module by driving the PWRKEY pin low for at least 8 s. If the PWRKEY pin is driven low for at least 8 s, the module will execute a forced shut-down and then restart. The restart timing is illustrated in the following figure.

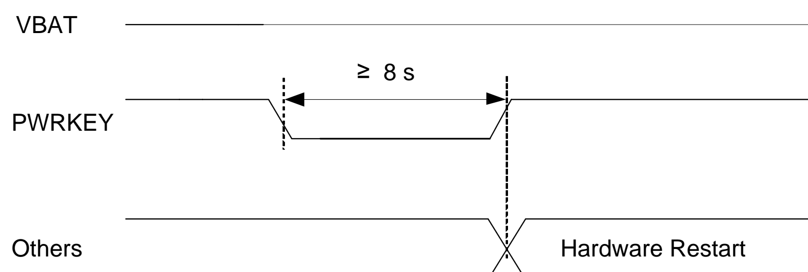


Figure 11: Restart Timing

3.4. VRTC

The RTC (Real Time Clock) can be powered by an external power source when the module is powered down and there is no power supply for the VBAT. The external power source can be a capacitor according to application demands.

The following are reference circuit designs when an external battery is utilized for powering RTC.

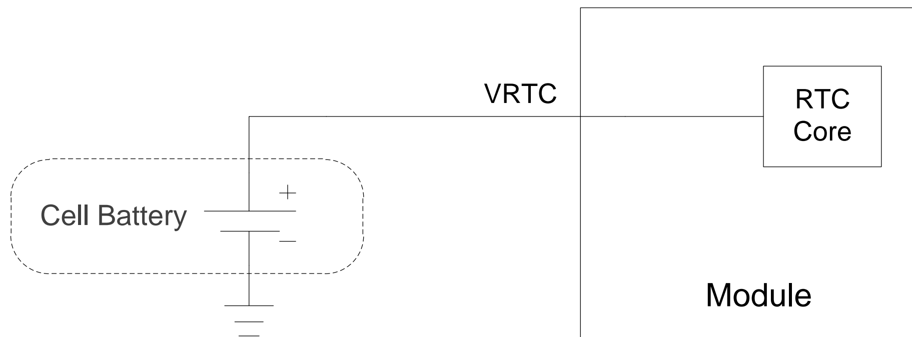


Figure 12: RTC Powered by a Rechargeable Cell Battery

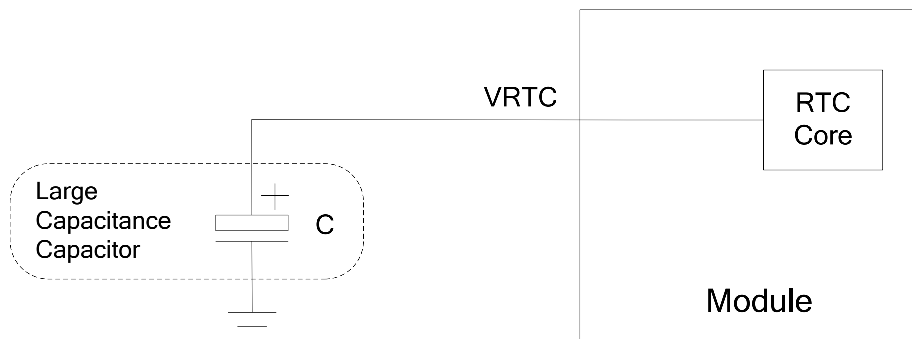


Figure 13: RTC Powered by Capacitor

- If RTC fails, the module can synchronize time through the network after being powering up.
- The recommended input voltage range for VRTC is 2.0–3.25 V and the recommended typical value is 3.0 V.
- When powered by VBAT, the RTC error is 50 ppm. When powered by VRTC, the RTC error is 500 ppm.
- If a rechargeable battery is used, ESR of the battery should be less than 2 kΩ.

3.5. Power Output

The module supports output of regulated voltages for peripheral circuits. During application, it is recommended to connect a 30 pF and a 10 pF capacitor in parallel to suppress high-frequency noise.

Table 10: Pin Definition of Power Suppy Interface

Pin Name	Pin No.	I/O	Description	Comment
VPH_PWR	420, 421, 424	PO	Power supply for peripherals	Keep on. 1.5 A in total.
LDO7C_3V0	412	PO	3.0 V output power for sensors and TP	When using it, it is recommended to add 1–4.7 µF bypass capacitors with a total capacitance not exceeding 18.8 µF.
LDO13C_2V8	409	PO	2.8 V output power for LCM	When using it, it is recommended to add 1–4 µF bypass capacitors with a total capacitance not exceeding 4 µF.
LDO18B_1V8	336	PO	1.8 V output power for I/O pull-up	Keep on. When using it, it is recommended to add 1–4.7 µF bypass capacitors with a total capacitance not exceeding 14.1 µF.
LDO17B_1V8	408	PO	1.8 V output for I/O power supply	When using it, it is recommended to add 1–4.7 µF bypass capacitors with a total capacitance not exceeding 18.8 µF.
LDO12C_1V8	109	PO	1.8 V output for I/O power supply of LCM	When using it, it is recommended to add 1–4 µF bypass capacitors with a total capacitance not exceeding 4 µF.

LDO8C_1V8	112	PO	1.8 V output power for sensors	When using it, it is recommended to add 1–4.7 μF bypass capacitors with a total capacitance not exceeding 18.8 μF.
LDO3C_3V0	624	PO	3.0 V output (reserved power)	When using them, it is recommended to add 1–4 μF bypass capacitors with a total capacitance not exceeding 4 μF.
LDO2C_1V8	626	PO	1.8 V output (reserved power)	
VRTC	312	PIO	Power supply for RTC	
USIM1_VDD	160	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by the module. When using them, it is recommended to add bypass capacitors with a total capacitance not exceeding 3 μF.
USIM2_VDD	172	PO	(U)SIM2 card power supply	
SD_LDO9C	176	PO	Power supply for SD card	When using it, it is recommended to add 1–4.7 μF bypass capacitors with a total capacitance not exceeding 18.8 μF.
SD_LDO6C	173	PO	SD card pull-up power supply	Only for SD card pull-up. When using it, it is recommended to add 1–3 μF bypass capacitors with a total capacitance not exceeding 3 μF.

VREG_L1P_1P05	116	PO	DVDD for cameras 1 and 2	When using them, it is recommended to add bypass capacitors with a total capacitance not exceeding 45.3 μF.
VREG_L2P_1P1	121	PO	DVDD for cameras 0 and 3	
VREG_L3P_2P8	113	PO	AVDD for cameras 1 and 3	When using them, it is recommended to add bypass capacitors with a total capacitance not exceeding 19 μF.
VREG_L4P_2P9	124	PO	AVDD for cameras 0	
VREG_L5P_2P8	128	PO	AFVDD for cameras 0	
VREG_L6P_1P8	117	PO	DOVDD for cameras 0, 1, 2 and 3	
VREG_L7P_2P8	120	PO	AVDD for camera 2	

4 Application Interfaces

4.1. USB Interfaces

The module provides two USB interfaces: USB0 and USB1. USB0 complies with USB 3.1 Gen1 and USB 2.0 specifications and supports USB OTG. USB1 complies with USB 2.0 specification and only supports host mode. The module supports SuperSpeed (5 Gbps) for USB 3.1, and supports high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) for USB 2.0. USB0 can be used for AT command communication, data transmission, software debugging, firmware upgrade and vocie over USB.

4.1.1. USB0 Interface

The following table shows the pin definition of USB0.

Table 11: Pin Definition of USB0

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	429–432	PIO	USB/charger insertion detection Charging power input Power output for OTG device	The maximum output current in OTG mode is 1.5 A. A test point must be reserved.
USB0_DP	354	AIO	USB 2.0 differential data (+)	Requires differential impedance of 90 Ω. Complies with USB 2.0 specification. Supports OTG. Test points must be reserved.
USB0_DM	358	AIO	USB 2.0 differential data (-)	
USB0_SS1_TX_P	360	AO	USB 3.1 channel 1 SuperSpeed transmit (+)	Requires differential impedance of 90 Ω. Complies with USB 3.1 Gen 1 Specification.
USB0_SS1_TX_M	357	AO	USB 3.1 channel 1 SuperSpeed transmit (-)	

USB0_SS1_RX_P	356	AI	USB 3.1 channel 1 SuperSpeed receive (+)	
USB0_SS1_RX_M	353	AI	USB 3.1 channel 1 SuperSpeed receive (-)	
USB0_SS2_TX_P	348	AO	USB 3.1 channel 2 SuperSpeed transmit (+)	
USB0_SS2_TX_M	345	AO	USB 3.1 channel 2 SuperSpeed transmit (-)	
USB0_SS2_RX_P	352	AI	USB 3.1 channel 2 SuperSpeed receive (+)	
USB0_SS2_RX_M	349	AI	USB 3.1 channel 2 SuperSpeed receive (-)	
USB_VCONN	375	PI	Power supply for E-Mark cables	Externally connected to VPH_PWR or dedicated boost converter.
USB0_CC1	339	AI	USB Type-C detect 1	When Micro-USB mode is used, this pin can be used as USB_ID.
USB0_CC2	342	AI	USB Type-C detect 2	
USB_PHY_PS	338	DI	Configuration channel status detection	When USB Type-C mode is used, connect it to SS_DIR_OUT. When Micro-USB mode is used, this pin needs to be connected to ground through a 1 kΩ resistor.
SS_DIR_OUT	341	DO	Configuration channel status output	
USB_OPTION	337	AI	Initial configuration for mode selection when powering up USB	When USB Type-C mode is used, keep it unconnected. When Micro-USB mode is used, it needs to be connected to ground.
USB0_DP_AUX_P	620	AIO	Displayport auxiliary channel (+)	
USB0_DP_AUX_M	619	AIO	Displayport auxiliary channel (-)	

4.1.1.1. USB Type-C Mode

A reference circuit of USB Type-C mode of USB0 is shown below.

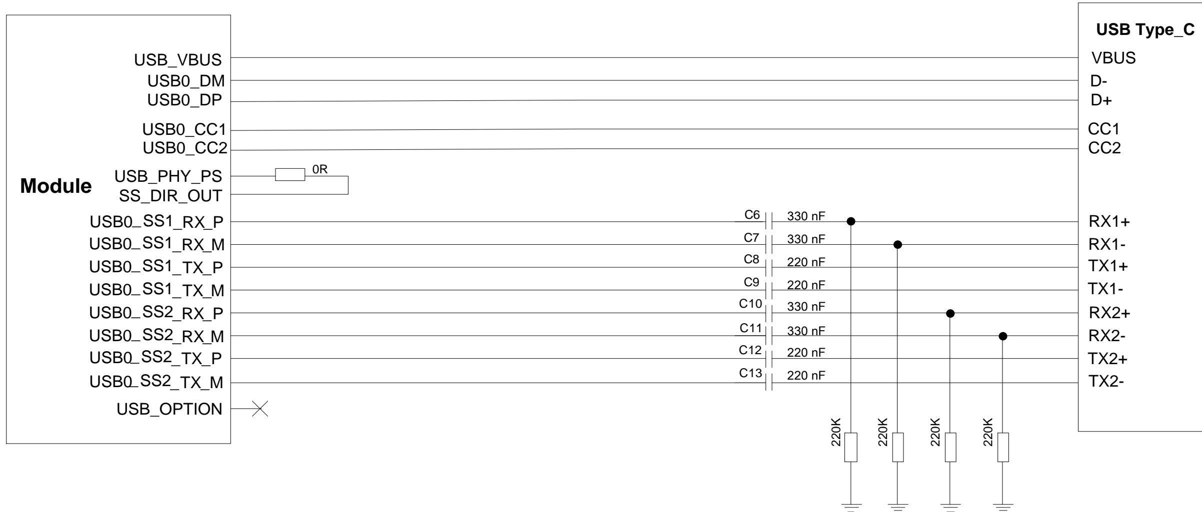


Figure 14: USB Type-C Reference Circuit of USB0

4.1.1.2. Micro USB Mode

USB Type-C mode is used on USB0 by default. Micro USB mode can be used via hardware configuration.

A reference circuit of Micro USB mode of USB0 is shown below.

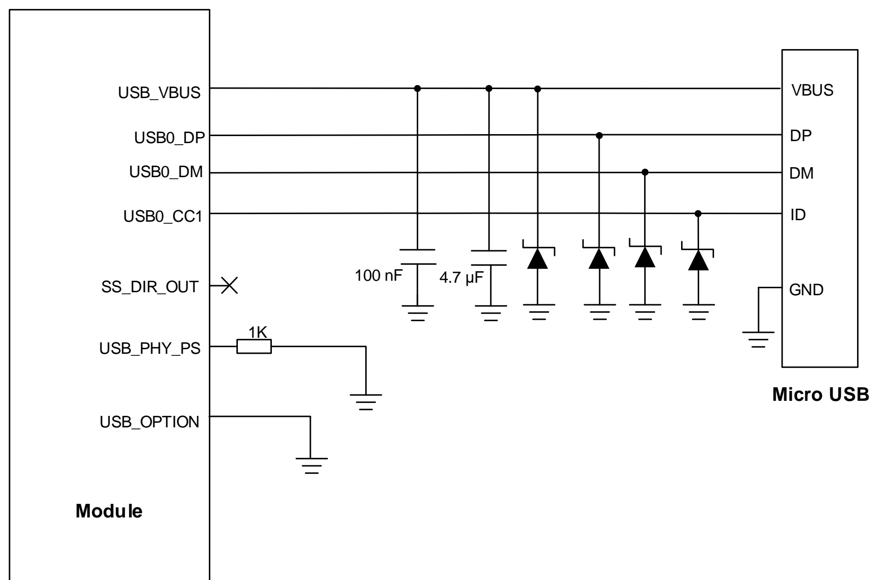


Figure 15: Micro USB Reference Circuit of USB0

4.1.1.3. DisplayPort Mode

The module supports DisplayPort 1.4, which is implemented through USB Type-C interface and supports 4-lane interface with a resolution of 4K @ 60 fps. Pin mapping between USB Type-C interface and DisplayPort interface is defined as follows.

Table 12: USB Type-C Mode and DisplayPort Mode Pin Mapping

Pin Name	Pin No.	USB Type-C Mode	DisplayPort Mode
USB0_SS1_TX_P/M	360, 357	USB0_SS1_TX_P/M	DP_LANE2_P/M
USB0_SS1_RX_P/M	356, 353	USB0_SS1_RX_P/M	DP_LANE3_P/M
USB0_SS2_TX_P/M	348, 345	USB0_SS2_TX_P/M	DP_LANE1_P/M
USB0_SS2_RX_P/M	352, 349	USB0_SS2_RX_P/M	DP_LANE0_P/M
USB0_DP_AUX_P/M	620, 619	SBU1/2	DP_AUX_P/M
USB_VBUS	429–432	USB_VBUS	USB_VBUS
USB0_CC1/CC2	339, 342	USB0_CC1/CC2	DP_HOT_PLUG
USB0_DP/DM	354, 358	USB0_DP/DM	USB0_DP/DM

A reference circuit of the DisplayPort interface is given as follows.

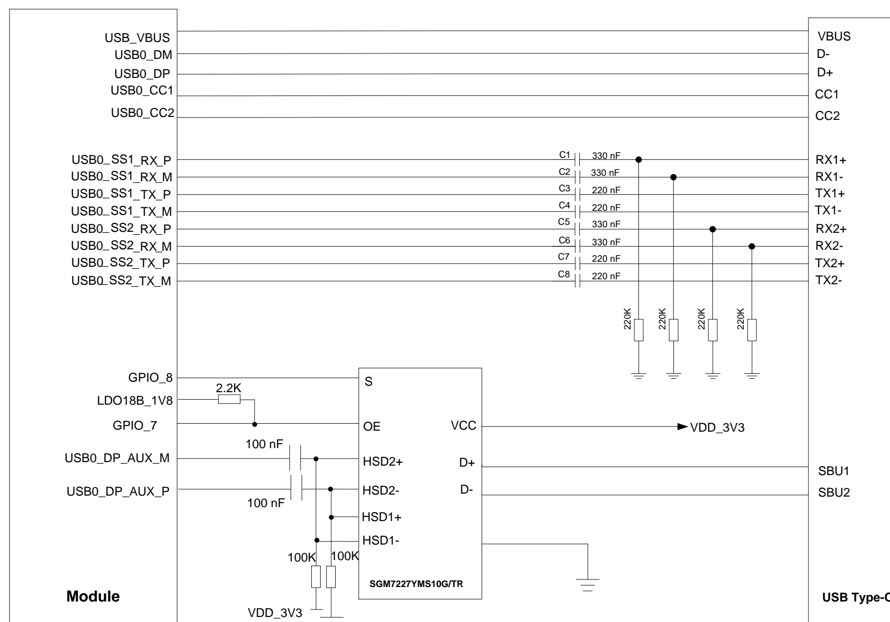


Figure 16: DisplayPort Mode Reference Circuit

4.1.2. USB1 Interface

The following table shows the pin definition of USB1 interface.

Table 13: Pin Description of USB1 Interface

Pin Name	Pin No.	I/O	Description	Comment
USB1_DP	622	AIO	USB1 2.0 differential data (+)	Requires differential impedance of 90 Ω. Complies with USB 2.0 specification. Only supports host mode. Test points must be reserved.
USB1_DM	621	AIO	USB1 2.0 differential data (-)	

4.1.3. Design Principles for USB Interfaces

Table 14: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Mismatch (P – M)
354	USB0_DP	24.43	-0.15
358	USB0_DM	24.58	
360	USB0_SS1_TX_P	25.89	-0.18
357	USB0_SS1_TX_M	26.07	
356	USB0_SS1_RX_P	24.44	0.13
353	USB0_SS1_RX_M	24.31	
348	USB0_SS2_TX_P	26.34	-0.31
345	USB0_SS2_TX_M	26.65	
352	USB0_SS2_RX_P	26.11	0.11
349	USB0_SS2_RX_M	26.00	
622	USB1_DP	23.19	0.29
621	USB1_DM	22.90	
620	USB0_DP_AUX_P	21.97	0.25
619	USB0_DP_AUX_M	21.72	

To ensure USB performance, follow the following principles while designing the USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- The ground reference plane under the USB signals must be continuous without any cuts or any holes to ensure impedance continuity.
- Pay attention to the influence of junction capacitance of ESD protection components on USB data lines. Typically, the capacitance value should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.1. Keep the ESD protection components as close as possible to the USB connector.
- Do not route USB signal traces under crystals, oscillators, magnetic devices, audio signal, and RF signal traces. Route USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Do not route USB 3.1 signal traces under RF signal traces. Crossing or paralleling with RF signal traces is forbidden. Isolation between USB 3.1 signals and RF signals should be more than 90 dB. Otherwise, the RF signals will be seriously affected.
- Ensure the trace length difference between TX_P and TX_M, as well as RX_P and RX_M of USB 3.1 does not exceed 0.7 mm.
- Ensure the trace length difference between USB 2.0 DP and USB 2.0 DM differential pair does not exceed 2 mm.
- For USB 3.1, the spacing between Rx and Tx signal traces should be three times the signal trace width. The spacing between USB 3.1 signal trace and other signal traces should be four times the signal trace width.
- For USB 2.0, the spacing between DP and DM signal traces should be three times the signal trace width. The spacing between USB 2.0 signal traces and other signal traces should be four times the signal trace width.

4.2. (U)SIM Interfaces

The module provides two (U)SIM interfaces which meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported.

Table 15: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	160	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by the module. When using it, it is

				recommended to add bypass capacitors with a total capacitance not exceeding 3 μF.
USIM1_DATA	165	DIO	(U)SIM1 card data	Pull it up to USIM1_VDD with an external 20 kΩ resistor.
USIM1_CLK	164	DO	(U)SIM1 card clock	
USIM1_RST	162	DO	(U)SIM1 card reset	
USIM1_DET	159	DI	(U)SIM1 card hot-plug detect	Active low. Pull it up to 1.8 V externally. If not used, keep it unconnected. Disabled by default, and can be enabled via software configuration.
USIM2_VDD	172	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported and can be identified automatically by the module. When using it, it is recommended to add bypass capacitors with a total capacitance not exceeding 3 μF.
USIM2_DATA	169	DIO	(U)SIM2 card data	Pull it up to USIM2_VDD with an external 20 kΩ resistor.
USIM2_CLK	168	DO	(U)SIM2 card clock	
USIM2_RST	166	DO	(U)SIM2 card reset	
USIM2_DET	163	DI	(U)SIM2 card hot-plug detect	Active low. Pull it up to 1.8 V externally.

	If not used, keep it unconnected. Disabled by default, and can be enabled via software configuration.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

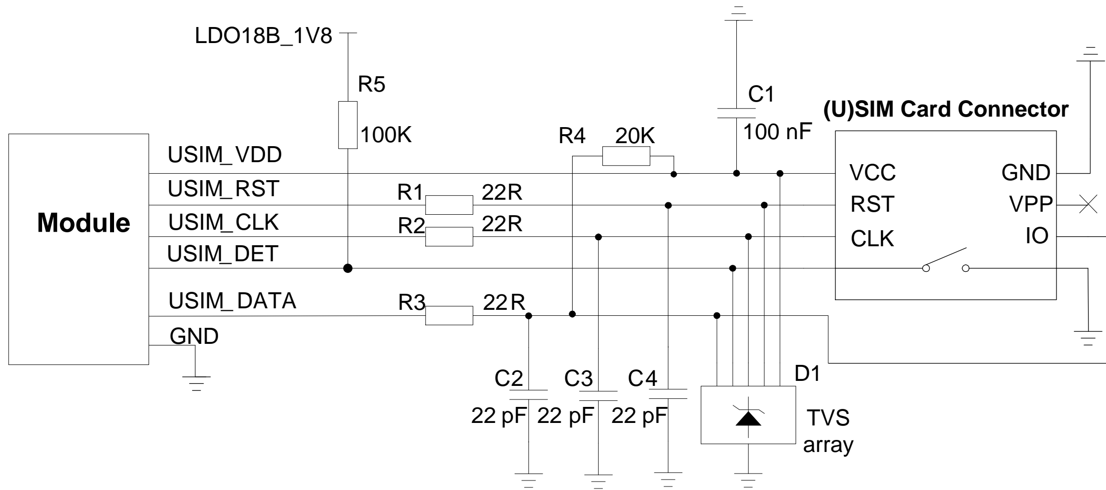


Figure 17: Reference Circuit of (U)SIM Interface with 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected.

A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

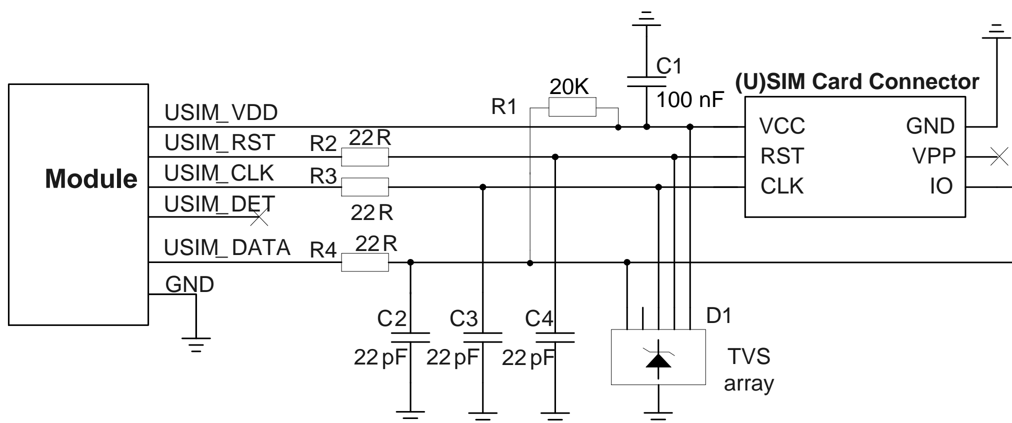


Figure 18: Reference Circuit of (U)SIM Interface with 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signals away from RF and VBAT traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground. In addition, USIM_RST also needs to be shielded with surrounded ground.
- To offer good ESD protection, it is recommended to add a TVS diode array with a parasitic capacitance not exceeding 50 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. Add 22 pF capacitors parallel on USIM_DATA, USIM_CLK and USIM_RST signal traces to filter RF interference, and place them as close to the (U)SIM card connector as possible. Please note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.3. SD Card Interface

The module supports SD 3.0 protocol. The pin definition of the SD card interface is shown below.

Table 16: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	188	DO	SD card clock	Control characteristic impedance as 45 Ω.
SD_CMD	180	DIO	SD card command	
SD_DATA0	184	DIO	SDIO data bit 0	
SD_DATA1	185	DIO	SDIO data bit 1	
SD_DATA2	177	DIO	SDIO data bit 2	
SD_DATA3	181	DIO	SDIO data bit 3	
SD_DET	174	DI	SD card hot-plug detect	Active low by default. External 1.8 V pull-up is required.
SD_LDO9C	176	PO	Power supply for SD card	When using it, it is recommended to add 1–4.7 μF bypass capacitors with a total capacitance not exceeding 18.8 μF.

SD_LDO6C	173	PO	SD card pull-up power supply	Only for SD card pull-up. When using it, it is recommended to add 1–3 µF bypass capacitors with a total capacitance not exceeding 3 µF.

A reference circuit for SD card interface is shown below.

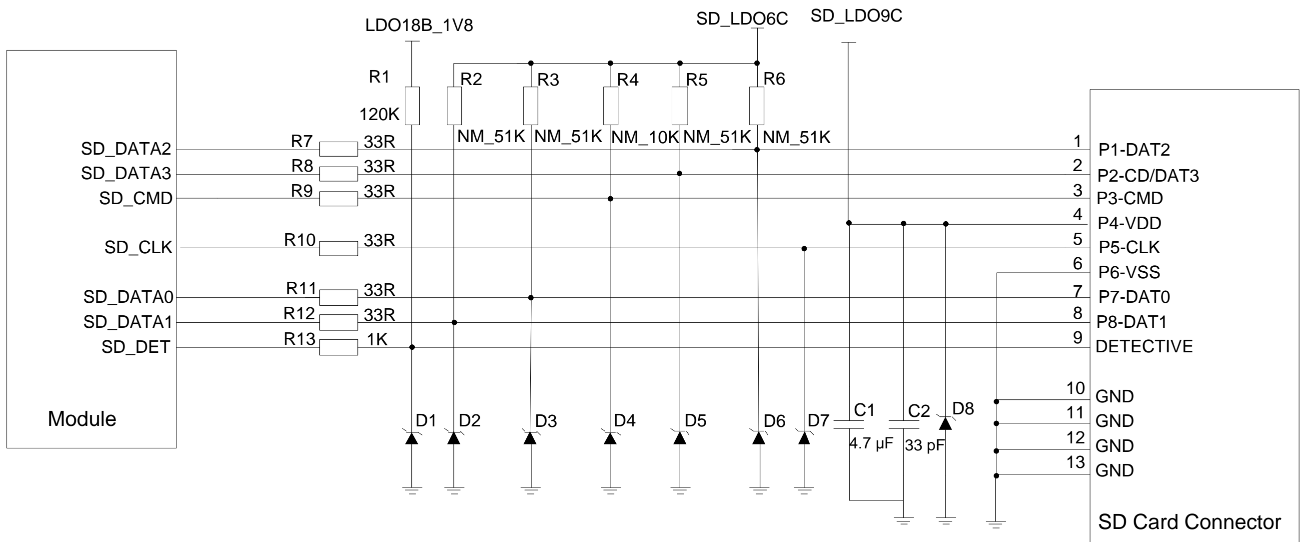


Figure 19: Reference Circuit for SD Card Interface

SD_LDO9C is a peripheral driver power supply for SD card. The maximum drive current is 600 mA. Because of the high drive current, it is recommended that the trace width is 0.6 mm or above. To ensure the stability of drive power, add a 4.7 µF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK and SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of them as 45 Ω, and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB, and keep them of the same length. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 45 Ω ±10 %, and add ground shielding.
- The trace length difference between SD_CLK and SD_CMD/SD_DATA[0:3] should be less than 2 mm.
- Trace length requirements: less than 150 mm for SDR50 mode; less than 50 mm for SDR104 mode.
- The spacing between signal lines should be 1.5 times the line width.
- The capacitive reactance of SD_DATA[0:3] traces should be less than 8 pF.

Table 17: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)
188	SD_CLK	49.25
180	SD_CMD	49.16
184	SD_DATA0	49.51
185	SD_DATA1	49.80
177	SD_DATA2	49.47
181	SD_DATA3	49.63

4.4. GPIO Interfaces

The module has abundant GPIO interfaces with power domain of 1.8 V. The pin definition is listed below.

Table 18: Pin Definition of GPIO Interfaces

<table>
<tr><th>Pin Name</th><th>Pin No.</th><th>I/O</th><th>Description</th><th>Comment</th></tr>
<tr><td>GPIO_6</td><td>94</td><td>DIO</td><td rowspan="10">General-purpose input/output</td><td></td></tr>
<tr><td>GPIO_7</td><td>19</td><td>DIO</td><td rowspan="2">Wakeup.</td></tr>
<tr><td>GPIO_8</td><td>311</td><td>DIO</td></tr>
<tr><td>GPIO_9</td><td>307</td><td>DIO</td><td></td></tr>
<tr><td>GPIO_12</td><td>198</td><td>DIO</td><td>Wakeup.</td></tr>
<tr><td>GPIO_13</td><td>191</td><td>DIO</td><td></td></tr>
<tr><td>GPIO_14</td><td>183</td><td>DIO</td><td>Do not pull it up during startup.</td></tr>
<tr><td>GPIO_15</td><td>187</td><td>DIO</td><td>Do not pull it up during startup;
Wakeup.</td></tr>
<tr><td>GPIO_16</td><td>111</td><td>DIO</td><td>Wakeup.</td></tr>
<tr><td>GPIO_17</td><td>110</td><td>DIO</td><td></td></tr>
</table>

GPIO_18	122	DIO	Wakeup.
GPIO_19	119	DIO	
GPIO_24	43	DIO	
GPIO_32	351	DIO	
GPIO_33	170	DIO	
GPIO_34	315	DIO	Wakeup.
GPIO_35	178	DIO	
GPIO_42	318	DIO	
GPIO_43	155	DIO	Wakeup.
GPIO_44	202	DIO	
GPIO_45	203	DIO	
GPIO_46	207	DIO	
GPIO_47	319	DIO	Wakeup.
GPIO_61	51	DIO	
GPIO_62	322	DIO	
GPIO_63	326	DIO	Do not pull it up during startup.
GPIO_68	123	DIO	Wakeup.
GPIO_93	147	DIO	Do not pull it up during startup; Wakeup.
GPIO_105	175	DIO	
GPIO_106	167	DIO	
GPIO_107	210	DIO	
GPIO_108	310	DIO	
GPIO_165	150	DIO	
GPIO_166	154	DIO	
GPIO_158	151	DIO	Wakeup.

4.5. UART Interfaces

The module supports up to eleven UART interfaces. Two of them are default configurations, see ***Table 19*** for details. Nine of them can be multiplexed from other interfaces, see ***Table 23*** for details.

Two default UART interfaces are:

- UART: 4-wire UART interface, supports RTS and CTS hardware flow control, up to 4 Mbps.
- DBG_UART: 2-wire UART interface, dedicated for debugging.

Pin definition of the UART interfaces is given as follows:

Table 19: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	317	DO	Debug UART transmit	If not used, keep them unconnected. Cannot be multiplexed into generic GPIOs. Test points must be reserved.
DBG_RXD	320	DI	Debug UART receive	
UART_TXD	308	DO	UART transmit	If not used, keep them unconnected.
UART_RXD	309	DI	UART receive	
UART_RTS	305	DO	Request to send signal from the module	
UART_CTS	306	DI	Clear to send signal to the module	

UART is a 4-wire UART interface with 1.8 V power domain. A level-shifting chip should be used if your application is equipped with a 3.3 V UART interface. The following figure shows a reference design.

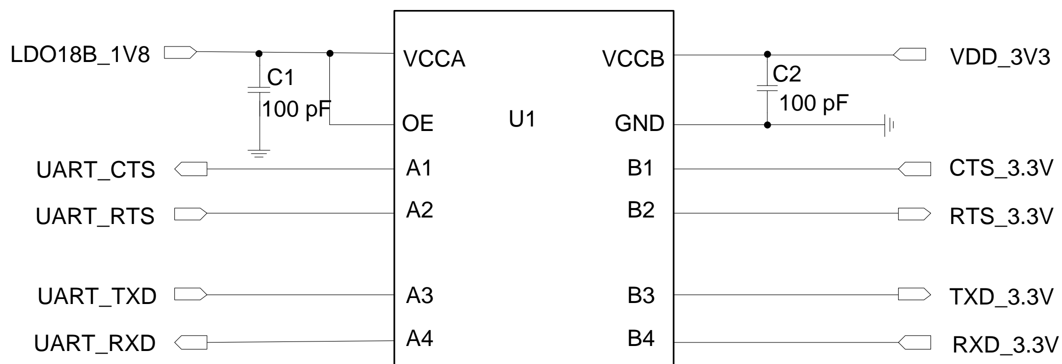


Figure 20: Reference Circuit with Level-Shifting Chip (for UART)

A level translator and an RS-232 level-shifting chip are recommended to be added between the module and PC, as shown below.

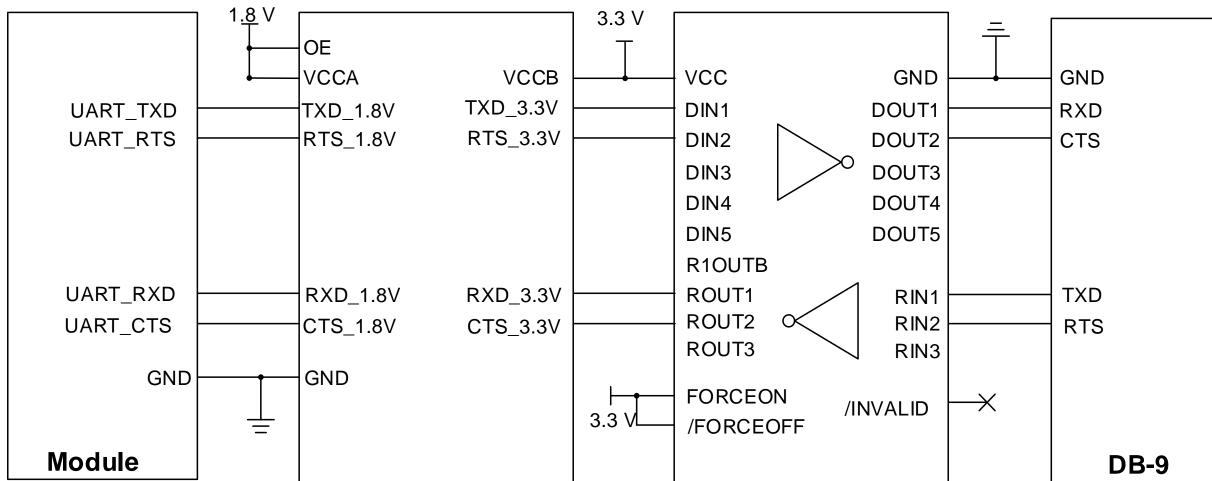


Figure 21: Reference Circuit with RS232 Level-Shifting Chip (for UART)

NOTE

DBG_UART is similar to UART. For the reference design of DBG_UART, refer to that of UART.

4.6. I2C Interfaces

The module provides up to sixteen I2C interfaces. Five of them are dedicated I2C interfaces used for camera and sensor peripherals. Three of them are generic I2C interfaces that can be used for TP and NFC peripherals, see ***Table 20*** for details. Eight of them can be multiplexed from other interfaces, see ***Table 23*** for details.

All I2C interfaces are open drain signals and therefore must be pulled up externally. The reference power domain is 1.8 V. The sensor I2C interface only supports sensors of aDSP architecture. CCI_I2C signals are controlled by Linux Kernel code and support connection to video output related devices.

Table 20: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C0_SCL	192	OD	I2C serial clock	External 1.8 V pull-up is required. If not used, keep them unconnected. 1.8 V power domain.
I2C0_SDA	189	OD	I2C serial data	

LPI_SENSOR_I2C1_SDA	152	OD	I2C data 1 for external sensor	The sensor I2C interface only supports sensors of aDSP architecture.
LPI_SENSOR_I2C1_SCL	149	OD	I2C clock 1 for external sensor	
LPI_SENSOR_I2C2_SDA	153	OD	I2C data 2 for external sensor	
LPI_SENSOR_I2C2_SCL	156	OD	I2C clock 2 for external sensor	
TP_I2C_SCL	328	OD	TP I2C clock	1.8 V power domain. External 1.8 V pull-up is required. If not used, keep them unconnected.
TP_I2C_SDA	325	OD	TP I2C data	
NFC_I2C_SDA	106	OD	NFC I2C clock	
NFC_I2C_SCL	107	OD	NFC I2C data	
CCI_I2C_SDA0	33	OD	I2C data of camera 0	
CCI_I2C_SCL0	36	OD	I2C clock of camera 0	
CCI_I2C_SDA1	401	OD	I2C data of camera 1	
CCI_I2C_SCL1	402	OD	I2C clock of camera 1	
CCI_I2C_SDA2	71	OD	I2C data of camera 2 and 3	
CCI_I2C_SCL2	70	OD	I2C clock of camera 2 and 3	

4.7. SPI Interface

The module supports up to ten SPI interfaces. One of them is default configuration, and supports master mode only, see ***Table 21*** for details. Nine of them can be multiplexed from other interfaces, see ***Table 23*** for details.

Table 21: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	197	DO	SPI clock	1.8 V power doamin. Supports master mode only.
SPI_CS	193	DO	SPI chip select	
SPI_MISO	196	DI	SPI master-in salve-out	
SPI_MOSI	194	DO	SPI master-out slave-in	

4.8. I2S Interfaces

The module supports up to five I2S interfaces. Two of them are default configurations, see ***Table 22*** for details. Three of them can be multiplexed from other interfaces, see ***Table 24*** for details.

Table 22: Pin Definition of I2S Interfaces

Pin Name	Pin No.	I/O	Description
MI2S_MCLK	142	DO	I2S master clock
MI2S_SCLK	140	DO	I2S serial clock
MI2S_WS	137	DO	I2S word select
MI2S_DATA0	133	DIO	I2S data channel 0
MI2S_DATA1	136	DIO	I2S data channel 1
LPI_MI2S_SCLK	138	DO	LPI I2S serial clock
LPI_MI2S_WS	139	DO	LPI I2S word select
LPI_MI2S_DATA0	135	DIO	LPI I2S data channel 0
LPI_MI2S_DATA1	134	DIO	LPI I2S data channel 1
LPI_MI2S_DATA2	130	DIO	LPI I2S data channel 2
LPI_MI2S_DATA3	131	DIO	LPI I2S data channel 3
CODEC_RST_N	126	DO	Audio codec reset

4.9. UART/SPI/I2C/I2S Multiplexing Relationship

UART/SPI/I2C multiplexing relationship is shown in the following table.

Table 23: UART/SPI/I2C Multiplexing Relationship

Channel	Pin No.	Pin Name	GPIO No.	Multiplex Function		
				UART	SPI	I2C
QUP0-SE0	189	I2C0_SDA	GPIO_0	UART00_CTS	SPI00_MISO	I2C00_SDA

	192	I2C0_SCL	GPIO_1	UART00_RTS	SPI00_MOSI	I2C00_SCL
	605	PCIE1_RST_N	GPIO_2	UART00_TXD	SPI00_CLK	-
	607	PCIE1_WAKE_N	GPIO_3	UART00_RXD	SPI00_CS0	-
QUP0-SE2	311	GPIO_8	GPIO_8	-	-	I2C02_SDA
	307	GPIO_9	GPIO_9	-	-	I2C02_SCL
QUP0-SE3	198	GPIO_12	GPIO_12	UART03_CTS	SPI03_MISO	I2C03_SDA
	191	GPIO_13	GPIO_13	UART03_RTS	SPI03_MOSI	I2C03_SCL
	183	GPIO_14	GPIO_14	UART03_TXD	SPI03_CLK	-
	187	GPIO_15	GPIO_15	UART03_RXD	SPI03_CS0	-
QUP0-SE4	111	GPIO_16	GPIO_16	UART04_CTS	SPI04_MISO	I2C04_SDA
	110	GPIO_17	GPIO_17	UART04_RTS	SPI04_MOSI	I2C04_SCL
	122	GPIO_18	GPIO_18	UART04_TXD	SPI04_CLK	-
	119	GPIO_19	GPIO_19	UART04_RXD	SPI04_CS0	-
QUP1-SE0	351	GPIO_32	GPIO_32	UART10_CTS	SPI10_MISO	I2C10_SDA
	170	GPIO_33	GPIO_33	UART10_RTS	SPI10_MOSI	I2C10_SCL
	315	GPIO_34	GPIO_34	UART10_TXD	SPI10_CLK	-
	178	GPIO_35	GPIO_35	UART10_RXD	SPI10_CS0	-
QUP1-SE1	106	NFC_I2C_SDA*	GPIO_36	UART11_CTS	SPI11_MISO	I2C11_SDA
	107	NFC_I2C_SCL*	GPIO_37	UART11_RTS	SPI11_MOSI	I2C11_SCL
	98	NFC_EN*	GPIO_38	UART11_TXD	SPI11_CLK	-
	102	NFC_CLK_REQ*	GPIO_39	UART11_RXD	SPI11_CS0	-
QUP1-SE2	103	NFC_DWL_REQ*	GPIO_40	UART12_CTS	SPI12_MISO	I2C12_SDA
	99	NFC_INT*	GPIO_41	UART12_RTS	SPI12_MOSI	I2C12_SCL
	318	GPIO_42	GPIO_42	UART12_TXD	SPI12_CLK	-
	155	GPIO_43	GPIO_43	UART12_RXD	SPI12_CS0	-
QUP1-SE3	202	GPIO_44	GPIO_44	UART13_CTS	SPI13_MISO	I2C13_SDA

	203	GPIO_45	GPIO_45	UART13_RTS	SPI13_MOSI	I2C13_SCL
	207	GPIO_46	GPIO_46	UART13_TXD	SPI13_CLK	-
	319	GPIO_47	GPIO_47	UART13_RXD	SPI13_CS0	-
QUP1-SE4	306	UART_CTS	GPIO_48	UART14_CTS	SPI14_MISO	I2C14_SDA
	305	UART_RTS	GPIO_49	UART14_RTS	SPI14_MOSI	I2C14_SCL
	308	UART_TXD	GPIO_50	UART14_TXD	SPI14_CLK	-
	309	UART_RXD	GPIO_51	UART14_RXD	SPI14_CS0	-
	324	TP_RST	GPIO_55	-	SPI14_CS1	-
	378	LCD_RST	GPIO_54	-	SPI14_CS2	-
	98	NFC_EN*	GPIO_38	-	SPI14_CS3	-
QUP1-SE5	325	TP_I2C_SDA	GPIO_52	UART15_CTS	SPI15_MISO	I2C15_SDA
	328	TP_I2C_SCL	GPIO_53	UART15_RTS	SPI15_MOSI	I2C15_SCL
	378	LCD_RST	GPIO_54	UART15_TXD	SPI15_CLK	-
	324	TP_RST	GPIO_55	UART15_RXD	SPI15_CS0	-
QUP1-SE6	196	SPI_MISO	GPIO_56	UART16_CTS	SPI16_MISO	I2C16_SDA
	194	SPI_MOSI	GPIO_57	UART16_RTS	SPI16_MOSI	I2C16_SCL
	197	SPI_CLK	GPIO_58	UART16_TXD	SPI16_CLK	-
	193	SPI_CS	GPIO_59	UART16_RXD	SPI16_CS0	-
	322	GPIO_62	GPIO_62	-	SPI16_CS1	-
	326	GPIO_63	GPIO_63	-	SPI16_CS2	-
	308	UART_TXD	GPIO_50	-	SPI16_CS3	-

NOTE

1. The QUP SE channel can be used flexibly to support UART, SPI and I2C interfaces.
2. Note that one QUP SE channel cannot support two protocols at the same time. For example, QUP0-SE0 cannot support UART and I2C at the same time. If one interface only occupies parts of the pins in one QUP SE channel, then other pins in the channel can only be used as GPIOs.

Table 24: I2S Multiplexing Relationship

Channel	Pin No.	Pin Name	GPIO No.	Multiplex Function
				I2S
1	144	LPI_DMIC1_CLK	GPIO_150	LPI_I2S1_SCLK
	141	LPI_DMIC1_DATA	GPIO_151	LPI_I2S1_WS
	145	LPI_DMIC2_CLK	GPIO_152	LPI_I2S1_DATA0
	148	LPI_DMIC2_DATA	GPIO_153	LPI_I2S1_DATA1
2	142	MI2S_MCLK	GPIO_96	PRI_MI2S_MCLK
	140	MI2S_SCLK	GPIO_97	MI2S0_SCLK
	137	MI2S_WS	GPIO_100	MI2S0_WS
	133	MI2S_DATA0	GPIO_98	MI2S0_DATA0
	136	MI2S_DATA1	GPIO_99	MI2S0_DATA1
3	175	GPIO_105	GPIO_105	MI2S1_DATA1
	167	GPIO_106	GPIO_106	MI2S1_SCLK
	210	GPIO_107	GPIO_107	MI2S1_DATA0
	310	GPIO_108	GPIO_108	MI2S1_WS
4	190	HALL_INT	GPIO_101	MI2S2_SCLK
	158	ACCEL_GYRO_INT2	GPIO_102	MI2S2_DATA0
	161	ACCEL_GYRO_INT1	GPIO_103	MI2S2_WS
	186	MAG_INT	GPIO_104	MI2S2_DATA1
5	138	LPI_MI2S_SCLK	GPIO_144	LPI_MI2S_SCLK
	139	LPI_MI2S_WS	GPIO_145	LPI_MI2S_WS
	135	LPI_MI2S_DATA0	GPIO_146	LPI_MI2S_DATA0
	134	LPI_MI2S_DATA1	GPIO_147	LPI_MI2S_DATA1
	130	LPI_MI2S_DATA2	GPIO_148	LPI_MI2S_DATA2
	131	LPI_MI2S_DATA3	GPIO_149	LPI_MI2S_DATA3

4.10. ADC Interfaces

The module provides six analog-to-digital converter (ADC) interfaces that support up to 15-bit resolution. The pin definition is shown below.

Table 25: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	399	AI	General-purpose ADC interface	Maximum input voltage 1.8 V.
ADC1	11	AI		
ADC2	15	AI		
ADC3	403	AI		
ADC4	75	AI		
ADC5	383	AI		

4.11. LCM Interface

The module provides one LCM interface based on MIPI DSI standard. The interface supports one 4-lane high-speed differential data transmission with maximum speed rate of 2.5 Gbps/lane and supports FHD + (1200 × 2520) @ 144 fps. The pin definition of the LCM interface is shown below.

Table 26: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PWM1	340	DO	PWM output 1	Backlight control.
DSI_CLK_P	366	AO	LCD MIPI clock (+)	Requires differential impedance of 85 Ω.
DSI_CLK_N	370	AO	LCD MIPI clock (-)	
DSI_LN0_P	380	AO	LCD MIPI lane 0 data (+)	
DSI_LN0_N	377	AO	LCD MIPI lane 0 data (-)	
DSI_LN1_P	376	AO	LCD MIPI lane 1 data (+)	

DSI_LN1_N	373	AO	LCD MIPI lane 1 data (-)	
DSI_LN2_P	372	AO	LCD MIPI lane 2 data (+)	
DSI_LN2_N	369	AO	LCD MIPI lane 2 data (-)	
DSI_LN3_P	368	AO	LCD MIPI lane 3 data (+)	
DSI_LN3_N	365	AO	LCD MIPI lane 3 data (-)	
LCD_TE	374	DI	LCD tearing effect	1.8 V power domain.
LCD_RST	378	DO	LCD reset	1.8 V power domain. External pull-up is not required.

The following figure shows a reference design for LCM interface.

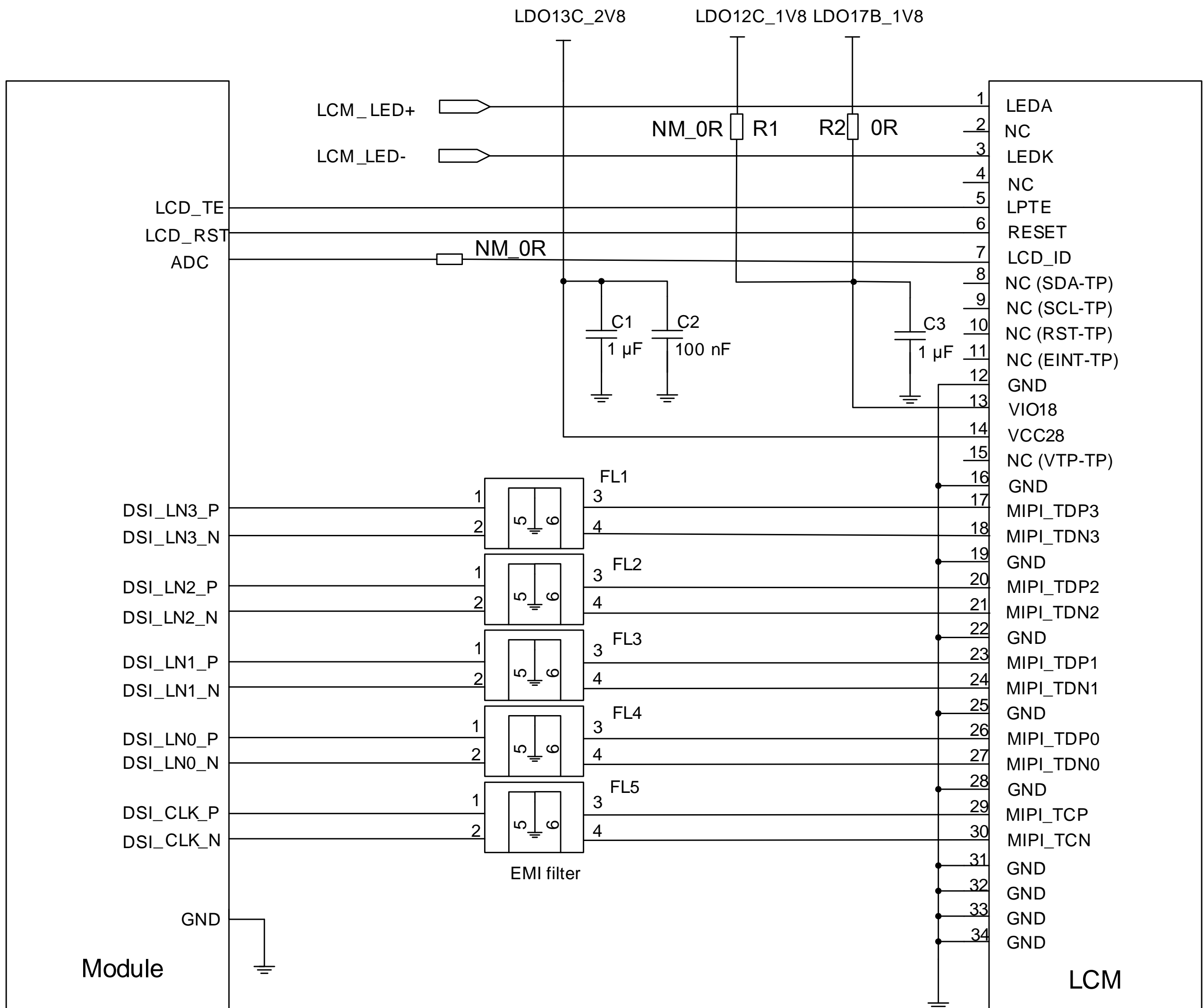


Figure 22: Reference Circuit for LCM Interface

MIPI are high-speed signal traces. It is recommended to add common-mode chokes in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that the LCM module factory should burn an OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to the ADC pin of the module, but note that the output voltage of LCD_ID should not exceed the voltage range of the ADC pin.

You can design external backlight driver circuit for LCM according to actual requirement. The reference design is shown in the figure below, in which PWM1 is used for backlight brightness adjustment.

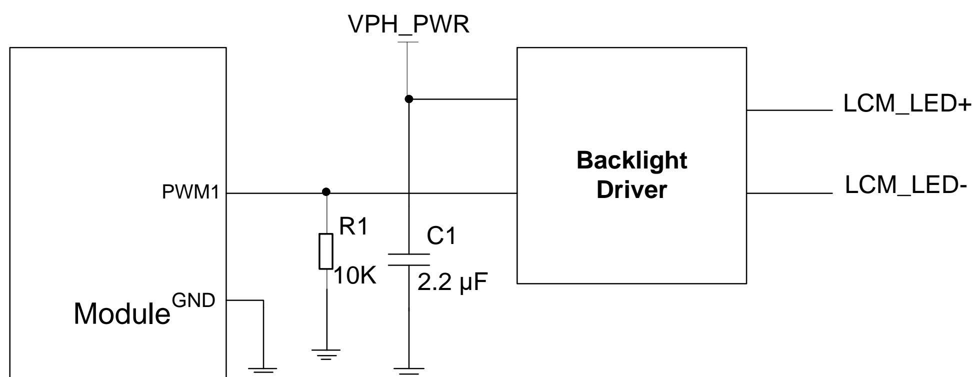


Figure 23: LCM External Backlight Driver Reference Circuit

4.12. Touch Panel Interface

The module provides one I2C interface for connection with Touch Panel (TP), and provides the corresponding power supply and interrupt pins for TP. The pin definition of touch panel interface is given below.

Table 27: Pin Definition of Touch Panel Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	324	DO	TP reset	1.8 V power domain.
TP_INT	321	DI	TP interrupt	
TP_I2C_SCL	328	OD	TP I2C clock	External 1.8 V pull-up is required. If not used, keep them unconnected.
TP_I2C_SDA	325	OD	TP I2C data	

A reference design for TP interface is shown below.

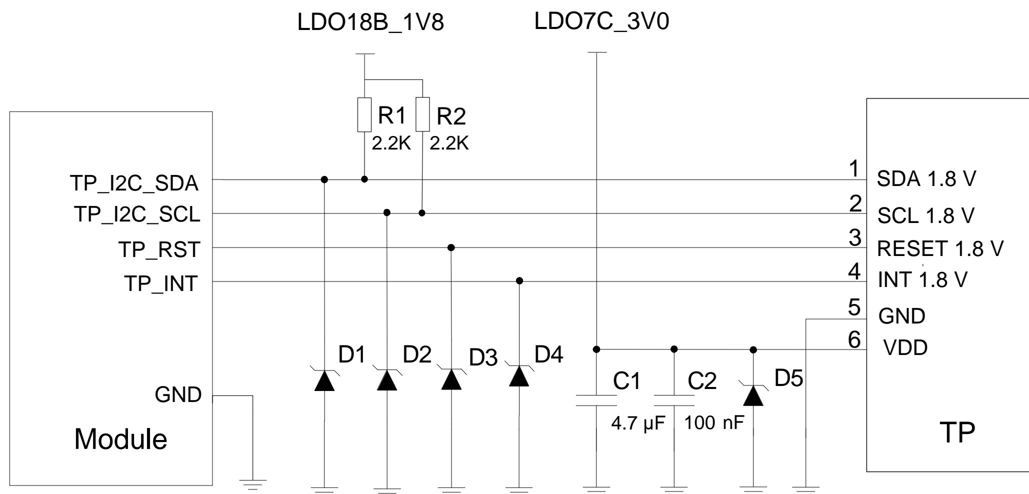


Figure 24: Reference Circuit for TP Interface

4.13. Camera Interfaces

Based on the MIPI CSI standard, the module provides four 4-lane MIPI CSI with maximum transmission rate of 2.5 Gbps/lane. The module supports two cameras (4-lane + 4-lane), or three cameras (4-lane + 4-lane + 4-lane), or five cameras (4-lane + 4-lane + 4-lane + 2-lane + 1-lane). The video and photo quality are determined by various factors such as the camera sensor, camera lens quality.

Table 28: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
VREG_L1P_1P05	116	PO	DVDD for cameras 1 and 2	When using them, it is recommended to add bypass capacitors with a total capacitance not exceeding 45.3 μF.
VREG_L2P_1P1	121	PO	DVDD for cameras 0 and 3	
VREG_L3P_2P8	113	PO	AVDD for cameras 1 and 3	When using them, it is recommended to add bypass capacitors with a total capacitance not exceeding 19 μF.
VREG_L4P_2P9	124	PO	AVDD for camera 0	
VREG_L5P_2P8	128	PO	AFVDD for camera 0	
VREG_L6P_1P8	117	PO	DOVDD for cameras 0, 1, 2 and 3	

VREG_L7P_2P8	120	PO	AVDD for camera 2	
CSI0_CLK_P	14	AI	MIPI CSI0 clock (+)	Requires differential impedance of 85 Ω.
CSI0_CLK_N	18	AI	MIPI CSI0 clock (-)	
CSI0_LN0_P	16	AI	MIPI CSI0 lane 0 data (+)	
CSI0_LN0_N	17	AI	MIPI CSI0 lane 0 data (-)	
CSI0_LN1_P	20	AI	MIPI CSI0 lane 1 data (+)	
CSI0_LN1_N	21	AI	MIPI CSI0 lane 1 data (-)	
CSI0_LN2_P	24	AI	MIPI CSI0 lane 2 data (+)	
CSI0_LN2_N	25	AI	MIPI CSI0 lane 2 data (-)	
CSI0_LN3_P	28	AI	MIPI CSI0 lane 3 data (+)	
CSI0_LN3_N	29	AI	MIPI CSI0 lane 3 data (-)	
CAM0_MCLK	30	DO	Master clock of camera 0	
CAM0_RST	26	DO	Reset of camera 0	
CSI1_CLK_P	38	AI	MIPI CS1 clock (+)	Requires differential impedance of 85 Ω.
CSI1_CLK_N	42	AI	MIPI CSI1 clock (-)	
CSI1_LN0_P	40	AI	MIPI CSI1 lane 0 data (+)	
CSI1_LN0_N	41	AI	MIPI CSI1 lane 0 data (-)	
CSI1_LN1_P	44	AI	MIPI CSI1 lane 1 data (+)	
CSI1_LN1_N	45	AI	MIPI CSI1 lane 1 data (-)	
CSI1_LN2_P	48	AI	MIPI CSI1 lane 2 data (+)	
CSI1_LN2_N	49	AI	MIPI CSI1 lane 2 data (-)	
CSI1_LN3_P	52	AI	MIPI CSI1 lane 3 data (+)	
CSI1_LN3_N	53	AI	MIPI CSI1 lane 3 data (-)	
CAM1_MCLK	54	DO	Master clock of camera 1	
CAM1_RST	50	DO	Reset of camera 1	

CSI2_CLK_P	390	AI	MIPI CSI2 clock (+)	Requires differential impedance of 85 Ω.
CSI2_CLK_N	386	AI	MIPI CSI2 clock (-)	
CSI2_LN0_P	392	AI	MIPI CSI2 lane 0 data (+)	
CSI2_LN0_N	389	AI	MIPI CSI2 lane 0 data (-)	
CSI2_LN1_P	388	AI	MIPI CSI2 lane 1 data (+)	
CSI2_LN1_N	385	AI	MIPI CSI2 lane 1 data (-)	
CSI2_LN2_P	396	AI	MIPI CSI2 lane 2 data (+)	
CSI2_LN2_N	393	AI	MIPI CSI2 lane 2 data (-)	
CSI2_LN3_P	400	AI	MIPI CSI2 lane 3 data (+)	
CSI2_LN3_N	397	AI	MIPI CSI2 lane 3 data (-)	
CAM2_MCLK	398	DO	Master clock of camera 2	
CAM2_RST	384	DO	Reset of camera 2	
CSI3_CLK_P	62	AI	MIPI CSI3 clock (+)	Requires differential impedance of 85 Ω.
CSI3_CLK_N	66	AI	MIPI CSI3 clock (-)	
CSI3_LN0_P	60	AI	MIPI CSI3 lane 0 data (+)	
CSI3_LN0_N	61	AI	MIPI CSI3 lane 0 data (-)	
CSI3_LN1_P	68	AI	MIPI CSI3 lane 1 data (+)	
CSI3_LN1_N	69	AI	MIPI CSI3 lane 1 data (-)	
CSI3_LN2_P	64	AI	MIPI CSI3 lane 2 data (+)	
CSI3_LN2_N	65	AI	MIPI CSI3 lane 2 data (-)	
CSI3_LN3_P	72	AI	MIPI CSI3 lane 3 data (+)	
CSI3_LN3_N	73	AI	MIPI CSI3 lane 3 data (-)	
CAM3_MCLK	74	DO	Master clock of camera 3	
CAM3_RST	67	DO	Reset of camera 3	

The following is a reference circuit for dual-camera applications.

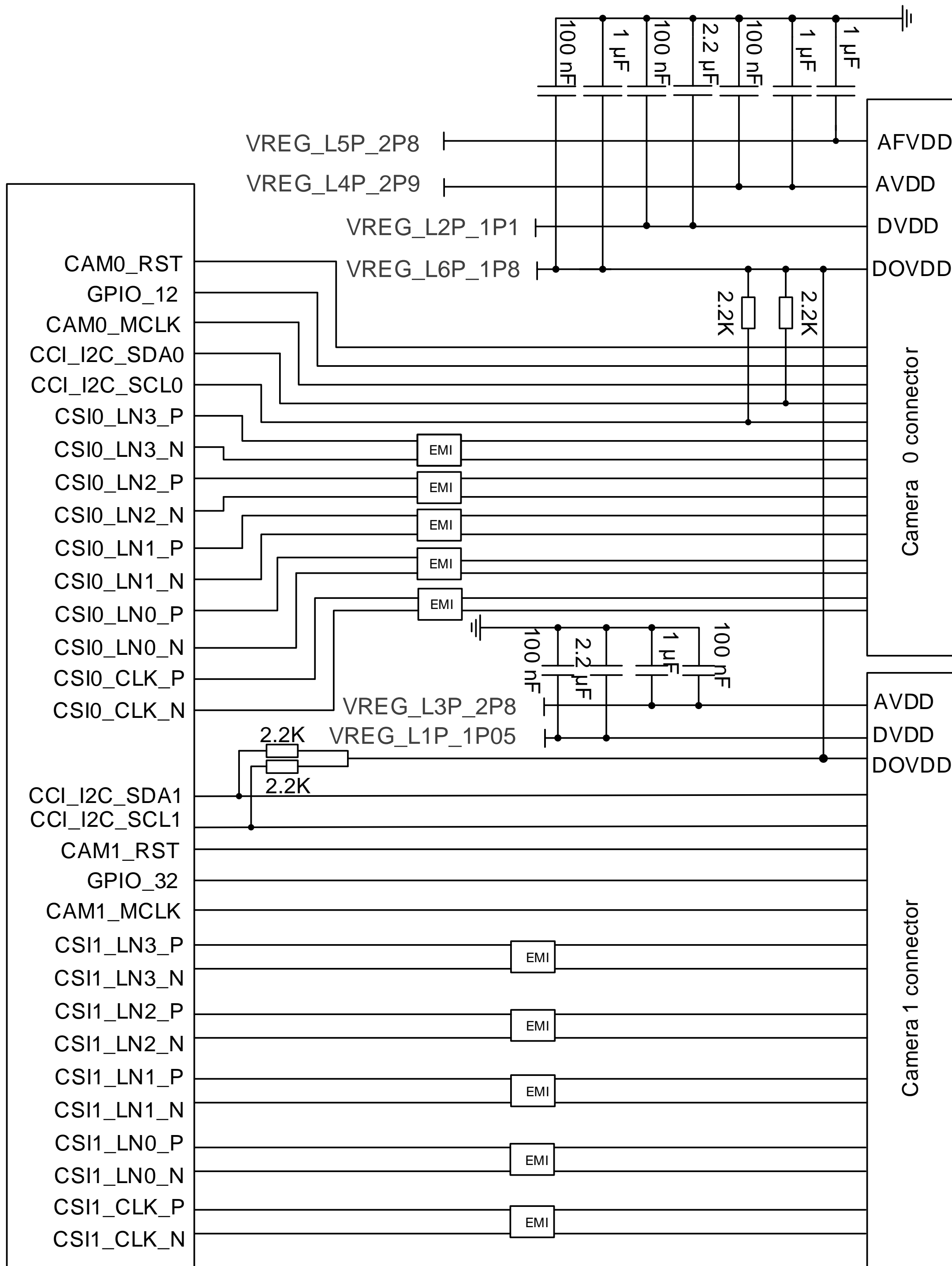


Figure 25: Reference Circuit for Dual-Camera Applications

The following is a reference circuit for tri-camera applications.

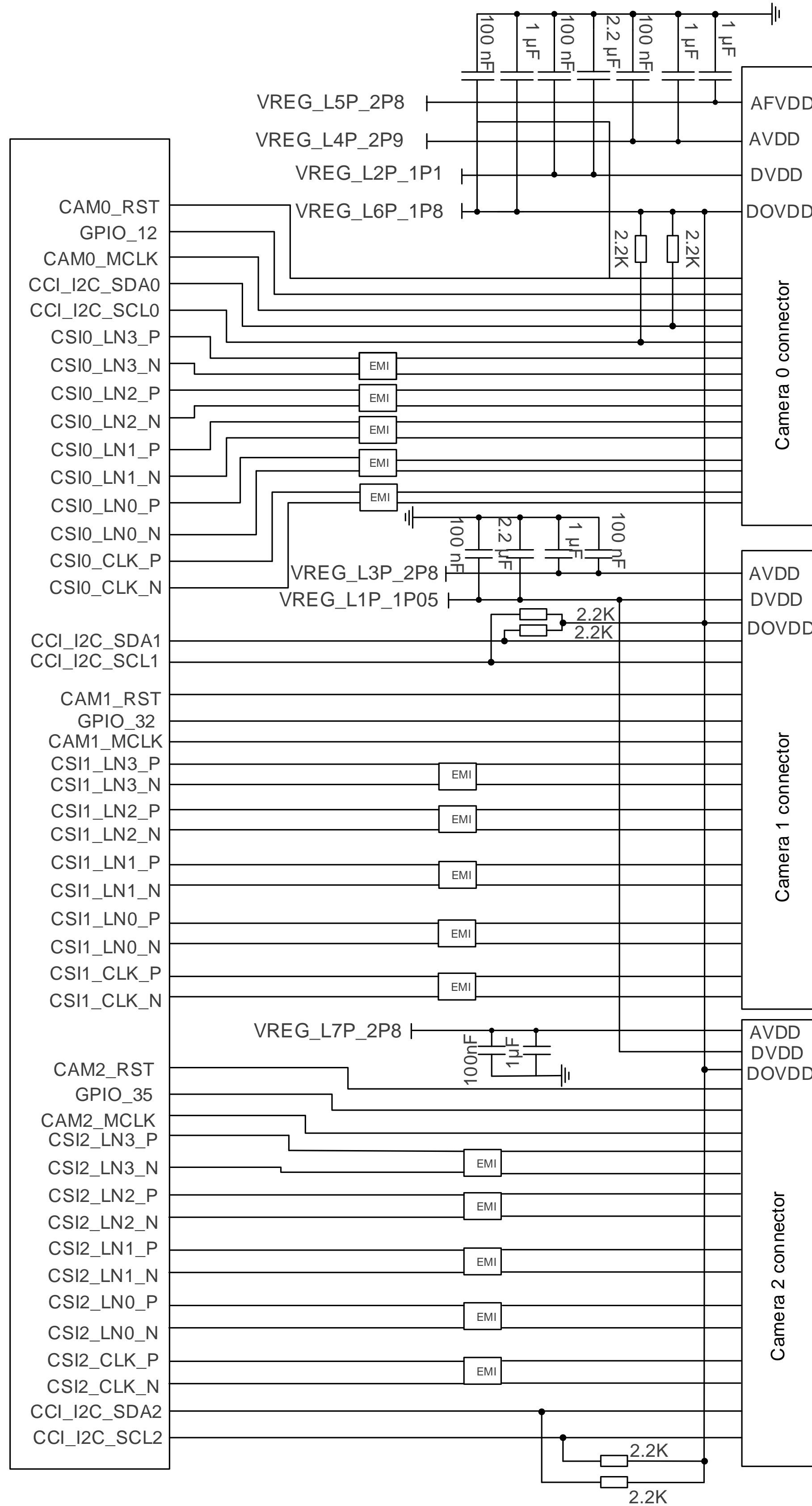


Figure 26: Reference Circuit for Three-Camera Applications

4.13.1. MIPI Design Considerations

- Special attention should be paid to the pin definition of LCM/camera connectors. Ensure that the module and the connectors are correctly connected.
- MIPI are high-speed signal lines, supporting maximum data rate of 2.5 Gbps/lane. The differential impedance should be controlled to 85 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB, and do not cross them with other traces. For the same group of DSI or CSI signals, keep all MIPI traces of the same length. To avoid crosstalk, a distance of 1.5 times the trace width among MIPI signal traces is recommended. During impedance matching, do not connect MIPI signal traces to GND on different planes to ensure impedance consistency.
- Make sure the reference ground plane for CSI/DSI is complete and integral without any cut or void.
- Route the camera CLK signals on the inner layer of the PCB and surround them with ground.
- Route CSI and DSI traces according to the following rules:
  - a) The intra-pair (P/N) spacing should be equal to the trace width.
  - b) The inter-pair spacing should be 1.5 times the trace width.
  - c) The spacing relative to other signal lines should be 2.5 times the trace width.
- Route MIPI traces according to the following rules:
  - a) Control the differential impedance to 85 Ω ±10 %.
  - b) Control intra-lane (P/N) length difference within 0.7 mm.
  - c) Control inter-lane length difference within 2.1 mm.

Table 29: Relationship Between CSI Rate and Line Length (D-PHY)

Data Rate	Cable Length (mm)	Cable Insertion Loss (Db)	Line Length (mm)
500 Mbps/Lane	76.2	-0.5	< 260
	152.4	-1	< 190
750 Mbps/Lane	76.2	-0.7	< 210
	152.4	-1.15	< 155
1.0 Gbps/Lane	76.2	-0.75	< 200
	152.4	-1.4	< 125
1.5 Gbps/Lane	76.2	-0.9	< 145
	152.4	-1.8	< 60
2.1 Gbps/Lane	76.2	-1.3	< 170
	152.4	-2.3	< 90
2.5 Gbps/Lane	76.2	-2.1	< 210
	152.4	-3.5	< 150

Table 30: Relationship Between DSI Rate and Line Length (D-PHY)

Data Rate	Cable Length (mm)	Cable Insertion Loss (Db)	Line Length (mm)
500 Mbps/Lane	76.2	-0.5	< 280
	152.4	-1.0	< 210
750 Mbps/Lane	76.2	-0.7	< 210
	152.4	-1.15	< 150
1.0 Gbps/Lane	76.2	-0.75	< 200
	152.4	-1.4	< 100
1.5 Gbps/lane	76.2	-0.9	< 135
	152.4	-1.8	< 40
2.1 Gbps/lane	76.2	-1.3	< 150
	152.4	-2.3	< 80
2.5 Gbps/lane	76.2	-2.1	< 70
	152.4	-3.5	< 0

NOTE

1. The cable length listed above is an example with specified insertion loss.
2. The cable insertion loss can be obtained from the cable datasheet provided by the manufacturer. The cable insertion loss in the actual design should not be worse than those listed above.
3. The line length in the above table includes the length of the line inside the module.

Table 31: Trace Length of MIPI Differential Pairs Inside the Module

Pin No.	Pin Name	Length (mm)	Length Mismatch (P – N)
370	DSI_CLK_N	25.99	-0.28
366	DSI_CLK_P	25.71	
377	DSI_LN0_N	25.78	0.31
380	DSI_LN0_P	26.09	
373	DSI_LN1_N	26.18	-0.14

376	DSI_LN1_P	26.04	
369	DSI_LN2_N	25.64	0.13
372	DSI_LN2_P	25.77	
365	DSI_LN3_N	25.92	0.01
368	DSI_LN3_P	25.93	
18	CSI0_CLK_N	45.08	0.01
14	CSI0_CLK_P	45.09	
17	CSI0_LN0_N	44.98	-0.01
16	CSI0_LN0_P	44.97	
21	CSI0_LN1_N	45.11	-0.07
20	CSI0_LN1_P	45.04	
25	CSI0_LN2_N	45.26	-0.04
24	CSI0_LN2_P	45.22	
29	CSI0_LN3_N	45.09	-0.01
28	CSI0_LN3_P	45.08	
42	CSI1_CLK_N	41.66	0.03
38	CSI1_CLK_P	41.69	
41	CSI1_LN0_N	41.70	0.05
40	CSI1_LN0_P	41.75	
45	CSI1_LN1_N	41.46	0.15
44	CSI1_LN1_P	41.61	
49	CSI1_LN2_N	41.86	-0.14
48	CSI1_LN2_P	41.72	
53	CSI1_LN3_N	41.72	0.07
52	CSI1_LN3_P	41.79	
386	CSI2_CLK_N	40.69	0.00
390	CSI2_CLK_P	40.69	
389	CSI2_LN0_N	40.68	0.17

392	CSI2_LN0_P	40.85	
385	CSI2_LN1_N	40.95	-0.04
388	CSI2_LN1_P	40.91	
393	CSI2_LN2_N	40.50	0.23
396	CSI2_LN2_P	40.73	
397	CSI2_LN3_N	41.03	-0.20
400	CSI2_LN3_P	40.83	
66	CSI3_CLK_N	39.40	-0.15
62	CSI3_CLK_P	39.25	
61	CSI3_LN0_N	39.31	0.10
60	CSI3_LN0_P	39.41	
69	CSI3_LN1_N	39.39	-0.04
68	CSI3_LN1_P	39.35	
65	CSI3_LN2_N	39.39	0.06
64	CSI3_LN2_P	39.45	
73	CSI3_LN3_N	39.51	-0.12
72	CSI3_LN3_P	39.39	

4.14. Sensor Interfaces

The module supports communication with sensors via I2C interface, and supports various sensors such as acceleration sensor, gyroscopic sensor, compass, and light sensor.

Table 32: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ACCEL_GYRO_INT1	161	DI	Acceleration/ gyroscope sensor interrupt 1	1.8 V power domain.
ACCEL_GYRO_INT2	158	DI	Acceleration/ gyroscope sensor interrupt 2	

MAG_INT	186	DI	Geomagnetic sensor interrupt	
ALPS_INT	157	DI	Light/proximity sensor interrupt	
HALL_INT	190	DI	Hall sensor interrupt	

4.15. Forced Download Interface

USB_BOOT is a forced download interface. Pulling it up to LDO18B_1V8 during power-up will force the module into download mode. This is a forced option when failures such as abnormal start-up or running occur. For the convenient firmware upgrade and debugging in the future, please reserve this pin.

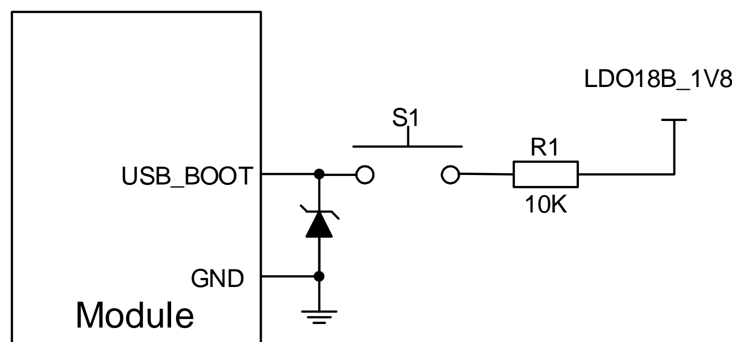


Figure 27: Reference Circuit for Forced Download Interface

4.16. PCIe Interface

The module provides one PCIe interface, which supports 2-lane PCIe Gen 3 with data rate up to 8 Gbps.

Table 33: Pin Definition of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE1_REFCLK_P	594	AIO	PCIe1 reference clock (+)	Requires differential impedance of 85 Ω.
PCIE1_REFCLK_M	593	AIO	PCIe1 reference clock (-)	
PCIE1_RX0_P	597	AI	PCIe1 recive 0 (+)	
PCIE1_RX0_M	596	AI	PCIe1 recive 0 (-)	

PCIE1_RX1_P	599	AI	PCIe1 recive 1 (+)	
PCIE1_RX1_M	598	AI	PCIe1 recive 1 (-)	
PCIE1_TX0_P	601	AO	PCIe1 transmit 0 (+)	
PCIE1_TX0_M	600	AO	PCIe1 transmit 0 (-)	
PCIE1_TX1_P	603	AO	PCIe1 transmit 1 (+)	
PCIE1_TX1_M	602	AO	PCIe1 transmit 1 (-)	
PCIE1_RST_N	605	DO	PCIe1 reset	
PCIE1_CLKREQ_N	606	DI	PCIe1 clock request	1.8 V power domain.
PCIE1_WAKE_N	607	DI	PCIe1 wake up	

Table 34: Trace Length of Differential Pairs Inside the Module

Pin No.	Signal	Length (mm)	Length Mismatch (P – M)
594	PCIE1_REFCLK_P	19.71	0.22
593	PCIE1_REFCLK_M	19.49	
601	PCIE1_TX0_P	28.55	0.00
600	PCIE1_TX0_M	28.55	
603	PCIE1_TX1_P	34.65	-0.23
602	PCIE1_TX1_M	34.88	
597	PCIE1_RX0_P	19.58	0.27
596	PCIE1_RX0_M	19.31	
599	PCIE1_RX1_P	21.84	0.22
598	PCIE1_RX1_M	21.62	

4.17. NFC Interface*

The module provides one NFC interface.

Table 35: Pin Definition of NFC Interface

Pin Name	Pin No.	I/O	Description	Comment
NFC_CLK	95	DO	NFC clock	
NFC_CLK_REQ	102	DI	NFC clock request	
NFC_DWL_REQ	103	DO	NFC download control request	
NFC_EN	98	DO	NFC enable	Internally pulled up by default.
NFC_INT	99	DI	NFC interrupt	
NFC_I2C_SDA	106	OD	NFC I2C data	External 1.8 V pull-up is required. If not used, keep them unconnected.
NFC_I2C_SCL	107	OD	NFC I2C clock	

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

The pin definition is shown below:

Table 36: Pin Definition of Cellular Network Interfaces of SG560D-CE

Pin Name	Pin No.	I/O	Description
ANT0	211	AIO	5G NR: LB DRX & MHB TRX (n41 DRX) LTE: LB DRX & MHB TRX (B38/B41 DRX) WCDMA: LB DRX & MHB TRX
ANT1	220	AIO	5G NR: n78/n79 TRX
ANT2	244	AIO	5G NR: n1 PRX MIMO & n78/n79 PRX MIMO & n41 DRX MIMO LTE: MHB PRX MIMO
ANT3	268	AIO	5G NR: n1 DRX MIMO & n78/n79 DRX MIMO & n41 PRX MIMO LTE: MHB DRX MIMO
ANT4	280	AIO	5G NR: LB TRX & MHB DRX (n41 TRX) & n78/n79 DRX LTE: LB TRX & MHB DRX (B38/B41 TRX) WCDMA: LB TRX & MHB DRX

Table 37: Pin Definition of Cellular Network Interfaces of SG560D-EM

Pin Name	Pin No.	I/O	Description
ANT0	211	AIO	5G NR: LB DRX & MHB TRX0 LTE: LB DRX & MHB TRX WCDMA: LB DRX & MHB TRX GSM: DCS1800/PCS1900 TRX
ANT1	220	AIO	5G NR: n77/n78/n79 TRX0 LTE: B42 TRX
ANT2	244	AIO	5G NR: MHB PRX MIMO & n77/n78/n79 PRX MIMO LTE: MHB PRX MIMO & B42 PRX MIMO & B32 PRX & LB + LB EN-DC PRX
ANT3	268	AIO	5G NR: MHB DRX MIMO & n77/n78/n79 DRX MIMO LTE: MHB DRX MIMO & B42 DRX MIMO & B32 DRX & LB + LB EN-DC DRX
ANT4	280	AIO	5G NR: LB TRX & MHB TX1 + DRX & n77/n78/n79 TX1 + DRX LTE: LB TRX & MHB DRX & B42 DRX WCDMA: LB TRX & MHB DRX GSM: GSM850/EGSM900 TRX

Table 38: Pin Definition of Cellular Network Interfaces of SG560D-NA

Pin Name	Pin No.	I/O	Description
ANT0	211	AIO	5G NR: LB DRX & MHB TRX LTE: LB DRX & MHB TRX
ANT1	220	AIO	5G NR: n77/n78 TRX0 LTE: B42/B43/B48 TRX & B46 PRX
ANT2	244	AIO	5G NR: MHB PRX MIMO & n77/n78 PRX MIMO LTE: MHB PRX MIMO & B46 DRX & B5 EN-DC PRX
ANT3	268	AIO	5G NR: MHB DRX MIMO & n77/n78 DRX MIMO LTE: MHB DRX MIMO & B5 EN-DC DRX
ANT4	280	AIO	5G NR: LB TRX & MHB TX1 + DRX & n77/n78 TX1 + DRX LTE: LB TRX & MHB DRX

Table 39: Operating Frequency of SG560D-CE

Operating Frequency	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
IMT (2100)	1920–1980	2110–2170	B1	-	B1	n1
DCS (1800)	1710–1785	1805–1880	B3	-	-	n3
Cell (850)	824–849	869–894	B5	-	B5	n5
EGSM (950)	880–915	925–960	B8	-	B8	n8
700 APAC	703–748	758–803	-	-	-	n28
B34	2010–2025	2010–2025	-	B34	-	-
B38	2570–2620	2570–2620	-	B38	-	-
B39	1880–1920	1880–1920	-	B39	-	-
B40	2300–2400	2300–2400	-	B40	-	-
B41/B41-XGP	2496–2690	2496–2690	-	B41	-	n41
n78	3300–3800	3300–3800	-	-	-	n78
n79	4400–5000	4400–5000	-	-	-	n79

Table 40: Operating Frequency of SG560D-EM

Operating Frequency	Transmit (MHz)	Receive (MHz)	GSM	LTE-FDD	LTE-TDD	UMTS	5G NR
IMT (2100)	1920–1980	2110–2170	-	B1	-	B1	n1
B2	1850–1910	1930–1990	PCS1900	B2	-	B2	-
B3	1710–1785	1805–1880	DCS1800	B3	-	-	n3
B4	1710–1755	2110–2155	-	B4	-	B4	
B5	824–849	869–894	GSM850	B5	-	B5	n5
B6	830–840	875–885	-	-	-	B6	
B7	2500–2570	2620–2690	-	B7	-	-	n7
B8	880–915	925–960	GSM900	B8	-	B8	n8

B12	699–716	729–746	-	B12	-	-	-
B17	704–716	734–746	-	B17	-	-	-
B18	815–830	860–875	-	B18	-	-	-
B19	830–845	875–890	-	B19	-	B19	-
B20	832–862	791–821	-	B20	-	-	n20
B26	814–849	859–894	-	B26			
B28	703–748	758–803	-	B28	-	-	n28
B32	-	1452–1496	-	B32	-	-	-
B34	2010–2025	2010–2025	-	-	B34	-	-
B38	2570–2620	2570–2620	-	-	B38	-	n38
B39	1880–1920	1880–1920	-	-	B39	-	-
B40	2300–2400	2300–2400	-	-	B40	-	n40
B41/B41-XGP	2496–2690	2496–2690	-	-	B41	-	n41
B42	3400–3600	3400–3600	-	-	B42	-	-
n77	3300–4200	3300–4200	-	-	-	-	n77
n78	3300–3800	3300–3800	-	-	-	-	n78
n79	4400–5000	4400–5000	-	-	-	-	n79

Table 41: Operating Frequency of SG560D-NA

Operating Frequency	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	5G NR
B2	1850–1910	1930–1990	B2	-	n2
B4	1710–1754.9	2110–2154.9	B4	-	-
B5	824–849	869–894	B5	-	n5
B7	2500–2570	2620–2690	B7	-	n7
B12	699–716	729–746	B12	-	n12

B13	777–787	746–756	B13	-	n13
B14	788–798	758–768	B14	-	n14
B17	704–716	734–746	B17	-	-
B25	1850–1915	1930–1995	B25	-	n25
B26	814–849	859–894	B26	-	n26
B29	-	717–728	B29	-	n29
B30	2305–2315	2350–2360	B30	-	n30
B66	1710–1780	2110–2200	B66	-	n66
n70	1695–1710	1995–2020	-	-	n70
B71	663–698	617–652	B71	-	n71
B38	2570–2620	2570–2620	-	B38	n38
B41/B41-XGP	2496–2690	2496–2690	-	B41	n41
B42	3400–3600	3400–3600	-	B42	-
B43	3600–3800	3600–3800	-	B43	-
B46	5150–5925	5150–5925	-	B46	-
B48	3550–3700	3550–3700	-	B48	n48
n77	3300–4200	3300–4200	-	-	n77
n78	3300–3800	3300–3800	-	-	n78

5.1.2. Transmitting Power

The following table shows the RF output power of the module.

Table 42: Tx Power of SG560D-CE

Mode	Frequency Range	Max.	Min.
WCDMA	WCDMA bands	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	LTE HPUE band (B41)	26 dBm ±2 dB (Class 2)	< -40 dBm
	Other LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm

5G NR	5G NR HPUE bands (n41/n78/n79)	26 dBm +2/-3 dB (Class 2)	< -40 dBm [10]
	Other 5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm [10]

Table 43: Tx Power of SG560D-EM

Mode	Frequency Range	Max.	Min.
GSM	EGSM900/GSM850	33 dBm ±2 dB	5 dBm ±5 dB
	DCS1800/PCS1900	30 dBm ±2 dB	0 dBm ±5 dB
WCDMA	WCDMA bands	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	LTE HPUE band (B41)	26 dBm ±2 dB (Class 2)	< -40 dBm
	Other LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
5G NR	5G NR HPUE bands (n41/n77/n78/n79)	26 dBm +2/-3 dB (Class 2)	< -40 dBm [10]
	Other 5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm [10]

Table 44: Tx Power of SG560D-NA

Mode	Frequency Range	Max.	Min.
LTE	LTE HPUE band (B41)	26 dBm ±2 dB (Class 2)	< -40 dBm
	Other LTE bands	23 dBm ±2 dB (Class 3)	< -40 dBm
5G NR	5G NR HPUE bands (n41/n77/n78)	26 dBm +2/-3 dB (Class 2)	< -40 dBm [10]
	Other 5G NR bands	23 dBm ±2 dB (Class 3)	< -40 dBm [10]

[10] For 5G NR frequency band, there are different minimum power standards under different channel bandwidths. For details, see ***clause 6.3.1*** of *TS 38.101-1 [2]*.

5.1.3. Rx Sensitivity

The following table shows conducted RF receiving sensitivity of the module.

Table 45: Conducted RF Rx Sensitivity of SG560D-CE (Unit:dBm)

Mode	Frequency	Primary	Diversity	SIMO [11]	3GPP (SIMO)
WCDMA	WCDMA B1	-109.9	-109.8	-	-106.7
	WCDMA B5	-110.7	-113	-	-104.7
	WCDMA B8	-110.8	-112.9	-	-103.7
LTE	LTE-FDD B1 (10 MHz)	-97.4	-98.1	-103.4	-96.3
	LTE-FDD B3 (10 MHz)	-98.2	-97.3	-100.7	-93.3
	LTE-FDD B5 (10 MHz)	-98.3	-100.5	-102.6	-94.3
	LTE-FDD B8 (10 MHz)	-98.3	-100.2	-102.5	-93.3
	LTE- TDD B34 (10 MHz)	-97.6	-97.9	-100.7	-96.3
	LTE- TDD B38 (10 MHz)	-97.2	-96.1	-99.6	-96.3
	LTE- TDD B39 (10 MHz)	-98.1	-97.5	-100.9	-96.3
	LTE- TDD B40 (10 MHz)	-96.7	-96.9	-99.9	-96.3
	LTE- TDD B41 (10 MHz)	-96.7	-96.3	-101	-94.3
5G NR	5G NR FDD n1 (40 MHz)	-90.7	-91.2	-97	-90.6
	5G NR FDD n3 (20 MHz)	-94.3	-94	-97.3	-90.8
	5G NR FDD n5 (20 MHz)	-94.8	-96.3	-98.4	-86.8
	5G NR FDD n8 (20 MHz)	-94.6	-96.2	-98.4	-85.8
	5G NR FDD n28 (30 MHz)	-92.2	-93.4	-97.2	-78.5
	5G NR TDD n41 (100 MHz)	-86	-84.9	-90.9	-87.4
	5G NR TDD n78 (100 MHz)	-89.4	-89	-93.9	-87.8
	5G NR TDD n79 (100 MHz)	-88.6	-89.2	-91.4	-87.8

[11] For the SIMO receiving sensitivity, WCDMA and LTE B3/B5/B8/B34/B38/B39/B40 bands and 5G NR n3/n5/n8/n28 are tested with 2 RX antennas, and LTE B1/B41 bands and 5G NR n1/n41/n78/n79 bands are tested with 4 RX antennas.

Table 46: Conducted RF Rx Sensitivity of SG560D-EM (Unit:dBm)

Mode	Frequency	Primary	Diversity	SIMO [12]	3GPP (SIMO)
GSM	GSM850	-110	-	-	-102.4
	EGSM900	-109	-	-	-102.4
	DCS1800	-109	-	-	-102.4
	PCS1900	-108.5	-	-	-102.4
WCDMA	WCDMA B1	-110	-109.5	-	-106.7
	WCDMA B2	-110	-110	-	-104.7
	WCDMA B4	-110	-109.5	-	-106.7
	WCDMA B5	-112	-110.5	-	-104.7
	WCDMA B6	-112	-110.5	-	-106.7
	WCDMA B8	-111.5	-111	-	-103.7
	WCDMA B19	-112	-110.5	-	-106.7
LTE	LTE-FDD B1 (10 MHz)	-96.5	-96.5	-102	-96.3
	LTE-FDD B2 (10 MHz)	-97.5	-97.7	-101	-94.3
	LTE-FDD B3 (10 MHz)	-98	-97	-102.5	-93.3
	LTE-FDD B4 (10 MHz)	-96.5	-96.5	-99.5	-96.3
	LTE-FDD B5 (10 MHz)	-99	-98	-101.5	-94.3
	LTE-FDD B7 (10 MHz)	-96	-97	-102	-94.3
	LTE-FDD B8 (10 MHz)	-98	-97.5	-100.8	-93.3
	LTE-FDD B12 (10 MHz)	-98.2	-99	-101.8	-93.3
	LTE-FDD B17 (10 MHz)	-98	-99	-101.5	-93.3
	LTE-FDD B18 (10 MHz)	-98.6	-98	-101.3	-96.3
	LTE-FDD B19 (10 MHz)	-99	-98	-101.5	-96.3
	LTE-FDD B20 (10 MHz)	-98.3	-98.5	-101.5	-93.3
	LTE-FDD B26 (10 MHz)	-98.6	-98	-101.3	-93.8

[12] For the SIMO receiving sensitivity, WCDMA and LTE B2/B4/B5/B8/B12/B17/B18/B19/B20/B26/B28/B32/B34/B39 bands and 5G NR n5/n8/n20/n28 bands are tested with 2 RX antennas, and LTE B1/B3/B7/B38/B40/B41/B42 bands and 5G NR n1/n3/n7/n38/n40/n41/n77/n78/n79 bands are tested with 4 RX antennas.

	LTE-FDD B28 (10 MHz)	-98.5	-98.7	-101.6	-94.8
	LTE-FDD B32 (10 MHz)	TBD	TBD	TBD	-95.3
	LTE-TDD B34 (10 MHz)	-97.5	-97.5	-100.5	-96.3
	LTE-TDD B38 (10 MHz)	-95.5	-97	-101.5	-96.3
	LTE-TDD B39 (10 MHz)	-97.7	-97.7	-100.7	-96.3
	LTE-TDD B40 (10 MHz)	-95.5	-96	-101.5	-96.3
	LTE-TDD B41 (10 MHz)	-95	-96	-101	-94.3
	LTE-TDD B42 (10 MHz)	-98	-97.5	-103	-95
5G NR	5G NR FDD n1 (40 MHz)	-91	-91.6	-96.5	-90.6
	5G NR FDD n3 (20 MHz)	-95.5	-94.5	-100	-90.8
	5G NR FDD n5 (20 MHz)	-95	-95.2	-98	-86.8
	5G NR FDD n7 (20 MHz)	-93.7	-94	-99.8	-91.8
	5G NR FDD n8 (20 MHz)	-94.5	-94.5	-97.5	-85.8
	5G NR FDD n20 (20 MHz)	-95.6	-95.9	-98.4	-89.8
	5G NR FDD n28 (30 MHz)	-93	-93.4	-97	-78.5
	5G NR TDD n38 (40 MHz)	-91	-90	-97	-90.7
	5G NR TDD n40 (80 MHz)	-88	-87.3	-93.5	-87.6
	5G NR TDD n41 (100 MHz)	-86.5	-85.5	-92.4	-87.4
	5G NR TDD n77 (100 MHz)	-89	-89	-93	-87.3
	5G NR TDD n78 (100 MHz)	-89	-89	-94.3	-87.8
	5G NR TDD n79 (100 MHz)	-88.5	-89	-94.5	-87.8

Table 47: Conducted RF Rx Sensitivity of SG560D-NA (Unit: dBm)

Mode	Frequency	Primary	Diversity	SIMO [13]	3GPP (SIMO)
LTE	LTE-FDD B2 (10 MHz)	-98	-98.6	-103.7	-94.3
	LTE-FDD B4 (10 MHz)	-97	-97.6	-102.7	-96.3

[13] For the SIMO receiving sensitivity, LTE B5/B12/B13/B14/B17/B26/B29/B46/B71 bands and 5G NR n5/n12/n13/n14/n26/n29/n71 bands are tested with 2 RX antennas, and LTE B2/B4/B7/B25/B30/B38/B41/B42/B43/B48/B66 bands and 5G NR n2/n7/n25/n30/n38/n41/n48/n66/n70/n77/n78 bands are tested with 4 RX antennas.

	LTE-FDD B5 (10 MHz)	-98.7	-99.7	-102.1	-94.3
	LTE-FDD B7 (10 MHz)	-96.3	-96.2	-102.1	-94.3
	LTE-FDD B12 (10 MHz)	-98.3	-99.1	-101.7	-93.3
	LTE-FDD B13 (10 MHz)	-98.5	-99.3	-101.9	-93.3
	LTE-FDD B14 (10 MHz)	-98.1	-99.1	-101.7	-93.3
	LTE-FDD B17 (10 MHz)	-98.2	-99.5	-101.9	-93.3
	LTE-FDD B25 (10 MHz)	-97.8	-98.4	-103.6	-92.8
	LTE-FDD B26 (10 MHz)	-98.4	-99.6	-102.1	-93.8
	LTE-FDD B29 (10 MHz)	TBD	TBD	-101.7	-93.3
	LTE-FDD B30 (10 MHz)	-96.4	-96	-101	-95.3
	LTE-FDD B66 (10 MHz)	-96.5	-97.5	-102.4	-95.8
	LTE-FDD B71 (10 MHz)	-98.6	TBD	-102.6	-93.5
	LTE-TDD B38 (10 MHz)	-96.5	-95.4	-101.4	-96.3
	LTE-TDD B41 (10 MHz)	-96.4	-94.6	-101	-94.3
	LTE-TDD B42 (10 MHz)	-96.7	-97.4	-102.5	-95
	LTE- TDD B43 (10 MHz)	-96.5	-97.5	-102.3	-95
	LTE-TDD B46 (20 MHz)	TBD	TBD	-97.3	TBD
	LTE-TDD B48 (10 MHz)	-96.6	-97.5	-102.3	-96
5G NR	5G NR FDD n2 (20 MHz)	-95.6	-96.3	-101.4	-94.5
	5G NR FDD n5 (20 MHz)	-95.9	-97	-99.4	-86.8
	5G NR FDD n7 (20 MHz)	-95	-94.3	-100.5	-94.5
	5G NR FDD n12 (15 MHz)	-96.9	-97	-98.9	-84
	5G NR FDD n13 (10 MHz)	-98.8	-99.9	-102.3	TBD
	5G NR FDD n14 (10 MHz)	-98.6	-99.6	-102	-93.8
	5G NR FDD n25 (20 MHz)	-95.6	-96.2	-101.1	-90.3
	5G NR FDD n26 (20 MHz)	-95.8	-96.9	-99.3	-87.6
	5G NR FDD n29 (20 MHz)	TBD	TBD	TBD	TBD
	5G NR FDD n30 (10 MHz)	-96.3	-96.2	-102.3	-95.8

	5G NR TDD n38 (40 MHz)	91.3	-90.6	97.3	-93.4
	5G NR TDD n41 (100 MHz)	-87	-86.6	-91.7	-87.4
	5G NR TDD n48 (40 MHz)	-92.2	-93.8	-98.4	-92.1
	5G NR FDD n66 (20 MHz)	-94.3	-94.3	-100.3	-93
	5G NR FDD n70 (15 MHz)	-96.8	-97.5	-101.9	-95
	5G NR FDD n71 (20 MHz)	-96.6	97.9	-99.9	-86
	5G NR TDD n77 (100 MHz)	-87.8	-89	-93.9	-87.3
	5G NR TDD n78 (100 MHz)	-87.9	-89	-93.9	-87.8

5.1.4. Reference Design of Cellular Antenna Interfaces

The module provides five RF antenna interfaces for antenna connection.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (a capacitor-resistor-capacitor group) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

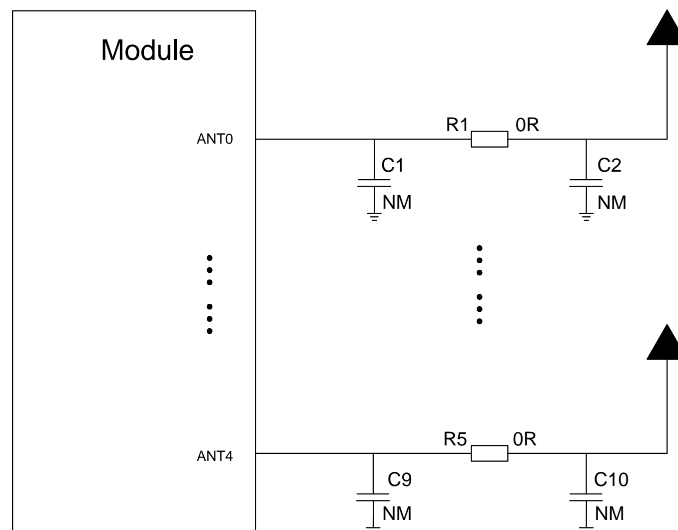


Figure 28: Reference Circuit for RF Antenna Interfaces

NOTE

It is recommended that the straight-line distance between the antenna and the module be greater than 15 mm to achieve better wireless performance of the whole device.

5.2. GNSS (Optional)

The module integrates the IZat™ GNSS engine (Gen 9) which supports multiple positioning and navigation systems including GPS, GLONASS, BDS, Galileo, NavIC, QZSS, SBAS. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.2.1. Antenna Interface & Frequency Bands

The following table shows the pin definition, frequency, and performance of GNSS antenna interface.

Table 48: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description
ANT_GNSS	302	AI	GNSS antenna interface

Table 49: Operating Frequency

Type	Frequency	Unit
GPS/SBAS/QZSS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)	MHz
GLONASS	1597.5–1605.8	
Galileo	1575.42 ±2.046 (E1) 1176.45 ±10.23 (E5a)	
BDS	1561.098 ±2.046	
NAVIC	1176.45 ±10.23 (L5)	

5.2.2. GNSS Performance

Table 50: GNSS Performance

Parameter	Description	Typ.	Unit
Sensitivity (GNSS)	Acquisition	-146	dBm
	Reacquisition	-158	
	Tracking	-159	

TTFF (GNSS)	Cold start @ open sky	33.21	s
	Warm start @ open sky	22.84	
	Hot start @ open sky	0.92	
Accuracy (GNSS)	CEP-50	2	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

5.2.3.1. Reference Design for GNSS Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

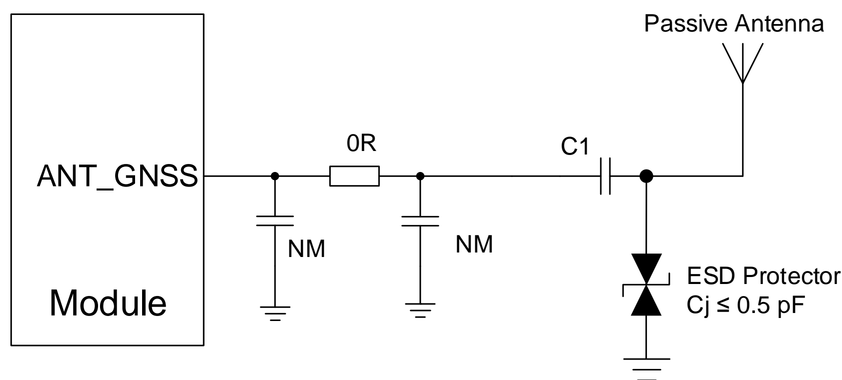


Figure 29: Reference Circuit for GNSS Passive Antenna

NOTE

It is not recommended to add an external LNA when using a passive GNSS antenna.

5.2.3.2. Reference Design for GNSS Active Antenna

In any case, it is recommended to use a passive antenna. However, if an active antenna is needed in your application, it is recommended to reserve a π-type attenuation circuit and use a high-performance LDO in the power system design. The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. A reference design of the GNSS active antenna is shown below.

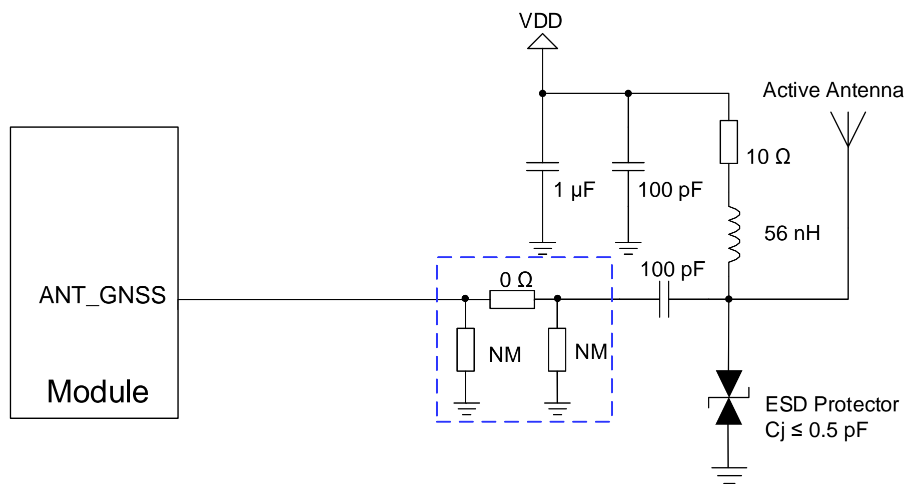


Figure 30: Reference Circuit for GNSS Active Antenna

5.2.3.3. GNSS RF Design Guidelines

Improper design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. To avoid this, follow the reference design rules as below:

- Maximize the distance between the GNSS RF part and the other RF part (including trace routing and antenna layout) to avoid mutual interference.
- In user systems, GNSS RF signal traces and RF components should be placed far away from high-speed circuits, switch-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For harsh electromagnetic environment or a design that requires better ESD protection, diodes with ultra-low junction capacitance such as 0.5 pF can be selected and added in the antenna interface. Otherwise, there will be effects on the impedance characteristic of the RF circuit loop or attenuation of the bypass RF signal may be caused.
- Control the impedance of either feeder line or PCB trace to 50 Ω, and keep the trace length as short as possible.
- Refer to ***Chapter 5.5*** for the GNSS reference circuit design.

5.3. Wi-Fi/Bluetooth

The module provides one shared antenna interface ANT_WIFI/BT to suppport Wi-Fi and Bluetooth functions. The interface impedance is 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna and ceramic antenna to the module via the interface to achieve Wi-Fi and Bluetooth functions. The module further provides one Wi-Fi antenna interface ANT_WIFI_MIMO to support Wi-Fi 2 × 2 MU-MIMO, 2.4 GHz, 5 GHz and 6 GHz tri-band function. The module complies with IEEE 802.11a/b/g/n/ac/ax and supports Dual Band Simultaneous (DBS) with dual MAC.

5.3.1. Antenna Interface & Frequency Bands

Table 51: Pin Definition of Wi-Fi/Bluetooth Interfaces

Pin Name	Pin No.	I/O	Description
ANT_WIFI/BT	92	AIO	Wi-Fi/Bluetooth antenna interface
ANT_WIFI_MIMO	86	AIO	Wi-Fi MIMO antenna interface

Table 52: Wi-Fi/Bluetooth Frequency

Type	Frequency	Unit
Wi-Fi 802.11a/b/g/n/ac/ax	2400–2483.5 5150–5850 5925–7125	MHz
Bluetooth 5.2	2402–2480	MHz

5.3.2. Wi-Fi Overview

The module supports 2.4 GHz, 5 GHz and 6 GHz tri-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac/ax standard protocols. The maximum data rate is 3.6 Gbps. The features are as below:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption
- Support AP and STA modes
- Support Wi-Fi Direct
- Support Dual Band Simultaneous (DBS)
- Support 20/40 MHz channel bandwidths for 2.4 GHz and 20/40/80/160 MHz channel bandwidths for 5 GHz and 6 GHz

- Support MCS 0–7 for HT20 and HT40
- Support MCS 0–8 for VHT20
- Support MCS 0–9 for VHT40 and VHT80
- Support MCS 0–13 for HE20, HE40, HE80 and HE160

The following table lists the Wi-Fi transmitting and receiving performance of the module.

Table 53: Wi-Fi Transmitting Performance

Frequency	Standard	Rate	Output
2.4 GHz	802.11b	1 Mbps	17 dBm ±2.5 dB
	802.11b	11 Mbps	17 dBm ±2.5 dB
	802.11g	6 Mbps	16 dBm ±2.5 dB
	802.11g	54 Mbps	15 dBm ±2.5 dB
	802.11n HT20	MCS0	16 dBm ±2.5 dB
	802.11n HT20	MCS7	14 dBm ±2.5 dB
	802.11n HT40	MCS0	16 dBm ±2.5 dB
	802.11n HT40	MCS7	14 dBm ±2.5 dB
	802.11ax HE20	MCS0	16 dBm ±2.5 dB
	802.11ax HE20	MCS11	11.5 dBm ±2.5 dB
	802.11ax HE20	MCS13	10 dBm ±2.5 dB
	802.11ax HE40	MCS0	16 dBm ±2.5 dB
	802.11ax HE40	MCS11	11.5 dBm ±2.5 dB
	802.11ax HE40	MCS13	10 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	16 dBm ±2.5 dB
	802.11a	54 Mbps	14 dBm ±2.5 dB
	802.11n HT20	MCS0	15 dBm ±2.5 dB
	802.11n HT20	MCS7	14 dBm ±2.5 dB
	802.11n HT40	MCS0	15 dBm ±2.5 dB

	802.11n HT40	MCS7	14 dBm ±2.5 dB
	802.11ac VHT20	MCS0	15 dBm ±2.5 dB
	802.11ac VHT20	MCS8	13 dBm ±2.5 dB
	802.11ac VHT40	MCS0	15 dBm ±2.5 dB
	802.11ac VHT40	MCS9	13 dBm ±2.5 dB
	802.11ac VHT80	MCS0	15 dBm ±2.5 dB
	802.11ac VHT80	MCS9	13 dBm ±2.5 dB
	802.11ax HE20	MCS0	16 dBm ±2.5 dB
	802.11ax HE20	MCS11	12 dBm ±2.5 dB
	802.11ax HE20	MCS13	10 dBm ±2.5 dB
	802.11ax HE40	MCS0	16 dBm ±2.5 dB
	802.11ax HE40	MCS11	11.5 dBm ±2.5 dB
	802.11ax HE40	MCS13	10 dBm ±2.5 dB
	802.11ax HE80	MCS0	16 dBm ±2.5 dB
	802.11ax HE80	MCS11	11.5 dBm ±2.5 dB
	802.11ax HE80	MCS13	10 dBm ±2.5 dB
	802.11ax HE160	MCS0	14 dBm ±2.5 dB
	802.11ax HE160	MCS11	11.5 dBm ±2.5 dB
	802.11ax HE160	MCS13	10 dBm ±2.5 dB
6 GHz	802.11a	6 Mbps	16 dBm ±2.5 dB
	802.11a	54 Mbps	14 dBm ±2.5 dB
	802.11ax HE20	MCS0	15 dBm ±2.5 dB
	802.11ax HE20	MCS11	12 dBm ±2.5 dB
	802.11ax HE20	MCS13	10 dBm ±2.5 dB
	802.11ax HE40	MCS0	15 dBm ±2.5 dB

	802.11ax HE40	MCS11	12 dBm ±2.5 dB
	802.11ax HE40	MCS13	10 dBm ±2.5 dB
	802.11ax HE80	MCS0	15 dBm ±2.5 dB
	802.11ax HE80	MCS11	12 dBm ±2.5 dB
	802.11ax HE80	MCS13	10 dBm ±2.5 dB
	802.11ax HE160	MCS0	14 dBm ±2.5 dB
	802.11ax HE160	MCS11	11 dBm ±2.5 dB
	802.11ax HE160	MCS13	10 dBm ±2.5 dB

Table 54: Wi-Fi Receiving Performance

Frequency	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-95 dBm
	802.11b	11 Mbps	-90 dBm
	802.11g	6 Mbps	-94 dBm
	802.11g	54 Mbps	-77 dBm
	802.11n HT20	MCS0	-93 dBm
	802.11n HT20	MCS7	-73 dBm
	802.11n HT40	MCS0	-89 dBm
	802.11n HT40	MCS7	-70 dBm
	802.11ax HE20	MCS0	-93 dBm
	802.11ax HE20	MCS11	-64 dBm
	802.11ax HE20	MCS13	-56 dBm
	802.11ax HE40	MCS0	-89 dBm
	802.11ax HE40	MCS11	-62 dBm
	802.11ax HE40	MCS13	-51 dBm

5 GHz	802.11a	6 Mbps	-93 dBm
	802.11a	54 Mbps	-76 dBm
	802.11n HT20	MCS0	-91 dBm
	802.11n HT20	MCS7	-73 dBm
	802.11n HT40	MCS0	-88 dBm
	802.11n HT40	MCS7	-70 dBm
	802.11ac VHT20	MCS0	-92 dBm
	802.11ac VHT20	MCS8	-70 dBm
	802.11ac VHT40	MCS0	-89 dBm
	802.11ac VHT40	MCS9	-66 dBm
	802.11ac VHT80	MCS0	-85 dBm
	802.11ac VHT80	MCS9	-63 dBm
	802.11ax HE20	MCS0	-91 dBm
	802.11ax HE20	MCS11	-63 dBm
	802.11ax HE20	MCS13	-56 dBm
	802.11ax HE40	MCS0	-88 dBm
	802.11ax HE40	MCS11	-61 dBm
	802.11ax HE40	MCS13	-54 dBm
	802.11ax HE80	MCS0	-86 dBm
	802.11ax HE80	MCS11	-57 dBm
	802.11ax HE80	MCS13	-51 dBm
	802.11ax HE160	MCS0	-83 dBm
	802.11ax HE160	MCS11	-55 dBm
	802.11ax HE160	MCS13	-47 dBm
6 GHz	802.11a	6 Mbps	-93 dBm
	802.11a	54 Mbps	-76 dBm

	802.11ax HE20	MCS0	-92 dBm
	802.11ax HE20	MCS11	-63 dBm
	802.11ax HE20	MCS13	-55 dBm
	802.11ax HE40	MCS0	-89 dBm
	802.11ax HE40	MCS11	-60 dBm
	802.11ax HE40	MCS13	-53 dBm
	802.11ax HE80	MCS0	-86 dBm
	802.11ax HE80	MCS11	-57 dBm
	802.11ax HE80	MCS13	-50 dBm
	802.11ax HE160	MCS0	-83 dBm
	802.11ax HE160	MCS11	-54 dBm
	802.11ax HE160	MCS13	-47 dBm

NOTE

The module conforms to the IEEE specifications.

5.3.3. Bluetooth Overview

The module supports Bluetooth 5.2 (BR/EDR+BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulation modes.

- Maximally support up to 7-lane wireless connections.
- Maximally support up to 3.5 Piconets at the same time.
- Support one SCO or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 55: Bluetooth Data Rate and Version

Version	Data Rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 kbit/s
2.0 + EDR	3 Mbit/s	> 80 kbit/s
3.0 + HS	24 Mbit/s	Refer to 3.0 + HS
4.0	24 Mbit/s	Refer to 4.0 LE
5.0	48 Mbit/s	Refer to 5.0 LE
5.1	TBD	Refer to 5.1 LE
5.2	TBD	Refer to 5.2 LE

Referenced specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016*

Table 56: Bluetooth Transmitting and Receiving Performance

Condition (VBAT = 4.0 V; Temp.: 25 °C)	Transmit Power	Receiver Sensitivity
BR	8 dBm ±2.5 dB	-93 dBm
EDR (π/4-DQPSK)	6 dBm ±2.5 dB	-94 dBm
EDR (8-DQPSK)	6 dBm ±2.5 dB	-88 dBm
BLE (1 Mbps)	0 dBm ±2.5 dB	-97 dBm
BLE (2 Mbps)	0 dBm ±2.5 dB	-95 dBm

5.3.4. Reference Design

A reference circuit design for Wi-Fi/Bluetooth antenna interface is shown as below. C1 and C2 are not mounted and a 0 Ω resistor is mounted on R1 by default.

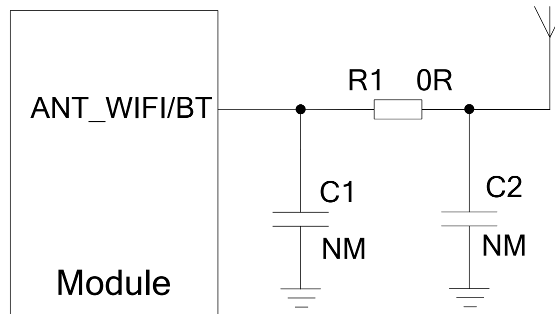


Figure 31: Reference Circuit for Wi-Fi/Bluetooth Antenna

A reference circuit design for Wi-Fi MIMO antenna interface is shown as below. C3 and C4 are not mounted and a 0 Ω resistor is mounted on R2 by default.

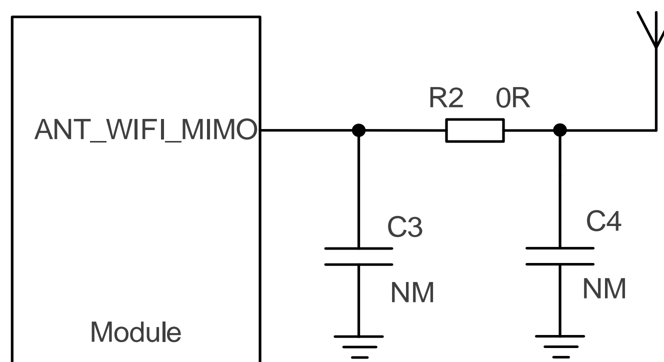


Figure 32: Reference Circuit for Wi-Fi MIMO Antenna

5.4. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

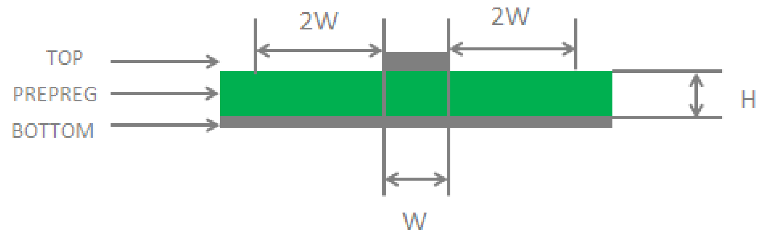


Figure 33: Microstrip Design on a 2-layer PCB

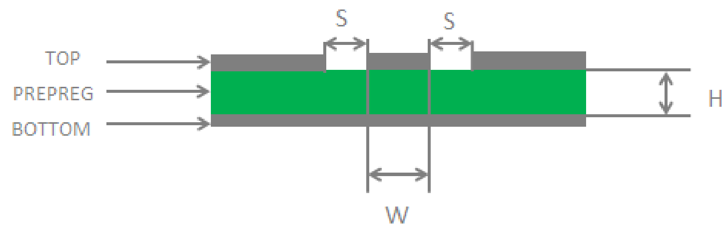


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

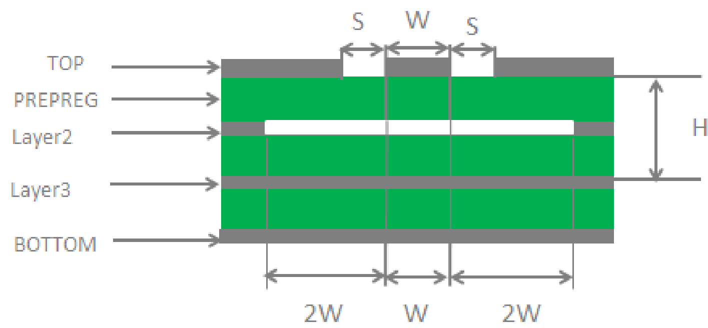


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

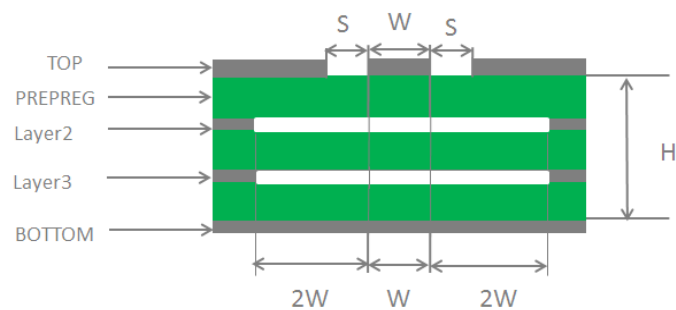


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between any traces on adjacent layers.

For more details about RF layout, see ***document [2]***.

5.5. Antenna Installation

5.5.1. Antenna Design Requirement

Requirements for antenna design are as follows:

Table 57: Antenna Design Requiremets

Antenna Type	Requirements
GNSS	● Frequency range: L1: 1559–1609 MHz L5: 1166–1187 MHz ● Polarization: RHCP or linear ● VSWR: ≤ 2 (Typ.)
	For passive antenna application: Passive antenna gain: > 0 dBi
	For active antenna application: Active antenna noise figure: < 1.5 dB Active antenna embedded LNA gain: < 17 dB
Cellular	● VSWR: ≤ 2 ● Gain: 1 dBi ● Max Input Power: 50 W ● Input Impedance: 50 Ω ● Polarization Type: Vertical

	● Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)
Wi-Fi/Bluetooth	● VSWR: ≤ 2 ● Gain: 1 dBi ● Max Input Power: 50 W ● Input Impedance: 50 Ω ● Polarization Type: Vertical ● Cable Insertion Loss: **< 1 dB:** LB (<1 GHz)

5.5.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by Hirose.

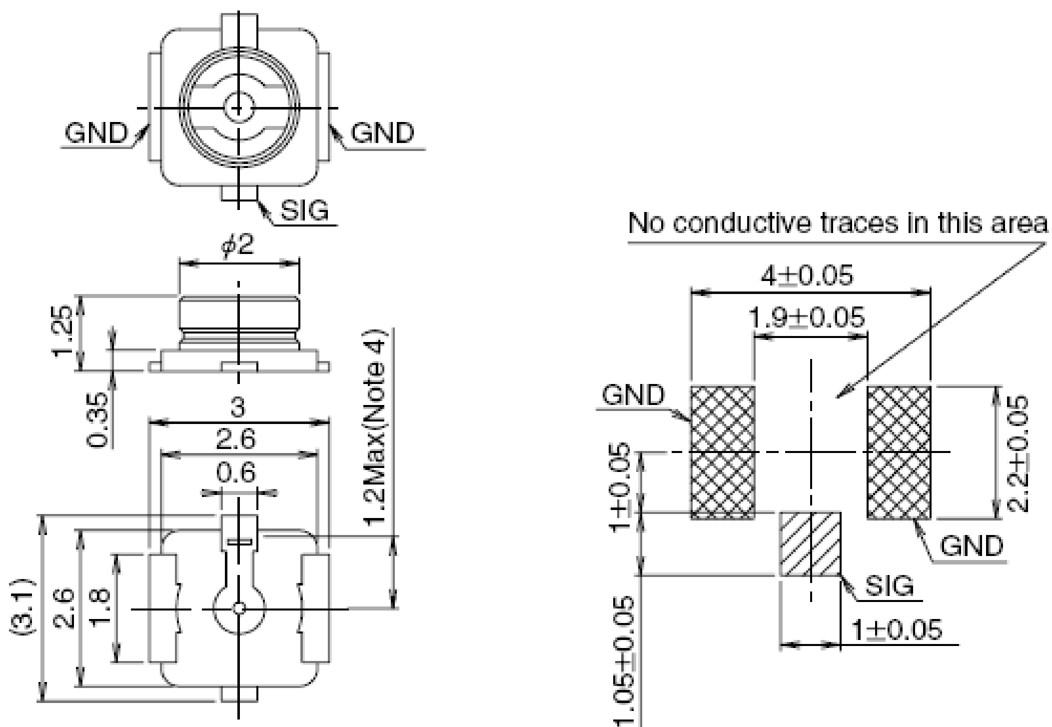


Figure 37: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of mated connector.

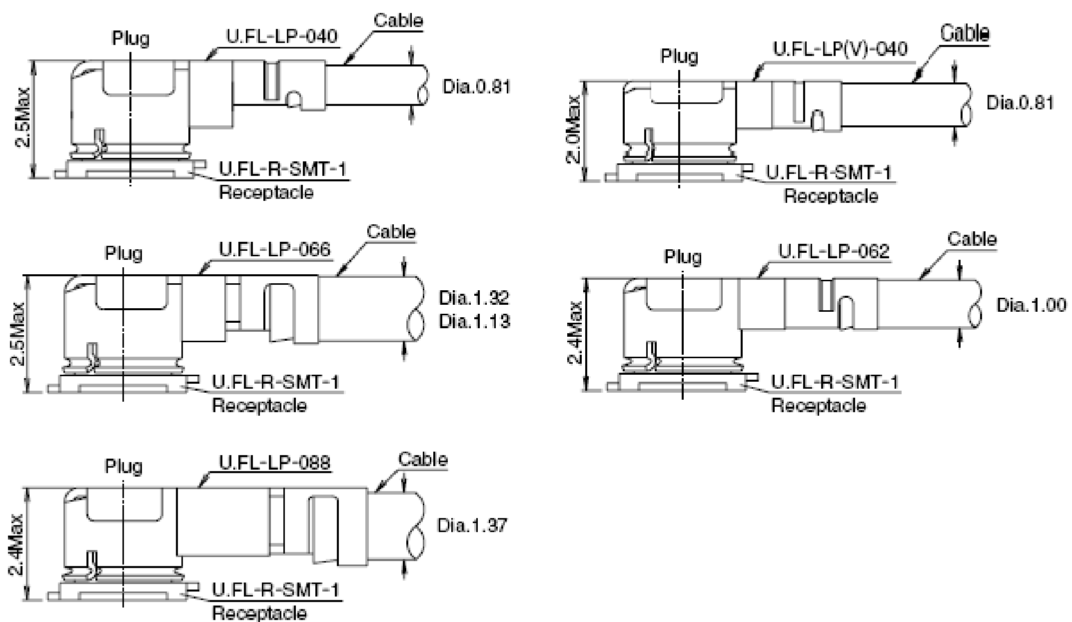


Figure 39: Space Factor of Mated Connectors (Unit: mm)

Please visit http://www.hirose.com for more information.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 58: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.5	4.8	V
USB_VBUS	-0.3	12.6	V
Peak current of VBAT	-	TBD	A
Voltage on digital pins	-0.3	2.1	V

6.2. Power Supply Ratings

Table 59: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT	The actual input voltages must stay between the minimum and maximum values.	3.55	4	4.4	V
USB_VBUS	USB/charger insertion detection; Charging power input;	-	3.7	5.0	12.6	V

	Power output for OTG device					
VRTC	Power supply for RTC	-	2.0	3.0	3.25	V

6.3. Power Consumption

Table 60: Power Consumption of SG560D-CE

Mode	Conditions	Typ.	Unit
OFF state	Power down	205	μA
Sleep state (USB disconnected)	WCDMA PF = 64	5.87	mA
	WCDMA PF = 128	5.41	mA
	WCDMA PF = 256	5.02	mA
	WCDMA PF = 512	4.75	mA
	LTE-FDD PF = 32	7.85	mA
	LTE-FDD PF = 64	6.38	mA
	LTE-FDD PF = 128	5.49	mA
	LTE-FDD PF = 256	5.09	mA
	LTE-TDD PF = 32	7.91	mA
	LTE-TDD PF = 64	6.39	mA
	LTE-TDD PF = 128	5.56	mA
	LTE-TDD PF = 256	5.16	mA
	5G NR FDD PF = 32	11.82	mA
	5G NR FDD PF = 64	9.66	mA
	5G NR FDD PF = 128	7.35	mA
	5G NR FDD PF = 256	6.55	mA

	5G NR TDD PF = 32	11.75	mA
	5G NR TDD PF = 64	9.23	mA
	5G NR TDD PF = 128	7.94	mA
	5G NR TDD PF = 256	7.3	mA
WCDMA voice calls	B1 @ max. power	617	mA
	B5 @ max. power	553	mA
	B8 @ max. power	612	mA
LTE data transmission	LTE-FDD B1 @ max. power	735	mA
	LTE-FDD B3 @ max. power	624	mA
	LTE-FDD B5 @ max. power	597	mA
	LTE-FDD B8 @ max. power	637	mA
	LTE-TDD B34 @ max. power	344	mA
	LTE-TDD B38 @ max. power	318	mA
	LTE-TDD B39 @ max. power	302	mA
	LTE-TDD B40 @ max. power	392	mA
	LTE-TDD B41 @ max. power	410	mA
WCDMA data transmission	B1 (HSDPA) @ max. power	587	mA
	B5 (HSDPA) @ max. power	513	mA
	B8 (HSDPA) @ max. power	565	mA
5G NR SA data transmission	n1 @ max. power 40 MHz, SCS 15 kHz	807	mA
	n3 @ max. power 20 MHz, SCS 15 kHz	613	mA
	n5 @ max. power 20 MHz, SCS 15 kHz	597	mA
	n8 @ max. power 20 MHz, SCS 15 kHz	687	mA
	n28 @ max. power 30 MHz, SCS 15 kHz	679	mA

	n41 @ max. power 100 MHz, SCS 30 kHz	446	mA
	n78 @ max. power 100 MHz, SCS 30 kHz	470	mA
	n79 @ max. power 100 MHz, SCS 30 kHz	506	mA
5G NR NSA data transmission	DC_3A_n41A 100 MHz, SCS 30 kHz	775	mA
	DC_39A_n41A 100 MHz, SCS 30 kHz	450	mA
	DC_1A_n78A 100 MHz, SCS 30 kHz	929	mA
	DC_3A_n78A 100 MHz, SCS 30 kHz	885	mA
	DC_5A_n78A 100 MHz, SCS 30 kHz	801	mA
	DC_8A_n78A 100 MHz, SCS 30 kHz	818	mA
	DC_3A_n79A 100 MHz, SCS 30 kHz	839	mA
	DC_39A_n79A 100 MHz, SCS 30 kHz	492	mA

Table 61: Power Consumption of SG560D-EM

Mode	Conditions	Typ.	Unit
OFF state	Power down	250	μA
GSM/GPRS supply current	Sleep state (USB disconnected) @ DRX = 2	6.86	mA
	Sleep state (USB disconnected) @ DRX = 5	6.02	mA
	Sleep state (USB disconnected) @ DRX = 9	5.84	mA
Sleep state (USB disconnected)	WCDMA PF = 64	6.70	mA
	WCDMA PF = 128	6.15	mA
	WCDMA PF = 256	5.88	mA
	WCDMA PF = 512	5.69	mA

	LTE-FDD PF = 32	8.02	mA
	LTE-FDD PF = 64	6.71	mA
	LTE-FDD PF = 128	5.80	mA
	LTE-FDD PF = 256	5.34	mA
	LTE-TDD PF = 32	8.22	mA
	LTE-TDD PF = 64	6.93	mA
	LTE-TDD PF = 128	6.04	mA
	LTE-TDD PF = 256	5.46	mA
	5G NR FDD PF = 32	10.95	mA
	5G NR FDD PF = 64	8.36	mA
	5G NR FDD PF = 128	7.26	mA
	5G NR FDD PF = 256	6.48	mA
	5G NR TDD PF = 32	11.16	mA
	5G NR TDD PF = 64	8.65	mA
	5G NR TDD PF = 128	7.55	mA
	5G NR TDD PF = 256	6.88	mA
GSM voice call	GSM850 @ PCL 5	390	mA
	GSM850 @ PCL 12	194	mA
	GSM850 @ PCL 19	131	mA
	GSM900 @ PCL 5	286	mA
	GSM900 @ PCL 12	193	mA
	GSM900 @ PCL 19	131	mA
	DCS1800 @ PCL 0	218	mA
	DCS1800 @ PCL 7	145	mA
	DCS1800 @ PCL 15	86	mA

	PCS1900 @ PCL 0	246	mA
	PCS1900 @ PCL 7	145	mA
	PCS1900 @ PCL 15	86	mA
WCDMA voice calls	B1 @ max. power	624	mA
	B2 @ max. power	614	mA
	B4 @ max. power	680	mA
	B5 @ max. power	630	mA
	B6 @ max. power	613	mA
	B8 @ max. power	600	mA
	B19 @ max. power	613	mA
LTE data transmission	LTE-FDD B1 @ max. power	740	mA
	LTE-FDD B2 @ max. power	663	mA
	LTE-FDD B3 @ max. power	722	mA
	LTE-FDD B4 @ max. power	723	mA
	LTE-FDD B5 @ max. power	595	mA
	LTE-FDD B7 @ max. power	818	mA
	LTE-FDD B8 @ max. power	574	mA
	LTE-FDD B12 @ max. power	618	mA
	LTE-FDD B17 @ max. power	652	mA
	LTE-FDD B18 @ max. power	593	mA
	LTE-FDD B19 @ max. power	574	mA
	LTE-FDD B20 @ max. power	645	mA
	LTE-FDD B26 @ max. power	611	mA
	LTE-FDD B28 @ max. power	551	mA
	LTE-TDD B34 @ max. power	290	mA

	LTE-TDD B38 @ max. power	375	mA
	LTE-TDD B39 @ max. power	290	mA
	LTE-TDD B40 @ max. power	437	mA
	LTE-TDD B41 @ max. power	460	mA
	LTE-TDD B42 @ max. power	440	mA
WCDMA data transmission	B1 (HSDPA) @ max. power	579	mA
	B2 (HSDPA) @ max. power	573	mA
	B4 (HSDPA) @ max. power	624	mA
	B5 (HSDPA) @ max. power	580	mA
	B6 (HSDPA) @ max. power	565	mA
	B8 (HSDPA) @ max. power	549	mA
	B19 (HSDPA) @ max. power	565	mA
GPRS data transmission	GSM850 (1UL/4DL) @ PCL 5	331	mA
	GSM850 (2UL/3DL) @ PCL 5	570	mA
	GSM850 (3UL/2DL) @ PCL 5	657	mA
	GSM850 (4UL/1DL) @ PCL 5	825	mA
	EGSM900 (1UL/4DL) @ PCL 5	286	mA
	EGSM900 (2UL/3DL) @ PCL 5	469	mA
	EGSM900 (3UL/2DL) @ PCL 5	618	mA
	EGSM900 (4UL/1DL) @ PCL 5	790	mA
	DCS1800 (1UL/4DL) @ PCL 0	216	mA
	DCS1800 (2UL/3DL) @ PCL 0	314	mA
	DCS1800 (3UL/2DL) @ PCL 0	419	mA
	DCS1800 (4UL/1DL) @ PCL 0	522	mA
	PCS1900 (1UL/4DL) @ PCL 0	247	mA

	PCS1900 (2UL/3DL) @ PCL 0	389	mA
	PCS1900 (3UL/2DL) @ PCL 0	468	mA
	PCS1900 (4UL/1DL) @ PCL 0	576	mA
EDGE data transmission	GSM850 (1UL/4DL) @ PCL 8	229	mA
	GSM850 (2UL/3DL) @ PCL 8	397	mA
	GSM850 (3UL/2DL) @ PCL 8	566	mA
	GSM850 (4UL/1DL) @ PCL 8	511	mA
	EGSM900 (1UL/4DL) @ PCL 8	227	mA
	EGSM900 (2UL/3DL) @ PCL 8	397	mA
	EGSM900 (3UL/2DL) @ PCL 8	556	mA
	EGSM900 (4UL/1DL) @ PCL 8	502	mA
	DCS1800 (1UL/4DL) @ PCL 2	185	mA
	DCS1800 (2UL/3DL) @ PCL 2	296	mA
	DCS1800 (3UL/2DL) @ PCL 2	388	mA
	DCS1800 (4UL/1DL) @ PCL 2	345	mA
	PCS1900 (1UL/4DL) @ PCL 2	200	mA
	PCS1900 (2UL/3DL) @ PCL 2	319	mA
	PCS1900 (3UL/2DL) @ PCL 2	407	mA
	PCS1900 (4UL/1DL) @ PCL 2	340	mA
5G NR SA data transmission	n1 @ 23 dBm 20 MHz, SCS 15 kHz	808	mA
	n3 @ 23 dBm 20 MHz, SCS 15 kHz	881	mA
	n5 @ 23 dBm 20 MHz, SCS 15 kHz	705	mA
	n7 @ 23 dBm 20 MHz, SCS 15 kHz	900	mA
	n8 @ 23 dBm 20 MHz, SCS 15 kHz	625	mA
	n20 @ 23 dBm 20 MHz, SCS 15 kHz	697	mA

	n28 @ 23 dBm 20 MHz, SCS 15 kHz	685	mA
	n38 @ 23 dBm 20 MHz, SCS 30 kHz	357	mA
	n40 @ 23 dBm 20 MHz, SCS 30 kHz	372	mA
	n41 @ 26 dBm 100 MHz, SCS 30 kHz	517	mA
	n77 @ 26 dBm 100 MHz, SCS 30 kHz	449	mA
	n78 @ 26 dBm 100 MHz, SCS 30 kHz	469	mA
	n79 @ 26 dBm 100 MHz, SCS 30 kHz	544	mA
5G NR NSA data transmission	DC_3A_n78A @ 23 dBm 100 MHz, SCS 30 kHz	909	mA
	DC_7A_n20A @ 23 dBm 100 MHz, SCS 30 kHz	1020	mA
	DC_5A_n79A @ 23 dBm 100 MHz, SCS 30 kHz	889	mA
5G NR UL MIMO data transmission	n38 @ 22.1dBm 40 MHz, SCS 30 kHz	386	mA
	n40 @ 22.1 dBm 80 MHz, SCS 30 kHz	433	mA
	n41 @ 25.6 dBm 100 MHz, SCS 30 kHz	607	mA
	n77 @ 25.5 dBm 100 MHz, SCS 30 kHz	613	mA
	n78 @ 25.1 dBm 100 MHz, SCS 30 kHz	526	mA
	n79 @ 25.6 dBm 100 MHz, SCS 30 kHz	672	mA

Table 62: Power Consumption of SG560D-NA

Mode	Conditions	Typ.	Unit
OFF state	Power down	224	μA
Sleep state (USB disconnected)	LTE-FDD PF = 32	8.68	mA
	LTE-FDD PF = 64	7.11	mA

	LTE-FDD PF = 128	6.11	mA
	LTE-FDD PF = 256	5.63	mA
	LTE-TDD PF = 32	8.76	mA
	LTE-TDD PF = 64	7.22	mA
	LTE-TDD PF = 128	6.32	mA
	LTE-TDD PF = 256	5.86	mA
	5G NR FDD PF = 32	12.01	mA
	5G NR FDD PF = 64	9.18	mA
	5G NR FDD PF = 128	7.76	mA
	5G NR FDD PF = 256	6.93	mA
	5G NR TDD PF = 32	11.58	mA
	5G NR TDD PF = 64	9.07	mA
	5G NR TDD PF = 128	7.84	mA
	5G NR TDD PF = 256	7.15	mA
LTE data transmission	LTE-FDD B2 @ max. power	692	mA
	LTE-FDD B4 @ max. power	685	mA
	LTE-FDD B5 @ max. power	528	mA
	LTE-FDD B7 @ max. power	834	mA
	LTE-FDD B12 @ max. power	648	mA
	LTE-FDD B13 @ max. power	666	mA
	LTE-FDD B14 @ max. power	564	mA
	LTE-FDD B17 @ max. power	584	mA
	LTE-FDD B25 @ max. power	661	mA
	LTE-FDD B26 @ max. power	531	mA
	LTE-FDD B30 @ max. power	874	mA

	LTE-FDD B66 @ max. power	738	mA
	LTE-FDD B71 @ max. power	707	mA
	LTE-TDD B38 @ max. power	474	mA
	LTE-TDD B41 @ max. power	525	mA
	LTE-TDD B42 @ max. power	358	mA
	LTE-TDD B43 @ max. power	402	mA
	LTE-TDD B48 @ max. power	410	mA
5G NR SA data transmission	n2 @ max. power 20 MHz, SCS 15 kHz	721	mA
	n5 @ max. power 20 MHz, SCS 15 kHz	518	mA
	n7 @ max. power 20 MHz, SCS 15 kHz	828	mA
	n12 @ max. power 15 MHz, SCS 15 kHz	591	mA
	n13 @ max. power 10 MHz, SCS 15 kHz	544	mA
	n14 @ max. power 10 MHz, SCS 15 kHz	611	mA
	n25 @ max. power 20 MHz, SCS 15 kHz	685	mA
	n26 @ max. power 20 MHz, SCS 15 kHz	512	mA
	n30 @ max. power 10 MHz, SCS 15 kHz	868	mA
	n66 @ max. power 20 MHz, SCS 15 kHz	778	mA
	n70 @ max. power 15 MHz, SCS 15 kHz	686	mA
	n71 @ max. power 20 MHz, SCS 15 kHz	616	mA
	n38 @ max. power 40 MHz, SCS 30 kHz	310	mA
	n41 @ 26 dBm 100 MHz, SCS 30 kHz	484	mA
	n48 @ max. power 40 MHz, SCS 30 kHz	306	mA

	n77 @ 26 dBm 100 MHz, SCS 30 kHz	423	mA
	n78 @ 26 dBm 100 MHz, SCS 30 kHz	402	mA
5G NR NSA data transmission	DC_2A_n66A 20 MHz, SCS 15 kHz	826	mA
	DC_2A_n77A 100 MHz, SCS 30 kHz	960	mA
	DC_4A_n78A 20 MHz, SCS 30 kHz	607	mA
	DC_5A_n7A 20 MHz, SCS 15 kHz	810	mA
	DC_5A_n25A 10 MHz, SCS 15 kHz	930	mA
	DC_5A_n48A 40 MHz, SCS 30 kHz	820	mA
	DC_7A_n71A 100 MHz, SCS 15 kHz	584	mA
	DC_12A_n2A 20 MHz, SCS 15 kHz	758	mA
	DC_12A_n30A 20 MHz, SCS 15 kHz	938	mA
	DC_12A_n38A 20 MHz, SCS 30 kHz	849	mA
	DC_12A_n41A 20 MHz, SCS 30 kHz	870	mA
	DC_48A_n12A 10 MHz, SCS 15 kHz	874	mA
	DC_66A_n5A 20 MHz, SCS 15 kHz	556	mA
	DC_66A_n14A 10 MHz, SCS 15 kHz	905	mA
5G NR UL MIMO data transmission	n38 @ max. power 40 MHz, SCS 30 kHz	444	mA
	n41 @ max. power 100 MHz, SCS 30 kHz	596	mA
	n77 @ max. power 100 MHz, SCS 30 kHz	471	mA
	n78 @ max. power 100 MHz, SCS 30 kHz	475	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact Quectel Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristic

Table 63: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.17	2.1	V
V_{IL}	Low-level input voltage	-0.3	0.63	V
V_{OH}	High-level output voltage	1.35	1.8	V
V_{OL}	Low-level output voltage	0	0.45	V

Table 64: (U)SIM Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.65	1.95	V
V_{IH}	High-level input voltage	1.16	2.25	V
V_{IL}	Low-level input voltage	-0.3	0.39	V
V_{OH}	High-level output voltage	1.32	1.95	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 65: (U)SIM High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	High-level input voltage	1.89	3.35	V
V_{IL}	Low-level input voltage	-0.3	0.61	V
V_{OH}	High-level output voltage	2.16	3.05	V
V_{OL}	Low-level output voltage	0	0.4	V

Table 66: SD Card Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
SD_LDO6C	Power supply	1.65	1.9	V
V_{IH}	High-level input voltage	1.27	2	V
V_{IL}	Low-level input voltage	-0.3	0.58	V
V_{OH}	High-level output voltage	1.4	-	V
V_{OL}	Low-level output voltage	-	0.45	V

Table 67: SD Card High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
SD_LDO6C	Power supply	2.72	3.54	V
V_{IH}	High-level input voltage	1.7	3.84	V
V_{IL}	Low-level input voltage	-0.3	0.89	V
V_{OH}	High-level output voltage	2.04	3.54	V
V_{OL}	Low-level output voltage	0	0.44	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 68: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interface	±5	±10	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 69: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [14]	-35	+25	+75	°C
Storage Temperature Range	-40	-	+90	°C

[14] Within operating temperature range, the module is 3GPP compliant.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

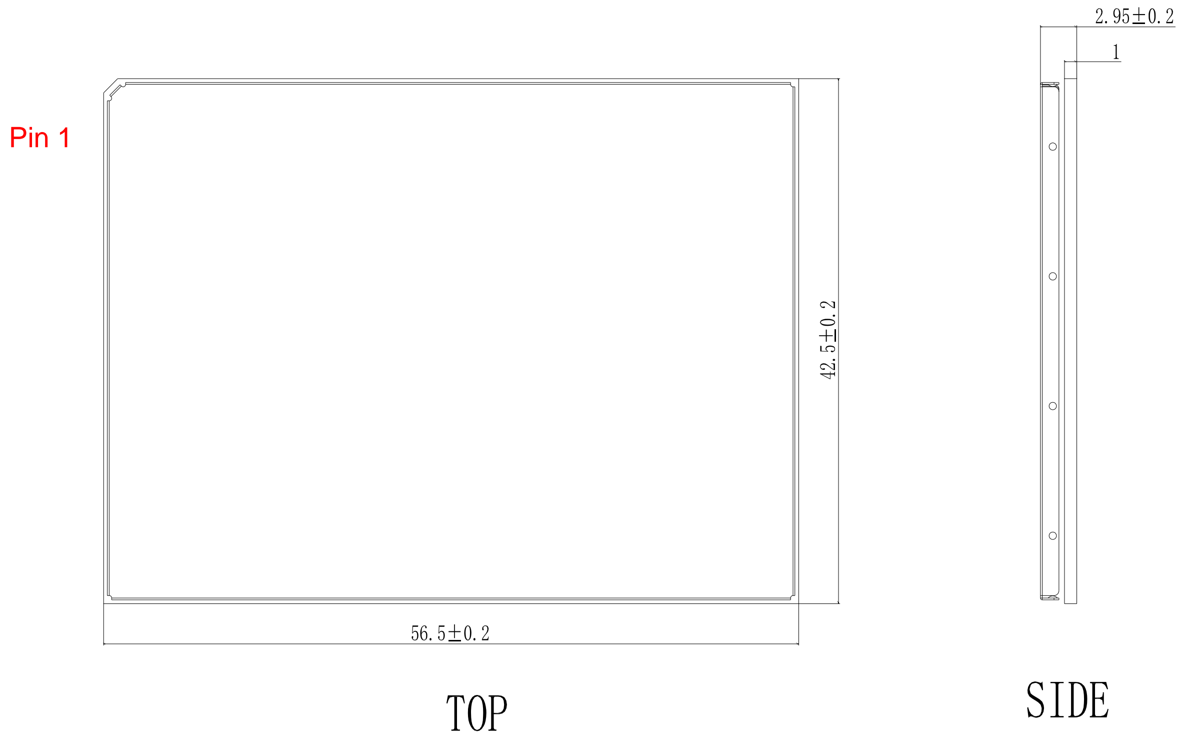


Figure 40: Module Top and Side Dimensions

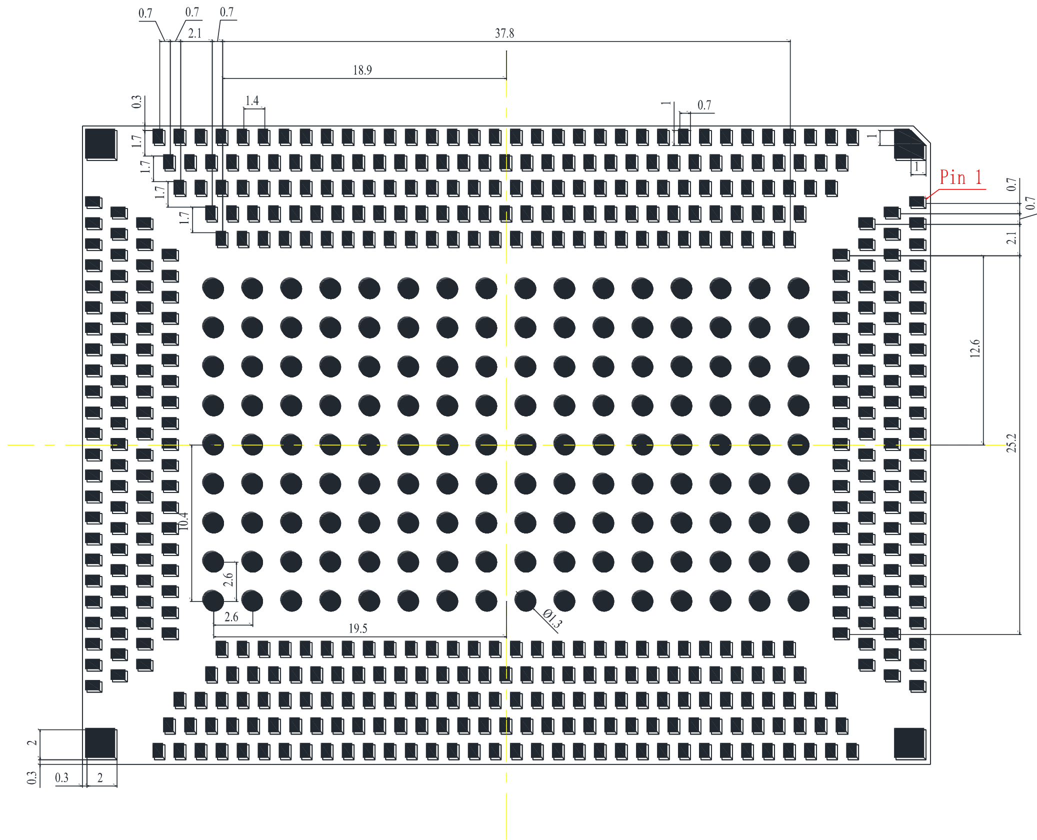


Figure 41: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

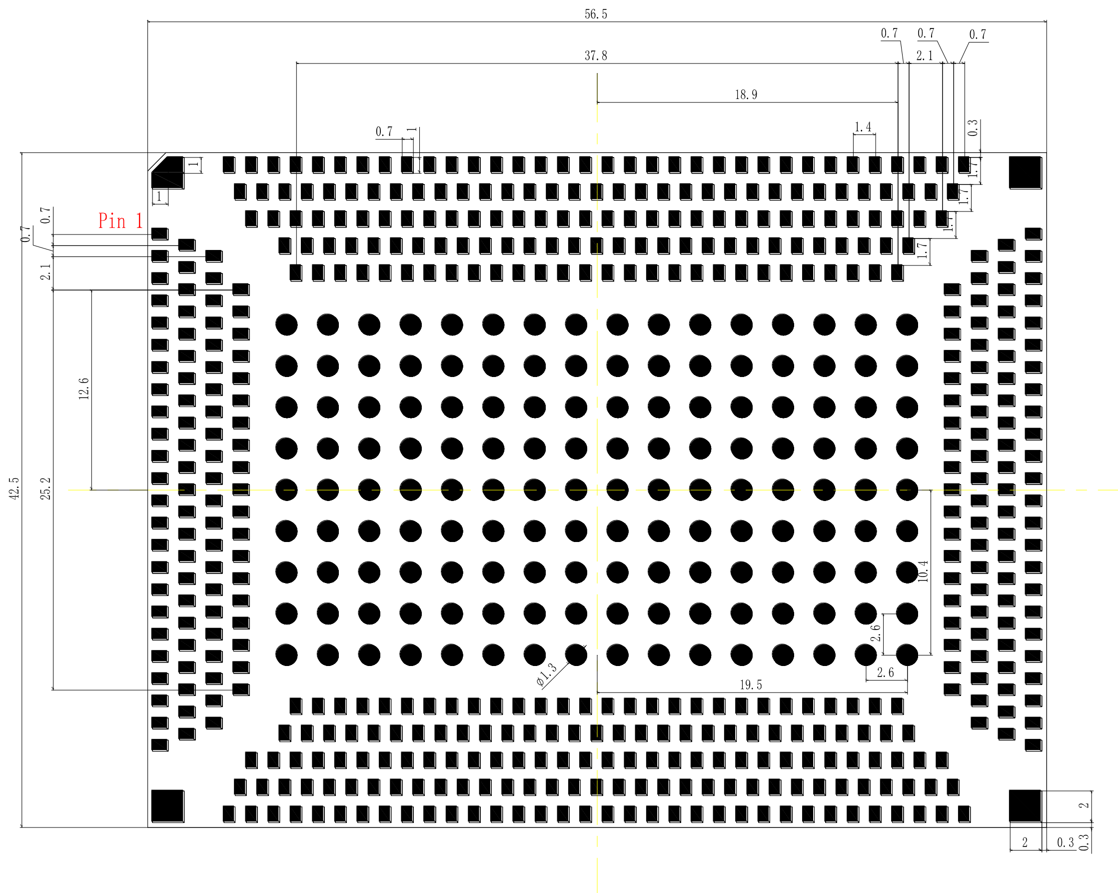


Figure 42: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

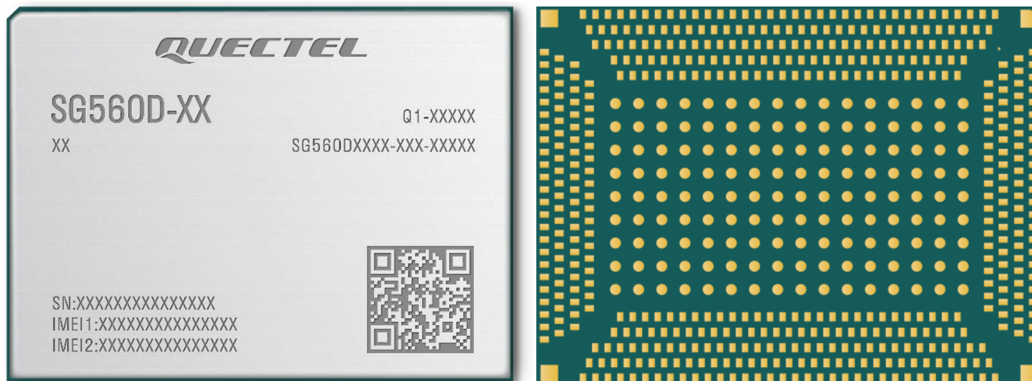


Figure 43: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [15] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[15] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [3]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

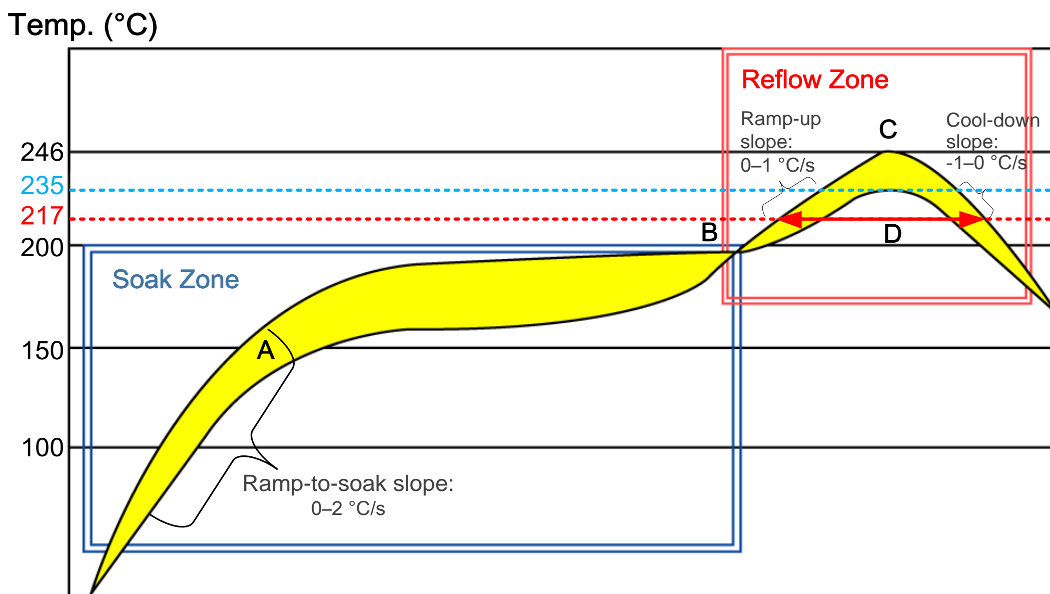


Figure 44: Recommended Reflow Soldering Thermal Profile

Table 70: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–2 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C ramp-up slope	0–1 °C/s
Reflow time (D: over 217°C)	40–65 s
Max temperature	235–246 °C
235–217 °C cool-down slope	-1–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, to avoid excessive temperature change, which may cause excessive thermal deformation of the metal shielding frame and cover, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste. If possible, please choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery.

The modules are packed in an injection tray packaging as specified in the sub-chapters below.

8.3.1. Injection Tray

Injection tray dimensions are illustrated in the following figure:

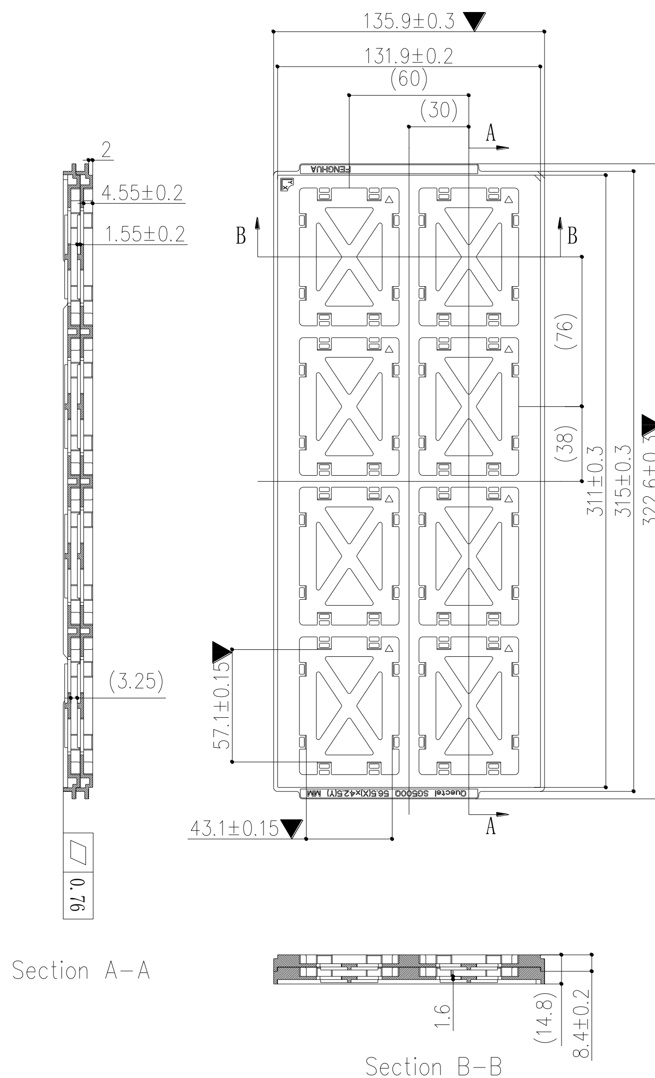
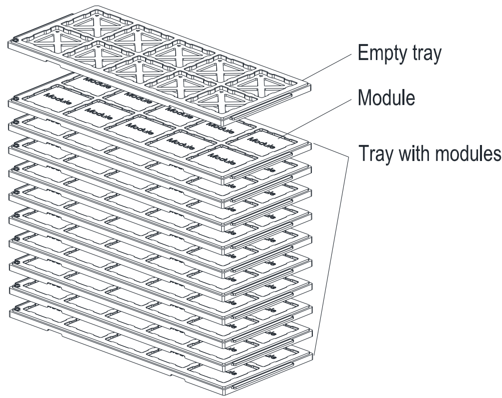


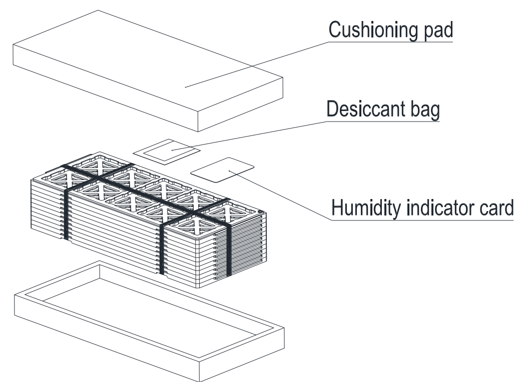
Figure 45: Injection Tray Dimension Drawing (Unit: mm)

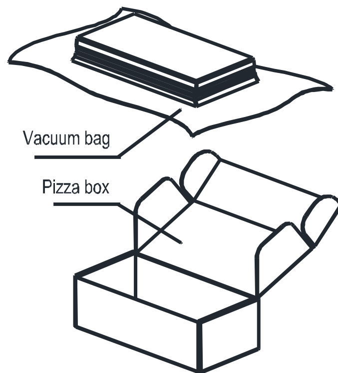
8.3.2. Packaging Process



Each injection tray packs 8 modules. Stack 10 trays with modules, and place 1 empty tray on top.

Fasten the 11 trays. Add the humidity indicator card and desiccant bag on top, and place 2 cushioning pads on the top and bottom of the trays.





Place the injection trays with cushioning pads into a vacuum bag, and vacuumize it. Then, place the vacuum-packed trays into a pizza box. 1 pizza box can pack 80 modules.

Place 2 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 160 modules.

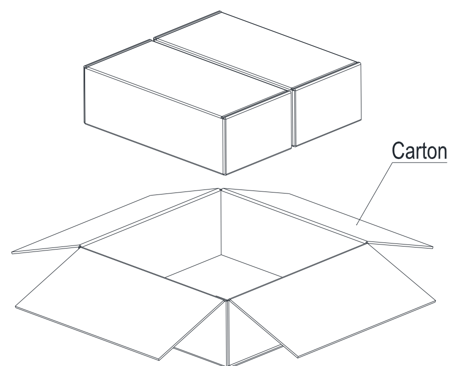


Figure 46: Packaging Process

9 Appendix References

Table 71: Related Documents

Document Name
[1] Quectel_Smart_5G_EVB_User_Guide
[2] Quectel_RF_Layout_Application_Note
[3] Quectel_Module_Stencil_Design_Requirements
[4] Quectel_Module_SMT_Application_Note

Table 72: Terms and Abbreviations

Abbreviation	Description
AMR	Adaptive Multi-Rate
BDS	BeiDou Navigation Satellite System
BLE	Bluetooth Low Energy
bps	Bytes per second
BPSK	Binary Phase Shift Keying
BR	Basic Rate
CDMA	Code Division Multiple Access
CEP	Circular Error Probable
Cj	Junction Capacitance
CPE	Customer-Premise Equipment
CPU	Central Processing Unit
CS	Coding Scheme

CSI	Camera Serial Interface
CTS	Clear To Send
DBS	Dual Band Simultaneous
DCS	Data Coding Scheme
DMIC	Digital Microphone
DRX	Discontinuous Reception
DSI	Display Serial Interface
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EPE	Expandable Polyethylene
EGSM	Enhanced GSM
eSCO	Extended Synchronous Connection Oriented
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
EVB	Evaluation Board
EVDO	Evolution-Data Optimized
FDD	Frequency Division Duplexing
FHD	Full High Definition
FR	Full Rate
Galileo	Galileo Satellite Navigation System (EU)
GLONASS	Global Navigation Satellite System (Russia)
GND	Ground
GNSS	Global Navigation Satellite System
GPIO	General-Purpose Input/Output

GPRS	General Packet Radio Service
GPS	Global Positioning System
GPU	Graphics Processing Unit
GSM	Global System for Mobile Communications
HPUE	High Power User Equipment
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HTTP	Hypertext Transfer Protocol
I2S	Inter-IC Sound
IEEE	Institute of Electrical and Electronics Engineers
IMT	International Mobile Telecommunications
LCD	Liquid Crystal Display
LCM	Liquid Crystal Monitor
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
MCS	Modulation and Coding Scheme
ME	Mobile Equipment
MIMO	Multi-Input Multi-Output / Multiple Input Multiple Output
MLCC	Multi-layer Ceramic Capacitor
MO	Mobile Origination
MT	Mobile Terminating
NFC	Near Field Communication
NSA	Non-Standalone

NTC	Negative Temperature Coefficient
OTA	Over-the-air programming
OTG	On-The-Go
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PF	Paging Frame
PMU	Power Management Unit
PND	Portable Navigation Devices
POS	Point of Sale
PSK	Phase Shift Keying
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RoHS	Restriction of Hazardous Substances
RTC	Right Hand Circular Polarization
RTS	Request To Send
SA	Standalone
SCO	Synchronous Connection Oriented
SCS	Sub-Carrier Space
SDIO	Secure Digital Input and Output Card
SIM	Subscriber Identity Module
SMS	Short Message Service

SPI	Serial Peripheral Interface
STA	Station
TBD	To Be Determined
TDD	Time Division Duplexing
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TP	Touch Panel
TTFF	Time to First Fix
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UFS	Universal Flash Storage
UMTS	Universal Mobile Telecommunications System
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}	High-level Input Voltage
V_{IL}	Low-level Input Voltage
V_{OH}	High-level Output Voltage
V_{OL}	Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WCN	Wireless Communication Network
WLAN	Wireless Local Area Network

IC

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).

The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change

the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC/IC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2023SG560DWF”
“Contains IC: 10224A-23SG560DWF “
The FCC ID/IC ID can be used only when all FCC/IC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	2.4GHz band Peak Gain (dBi)	5.2GHz band Peak Gain (dBi)	5.3GHz band Peak Gain (dBi)	5.5GHz band Peak Gain (dBi)	5.8GHz band Peak Gain (dBi)	6.5GHz band Peak Gain (dBi)	6.6GHz band Peak Gain (dBi)	6.7GHz band Peak Gain (dBi)	6.8GHz band Peak Gain (dBi)
Dipole	0.2	-0.7	-0.8	-1.2	-1.5	-0.9	-0.9	0.4	1.6

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is

connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 15.247 and 15.407 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions:

(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

FCC regulations restrict the operation of this device to indoor use only.
The operation of this device is prohibited on oil platforms, cars, trains, boats, and aircraft, except that operation of this device is permitted in large aircraft while flying above 10,000 feet in the 5.925-6.425 GHz band.
Operation of transmitters in the 5.925-7.125 GHz band is prohibited for control of or communications with unmanned aircraft systems

IC

Industry Canada Statement

This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions:
(1) This device may not cause interference; and
(2) This device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:
(1) l'appareil ne doit pas produire de brouillage, et
(2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Radiation Exposure Statement

This equipment complies with IC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Déclaration d'exposition aux radiations:

Cet équipement est conforme aux limites d'exposition aux rayonnements ISED établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20 cm de distance entre la source de rayonnement et votre corps.

RSS-247 Section 6.4 (5) (6) (for local area network devices, 5GHz)

The device could automatically discontinue transmission in case of absence of information to transmit, or operational failure. Note that this is not intended to prohibit transmission of control or signaling information or the use of repetitive codes where required by the technology.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;
The maximum antenna gain permitted for devices in the bands 5250–5350 MHz and 5470–5725 MHz shall comply with the e.i.r.p. limit; and
The maximum antenna gain permitted for devices in the band 5725–5825 MHz shall comply with the e.i.r.p. limits specified for point-to-point and non point-to-point operation as appropriate.

L'appareil peut interrompre automatiquement la transmission en cas d'absence d'informations à transmettre ou de panne opérationnelle. Notez que ceci n'est pas destiné à interdire la transmission

d'informations de contrôle ou de signalisation ou l'utilisation de codes répétitifs lorsque cela est requis par la technologie.

Le dispositif utilisé dans la bande 5150-5250 MHz est réservé à une utilisation en intérieur afin de réduire le risque de brouillage préjudiciable aux systèmes mobiles par satellite dans le même canal;
Le gain d'antenne maximal autorisé pour les dispositifs dans les bandes 5250-5350 MHz et 5470-5725 MHz doit être conforme à la norme e.r.p. limite; et
Le gain d'antenne maximal autorisé pour les appareils de la bande 5725-5825 MHz doit être conforme à la norme e.i.r.p. les limites spécifiées pour un fonctionnement point à point et non point à point, selon le cas.

This device is intended only for OEM integrators under the following conditions:

(For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Cet appareil est conçu uniquement pour les intégrateurs OEM dans les conditions

suivantes: (Pour utilisation de dispositif module)

1) L'antenne doit être installée de telle sorte qu'une distance de 20 cm est respectée entre l'antenne et les utilisateurs, et
2) Le module émetteur peut ne pas être coïmplanté avec un autre émetteur ou antenne.

Tant que les 2 conditions ci-dessus sont remplies, des essais supplémentaires sur l'émetteur ne seront pas nécessaires. Toutefois, l'intégrateur OEM est toujours responsable des essais sur son produit final pour toutes exigences de conformité supplémentaires requis pour ce module installé.

IMPORTANT NOTE:

In the event that these conditions can not be met (for example certain laptop configurations or colocation with another transmitter), then the Canada authorization is no longer considered valid and the IC ID can not be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate Canada authorization.

NOTE IMPORTANTE:

Dans le cas où ces conditions ne peuvent être satisfaites (par exemple pour certaines configurations d'ordinateur portable ou de certaines co-localisation avec un autre émetteur), l'autorisation du Canada n'est plus considéré comme valide et l'ID IC ne peut pas être utilisé sur le produit final. Dans ces circonstances, l'intégrateur OEM sera chargé de réévaluer le produit final (y compris l'émetteur) et l'obtention d'une autorisation distincte au Canada.

End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: “Contains IC: 10224A-23SG560DWF”.

Plaque signalétique du produit final

Ce module émetteur est autorisé uniquement pour une utilisation dans un dispositif où l'antenne peut être installée de telle sorte qu'une distance de 20cm peut être maintenue entre l'antenne et les utilisateurs. Le produit final doit être étiqueté dans un endroit visible avec l'inscription suivante: "Contient des IC: 10224A-23SG560DWF ".

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module.
The end user manual shall include all required regulatory information/warning as show in this manual.

Manuel d'information à l'utilisateur final

L'intégrateur OEM doit être conscient de ne pas fournir des informations à l'utilisateur final quant à la façon d'installer ou de supprimer ce module RF dans le manuel de l'utilisateur du produit final qui intègre ce module.
Le manuel de l'utilisateur final doit inclure toutes les informations réglementaires requises et avertissements comme indiqué dans ce manuel.

Operation shall be limited to indoor use only.
Devices shall not be used for control of or communications with unmanned aircraft systems.
Operation on oil platforms, automobiles, trains, maritime vessels and aircraft shall be prohibited except for on large aircraft flying above 3,048 m (10,000 ft).

L’opération doit être limitée à l’usage d’intérieur seulement.
Les dispositifs ne doivent pas être utilisés pour le contrôle ou les communications avec les systèmes

d’aéronef sans pilote.
L’exploitation sur des plates-formes pétrolières, des automobiles, des trains, des navires maritimes et des aéronefs doit être interdite, sauf à bord de gros aéronefs volant au-dessus de 3 048 m (10 000 pi).