QUECTEL

SG368Z Series

Hardware Design

Smart Module Series

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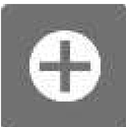
The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

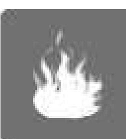
Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.



Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.



In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

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1 Introduction

This document describes the SG368Z series module's features, performance, and air interfaces and hardware interfaces connected to your applications. The document provides a quick insight into interface specifications, RF performance, electrical and mechanical specifications, and other module information, as well.

NOTE

For conciseness purposes, SG368Z-WF and SG368Z-AP will hereinafter be referred to collectively as "the module" in parts hereof applicable to both models, and individually as "SG368Z-WF" and "SG368Z-AP" in parts hereof referring to the differences between them.

1.1. Special Marks

Table 1: Special Marks

Marks	Definitions
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA[0:3] refers to all four SDIO_DATA pins, SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3.

2 Product Overview

SG368Z series is Quectel's new generation of Linux/Android smart module. It is an SMD module with compact packaging and it supports built-in high performance ARM Mali G52 GPU, multiple audio and video codecs, and multiple audio and video input/output interfaces as well as abundant GPIO interfaces. With these, the module is engineered to meet most of the demands of M2M applications, for instance:

- IoT gateways
- smart commercial displays
- AI industrial automation
- security surveillance
- NAS
- NVR/DVR

Table 2: Basic Information

SG368Z Series	
Packaging type	LGA
Pin counts	453
Dimensions	46.0 × 42.0 × 3.15 mm
Weight	SG368Z-WF: approx. 13.1 g SG368Z-AP: approx. 12.8 g
Models	SG368Z-WF, SG368Z-AP

2.1. Frequency Bands and Functions

Table 3: Frequency Bands and Functions

Wireless Network Type	SG368Z-WF	SG368Z-AP
Wi-Fi 802.11a/b/g/n/ac	2402–2482 MHz	-

	5180–5825 MHz	
Bluetooth 4.2	2402–2480 MHz	-

2.2. Key Features

Table 4: Key Features

Categories	Descriptions
Application Processor	● Quad-core 64-bit ARM Cortex-A55 CPU ● Up to 2 GHz ● 32 KB L1 I-cache, 32 KB L1 D-cache, 512 KB L3 cache
GPU	ARM Mali G52 GPU
Memory	**Industrial grade:** ● 8 GB eMMC + 1 GB LPDDR4X (default) ● 16 GB eMMC + 2 GB LPDDR4X (optional) **Commercial grade:** ● 32 GB eMMC + 2 GB LPDDR4X (default) ● 32 GB eMMC + 4 GB LPDDR4X (optional)
Operating System	Android 11*/12*/13, Linux (Kernel 4.19/5.10*)
Supply Voltage	● 3.3–3.5 V ● Typ.: 3.4 V
USB Interfaces	● 1 × USB 3.0 and 2.0 OTG interface (USB0): – Supports Host and Device modes – Supports AT command communication, data transmission, software debugging, firmware upgrade (only supports firmware upgrade through USB 2.0) – SS channel can be multiplexed into SATA0* interface ● 1 × USB 3.0 and 2.0 Host interface (USB1): – Only supports Host mode – SS channel can be multiplexed into SATA1 or QSGMII/SGMII* interface ● 2 × USB 2.0 Host interfaces (USB2 and USB3): – Only support Host mode
SD Card Interface	● Complies with SD 3.0 protocol ● 1.8/3.3 V SD card ● SD card hot-plug

UART	● Up to 8 groups of UART for SG368Z-WF; Up to 10 groups of UART for SG368Z-AP ● Speed rate up to 4 Mbps
I2C Interfaces	● Up to 5 groups of I2C interfaces ● Only support master mode
I2S Interfaces	● Up to 2 groups of I2S interfaces for SG368Z-AP ● Up to 1 group of I2S interface for SG368Z-WF
Analog Audio Interfaces	**Audio input:** ● 1 analog microphone input **Audio outputs:** ● Class AB stereo headphone output ● Class D loudspeaker differential amplifier output
PDM Interface	● 1 group of PDM interface ● Supports up to 6-lane PDM audio input
Audio Codec	MP3, AAC, AAC+ and PCM
ADC Interfaces	● 5 generic ADC interfaces ● Resolution: up to 10-bit
eDP Interface	● 1 group of 4-lane eDP interface ● Data rate: up to 2.7 Gbps/lane ● Supports 1-lane or 2-lane or 4-lane mode ● Supports AUX channel ● Supports up to 2560 × 1600 @ 60 fps
HDMI Interface	● HDMI 2.0 ● Supports hot-plug ● Supports up to 4096 × 2160 @ 60 fps
LCM Interfaces	● 2 groups of MIPI DSI: 4-lane MIPI DSI0 and 4-lane MIPI DSI1 ● Data rate: up to 2.5 Gbps/lane ● 1 group of MIPI DSI (4-lane) supports up to 1920 × 1080 @ 60 fps ● 2 groups of MIPI DSI (8-lane) supports up to 2048 × 1536 @ 60 fps ● MIPI DSI0 can be multiplexed into LVDS, supports up to 1280 × 800 @ 60 fps
Video Codec	● Encoding: 1080p @ 60 fps ● Decoding: 4K @ 60 fps
Camera Interface	● Supports 1 group of 4-lane MIPI CSI or 2 groups of 2-lane MIPI CSI ● Data rate: up to 2.5 Gbps/lane ● Up to 8 MP
Touch Panel Interface	Supports I2C TP interface
PCIe Interfaces	● 1 group of 1-lane PCIe 2.0 interface, only supports RC mode, can be multiplexed into SATA2 or QSGMII/SGMII* interface ● 1 group of 2-lane PCIe 3.0 interface
RGMII Interfaces	● Up to 1 group of RGMII interface for SG368Z-WF ● Up to 2 groups of RGMII interfaces for SG368Z-AP

Antenna Interface	● Wi-Fi & Bluetooth antenna interface (ANT_RF) ● 50 Ω characteristic impedance
WLAN Features	● Operating modes: AP and STA ● Operating frequency: 2.4 GHz, 5 GHz ● Protocol features: IEEE 802.11a/b/g/n/ac ● Data rate: up to 433.3 Mbps
Bluetooth Features	● *Bluetooth Core Specification Version 4.2* ● Bluetooth Classic & Bluetooth Low Energy (BLE)
Real Time Clock	The module supports RTC function
Temperature Ranges	● Normal operating temperature [1]: - Commercial grade: -10 °C to +75 °C - Industrial grade: -40 °C to +85 °C ● Storage temperature: -40 to +90 °C
Firmware Upgrade	● USB 2.0 interface ● OTA
RoHS	All hardware components are fully Complies with EU RoHS directive

2.3. Functional Diagram

The main components of the block diagram are explained below:

- Power management
- Baseband part
- eMMC + LPDDR4X flash
- Radio frequency part
- Peripheral interfaces

[1] Within the operating temperature range, the module meets IEEE specifications.

NOTE

1. SG368Z-AP does not support WLAN and Bluetooth function.
2. SG368Z-WF only supports 1 group of RGMII interface.

2.4. Pins Assignment

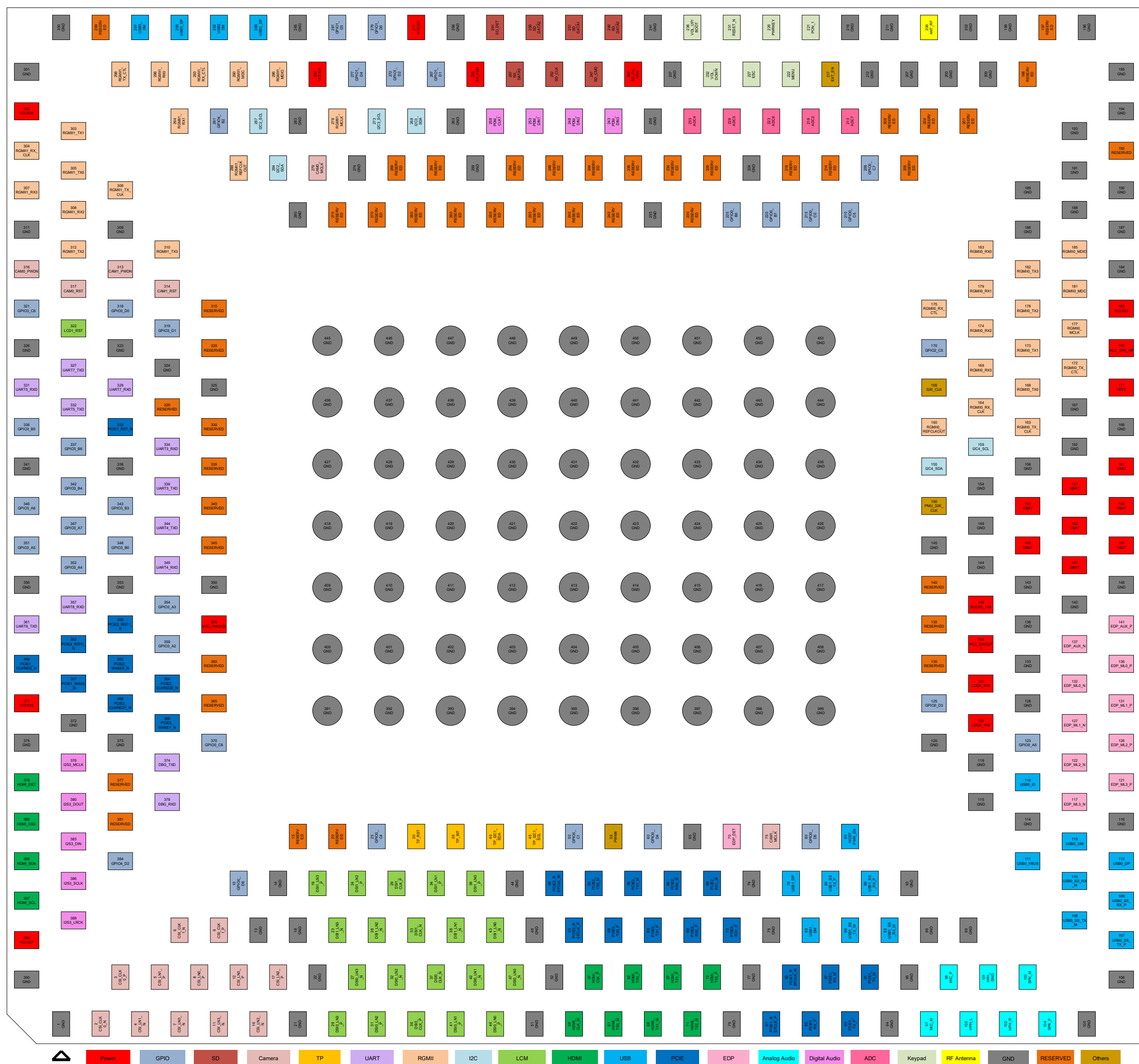


Figure 1: Pins Assignment (Top View)

NOTE

1. Keep all RESERVED pins and unused pins unconnected unless otherwise specified.
2. All GND pins should be connected to ground.

2.5. Pins Description

Table 5: Parameters Definition

Parameters	Descriptions
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current in the table below.

Table 6: Pins Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	147, 148, 151, 152, 153, 156, 157, 161	PI	Power supply for the module	Vmax = 3.5 V Vmin = 3.3 V Vnom = 3.4 V	
VCCIO1	282	PO	1.8 V output power, reference voltage for VCCIO1 power domain	Vnom = 1.8 V	
VCCIO2	271	PO	1.8 V output power, reference voltage for VCCIO2 power domain	Vnom = 1.8 V	

VCCIO4	180	PO	1.8 V output power, reference voltage for VCCIO4 power domain	Vnom = 1.8 V	
VCCIO5	371	PO	1.8 V output power, reference voltage for VCCIO5 power domain	Vnom = 1.8 V	
VCCIO6	302	PO	1.8 V output power, reference voltage for VCCIO6 power domain	Vnom = 1.8 V	
VCCIO7	389	PO	1.8 V output power, reference voltage for VCCIO7 power domain	Vnom = 1.8 V	
VCC_PMUIO2	355	PO	1.8 V output power, reference voltage for PMUIO2 and PMUIO0 power domain	Vnom = 1.8 V	
LDO6_3V3	129	PO	3.3 V output power, reference voltage for PMUIO1 power domain	Vnom = 3.3 V	
LDO9_1V8	124	PO	1.8 V output power for MIPI LCM VIO	Vnom = 1.8 V	
BUCK5_1V8	139	PO	1.8 V output power	Vnom = 1.8 V	
VCC_SWOUT1	134	PO	VBAT output power 1	Vnom = VBAT	
VRTC*	171	PI	Power supply for RTC		Keep this pin unconnected.
GND	1, 13, 14, 18, 21, 22, 44, 48, 51, 52, 65, 74, 76–78, 93–96, 99, 105, 106, 114–116, 119, 120, 128, 133, 138, 142–146, 149, 154, 158, 162, 166, 167, 184, 186–191, 193–196, 199, 200, 202, 203, 207, 211, 212, 216, 224, 235, 237, 238, 241, 259, 263, 266, 274, 280, 283, 285, 300, 301, 309, 311, 323, 324, 325, 326, 338, 341, 350, 353, 356, 372, 373, 375, 390–453				
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
HPH_L	100	AO	Headphone left channel output		

HPH_R	102	AO	Headphone right channel output		
HPH_GND	101	AI	Headphone reference ground		If unused, connect this pin to ground.
SPK_P	104	AO	Loudspeaker output (+)		
SPK_M	103	AO	Loudspeaker output (-)		
MIC_P	98	AI	Microphone input (+)		
MIC_M	97	AI	Microphone input (-)		
VCC_SPK_HP	176	PI	Analog audio power supply	Vmax = 5.5 V Vmin = 2.7 V Vnom = 5 V	If the analog audio function is not used, this pin needs to be connected to VBAT.
USB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
HOST_PWR_EN	85	DO	Host USB VBUS power enable	PMUIO1	
USB0_VBUS	111	DI	USB0 insertion detection	V_{IH}max = 2.7 V V_{IH}min = 3.3 V	Can not supply power for peripherals. A test point must be reserved.
USB0_ID	118	DI	USB0 ID detect	V_{IL}max = 0.3 V	Internally pull up to 1.8 V.
USB0_DP	112	AIO	USB0 2.0 differential data (+)		A test point must be reserved.
USB0_DM	113	AIO	USB0 2.0 differential data (-)		A test point must be reserved.
USB0_SS_TX_P	107	AO	USB0 3.0 transmit (+)		
USB0_SS_TX_M	108	AO	USB0 3.0 transmit (-)		
USB0_SS_RX_P	109	AI	USB0 3.0 receive (+)		
USB0_SS_RX_M	110	AI	USB0 3.0 receive (-)		
USB1_DP	79	AIO	USB1 2.0 differential data (+)		

USB1_DM	83	AIO	USB1 2.0 differential data (-)		
USB1_SS_TX_P	84	AO	USB1 3.0 transmit (+)		
USB1_SS_TX_M	88	AO	USB1 3.0 transmit (-)		
USB1_SS_RX_P	89	AI	USB1 3.0 receive (+)		
USB1_SS_RX_M	92	AI	USB1 3.0 receive (-)		
USB2_DP	289	AIO	USB2 2.0 differential data (+)		
USB2_DM	292	AIO	USB2 2.0 differential data (-)		
USB3_DP	295	AIO	USB3 2.0 differential data (+)		
USB3_DM	297	AIO	USB3 2.0 differential data (-)		
PCIe Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE1_TX_P	90	AO	PCIe1 transmit (+)		
PCIE1_TX_M	91	AO	PCIe1 transmit (-)		
PCIE1_RX_P	86	AI	PCIe1 receive (+)		
PCIE1_RX_M	87	AI	PCIe1 receive (-)		
PCIE1_REFCLK_P	81	AO	PCIe1 reference clock (+)		
PCIE1_REFCLK_M	82	AO	PCIe1 reference clock (-)		
PCIE1_CLKREQ_N	366	DI	PCIe1 clock request	VCCIO5	
PCIE1_WAKE_N	367	DI	PCIe1 wake up	VCCIO5	
PCIE1_RST_N	333	DO	PCIe1 reset	VCCIO5	
PCIE2_TX0_P	58	AO	PCIe2 transmit 0 (+)		
PCIE2_TX0_M	54	AO	PCIe2 transmit 0 (-)		
PCIE2_TX1_P	63	AO	PCIe2 transmit 1 (+)		
PCIE2_TX1_M	59	AO	PCIe2 transmit 1 (-)		

PCIE2_RX0_P	68	AI	PCIe2 receive 0 (+)		
PCIE2_RX0_M	64	AI	PCIe2 receive 0 (-)		
PCIE2_RX1_P	73	AI	PCIe2 receive 1 (+)		
PCIE2_RX1_M	69	AI	PCIe2 receive 1 (-)		
PCIE2_REFCLK_P	53	AI	PCIe2 reference clock (+)		If unused, connect this pin to ground.
PCIE2_REFCLK_M	49	AI	PCIe2 reference clock (-)		If unused, connect this pin to ground.
PCIE2_CLKREQ0_N	364	DIO	PCIe2 channel 0 clock request	VCCIO5	When PCIe2 is configured in PCIe × 2 lane mode, this pin is used for clock request function.
PCIE2_WAKE0_N	363	DIO	PCIe2 channel 0 wake up	VCCIO5	When PCIe2 is configured in PCIe × 2 lane mode, this pin is used for wake up function.
PCIE2_RST0_N	362	DIO	PCIe2 channel 0 reset	VCCIO5	When PCIe2 is configured in PCIe × 2 lane mode, this pin is used for reset function.
PCIE2_CLKREQ1_N	368	DI	PCIe2 channel 1 clock request	VCCIO5	
PCIE2_WAKE1_N	369	DI	PCIe2 channel 1 wake up	VCCIO5	
PCIE2_RST1_N	358	DO	PCIe2 channel 1 reset	VCCIO5	
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_VDD	262	PO	SD card power supply	Vnom = VBAT	Dedicated for SD card power supply.
SD_CLK	252	DO	SD card clock	VCCIO3	
SD_CMD	247	DIO	SD card command	VCCIO3	
SD_DATA0	246	DIO	SDIO data bit 0	VCCIO3	

SD_DATA1	251	DIO	SDIO data bit 1	VCCIO3	
SD_DATA2	256	DIO	SDIO data bit 2	VCCIO3	
SD_DATA3	257	DIO	SDIO data bit 3	VCCIO3	
SD_DET	261	DI	SD card hot-plug detect	PMUIO1	
SD_PU_VDD	242	PO	1.8/3.3 V output power for SD card pull-up circuits	Vnom = 1.8/3.3 V	
Touch Panel Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_RST	30	DO	TP reset	PMUIO2	
TP_INT	35	DI	TP interrupt	PMUIO2	
TP_I2C1_SCL	45	OD	TP I2C clock	PMUIO2	
TP_I2C1_SDA	40	OD	TP I2C data	PMUIO2	
LCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD1_RST	322	DO	LCD1 reset	VCCIO6	
DSI0_CLK_N	37	AO	LCD0 MIPI clock (-)		
DSI0_CLK_P	36	AO	LCD0 MIPI clock (+)		
DSI0_LN0_N	47	AO	LCD0 MIPI lane 0 data (-)		
DSI0_LN0_P	46	AO	LCD0 MIPI lane 0 data (+)		
DSI0_LN1_N	42	AO	LCD0 MIPI lane 1 data (-)		
DSI0_LN1_P	41	AO	LCD0 MIPI lane 1 data (+)		
DSI0_LN2_N	32	AO	LCD0 MIPI lane 2 data (-)		
DSI0_LN2_P	31	AO	LCD0 MIPI lane 2 data (+)		
DSI0_LN3_N	27	AO	LCD0 MIPI lane 3 data (-)		

DSI0_LN3_P	26	AO	LCD0 MIPI lane 3 data (+)		
DSI1_CLK_N	33	AO	LCD1 MIPI clock (-)		
DSI1_CLK_P	29	AO	LCD1 MIPI clock (+)		
DSI1_LN0_N	43	AO	LCD1 MIPI lane 0 data (-)		
DSI1_LN0_P	39	AO	LCD1 MIPI lane 0 data (+)		
DSI1_LN1_N	38	AO	LCD1 MIPI lane 1 data (-)		
DSI1_LN1_P	34	AO	LCD1 MIPI lane 1 data (+)		
DSI1_LN2_N	28	AO	LCD1 MIPI lane 2 data (-)		
DSI1_LN2_P	24	AO	LCD1 MIPI lane 2 data (+)		
DSI1_LN3_N	23	AO	LCD1 MIPI lane 3 data (-)		
DSI1_LN3_P	19	AO	LCD1 MIPI lane 3 data (+)		
eDP Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EDP_ML0_P	136	AO	eDP data 0 (+)		
EDP_ML0_N	132	AO	eDP data 0 (-)		
EDP_ML1_P	131	AO	eDP data 1 (+)		
EDP_ML1_N	127	AO	eDP data 1 (-)		
EDP_ML2_P	126	AO	eDP data 2 (+)		
EDP_ML2_N	122	AO	eDP data 2 (-)		
EDP_ML3_P	121	AO	eDP data 3 (+)		
EDP_ML3_N	117	AO	eDP data 3 (-)		
EDP_AUX_P	141	AIO	eDP auxiliary channel (+)		
EDP_AUX_N	137	AIO	eDP auxiliary channel (-)		
EDP_DET	70	DI	eDP hot-plug detect	PMUIO2	

HDMI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
HDMI_TX2_P	72	AO	HDMI data 2 (+)		
HDMI_TX2_M	71	AO	HDMI data 2 (-)		
HDMI_TX1_P	67	AO	HDMI data 1 (+)		
HDMI_TX1_M	66	AO	HDMI data 1 (-)		
HDMI_TX0_P	62	AO	HDMI data 0 (+)		
HDMI_TX0_M	61	AO	HDMI data 0 (-)		
HDMI_CLK_P	57	AO	HDMI clock (+)		
HDMI_CLK_M	56	AO	HDMI clock (-)		
HDMI_DET	379	DI	HDMI hot-plug detect	V_{IH}max = 5.3 V V_{IH}min = 2.4 V	Active high.
HDMI_SCL	387	OD	HDMI I2C clock	VCCIO7	
HDMI_SDA	385	OD	HDMI I2C data	VCCIO7	
HDMI_CEC	382	DIO	HDMI CEC signal	VCCIO7	
Camera Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI_CLK0_N	2	AI	MIPI CSI clock 0 (-)		
CSI_CLK0_P	3	AI	MIPI CSI clock 0 (+)		
CSI_CLK1_N	6	AI	MIPI CSI clock 1 (-)		
CSI_CLK1_P	9	AI	MIPI CSI clock 1 (+)		
CSI_LN0_N	7	AI	MIPI CSI lane 0 data (-)		
CSI_LN0_P	8	AI	MIPI CSI lane 0 data (+)		
CSI_LN1_N	4	AI	MIPI CSI lane 1 data (-)		
CSI_LN1_P	5	AI	MIPI CSI lane 1 data (+)		
CSI_LN2_N	16	AI	MIPI CSI lane 2 data (-)		

CSI_LN2_P	17	AI	MIPI CSI lane 2 data (+)		
CSI_LN3_N	11	AI	MIPI CSI lane 3 data (-)		
CSI_LN3_P	12	AI	MIPI CSI lane 3 data (+)		
CAM0_MCLK	279	DO	Master clock of camera 0	VCCIO6	
CAM0_RST	317	DO	Reset of camera 0	VCCIO6	
CAM0_PWDN	316	DO	Power down of camera 0	VCCIO6	
CAM1_MCLK	75	DO	Master clock of camera 1	PMUIO1	
CAM1_RST	314	DO	Reset of camera 1	VCCIO6	
CAM1_PWDN	313	DO	Power down of camera 1	VCCIO6	
RGMII Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RGMII0_RX0	183	DI	RGMII0 receive data bit 0	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_RX1	179	DI	RGMII0 receive data bit 1	VCCIO4	
RGMII0_RX2	174	DI	RGMII0 receive data bit 2	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_RX3	169	DI	RGMII0 receive data bit 3	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_RX_CTL	175	DI	RGMII0 receive control	VCCIO4	
RGMII0_RX_CLK	164	DI	RGMII0 receive clock	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_TX0	168	DO	RGMII0 transmit data bit 0	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_TX1	173	DO	RGMII0 transmit data bit 1	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_TX2	178	DO	RGMII0 transmit data bit 2	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_TX3	182	DO	RGMII0 transmit data bit 3	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_TX_CTL	172	DO	RGMII0 transmit control	VCCIO4	Only SG368Z-AP supports this pin.

RGMII0_TX_CLK	163	DO	RGMII0 transmit clock	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_MDC	181	DO	RGMII0 management data clock	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_MDIO	185	OD	RGMII0 management data input/output	VCCIO4	Only SG368Z-AP supports this pin.
RGMII0_REFCLKOUT	160	DO	RGMII0 reference clock output	VCCIO4	The output frequency of reference clock is 25 MHz.
RGMII0_MCLK	177	DI	RGMII0 clock input	VCCIO4	The output frequency of reference clock is 125 MHz; Only SG368Z-AP supports this pin.
RGMII1_RX0	296	DI	RGMII1 receive data bit 0	VCCIO6	
RGMII1_RX1	294	DI	RGMII1 receive data bit 1	VCCIO6	
RGMII1_RX2	308	DI	RGMII1 receive data bit 2	VCCIO6	
RGMII1_RX3	307	DI	RGMII1 receive data bit 3	VCCIO6	
RGMII1_RX_CTL	293	DI	RGMII1 receive control	VCCIO6	
RGMII1_RX_CLK	304	DI	RGMII1 receive clock	VCCIO6	
RGMII1_TX0	305	DO	RGMII1 transmit data bit 0	VCCIO6	
RGMII1_TX1	303	DO	RGMII1 transmit data bit 1	VCCIO6	
RGMII1_TX2	312	DO	RGMII1 transmit data bit 2	VCCIO6	
RGMII1_TX3	310	DO	RGMII1 transmit data bit 3	VCCIO6	
RGMII1_TX_CTL	298	DO	RGMII1 transmit control	VCCIO6	
RGMII1_TX_CLK	306	DO	RGMII1 transmit clock	VCCIO6	
RGMII1_MDC	290	DO	RGMII1 management data	VCCIO6	

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
			clock		
RGMII1_MDIO	286	OD	RGMII1 management data input/output	VCCIO6	
RGMII1_ REFCLKOUT	288	DO	RGMII1 reference clock output	VCCIO6	The output frequency of reference clock is 25 MHz.
RGMII1_MCLK	278	DI	RGMII1 clock input	VCCIO6	The output frequency of reference clock is 125 MHz.
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	226	DI	Turn on/off the module	VBAT	Active low.
VOL_UP/BOOT	236	AI	Volume up; Control the module into firmware upgrade mode	1.8 V	Active low. A test point is recommended to be reserved.
VOL_DOWN	232	AI	Volume down	1.8 V	Active low.
RESET_N	231	DI	Reset the module	1.8 V	Active low. A test point is recommended to be reserved if unused.
PON_1	221	DI	LOW to HIGH indicates power on	$V_{IH}max$ = 1.4 V $V_{IH}min$ = 0.8 V	Under normal VBAT power supply conditions, if this pin is detected as high level, the turning-on process will be triggered. After turning-on, PON_1 can be pulled down or kept high, which does not affect the turning-on status.

ESC	227	AI	Esc keypad	1.8 V	Active low.
MENU	222	AI	Menu keypad	1.8 V	Active low.
UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	374	DO	Debug UART transmit	PMUIO2	The default baud rate is 115200 bps. Test points must be reserved.
DBG_RXD	378	DI	Debug UART receive	PMUIO2	
UART3_TXD	339	DO	UART3 transmit	VCCIO5	
UART3_RXD	334	DI	UART3 receive	VCCIO5	
UART4_TXD	344	DO	UART4 transmit	VCCIO5	
UART4_RXD	349	DI	UART4 receive	VCCIO5	
UART5_TXD	332	DO	UART5 transmit	VCCIO5	
UART5_RXD	331	DI	UART5 receive	VCCIO5	
UART7_TXD	327	DO	UART7 transmit	VCCIO5	
UART7_RXD	328	DI	UART7 receive	VCCIO5	
UART8_TXD	361	DO	UART8 transmit	VCCIO5	
UART8_RXD	357	DI	UART8 receive	VCCIO5	
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C2_SDA	284	OD	I2C2 serial data	VCCIO6	
I2C2_SCL	287	OD	I2C2 serial clock	VCCIO6	
I2C3_SDA	268	OD	I2C3 serial data	VCCIO1	
I2C3_SCL	273	OD	I2C3 serial clock	VCCIO1	
I2C4_SDA	155	OD	I2C4 serial data	VCCIO4	
I2C4_SCL	159	OD	I2C4 serial clock	VCCIO4	
I2S and PDM Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
I2S3_SCLK	386	DO	I2S3 bit clock	VCCIO7	
I2S3_LRCK	388	DO	I2S3 channel select	VCCIO7	
I2S3_DOUT	380	DO	I2S3 data output	VCCIO7	
I2S3_DIN	383	DI	I2S3 data input	VCCIO7	
I2S3_MCLK	376	DO	I2S3 master clock	VCCIO7	
PDM_CLK1	258	DO	PDM clock 1	VCCIO1	
PDM_DIN1	253	DI	PDM data input 1	VCCIO1	
PDM_DIN2	248	DI	PDM data input 2	VCCIO1	
PDM_DIN3	243	DI	PDM data input 3	VCCIO1	
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_RF	206	AIO	Wi-Fi/Bluetooth antenna interface		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC2	218	AI	General-purpose ADC interface		Input voltage range: 0~1.8 V
ADC4	233	AI	General-purpose ADC interface		
ADC5	228	AI	General-purpose ADC interface		
ADC6	223	AI	General-purpose ADC interface		
ADC7	213	AI	General-purpose ADC interface		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
EXT_EN	217	DO	External device enable signal	Vnom = VBAT	After the module is turned on, this pin outputs a high level.

PMU_32K_CLK	150	OD	PMU 32 kHz clock output		Only SG368Z-AP supports this pin.
32K_CLK	165	DO	32 kHz clock output	VCCIO4	Only SG368Z-AP supports this pin.
PWM4	55	DO	PWM output 4	PMUIO2	
GPIO					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO0_D3	125	DIO	General-purpose input/output	PMUIO0	
GPIO0_D4	60	DIO	General-purpose input/output	PMUIO0	
GPIO0_D5	80	DIO	General-purpose input/output	PMUIO0	
GPIO0_D6	10	DIO	General-purpose input/output	PMUIO0	
GPIO0_A5	123	DIO	General-purpose input/output	PMUIO1	
GPIO0_B0	225	DIO	General-purpose input/output	PMUIO2	Only SG368Z-AP supports this pin.
GPIO0_B7	220	DIO	General-purpose input/output	PMUIO2	Only SG368Z-AP supports this pin.
GPIO0_C0	215	DIO	General-purpose input/output	PMUIO2	Only SG368Z-AP supports this pin.
GPIO0_C1	50	DIO	General-purpose input/output	PMUIO2	Only SG368Z-AP supports this pin.
GPIO0_C4	25	DIO	General-purpose input/output	PMUIO2	
GPIO0_C5	210	DIO	General-purpose input/output	PMUIO2	Only SG368Z-AP supports this pin.
GPIO0_C6	370	DIO	General-purpose input/output	PMUIO2	
GPIO0_C7	209	DIO	General-purpose input/output	PMUIO2	Only SG368Z-AP supports this pin.
GPIO1_D0	276	DIO	General-purpose input/output	VCCIO2	
GPIO1_D1	267	DIO	General-purpose input/output	VCCIO2	
GPIO1_D2	272	DIO	General-purpose input/output	VCCIO2	
GPIO1_D3	281	DIO	General-purpose input/output	VCCIO2	

GPIO1_D4	277	DIO	General-purpose input/output	VCCIO2	
GPIO2_C5	170	DIO	General-purpose input/output	VCCIO4	Only SG368Z-AP supports this pin.
GPIO3_A2	359	DIO	General-purpose input/output	VCCIO5	
GPIO3_A3	354	DIO	General-purpose input/output	VCCIO5	
GPIO3_A4	352	DIO	General-purpose input/output	VCCIO5	
GPIO3_A5	351	DIO	General-purpose input/output	VCCIO5	
GPIO3_A6	346	DIO	General-purpose input/output	VCCIO5	
GPIO3_A7	347	DIO	General-purpose input/output	VCCIO5	
GPIO3_B0	348	DIO	General-purpose input/output	VCCIO5	
GPIO3_B3	343	DIO	General-purpose input/output	VCCIO5	
GPIO3_B4	342	DIO	General-purpose input/output	VCCIO5	
GPIO3_B5	336	DIO	General-purpose input/output	VCCIO5	
GPIO3_B6	337	DIO	General-purpose input/output	VCCIO5	
GPIO3_C6	321	DIO	General-purpose input/output	VCCIO6	
GPIO3_D0	318	DIO	General-purpose input/output	VCCIO6	
GPIO3_D1	319	DIO	General-purpose input/output	VCCIO6	
GPIO4_B2	291	DIO	General-purpose input/output	VCCIO6	
GPIO4_D2	384	DIO	General-purpose input/output	VCCIO7	
RESERVED Pins					
Pin Name	**Pin No.**				
RESERVED	15, 20, 130, 135, 140, 192, 197, 198, 201, 204, 205, 208, 214, 219, 229, 230, 234, 239, 240, 244, 245, 249, 250, 254, 255, 260, 264, 265, 269, 270, 275, 299, 315, 320, 329, 330, 335, 340, 345, 360, 365, 377, 381				

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (SG368Z Series EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Interface

The module provides 8 VBAT pins dedicate to connecting with the external power supply. The power supply range of the module is 3.3–3.5 V, and the recommended value is 3.4 V.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Comment
VBAT	147, 148, 151, 152, 153, 156, 157, 161	PI	Power supply for the module	
GND	142, 143, 144, 146, 149, 154, 158, 162, 166		Ground	

3.1.2. Reference Design for Power Supply

Power design for the module is essential. The power supply of the module should be able to provide sufficient current of 3 A* at least. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for LDO power supply:

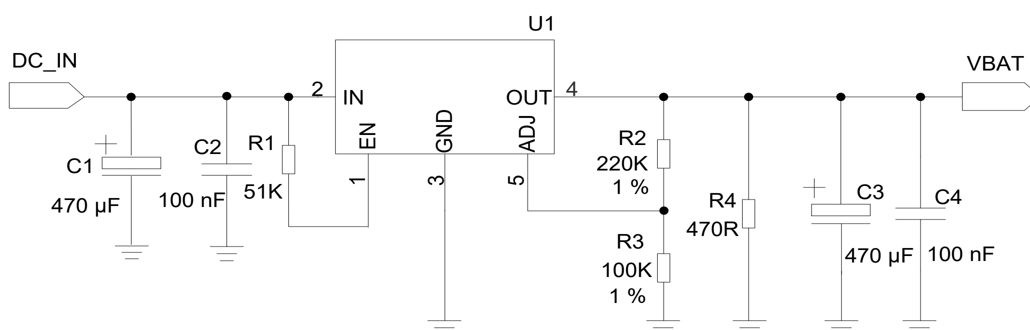


Figure 2: Reference Design of Power Input

NOTE

To avoid corrupting the data in the internal flash, do not turn off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY, then you can cut off the power supply.

3.1.3. Requirements for Voltage Stability

The recommended power supply voltage of the module is 3.4 V. The power supply performance, such as load capacity, voltage ripple, etc. will directly influence the module's performance and stability. Under ultimate conditions, the module may have a transient peak current up to 3 A*. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.3 V, the module will turn off automatically. Therefore, ensure the input voltage never drops below 3.3 V.

To prevent the voltage from dropping below 3.3 V, it is recommended to connect a 100 μF bypass capacitor with low ESR as well as 4.7 μF, 100 nF, 33 pF and 10 pF filter capacitors in parallel near the VBAT pins of the module. It is also recommended that the PCB traces of VBAT should be as short as possible and wide enough to reduce the equivalent impedance of the VBAT traces and ensure that there will be no large voltage drop under high current at the maximum transmission power. The width of VBAT trace should be at least 3 mm*. As per design rules, the longer the VBAT trace is, the wider it should be. Additionally, the ground plane of the power supply part should be as complete as possible.

To suppress the impact of power fluctuations and ensure the stability of the output power supply, it is suggested to add a TVS component of at least 2000 W and place it as close to the VBAT pins as possible to enhance surge protection. The following figure shows a reference circuit:

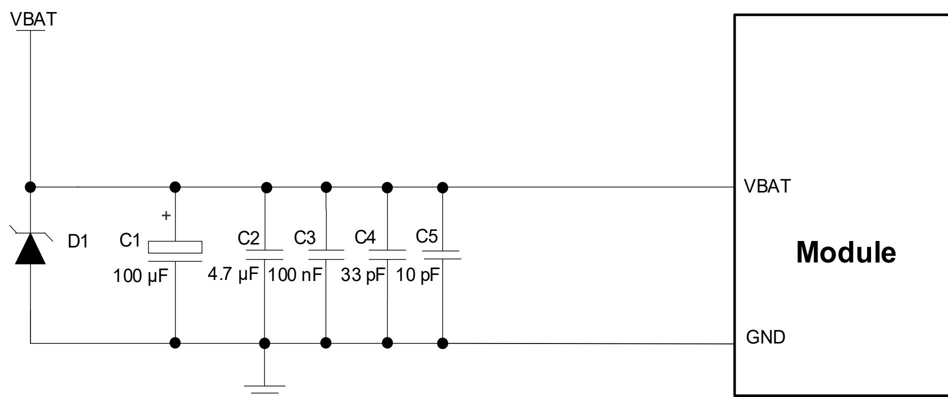


Figure 3: Reference Design of Power Supply

3.2. Turn On

3.2.1. Turn On with PWRKEY

Table 8: Pins Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	226	DI	Turn on/off the module	Active low.

When powering up the VBAT, the module can be turned on by driving PWRKEY low for at least 200 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. PWRKEY is pulled up to VBAT internally.

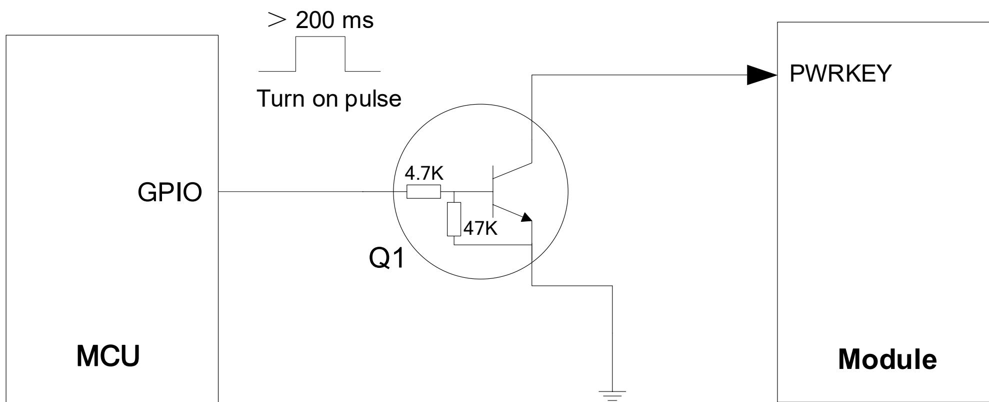


Figure 4: Reference Design of Turn On with Driving Circuit

Another way to control the PWRKEY is using a keystroke directly. When pressing the keystroke, an electrostatic strike may be generated from finger. Therefore, you should place a TVS near the keystroke for ESD protection. Additionally, a 1 kΩ resistor is connected in series to PWRKEY for ESD protection.

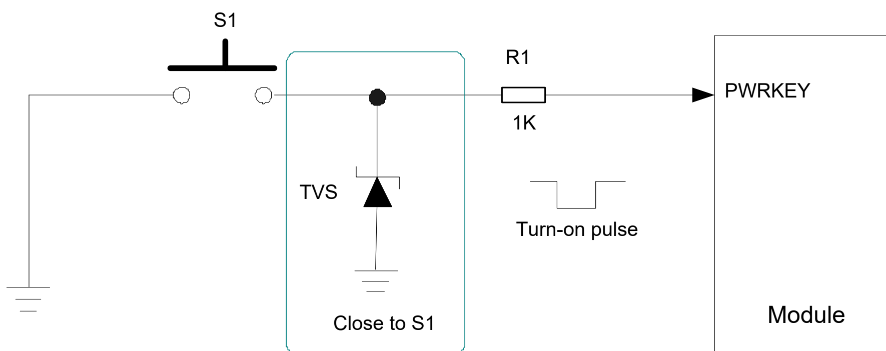


Figure 5: Reference Design of Turn On with Keystroke

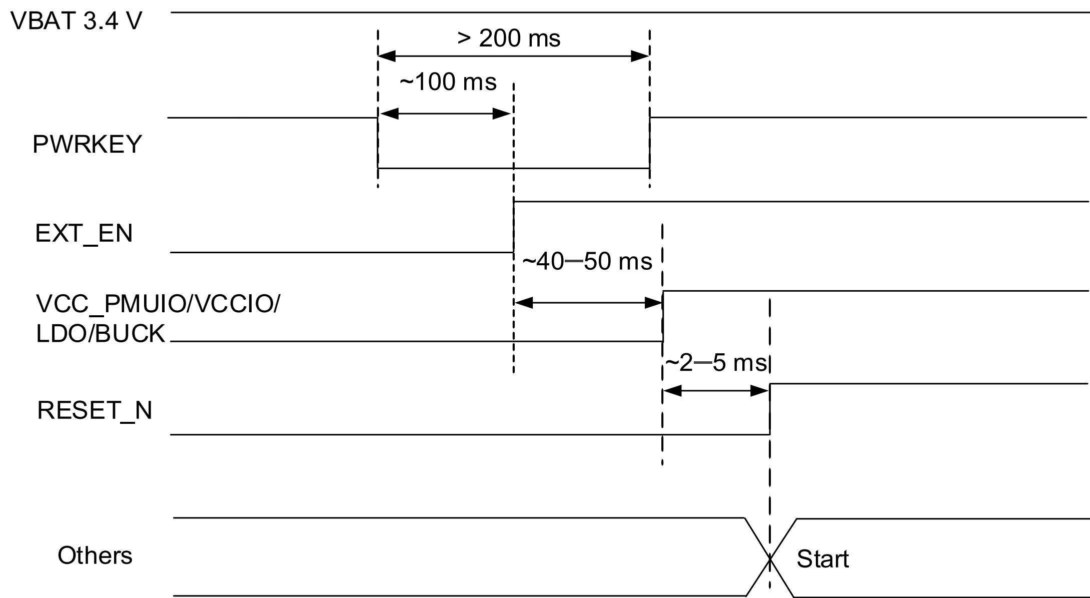


Figure 6: Timing of Turn On with PWRKEY

NOTE

1. When the module is powered up for the first time, its turn on timing may be different from that shown in the figure above.
2. Ensure the voltage of VBAT is stable before driving the PWRKEY low. It is recommended to drive PWRKEY low after VBAT reaches 3.4 V and remains stable. PWRKEY cannot be driven low all the time.

3.2.2. Turn On with PON_1

Table 9: Pins Description of PON_1

Pin Name	Pin No.	I/O	Description	Comment
PON_1	221	DI	LOW to HIGH indicates power on	High level voltage range: 0.8–1.4 V Recommended value: 1.2 V

Under normal VBAT power supply conditions, pull up PON_1, and then the turning-on process will be triggered. After the module is turned on, PON_1 can be pulled down or kept high, which does not affect the turning-on status.

3.3. Turn Off/Restart

The module can be turned off by driving the PWRKEY low for at least 6 seconds. It can be restarted by driving RESET_N low (for at least 100 ms).

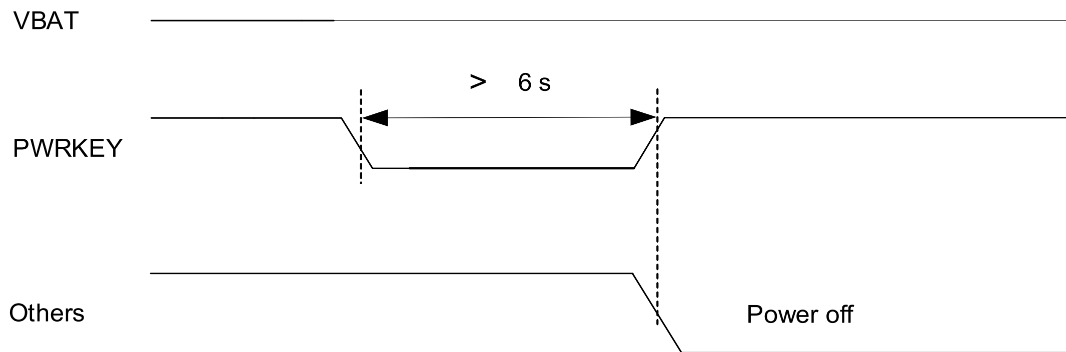


Figure 7: Timing of Turn Off

3.4. Standby

Under normal conditions, driving PWRKEY low for 0.5–1 s can make the module enter standby state. Then driving PWRKEY low for 0.5–1 s again can wake up the module.

3.5. Power Output

The module supports multiple regulated voltage output for peripheral circuits. In practical application, it is recommended to use a 10-pF and a 33-pF capacitor in parallel to suppress high-frequency noise.

Table 10: Power Information

Pin Name	Default Voltage (V)	Drive Current (mA)	Standby
VCCIO1	1.8	50	OFF
VCCIO2	1.8	50	OFF
VCCIO4	1.8	50	ON
VCCIO5	1.8	50	OFF

VCCIO6	1.8	50	OFF
VCCIO7	1.8	50	OFF
VCC_PMUIO2	1.8	50	ON
LDO6_3V3	3.3	50	ON
LDO9_1V8	1.8	50	OFF
BUCK5_1V8	1.8	100	OFF
VCC_SWOUT1	1.8	100	OFF

NOTE

IO of VCCIO4 power domain will power down in standby state.

4 Application Interfaces

4.1. USB Interfaces

The module provides 4 USB interfaces which complies with USB 3.0 and USB 2.0 specifications. USB 3.0 supports SuperSpeed mode and the data rate is up to 5 Gbps; USB 2.0 supports high-speed mode and the data rate is up to 480 Mbps.

USB0 interface:

- Supports USB 3.0 and USB 2.0 specifications
- Supports USB OTG function
- Supports Host mode and Device mode
- Supports AT command communication, data transmission, software debugging, firmware upgrade (only supports firmware upgrade through USB 2.0)
- USB 3.0 SS channel can be multiplexed into SATA0* interface. For the multiplexing relationship, see ***document [2]***

USB1 interface:

- Supports USB 3.0 and USB 2.0 specifications
- Only supports Host mode
- USB3.0 SS channel can be multiplexed into SATA1 or QSGMII/SGMII* interface. For the multiplexing relationship, see ***document [2]***

USB2 and USB3 interfaces:

- Support USB 2.0 specifications
- Only support Host mode

Table 11: Pins Description of USB Interfaces

Pin Name	Pin No.	I/O	Description	Comment
HOST_PWR_EN	85	DO	Host USB VBUS power enable	

USB0_VBUS	111	DI	USB0 insertion detection	Can not supply power for peripherals. A test point must be reserved.
USB0_ID	118	DI	USB0 ID detect	Internally pull up to 1.8 V.
USB0_DP	112	AIO	USB0 2.0 differential data (+)	A test point must be reserved.
USB0_DM	113	AIO	USB0 2.0 differential data (-)	A test point must be reserved.
USB0_SS_TX_P	107	AO	USB0 3.0 transmit (+)	
USB0_SS_TX_M	108	AO	USB0 3.0 transmit (-)	
USB0_SS_RX_P	109	AI	USB0 3.0 receive (+)	
USB0_SS_RX_M	110	AI	USB0 3.0 receive (-)	
USB1_DP	79	AIO	USB1 2.0 differential data (+)	
USB1_DM	83	AIO	USB1 2.0 differential data (-)	
USB1_SS_TX_P	84	AO	USB1 3.0 transmit (+)	
USB1_SS_TX_M	88	AO	USB1 3.0 transmit (-)	
USB1_SS_RX_P	89	AI	USB1 3.0 receive (+)	
USB1_SS_RX_M	92	AI	USB1 3.0 receive (-)	
USB2_DP	289	AIO	USB2 2.0 differential data (+)	
USB2_DM	292	AIO	USB2 2.0 differential data (-)	
USB3_DP	295	AIO	USB3 2.0 differential data (+)	
USB3_DM	297	AIO	USB3 2.0 differential data (-)	

4.1.1. Micro USB Interface

Only USB0_DP and USB0_DM are the system firmware burning interface. If you do not use this interface, please be sure to reserve this interface and test points during the debugging and production process, otherwise you will not be able to debug and produce burning firmware.

USB0_ID is internally pulled up to 1.8 V with an about 200 kΩ resistor.

USB0_VBUS is used to detect OTG mode and Device mode. It is active at high level. Its voltage range is 2.7–3.3 V, and the typical value is 3.0 V. It is recommended to place a 100 nF capacitor near

USB0_VBUS.

USB0 can be configured in the following three modes:

- OTG mode (default): USB0 can switch automatically between Device mode and Host mode according to the state of USB0_ID. If USB0_ID is at high level, USB0 is in Device mode, and if USB0_ID is at low level, USB0 is in Host mode. In Device mode, the module can judge whether the USB0_VBUS pin is at high level. If it is, USB0_DP will be pulled up to start enumeration.
- Device mode: When USB0 is configured to this mode, there is no need to pay attention to the state of USB0_ID. The module only needs to judge whether the USB0_VBUS pin is at high level. If it is, USB0_DP will be pulled up to start enumeration.
- Host mode: When USB0 is configured to this mode, there is no need to pay attention to the states of USB0_ID and USB0_VBUS. (If you only need Host mode, but you also need to use USB0_DP/USB0_DM for system firmware burning during debugging and production, then you need to configure USB0 to Device mode during burning and ABD debugging. Under this condition, USB0_VBUS signal must be connected.)
- Before Uboot starts, USB0 is in Device mode by default; after Uboot starts, USB0 can be configured to the above three modes according to demand.

The reference design of Micro USB interface realized by USB0 is shown below:

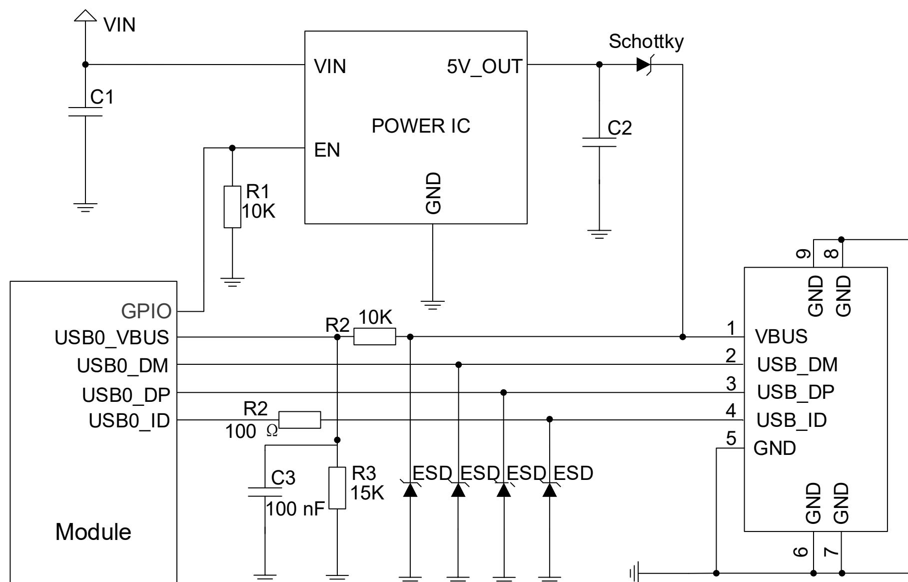


Figure 8: Reference Design of Micro USB Interface

NOTE

1. To suppress electromagnetic radiation, common-mode chokes (common-mode choke coil) can be added on the USB0_DP/USB0_DM signals, and other USB 2.0 interfaces can also refer to this

design.

2. The Schottky diode in the above figure is used for anti-backflow, which will affect the VBUS output power supply capability. If there is a high requirement for power supply capability, it is recommended to choose a power chip that supports anti-backflow.

4.1.2. USB Type-A Interface

The reference design of USB Type-A interface realized by USB0 is shown below:

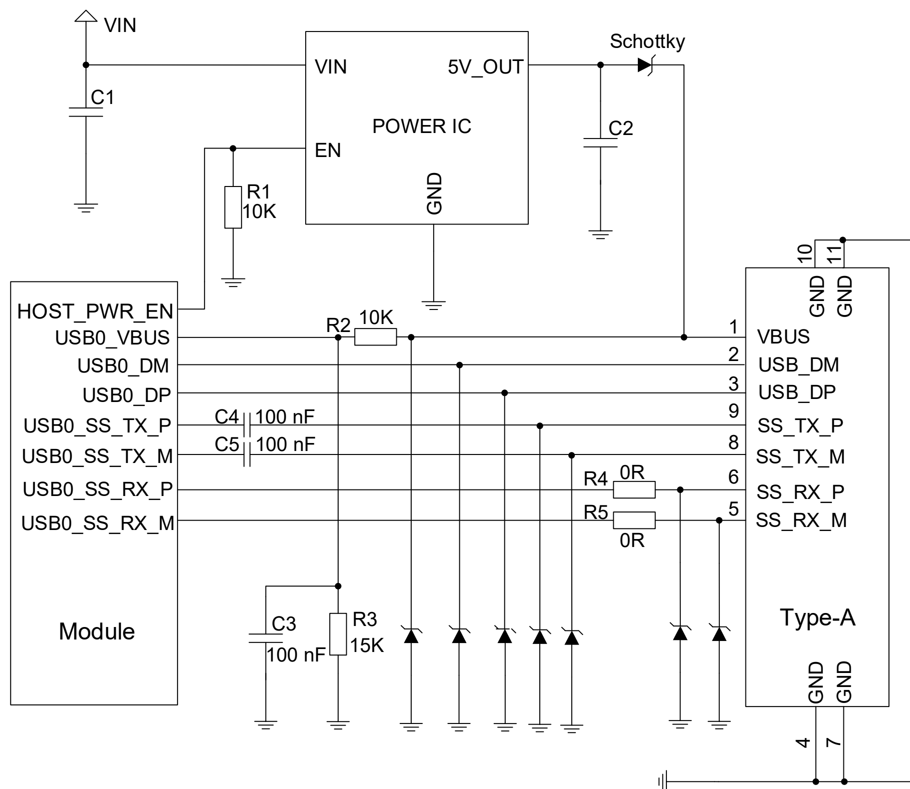


Figure 9: Reference Design of USB Type-A Interface

NOTE

1. USB Type-C design requires an external CC logic chip and an SS channel switch. For details, see ***document [3]***.
2. The Type-A design of USB1, USB2, and USB3 interfaces can refer to the above figure. It should be noted that the module does not have corresponding VBUS and USB_ID. For external VBUS 5 V output enable control pin, you can choose HOST_PWR_EN, or choose other GPIO.

4.1.3. USB Interface Design Considerations

Table 12: USB Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching (P-M)
USB0_DP	112	31.89	0.09
USB0_DM	113	31.80	
USB0_SS_TX_P	107	34.35	-0.03
USB0_SS_TX_M	108	34.38	
USB0_SS_RX_P	109	31.63	0.08
USB0_SS_RX_M	110	31.55	
USB1_DP	79	21.90	0.09
USB1_DM	83	21.81	
USB1_SS_TX_P	84	22.27	-0.18
USB1_SS_TX_M	88	22.45	
USB1_SS_RX_P	89	26.00	-0.12
USB1_SS_RX_M	92	26.12	
USB2_DP	289	43.18	0.18
USB2_DM	292	43.00	
USB3_DP	295	42.56	0.25
USB3_DM	297	42.31	

To ensure performance, you should follow the following principles when designing USB interfaces:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- The reference ground plane under the USB signal traces must be continuous without any cuts or vias

to ensure impedance continuity.

- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data traces. Typically, stray capacitance should be less than 3 pF for USB 2.0, and less than 0.4 pF for USB 3.0.
- Do not route USB 3.0 signal traces under RF signal traces. Crossing or being parallel with RF signal traces is forbidden.
- For USB 3.0 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 0.3 mm.
- For USB 3.0, the clearance between Rx and Tx signal traces should be 4 times the signal trace width. The clearance between USB 3.0 signal traces and other signal traces should be 4 times the signal trace width.
- For USB 2.0 signal traces, the differential data pair matching (P/M) should be less than 0.5 mm.
- For USB 2.0, the clearance between DP-DM signal traces and other signal traces should be 3 times the signal trace width.

4.2. VOL_UP/BOOT

VOL_UP/BOOT is used to control the module to enter firmware upgrade mode. It is at high level by default. On the premise that VOL_UP/BOOT is not pressed and the module has been burned with firmware, VOL_UP/BOOT is used for the volume up function by default after the module is turned on. If VOL_UP/BOOT button is pressed when the module is turned on, that is, VOL_UP/BOOT is kept at low level, the module enters the Loader burning mode. When the PC recognizes the USB device, release the button to restore the VOL_UP/BOOT to high level and then you can upgrade the firmware.

Table 13: Pins Description of VOL_UP/BOOT

Pin Name	Pin No.	I/O	Description	Comment
VOL_UP/BOOT	236	AI	Volume up; Control the module into firmware upgrade mode	Active low. A test point is recommended to be reserved.

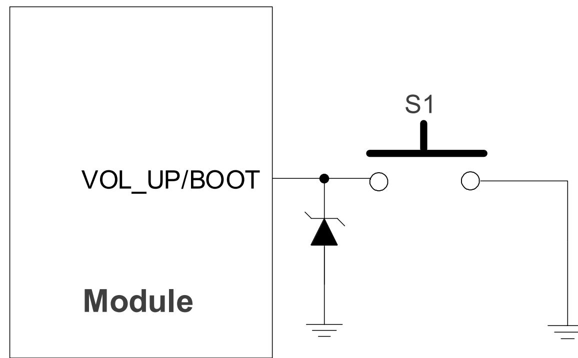


Figure 10: Reference Design of VOL_UP/BOOT

NOTE

The VOL_UP/BOOT grounded circuit cannot be connected in series with resistors to prevent affecting the internal voltage division.

4.3. SD Card Interface

SD card interface of the module complies with SD 3.0 specifications:

Table 14: Pins Description of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_VDD	262	PO	SD card power supply	Dedicated for SD card power supply.
SD_CLK	252	DO	SD card clock	
SD_CMD	247	DIO	SD card command	
SD_DATA0	246	DIO	SDIO data bit 0	
SD_DATA1	251	DIO	SDIO data bit 1	
SD_DATA2	256	DIO	SDIO data bit 2	
SD_DATA3	257	DIO	SDIO data bit 3	
SD_DET	261	DI	SD card hot-plug detect	

SD_PU_VDD	242	PO	1.8/3.3 V output power for SD card pull-up circuits

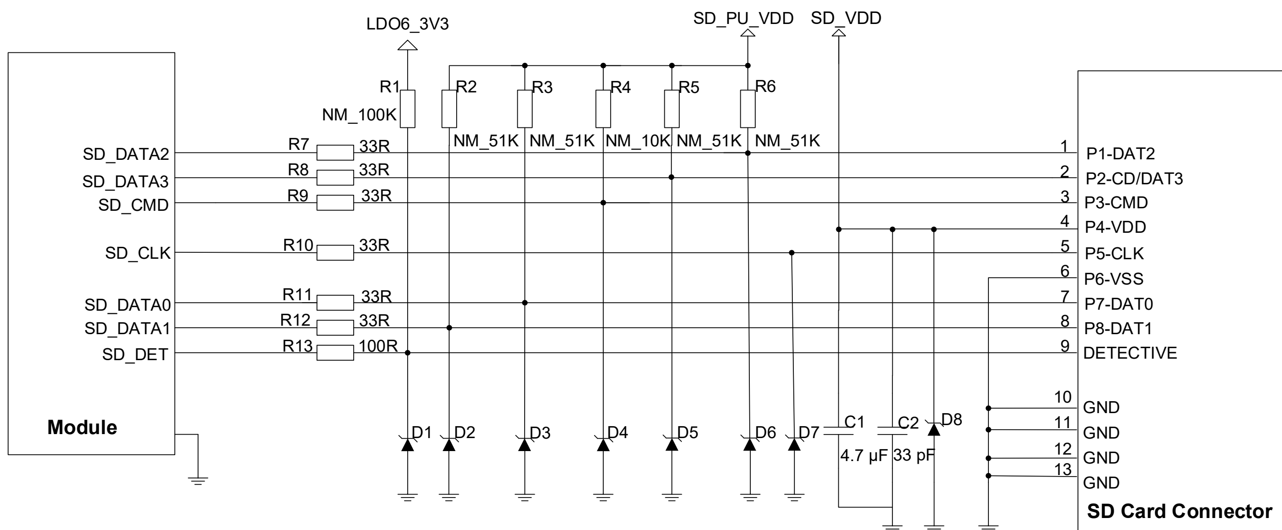


Figure 11: Reference Design of SD Card Interface

SD_VDD is a peripheral driver power supply for SD card. The maximum drive current is 600 mA. Because of the high drive current, it is recommended to keep the trace width as at least 0.6 mm. To ensure the stability of drive power, you should add a 4.7-μF and a 33-pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK and SD_DATA[0:3] are all high-speed signal traces. In PCB design, control the characteristic impedance of these traces as 50 Ω, shield them and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB and keep their lengths the same. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 50 Ω ±10 %, and add ground shielding.
- Trace length matching between SD_CLK and SD_CMD/SD_DATA should be less than 3 mm.
- Trace length requirements: less than 150 mm when SD_CLK frequency is less than or equal to 50 MHz; less than 100 mm when SD_CLK frequency is greater than 50 MHz.
- Clearance between SD card signal traces should be greater than or equal to 2 times the trace width and the clearance between SD card signal traces and other signal traces should be greater than or equal to 3 times the trace width.
- The load capacitance requirements of SD_DATA[0:3], SD_CLK and SD_CMD traces: less than 9 pF for SD 2.0; less than 1 pF for SD 3.0.

Table 15: SD Card Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching with SD_CLK
SD_CLK	252	43.60	-
SD_CMD	247	42.92	0.68
SD_DATA0	246	41.08	2.52
SD_DATA1	251	41.44	2.16
SD_DATA2	256	41.73	1.87
SD_DATA3	257	41.83	1.77

4.4. UART

SG368Z-WF supports up to 8 groups of UART and SG368Z-AP supports up to 10 groups of UART. 6 of them are configured by default, and the rest of them are multiplexed from other interfaces. For detailed multiplexing relationship, see ***document [2]***.

UART features:

- Each UART contains two 64-byte FIFOs for data reception and transmission
- Support 115.2 kbps, 460.8 kbps, 921.6 kbps, 1.5 Mbps, 3 Mbps and 4 Mbps
- Support programmable baud rate and non-integer clock divider
- Support 5–8 bit width transmission

Table 16: Pins Description of UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	374	DO	Debug UART transmit	The default baud rate is 115200 bps. Test points must be reserved.
DBG_RXD	378	DI	Debug UART receive	
UART3_TXD	339	DO	UART3 transmit	
UART3_RXD	334	DI	UART3 receive	
UART4_TXD	344	DO	UART4 transmit	

UART4_RXD	349	DI	UART4 receive
UART5_TXD	332	DO	UART5 transmit
UART5_RXD	331	DI	UART5 receive
UART7_TXD	327	DO	UART7 transmit
UART7_RXD	328	DI	UART7 receive
UART8_TXD	361	DO	UART8 transmit
UART8_RXD	357	DI	UART8 receive

The power domain of UART is 1.8 V. You can use a level-shifting chip between the module and host's UART if the power domains are not matching:

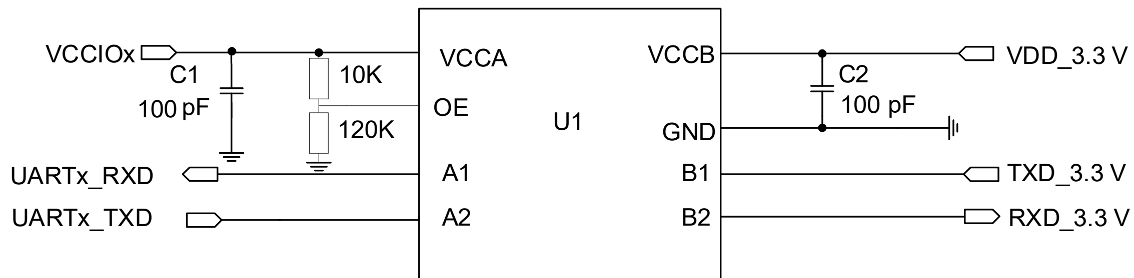


Figure 12: Reference Design of UART with Level-shifting Chip

NOTE

Debug UART is similar to UARTx and for the reference design, refer to ***Figure 12***. For debug UART, VCC_PMUIO2 is used as power supply pin for VCCA.

4.5. I2C Interfaces

The module supports up to 5 groups of I2C interfaces. 4 of them are configured by default, and 1 of them is multiplexed from other interfaces. For detailed multiplexing relationship, see ***document [2]***. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V.

I2C features:

- Support I2C bus master mode
- Support programmable clock frequency by software and the data rate is up to 400 kbps
- Support 7-bit and 10-bit addressing modes

Table 17: Pins Description of I2C Interfaces

Pin Name	Pin No.	I/O	Description
I2C2_SDA	284	OD	I2C2 serial data
I2C2_SCL	287	OD	I2C2 serial clock
I2C3_SDA	268	OD	I2C3 serial data
I2C3_SCL	273	OD	I2C3 serial clock
I2C4_SDA	155	OD	I2C4 serial data
I2C4_SCL	159	OD	I2C4 serial clock
TP_I2C1_SCL	45	OD	TP I2C clock
TP_I2C1_SDA	40	OD	TP I2C data

4.6. I2S Interfaces

SG368Z-WF supports up to 1 group of I2S interface; SG368Z-AP supports up to 2 groups of I2S interfaces. 1 of them is configured by default and 1 of them is multiplexed from other interface, see ***document [2]***.

I2S features:

- Bit rate is from 16 bits to 32 bits
- Sampling rate is up to 192 kHz
- Support master or slave mode
- Support I2S, PCM, TDM modes
- Support PCM formats: early, late1, late2, late3
- Support up to TDM 16 channels
- I2S, PCM, TDM modes can not be used simultaneously

Table 18: Pins Description of I2S Interfaces

Pin Name	Pin No.	I/O	Description
I2S3_SCLK	386	DO	I2S3 bit clock
I2S3_LRCK	388	DO	I2S3 channel select
I2S3_DOUT	380	DO	I2S3 data output
I2S3_DIN	383	DI	I2S3 data input
I2S3_MCLK	376	DO	I2S3 master clock

4.7. PDM Interface

The module supports 1 group of digital audio interface. The interface supports up to 6-lane PDM audio input. The sampling rate is up to 192 kHz and the bit rate is from 16 bits to 32 bits.

Table 19: Pins Description of PDM Interface

Pin Name	Pin No.	I/O	Description
PDM_CLK1	258	DO	PDM clock 1
PDM_DIN1	253	DI	PDM data input 1
PDM_DIN2	248	DI	PDM data input 2
PDM_DIN3	243	DI	PDM data input 3

4.8. Analog Audio Interfaces

The module provides 1 analog input channels and 2 analog output channels:

Table 20: Pins Description of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
HPH_L	100	AO	Headphone left channel output	

HPH_R	102	AO	Headphone right channel output	
HPH_GND	101	AI	Headphone reference ground	If unused, connect this pin to ground.
SPK_P	104	AO	Loudspeaker output (+)	
SPK_M	103	AO	Loudspeaker output (-)	
MIC_P	98	AI	Microphone input (+)	
MIC_M	97	AI	Microphone input (-)	
VCC_SPK_HP	176	PI	Analog audio power supply	If the analog audio function is not used, this pin needs to be connected to VBAT.

- The module offers 1 differential MIC input pair, which can also be used as 2 single-ended MIC input channels.
- VCCIO1 can be used as MIC_BIAS and the output voltage is 1.8 V by default.
- The loudspeaker interface uses the differential output. The output channel is available with a Class D amplifier whose maximum output power is 1.3 W when the load is 8 Ω.
- The headset interface features stereo left and right channel output, and headset insert detection function is supported.

4.8.1. Microphone Interface Reference Design

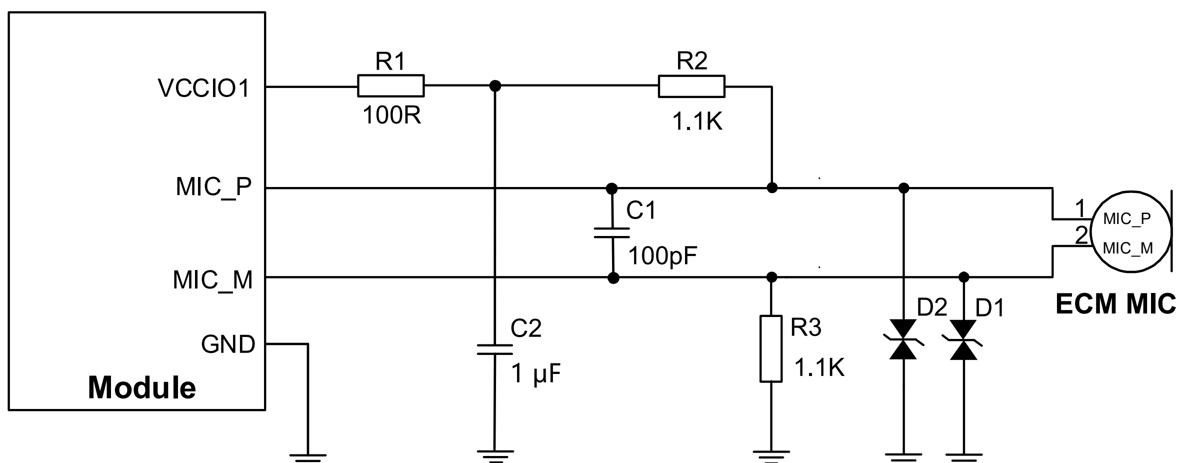


Figure 13: Reference Design of Differential Microphone Interface

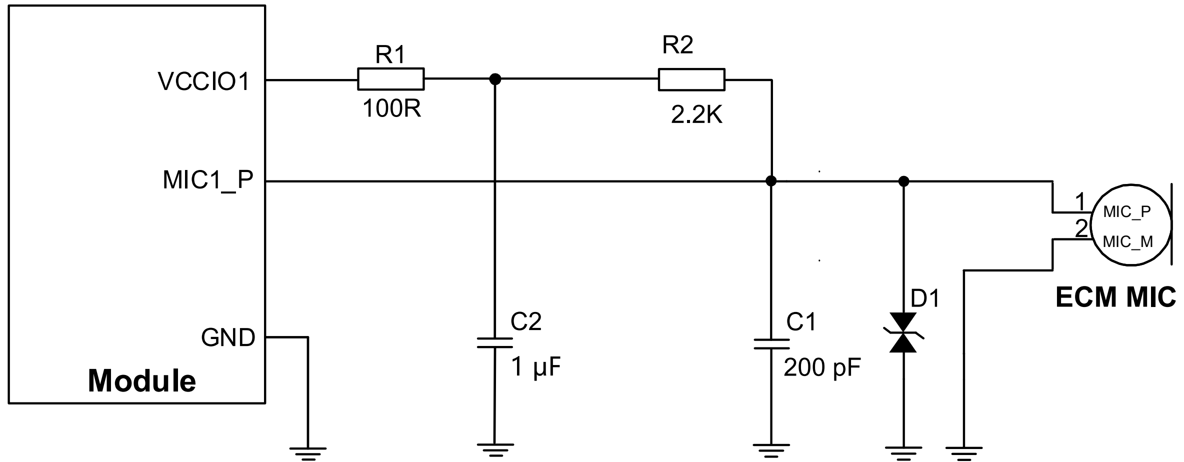


Figure 14: Reference Design of Single-ended Microphone Interface

4.8.2. Headset Interface Reference Design

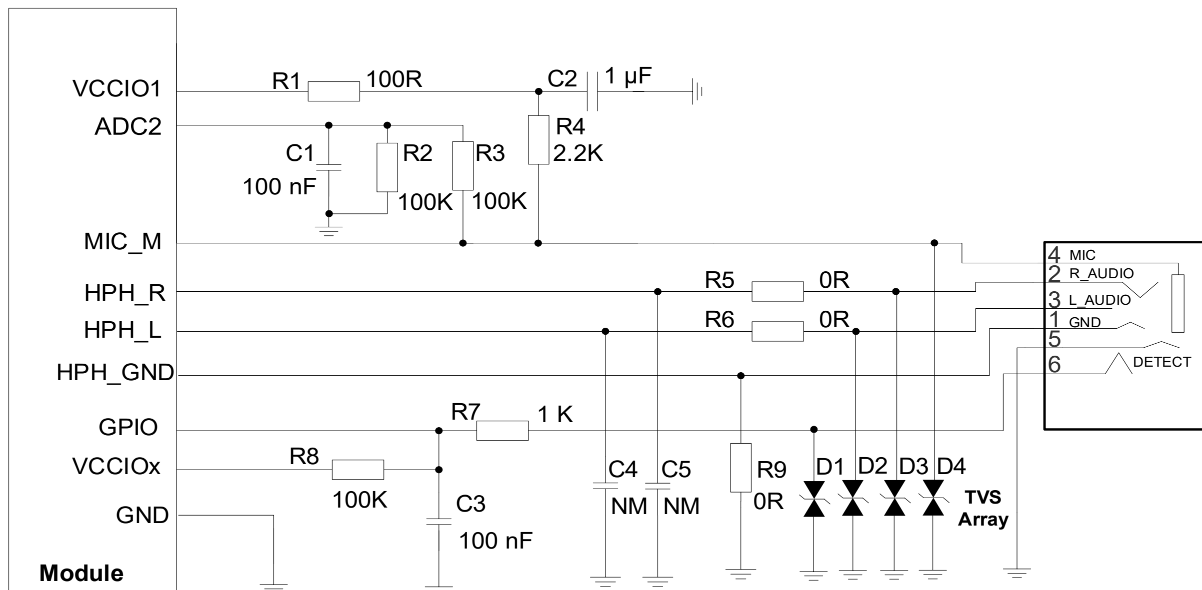


Figure 15: Reference Design of Headset Interface

NOTE

1. ADC2 can be used for headset HOOK function, which is under development.
2. GPIO is used for headset insert detection function. VCCIOx indicates the reference voltage of GPIO. If it is required to support headset insert detection function in a low power consumption state, the GPIO of PMUIO power domain should be selected.
3. HPH_GND needs to be routed separately to the headset socket and connected to GND to reduce the

level difference between the headset GND. Route HPH_GND trace between HPH_R and HPH_L to avoid interference from other signals.
4. HPH_R/HPH_L can be used for LINEOUT function to connect to an external power amplifier. In this scenario, HPH_GND can be connected to ground at the module end.

4.8.3. Loudspeaker Interface Reference Design

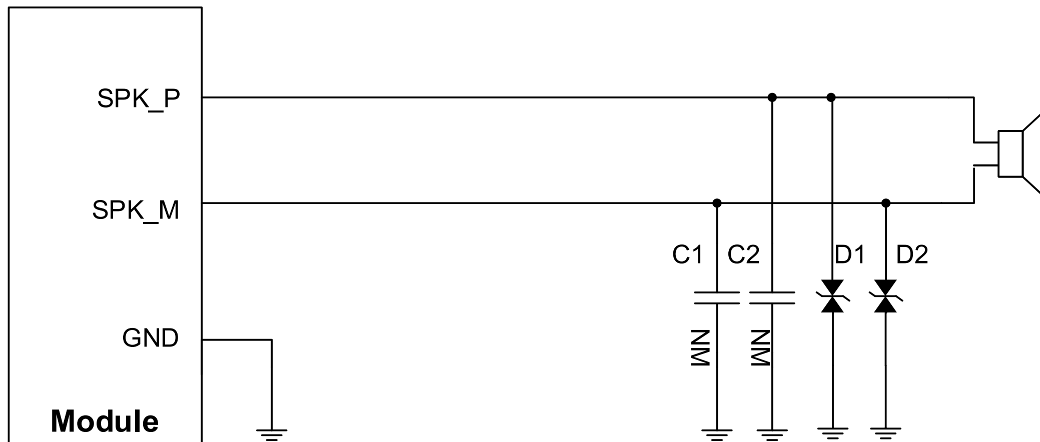


Figure 16: Reference Design of Loudspeaker Interface

NOTE

1. The headset and loudspeaker functions require an external 5 V power supply input, and the power supply input pin is VCC_SPK_HP.
2. The module can provide a maximum driving capacity of 1.3 W @ 8 Ω (5 V power supply). If you need to drive a higher-power speaker, it is recommended to add an power amplifier chip.

4.8.4. Audio Interfaces Design Considerations

The filter capacitor on the PCB should be placed near the audio device or audio interface as close as possible, and the trace should be as short as possible. The filter capacitor should be passed before reaching other connection points.

To decrease signal interferences, RF antennas should be placed away from audio interfaces and audio traces. Power traces and audio traces should not be parallel, and they should be far away from each other.

The differential audio traces must be routed according to the differential signal layout rule.

4.9. ADC Interfaces

The module provides 5 ADC interfaces which support up to 10-bit resolution.

Table 21: Pins Description of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC2	218	AI	General-purpose ADC interface	Input voltage range: 0~1.8 V
ADC4	233	AI	General-purpose ADC interface	
ADC5	228	AI	General-purpose ADC interface	
ADC6	223	AI	General-purpose ADC interface	
ADC7	213	AI	General-purpose ADC interface	

4.10. Video Output Interfaces

The module has a built-in VOP controller and it has three output ports:

- Port 1: Supports HDMI, MIPI DSI0, MIPI DSI1 and eDP video output
- Port 2: Supports HDMI, MIPI DSI0, MIPI DSI1, eDP and LVDS video output
- Port 3: Supports LVDS, RGB*, BT1120*, BT656* video output

Each port only supports one kind of video signal. The module supports triple-screen display and the three screens can support different video signal.

The module supports multiple video display interfaces:

- 1 group of HDMI interface: supports HDMI 2.0, with the maximum output resolution up to 4096 × 2160 @ 60 fps
- 1 group of MIPI DSI0 interface: supports MIPI 1.2, with the maximum output resolution up to 1920 × 1080 @ 60 fps; it can be multiplexed into LVDS interface, with the maximum output resolution up to 1280 × 800 @ 60 fps
- 1 group of MIPI DSI1 interface: supports MIPI 1.2, with the maximum output resolution up to 1920 × 1080 @ 60 fps. MIPI DSI0 and MIPI DIS1 can be combined to support Dual-MIPI, with the maximum output resolution up to 2048 × 1536 @ 60 fps
- 1 group of eDP interface: supports eDP V1.3, with the maximum output resolution up to 2560 × 1600 @ 60 fps

- 1 group of RGB* interface: supports parallel 24 bits RGB output, with the maximum output resolution up to 1920 × 1080 @ 60 fps
- 1 group of BT1120* interface: supports 16 bits BT1120 output, with the maximum output resolution up to 1920 × 1080 @ 60 fps
- 1 group of BT656* interface: supports 8 bits BT656 output

4.10.1. eDP Interface

The module supports eDP V1.3 and supports 1 group of 4-lane eDP interface, with the maximum output resolution up to 2560 × 1600 @ 60 fps.

- Supports data rate: up to 2.7 Gbps/lane
- Supports 1-lane or 2-lane or 4-lane mode
- Supports AUX channel
- Supports data rate up to 1 Mbps

Table 22: Pins Description of eDP Interface

Pin Name	Pin No.	I/O	Description
EDP_ML0_P	136	AO	eDP data 0 (+)
EDP_ML0_N	132	AO	eDP data 0 (-)
EDP_ML1_P	131	AO	eDP data 1 (+)
EDP_ML1_N	127	AO	eDP data 1 (-)
EDP_ML2_P	126	AO	eDP data 2 (+)
EDP_ML2_N	122	AO	eDP data 2 (-)
EDP_ML3_P	121	AO	eDP data 3 (+)
EDP_ML3_N	117	AO	eDP data 3 (-)
EDP_AUX_P	141	AIO	eDP auxiliary channel (+)
EDP_AUX_N	137	AIO	eDP auxiliary channel (-)
EDP_DET	70	DI	eDP hot-plug detect

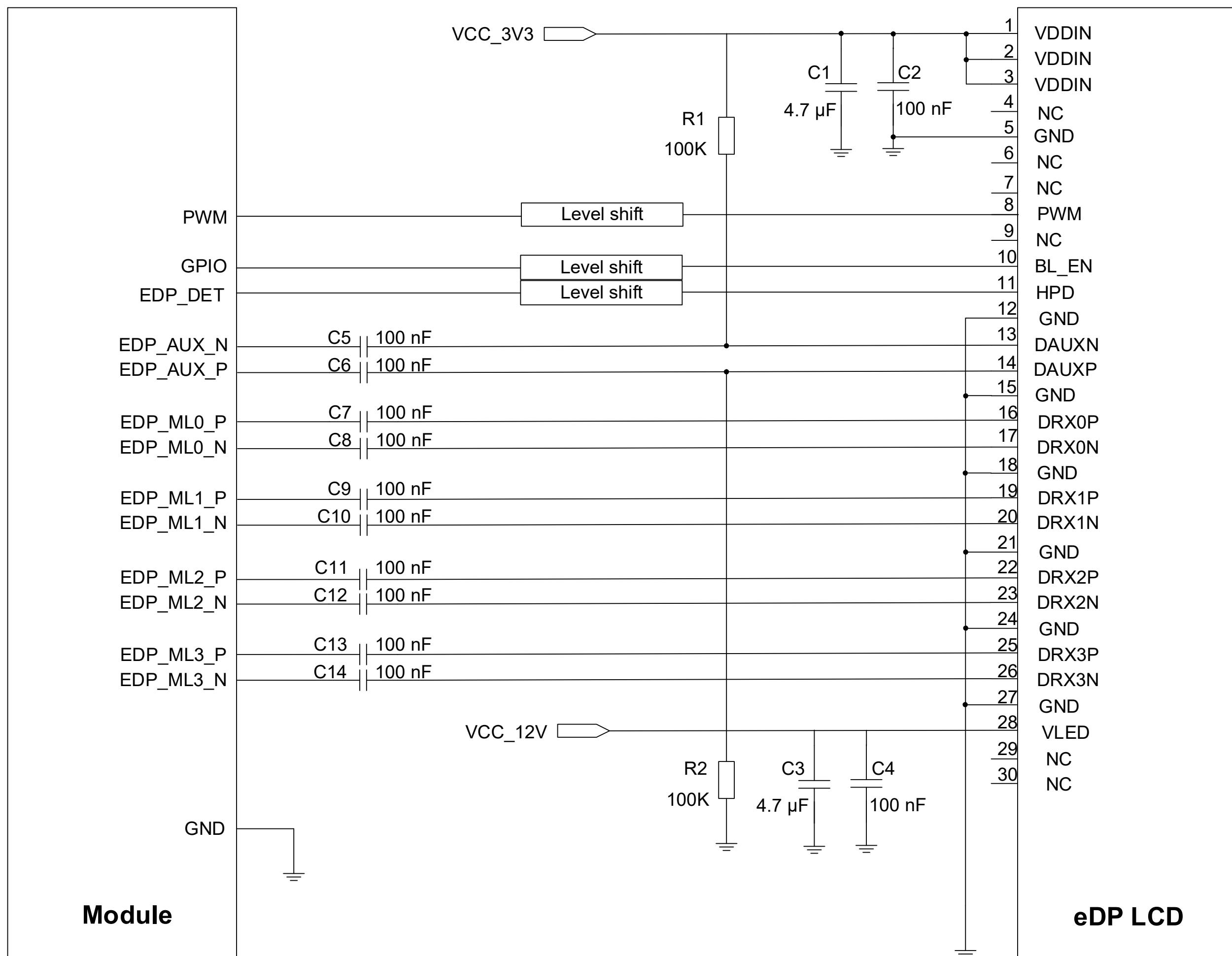


Figure 17: Reference Design of eDP Interface

NOTE

1. Confirm that whether level-shift is needed for PWM, BL_EN, HPD and other signals according to the selected module pins and eDP LCD specifications.
2. For LCDs that support eDP V1.2a and above protocols, R1 and R2 are not mounted.
3. If the eDP LCD has requirements on the power-up timing, the module's GPIO can be selected for timing control.
4. If the application scenario involves frequent plugging and unplugging of the eDP connector or has high requirements for ESD protection, it is recommended to reserve a TVS near the connector, and the TVS junction capacitance should not exceed 0.4 pF.
5. EDP_DET is optional and can be configured as required.

Table 23: eDP Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching (N-P)
EDP_ML0_P	136	33.18	-0.16
EDP_ML0_N	132	33.34	
EDP_ML1_P	131	31.89	-0.03
EDP_ML1_N	127	31.92	
EDP_ML2_P	126	34.51	-0.15
EDP_ML2_N	122	34.66	
EDP_ML3_P	121	31.55	-0.23
EDP_ML3_N	117	31.78	
EDP_AUX_P	141	30.86	-0.08
EDP_AUX_N	137	30.94	

To ensure performance, the following principles should be complied with when designing eDP interface:

- Special attention should be paid to the pin description of eDP interface. Different eDP device will have varied definitions for their corresponding connectors. Ensure that the devices and the connectors are correctly connected.
- eDP are high-speed signal traces, supporting maximum data rate up to 2.7 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB and do not cross it with other traces. To avoid crosstalk, a clearance of 4 times the trace width is recommended among eDP signal traces. During impedance matching, do not connect eDP signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a TVS of low capacitance for ESD protection and the recommended parasitic capacitance should be lower than 0.4 pF.
- Route eDP traces according to the following requirements:
  a) The total trace length should not exceed 150 mm;
  b) Control the differential impedance to 100 Ω ±10 %;
  c) Control intra-lane length matching within 0.3 mm.

4.10.2. HDMI Interface

The module supports HDMI 2.0 and supports 1 group of 3-lane HDMI interface, with the maximum output resolution up to 4096 × 2160 @ 60 fps.

Table 24: Pins Description of HDMI Interface

Pin Name	Pin No.	I/O	Description	Comment
HDMI_TX2_P	72	AO	HDMI data 2 (+)	
HDMI_TX2_M	71	AO	HDMI data 2 (-)	
HDMI_TX1_P	67	AO	HDMI data 1 (+)	
HDMI_TX1_M	66	AO	HDMI data 1 (-)	
HDMI_TX0_P	62	AO	HDMI data 0 (+)	
HDMI_TX0_M	61	AO	HDMI data 0 (-)	
HDMI_CLK_P	57	AO	HDMI clock (+)	
HDMI_CLK_M	56	AO	HDMI clock (-)	
HDMI_DET	379	DI	HDMI hot-plug detect	Active high.
HDMI_SCL	387	OD	HDMI I2C clock	
HDMI_SDA	385	OD	HDMI I2C data	
HDMI_CEC	382	DIO	HDMI CEC signal	

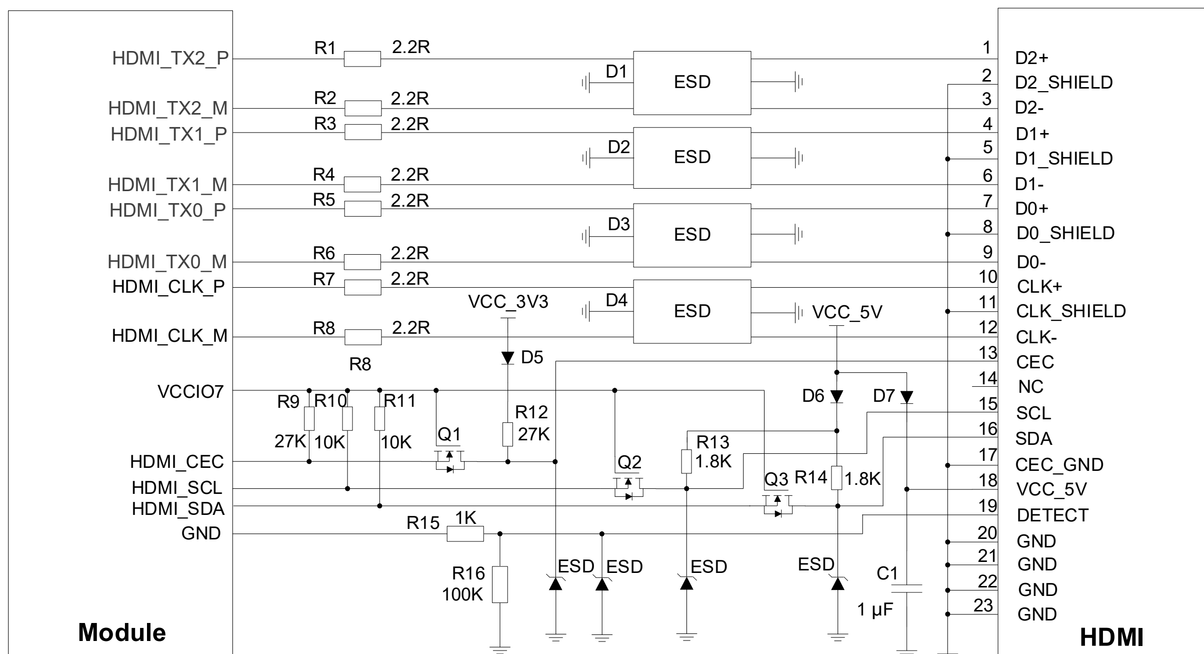


Figure 18: Reference Design of HDMI Interface

NOTE

1. The junction capacitance of D1, D2, D3 and D4 should not exceed 0.4 pF, and that of other ESD protection components should not exceed 1 pF.
2. VCC_3V3 and VCC_5V are provided by the terminal board.
3. D5, D6, and D7 use Schottky diodes.
4. For Q1, Q2, Q3, it is recommended to use 2SK3018.

Table 25: HDMI Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching (P-M)
HDMI_TX2_P	72	20.84	0.2
HDMI_TX2_M	71	20.64	
HDMI_TX1_P	67	19.89	0.25
HDMI_TX1_M	66	19.64	
HDMI_TX0_P	62	18.77	0.22
HDMI_TX0_M	61	18.55	
HDMI_CLK_P	57	18.06	0.27
HDMI_CLK_M	56	17.79	

To ensure performance, the following principles should be complied with when designing HDMI interface:

- Special attention should be paid to the pin description of HDMI interface. Different HDMI device will have varied definitions for their corresponding connectors. Ensure that the devices and the connectors are correctly connected.
- HDMI are high-speed signal traces, supporting maximum data rate up to 6 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB and do not cross it with other traces. To avoid crosstalk, a clearance of 4 times the trace width among HDMI data signal traces and a clearance of 5 times the trace width between HDMI data signal traces and clock signal traces are recommended. During impedance matching, do not connect HDMI signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a TVS of low capacitance for ESD protection and the recommended parasitic capacitance on HDMI data and clock signals should be lower than 0.4 pF and lower than 1 pF on other HDMI signals.
- Route HDMI traces according to the following requirements:
  a) The total trace length should not exceed 150 mm;

b) Control the differential impedance to 100 Ω ±10 %;
c) Control intra-lane length matching within 0.3 mm.
d) Control the length matching between clock signal traces and data signals traces within 12 mm.

4.10.3. LCM Interfaces

Table 26: Pins Description of LCM Interfaces

Pin Name	Pin No.	I/O	Description
LCD1_RST	322	DO	LCD1 reset
DSI0_CLK_N	37	AO	LCD0 MIPI clock (-)
DSI0_CLK_P	36	AO	LCD0 MIPI clock (+)
DSI0_LN0_N	47	AO	LCD0 MIPI lane 0 data (-)
DSI0_LN0_P	46	AO	LCD0 MIPI lane 0 data (+)
DSI0_LN1_N	42	AO	LCD0 MIPI lane 1 data (-)
DSI0_LN1_P	41	AO	LCD0 MIPI lane 1 data (+)
DSI0_LN2_N	32	AO	LCD0 MIPI lane 2 data (-)
DSI0_LN2_P	31	AO	LCD0 MIPI lane 2 data (+)
DSI0_LN3_N	27	AO	LCD0 MIPI lane 3 data (-)
DSI0_LN3_P	26	AO	LCD0 MIPI lane 3 data (+)
DSI1_CLK_N	33	AO	LCD1 MIPI clock (-)
DSI1_CLK_P	29	AO	LCD1 MIPI clock (+)
DSI1_LN0_N	43	AO	LCD1 MIPI lane 0 data (-)
DSI1_LN0_P	39	AO	LCD1 MIPI lane 0 data (+)
DSI1_LN1_N	38	AO	LCD1 MIPI lane 1 data (-)
DSI1_LN1_P	34	AO	LCD1 MIPI lane 1 data (+)
DSI1_LN2_N	28	AO	LCD1 MIPI lane 2 data (-)
DSI1_LN2_P	24	AO	LCD1 MIPI lane 2 data (+)

DSI1_LN3_N	23	AO	LCD1 MIPI lane 3 data (-)
DSI1_LN3_P	19	AO	LCD1 MIPI lane 3 data (+)

NOTE

LVDS is multiplexed from DSI0. For the detailed multiplexing relationship, see ***document [2]***.

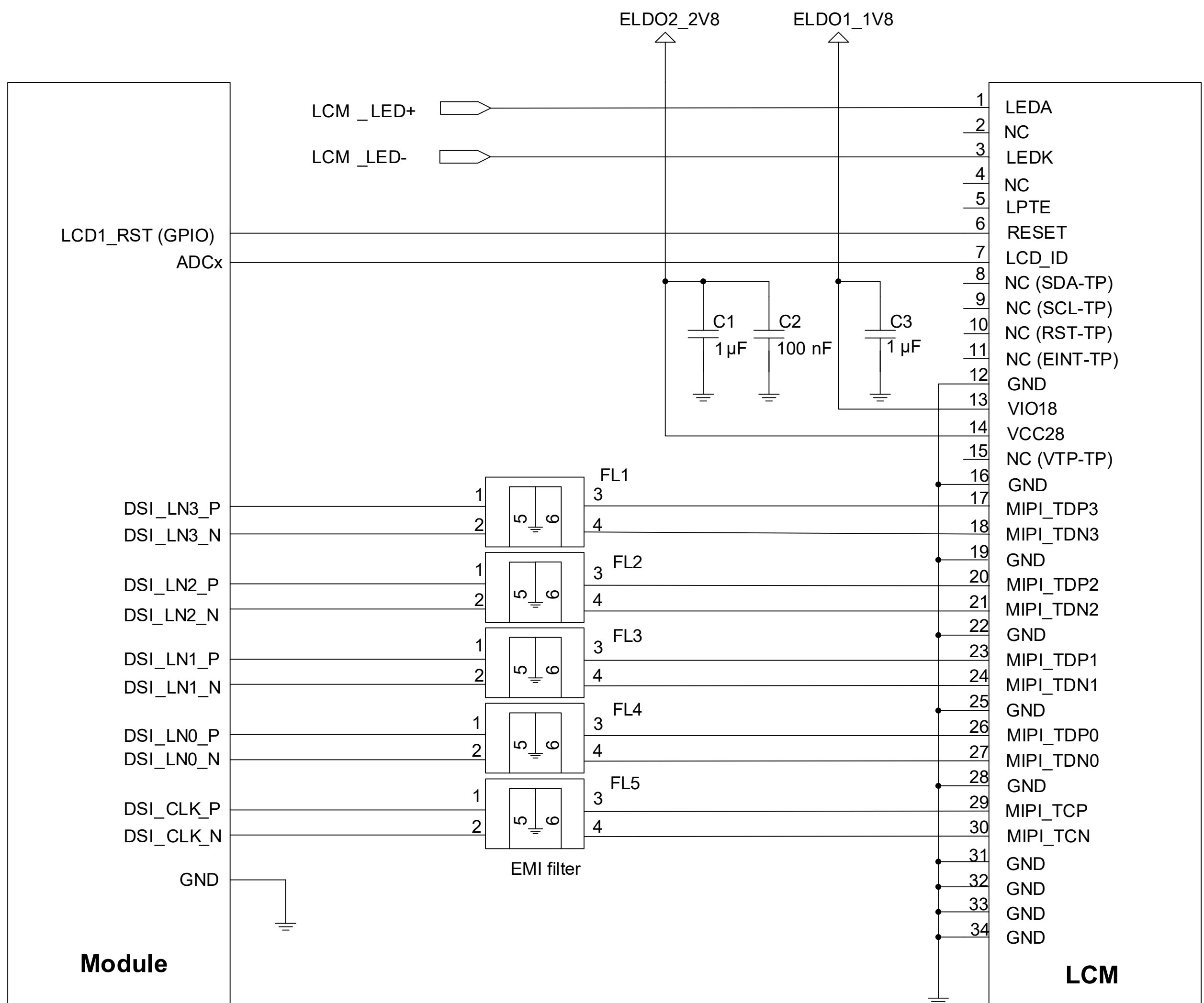


Figure 19: Reference Design of LCM Interface

NOTE

The power supply of VIO18 can be either external ELDO1_1V8 or LDO9_1V8 of the module.

MIPI are high-speed signal traces. It is recommended to add common-mode chokes in series near the LCM connector to reduce electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that LCM factory burn an OTP register to distinguish different screens. You can also connect the LCD_ID of LCM to the ADC of the module to distinguish different screens by level detection. But note that the output voltage of LCD_ID should not exceed the voltage range of the ADC.

You can design an external backlight drive circuit for LCM according to actual requirement. PWM can be used for backlight brightness adjustment.

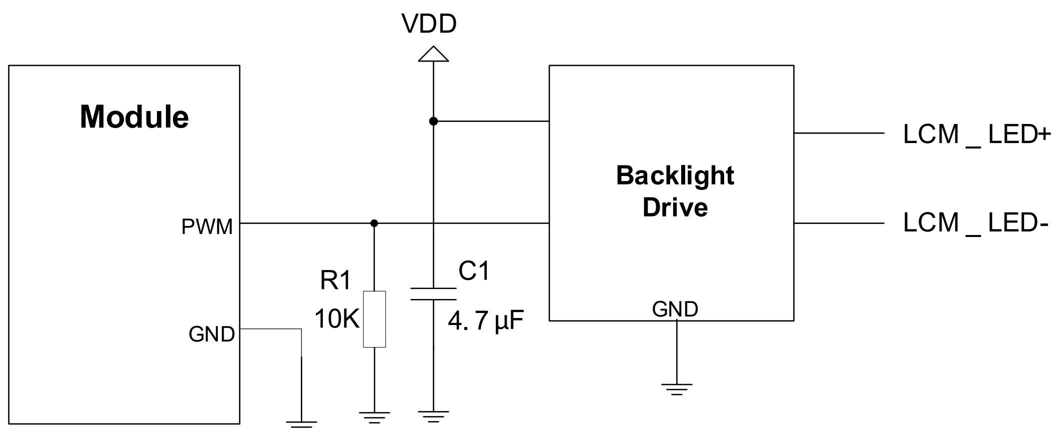


Figure 20: Reference Design of LCM Interface External Backlight Drive

For more details about the principles when designing LCM interfaces, see ***Chapter 4.11.1***.

4.11. Camera Interface

Based on MIPI CSI standard, the module supports 1 camera (4-lane) or 2 cameras (2-lane + 2-lane). The maximum pixel of the camera is up to 8 MP. The video and photo quality are determined by various factors such as the camera sensor, camera lens specifications, etc.

Table 27: Pins Description of Camera Interface

Pin Name	Pin No.	I/O	Description
CSI_CLK0_N	2	AI	MIPI CSI clock 0 (-)
CSI_CLK0_P	3	AI	MIPI CSI clock 0 (+)

CSI_CLK1_N	6	AI	MIPI CSI clock 1 (-)
CSI_CLK1_P	9	AI	MIPI CSI clock 1 (+)
CSI_LN0_N	7	AI	MIPI CSI lane 0 data (-)
CSI_LN0_P	8	AI	MIPI CSI lane 0 data (+)
CSI_LN1_N	4	AI	MIPI CSI lane 1 data (-)
CSI_LN1_P	5	AI	MIPI CSI lane 1 data (+)
CSI_LN2_N	16	AI	MIPI CSI lane 2 data (-)
CSI_LN2_P	17	AI	MIPI CSI lane 2 data (+)
CSI_LN3_N	11	AI	MIPI CSI lane 3 data (-)
CSI_LN3_P	12	AI	MIPI CSI lane 3 data (+)
CAM0_MCLK	279	DO	Master clock of camera 0
CAM0_RST	317	DO	Reset of camera 0
CAM0_PWDN	316	DO	Power down of camera 0
CAM1_MCLK	75	DO	Master clock of camera 1
CAM1_RST	314	DO	Reset of camera 1
CAM1_PWDN	313	DO	Power down of camera 1

The following is a reference design of one-camera application:

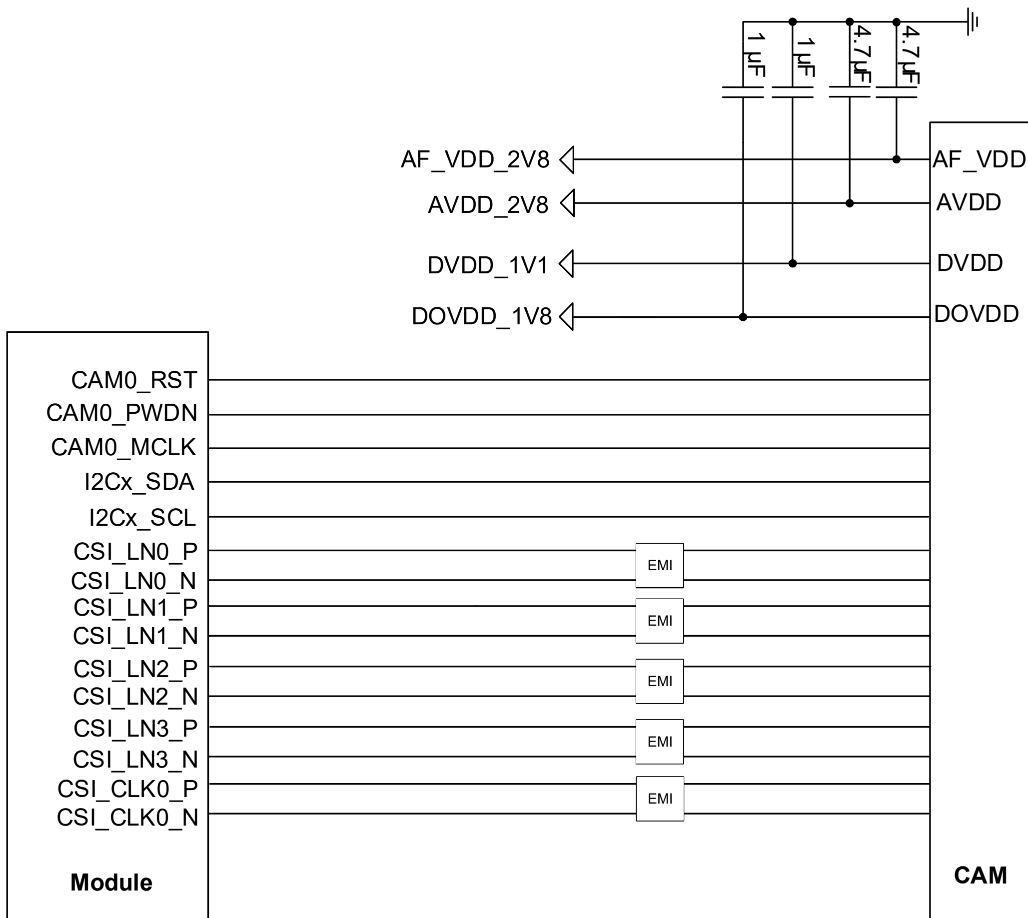


Figure 21: Reference Design of One-Camera Application

The following is a reference design of dual-camera application:

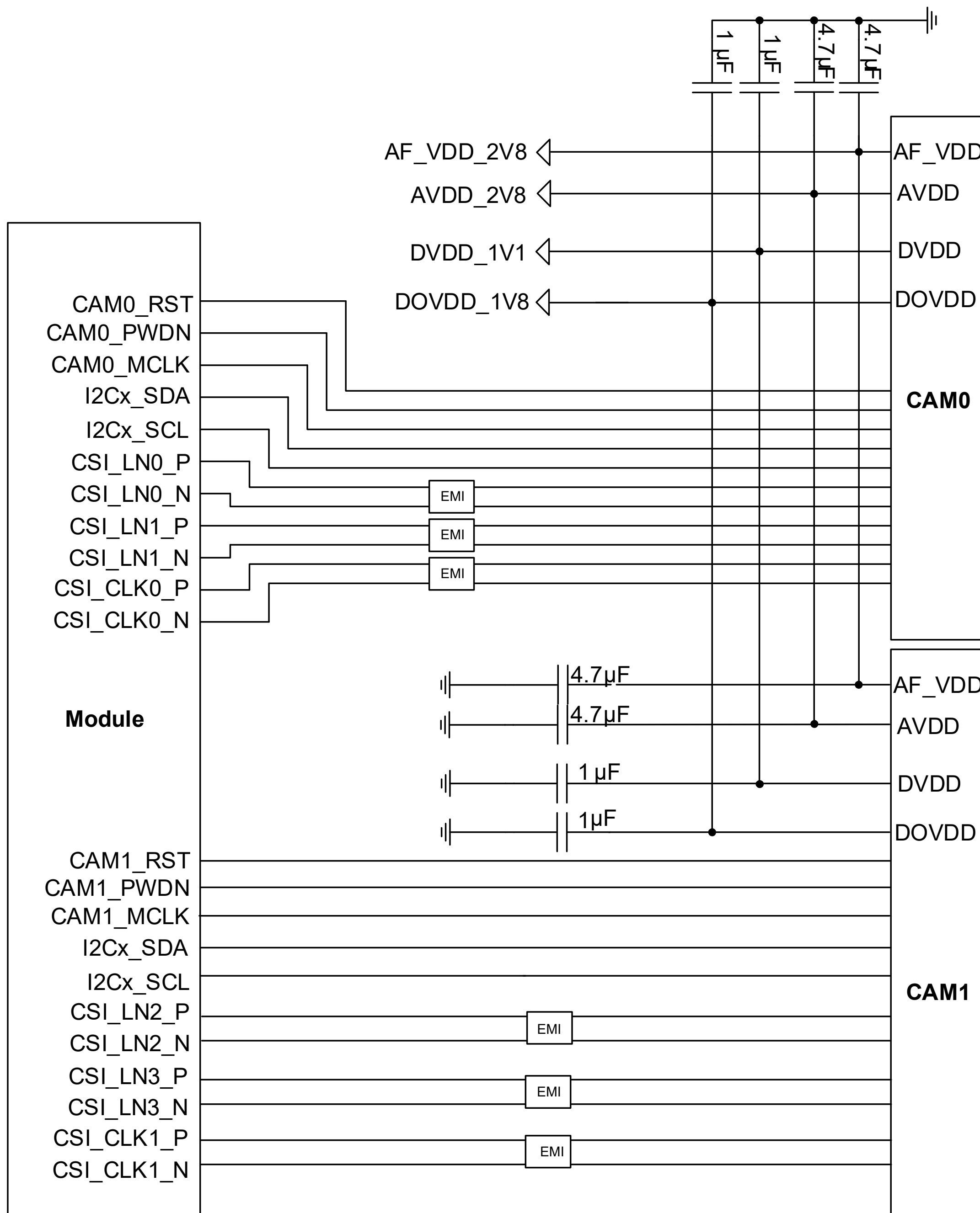


Figure 22: Reference Design of Dual-Camera Application

NOTE

1. When the I2C addresses of the two cameras are different, they can be connected to the same I2C interface.
2. The module's ISP supports up to 8 MP camera input.
3. EMI devices should be placed near the camera.

4. AVDD, AF_VDD, DVDD, and DOVDD must be provided by the terminal board. If the camera has power supply timing requirements, the timing control can be performed through the module's GPIO.
5. The power domain of CAM1_MCLK is 3.3 V. If it does not match with the camera's power domain, the level-shift is required.

4.11.1. MIPI Design Considerations

To ensure performance, the following principles should be complied with when designing LCM and camera interfaces:

- Special attention should be paid to the pin description of LCM and camera interfaces. Different video devices will have varied definitions for their corresponding connectors. Ensure that the devices and the connectors are correctly connected.
- MIPI are high-speed signal traces, supporting maximum data rate up to 2.5 Gbps. The differential impedance should be controlled to 100 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB and do not cross it with other traces. For the same video device, keep all the MIPI traces be of the same length. To avoid crosstalk, a clearance of 3 times the trace width is recommended among MIPI signal traces. During impedance matching, do not connect MIPI signal traces to GND on different planes to ensure impedance consistency.
- It is recommended to select a TVS of low capacitance for ESD protection and the recommended parasitic capacitance should be lower than 1 pF.
- Route MIPI traces according to the following requirements:
  a) The total trace length should not exceed 150 mm;
  b) Control the differential impedance to 100 Ω ±10 %;
  c) Control intra-lane length matching within 0.3 mm;
  d) Control inter-lane length matching within 0.9 mm.

Table 28: MIPI Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching (N-P)
CSI_CLK0_N	2	19.59	-0.03
CSI_CLK0_P	3	19.62	
CSI_CLK1_N	6	14.00	-0.07
CSI_CLK1_P	9	14.07	
CSI_LN0_N	7	17.27	0.2
CSI_LN0_P	8	17.07	
CSI_LN1_N	4	18.30	0

CSI_LN1_P	5	18.30	
CSI_LN2_N	16	15.42	0.06
CSI_LN2_P	17	15.36	
CSI_LN3_N	11	15.74	0.27
CSI_LN3_P	12	15.47	
DSI0_CLK_N	37	13.68	0.14
DSI0_CLK_P	36	13.54	
DSI0_LN0_N	47	14.91	0.23
DSI0_LN0_P	46	14.68	
DSI0_LN1_N	42	13.99	0.01
DSI0_LN1_P	41	13.98	
DSI0_LN2_N	32	14.15	0.23
DSI0_LN2_P	31	13.92	
DSI0_LN3_N	27	14.69	0.19
DSI0_LN3_P	26	14.50	
DSI1_CLK_N	33	9.24	0
DSI1_CLK_P	29	9.24	
DSI1_LN0_N	43	11.08	0.15
DSI1_LN0_P	39	10.93	
DSI1_LN1_N	38	10.46	0.06
DSI1_LN1_P	34	10.40	
DSI1_LN2_N	28	9.33	0.24
DSI1_LN2_P	24	9.09	
DSI1_LN3_N	23	9.79	0.13
DSI1_LN3_P	19	9.66	

4.12. Touch Panel Interface

The module provides 1 I2C interface for connection with Touch Panel (TP) by default, and provides the corresponding power supply and interrupt pins.

Table 29: Pins Description of Touch Panel Interface

Pin Name	Pin No.	I/O	Description
TP_RST	30	DO	TP reset
TP_INT	35	DI	TP interrupt
TP_I2C1_SCL	45	OD	TP I2C clock
TP_I2C1_SDA	40	OD	TP I2C data

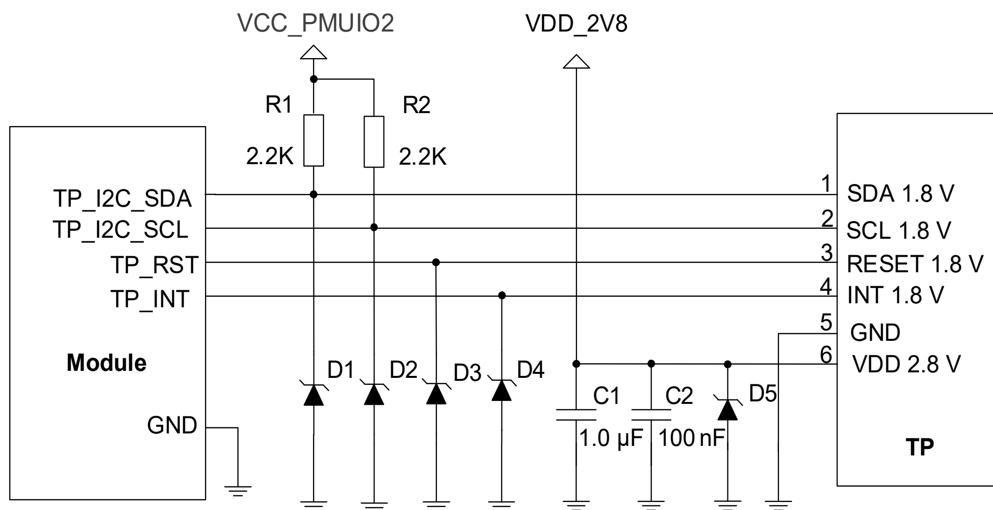


Figure 23: Reference Design of Touch Panel Interface

4.13. PCIe Interfaces

The module provides 2 PCIe interfaces.

PCIe1 interface:

- 1 group of 1-lane PCIe 2.0 interface
- Only supports RC mode
- PCIE1_REFCLK_P/M can support both output and input, but they output clock signals for EP device by default.
- PCIe1 data channel can be multiplexed into SATA2 or QSGMII/SGMII* interface. For detailed multiplexing relationship, see ***document [2]***.

PCIe2 Interface:

- 1 group of 2-lane PCIe 3.0 interface
- Supports PCIe 3.0 × 2 lane RC mode, compatible with PCIe 3.0 × 1 lane RC mode;
  PCIe 3.0 × 1 lane RC mode uses PCIE2_TX0_P/M, PCIE2_RX0_P/M channel
- Supports PCIe 3.0 × 2 lane EP mode, compatible with PCIe 3.0 × 1 lane EP mode;
  PCIe 3.0 × 1 lane EP mode uses PCIE2_TX0_P/M, PCIE2_RX0_P/M channel
- Supports PCIe 3.0 × 1 lane RC mode + PCIe 3.0 × 1 lane RC mode
- PCIE2_REFCLK_P/M only support input:
  Need to provide HCSL level clock input;
  Must meet the requirements for PCIe 3.0 clock.

Table 30: Pins Description of PCIe Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIE1_TX_P	90	AO	PCIe1 transmit (+)	
PCIE1_TX_M	91	AO	PCIe1 transmit (-)	
PCIE1_RX_P	86	AI	PCIe1 receive (+)	
PCIE1_RX_M	87	AI	PCIe1 receive (-)	
PCIE1_REFCLK_P	81	AO	PCIe1 reference clock (+)	
PCIE1_REFCLK_M	82	AO	PCIe1 reference clock (-)	
PCIE1_CLKREQ_N	366	DI	PCIe1 clock request	
PCIE1_WAKE_N	367	DI	PCIe1 wake up	
PCIE1_RST_N	333	DO	PCIe1 reset	
PCIE2_TX0_P	58	AO	PCIe2 transmit 0 (+)	
PCIE2_TX0_M	54	AO	PCIe2 transmit 0 (-)	
PCIE2_TX1_P	63	AO	PCIe2 transmit 1 (+)	

PCIE2_TX1_M	59	AO	PCIe2 transmit 1 (-)	
PCIE2_RX0_P	68	AI	PCIe2 receive 0 (+)	
PCIE2_RX0_M	64	AI	PCIe2 receive 0 (-)	
PCIE2_RX1_P	73	AI	PCIe2 receive 1 (+)	
PCIE2_RX1_M	69	AI	PCIe2 receive 1 (-)	
PCIE2_REFCLK_P	53	AI	PCIe2 reference clock (+)	If unused, connect this pin to ground.
PCIE2_REFCLK_M	49	AI	PCIe2 reference clock (-)	If unused, connect this pin to ground.
PCIE2_CLKREQ0_N	364	DIO	PCIe2 channel 0 clock request	When PCIe2 is configured in PCIe × 2 lane mode, this pin is used for clock request function.
PCIE2_WAKE0_N	363	DIO	PCIe2 channel 0 wake up	When PCIe2 is configured in PCIe × 2 lane mode, this pin is used for wake up function.
PCIE2_RST0_N	362	DIO	PCIe2 channel 0 reset	When PCIe2 is configured in PCIe × 2 lane mode, this pin is used for reset function.
PCIE2_CLKREQ1_N	368	DI	PCIe2 channel 1 clock request	
PCIE2_WAKE1_N	369	DI	PCIe2 channel 1 wake up	
PCIE2_RST1_N	358	DO	PCIe2 channel 1 reset	

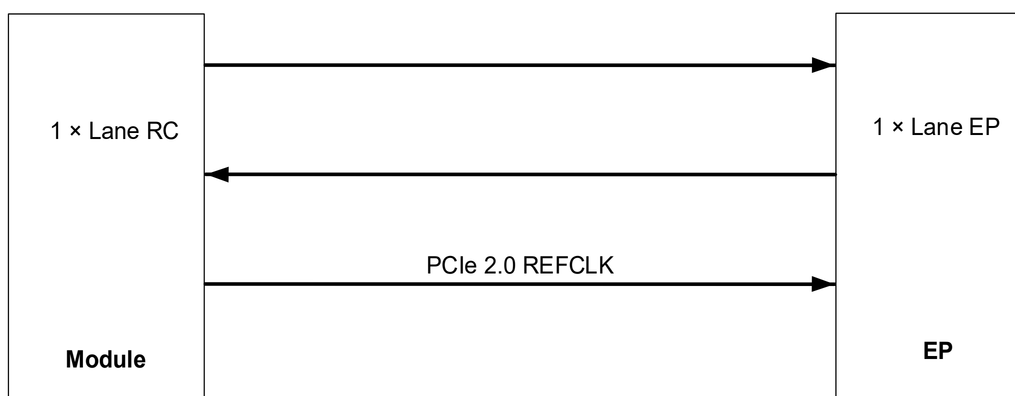


Figure 24: Schematic Diagram of PCIe1 Interface

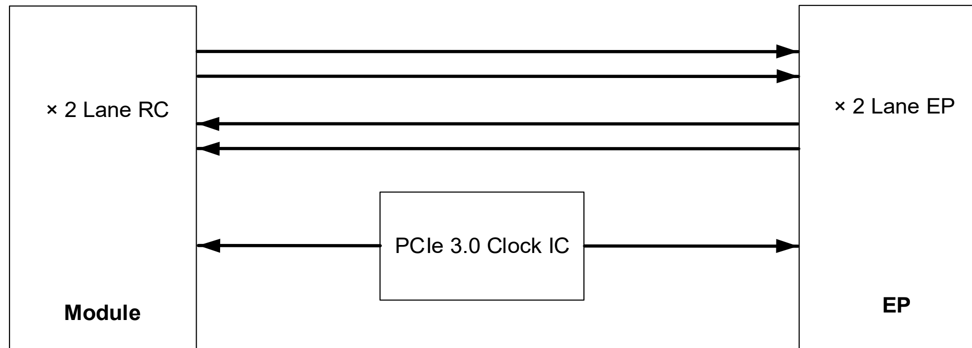


Figure 25: Schematic Diagram of 2 Lane RC Mode of PCIe2 Interface

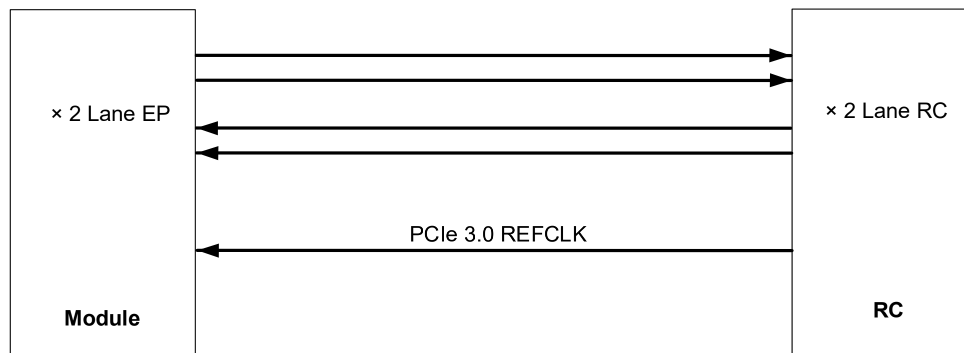


Figure 26: Schematic Diagram of 2 Lane EP Mode of PCIe2 Interface

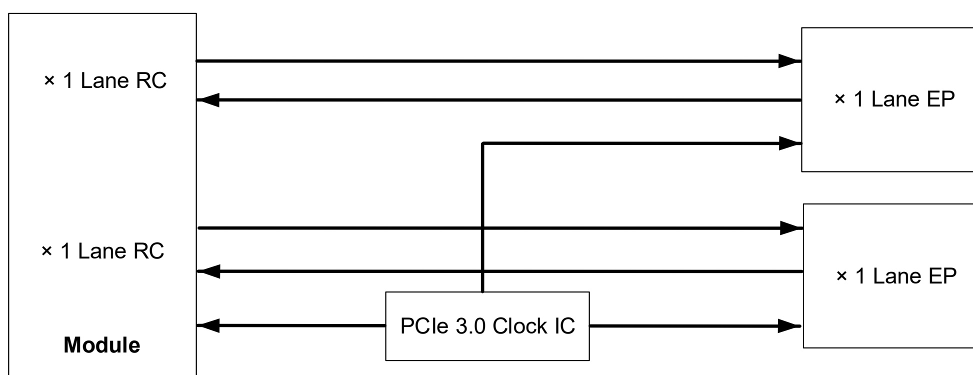


Figure 27: Schematic Diagram of 1 Lane RC + 1 Lane RC Mode of PCIe2 Interface

NOTE

1. 100 nF AC coupling capacitors are connected in series on the PCIe 2.0 data traces, and 220 nF AC coupling capacitors are connected in series on the PCIe 3.0 data traces.
2. When PCIe2 uses × 2 lane mode or × 1 lane mode, control signals are PCIE2_CLKREQ0_N, PCIE2_WAKE0_N and PCIE2_RST0_N.
3. When PCIe2 uses × 1 lane mode + × 1 lane mode, channel 0 control signals are PCIE2_CLKREQ0_N, PCIE2_WAKE0_N and PCIE2_RST0_N; channel 1 control signals are PCIE2_CLKREQ1_N, PCIE2_WAKE1_N and PCIE2_RST1_N.
4. The impedance of the PCIe 2.0 data traces is controlled to 90 Ω, and the impedance of the PCIe 3.0 data traces is controlled to 85 Ω.
5. The impedance of the PCIe reference clock traces is controlled to 100 Ω.
6. For detailed signal connection, refer to ***document [3]***.

To ensure performance, the following principles should be complied with when designing PCIe interfaces:

- PCIe are high-speed signal traces, supporting maximum data rate up to 2.5 Gbps for PCIe 2.0 and the differential impedance should be controlled to 90 Ω. The maximum data rate is up to 4 Gbps for PCIe 3.0 and the differential impedance should be controlled to 85 Ω. Additionally, it is recommended to route the traces on the inner layer of PCB and do not cross it with other traces. To avoid crosstalk, a clearance of 4 times the trace width among PCIe 2.0 signal traces and a clearance of 5 times the trace width among PCIe 3.0 signal traces are recommended. During impedance matching, do not connect PCIe signal traces to GND on different planes to ensure impedance consistency.
- Route PCIe traces according to the following requirements:
  a) The total trace length should not exceed 150 mm;
  b) Control the differential impedance of data traces and reference clock traces according to requirements and the deviation is at most 10 %;
  c) Control intra-lane length matching within 0.3 mm.

Table 31: PCIe Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length	Length Matching (P-M)
PCIE1_TX_P	90	25.20	-0.07
PCIE1_TX_M	91	25.27	
PCIE1_RX_P	86	22.63	0.05
PCIE1_RX_M	87	22.58	
PCIE1_REFCLK_P	81	23.13	-0.18

PCIE1_REFCLK_M	82	23.31	
PCIE2_TX0_P	58	14.43	-0.19
PCIE2_TX0_M	54	14.62	
PCIE2_TX1_P	63	13.07	0.20
PCIE2_TX1_M	59	12.87	
PCIE2_RX0_P	68	15.30	-0.21
PCIE2_RX0_M	64	15.51	
PCIE2_RX1_P	73	18.28	0.15
PCIE2_RX1_M	69	18.13	
PCIE2_REFCLK_P	53	13.41	0.17
PCIE2_REFCLK_M	49	13.24	

4.14. RGMII Interfaces

The module has two built-in Gigabit MAC (GMAC0 + GMAC1) controllers, and supports up to two external 10/100/1000 Mbps network ports.

The dual network port solution of the SG368Z-AP module:

- RGMII0 (GMAC0) + RGMII1 (GMAC1) respectively connected to an Ethernet PHY
- RGMII0 (GMAC0) externally connected to an Ethernet PHY + multiplexed SGMII (GMAC1) externally connected to an Ethernet PHY
- RGMII1 (GMAC1) externally connected to an Ethernet PHY + multiplexed SGMII (GMAC0) externally connected to an Ethernet PHY
- Multiplexed QSGMII (GMAC0 + GMAC1) externally connected a 4-port Ethernet PHY (the module only supports 2 ports)

The dual network port solution of the SG368Z-WF module:

- Multiplexed QSGMII (GMAC0 + GMAC1) externally connected a 4-port Ethernet PHY (the module only supports 2 ports)

Table 32: Pins Description of RGMII Interfaces

Pin Name	Pin No.	I/O	Description	Comment
RGMII0_RX0	183	DI	RGMII0 receive data bit 0	Only SG368Z-AP supports this pin.
RGMII0_RX1	179	DI	RGMII0 receive data bit 1	
RGMII0_RX2	174	DI	RGMII0 receive data bit 2	Only SG368Z-AP supports this pin.
RGMII0_RX3	169	DI	RGMII0 receive data bit 3	Only SG368Z-AP supports this pin.
RGMII0_RX_CTL	175	DI	RGMII0 receive control	
RGMII0_RX_CLK	164	DI	RGMII0 receive clock	Only SG368Z-AP supports this pin.
RGMII0_TX0	168	DO	RGMII0 transmit data bit 0	Only SG368Z-AP supports this pin.
RGMII0_TX1	173	DO	RGMII0 transmit data bit 1	Only SG368Z-AP supports this pin.
RGMII0_TX2	178	DO	RGMII0 transmit data bit 2	Only SG368Z-AP supports this pin.
RGMII0_TX3	182	DO	RGMII0 transmit data bit 3	Only SG368Z-AP supports this pin.
RGMII0_TX_CTL	172	DO	RGMII0 transmit control	Only SG368Z-AP supports this pin.
RGMII0_TX_CLK	163	DO	RGMII0 transmit clock	Only SG368Z-AP supports this pin.
RGMII0_MDC	181	DO	RGMII0 management data clock	Only SG368Z-AP supports this pin.
RGMII0_MDIO	185	OD	RGMII0 management data input/output	Only SG368Z-AP supports this pin.
RGMII0_ REFCLKOUT	160	DO	RGMII0 reference clock output	The output frequency of reference clock is 25 MHz.
RGMII0_MCLK	177	DI	RGMII0 clock input	The output frequency of reference clock is 125 MHz; Only SG368Z-AP supports this pin.
RGMII1_RX0	296	DI	RGMII1 receive data bit 0	
RGMII1_RX1	294	DI	RGMII1 receive data bit 1	
RGMII1_RX2	308	DI	RGMII1 receive data bit 2	

RGMII1_RX3	307	DI	RGMII1 receive data bit 3	
RGMII1_RX_CTL	293	DI	RGMII1 receive control	
RGMII1_RX_CLK	304	DI	RGMII1 receive clock	
RGMII1_TX0	305	DO	RGMII1 transmit data bit 0	
RGMII1_TX1	303	DO	RGMII1 transmit data bit 1	
RGMII1_TX2	312	DO	RGMII1 transmit data bit 2	
RGMII1_TX3	310	DO	RGMII1 transmit data bit 3	
RGMII1_TX_CTL	298	DO	RGMII1 transmit control	
RGMII1_TX_CLK	306	DO	RGMII1 transmit clock	
RGMII1_MDC	290	DO	RGMII1 management data clock	
RGMII1_MDIO	286	OD	RGMII1 management data input/output	
RGMII1_ REFCLKOUT	288	DO	RGMII1 reference clock output	The output frequency of reference clock is 25 MHz.
RGMII1_MCLK	278	DI	RGMII1 clock input	The output frequency of reference clock is 125 MHz.

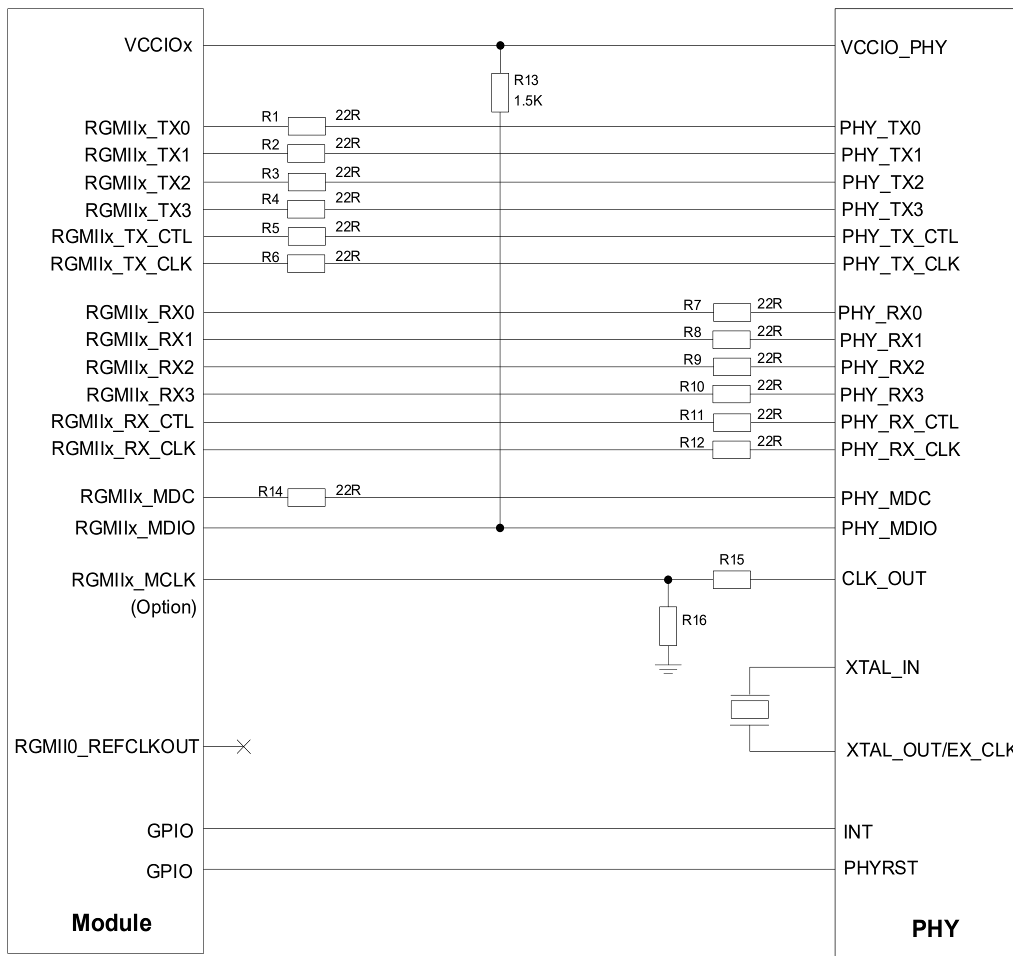


Figure 28: Reference Design of RGMII Interface PHY with External Crystal

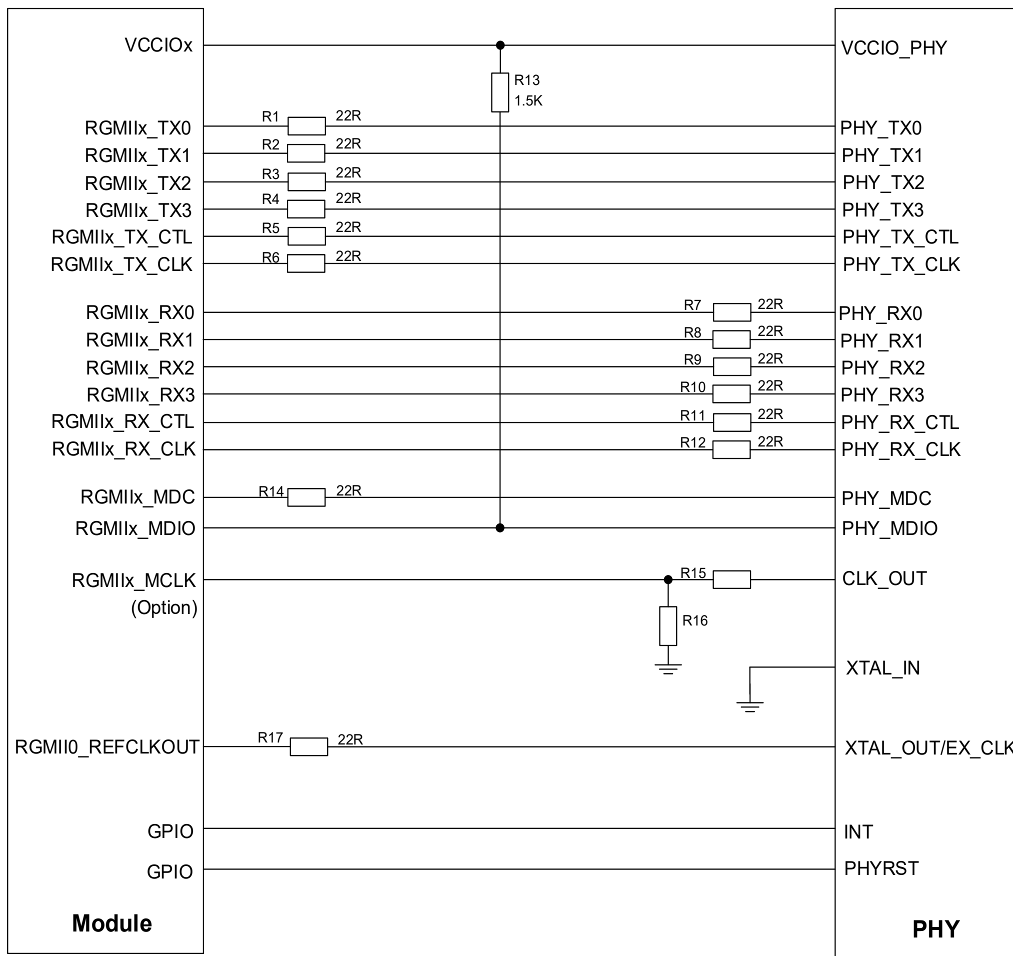


Figure 29: Reference Design of RGMII Interface PHY with Module's 25 MHz Clock

NOTE

1. SG368Z-AP supports RGMII0 and RGMII1 interfaces, while SG368Z-WF only supports RGMII1 interface. RGMII0 uses GMAC0 controller and RGMII1 uses GMAC1 controller.
2. The power domain of RGMII interface is 1.8 V. Please pay attention to level matching with the voltage of the PHY.
3. RGMII_MCLK is an optional function and can be left unconnected.
4. For the design of PHY end, please refer to the reference design of the PHY chip. The designs above are for reference only.
5. If you choose the multiplexed SGMII interface, the used MDC/MDIO needs to match the GMACx used, that is, if SGMII uses GMAC0, select RGMII0_MDC/RGMII0_MDIO, and if SGMII uses GMAC1, select RGMII1_MDC/RGMII1_MDIO.
6. If you choose the multiplexed QSGMII interface, you can choose RGMII0_MDC/RGMII0_MDIO or RGMII1_MDC/RGMII1_MDIO for MDC/MDIO functions.

RGMII_TX and RGMII_RX are all high-speed signal traces. In PCB design, control the characteristic impedance of these traces as 50 Ω, shield them and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB and keep their lengths the same. Additionally, RGMII_RX_CLK, RGMII_TX_CLK, RGMII_MCLK and RGMII_REFCLKOUT need separate ground shielding.

Layout guidelines:

- Control the differential impedance to 50 Ω ±10 % and shield them.
- The trace length difference among RGMII_TX0, RGMII_TX1, RGMII_TX2, RGMII_TX3, RGMII_TX_CTL and RGMII_TX_CLK should not exceed 3 mm.
- The trace length difference among RGMII_RX0, RGMII_RX1, RGMII_RX2, RGMII_RX3, RGMII_RX_CTL and RGMII_RX_CLK should not exceed 3 mm.
- The total trace length of each RGMII signal should not exceed 125 mm.
- Clearance between RGMII signal traces should be greater than or equal to 2 times the trace width and the clearance between RGMII signal traces and other signal traces should be greater than or equal to 3 times the trace width.

Table 33: RGMII Interface Trace Length Inside the Module (Unit: mm)

Pin Name	Pin No.	Length (mm)
RGMII0_RX0	183	36.09
RGMII0_RX1	179	35.98
RGMII0_RX2	174	33.79
RGMII0_RX3	169	30.34
RGMII0_RX_CTL	175	32.16
RGMII0_RX_CLK	164	29.21
RGMII0_TX0	168	34.48
RGMII0_TX1	173	33.93
RGMII0_TX2	178	35.60
RGMII0_TX3	182	35.37
RGMII0_TX_CTL	172	54.48
RGMII0_TX_CLK	163	29.78

RGMII1_RX0	296	56.84
RGMII1_RX1	294	56.26
RGMII1_RX2	308	56.87
RGMII1_RX3	307	57.30
RGMII1_RX_CTL	293	56.84
RGMII1_RX_CLK	304	56.02
RGMII1_TX0	305	43.33
RGMII1_TX1	303	43.90
RGMII1_TX2	312	42.52
RGMII1_TX3	310	42.21
RGMII1_TX_CTL	298	45.08
RGMII1_TX_CLK	306	43.29

4.15. GPIO

SG368Z-WF supports up to 107 GPIOs and SG368Z-AP supports up to 128 GPIOs. The reference voltages of these GPIOs refer to the corresponding power domain. For the multiplexed GPIO, see ***document [2]***.

Table 34: Pins Description of GPIO

Pin Name	Pin No.	I/O	Description	Comment
GPIO0_D3	125	DIO	General-purpose input/output	
GPIO0_D4	60	DIO	General-purpose input/output	
GPIO0_D5	80	DIO	General-purpose input/output	
GPIO0_D6	10	DIO	General-purpose input/output	
GPIO0_A5	123	DIO	General-purpose input/output	

GPIO0_B0	225	DIO	General-purpose input/output	Only SG368Z-AP supports this pin.
GPIO0_B7	220	DIO	General-purpose input/output	Only SG368Z-AP supports this pin.
GPIO0_C0	215	DIO	General-purpose input/output	Only SG368Z-AP supports this pin.
GPIO0_C1	50	DIO	General-purpose input/output	Only SG368Z-AP supports this pin.
GPIO0_C4	25	DIO	General-purpose input/output	
GPIO0_C5	210	DIO	General-purpose input/output	Only SG368Z-AP supports this pin.
GPIO0_C6	370	DIO	General-purpose input/output	
GPIO0_C7	209	DIO	General-purpose input/output	Only SG368Z-AP supports this pin.
GPIO1_D0	276	DIO	General-purpose input/output	
GPIO1_D1	267	DIO	General-purpose input/output	
GPIO1_D2	272	DIO	General-purpose input/output	
GPIO1_D3	281	DIO	General-purpose input/output	
GPIO1_D4	277	DIO	General-purpose input/output	
GPIO2_C5	170	DIO	General-purpose input/output	Only SG368Z-AP supports this pin.
GPIO3_A2	359	DIO	General-purpose input/output	
GPIO3_A3	354	DIO	General-purpose input/output	
GPIO3_A4	352	DIO	General-purpose input/output	
GPIO3_A5	351	DIO	General-purpose input/output	
GPIO3_A6	346	DIO	General-purpose input/output	
GPIO3_A7	347	DIO	General-purpose input/output	
GPIO3_B0	348	DIO	General-purpose input/output	
GPIO3_B3	343	DIO	General-purpose input/output	
GPIO3_B4	342	DIO	General-purpose input/output	
GPIO3_B5	336	DIO	General-purpose input/output	
GPIO3_B6	337	DIO	General-purpose input/output	

GPIO3_C6	321	DIO	General-purpose input/output
GPIO3_D0	318	DIO	General-purpose input/output
GPIO3_D1	319	DIO	General-purpose input/output
GPIO4_B2	291	DIO	General-purpose input/output
GPIO4_D2	384	DIO	General-purpose input/output

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to conduct a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Wi-Fi & Bluetooth

The module provides a shared antenna interface: ANT_RF for Wi-Fi and Bluetooth functions. The impedance shall be kept as 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna or ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

Table 35: Pins Description of Wi-Fi & Bluetooth Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_RF	206	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω characteristic impedance

Table 36: Wi-Fi & Bluetooth Frequency (Unit: MHz)

Types	Frequency
Wi-Fi 802.11a/b/g/n/ac	2402–2482 5180–5825
Bluetooth 4.2	2402–2480

5.1.1. Wi-Fi Overview

The module supports 2.4 GHz and 5 GHz dual-band WLAN wireless communication based on Wi-Fi 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433.3 Mbps. The supported features are as below:

- Wake-on-WLAN (WoWLAN)

- CCA on secondary through RTS/CTS handshake
- TCP/UDP/IP checksum offload
- Transmit Beamforming
- WPA, WPA2
- AP and STA modes
- Wi-Fi Direct
- MCS 0–MCS 7: HT20 and HT40
- MCS 0–MCS 8: VHT20
- MCS 0–MCS 9: VHT40 and VHT80

Table 37: Wi-Fi Transmitting Performance

Bands	Standards	Speed Rates	Output Power
2.4 GHz	802.11b	1 Mbps	17 dBm ±3 dB
	802.11b	11 Mbps	17 dBm ±3 dB
	802.11g	6 Mbps	17 dBm ±3 dB
	802.11g	54 Mbps	15 dBm ±3 dB
	802.11n @ HT20	MCS 0	17 dBm ±3 dB
	802.11n @ HT20	MCS 7	13.5 dBm ±3 dB
	802.11n @ HT40	MCS 0	17 dBm ±3 dB
	802.11n @ HT40	MCS 7	13.5 dBm ±3 dB
5 GHz	802.11a	6 Mbps	15.5 dBm ±3 dB
	802.11a	54 Mbps	14 dBm ±3 dB
	802.11n @ HT20	MCS 0	15 dBm ±3 dB
	802.11n @ HT20	MCS 7	13 dBm ±3 dB
	802.11n @ HT40	MCS 0	15 dBm ±3 dB
	802.11n @ HT40	MCS 7	13 dBm ±3 dB
	802.11ac @ VHT20	MCS 0	15 dBm ±3 dB
	802.11ac @ VHT20	MCS 8	13 dBm ±3 dB
	802.11ac @ VHT40	MCS 0	15 dBm ±3 dB

	802.11ac @ VHT40	MCS 9	12 dBm ±3 dB
	802.11ac @ VHT80	MCS 0	15 dBm ±3 dB
	802.11ac @ VHT80	MCS 9	12 dBm ±3 dB

Table 38: Wi-Fi Receiving Performance

Bands	Standards	Speed Rates	Sensitivity (dBm)
2.4 GHz	802.11b	1 Mbps	-96
	802.11b	11 Mbps	-86
	802.11g	6 Mbps	-90
	802.11g	54 Mbps	-73
	802.11n @ HT20	MCS 0	-88
	802.11n @ HT20	MCS 7	-69
	802.11n @ HT40	MCS 0	-85
	802.11n @ HT40	MCS 7	-67
5 GHz	802.11a	6 Mbps	-90
	802.11a	54 Mbps	-73
	802.11n @ HT20	MCS 0	-89
	802.11n @ HT20	MCS 7	-70
	802.11n @ HT40	MCS 0	-86
	802.11n @ HT40	MCS 7	-67
	802.11ac @ VHT20	MCS 0	-90
	802.11ac @ VHT20	MCS 8	-68
	802.11ac @ VHT40	MCS 0	--87
	802.11ac @ VHT40	MCS 9	-63
	802.11ac @ VHT80	MCS 0	-83

	802.11ac @ VHT80	MCS 9	-60

NOTE

The product complies with the IEEE specifications.

5.1.2. Bluetooth Overview

The model with built-in Bluetooth function provides Bluetooth antenna interface. The module supports Bluetooth 4.2 (BR/EDR + BLE) specification, as well as GFSK, 8-DPSK, π/4-DQPSK modulations. Supported characteristics include:

- Enhanced Bluetooth/WLAN coexistence control to improve transmission quality in different profiles
- Secure Simple Pairing
- SCO or eSCO connection

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 39: Bluetooth Data Rates and Versions

Versions	Data Rates (Mbit/s)	Maximum Application Throughput
1.2	1	> 80 kbit/s
2.0 + EDR	3	> 80 kbit/s
3.0 + HS	24	Refer to 3.0 + HS
4.0	24	Refer to 4.0 LE
4.2	24	Refer to 4.2 LE

Referenced specifications are listed below:

- *Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1 + EDR/3.0/3.0 + HS, August 6, 2009*
- *Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009*
- *Bluetooth Low Energy RF PHY Test Specifications, Core_v4.2, December 12, 2014*

Table 40: Bluetooth Transmitting and Receiving Performance (Unit: dBm)

Transmitting Performance			
Packet types	DH5	2-DH5	3-DH5
Transmitting power	6 ±3	4.5 ±3	4.5 ±3
Receiving Performance			
Packet types	DH5	2-DH5	3-DH5
Receiving sensitivity	-89	-89	-83

5.1.3. Reference Design

A reference design of Wi-Fi & Bluetooth antenna interface is shown as below. C1 and C2 are not mounted by default. Only a 0 Ω resistor is mounted on R1.

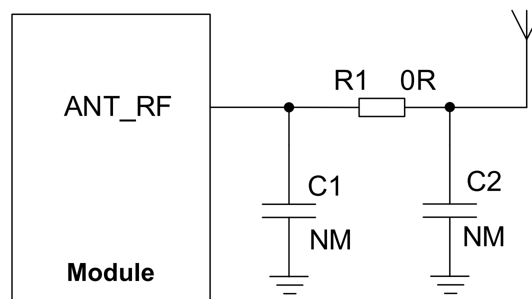


Figure 30: Reference Design of Wi-Fi & Bluetooth Antenna

5.2. RF Routing Guidelines

When designing PCB, characteristic impedance of all RF traces should be controlled to 50 Ω. Generally, the impedance of RF traces is determined by materials' dielectric constant, trace width (W), space between RF traces and grounds (S) and height from the reference ground to the signal layer (H). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures when characteristic impedance of RF traces is controlled to 50 Ω.

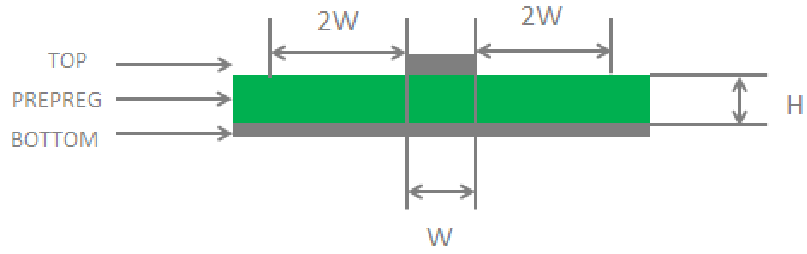


Figure 31: Microstrip Design on a 2-layer PCB

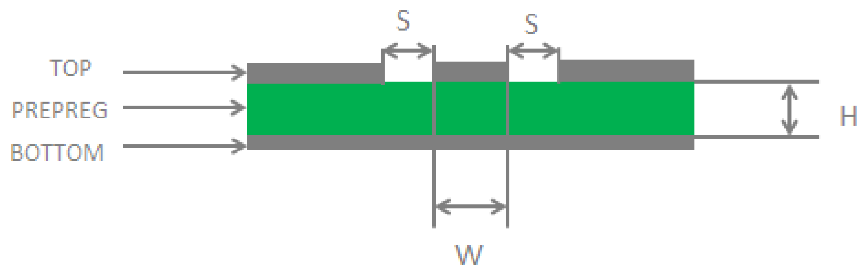


Figure 32: Coplanar Waveguide Design on a 2-layer PCB

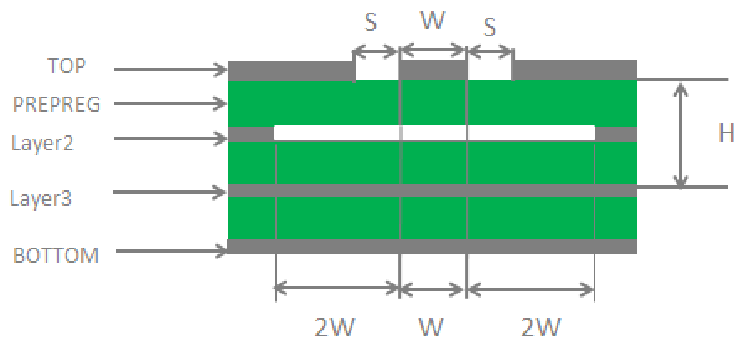


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

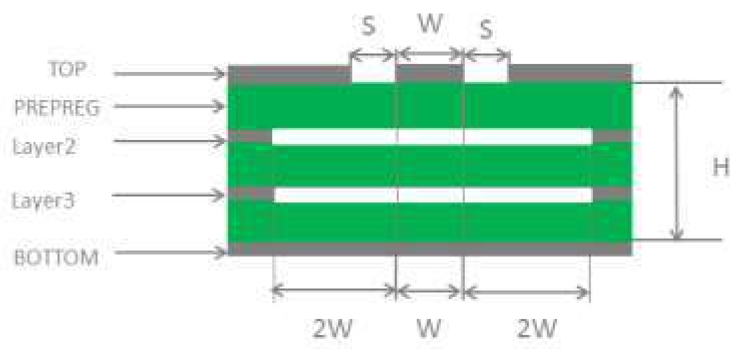


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure better RF performance and reliability, the following conditions should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- Clearance between RF pins and RF connector should be as short as possible, and all right-angle (90°) traces should be changed to the ones with the angle of 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground can improve RF performance. The clearance between ground vias and RF traces should be at least twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between any traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

5.3. Requirements for Antenna Design

Table 41: Requirements for Antenna Design

Antenna Types	Requirements
Wi-Fi & Bluetooth	VSWR: ≤ 2 Gain: 1 dBi Max input power: 50 W Input impedance: 50 Ω Vertical polarization

	Cable insertion loss: < 1 dB

5.4. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

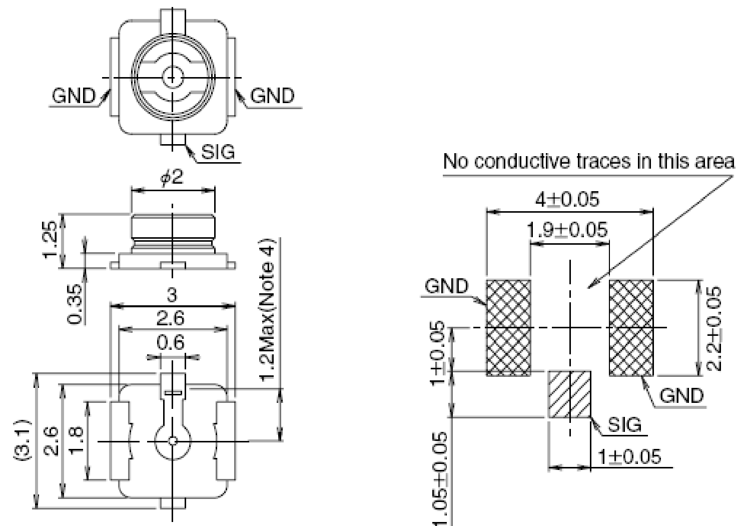


Figure 35: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 36: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

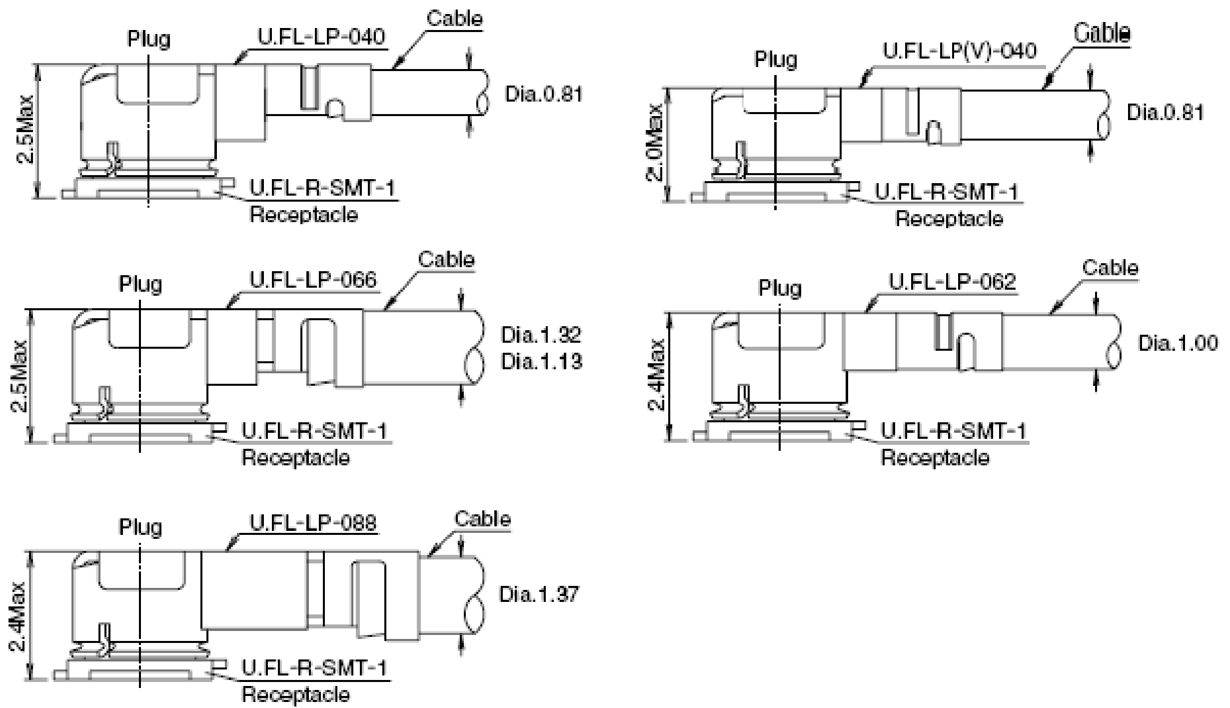


Figure 37: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 42: Absolute Maximum Ratings

Parameters	Min.	Max.	Units
Voltage at VBAT	-0.3	3.55	V
Voltage at USB_VBUS	-0.3	3.3	V
Voltage at digital pins	-0.3	VCCIOx + 0.3	V

6.2. Power Supply Ratings

Table 43: Module's Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Units
VBAT	Power supply for the module	The actual input voltage must be within this range	3.3	3.4	3.5	V
I_{VBAT}	Peak supply current	TBD	-	-	TBD	A

6.3. Power Consumption

Table 44: SG368Z-WF Power Consumption

Modes	Conditions	Typ.	Units
OFF state	Power off	100	μA
Standby state	Screen off	5.5	mA
Wi-Fi 11a Tx	@ 6 Mbps	380	mA
	@ 54 Mbps	370	mA
Wi-Fi 11b Tx	@ 1 Mbps	445	mA
	@ 11 Mbps	380	mA
Wi-Fi 11g Tx	@ 6 Mbps	443	mA
	@ 54 Mbps	369	mA
Wi-Fi 11n Tx	@ 7.2 Mbps 20 MHz	375	mA
	@ 72.2 Mbps 20 MHz	355	mA
Wi-Fi 11n Tx	@ 15 Mbps 40 MHz	373	mA
	@ 150 Mbps 40 MHz	364	mA
Wi-Fi 11ac Tx	@ 7.2 Mbps 20 MHz	395	mA
	@ 86.7 Mbps 20 MHz	438	mA
	@ 15 Mbps 40 MHz	391	mA
	@ 200 Mbps 40 MHz	429	mA
	@ 32.5 Mbps 80 MHz	392	mA
	@ 433.3 Mbps 80 MHz	432	mA
Wi-Fi 11a Rx	@ 54 Mbps	TBD	mA
Wi-Fi 11b Rx	@ 11 Mbps	TBD	mA
Wi-Fi 11g Rx	@ 54 Mbps	TBD	mA
Wi-Fi 11n Rx	@ 200 Mbps 40 MHz	TBD	mA

Wi-Fi 11ac Rx	@ 433.3 Mbps 80 MHz	TBD	mA
Bluetooth Tx Channel 0	-	322	mA
Bluetooth Tx Channel 38	-	324	mA
Bluetooth Tx Channel 78	-	326	mA
Bluetooth Rx Channel 38	-	TBD	mA

Table 45: SG368Z-AP Power Consumption

Modes	Conditions	Typ.	Units
OFF state	Power off	100	μA
Standby state	Screen off	5.5	mA

NOTE

The power consumption data above is for reference only, which may vary among different modules. For detailed information, contact Quectel Technical Support for the power consumption test report of the specific module.

6.4. Digital I/O Characteristics

Table 46: 1.8 V VCCIO I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	0.65 × VCCIO	VCCIO + 0.3
V_{IL}	Low-level input voltage	-0.3	0.35 × VCCIO
V_{OH}	High-level output voltage	1.4	VCCIO + 0.3
V_{OL}	Low-level output voltage	-0.3	0.4

Table 47: PMUIO0 I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.65 × PMUIO0	PMUIO0 + 0.3
V_{IL}	Low-level input voltage	-0.3	0.35 × PMUIO0
V_{OH}	High-level output voltage	1.4	PMUIO0 + 0.3
V_{OL}	Low-level output voltage	-0.3	0.4

Table 48: PMUIO1 I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	2.0	PMUIO1 + 0.3
V_{IL}	Low-level input voltage	-0.3	0.8
V_{OH}	High-level output voltage	2.4	PMUIO1 + 0.3
V_{OL}	Low-level output voltage	-0.3	0.4

Table 49: PMUIO2 I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.65 × PMUIO2	PMUIO2 + 0.3
V_{IL}	Low-level input voltage	-0.3	0.35 × PMUIO2
V_{OH}	High-level output voltage	1.4	PMUIO2 + 0.3
V_{OL}	Low-level output voltage	-0.3	0.4

Table 50: SD Card High-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	2.0	VCCIO3 + 0.3
V_{IL}	Low-level input voltage	-0.3	0.8

V_{OH}	High-level output voltage	2.4	VCCIO3 + 0.3
V_{OL}	Low-level output voltage	-0.3	0.4

Table 51: SD Card Low-voltage I/O Characteristics (Unit: V)

Parameter	Description	Min.	Max.
V_{IH}	High-level input voltage	0.65 × VCCIO3	VCCIO3 + 0.3
V_{IL}	Low-level input voltage	-0.3	0.35 × VCCIO3
V_{OH}	High-level output voltage	1.4	VCCIO3 + 0.3
V_{OL}	Low-level output voltage	-0.3	0.4

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 52: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %, Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT and GND	±TBD	±TBD
Antenna interface	±4	±8
Other interfaces	±TBD	±TBD

6.6. Operating and Storage Temperatures

Table 53: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Industrial grade Operating Temperature [2]	-40	+25	+85
Commercial grade Operating Temperature [2]	-10	+25	+75
Storage Temperature	-40	-	+90

[2] Within the operating temperature range, the module meets IEEE specifications.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

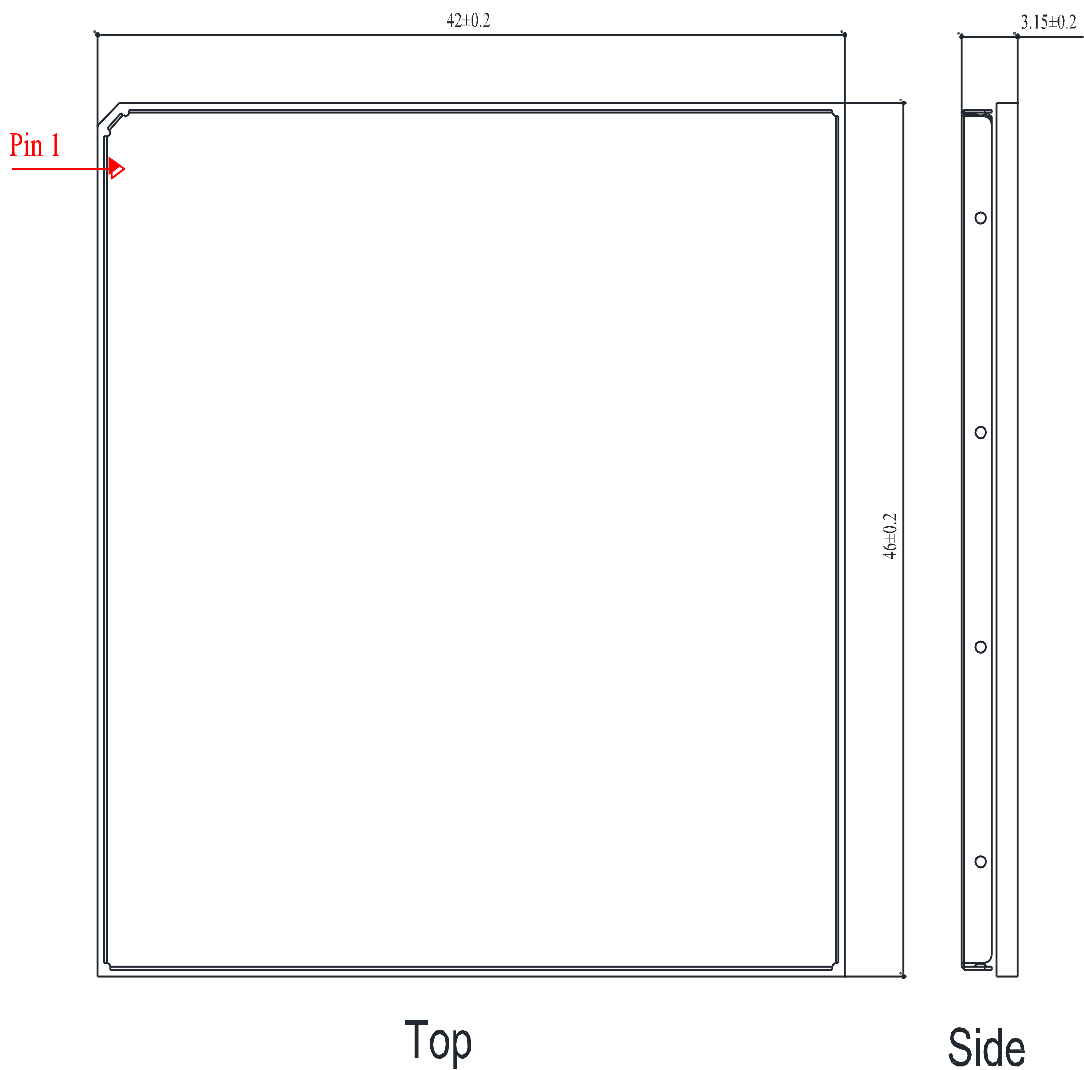


Figure 38: Top and Side Dimensions

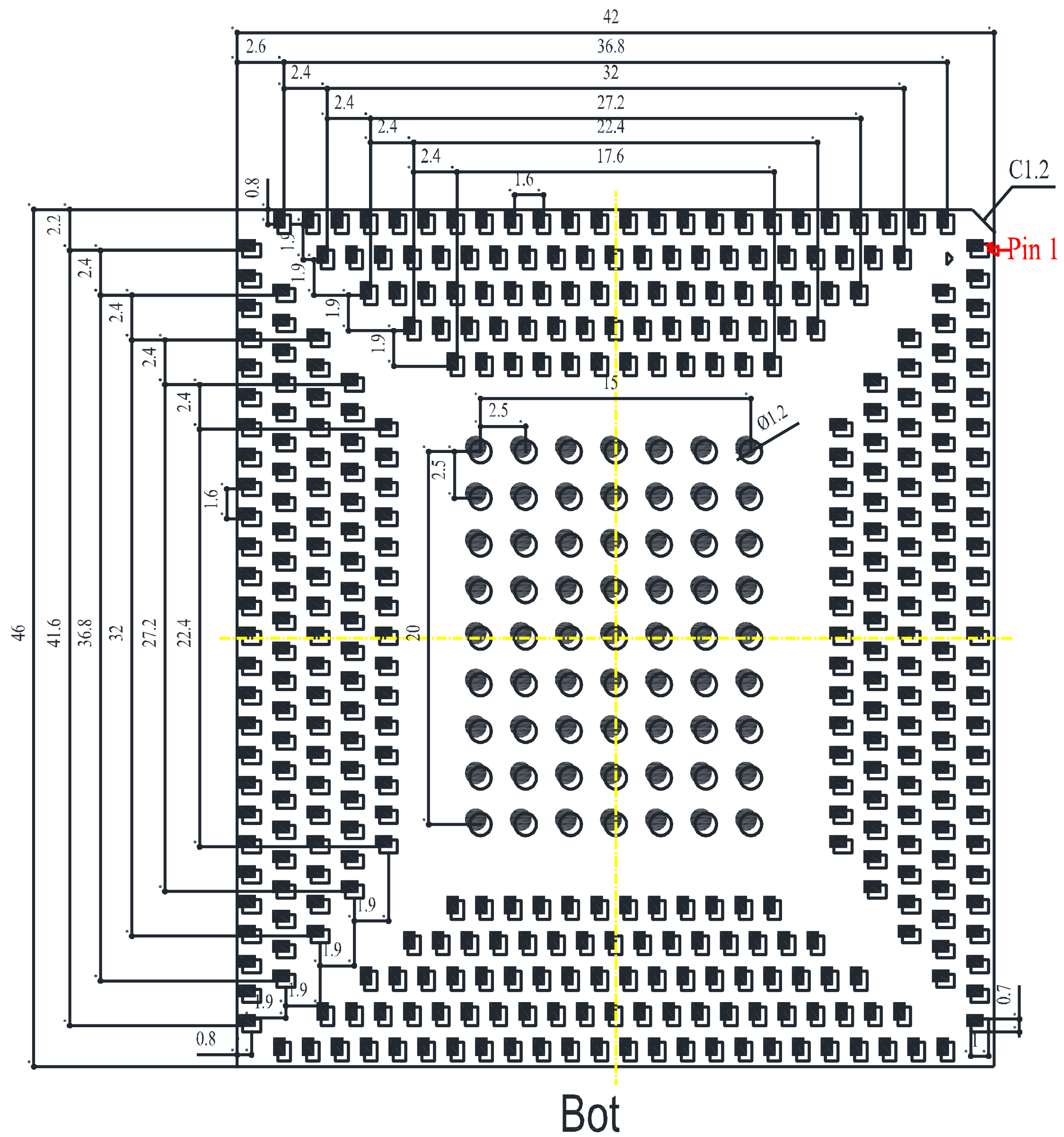


Figure 39: Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

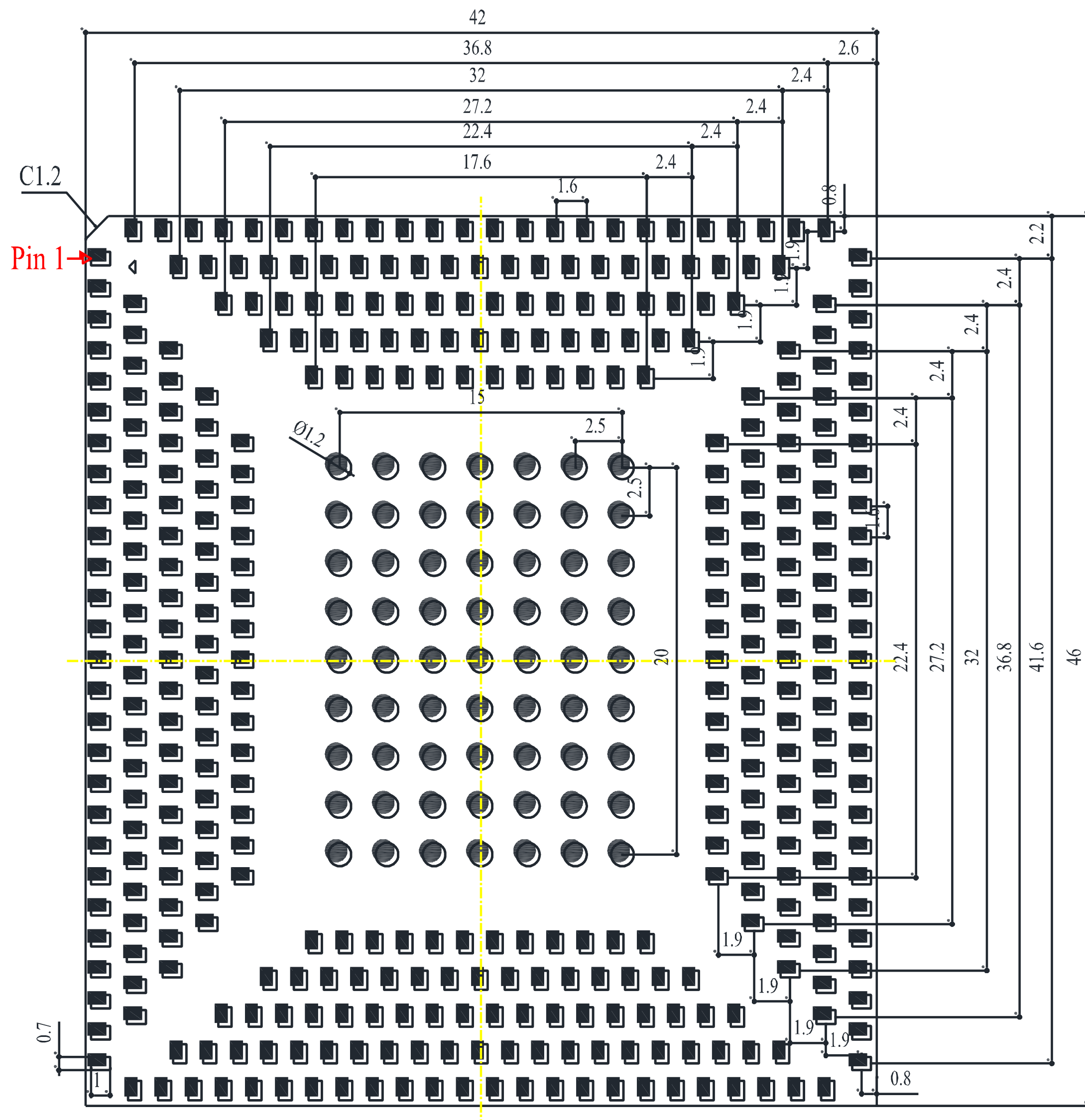


Figure 40: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

Figure 41: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended storage condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in recommended storage condition.

3. Floor life: 168 hours [3] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in recommended storage condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[3] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be TBD mm. For more details, see ***document [5]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

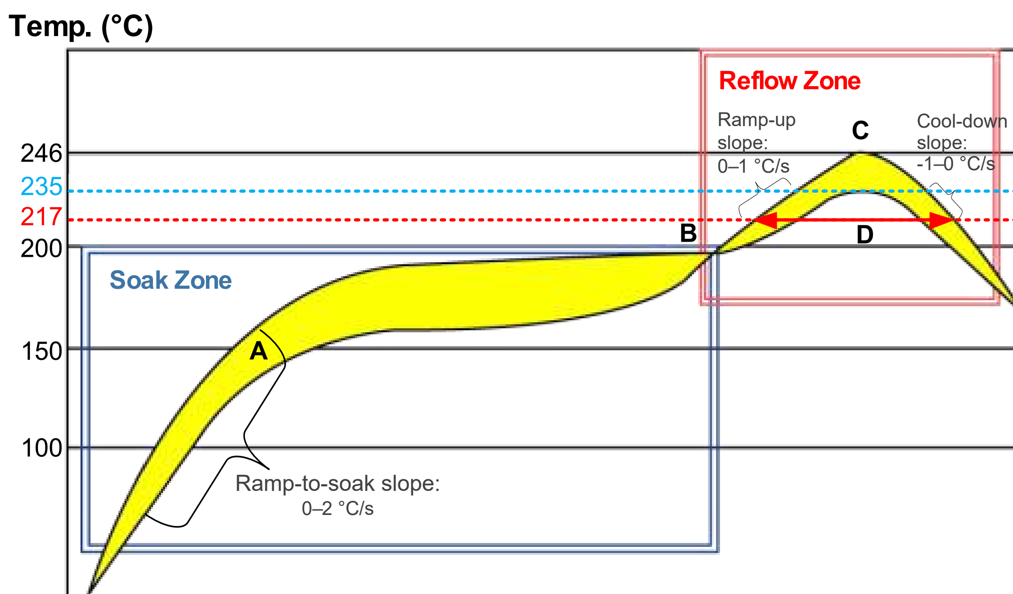


Figure 42: Recommended Reflow Soldering Thermal Profile

Table 54: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–2 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
217–235 °C ramp-up slope	0–1 °C/s
Reflow time (D: over 217°C)	40–65 s
Max temperature	235–246 °C
235–217 °C cool-down slope	-1–0 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. Due to the large-size form factor, to avoid excessive temperature change, which may cause excessive thermal deformation of the metal shielding frame and cover, it is recommended to reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste. If possible, please choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [5]***.

8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

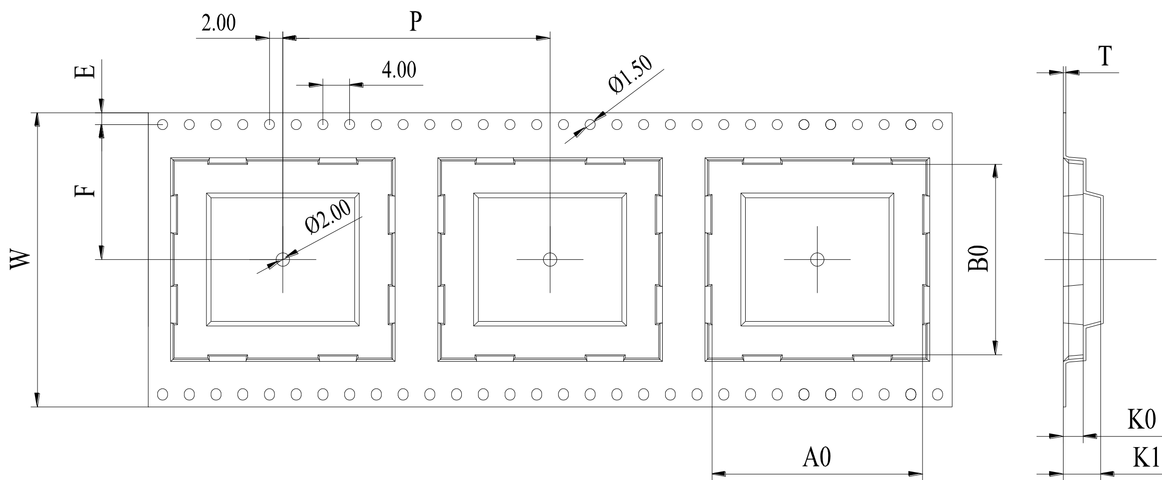


Figure 43: Carrier Tape Dimension Drawing

Table 55: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.4	42.6	46.6	4.25	5.25	34.2	1.75

8.3.2. Plastic Reel

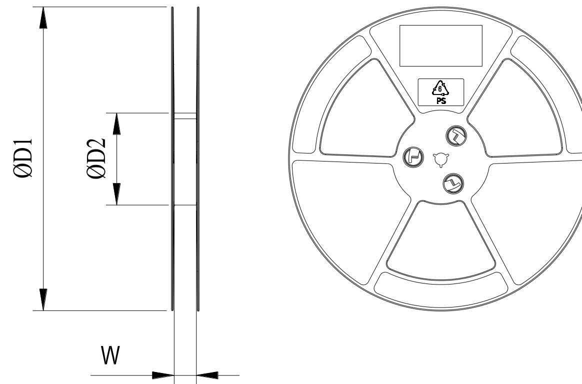


Figure 44: Plastic Reel Dimension Drawing

Table 56: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

8.3.3. Mounting Direction

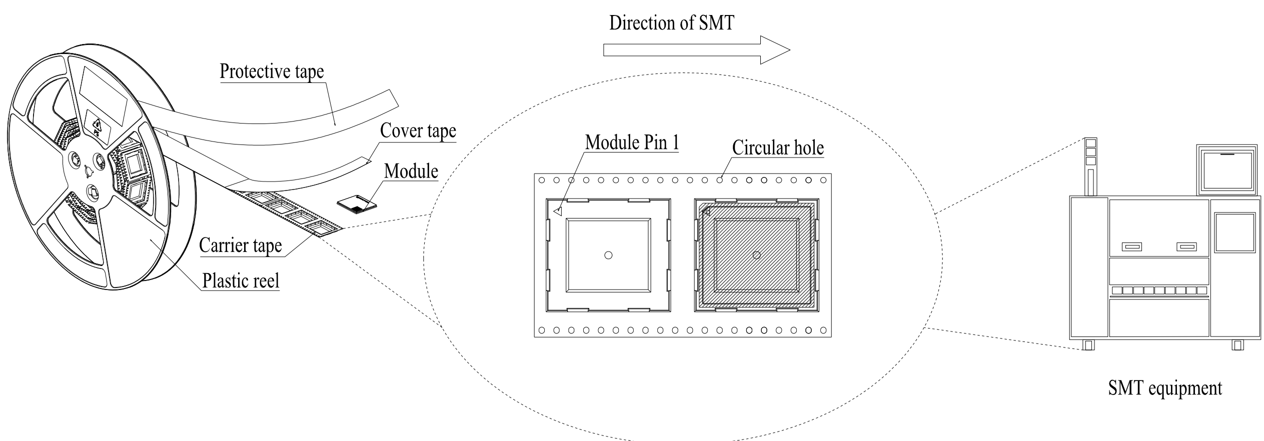
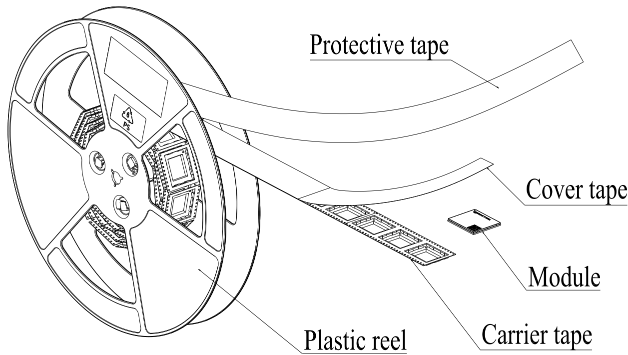


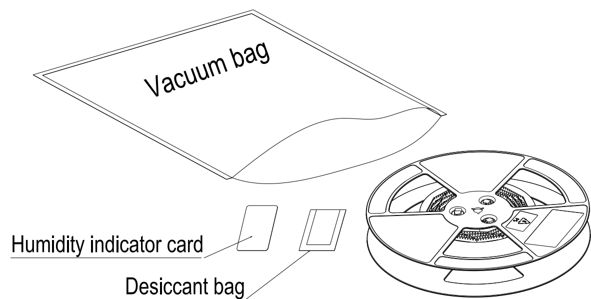
Figure 45: Mounting Direction

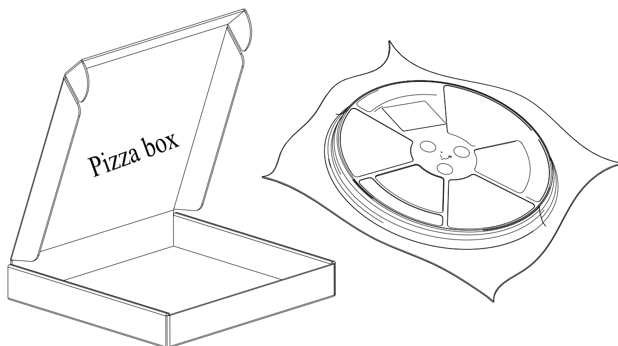
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 200 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 800 modules.

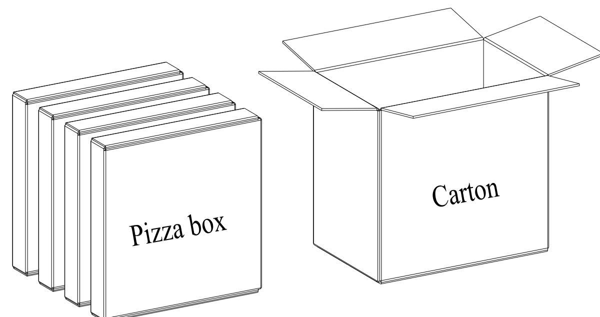


Figure 46: Packaging Process

9 Appendix References

Table 57: Related Documents

Document Name
[1] Quectel_SG368Z_Series_EVB_User_Guide
[2] Quectel_SG368Z_Series_GPIO_Configuration
[3] Quectel_SG368Z_Series_Reference_Design
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_SMT_Application_Note

Table 58: Terms and Abbreviations

Abbreviation	Description
AAC	Advanced Audio Coding
ABD	Android Debug Bridge
AC	Alternating Current
AP	Application Processor
ARM	Advanced RISC Machine
BLE	Bluetooth Low Energy
bps	Bytes per second
BR	Basic Rate
CC	Configuration Channel
CEC	Consumer Electronic Control
CSI	Camera Serial Interface

CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-The-Air
DPSK	Differential Phase Shift Keying
DQPSK	Differential Quadrature Phase Shift Keying
DSI	Display Serial Interface
DVR	Digital Video Recorder
eDP	Embedded DisplayPort
EDR	Enhanced Data Rate
EFR	Enhanced Full Rate
EMI	Electromagnetic Interference
eMMC	Embedded Multimedia Card
EP	End Point
eSCO	Extended Synchronous Connection Oriented
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
EVB	Evaluation Board
FIFO	First In First Out
FR	Full Rate
GFSK	Gaussian Frequency Shift Keying
GMAC	Gigabit Media Access Controller
GND	Ground
GPU	Graphics Processing Unit
HCSL	High-speed Current Steering Logic
HDMI	High Definition Multimedia Interface
HR	Half Rate

HS	High Speed
HT	High Throughput
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IEEE	Institute of Electrical and Electronics Engineers
IP	Internet Protocol
ISP	Image Signal Processor
LCM	Liquid Crystal Monitor
LDO	Low Dropout Regulator
LGA	Land Grid Array
LPDDR	Low-Power Double Data Rate
LVDS	Low-Voltage Differential Signaling
M2M	Machine to Machine
MAC	Media Access Control
MCS	Modulation and Coding Scheme
MIPI	Mobile Industry Processor Interface
MP	Megapixel
MP3	Moving Picture Experts Group Audio Layer III
MSL	Moisture Sensitivity Levels
NAS	Non-Access Stratum
NVR	Network Video Recorder
OTG	On-The-Go
OTP	One Time Programmable
PC	Personal Computer
PCB	Printed Circuit Board

PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDM	Pulse Density Modulation
PHY	Physical Layer
RC	Root Complex
RF	Radio Frequency
RGB	Red Green Blue
RGMII	Reduced Gigabit Media Independent Interface
RoHS	Restriction of Hazardous Substances
RTS	Request To Send
SATA	Serial Advanced Technology Attachment
SCO	Synchronous Connection Oriented
SD	Secure Digital
SDIO	Secure Digital Input and Output Card
SGMII	Serial Gigabit Media Independent Interface
SMT	Surface Mount Technology
STA	Station
TCP	Transmission Control Protocol
TDM	Time-Division Multiplexing
TP	Touch Panel
TVS	Transient Voltage Suppressor
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module

VBAT	Voltage at Battery (Pin)
VHT	Very High Throughput
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Network
WPA	Wi-Fi Protected Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage

$V_{I}max$	Absolute Maximum Input Voltage
$V_{I}min$	Absolute Minimum Input Voltage
$V_{OH}max$	Maximum High-level Output Voltage
$V_{OH}min$	Minimum High-level Output Voltage
$V_{OL}max$	Maximum Low-level Output Voltage
$V_{OL}min$	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network

Modifications:

Any changes or modifications not expressly approved by Quectel or the party responsible for compliance could void the user's authority to operate the equipment and invalidate the regulatory approval.

Host manufacturer must follow KDB Publication 996369 D04 Modulen Integration Guide.

Host manufacturer is responsible for regression tests to show compliance to the applicable standards due to the following actions:

1.any modification done to the module.

2.Integration of the module into a host device

Host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

Final host product is required to show compliance to Part 15 Subpart B with the modular transmitter installed

Product Marketing Name：Quectel SG368Z-WF

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3. A label with the following statements must be attached to the host end product:
This device contains FCC ID: XMR2023SG368ZWF
FCC/ISED Regulations restrict operation of this device to Indoor Use Only

4. Antenna Requirements:

- The following antennae were approved with the modules:

Operating Band	Frequency (MHz)	Antenna Type	Antenna P/N	Antenna Gain (dBi)
Bluetooth	2400~2483.5	Dipole	YE0038BA	-0.5 dBi
2.4G WiFi				-0.5 dBi
5G WiFi	5150~5850			5150~5250 MHz:2.0 dBi 5250~5350 MHz:2.0 dBi 5470~5725 MHz:3.2 dBi 5725~5850 MHz:3.3 dBi

- The product is provided with an approved antenna. Use only supplied or approved antenna by Quectel. Any changes or modifications to the Antenna may void the regulatory approvals obtained for the product.
- Host device must comply with FCC Part 15 antenna requirements
- The OEM must design the host so that the antenna will be installed as an integrated antenna for the host containing the SG368Z-WF and the end user shall not be able to access, remove or replace the antenna.

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: “Contains Transmitter Module FCC ID: XMR2023SG368ZWF” or “Contains FCC ID: XMR2023SG368ZWF” must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module

and the FCC ID.
The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.
The user’s manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
Changes or modifications not expressly approved by the manufacturer could void the user’s authority to operate the equipment.
To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier’s Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.
Manual Information To the End User
The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement
IRSS-GEN
"This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d’Industrie Canada applicables aux appareils radio exempts de licence. L’exploitation est autorisée aux deux conditions suivantes :
1) l’appareil ne doit pas produire de brouillage; 2) l’utilisateur de l’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en compromettre le fonctionnement."
Déclaration sur l'exposition aux rayonnements RF
L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.
The host product shall be properly labeled to identify the modules within the host product.
The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows:
“Contains IC: 10224A-23SG368ZWF” or “where: 10224A-23SG368ZWF is the module’s certification

number”.
Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.
L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:
"Contient IC: 10224A-23SG368ZWF" ou "où: 10224A-23SG368ZWF est le numéro de certification du module".

i. the device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;

ii. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit;

iii. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits as appropriate;

iv. Omnidirectional antenna is recommended