RG500L Series QuecOpen Hardware Design

5G Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-09-02	Ellen LI/ Hank LIU/ Ballon SHI	Creation of the document
1.0	2021-09-02	Ellen LI/ Hank LIU/ Ballon SHI	First official release
1.1	2022-02-15	Ellen LI/ Hank LIU/ Ballon SHI	1. Updated supported frequency bands of RG500L-NA (Table 3). 2. Added MIMO information of RG500L-NA (Table 4). 3. Updated the 5G SA UL maximum data rate to 1.25 Gbps (Table 4). 4. Updated supported Internet protocol features (Table 4). 5. Added the chapter about USB application scenario of entering sleep mode (Chapter 3.2.2). 6. Updated timing of turning on/off the module (Figure 9 & 10). 7. Added a note for turning on the module with PWRKEY (Chapter 3.5.1). 8. Updated ADC resolution (Chapter 4.7). 9. Added operating frequency and cellular antenna mapping of RG500L-NA (Table 32 & 34). 10. Added RF receiving sensitivity of RG500L series (Table 36 & 37). 11. Added illustrations of installing the coaxial cable plug (Chapter 5.5.1 & 5.5.2). 12. Added peak current of VBAT_BB and VBAT_RF respectively (Table 42). 13. Added typical and maximum I_{VBAT} under maximum

			power control level at n41 (Table 43). 14. Added averaged power consumption (Table 44). 15. Added 1.86/3.0 V SDIO I/O requirements and 1.8/3.0 V (U)SIM I/O requirements (Table 47–50). 16. Updated the recommended max slope in Recommended Thermal Profile Parameters (Figure 49 & Table 53). 17. Added the chapter about related AT commands (Chapter 9).
1.2	2023-05-06	Grace GUO/ Hubery Huang/ Keil WEI/ Kelsey ZHUANG	1. Added applicable module: RG500L-LA. 2. Added footnotes for GNSS feature, 5G NR n5/n71, LTE-FDD B5/B71 and WCDMA B5 of RG500L-EU (Table 3). 3. Added optional frequency bands 5G NR n71 and LTE-FDD B71 to RG500L-EU (Table 3, Table 31 and Table 39). 4. Updated RG500L-EU cellular antenna mapping (Table 34 and Table 35). 5. Updated the RF receiving sensitivity of RG500L-NA (Table 40). 6. Updated the frequency range of GNSS L1 and VSWR parameter in antenna requirements (Table 45). 7. Updated the digital I/O characteristic (Table 50, Table 53 and Table 54). 8. Updated the recommended reflow soldering thermal profile, the recommended thermal profile parameters and related note (Chapter 8.2). 9. Updated the packaging information (Chapter 8.3).
1.3.0	2023-05-13	Colin SHI/ Reuben BAO/ Grace GUO	Preliminary: Added applicable modules: RG500L-JO and RG500L-AR.

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1 Introduction

QuecOpen® is a solution where the module acts as the main processor. Constant transition and evolution of both the communication technology and the market highlight its merits. It can help you to:

- Realize embedded applications' quick development and shorten product R&D cycle
- Simplify circuit and hardware structure design to reduce engineering costs
- Miniaturize products
- Reduce product power consumption
- Apply OTA technology
- Enhance product competitiveness and price-performance ratio

This document defines the RG500L series module under QuecOpen® solution and describes its air interfaces and hardware interfaces which relate to your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

RG500L series module is an SMD type module which is engineered to meet the demanding requirements in M2M applications, such as 5G wireless router, CPE, MiFi, business router, home gateway, etc. Related information and details are listed in the table below:

Table 2: Brief Introduction of the Module

Categories	
Package Type and Number of Pins	LGA; 430
Dimensions	(41.0 ±0.20) mm × (44.0 ±0.20) mm × (2.75 ±0.20) mm
Weight	RG500L-EU/-NA/-LA: Approx. 11 g
Wireless Network Functions	Cellular: 5G NR/LTE/WCDMA GNSS
Variant	RG500L-EU/RG500L-NA/RG500L-LA/RG500L-AR*/RG500L-JO*

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	RG500L-EU	RG500L-NA	RG500L-LA	RG500L-AR*	RG500L-JO*
5G NR	n1/n3/n5 [1]/ n7/n8/n20/n28/ n38/n40/n41/n71 [1]/ n77/n78	n2/n5/n7/n12/n25/ n38/n41/n48/n66/ n71/n77/n78	n2/n5/n7/n28/ n66/n78	n1/n3/n5/n8/ n40/n78	n28/n78
LTE-FDD	B1/B3/B5 [1]/B7/ B8/B20/B28/ B32/B71 [1]	B2/B4/B5/B7/B12/ B13/B14/B17/B25/ B26/B29/B30/B66/ B71	B2/B4/B5/B7/ B8/B28/B66	B1/B3/B5/B8	-

[1] For RG500L-EU, 5G NR n5/n71 bands and LTE B5/B71 bands and WCDMA B5 are optional. For details, please contact Quectel Technical Support.

LTE-TDD	B38/B40/B41/B42/ B43	B38/B41/B42/B43/ B48	B42/B43	B40	-
LTE-LAA	-	B46	-	-	-
WCDMA	B1/B5 [1]/B8	-	B2/B4/B5	-	-
GNSS [2]	GPS/BDS/ GLONASS/Galileo (L1 + L5)	GPS/BDS/ GLONASS/ Galileo (L1 only)	-	-	-

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card by default
(U)SIM Interfaces	● Supports USIM/SIM card: 1.8 V, 3.0 V ● Supports Dual SIM Single Standby
Audio Features	Supports two digital audio interfaces: PCM
PCM Interfaces	● Used for audio function with external SLIC ● Supports long frame synchronization and short frame synchronization ● Supports master and slave modes, but must be the master in long frame synchronization
SPI Interfaces	● Two SPI interfaces which support slave mode* and master mode ● Supports synchronous and serial communication link with the peripheral devices ● 1.8 V power domain with clock rates up to 52 MHz
I2C Interface	One I2C interface
SGMII Interfaces	● *IEEE 802.3* compliant ● Supports 10/100/1000/2500 Mbps in full duplex mode
Interface for WLAN Application	Supports PCIe interface for WLAN application

[2] For RG500L-EU/RG500L-NA, GNSS function is optional, but for RG500L-LA/RG500L-JO*/RG500L-AR*, GNSS function is not supported. For details, please contact Quectel Technical Support.

USB Interface	● Compliant with USB 3.0 and 2.0 specifications, with transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 ● Used for AT command communication, data transmission, GNSS NMEA* sentence output, software debugging and firmware upgrade ● USB serial driver: supports USB serial driver for Windows 7/8/8.1/10
SDIO Interface	**RG500L-EU/RG500L-NA/RG500L-LA**: ● Supports one SDIO interface ● Supports SD 3.0 protocol ● Only used for SD card **RG500L-AR*/RG500L-JO***: ● Not supported
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for Linux console and log output ● Baud rate: 921600 bps **Bluetooth UART:** ● Used for Bluetooth communication ● Baud rate: 115200 bps
PCIe Interfaces	● *PCI Express Base Specification Revision 3.0* compliant ● Data rate up to 8 Gbps per lane ● Only supports Root Complex mode ● Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC **RG500L-EU/RG500L-NA/RG500L-LA:** ● Supports four PCIe interfaces **RG500L-AR*/-JO*:** ● Supports two PCIe interfaces: PCIe0 and PCIe1
Network Indication*	NET_MODE and NET_STATUS to indicate network connectivity status
AT Commands	Compliant with 3GPP TS 27.007, 27.005 and Quectel enhanced AT commands
Antenna Interfaces	● Cellular antenna interfaces: – RG500L-EU/RG500L-NA/RG500L-LA/RG500L-AR*: 8 cellular antenna interfaces (ANT0-ANT7) – RG500L-JO*: 6 cellular antenna interfaces (ANT0/ANT2/ANT3/ANT4/ANT6/ANT7) ● GNSS antenna interface: – RG500L-EU: ANT_GNSS (L1 + L5) – RG500L-NA: ANT_GNSS (L1 only) – RG500L-LA/RG500L-AR*/RG500L-JO*: Not supported ● 50 Ω impedance

Transmitting Power	● WCDMA: Class 3 (23 dBm ±2 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB) ● LTE-TDD: Class 3 (23 dBm ±2 dB) ● 5G NR: Class 3 (23 dBm ±2 dB) ● 5G NR n40/n41/n77bands UL MIMO HPUE [3]: Class 2 (26 dBm +2/-3 dB) ● 5G NR n78 bands UL MIMO for Part27:21dBm+1.5/-1 ● 5G NR n78 bands UL MIMO for Part96:15dBm+1.5/-1 ● LTE B42: 22.5dBm+0.5/-1.5 dB
5G NR Features	● Supports 3GPP Rel-15 ● Supports 2CC CA ● Supports uplink 256QAM and downlink 256QAM ● Supports DL 4 × 4 MIMO: – RG500L-EU: n1/n3/n7/n38/n40/n41/n77/n78 – RG500L-NA: n2/n7/n25/n38/n41/n48/n66/n77/n78 – RG500L-LA: n2/n7/n66/n78 – RG500L-AR*: n1/n3/n5/n8/n40/n78 – RG500L-JO*: n78 ● Supports UL 2 × 2 MIMO [4]: – RG500L-EU: n40/n41/n77/n78 – RG500L-NA: n41/n48/n77/n78 – RG500L-LA: n78 – RG500L-AR*: n40/n78 – RG500L-JO*: n78 ● Supports SCS 15 kHz and 30 kHz ● Supports SA and NSA operation modes [5] ● Supports Option 3x, 3a, 3, and Option 2 ● Maximum data rates [6]: NSA: 3.74 Gbps (DL)/ 1.46 Gbps [7] (UL) SA: 4.67 Gbps (DL)/ 1.25 Gbps (UL)
LTE Features	● Supports both FDD and TDD ● Supports up to CA Cat 19 ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports LTE DL 4 × 4 MIMO: RG500L-EU: B1/B3/B7/B38/B40/B41/B42/B43 RG500L-NA: B2/B4/B7/B25/B30/B38/B41/B42/B43/B48/B66 RG500L-LA: B2/B4/B7/B42/B43/B66 RG500L-AR*: B1/B3/B5/B8/B40 ● Supports UL QPSK, 16QAM and 64QAM and 256QAM modulation ● Supports DL QPSK, 16QAM and 64QAM and 256QAM modulation

[3] HPUE only supports single-signal carrier waves.
[4] Uplink 2 × 2 MIMO is only supported in 5G TDD SA mode.
[5] RG500L-JO only support SA operation mode.
[6] The maximum rates are theoretical and the actual values are subject to the network configuration.
[7] 1.46 Gbps is the theoretical UL data rate when LTE and 5G NR uplink 256QAM are both enabled. As LTE uplink 256QAM in EN-DC is not required by operators, it is disabled by default.

	● Maximum data rates: LTE: 1.6 Gbps (DL)/ 211 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-9 DC-HSDPA/HSPA+/HSDPA/HSUPA/WCDMA ● Supports QPSK/16QAM/64QAM modulation ● Maximum data rates: DC-HSDPA: 42 Mbps HSUPA: 5.76 Mbps WCDMA: 384 kbps (DL)/ 384 kbps (UL)
Internet Protocol Features	● Supports MIPC/TCP/UDP/FTP/HTTP/NTP/PING/HTTPS/MMS/FTPS/ SSL protocols ● Support PAP and CHAP for PPP connections
GNSS Features [2]	● Supports GPS/BDS/GLONASS/Galileo ● Protocol: *NMEA 0183* ● Data update rate: 1 Hz by default, max. 5 Hz
Temperature Range	● Operating temperature range [8]: -30 °C to +70 °C ● Extended temperature range [9]: -40 °C to +85 °C ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	Use USB interface or FOTA for upgrade
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3.

2.3. Pin Assignment

The following figure illustrates the pin assignment of the module.

[8] To meet this operating temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this operating temperature range, the module can meet 3GPP specifications.

[9] To meet this extended temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

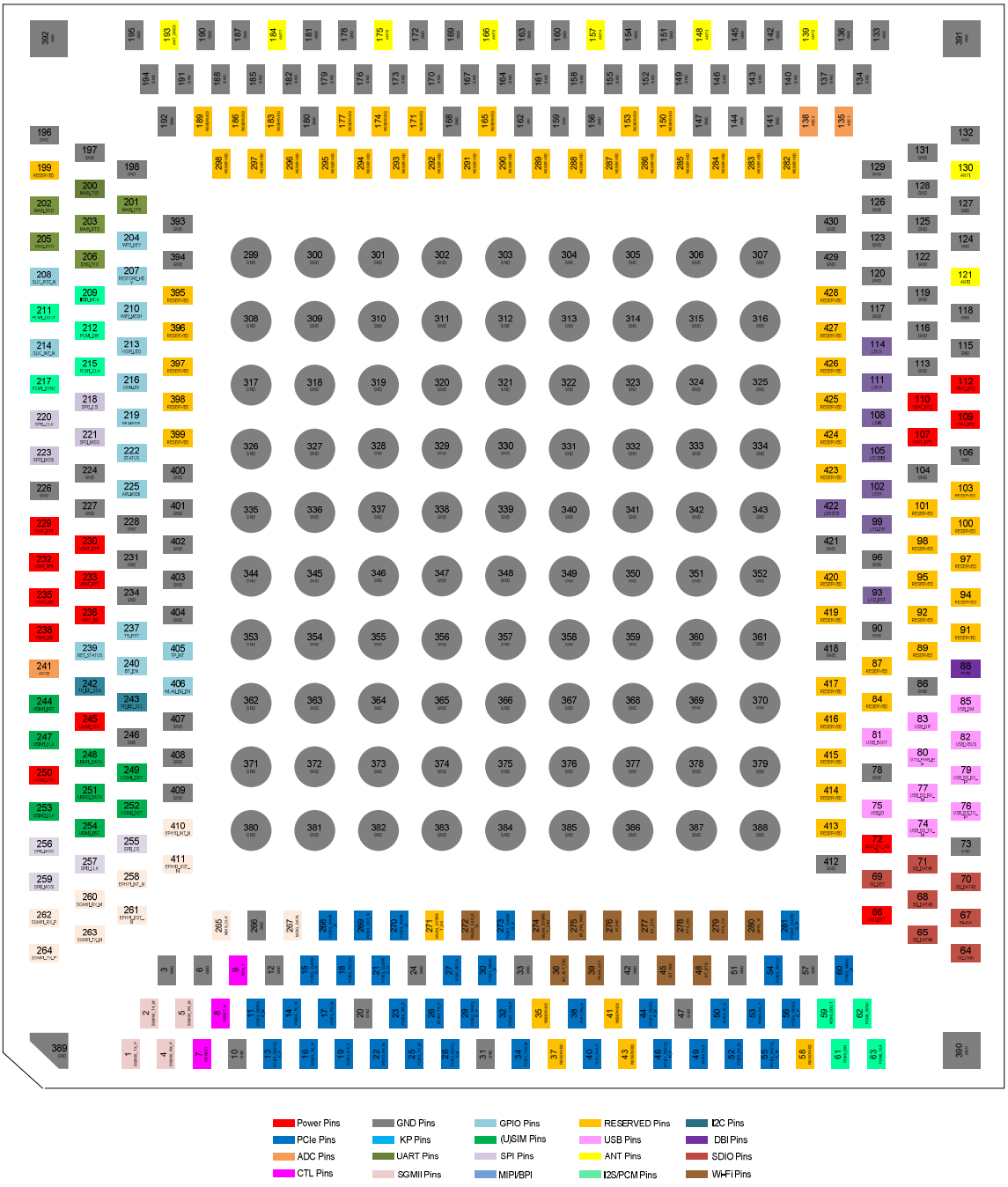


Figure 1: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins unconnected.
2. For RG500L-AR* and RG500L-JO*, SDIO interface, PCIe2 and PCIe3 interfaces are not supported, and the relevant pins should be reserved.

2.4. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	235, 236, 238	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	
VBAT_RF1	229, 230, 232, 233	PI	Power supply for the module's RF part		
VBAT_RF2	107, 109, 110, 112	PI	Used to connect decoupling capacitors		There is no need to connect VBAT_RF2 to the external power supply.
VDD_EXT	66	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits.

Turn On/Off & Other Control Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turn on/off the module	1.8 V	Internally pulled up to 1.8 V. Active low.
RESET_N	8	DI	Reset the module		Internally pulled up to 1.8 V. Active low.
PON_1	9	DI	Turn on/off the module	VBAT_BB	
RESTORE_KEY	207	DI	Restore the module	1.8 V	
WPS_KEY*	204	DI	Wi-Fi protected setup		
Indication Signals					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	222	OD	Indicate the module's operation status		PMIC_ISINK3
NET_MODE*	219	DO	Indicate the module's network registration mode	1.8 V	
NET_STATUS*	239	OD	Indicate the module's network activity status		PMIC_ISINK2
AIR_MODE	225	OD	Indicate the module's airplane mode		PMIC_ISINK1
WIFI_MESH*	210	DO	Indicate the Wi-Fi mesh function status	1.8 V	
USIM_LED*	216	DO	Indicate the (U)SIM card function status		
VOIP_LED*	213	DO	Indicate the VoIP function status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	82	AI	USB connection detect	Vmax = 15 V Vmin = 4.2 V Vnom = 5.0 V	Used for USB connection detection (disabled by default). Cannot be used for power supply.
USB_DP	83	AIO	USB differential data (+)		Require differential impedance of 90 Ω.

USB_DM	85	AIO	USB differential data (-)		
USB_SS_TX_P	76	AO	USB 3.0 super-speed transmit (+)		
USB_SS_TX_M	74	AO	USB 3.0 super-speed transmit (-)		Require differential impedance of 90 Ω. If unused, connect RX to GND directly.
USB_SS_RX_P	79	AI	USB 3.0 super-speed receive (+)		
USB_SS_RX_M	77	AI	USB 3.0 super-speed receive (-)		
USB_ID	75	DI	USB ID detect	1.8 V	
OTG_PWR_EN	80	DO	OTG power control		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	245	PO	(U)SIM1 card power supply	1.8/3.0 V	
USIM1_DATA	248	DIO	(U)SIM1 card data		
USIM1_CLK	247	DO	(U)SIM1 card clock		
USIM1_RST	244	DO	(U)SIM1 card reset		
USIM1_DET	249	DI	(U)SIM1 card hot-plug detect	1.8 V	
USIM2_VDD	250	PO	(U)SIM2 card power supply	1.8/3.0 V	
USIM2_DATA	251	DIO	(U)SIM2 card data		
USIM2_CLK	253	DO	(U)SIM2 card clock		
USIM2_RST	254	DO	(U)SIM2 card reset		
USIM2_DET	252	DI	(U)SIM2 card hot-plug detect	1.8 V	
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	67	DO	SD card clock	1.86/3.0 V	Only used for SD card. Not supported by RG500L-AR* and
SD_CMD	64	DIO	SD card command		
SD_DATA0	65	DIO	SDIO data bit 0		

SD_DATA1	71	DIO	SDIO data bit 1		RG500L-JO*.
SD_DATA2	70	DIO	SDIO data bit 2		
SD_DATA3	68	DIO	SDIO data bit 3		
SD_DET	69	DI	SD card hot-plug detect	1.8 V	
SDIO_PU_VDD	72	PO	SD card IO pull-up power supply	1.86/3.0 V	Not supported by RG500L-AR* and RG500L-JO*.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	201	DO	Clear to send signal from the module	1.8 V	Connect to the peripheral's CTS.
MAIN_RTS	203	DI	Request to send signal to the module		Connect to the peripheral's RTS.
MAIN_RXD	202	DI	Main UART receive		
MAIN_TXD	200	DO	Main UART transmit		
Bluetooth UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BT_TXD	45	DO	Bluetooth UART transmit	1.8 V	
BT_RXD	276	DI	Bluetooth UART receive		
BT_RTS	48	DI	Request to send signal to the module		Connect to the peripheral's RTS.
BT_CTS	277	DO	Clear to send signal from the module		Connect to the peripheral's CTS.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	205	DI	Debug UART receive	1.8 V	
DBG_TXD	206	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

TP_I2C_SCL	243	OD	I2C serial clock	1.8 V	Should be externally pulled up to 1.8 V. If unused, keep them open.
TP_I2C_SDA	242	OD	I2C serial data		
PCM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM0_SYNC*	62	DIO	PCM0 data frame sync	1.8 V	In master mode, they are output signals. In slave mode, they are input signals.
PCM0_CLK*	63	DIO	PCM0 clock		
PCM0_DIN*	61	DI	PCM0 data input		If unused, keep them open.
PCM0_DOUT*	59	DO	PCM0 data output		
PCM1_SYNC	217	DIO	PCM1 data frame sync		In master mode, they are output signals. In slave mode, they are input signals.
PCM1_CLK	215	DIO	PCM1 clock		
PCM1_DIN	212	DI	PCM1 data input		If unused, keep them open.
PCM1_DOUT	211	DO	PCM1 data output		
PCIe Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE0_REFCLK_P	56	AO	PCIe0 reference clock (+)		Require differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly.
PCIE0_REFCLK_M	55	AO	PCIe0 reference clock (-)		
PCIE0_TX_M	50	AO	PCIe0 transmit (-)		
PCIE0_TX_P	49	AO	PCIe0 transmit (+)		
PCIE0_RX_M	52	AI	PCIe0 receive (-)		
PCIE0_RX_P	53	AI	PCIe0 receive (+)		
PCIE0_CLKREQ_N	281	DI	PCIe0 clock request	1.8 V	
PCIE0_RST_N	54	DO	PCIe0 reset		
PCIE0_WAKE_N	60	DI	PCIe0 wake up		
PCIE1_REFCLK_P	46	AO	PCIe1 reference clock (+)		Require differential impedance of 85 Ω.

PCIE1_REFCLK_M	44	AO	PCIe1 reference clock (-)		PCIe Gen 3 compliant. If unused, connect RX to GND directly.
PCIE1_TX0_M	34	AO	PCIe1 transmit (-)		
PCIE1_TX0_P	32	AO	PCIe1 transmit (+)		
PCIE1_RX0_M	38	AI	PCIe1 receive (-)		
PCIE1_RX0_P	40	AI	PCIe1 receive (+)		
PCIE1_CLKREQ_N	273	DI	PCIe1 clock request	1.8 V	
PCIE1_RST_N	27	DO	PCIe1 reset		
PCIE1_WAKE_N	30	DI	PCIe1 wake up		
PCIE2_REFCLK_P	29	AO	PCIe2 reference clock (+)		Require differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly. Not supported by RG500L-AR* and RG500L-JO*.
PCIE2_REFCLK_M	28	AO	PCIe2 reference clock (-)		
PCIE2_TX_M	25	AO	PCIe2 transmit (-)		
PCIE2_TX_P	26	AO	PCIe2 transmit (+)		
PCIE2_RX_M	22	AI	PCIe2 receive (-)		
PCIE2_RX_P	23	AI	PCIe2 receive (+)		
PCIE2_CLKREQ_N	21	DI	PCIe2 clock request	1.8 V	Not supported by RG500L-AR* and RG500L-JO*.
PCIE2_RST_N	18	DO	PCIe2 reset		
PCIE2_WAKE_N	270	DI	PCIe2 wake up		
PCIE3_REFCLK_P*	13	AO	PCIe3 reference clock (+)		Require differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly. Not supported by RG500L-AR* and RG500L-JO*.
PCIE3_REFCLK_M*	11	AO	PCIe3 reference clock (-)		
PCIE3_TX_M*	14	AO	PCIe3 transmit (-)		
PCIE3_TX_P*	16	AO	PCIe3 transmit (+)		
PCIE3_RX_M*	17	AI	PCIe3 receive (-)		
PCIE3_RX_P*	19	AI	PCIe3 receive (+)		
PCIE3_CLKREQ_N*	15	DI	PCIe3 clock request	1.8 V	Not supported by RG500L-AR* and RG500L-JO*.
PCIE3_RST_N*	269	DO	PCIe3 reset		

PCIE3_WAKE_N*	268	DI	PCIe3 wake up		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LSDI	102	DI	SPI serial input data	1.8 V	
LSA0	108	DO	Indicate transmission of data or command		
LSCE0B	105	DO	SPI chip select		
LSRSTB	422	DO	SPI reset		
LSCK	114	DO	SPI serial clock		
LSDA	111	DO	SPI serial output data		
PWM	88	DO	PWM output		For LCD only.
LCD_TE	99	DI	LCM tearing effect		
LCD_RST	93	DO	LCM reset		
SGMII Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MDIO_DATA	267	DIO	MDIO data	1.8 V	
MDIO_CLK	265	DO	MDIO clock		
EPHY0_INT_N	410	DI	SGMII0 interrupt		
EPHY0_RST_N	411	DO	SGMII0 reset		
EPHY1_INT_N	258	DI	SGMII1 interrupt		
EPHY1_RST_N	261	DO	SGMII1 reset		
SGMII0_RX_M	5	AI	SGMII0 receive (-)		Require differential impedance of 100 Ω. If unused, connect RX to GND directly.
SGMII0_RX_P	4	AI	SGMII0 receive (+)		
SGMII0_TX_P	1	AO	SGMII0 transmit (+)		
SGMII0_TX_M	2	AO	SGMII0 transmit (-)		
SGMII1_RX_M	260	AI	SGMII1 receive (-)		
SGMII1_RX_P	262	AI	SGMII1 receive (+)		

SGMII1_TX_P	264	AO	SGMII1 transmit (+)		
SGMII1_TX_M	263	AO	SGMII1 transmit (-)		
WWAN/WLAN Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_SYSRST_5G	271	DO	WLAN 5 GHz system reset	1.8 V	
WLAN_2.4G_EN*	272	DO	WLAN 2.4 GHz function enable control		Reserved.
WLAN_SYSRST_2.4G	274	DO	WLAN 2.4 GHz system reset		
WLAN_5G_EN*	406	DO	WLAN 5 GHz function enable control		Reserved.
BT_ACT_TXD [10]	36	DO	Coexistence interface for WWAN and 5 GHz Wi-Fi		
BT_PRI_RXD [10]	275	DO	Coexistence interface for WWAN and 5 GHz Wi-Fi		
WLAN_ACT	39	DI	Coexistence interface for WWAN and 5 GHz Wi-Fi		Used for WWAN/WLAN coexistence by default.
PTA_TX	279	DO	Coexistence interface for WWAN and 2.4 GHz Wi-Fi		
PTA_RX	278	DO	Coexistence interface for WWAN and 2.4 GHz Wi-Fi		
GPIO_15	280	DI	Coexistence interface for WWAN and 2.4 GHz Wi-Fi		
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT0	121	AIO	Antenna 0 interface		50 Ω impedance.

[10] Please note that this pin is for WWAN and Wi-Fi coexistence, not for WWAN and Bluetooth coexistence.

ANT1	130	AIO	Antenna 1 interface		50 Ω impedance. Not supported by RG500L-JO*.
ANT2	139	AI	Antenna 2 interface		50 Ω impedance.
ANT3	148	AI	Antenna 3 interface		
ANT4	157	AI	Antenna 4 interface		
ANT5	166	AI	Antenna 5 interface		50 Ω impedance. Not supported by RG500L-JO*.
ANT6	175	AIO	Antenna 6 interface		50 Ω impedance.
ANT7	184	AIO	Antenna 7 interface		
ANT_GNSS	193	AI	GNSS antenna interface		50 Ω impedance. Not supported by RG500L-LA, RG500L-AR* and RG500L-JO*.
SPI Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI0_CS*	255	DO	SPI0 chip select	1.8 V	
SPI0_CLK*	257	DO	SPI0 clock		
SPI0_MOSI*	259	DO	SPI0 master-out slave-in		
SPI0_MISO*	256	DI	SPI0 master-in salve-out		
SPI3_CS	218	DO	SPI3 chip select		Recommended for SLIC IC communication.
SPI3_CLK	220	DO	SPI3 clock		
SPI3_MOSI	223	DO	SPI3 master-out slave-in		
SPI3_MISO	221	DI	SPI3 master-in salve-out		
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	241	AI	General-purpose ADC interface	1.78 V	Max input 1.78 V. If unused, connect it to GND directly.

ADC1	135	AI	General-purpose ADC interface	1.45 V	Max input 1.45 V. If unused, connect them to GND directly.
ADC2	138	AI	General-purpose ADC interface		
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	81	DI	Force the module into emergency download mode	1.8 V	
SLIC_RST_N	208	DO	SLIC reset		
SLIC_INT_N	214	DI	SLIC interrupt		
TP_RST	237	DO	TP reset		
TP_INT	405	DI	TP interrupt		
BT_EN*	240	DO	Bluetooth enable control		Reserved.
I2S0_MCK	209	DO	I2S0 master clock		
Reserved Pins					
Pin Name	**Pin No.**				
RESERVED	35, 37, 41, 43, 58, 84, 87, 89, 91, 92, 94, 95, 97, 98, 100, 101, 103, 150, 153, 165, 171, 174, 177, 183, 186, 189, 199, 282–298, 395–399, 413–417, 419, 420, 423–428				
GND					
Pin Name	**Pin No.**				
GND	3, 6, 10, 12, 20, 24, 31, 33, 42, 47, 51, 57, 73, 78, 86, 90, 96, 104, 106, 113, 115–120, 122–129, 131–134, 136, 137, 140–147, 149, 151, 152, 154–156, 158–164, 167–170, 172, 173, 176, 178–182, 185, 187, 188, 190–192, 194–198, 224, 226–228, 231, 234, 246, 266, 299–394, 400–404, 407–409, 412, 418, 421, 429, 430				

2.5. EVB

To help you to develop applications with the module conveniently, Quectel supplies an evaluation board (RG500L EVB), USB cable, earphone, antennas, and other peripherals to control or to test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

The table below outlines operating modes of the module.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module is registered on the network and ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command can set the module to the minimum functionality mode. In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** command can set the module to airplane mode. In this case, RF function is invalid.	
Sleep Mode	In this mode, current consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging, SMS, voice call and TCP/UDP data from network.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. Operating voltage (connected to VBAT_RF1 and VBAT_BB) remains applied.	

NOTE

For more details about **AT+CFUN**, see ***Chapter 9.1***.

3.2. Sleep Mode

DRX of the module is able to reduce the current consumption to a minimum value during sleep mode, and DRX cycle index values are broadcasted by the wireless network. The diagram below illustrates the relationship between the DRX run time and the current consumption of the module in this mode. The longer the DRX cycle is, the lower the current consumption will be.

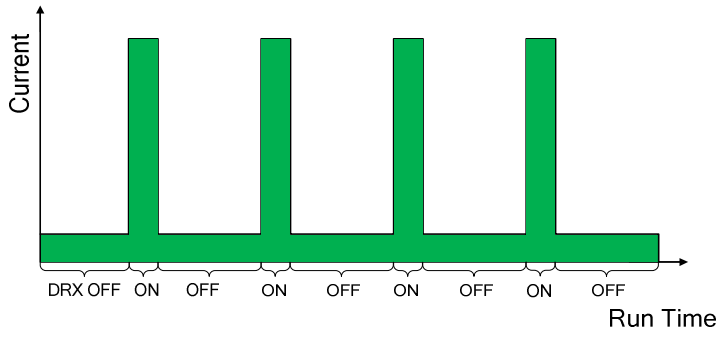


Figure 2: DRX Run Time and Current Consumption in Sleep Mode

3.2.1. UART Application Scenario

If the host communicates with the module via UART interface, the following precondition should be met to set the module into sleep mode:

- Execute **AT+QSCLK=1** command to enable sleep mode. For more details about **AT+QSCLK**, see ***Chapter 9.2***.

3.2.2. USB Application Scenario

If the host communicates with the module via USB interface, the following precondition should be met to set the module into sleep mode:

- Execute **AT+QSCLK=1** command to enable sleep mode. For more details about **AT+QSCLK**, see ***Chapter 9.2***.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via **AT+CFUN**.

AT+CFUN=<fun> command provides choices of the functionality level by setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality (Disable RF function and (U)SIM function).
- **AT+CFUN=1:** Full functionality (Default).
- **AT+CFUN=4:** Airplane mode (Disable RF function).

NOTE

The execution of **AT+CFUN** command will not affect GNSS function. For more details about **AT+CFUN**, see ***Chapter 9.1***.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides 7 VBAT pins dedicated to the connection with the external power supply and provides power supply for external GPIO's pull-up circuits with VDD_EXT. There are two separate voltage domains for VBAT and one voltage for external circuits.

- Four VBAT_RF1 pins for RF part.
- Three VBAT_BB pins for baseband part.
- One VDD_EXT pin for external GPIO's pull-up circuits

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Comment
VBAT_BB	235, 236, 238	PI	Power supply for the module's baseband part	
VBAT_RF1	229, 230, 232, 233	PI	Power supply for the module's RF part	
VDD_EXT	66	PO	Provide 1.8 V for external circuit	Power supply for external GPIO's pull-up circuits.

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 4.5 A at least. If the voltage difference between input and output is not too high, it is suggested that an LDO should be used to supply power to the module. If there is a big voltage difference between input and the desired output VBAT, a buck converter is preferred as the power supply.

The following figure illustrates a reference design for +5 V input power source.

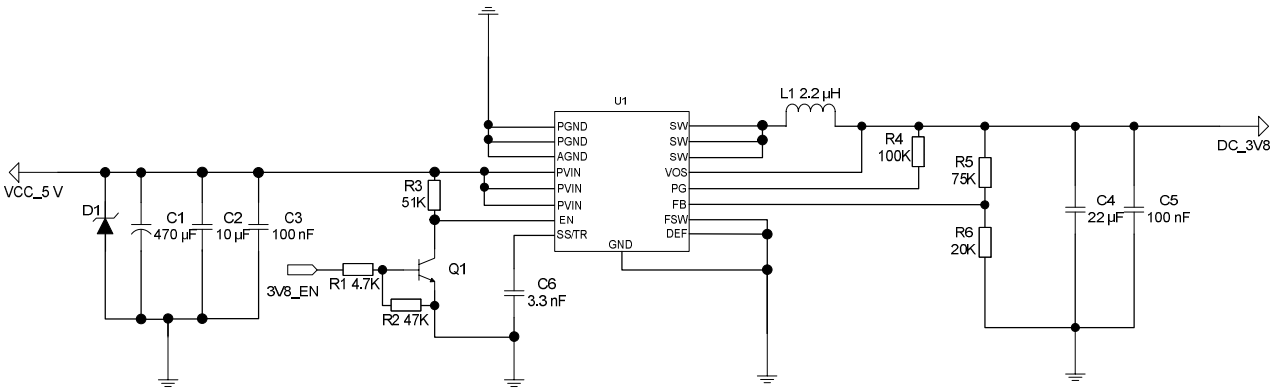


Figure 3: Reference Design of Power Supply

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage will never drop below 3.3 V.

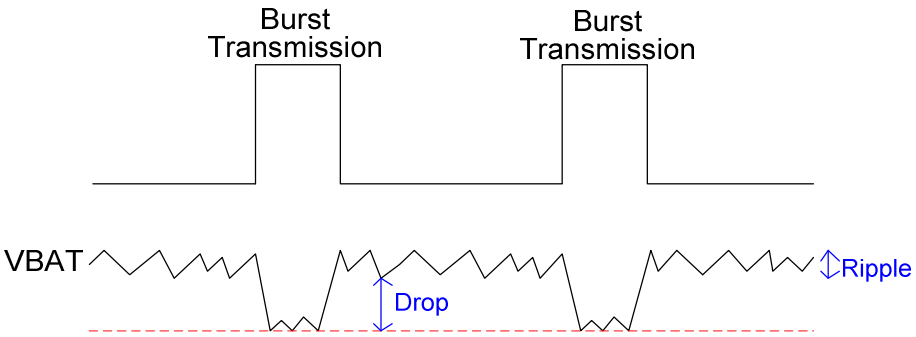


Figure 4: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 470 µF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use ceramic capacitors for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source and can be expanded to two sub paths with the star structure. The width of VBAT_BB trace should be no less than 2.5 mm. The width of VBAT_RF trace should be no less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to ensure the stability of the power supply, it is necessary to add a high-power TVS diode at the front end of the power supply. Reference circuit is shown as below:

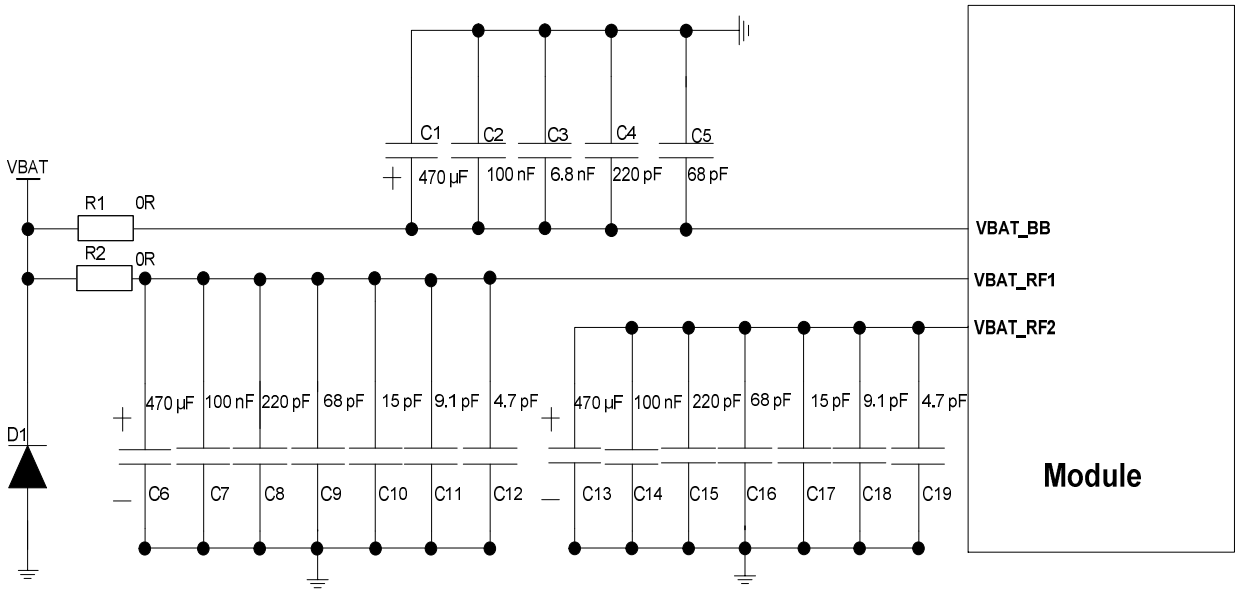


Figure 5: Star Structure of the Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or PON_1 can you cut off the power supply.

3.5. Turn On

3.5.1. Turn On the Module with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turn on/off the module	Internally pulled up to 1.8 V. Active low.

When the module is in power-off mode, you can turn it on to make it enter normal operation mode by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control PWRKEY.

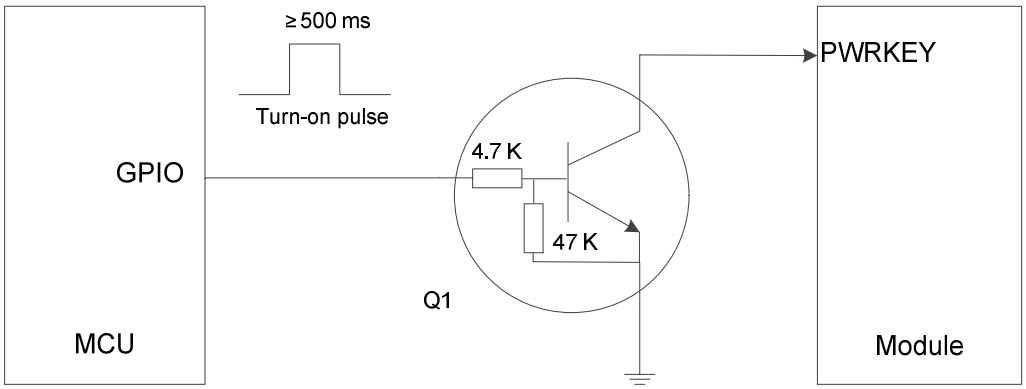


Figure 6: Reference Circuit of Turning On the Module with Driving Circuit

Another way to control PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may be generated from finger. Therefore, a TVS component shall be placed near the button for ESD protection.

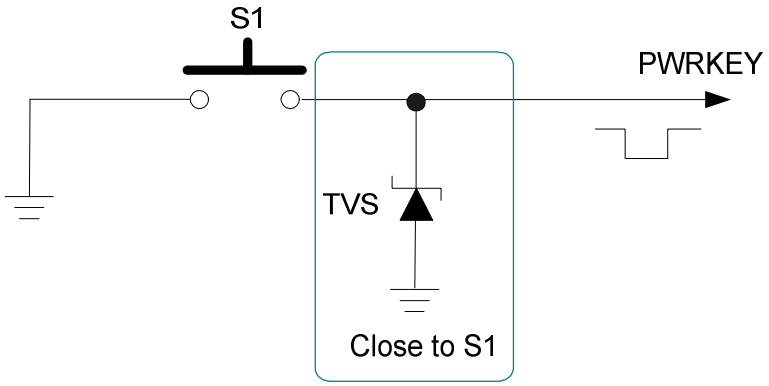


Figure 7: Reference Circuit of Turning On the Module with Keystroke

The turn-on scenario is illustrated in the following figure.

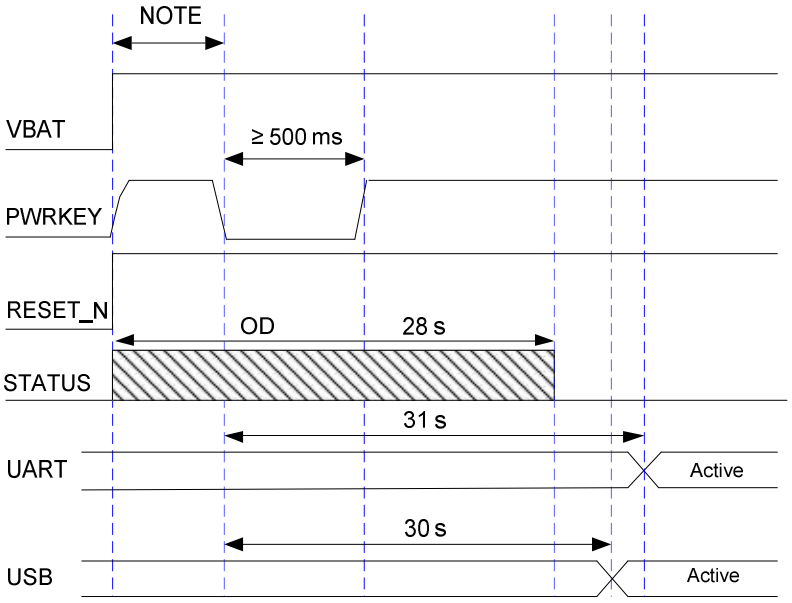


Figure 8: Timing of Turning On the Module

NOTE

1. Please ensure that VBAT is stable for at least 30 ms before pulling down PWRKEY.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.
3. If PWRKEY is kept low for more than 8 s after turning on the module, the module will reset repeatedly.

3.5.2. Turn On the Module with PON_1

When the module is in power-down mode, you can turn it on to normal mode by driving the PON_1 pin high.

Table 10: Pin Definition of PON_1

Pin Name	Pin No.	I/O	Description
PON_1	9	DI	Turn on/off the module

3.6. Turn Off

You can use the following ways to turn off the module.

3.6.1. Turn Off the Module with PWRKEY

You can turn off the module by driving PWRKEY low for at least 1000 ms and then releasing it.

The turn-off scenario is illustrated in the following figure.

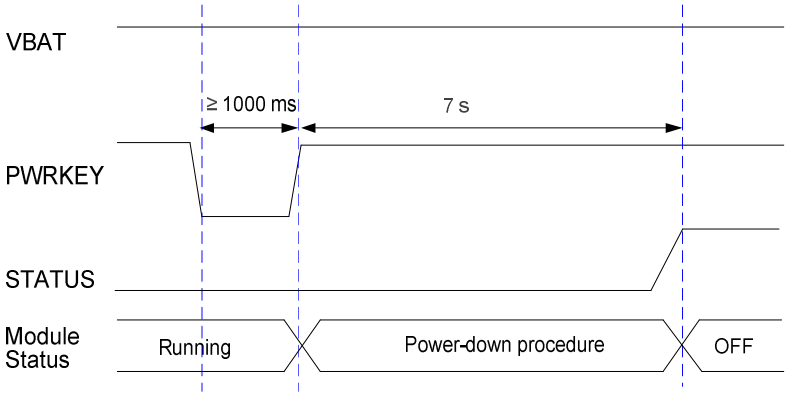


Figure 9: Timing of Turning Off the Module

3.6.2. Turn Off the Module with PON_1

You can turn off the module by driving PON_1 low.

NOTE

1. When turning off the module with PON_1, please keep PWRKEY at a high level after the execution of power-off. Otherwise, the module will be turned on again after power-off.
2. When USB_VBUS is in place, the module always remains in the power-on state.
3. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or PON_1 can you cut off the power supply.

3.7. Reset

You can reset the module by driving RESET_N low for at least 250–550 ms* and then releasing it. The

RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	8	DI	Reset the module	Internally pulled up to 1.8 V. Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

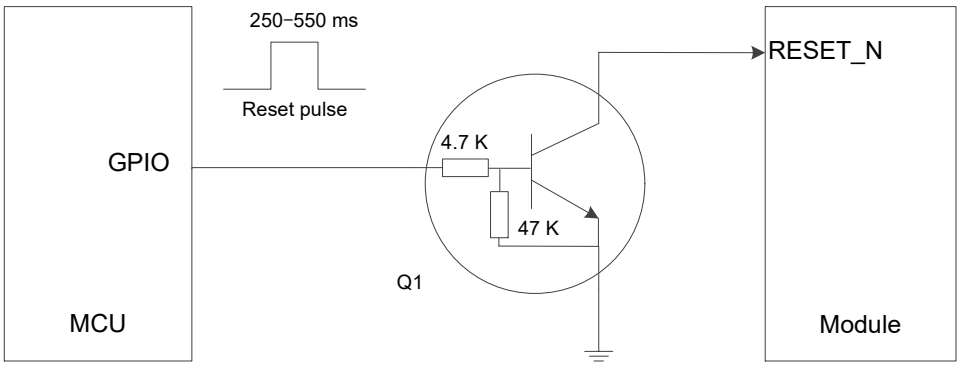


Figure 10: Reference Circuit of RESET_N with Driving Circuit

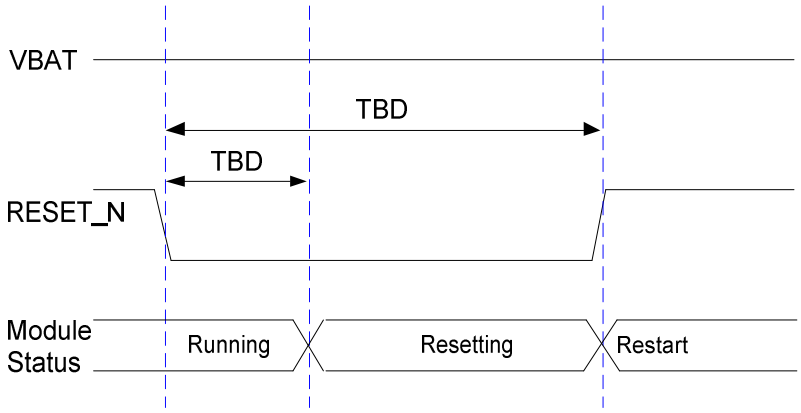


Figure 11: Timing of Resetting the Module

NOTE

1. Use RESET_N only when you fail to turn off the module with PWRKEY or PON_1.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

4 Application Interfaces

4.1. USB Interface

The module provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0/2.0 specifications and supports SuperSpeed (5 Gbps) on USB 3.0, high-speed (480 Mbps) and full-speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA* sentence output, software debugging and firmware upgrade.

Pin definition of the USB interface is as follows:

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	82	AI	USB connection detect	Used for USB connection detection (disabled by default). Cannot be used for power supply.
USB_DP	83	AIO	USB differential data (+)	Require differential impedance of 90 Ω.
USB_DM	85	AIO	USB differential data (-)	
USB_SS_TX_P	76	AO	USB 3.0 super-speed transmit (+)	Require differential impedance of 90 Ω. If unused, connect RX to GND directly.
USB_SS_TX_M	74	AO	USB 3.0 super-speed transmit (-)	
USB_SS_RX_P	79	AI	USB 3.0 super-speed receive (+)	
USB_SS_RX_M	77	AI	USB 3.0 super-speed receive (-)	
USB_ID	75	DI	USB ID detect	
OTG_PWR_EN	80	DO	OTG power control	

It is recommended to reserve test points for debugging and firmware upgrading in your design.

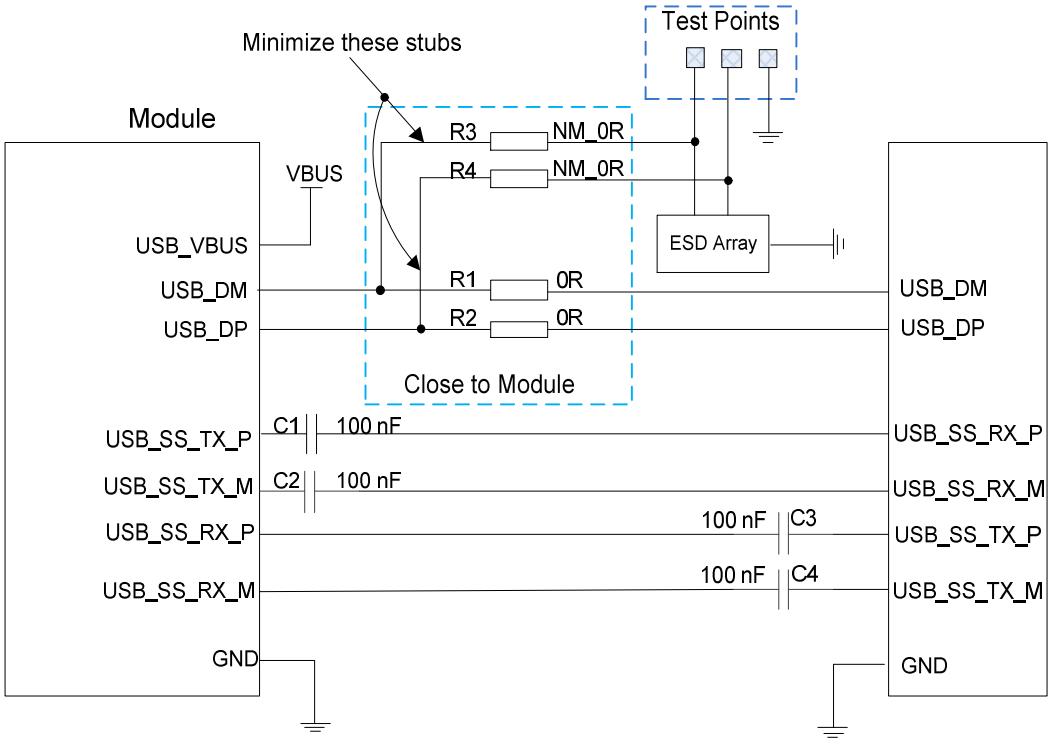


Figure 12: Reference Circuit of USB Interface

To ensure the signal integrity of USB data traces, you must place R1, R2, R3, R4, C1 and C2 close to the module, C3 and C4 close to the device, and keep these resistors close to each other. Keep the extra stubs of traces as short as possible.

To meet the USB specifications, the following principles should be complied with when designing the USB interface,

- It is important to route the USB signal traces as differential pairs with ground surrounded. The impedance of USB 2.0/3.0 differential trace is 90 Ω.
- For USB 2.0 signal traces, length matching within the differential data pair (between USB_DM and USB_DP) should be less than 0.5 mm. For USB 3.0 signal traces, length matching within each differential data pair (within TX or RX) should be less than 0.125 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data traces, so please pay attention to the selection of the device. Typically, the stray capacitance should be less than 3.0 pF for USB 2.0, and less than 0.5 pF for USB 3.0.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces respectively.

For more details about the USB specifications, please visit http://www.usb.org/home.

NOTE

1. Currently only USB 2.0 interface supports firmware upgrade.
2. When USB_VBUS is in place, the module always remains in the power-on state.

4.2. (U)SIM Interfaces

The (U)SIM interface circuitry meets *ETSI* and *IMT-2000* requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported, and Dual SIM Single Standby function is supported.

Table 13: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description
USIM1_VDD	245	PO	(U)SIM1 card power supply
USIM1_DATA	248	DIO	(U)SIM1 card data
USIM1_CLK	247	DO	(U)SIM1 card clock
USIM1_RST	244	DO	(U)SIM1 card reset
USIM1_DET	249	DI	(U)SIM1 card hot-plug detect
USIM2_VDD	250	PO	(U)SIM2 card power supply
USIM2_DATA	251	DIO	(U)SIM2 card data
USIM2_CLK	253	DO	(U)SIM2 card clock
USIM2_RST	254	DO	(U)SIM2 card reset
USIM2_DET	252	DI	(U)SIM2 card hot-plug detect

The module supports (U)SIM card hot-plug via the USIM_DET pin, which is a level-triggered pin.

4.2.1. Normally Closed (U)SIM Card Connector

With a normally closed (U)SIM card connector, USIM_DET is normally short-circuited to ground when there is no (U)SIM card inserted. (U)SIM card insertion will drive USIM_DET from low to high level, and the removal of it will drive USIM_DET from high to low level.

- When the (U)SIM is absent, CD is short-circuited to ground and USIM_DET is at low level.
- When the (U)SIM is inserted, CD is open from ground and USIM_DET is at high level.

The following figure shows a reference design of (U)SIM interface with a normally closed (U)SIM card connector.

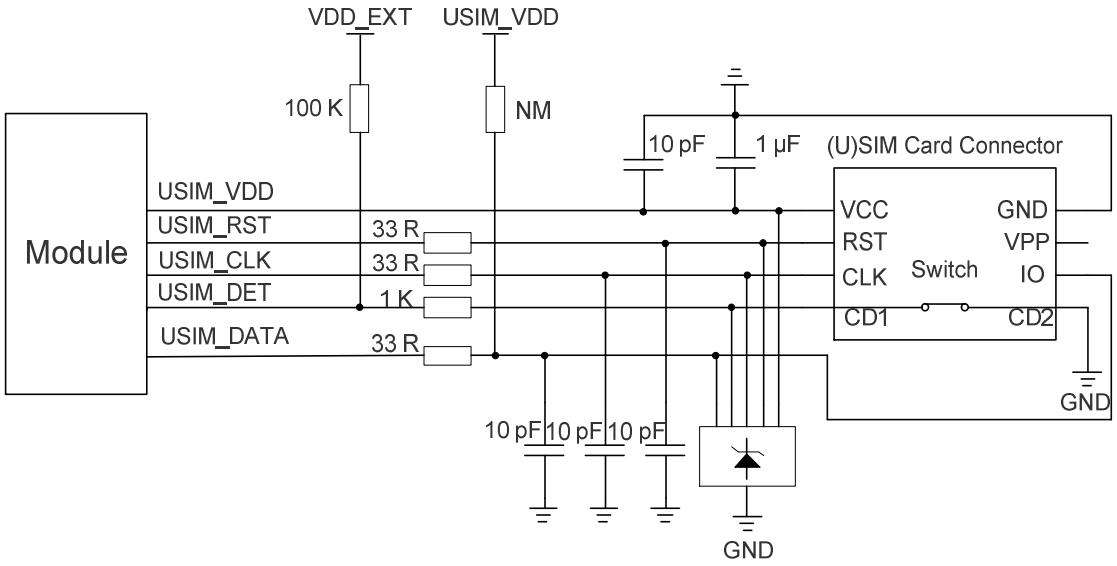


Figure 13: Reference Circuit of Normally Closed (U)SIM Card Connector

4.2.2. Normally Open (U)SIM Card Connector

With a normally open (U)SIM card connector, USIM_DET is normally open when there is no (U)SIM card inserted. (U)SIM card insertion will drive USIM_DET from high to low level, and the removal of it will drive USIM_DET from low to high level.

- When the (U)SIM is absent, CD1 is open from CD2 and USIM_DET is at high level.
- When the (U)SIM is inserted, CD1 is short-circuited to ground and USIM_DET is at low level.

The following figure shows a reference design of (U)SIM interface with a normally open (U)SIM card connector.

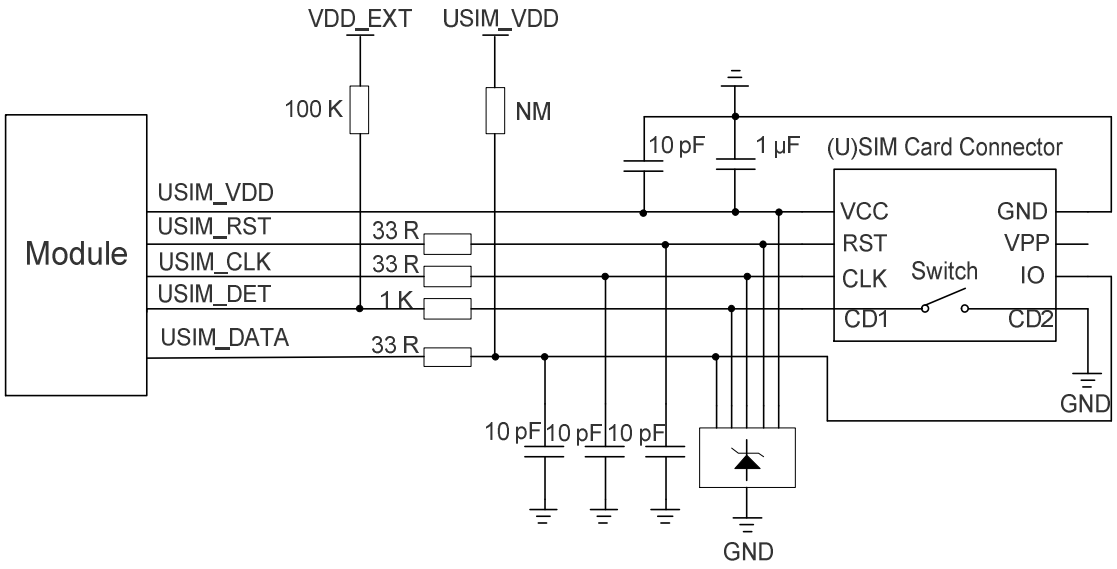


Figure 14: Reference Circuit of Normally Open (U)SIM Card Connector

4.2.3. (U)SIM Card Connector Without Hot-Plug

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected.

A reference circuit for (U)SIM card interface with a 6-pin (U)SIM card connector without hot-plug function is illustrated in the following figure.

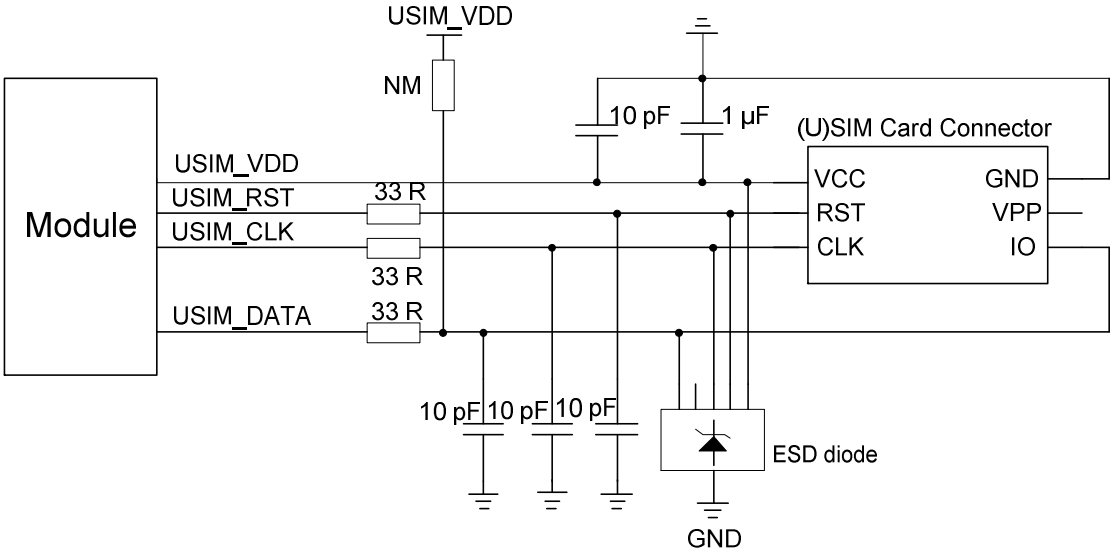


Figure 15: Reference Circuit of a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card interface in applications, please follow the criteria below in (U)SIM circuit design.

- Keep (U)SIM card connector as close as possible to the module. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signal traces away from RF and VCC traces.
- To avoid crosstalk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- To offer better ESD protection, it is recommended to add a TVS array with a parasitic capacitance not exceeding 45 pF. The 33 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection. The 10 pF capacitors are used to filter out RF interference.
- Reserve a 1 μF shunt capacitor on the power rails of (U)SIM and place this capacitor close to the (U)SIM connector.

4.3. I2C Interface

The module provides one I2C interface. As an open drain output, I2C interface should be pulled up to 1.8 V.

Table 14: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
TP_I2C_SCL	243	OD	I2C serial clock	Should be externally pulled up to 1.8 V. If unused, keep them open.
TP_I2C_SDA	242	OD	I2C serial data	

4.4. PCM Interfaces

The module provides two PCM interfaces. The key features of the PCM interfaces are listed below:

- Used for audio function with external SLIC
- Supports long frame synchronization/short frame synchronization
- Supports master and slave modes, but must be the master in long frame synchronization

Table 15: Pin Definition of PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM0_SYNC*	62	DIO	PCM0 data frame sync	In master mode, they are output signals. In slave mode, they are input signals.
PCM0_CLK*	63	DIO	PCM0 clock	
PCM0_DIN*	61	DI	PCM0 data input	If unused, keep them open.
PCM0_DOUT*	59	DO	PCM0 data output	
PCM1_SYNC	217	DIO	PCM1 data frame sync	In master mode, they are output signals. In slave mode, they are input signals.
PCM1_CLK	215	DIO	PCM1 clock	
PCM1_DIN	212	DI	PCM1 data input	If unused, keep them open.
PCM1_DOUT	211	DO	PCM1 data output	

NOTE

PCM1 is used for SLIC by default.

4.5. UART Interfaces

The module provides three UART interfaces and the following table shows their features:

Table 16: UART Information

UART Types	Baud Rate	Functions
Main UART interface	115200 bps	AT command communication and data transmission
Debug UART interface	921600 bps	Linux console and log output
Bluetooth UART interface	115200 bps	Bluetooth communication

Table 17: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	201	DO	Clear to send signal from the module	Connect to the peripheral's CTS.
MAIN_RTS	203	DI	Request to send signal to the module	Connect to the peripheral's RTS.
MAIN_RXD	202	DI	Main UART receive	
MAIN_TXD	200	DO	Main UART transmit	
BT_TXD	45	DO	Bluetooth UART transmit	
BT_RXD	276	DI	Bluetooth UART receive	
BT_RTS	48	DI	Request to send signal to the module	Connect to the peripheral's RTS.
BT_CTS	277	DO	Clear to send signal from the module	Connect to the peripheral's CTS.
DBG_RXD	205	DI	Debug UART receive	
DBG_TXD	206	DO	Debug UART transmit	

The following figure illustrates the reference design for Bluetooth UART interface connection between RG500L series and Wi-Fi/Bluetooth module.

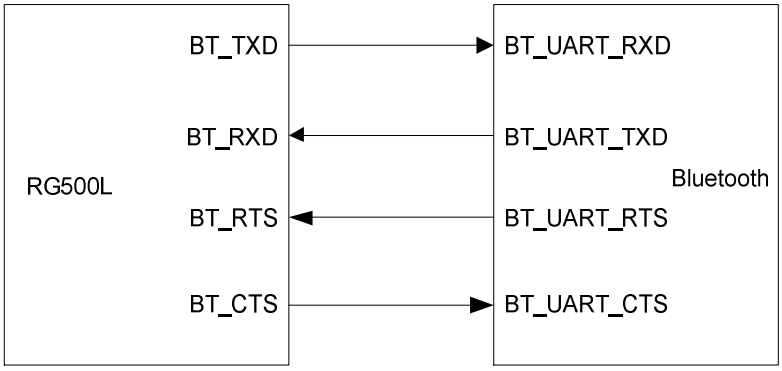


Figure 16: Bluetooth UART Interface Connection

The module provides 1.8 V UART interfaces. A level-shifting circuit should be used if the application is equipped with a 3.3 V UART interface. The following figure shows a reference design with voltage-level translator chip.

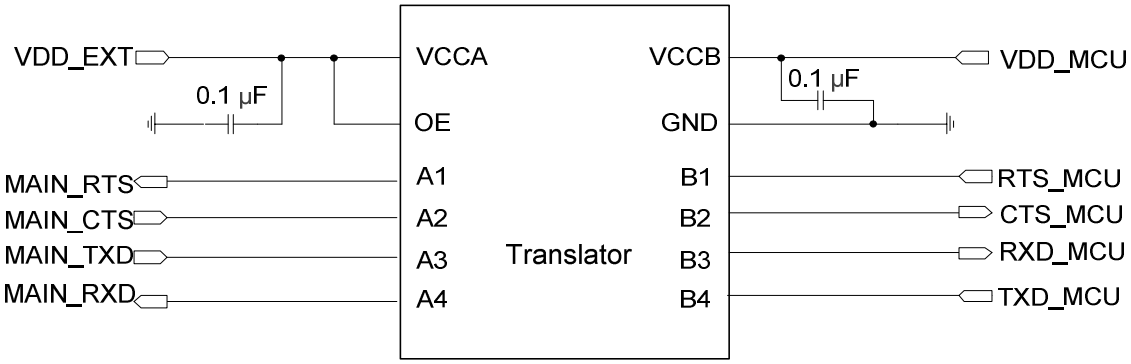


Figure 17: Reference Circuit with Level Translator Chip

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

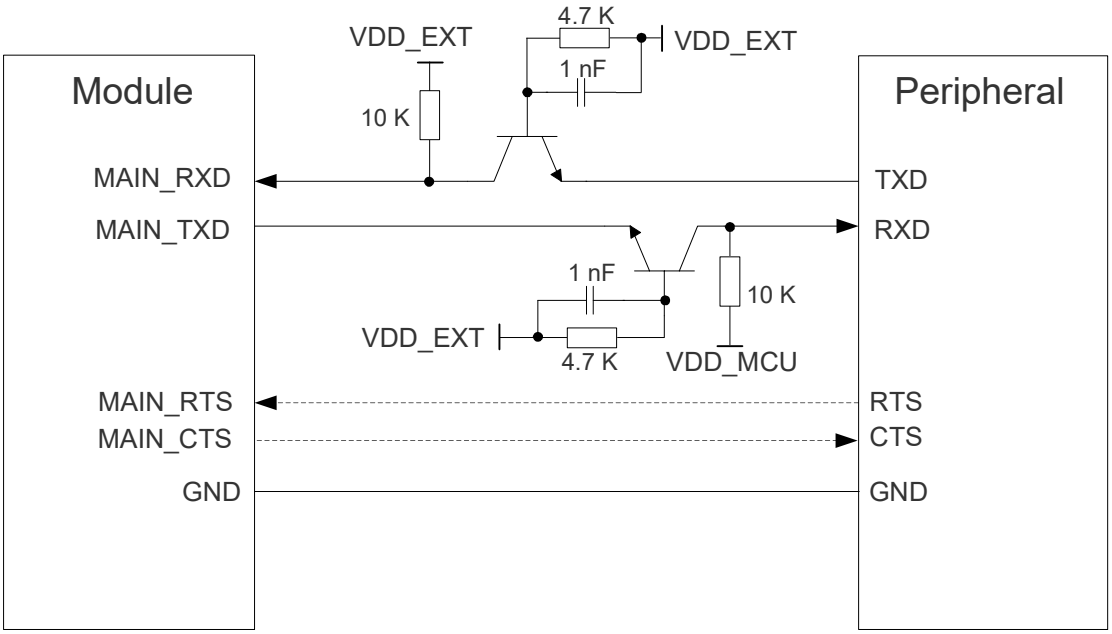


Figure 18: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the peripheral's CTS, and the module RTS is connected to the peripheral's RTS.

4.6. SDIO Interface

For RG500L-EU/RG500L-NA/RG500L-LA:

- Supports one SD 3.0 protocol compliant SDIO interface.

For RG500L-AR*/RG500L-JO*:

- SDIO interface is not supported.

Table 18: Pin Definition of SDIO Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	67	DO	SD card clock	Only used for SD card. Not supported by RG500L-AR* and RG500L-JO*.
SD_CMD	64	DIO	SD card command	
SD_DATA0	65	DIO	SDIO data bit 0	
SD_DATA1	71	DIO	SDIO data bit 1	
SD_DATA2	70	DIO	SDIO data bit 2	
SD_DATA3	68	DIO	SDIO data bit 3	
SD_DET	69	DI	SD card hot-plug detect	
SDIO_PU_VDD	72	PO	SD card IO pull-up power supply	Not supported by RG500L-AR* and RG500L-JO*.

The following figure illustrates a reference design of SD card interface with the module.

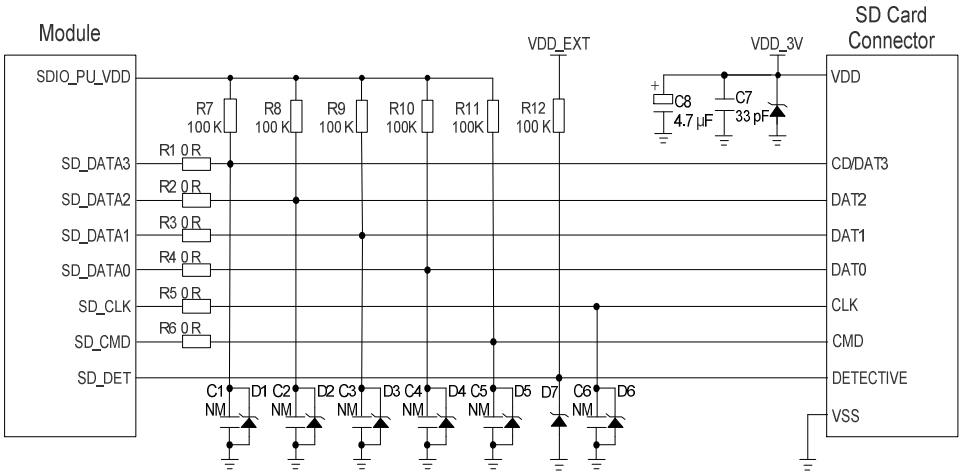


Figure 19: Reference Circuit of SD Card Interface

To ensure communication performance with SD card, the following design principles should be complied with:

- The voltage range of SD card power supply VDD_3V is 2.7–3.6 V and a sufficient current of up to 0.8 A should be provided. SDIO_PU_VDD is the SDIO bus power domain, which can be used for SD card IO signal pull-up.
- To avoid jitter of bus, pull up SD_CMD and SD_DATA to SDIO_PU_VDD with R7–R11. Value of these resistors can be 10–100 kΩ and the recommended value is 100 kΩ.
- To improve signal quality, it is recommended to add 0 Ω resistors R1 to R6 in series between the module and the SD card connector. The bypass capacitors C1 to C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the connector.
- For good ESD protection, it is recommended to add a TVS diode with capacitance value less than 3 pF on each SD card pins.
- It is important to route the SDIO signal traces with ground surrounded. The impedance of SDIO data trace is 50 Ω (±10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc., as well as noisy signals such as clock signals, DC-DC signals, etc.
- It is recommended to keep the trace length difference between SD_CLK and SD_DATA/CMD less than 7.7 mm and the total routing length less than 102 mm. The total trace length inside the module is 18 mm, so the exterior total trace length should be less than 84 mm.
- Ensure the adjacent trace spacing is two times the trace width and the load capacitance of SDIO bus should be less than 5 pF.

NOTE

For SD 3.0 SDR104 mode, a sufficient current of up to 800 mA and a 4.7 μF capacitor for the power supply is necessary.

4.7. ADC Interfaces

The module provides three Analog-to-Digital Converter (ADC) interfaces. To improve the accuracy of ADC, the traces of ADC interfaces should be surrounded by ground.

Table 19: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	241	AI	General-purpose ADC interface	Max input 1.78 V. If unused, connect it to GND directly.

ADC1	135	AI	General-purpose ADC interface	Max input 1.45 V. If unused, connect them to GND directly.
ADC2	138	AI	General-purpose ADC interface	

The voltage value on ADC pins can be read via **AT+QADC=<port>** command:

- **AT+QADC=0:** read the voltage value on ADC0
- **AT+QADC=1:** read the voltage value on ADC1
- **AT+QADC=2:** read the voltage value on ADC2

For more details about **AT+QADC**, see ***Chapter 9.3***.

The resolution is 15 bits for ADC0 and 12 bits for ADC1 and ADC2. The following table describes the voltage range of the ADC interfaces.

Table 20: Voltage Range of ADC Interfaces

ADC Interfaces	Min.	Max.	Unit
ADC0	0.04	1.78	V
ADC1	0.05	1.45	V
ADC2	0.05	1.45	V

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use voltage divider circuit for ADC application.

4.8. LCM Interface

The module provides an LCM interface, the pin definition of the LCM interface is shown below.

Table 21: Pin Definition of LCM Interface

Pin Name	Pin No.	I/O	Description
LSDI	102	DI	SPI serial input data
LSA0	108	DO	Indicate transmission of data or command
LSCE0B	105	DO	SPI chip select
LSRSTB	422	DO	SPI reset
LSCK	114	DO	SPI serial clock
LSDA	111	DO	SPI serial output data
PWM	88	DO	PWM output (For LCD only)
LCD_TE	99	DI	LCM tearing effect
LCD_RST	93	DO	LCM reset

The following figures show the reference design for LCM interface.

Figure 20: Reference Circuit Design for LCM Interface

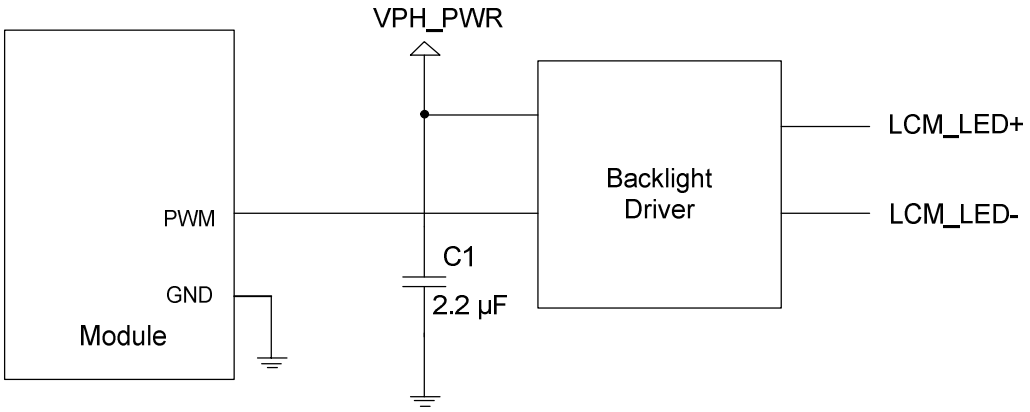


Figure 21: Reference Circuit of LCM External Backlight Driver

4.9. SGMII Interfaces

The module includes two integrated Ethernet MAC with two SGMII interfaces and one MDIO management interface. Key features of the SGMII interfaces are shown below:

- *IEEE 802.3* compliant
- Full duplex mode for 10/100/1000/2500 Mbps
- Can be connected to an external Ethernet Switch or PHY, such as MT7531AE and RTL8221B
- The MDIO management interface and SGMII interrupt/reset signals support 1.8 V power domain

Table 22: Pin Definition of SGMII Interfaces

Pin Name	Pin No.	I/O	Description	Comment
MDIO_DATA	267	DIO	MDIO data	
MDIO_CLK	265	DO	MDIO clock	
EPHY0_INT_N	410	DI	SGMII0 interrupt	
EPHY0_RST_N	411	DO	SGMII0 reset	
EPHY1_INT_N	258	DI	SGMII1 interrupt	
EPHY1_RST_N	261	DO	SGMII1 reset	
SGMII0_RX_M	5	AI	SGMII0 receive (-)	Require differential impedance of 100 Ω. If unused, connect
SGMII0_RX_P	4	AI	SGMII0 receive (+)	

SGMII0_TX_P	1	AO	SGMII0 transmit (+)	RX to GND directly.
SGMII0_TX_M	2	AO	SGMII0 transmit (-)	
SGMII1_RX_M	260	AI	SGMII1 receive (-)	
SGMII1_RX_P	262	AI	SGMII1 receive (+)	
SGMII1_TX_P	264	AO	SGMII1 transmit (+)	
SGMII1_TX_M	263	AO	SGMII1 transmit (-)	

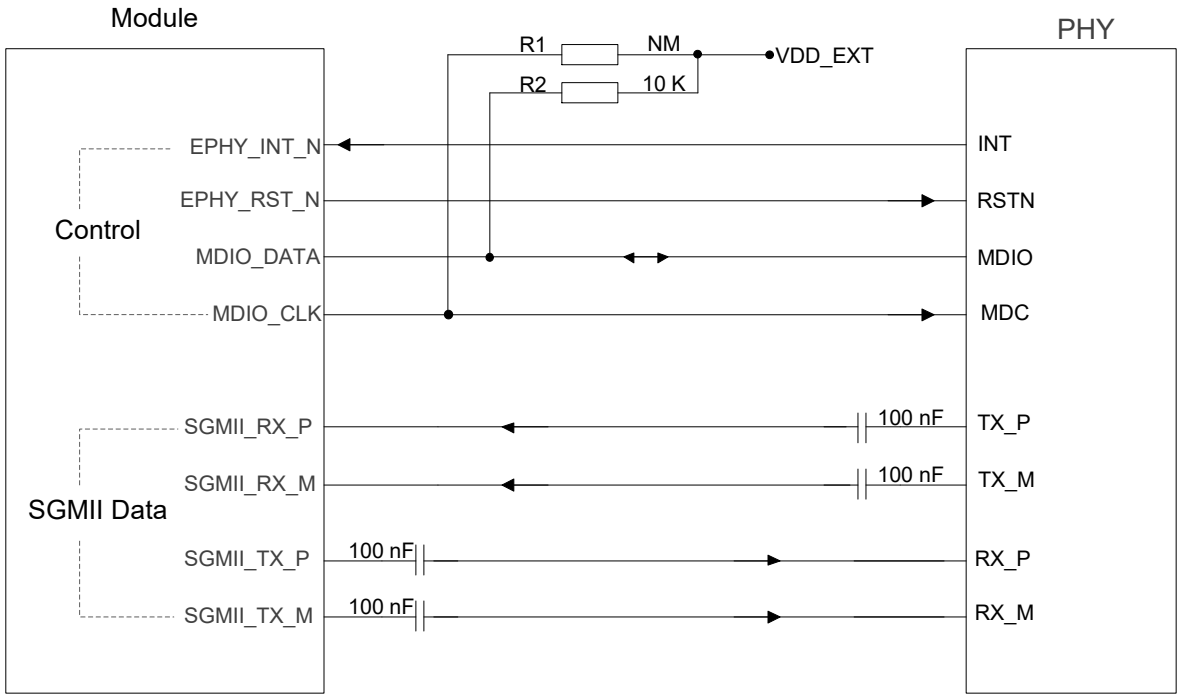


Figure 22: Reference Circuit of SGMII Interface with PHY Application

To enhance the reliability and availability of customers' application, please follow the criteria below in the Ethernet PHY circuit design:

- Keep SGMII data and control signals away from RF and VBAT traces.
- Keep the maximum trace length less than 150 mm and keep length matching within each differential pair less than 0.125 mm.
- The differential impedance of SGMII data traces is 100 Ω ±10%.
- To minimize crosstalk, the distance between separate adjacent pairs on the same layer must be equal to or larger than 1 mm.
- Less than 2 vias should be designed in each differential pair.
- Reserve enough GND planes between MDC and MDIO to prevent crosstalk.
- 0.1 μF AC coupling capacitors should be placed close to the transmitter source.

4.10. SPI Interfaces

The module provides two SPI interfaces which support slave mode* and master mode with a maximum clock frequency of up to 52 MHz.

Table 23: Pin Definition of SPI Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SPI0_CS*	255	DO	SPI0 chip select	
SPI0_CLK*	257	DO	SPI0 clock	
SPI0_MOSI*	259	DO	SPI0 master-out slave-in	
SPI0_MISO*	256	DI	SPI0 master-in salve-out	
SPI3_CS	218	DO	SPI3 chip select	Recommended for SLIC IC communication.
SPI3_CLK	220	DO	SPI3 clock	
SPI3_MOSI	223	DO	SPI3 master-out slave-in	
SPI3_MISO	221	DI	SPI3 master-in salve-out	

The module provides 1.8 V SPI interfaces. A voltage-level translator between the module and the host should be used if the application is equipped with a 3.3 V processor or device interface.

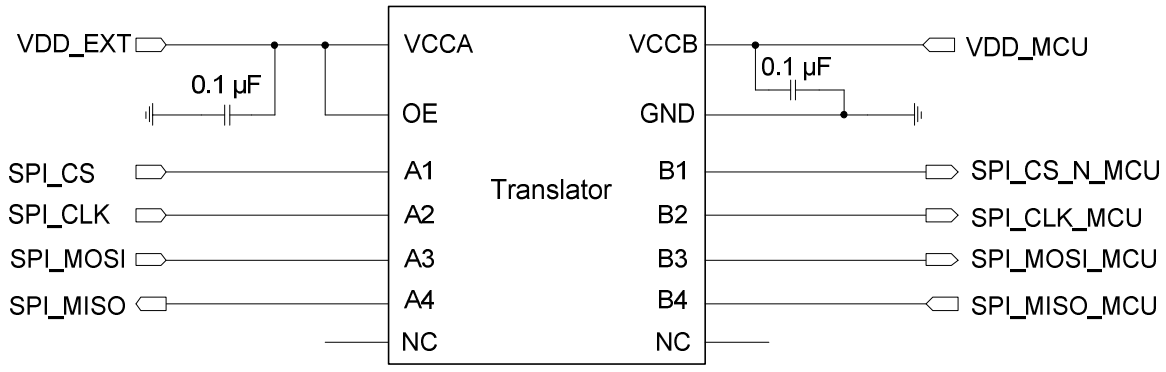


Figure 23: Reference Circuit of SPI Interface with a Level Translator

4.11. PCIe Interfaces

The module provides integrated PCIe (Peripheral Component Interconnect Express) interfaces which follow *PCI Express Base Specification Revision 3.0*. The key features of the PCIe interfaces are listed below:

- *PCI Express Base Specification Revision 3.0* compliant
- Data rate at 8 Gbps per lane
- Only supports Root Complex mode
- Can be used to connect to an external Ethernet IC (MAC and PHY) or WLAN IC
- **RG500L-EU/RG500L-NA/RG500L-LA**: Supports four PCIe interfaces
  RG500L-AR*/RG500L-JO*: Only supports PCIe0 and PCIe1 interfaces

Table 24: Pin Definition of PCIe Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCIE0_REFCLK_P	56	AO	PCIe0 reference clock (+)	Require differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly.
PCIE0_REFCLK_M	55	AO	PCIe0 reference clock (-)	
PCIE0_TX_M	50	AO	PCIe0 transmit (-)	
PCIE0_TX_P	49	AO	PCIe0 transmit (+)	
PCIE0_RX_M	52	AI	PCIe0 receive (-)	
PCIE0_RX_P	53	AI	PCIe0 receive (+)	
PCIE0_CLKREQ_N	281	DI	PCIe0 clock request	
PCIE0_RST_N	54	DO	PCIe0 reset	
PCIE0_WAKE_N	60	DI	PCIe0 wake up	
PCIE1_REFCLK_P	46	AO	PCIe1 reference clock (+)	Require differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly.
PCIE1_REFCLK_M	44	AO	PCIe1 reference clock (-)	
PCIE1_TX0_M	34	AO	PCIe1 transmit (-)	
PCIE1_TX0_P	32	AO	PCIe1 transmit (+)	
PCIE1_RX0_M	38	AI	PCIe1 receive (-)	

PCIE1_RX0_P	40	AI	PCIe1 receive (+)	
PCIE1_CLKREQ_N	273	DI	PCIe1 clock request	
PCIE1_RST_N	27	DO	PCIe1 reset	
PCIE1_WAKE_N	30	DI	PCIe1 wake up	
PCIE2_REFCLK_P	29	AO	PCIe2 reference clock (+)	Require differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly. Not supported by RG500L-AR* and RG500L-JO*.
PCIE2_REFCLK_M	28	AO	PCIe2 reference clock (-)	
PCIE2_TX_M	25	AO	PCIe2 transmit (-)	
PCIE2_TX_P	26	AO	PCIe2 transmit (+)	
PCIE2_RX_M	22	AI	PCIe2 receive (-)	
PCIE2_RX_P	23	AI	PCIe2 receive (+)	
PCIE2_CLKREQ_N	21	DI	PCIe2 clock request	Not supported by RG500L-AR* and RG500L-JO*.
PCIE2_RST_N	18	DO	PCIe2 reset	
PCIE2_WAKE_N	270	DI	PCIe2 wake up	
PCIE3_REFCLK_P*	13	AO	PCIe3 reference clock (+)	Require differential impedance of 85 Ω. PCIe Gen 3 compliant. If unused, connect RX to GND directly. Not supported by RG500L-AR* and RG500L-JO*.
PCIE3_REFCLK_M*	11	AO	PCIe3 reference clock (-)	
PCIE3_TX_M*	14	AO	PCIe3 transmit (-)	
PCIE3_TX_P*	16	AO	PCIe3 transmit (+)	
PCIE3_RX_M*	17	AI	PCIe3 receive (-)	
PCIE3_RX_P*	19	AI	PCIe3 receive (+)	
PCIE3_CLKREQ_N*	15	DI	PCIe3 clock request	Not supported by RG500L-AR* and RG500L-JO*.
PCIE3_RST_N*	269	DO	PCIe3 reset	
PCIE3_WAKE_N*	268	DI	PCIe3 wake up	

The following figure illustrates the PCIe interface connection.

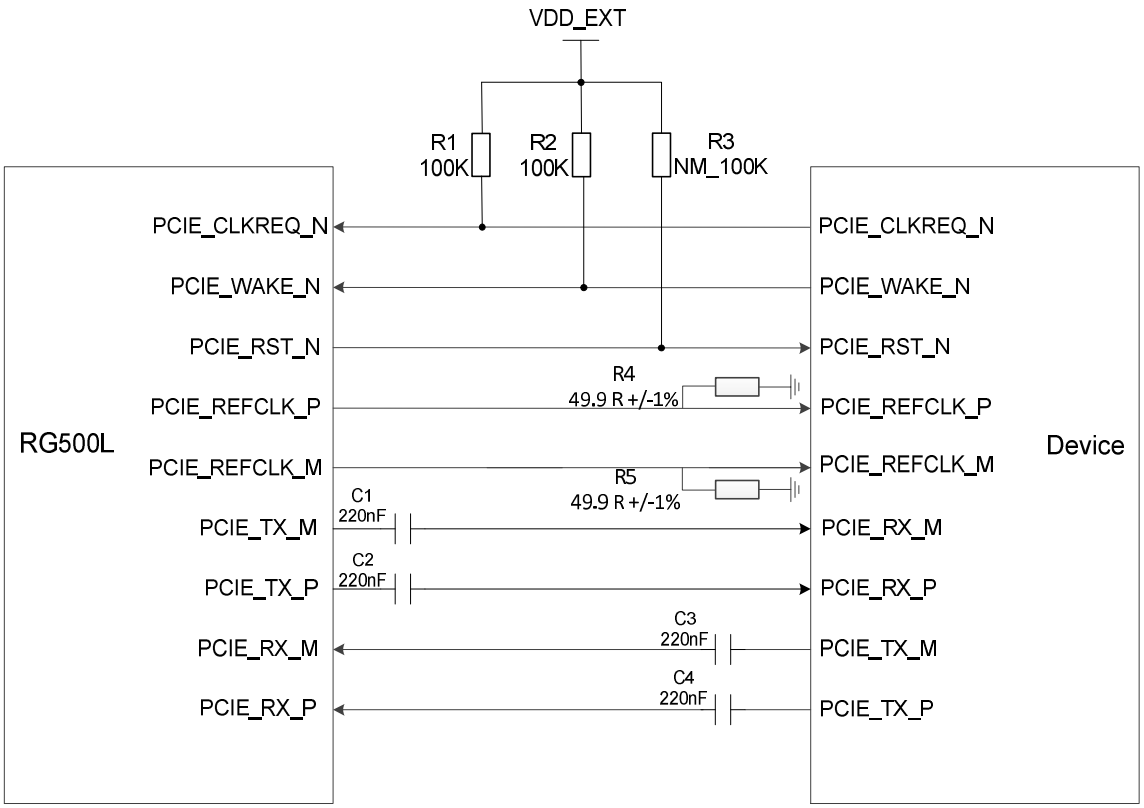


Figure 24: Reference Circuit of PCIe Interface

The following principles of PCIe interface design should be complied with to meet PCIe specifications.

- It is important to route the PCIE_TX/RX/REFCLK signal traces as differential pairs with ground surrounded. The differential impedance is 85 Ω is recommended.
- PCIe signals must be protected from noisy signals (clocks, DC-DC, RF and so forth). All other sensitive/high-speed signals and circuits must be routed far away from PCIe traces.
- For each differential pair, intra-lane length matching should be less than 0.125 mm.
- Inter-lane length matching, that is, (the trace length matching between the PCIE_TX/RX/REFCLK pairs) is not required.
- The PCIe inter-lane spacing, and the spacing between PCIe lanes and all other signals, should be larger than 4 times the trace width.
- It is better to place the PCIe AC coupling capacitors close to the transmitter source.
- Ensure not to stagger the capacitors. This can affect the differential integrity of the design and can create EMI.
- PCIe TX AC coupling capacitors should be 220 nF for Gen 3, and 100 nF is recommended for Gen 2 application.
- To reduce the probability for layer-to-layer manufacturing variation, minimize layer transitions on the main route (in other words, apply layer transitions only at module breakouts and connectors to

ensure minimum layer transitions on the main route).

- Hardware acceleration is supported by PCIe0 and PCIe1 only.
- For the PCIE_REFCLK pair, add resistors near the slot (EP) side and the recommended resister value is 49.9 Ω +/-1 %.

4.12. WWAN/WLAN Control Interface

Table 25: Pin Definition of WWAN/WLAN Control Interface

Pin Name	Pin No.	I/O	Description	Comment
WLAN_SYSRST_5G	271	DO	WLAN 5 GHz system reset	
WIFI_2.4G_EN*	272	DO	WLAN 2.4 GHz function enable control	Reserved.
WLAN_SYSRST_2.4G	274	DO	WLAN 2.4 GHz system reset	
WLAN_5G_EN*	406	DO	WLAN 5 GHz function enable control	Reserved.
BT_ACT_TXD [11]	36	DO	Coexistence interface for WWAN and 5 GHz Wi-Fi	Used for WWAN/WLAN coexistence by default.
BT_PRI_RXD [11]	275	DO	Coexistence interface for WWAN and 5 GHz Wi-Fi	
WLAN_ACT	39	DI	Coexistence interface for WWAN and 5 GHz Wi-Fi	
PTA_TX	279	DO	Coexistence interface for WWAN and 2.4 GHz Wi-Fi	
PTA_RX	278	DO	Coexistence interface for WWAN and 2.4 GHz Wi-Fi	
GPIO_15	280	DI	Coexistence interface for WWAN and 2.4 GHz Wi-Fi	

4.13. USB_BOOT Interface

Table 26: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description
USB_BOOT	81	DI	Force the module into emergency download mode

[11] Please note that this pin is for WWAN and Wi-Fi coexistence, not for WWAN and Bluetooth coexistence.

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before powering on the module, and then the module will enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

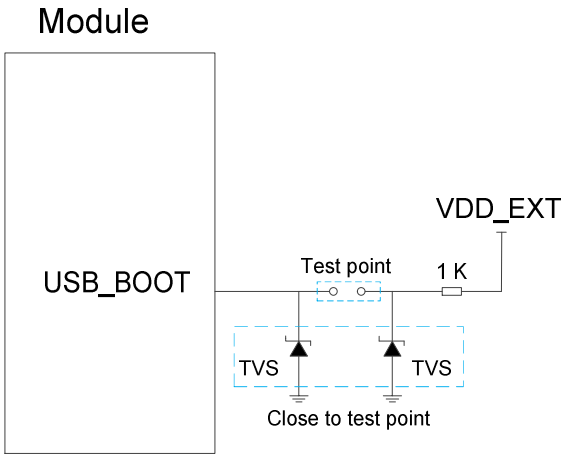


Figure 25: Reference Circuit of USB_BOOT Interface

NOTE

It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Directly connecting the test points as shown in the above figure can manually force the module to enter download mode.

4.14. Control Signals

Table 27: Pin Definition of Control Signals

Pin Name	Pin No.	I/O	Description
RESTORE_KEY	207	DI	Restore the module
WPS_KEY*	204	DI	Wi-Fi protected setup

A reference circuit is shown as below.

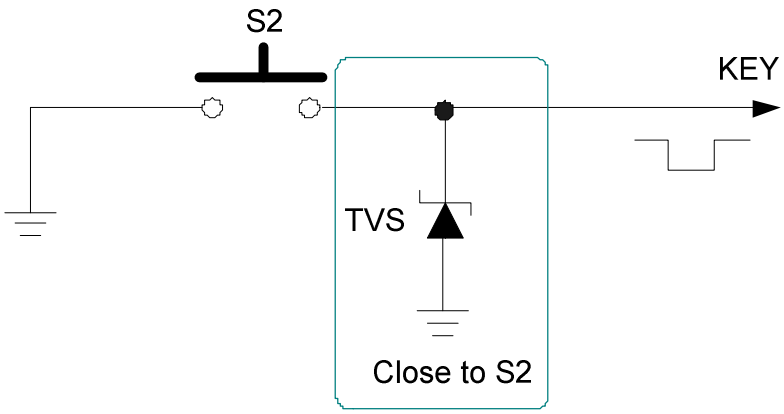


Figure 26: Reference Circuit of Control Keys

4.15. Indication Signals

Table 28: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	222	OD	Indicate the module's operation status	PMIC_ISINK3
NET_MODE*	219	DO	Indicate the module's network registration mode	
NET_STATUS*	239	OD	Indicate the module's network activity status	PMIC_ISINK2
AIR_MODE	225	OD	Indicate the module's airplane mode	PMIC_ISINK1
WIFI_MESH*	210	DO	Indicate the Wi-Fi mesh function status	
USIM_LED*	216	DO	Indicate the (U)SIM card function status	
VOIP_LED*	213	DO	Indicate the VoIP function status	

4.15.1. STATUS

The STATUS pin is an open drain output to indicate the module's operation status. It will output low level when the module is powered ON successfully. A reference circuit is shown as below.

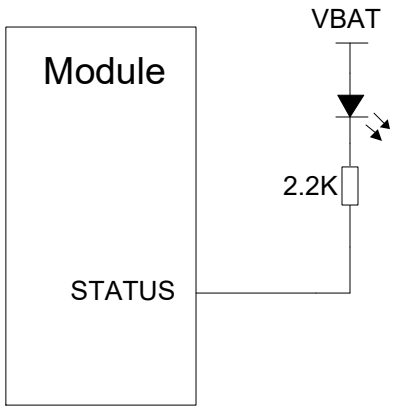


Figure 27: Reference Circuit of STATUS Indicator

4.15.2. Network Status Indication*

The network indication pins can be used to drive network status indication LEDs. The module provides two network indication pins: NET_MODE and NET_STATUS. The following tables describe pin definition and logic level changes in different network status.

Table 29: Working Mechanism of Network Registration Mode/Network Activity Indication

Pin Name	Status	Description
NET_MODE	Always High	Registered on 5G network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing
	Always High	Voice calling

Reference circuits are shown as below.

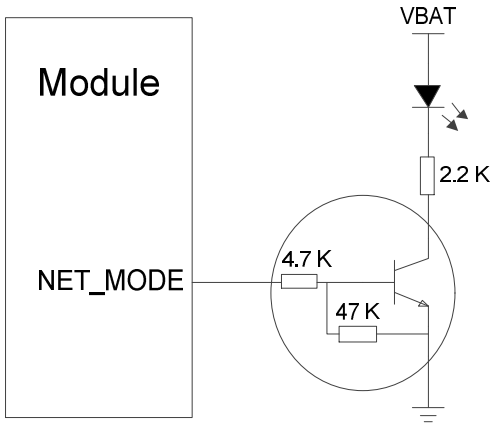


Figure 28: Reference Circuit of NET_MODE Indicator

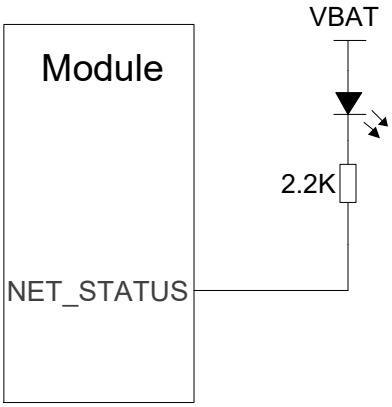


Figure 29: Reference Circuit of NET_STATUS Indicator

4.15.3. AIR_MODE

The AIR_MODE pin is an open drain output for indicating the module's airplane mode status. It will output low level when the module enters airplane mode successfully. A reference circuit is shown as below.

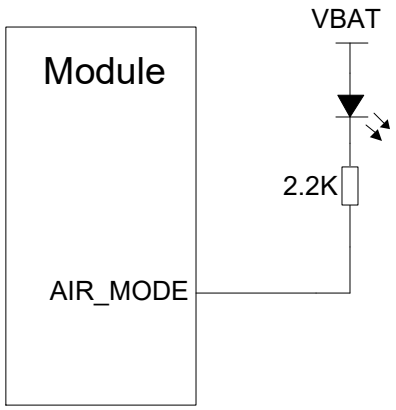


Figure 30: Reference Circuit of AIR_MODE Indicator

4.15.4. Other Indication Signals*

The WIFI_MESH, USIM_LED and VOIP_LED pins are output signals for indicating the functional state of the module. A reference circuit is shown as below.

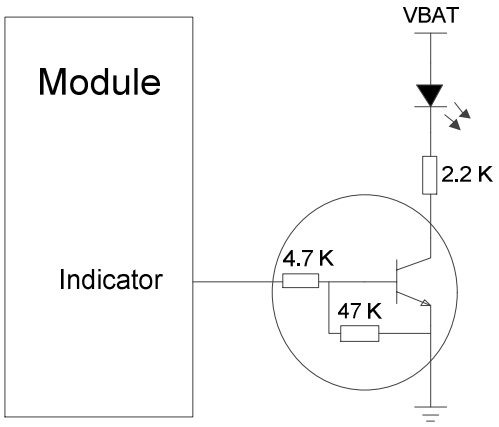


Figure 31: Reference Circuit of Other Indicators

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interfaces & Frequency Bands

The module provides several cellular antenna interfaces and the pin definition is shown below:

RG500L-EU/RG500L-NA/RG500L-LA/RG500L-AR*:

- Supports 8 cellular antenna interfaces (ANT0-ANT7)

RG500L-JO*:

- Supports 6 cellular antenna interfaces (ANT0/ANT2/ANT3/ANT4/ANT6/ANT7)

Table 30: Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	121	AIO	Antenna 0 interface	50 Ω impedance.
ANT1	130	AIO	Antenna 1 interface	
ANT2	139	AI	Antenna 2 interface	
ANT3	148	AI	Antenna 3 interface	
ANT4	157	AI	Antenna 4 interface	
ANT5	166	AI	Antenna 5 interface	
ANT6	175	AIO	Antenna 6 interface	
ANT7	184	AIO	Antenna 7 interface	

Table 31: Operating Frequency of RG500L-EU

Operating Frequency	Transmit (MHz)	Receive (MHz)	5G NR	LTE	UMTS
IMT (2100)	1920–1980	2110–2170	n1	B1	B1
DCS (1800)	1710–1785	1805–1880	n3	B3	
Cell (850)	824–849	869–894	n5 [12]	B5 [12]	B5 [12]
IMT-E (2600)	2500–2570	2620–2690	n7	B7	
EGSM (950)	880–915	925–960	n8	B8	B8
EU800	832–862	791–821	n20	B20	
700 APAC	703–748	758–803	n28	B28	
L-band	-	1452–1496		B32	
B38	2570–2620	2570–2620	n38	B38	
B40	2300–2400	2300–2400	n40	B40	
B41/B41-XGP	2496–2690	2496–2690	n41	B41	
B42	3400–3600	3400–3600		B42	
B43	3600–3800	3600–3800		B43	
B71	663–698	617–652	n71 [12]	B71 [12]	
n77	3300–4200	3300–4200	n77		
n78	3300–3800	3300–3800	n78		

Table 32: Operating Frequency of RG500L-NA

Operating Frequency	Transmit (MHz)	Receive (MHz)	5G NR	LTE
PCS (1900)	1850–1910	1930–1990	n2	B2
B4	1710–1755	2110–2155		B4

[12] For RG500L-EU, 5G NR n5/n71 bands and LTE B5/B71 bands and WCDMA B5 are optional. For details, please contact Quectel Technical Support.

Cell (850)	824–849	869–894	n5	B5
IMT-E (2600)	2500–2570	2620–2690	n7	B7
B12	699–716	729–746	n12	B12
B13	777–787	746–756		B13
B14	788–798	758–768		B14
B17	704–716	734–746		B17
B25	1850–1915	1930–1995	n25	B25
B26	814–849	859–894		B26
B29	-	717–728		B29
B30	2305–2315	2350–2360		B30
B38	2570–2620	2570–2620	n38	B38
B41	2496–2690	2496–2690	n41	B41
B42	3400–3600	3400–3600		B42
B43	3600–3800	3600–3800		B43
B46	-	5150–5925		B46
B48	3550–3700	3550–3700	n48	B48
B66	1710–1780	2110–2200	n66	B66
B71	663–698	617–652	n71	B71
n77	3300–4200	3300–4200	n77	
n78	3300–3800	3300–3800	n78	

Table 33: Operating Frequency of RG500L-LA

Operating Frequency	Transmit (MHz)	Receive (MHz)	5G NR	LTE	UMTS
PCS (1900)	1850–1910	1930–1990	n2	B2	B2
B4	1710–1755	2110–2155		B4	B4

Cell (850)	824–849	869–894	n5	B5	B5
IMT-E (2600)	2500–2570	2620–2690	n7	B7	
EGSM (950)	880–915	925–960		B8	
700 APAC	703–748	758–803	n28	B28	
B42	3400–3600	3400–3600		B42	
B43	3600–3800	3600–3800		B43	
B66	1710–1780	2110–2200	n66	B66	
n78	3300–3800	3300–3800	n78		

Table 34: Operating Frequency of RG500L-AR*

Operating Frequency	Transmit (MHz)	Receive (MHz)	5G NR	LTE	UMTS
IMT (2100)	1920–1980	2110–2170	n1	B1	
DCS (1800)	1710–1785	1805–1880	n3	B3	
Cell (850)	824–849	869–894	n5	B5	
EGSM (950)	880–915	925–960	n8	B8	
B40	2300–2400	2300–2400	n40	B40	
n78	3300–3800	3300–3800	n78		

Table 35: Operating Frequency of RG500L-JO*

Operating Frequency	Transmit (MHz)	Receive (MHz)	5G NR
700 APAC	703–748	758–803	n28
n78	3300–3800	3300–3800	n78

Table 36: RG500L-EU Cellular Antenna Mapping (Supporting 5G NR n5 and LTE B5 and WCDMA B5)

Antenna	UMTS	LTE	5G NR			LB (MHz)	MHB (MHz)	n77/n78 (MHz)	Pin No.
			Refarmed	n41	n77/n78				
ANT0		B42/B43 TRX			n77/n78 TRX0			3300–4200	121
ANT1	B1 TRX	MHB TRX0 [13]	n1/n3/n7/n38/n40 TRX0 n28 TRX0 [14]	TRX0		703–803	1710–2690		130
ANT2		B42/B43 PRX1			n77/n78 PRX1			3300–4200	139
ANT3		B42/B43 DRX1			n77/n78 DRX1			3300–4200	148
ANT4	B5/B8 DRX	MHB DRX1 LB DRX B32 DRX	n1/n3/n7/n38/n40 DRX1 n5/n8/n20/n28 DRX	DRX1		703–960	1450–2690		157
ANT5		MHB PRX1 B32 PRX	n1/n3/n7/n38/n40 PRX1	PRX1			1450–2690		166
ANT6		B42/B43 DRX			n77/n78 TRX1			3300–4200	175
ANT7	B1 DRX B5/B8 TRX	MHB TRX1 [13] LB TRX0	n1/n3/n7/n38/n40 TRX1 n28 TRX1 [14] n5/n8/n20 TRX0	TRX1		703–960	1710–2690		184

[13] LTE MHB TRX is activated when 5G NR FDD middle/high bands are supported in NSA mode.

[14] n28 TRX is activated when 5G NR FDD low bands are supported in NSA mode.

Table 37: RG500L-EU Cellular Antenna Mapping (Supporting 5G NR n71 and LTE B71)

Antenna	UMTS	LTE	5G NR			LB (MHz)	MHB (MHz)	n77/n78 (MHz)	Pin No.
			Refarmed	n41	n77/n78				
ANT0		B42/B43 TRX			n77/n78 TRX0			3300–4200	121
ANT1	B1 TRX	MHB TRX0 [13]	n1/n3/n7/n38/n40 TRX0	TRX0			1710–2690		130
ANT2		B42/B43 PRX1			n77/n78 PRX1			3300–4200	139
ANT3		B42/B43 DRX1			n77/n78 DRX1			3300–4200	148
ANT4	B8 DRX	MHB DRX1 LB DRX B32 DRX	n1/n3/n7/n38/n40 DRX1 n8/n20/n28/n71 DRX	DRX1		617–960	1450–2690		157
ANT5		MHB PRX1 B32 PRX	n1/n3/n7/n38/n40 PRX1	PRX1			1450–2690		166
ANT6		B42/B43 DRX			n77/n78 TRX1			3300–4200	175
ANT7	B1 DRX B8 TRX	MHB TRX1 [15] LB TRX0	n1/n3/n7/n38/n40 TRX1 n8/n20/n28/n71 TRX0	TRX1		617–960	1710–2690		184

[15] LTE MHB TRX is activated when 5G NR FDD middle/high bands are supported in NSA mode.

Table 38: RG500L-NA Cellular Antenna Mapping

Antenna	LTE	5G NR			LB (MHz)	MHB (MHz)	n48/n77/n78 (MHz)	Pin No.
		Refarmed	n41	n48/n77/n78				
ANT0	B42/B43/B48 TRX0			n48/n77/n78 TRX0			3300–4200	121
ANT1	B5/B26 TRX MHB TRX1 [13]	n2/n7/n25/n38/n66 TRX0 n5 TRX	TRX0		814–894	1710–2690		130
ANT2	B46 PRX B42/B43/B48 PRX1			n48/n77/n78 PRX1		5150–5925	3300–4200	139
ANT3	B46 DRX B42/B43/B48 DRX1			n48/n77/n78 DRX1		5150–5925	3300–4200	148
ANT4	B12/B13/B14/B17/B71 DRX MHB DRX1 B29 DRX	n2/n7/n25/n38/n66 DRX1 n12/n71 DRX	DRX1		617–798	1710–2690		157
ANT5	MHB PRX1 B5/B26 DRX	n2/n7/n25/n38/n66 PRX1 n5 DRX	PRX1		814–894	1710–2690		166
ANT6	B42/B43/B48 DRX0			n48/n77/n78 TRX1			3300–4200	175
ANT7	B12/B13/B14/B17/B71 TRX MHB TRX0 [13] B29 PRX	n12/n71 TRX n2/n7/n25/n38/n66 TRX1	TRX1		617–798	1710–2690		184

Table 39: RG500L-LA Cellular Antenna Mapping

Antenna	UMTS	LTE	5G NR		LB (MHz)	MHB (MHz)	n78 (MHz)	Pin No.
			Refarmed	n78				
ANT0		B42/B43 TRX0		n78 TRX0			3300–3800	121
ANT1	B2/B4 DRX	MHB TRX1 [13]	n2/n7/n66 TRX0			1710–2690		130
ANT2		B42/B43 PRX1		n78 PRX1			3300–3800	139
ANT3		B42/B43 DRX1		n78 DRX1			3300–3800	148
ANT4	B5 DRX	B5/B8/B28 DRX MHB DRX1	n2/n7/n66 DRX1 n5/n28 DRX		703–960	1710–2690		157
ANT5		MHB PRX1	n2/n7/n66 PRX1			1710–2690		166
ANT6		B42/B43 DRX0		n78 TRX1			3300–3800	175
ANT7	B2/B4/B5 TRX	B5/B8/B28 TRX MHB TRX0 [13]	n5/n28 TRX n2/n7/n66 TRX1		703–960	1710–2690		184

NOTE

TRX0/1 = TX + PRX/DRX; DRX1 = DRX MIMO; PRX1 = PRX MIMO

5.1.2.

5.1.2. Rx Sensitivity

The following table shows conducted RF receiving sensitivity of the module.

Table 40: Conducted RF Receiving Sensitivity of RG500L-EU

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO [17]	
LTE-FDD B1 (10 MHz)	-98.0	-98.5	-102.0	-96.3 dBm
LTE-FDD B3 (10 MHz)	-98.5	-99.0	-102.0	-93.3 dBm
LTE-FDD B5 (10 MHz)	-99.0	-101.0	-102.0	-94.3 dBm
LTE-FDD B7 (10 MHz)	-96.5	-97.5	-100.0	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99.0	-100.0	-102.0	-93.3 dBm
LTE-FDD B20 (10 MHz)	-98.5	-100.5	-101.5	-93.3 dBm
LTE-FDD B28 (10 MHz)	-98.5	-98.0	-101.5	-94.3 dBm
LTE-TDD B38 (10 MHz)	-98.5	-98.0	-101.0	-96.3 dBm
LTE-TDD B40 (10 MHz)	-98.5	-97.0	-100.0	-96.3 dBm
LTE-TDD B41 (10 MHz)	-97.5	-97.5	-101.0	-94.3 dBm
LTE-TDD B42 (10 MHz)	-99.0	-99.0	-103.0	-95 dBm
LTE-TDD B43 (10 MHz)	-99.0	-98.5	-101.5	-95 dBm
LTE-FDD B71 (10 MHz)	-100.0	-101.0	-103.0	-93.5 dBm
5G NR-FDD n1 (20 MHz) (SCS: 15 kHz)	-97	-97	-100	-94 dBm
5G NR-FDD n3 (20 MHz) (SCS: 15 kHz)	-96	-96	-99	-91 dBm
5G NR-FDD n5 (10 MHz) (SCS: 15 kHz)	-97	-97	-100	-94.8 dBm
5G NR-FDD n7 (20 MHz) (SCS: 15 kHz)	-96	-96	-99	-91.8 dBm
5G NR-FDD n8 (10 MHz)	-96	-96	-99	-94 dBm

[17] For the SIMO receiving sensitivity, LTE bands are tested with 2 Rx antennas, and 5G n1/n3/n7/n38/n40/n41/n71/n77/n78 bands are tested with 4 Rx antennas and 5G n5/n8/n20/n28 bands are tested with 2 Rx antennas.

(SCS: 15 kHz)				
5G NR-FDD n20 (10 MHz) (SCS: 15 kHz)	-97	-97	-100	-94 dBm
5G NR-FDD n28 (10 MHz) (SCS: 15 kHz)	-96	-96	-99	-96 dBm
5G NR-TDD n38 (20 MHz) (SCS: 30 kHz)	-97	-97	-100	-94 dBm
5G NR-TDD n40 (20 MHz) (SCS: 30 kHz)	-95	-95	-98	-94 dBm
5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-91	-91	-94	-84.7 dBm
5G NR-FDD n71 (10 MHz) (SCS: 15 kHz)	-97	-97	-100	-94 dBm
5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	-89	-89	-92	-85.1 dBm
5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-89	-89	-92	-85.6 dBm

Table 41: Conducted RF Receiving Sensitivity of RG500L-NA

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO [18]	
LTE-FDD B2 (10 MHz)	-99.0	-99.0	-102.0	-94.3 dBm
LTE-FDD B4 (10 MHz)	-98.0	-98.0	-101.0	-96.3 dBm
LTE-FDD B5 (10 MHz)	-100.0	-100.0	-103.0	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97.0	-97.0	-100.0	-94.3 dBm
LTE-FDD B12 (10 MHz)	-99.0	-99.0	-102.0	-93.3 dBm
LTE-FDD B13 (10 MHz)	-98.0	-98.0	-101.0	-93.3 dBm
LTE-FDD B14 (10 MHz)	-99.0	-99.0	-102.0	-93.3 dBm

[18] For the SIMO receiving sensitivity, LTE bands are tested with 2 Rx antennas, and 5G n2/n7/n25/n38/n41/n48/n66/n77/n78 bands are tested with 4 Rx antennas and 5G n5/n12/n71 bands are tested with 2 Rx antennas.

LTE-FDD B17 (10 MHz)	-99.0	-99.0	-102.0	-93.3 dBm
LTE-FDD B25 (10 MHz)	-99.0	-99.0	-102.0	-92.8 dBm
LTE-FDD B26 (10 MHz)	-100.0	-100.0	-103.0	-93.8 dBm
LTE-FDD B30 (10 MHz)	-97.0	-97.0	-100.0	-95.3 dBm
LTE-TDD B38 (10 MHz)	-98.0	-98.5	-101.0	-96.3 dBm
LTE-TDD B41 (10 MHz)	-96.0	-96.5	-99.0	-94.3 dBm
LTE-TDD B42 (10 MHz)	-98.0	-97.5	-101.0	-95.0 dBm
LTE-TDD B43 (10 MHz)	-97.5	-97.0	-100.5	-95.0 dBm
LTE-TDD B48 (10 MHz)	-98.0	-97.0	-100.5	-95.0 dBm
LTE-FDD B66 (10 MHz)	-97.5	-98.0	-100.5	-95.8 dBm
LTE-FDD B71 (10 MHz)	-100.0	-101.0	-103.0	-93.5 dBm
5G NR-FDD n2 (10 MHz) (SCS: 15 kHz)	-100	-100	-102	-94.8 dBm
5G NR-FDD n5 (10 MHz) (SCS: 15 kHz)	-97	-97	-100	-94.8 dBm
5G NR-FDD n7 (10 MHz) (SCS: 15 kHz)	-97	-97	-102	-94.8 dBm
5G NR-FDD n12 (10 MHz) (SCS: 15 kHz)	-97	-97	-100	-93.8 dBm
5G NR-FDD n25 (10 MHz) (SCS: 15 kHz)	-97	-97	-101	-93.3 dBm
5G NR-TDD n38 (10 MHz) (SCS: 30 kHz)	-98	-98	-101.2	-97.1 dBm
5G NR-TDD n41 (100 MHz) (SCS: 30 kHz)	-88	-88	-93.6	-84.7 dBm
5G NR-TDD n48 (100 MHz) (SCS: 30 kHz)	-89	-89	-94.8	-86.7 dBm
5G NR-FDD n66 (10 MHz) (SCS: 15 kHz)	-98	-98	-101	-96.3 dBm
5G NR-FDD n71 (10 MHz) (SCS: 15 kHz)	-97	-97	-100.8	-94 dBm
5G NR-TDD n77 (100 MHz) (SCS: 30 kHz)	-90	-90	-94.4	-85.1 dBm
5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-90	-90	-93.9	-85.6 dBm

Table 42: Conducted RF Receiving Sensitivity of RG500L-LA

Frequency	Receiving Sensitivity (Typ.)			3GPP Requirement (SIMO)
	Primary	Diversity	SIMO [19]	
LTE-FDD B2 (10 MHz)	-99.0	-99.0	-102.0	-94.3 dBm
LTE-FDD B4 (10 MHz)	-98.0	-98.0	-101.0	-96.3 dBm
LTE-FDD B5 (10 MHz)	-100.3	-101.8	-104.1	-94.3 dBm
LTE-FDD B7 (10 MHz)	-97.0	-97.0	-100.0	-94.3 dBm
LTE-FDD B8 (10 MHz)	-99.6	-101.7	-104.1	-93.3 dBm
LTE-FDD B28 (10 MHz)	-99.8	-101.9	-104.3	-93.3 dBm
LTE-TDD B42 (10 MHz)	-98.0	-97.5	-101.0	-95.0 dBm
LTE-TDD B43 (10 MHz)	-97.5	-97.0	-100.5	-95.0 dBm
LTE-FDD B66 (10 MHz)	-97.5	-98.0	-100.5	-95.8 dBm
5G NR-FDD n2 (10 MHz) (SCS: 15 kHz)	-100	-100	-106	-94.8 dBm
5G NR-FDD n5 (10 MHz) (SCS: 15 kHz)	99.6	-99.6	-102.8	-94.8 dBm
5G NR-FDD n7 (10 MHz) (SCS: 15 kHz)	-97	-97	-103	-94.8 dBm
5G NR-FDD n28 (10 MHz) (SCS: 15 kHz)	-99	-99	-101.1	-93.8 dBm
5G NR-FDD n66 (10 MHz) (SCS: 15 kHz)	-98	-98	-107	-96.3 dBm
5G NR-TDD n78 (100 MHz) (SCS: 30 kHz)	-87	-89	-94.5	-85.6 dBm

5.1.3.

5.1.3.

5.1.3. Reference Design

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components should be placed as close to the antenna as possible. The capacitors are not mounted by default.

[19] For the SIMO receiving sensitivity, LTE bands are tested with 2 Rx antennas, and 5G n2/n7/n66/n78 bands are tested with 4 Rx antennas and 5G n5/n28 bands are tested with 2 Rx antennas.

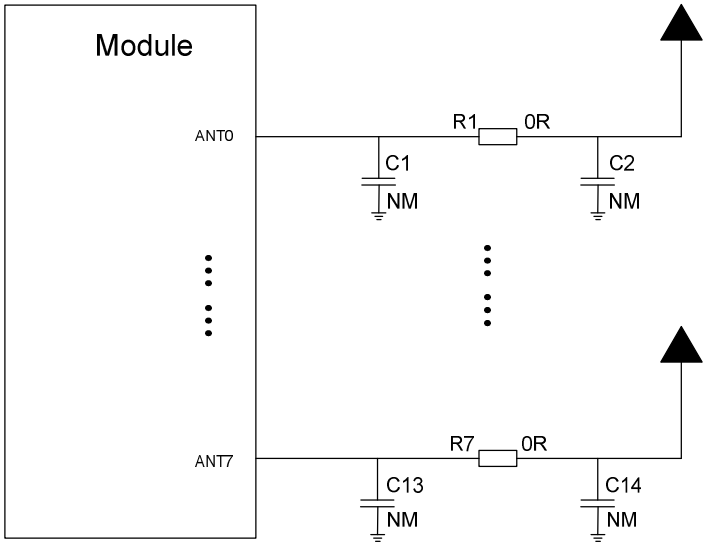
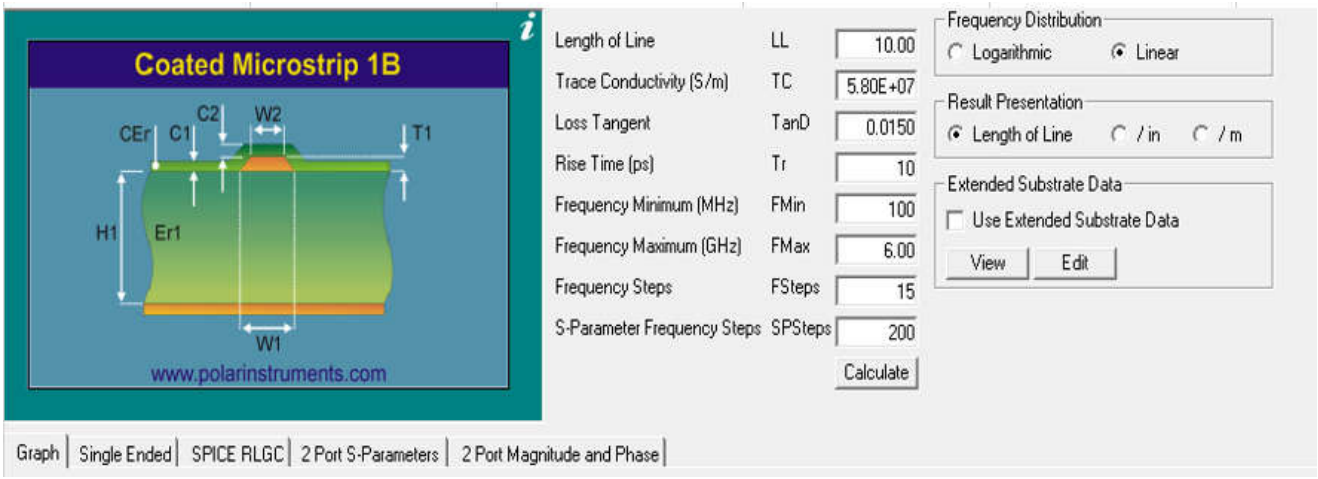


Figure 32: Reference Circuit for Cellular Antenna Interfaces

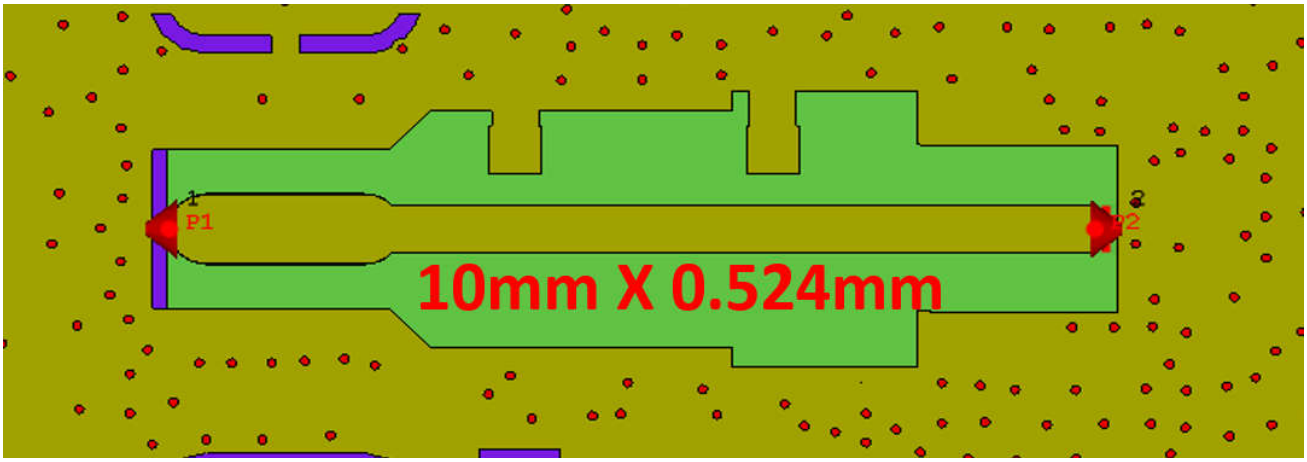
NOTE

1. Use a π-type circuit for all the antenna circuits to facilitate future debugging.
2. Keep the characteristic impedance of the cellular antenna (ANT0–ANT7) traces as 50 Ω.
3. Keep at least 15 dB isolation between RF antennas to improve the receiving sensitivity, and at least 20 dB isolation between 5G NR UL MIMO antennas.
4. Keep 75 dB isolation between each two antenna traces.
5. Keep digital circuits such as switch mode power supply, (U)SIM card, USB interface, camera module, display connector and SD card away from the antenna traces.

The characteristic impedance depends on the dielectric of PCB, the track width and theground plane spacing. Microstrip type is required. The detail simulation as below.



The RF trace of the test board which was used in the FCC test is defined as below.



Ant0~7 share the same design.

5.2. GNSS

The module includes a fully integrated global navigation satellite system solution that supports GPS/BDS/GLONASS/Galileo.

The module supports *NMEA 0183* protocol, and outputs NMEA* sentences via USB interface (data update rate: 1–5 Hz, 1 Hz by default).

For more details about configuration of GNSS [21] function, see ***document [2]***.

5.2.1. Antenna Interface & Frequency Bands

The following table shows the pin definition, frequency, and performance of GNSS antenna interface.

Table 43: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	193	AI	GNSS antenna interface	50 Ω impedance.

Table 44: GNSS Frequency

Type	Frequency	Unit

[21] For RG500L-EU/RG500L-NA, GNSS function is optional, but for RG500L-LA , GNSS function is not supported. For details, please contact Quectel Technical Support.

GPS	1575.42 ±1.023 (GPS L1) 1176.45 ±10.23 (GPS L5) (RG500L-EU only)	MHz
GLONASS	1597.5–1605.8	
Galileo	1575.42 ±2.046	
BDS	1561.098 ±2.046	

5.2.2. GNSS Performance

NOTE

1. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).

5.2.3. Reference Design

The following is the reference circuit of GNSS antenna.

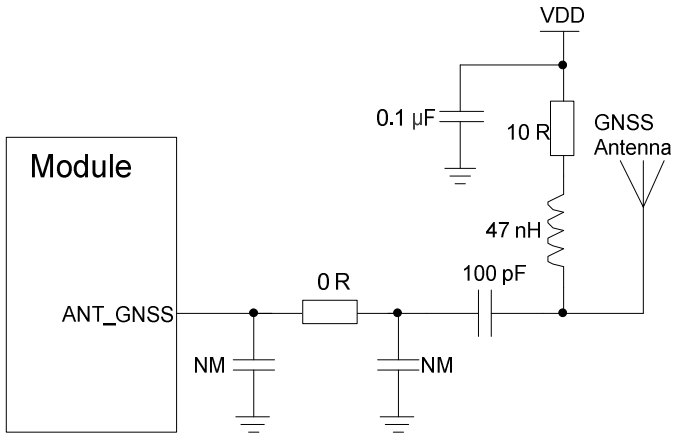


Figure 33: Reference Circuit of GNSS Antenna Interface

NOTE

1. You can select an external LDO for power supply according to the active antenna requirements.
2. If the module is designed with a passive antenna, then the VDD circuit is not needed.

3. Keep the characteristic impedance of GNSS antenna trace as 50 Ω.
4. Place the π-type matching components as close to the antenna as possible.
5. Keep digital circuits such as switch mode power supply, (U)SIM card, USB interface, camera module, display connector and SD card away from the antenna traces.
6. Keep 75 dB isolation between GNSS and cellular antenna traces.
7. Keep 15 dB isolation between GNSS and cellular antennas to improve the receiving sensitivity.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

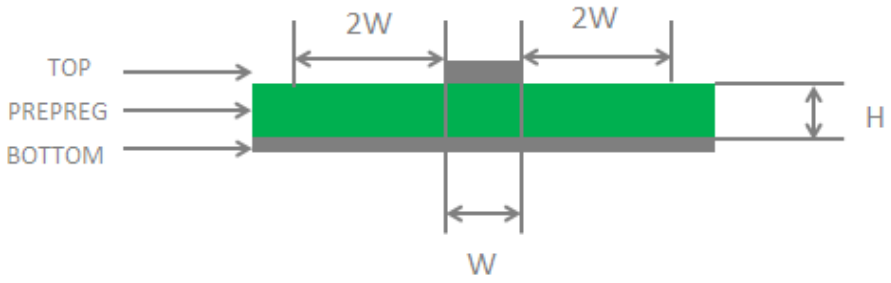


Figure 34: Microstrip Design on a 2-layer PCB

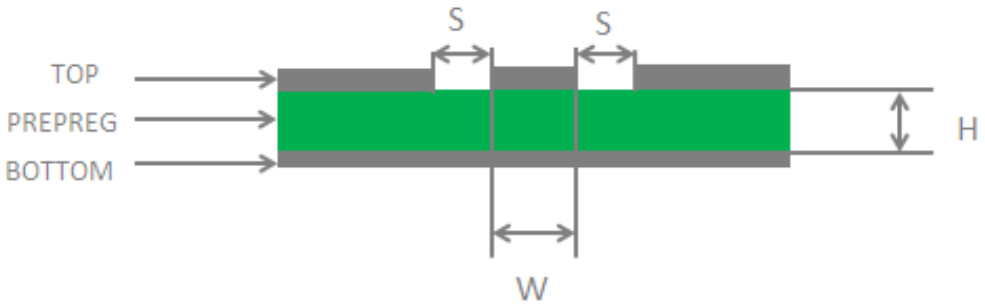


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

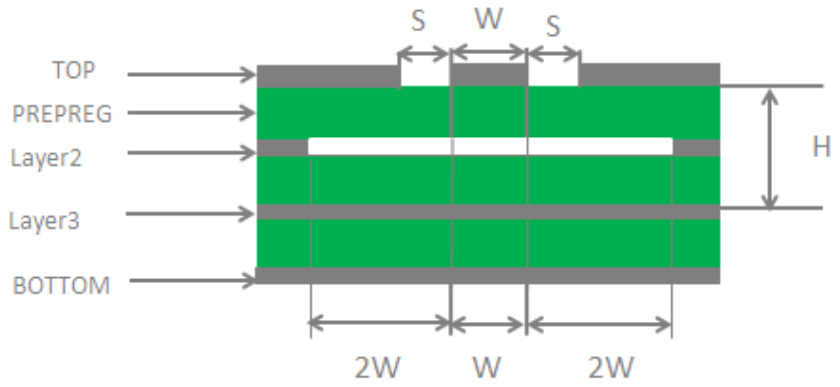


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

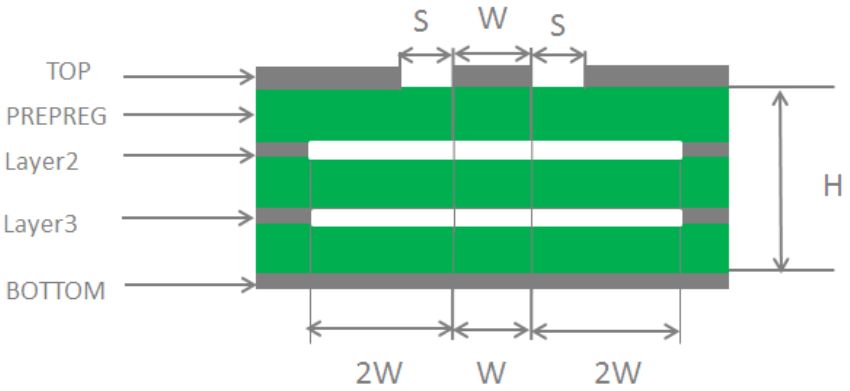


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.4. Requirements for Antenna Design

Table 45: Requirements for Antenna Design

Antenna Type	Requirements
GNSS	Frequency range: ● GNSS L1: 1559–1609 MHz (Supported by RG500L-EU/RG500L-NA) ● GNSS L5: 1166–1187 MHz (RG500L-EU only) Polarization: RHCP or linear VSWR: ≤ 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
5G NR/LTE/UMTS	VSWR: ≤ 2 Efficiency: > 30% Gain: > 0 dBi Max input power: 50 W Input impedance: 50 Ω Polarization: Vertical Cable insertion loss: ● **< 1 dB:** LB (<1 GHz) ● **< 1.5 dB:** MB (1–2.3 GHz) ● **< 2 dB:** HB (> 2.3 GHz)

5.5. RF Connector Recommendation

The recommended receptacle dimensions are illustrated as below.

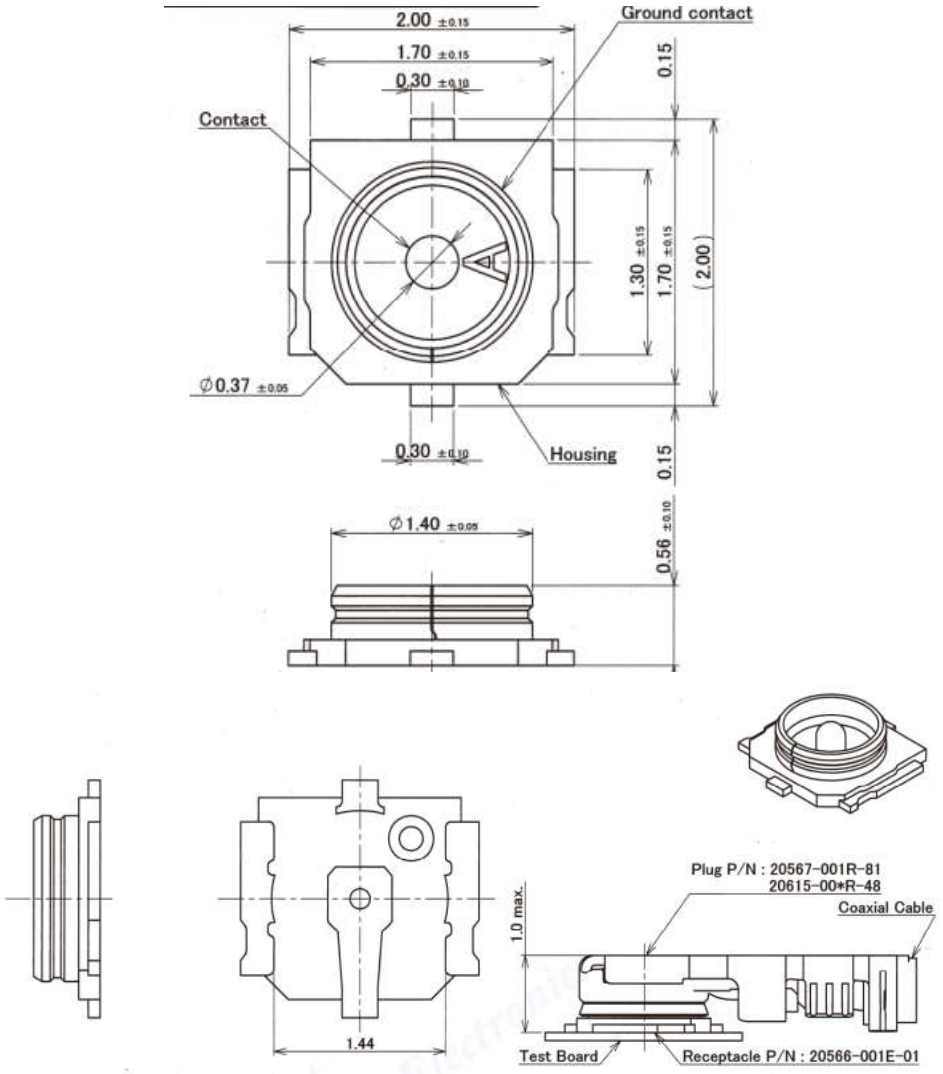


Figure 38: Dimensions of the Receptacles (Unit: mm)

The following figure shows the specifications of mating plugs using Ø0.81 mm coaxial cables.

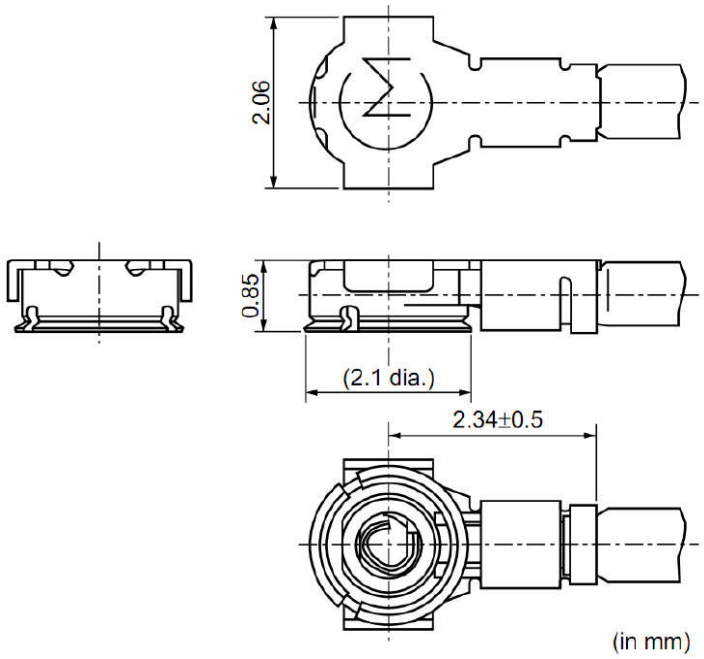


Figure 39: Specifications of Mating Plugs Using Ø0.81 mm Coaxial Cables (Unit: mm)

RF connecters and cables by I-PEX are recommended. For more details, please visit https://www.i-pex.com.

5.5.1. Assemble Coaxial Cable Plug Manually

The illustration of manually plugging in the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

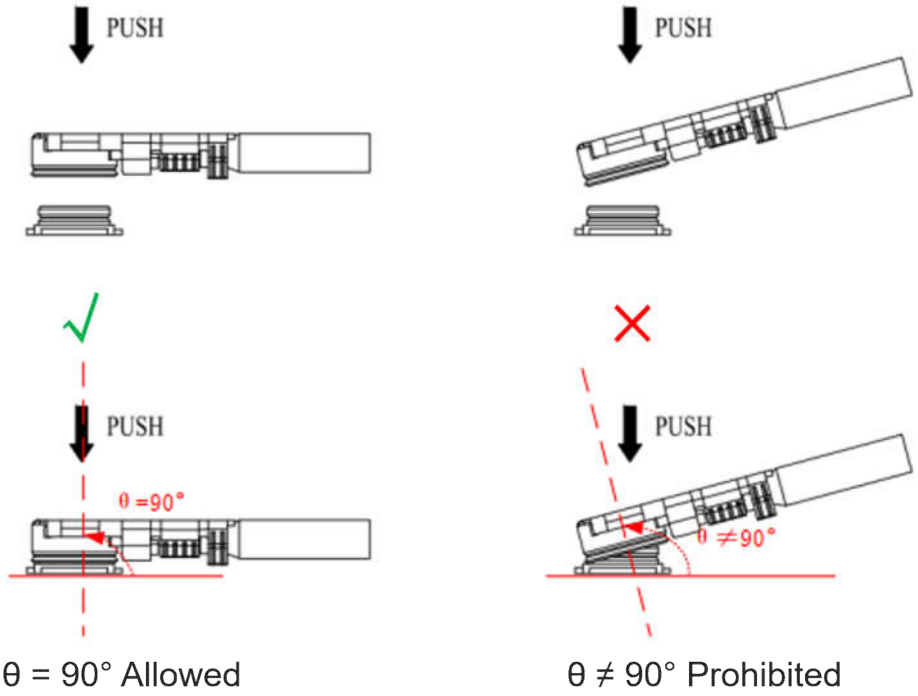


Figure 40: Manually Plug In a Coaxial Cable Plug

The illustration of manually pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

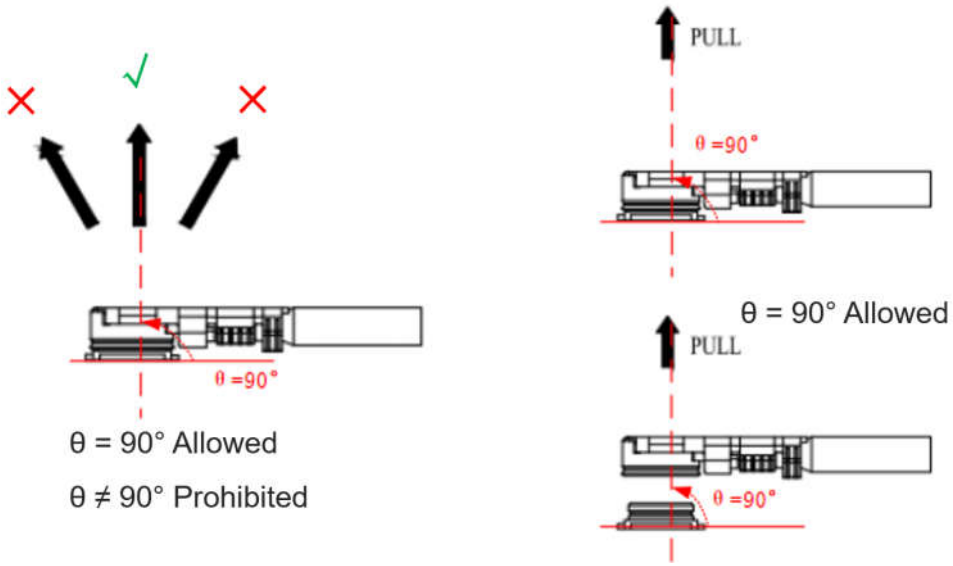


Figure 41: Manually Pull Out a Coaxial Cable Plug

5.5.2. Assemble Coaxial Cable Plug with Jig

The illustration of plugging in and pulling out the coaxial cable plug with a jig is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

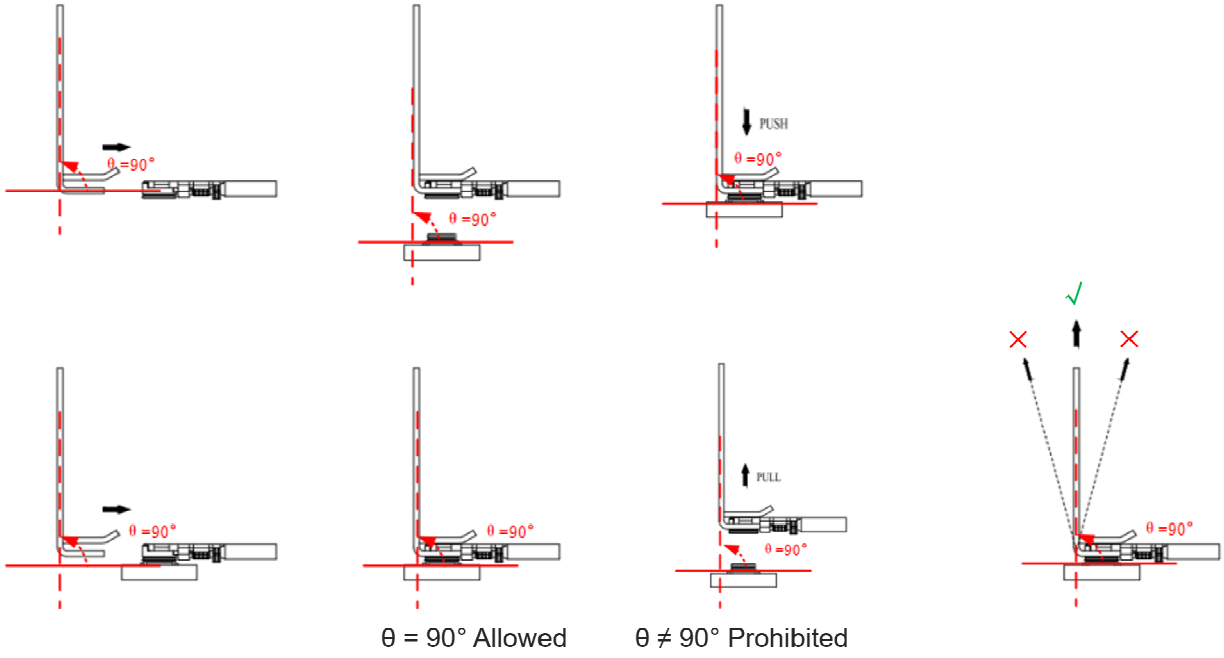


Figure 42: Install the Coaxial Cable Plug with Jig

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 46: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB/VBAT_RF	-0.5	5	V
USB_VBUS	0	21	V
Peak Current of VBAT_BB	-	2	A
Peak Current of VBAT_RF	-	2.5	A
Voltage on Digital Pins	-0.3	1.98	V
Voltage at ADC0	-0.5	1.98	V
Voltage at ADC1	0	1.45	V
Voltage at ADC2	0	1.45	V

6.2. Power Supply Ratings

Table 47: The Module's Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum	3.3	3.8	4.3	V

		values.				
I_{VBAT}	Peak supply current	Maximum power control level at n41	-	1.5	2	A
USB_VBUS	USB connection detection		4.2	5.0	15	V

6.3. Power Consumption

Table 48: Averaged Power Consumption for RG500L-EU/RG500L-NA/RG500L-LA

Mode	Conditions	Band/Combinations	Current	Unit
Power-off	Power off	-	80	μA
RF Disabled	**AT+CFUN=0** (USB disabled)	-	120	mA
	AT+CFUN=4 (USB disabled)	-	125	mA
Sleep State	**AT+CFUN=0** (USB disabled)	-	6.5	mA
Idle State	SA PF = 64 (USB 2.0 active)	-	125	mA
	SA PF = 64 (USB 3.0 active)	-	125	mA
	LTE UL QPSK			
	NR DL, 256QAM			
	NR UL QPSK			
	LTE Tx Power @ 23 dBm			
	NR Tx Power @ 23 dBm			

NOTE

1. Power consumption test is carried out under 3.8 V, 25 °C with EVB and thermal dissipation measures.
2. The power consumption above is for reference only, which may vary among variants of the module. Please contact Quectel Technical Supports for detailed power consumption test report of the specific model.

6.4. Digital I/O Characteristic

Table 49: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.65 × VDD_EXT	VDD_EXT + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.35 × VDD_EXT	V
V_{OH}	High-level output voltage	0.75 × VDD_EXT	-	V
V_{OL}	Low-level output voltage	-	0.25 × VDD_EXT	V

Table 50: SDIO 1.86 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.27	2.16	V
V_{IL}	Low-level input voltage	-0.3	0.58	V
V_{OH}	High-level output voltage	1.4	2.16	V
V_{OL}	Low-level output voltage	-0.3	0.45	V

Table 51: SDIO 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	1.875	3.3	V
V_{IL}	Low-level input voltage	-0.3	0.75	V
V_{OH}	High-level output voltage	2.25	3.3	V
V_{OL}	Low-level output voltage	-0.3	0.375	V

Table 52: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit

USIM_VDD	Power supply	1.62	1.98	V
V_{IH}	High-level input voltage	1.4	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.27	V
V_{OH}	High-level output voltage	1.4	USIM_VDD + 0.1	V
V_{OL}	Low-level output voltage	-0.3	0.36	V

Table 53: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.3	V
V_{IH}	High-level input voltage	2.6	USIM_VDD + 0.3	V
V_{IL}	Low-level input voltage	-0.3	0.4	V
V_{OH}	High-level output voltage	2.6	USIM_VDD + 0.1	V
V_{OL}	Low-level output voltage	-0.3	0.4	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 54: Electrostatics Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV

6.6. Operating and Storage Temperatures

Table 55: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [22]	-30	+25	+70	°C
Extended Operating Temperature Range [23]	-40	+25	+85	°C
Storage Temperature Range	-40	-	+90	°C

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal ICs always work within in the recommended operating temperature.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the heatsink should be larger than the module to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

[22] To meet this operating temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this operating temperature range, the module can meet 3GPP specifications.

[23] To meet this extended temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

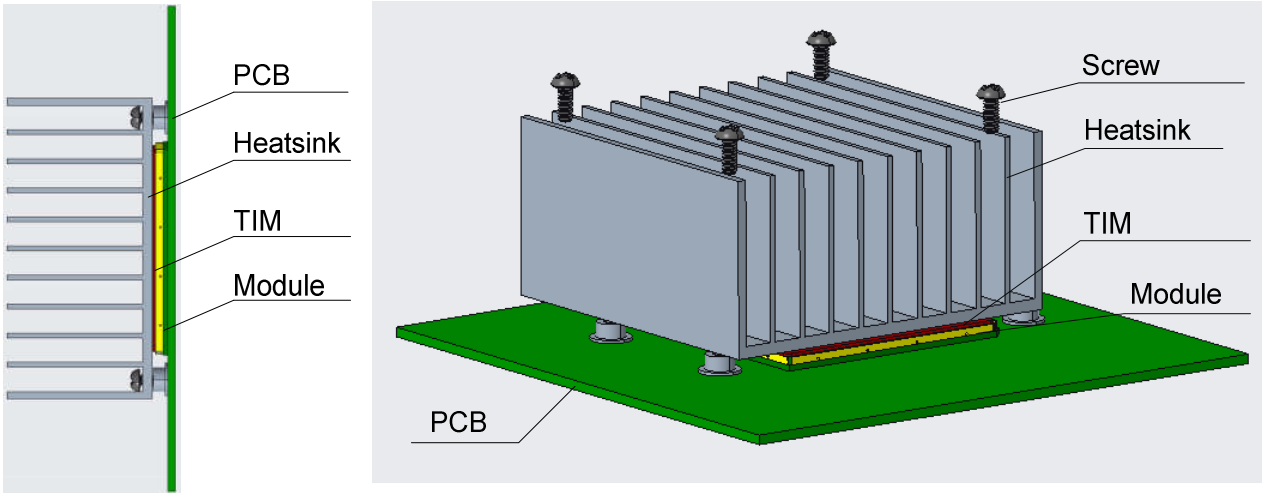


Figure 43: Placement and Fixing of Heatsink

NOTE

For more details about thermal design, see ***document [4]***.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

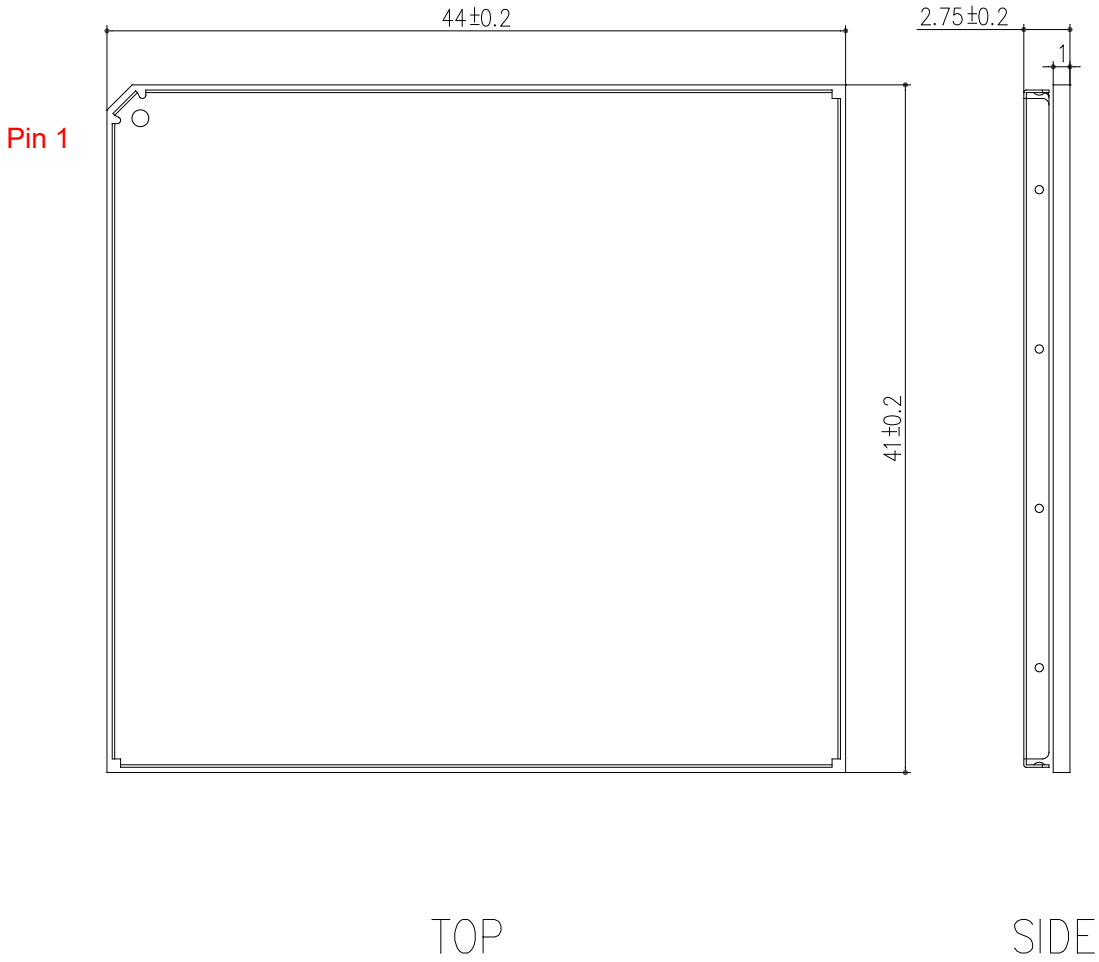


Figure 44: Module Top and Side Dimensions (Unit: mm)

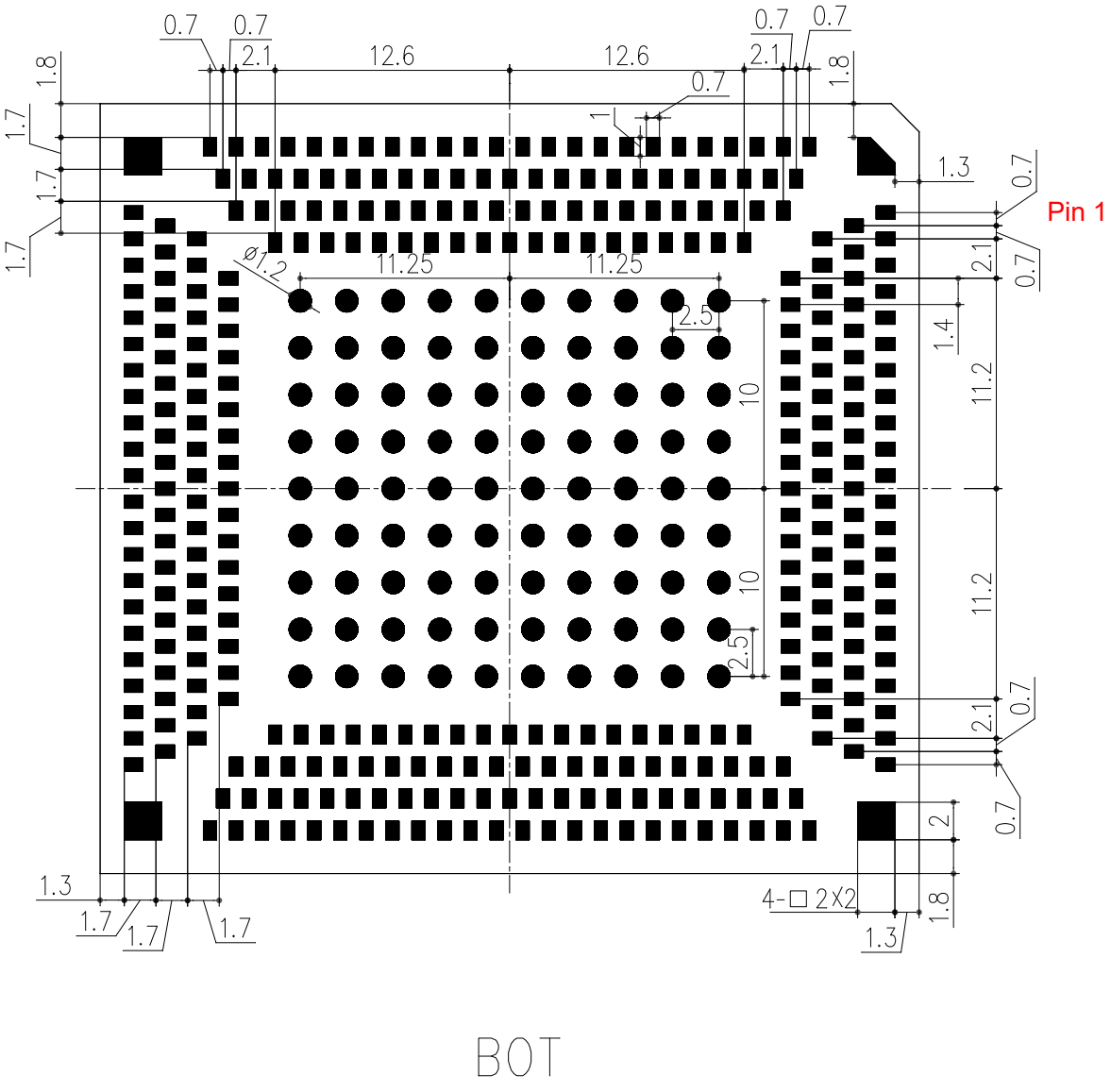


Figure 45: Module Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.