# EG950A Series

# Hardware Design

**LTE Standard Module Series**

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The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Quectel assumes no liability for customers' failure to comply with these precautions.

| | |
|---|---|
|  | Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving. |
|  | Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft. |
|  | Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities. |
|  | Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances. |
|  | The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment. |
|  | In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders. |

# About the Document

## Revision History

| Version | Date | Author | Description |
|---|---|---|---|
| - | 2022-12-15 | Clark ZHANG/ Liking LIN/ Alessa TANG | Creation of the document |
| 1.0 | 2023-08-09 | Clark ZHANG/ Liking LIN/ Jerry LIN | First official release |

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# 1 Introduction

This document introduces EG950A series module and its hardware interfaces and air interfaces connected to your application. It provides a quick insight into the module's information such as its interface characteristics, RF performance and electrical & mechanical specifications.

## 1.1. Special Marks

**Table 1: Special Marks**

| Mark | Definition |
|---|---|
| * | Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable. |
| […] | Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA [0:3] refers to all four SDIO_DATA pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2 and SDIO_DATA3. |

# 2 Product Overview

The module is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M applications, for instance:

- Automation field
- Smart metering
- Tracking system
- Security system
- Router
- Wireless POS
- Mobile computing device
- PDA phone
- Tablet computer

**Table 2: Basic Information**

| EG950A Series | |
|---|---|
| Packaging type | LGA |
| Pin counts | 102 |
| Dimensions | (29.0 ±0.2) mm × (25.0 ±0.2) mm × (2.4 ±0.2) mm |
| Weight | Approx. 3.74 g |
| Variants | EG950A-EL, EG950A-LA |

## 2.1. Frequency Bands and Functions

**Table 3: Frequency Bands of EG950A Series**

| Mode and Function | EG950A-EL | EG950A-LA |
|---|---|---|
| LTE-FDD | B1/B3/B5/B7/B8/B20/B28 | B1/B2/B3/B4/B5/B7/B8/B28/B66 |
| WCDMA | B1/B5/B8 | B1/B2/B4/B5/B8 |
| GNSS | GPS, GLONASS, BDS, QZSS | - |

**NOTE**

GNSS function is only supported by EG950A-EL module, and the function is optional. Only the module with built-in GNSS function has GNSS antenna interface.

## 2.2. Key Features

**Table 4: Key Features**

| Features | Details |
|---|---|
| Power Supply | ● Supply voltage range: 3.4–4.5 V<br>● Typical supply voltage: 3.8 V |
| SMS | ● Text and PDU modes<br>● Point-to-point MO and MT<br>● SMS cell broadcast<br>● SMS storage: ME by default |
| USB Interface | ● Complies with USB 2.0 specification (slave mode only)<br>● Data transmission rates: up to 480 Mbps<br>● Used for AT command communication, data transmission, software debugging, firmware upgrade and GNSS NMEA sentence output<br>● Supports USB serial drivers for Windows 7/8/8.1/10/11, Linux 2.6–6.5, Android 4.x–13.x |
| (U)SIM Interface | ● Supports (U)SIM cards: 1.8/3.0 V |
| SDIO Interface | ● Complies with SD 3.0 protocol |

| | |
|---|---|
| UART | **Main UART:**<br>● Used for AT command communication and data transmission<br>● Baud rate: 115200 bps by default, max. 921600 bps<br>● Supports RTS and CTS hardware flow control<br>**Debug UART:**<br>● Used for the output of partial logs<br>● Baud rate: 115200 bps |
| Audio Features | ● Supports one digital audio interface: PCM interface<br>● WCDMA: AMR and AMR-WB<br>● LTE: AMR and AMR-WB<br>● Supports echo cancellation and noise suppression |
| PCM Interface | ● Used for audio function with external codec<br>● Supports 16-bit linear encoding format<br>● Supports short frame mode<br>● Supports slave mode* and master mode |
| I2C Interface | ● Supports one I2C interface<br>● Complies with I2C bus protocol specifications (100/400 kHz)<br>● The multi-host mode is not supported |
| SPI Interface | ● Supports one SPI interface<br>● Supports master mode only<br>● Clock frequency: up to 52 MHz |
| Network Indication | ● NET_STATUS indicates network activity status |
| AT Commands | ● Complies with *3GPP TS 27.007*, *3GPP TS 27.005*<br>● Complies with Quectel enhanced AT commands |
| Antenna Interfaces | ● Main antenna interface (ANT_MAIN)<br>● Rx-diversity antenna interface (ANT_DRX)<br>● GNSS antenna interface (ANT_GNSS)<br>● 50 Ω characteristic impedance |
| Transmitting Power | ● LTE-FDD: Class 3 (23 dBm ±2 dB)<br>● WCDMA: Class 3 (23 dBm ±2 dB) |
| LTE Features | ● Supports 3GPP Rel-9 non-CA Cat 4 FDD<br>● 1.4 MHz, 3 MHz, 5 MHz, 10 MHz, 15 MHz and 20 MHz RF bandwidths<br>● DL modulations: QPSK, 16QAM, 64QAM<br>● UL modulations: QPSK, 16QAM<br>● DL MIMO<br>● LTE-FDD data transmission rates:<br>– Max. 150 Mbps (DL)<br>– Max. 50 Mbps (UL) |
| UMTS Features | ● Supports 3GPP Rel-7 HSPA+, HSDPA, HSUPA and WCDMA<br>● Modulations: QPSK, 16QAM and 64QAM<br>● Max. data transmission rates:<br>HSPA+: 21 Mbps (DL)<br>HSUPA: 5.76 Mbps (UL) |

| | |
|---|---|
| | WCDMA: 384 kbps (DL)/384 kbps (UL) |
| GNSS Features [1] | ● GPS, GLONASS, BDS and QZSS<br>● Complies with NMEA 0183 protocol<br>● Data update rate: 1 Hz by default, max. 5 Hz |
| Internet Protocol Features | ● Complies with TCP, UDP, PPP, NTP, NITZ, FTP, HTTP, PING, CMUX, HTTPS, FTPS, SSL, FILE, MQTT, MMS, SMTP and SMTPS protocols<br>● Supports PAP and CHAP for PPP connections |
| Temperature Ranges | ● Operating temperature range [2]: -35 °C to +75 °C<br>● Extended temperature range [3]: -40 °C to +85 °C<br>● Storage temperature range: -40 °C to +90 °C |
| Firmware Upgrade | ● USB 2.0<br>● DFOTA |
| RoHS | ● All hardware components are fully compliant with EU RoHS directive |

## 2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband part
- Flash
- Radio frequency part
- Peripheral interfaces

[1] GNSS function is only supported by EG950A-EL module, and the function is optional. Only the module with built-in GNSS function has GNSS antenna interface.
[2] Within the operating temperature range, the module meets 3GPP specifications.
[3] Within the extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, emergency call, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as $P_{out}$, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

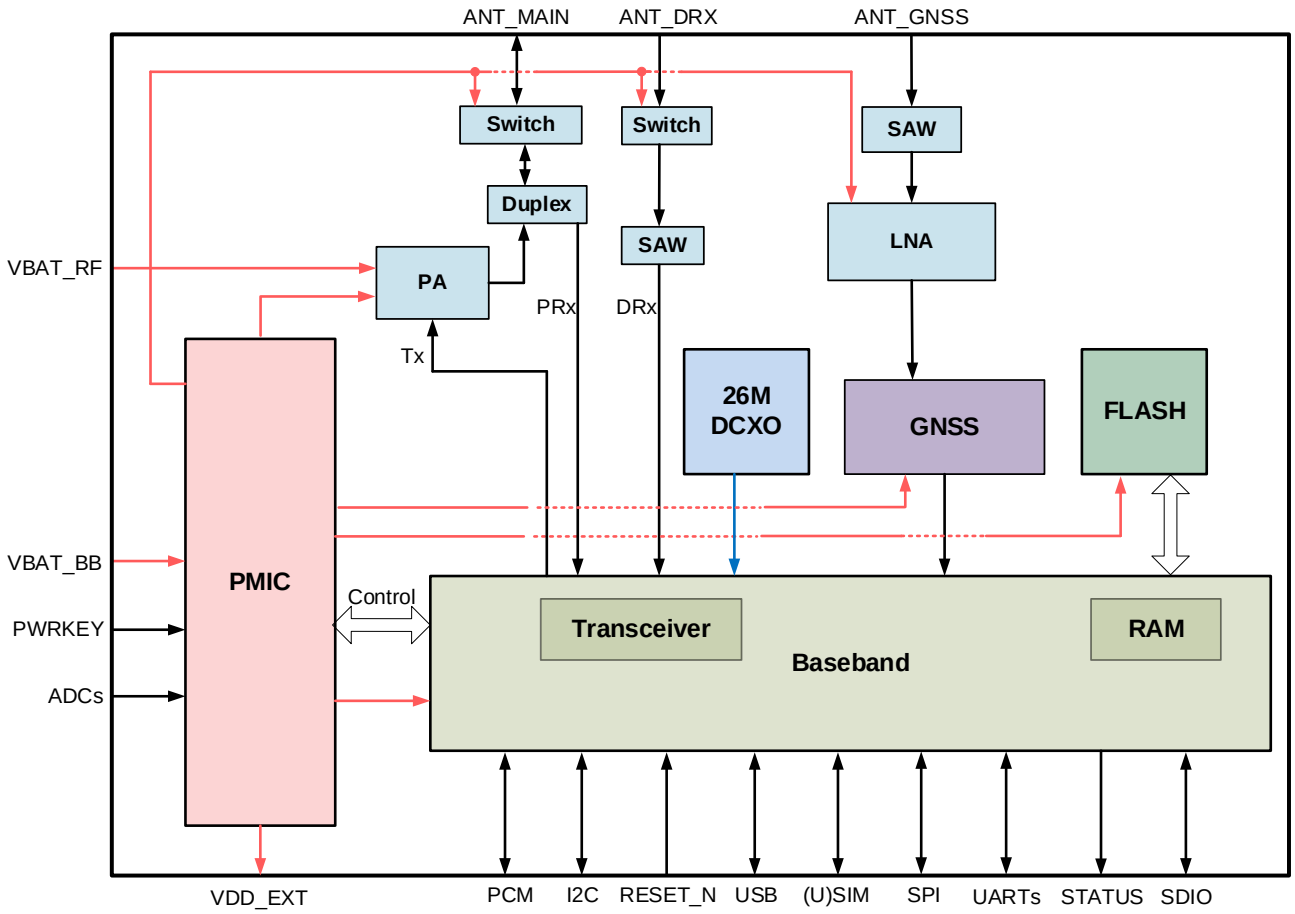



**Figure 1: Functional Diagram**

## 2.4. Pin Assignment


**Figure 2: Pin Assignment (Top View)**

**NOTE**

1. Keep all RESERVED pins and unused pins open and connect all GND pins to the ground network.
2. If the module is turned on normally, the USB_BOOT pin is prohibited to be pulled up to high level until the module is powered on successfully.

## 2.5. Pin Description

**Table 5: Parameter Definition**

| Parameter | Description |
|---|---|
| AI | Analog Input |
| AIO | Analog Input/Output |
| DI | Digital Input |
| DIO | Digital Input/Output |
| DO | Digital Output |
| OD | Open Drain |
| PI | Power Input |
| PO | Power Output |

DC characteristics include power domain and rated current.

**Table 6: Pin Description**

| **Power Supply** | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| VBAT_BB | 32, 33 | PI | Power supply for the module's baseband part | Vmin = 3.4 V<br>Vnom = 3.8 V<br>Vmax = 4.5 V | It must be provided with sufficient current of at least 2.0 A. |
| VBAT_RF | 52, 53 | PI | Power supply for the module's RF part | | It must be provided with sufficient current of at least 0.5 A. |
| VDD_EXT | 29 | PO | Provides 1.8 V for external circuit | Vmin = 1.67 V<br>Vnom = 1.8 V<br>Vmax = 1.93 V<br>$I_O$max = 50 mA | It can provide a pull-up power to the external GPIO.<br>A test point is recommended to be reserved. |
| GND | 3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102 | | | | |

| Turn On/Off | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| PWRKEY | 15 | DI | Turn on/off the module | $V_{IL}$max = 0.5 V | VBAT power domain. Active low. |
| RESET_N | 17 | DI | Reset the module | $V_{IL}$max = 0.5 V | 1.8 V power domain. Active low after turn-on. A test point is recommended to reserved. |
| **Indication Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| STATUS | 20 | DO | Indicate the module's operation status | VDD_EXT | 1.8 V power domain. If unused, keep them open. |
| NET_STATUS | 21 | DO | Indicate the module's network activity status | | |
| SLEEP_IND | 1 | DO | Indicate the module's sleep mode | | |
| **USB Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| USB_VBUS | 8 | AI | USB connection detect | Vmin = 3.0 V<br>Vnom = 5.0 V<br>Vmax = 5.25 V | Typ. 5.0 V. A test point must be reserved. |
| USB_DP | 9 | AIO | USB 2.0 differential data (+) | | 90 Ω differential impedance. USB 2.0 compliant. Test points must be reserved. |
| USB_DM | 10 | AIO | USB 2.0 differential data (-) | | |
| **(U)SIM Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| USIM_VDD | 43 | PO | (U)SIM card power supply | **Low-voltage:**<br>Vmin = 1.67 V<br>Vnom = 1.8 V<br>Vmax = 1.93 V<br>**High-voltage:**<br>Vmin = 2.7 V<br>Vnom = 3.0 V | Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. |

| | | | | | |
|---|---|---|---|---|---|
| | | | | Vmax = 3.3 V | |
| USIM_DATA | 45 | DIO | (U)SIM card data | USIM_VDD | |
| USIM_CLK | 46 | DO | (U)SIM card clock | | |
| USIM_RST | 44 | DO | (U)SIM card reset | | |
| USIM_DET | 42 | DI | (U)SIM card hot-plug detect | VDD_EXT | 1.8 V power domain. If unused, keep it open. |
| USIM_GND | 47 | - | Specified ground for (U)SIM card | | Connect to the ground of (U)SIM card. |
| **Main UART Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| MAIN_CTS | 36 | DO | Clear to send signal from the module | VDD_EXT | Connect to MCU's CTS. 1.8 V power domain. If unused, keep it open. |
| MAIN_RTS | 37 | DI | Request to send signal to the module | | Connect to MCU's RTS. 1.8 V power domain. If unused, keep it open. |
| MAIN_RXD | 34 | DI | Main UART receive | | 1.8 V power domain. If unused, keep them open. |
| MAIN_TXD | 35 | DO | Main UART transmit | | |
| MAIN_DCD | 38 | DO | Main UART data carrier detect | | |
| MAIN_RI | 39 | DO | Main UART ring indication | | |
| MAIN_DTR | 30 | DI | Main UART data terminal ready | | |
| **Debug UART Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| DBG_RXD | 22 | DI | Debug UART receive | VDD_EXT | 1.8 V power domain. Test points must be reserved. |
| DBG_TXD | 23 | DO | Debug UART transmit | | |

| I2C Interface | | | | | |
|---|---|---|---|---|---|
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| I2C_SCL | 40 | OD | I2C serial clock | | 1.8 V pull-up resistor is needed.<br>If unused, keep them open. |
| I2C_SDA | 41 | OD | I2C serial data | | |
| **PCM Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| PCM_SYNC | 5 | DIO | PCM data frame sync | VDD_EXT | 1.8 V power domain.<br>When the module is used as a master device, the pins are in output state;<br>When the module is used as a slave device*, the pins are in input state.<br>If unused, keep them open. |
| PCM_CLK | 4 | DIO | PCM clock | | |
| PCM_DIN | 6 | DI | PCM data input | | If unused, keep them open. |
| PCM_DOUT | 7 | DO | PCM data output | | |
| **SDIO Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| SDIO_VDD | 93 | PO | SDIO power supply | **Low-voltage:**<br>Vmin = 1.67 V<br>Vnom = 1.8 V<br>Vmax = 1.93 V<br><br>**High-voltage:**<br>Vmin = 2.7 V<br>Vnom = 2.85 V<br>Vmax = 3.05 V | 1.8/2.85 V configurable output voltage. |
| SDIO_DATA0 | 11 | DIO | SDIO data bit 0 | SDIO_VDD | 1.8/2.85 V power domain.<br>If unused, keep them open. |
| SDIO_DATA1 | 12 | DIO | SDIO data bit 1 | | |
| SDIO_DATA2 | 13 | DIO | SDIO data bit 2 | | |

| | | | | | |
|---|---|---|---|---|---|
| SDIO_DATA3 | 14 | DIO | SDIO data bit 3 | | |
| SDIO_CMD | 66 | DIO | SDIO command | | |
| SDIO_CLK | 65 | DO | SDIO clock | | |
| SDIO_DET* | 83 | DI | SD card hot-plug detect | VDD_EXT | 1.8 V power domain. If unused, keep it open. |
| **RF Antenna Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| ANT_MAIN | 60 | AIO | Main antenna interface | | 50 Ω characteristic impedance. |
| ANT_DRX | 56 | AI | Diversity antenna interface | | |
| ANT_GNSS | 49 | AI | GNSS antenna interface | | 50 Ω characteristic impedance. If unused, keep it open. |
| **SPI Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| SPI_CLK | 26 | DO | SPI clock | VDD_EXT | Master mode only. 1.8 V power domain. If unused, keep them open. |
| SPI_CS | 25 | DO | SPI chip select | | |
| SPI_DIN | 28 | DI | SPI data input | | |
| SPI_DOUT | 27 | DO | SPI data output | | |
| **ADC Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| ADC0 | 24 | AI | General-purpose ADC interface | Voltage Range: 0 V–VBAT_BB | If unused, keep them open. |
| ADC1 | 2 | AI | | | |
| **GNSS Interface** | | | | | |
| **Pin Name** | **Pin No.** | **I/O** | **Description** | **DC Characteristics** | **Comment** |
| GNSS_PPS* | 78 | DO | GNSS Pulse Per Second | | |
| **Other Interface** | | | | | |

| Pin Name | Pin No. | I/O | Description | DC Characteristics | Comment |
|---|---|---|---|---|---|
| USB_BOOT | 75 | DI | Forces the module to enter emergency download mode | VDD_EXT | 1.8 V power domain. Active high. A test point is recommended to be reserved. |
| W_DISABLE# | 18 | DI | Airplane mode control | | 1.8 V power domain. Pull-up by default. In low voltage level, the module can enter airplane mode. If unused, keep it open. |
| AP_READY* | 19 | DI | Application processor ready | | 1.8 V power domain. If unused, keep it open. |
| **RESERVED Pins** | | | | | |
| **Pin Name** | **Pin No.** | | | | **Comment** |
| RESERVED | 16, 51, 57, 63, 64, 76, 77, 84–88, 92, 94–99 | | | | Keep these pins open. |

**NOTE**

If antenna tuning control is required, please contact Quectel Technical Support.

## 2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (UMTS&LTE EVB) with accessories to develop or test the module. For more details, see ***document [1]***.

# 3 Operating Characteristics

## 3.1. Operating Modes

**Table 7: Operating Modes Overview**

| Mode | Descriptions | |
|---|---|---|
| Full Functionality Mode | Idle | Software is active. The module is registered on the network but has no data interaction with the network. |
| | Voice/Data | Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate. |
| Minimum Functionality Mode | **AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid. | |
| Airplane Mode | **AT+CFUN=4** or pulling down W_DISABLE# pin can set the module into airplane mode. In this case, RF function will be invalid. | |
| Sleep Mode | In this mode, current consumption of the module will be reduced to the minimal level. The module can still receive paging, SMS, voice call and TCP/UDP data from network. | |
| Power Down Mode | In this mode, the VBAT power supply is constantly turned on and the software stops working. | |

**NOTE**

For more details about **AT+CFUN**, see ***document [2]***.

## 3.2. Sleep Mode

In sleep mode, the module can reduce power consumption to a very low level, the following section describes power saving procedures.

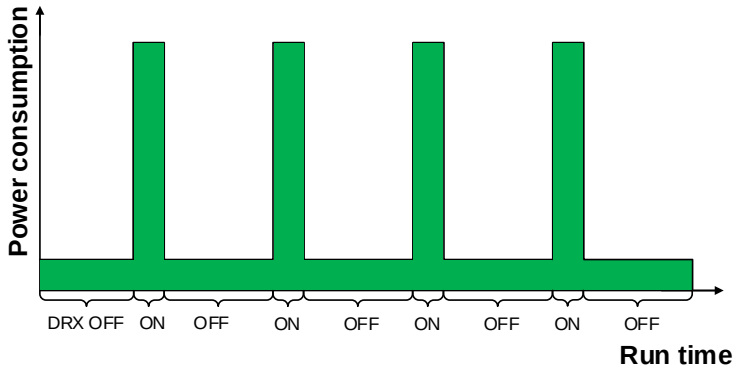



**Figure 3: Module Power Consumption in Sleep Mode**

**NOTE**

DRX cycle values are transmitted over the wireless network.

### 3.2.1. UART Application Scenario

If the module communicates with the MCU via main UART interface, the following preconditions should be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Drive MAIN_DTR high or keep it open.
- Drive USB_VBUS low or keep it open.

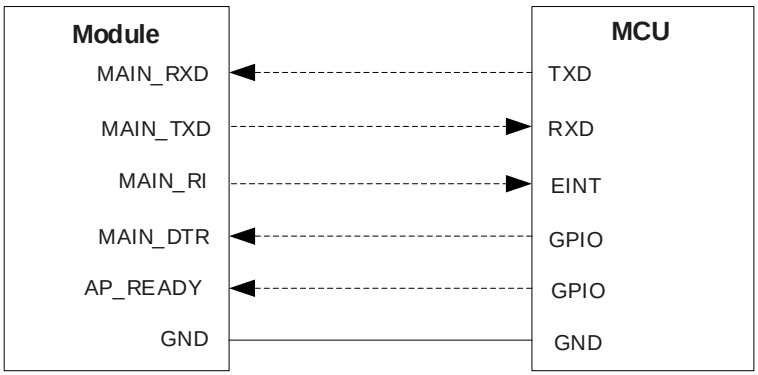



**Figure 4: Sleep Mode Application via UART**

Driving MAIN_DTR low by MCU will wake up the module.

When the module has a URC to report, MAIN_RI signal will wake up the MCU. Please refer to ***Chapter 4.10.3*** for details about MAIN_RI behavior.

### 3.2.2. USB Application Scenarios

For the two situations "USB application with USB remote wakeup function" and "USB application with USB suspend/resume and MAIN_RI function" below, three preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1**.
- Drive MAIN_DTR high or keep it open.
- Ensure that the host's USB bus, which is connected to the module's USB interface, enters suspend state.

#### 3.2.2.1. USB Application with USB Suspend/Resume and USB Remote Wakeup Function

The host supports USB suspend/resume and remote wakeup function.

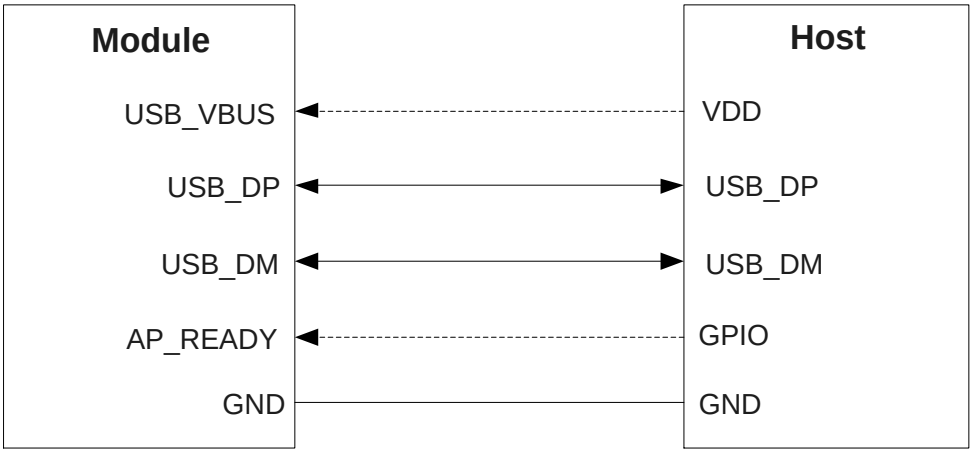



**Figure 5: Block Diagram of Application with USB Remote Wakeup Function in Sleep Mode**

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

#### 3.2.2.2. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB suspend/resume but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

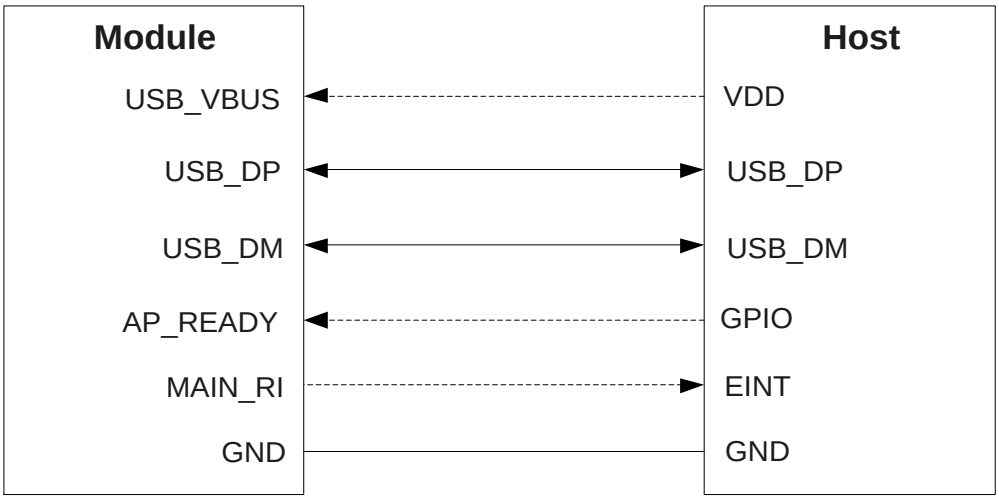



**Figure 6: Block Diagram of Application with NAIN_RI Function in Sleep Mode**

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will wake up the host through MAIN_RI signal.

#### 3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, the following three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Drive MAIN_DTR high or keep it open.
- Ensure that USB_VBUS is disconnected via the external control circuit.

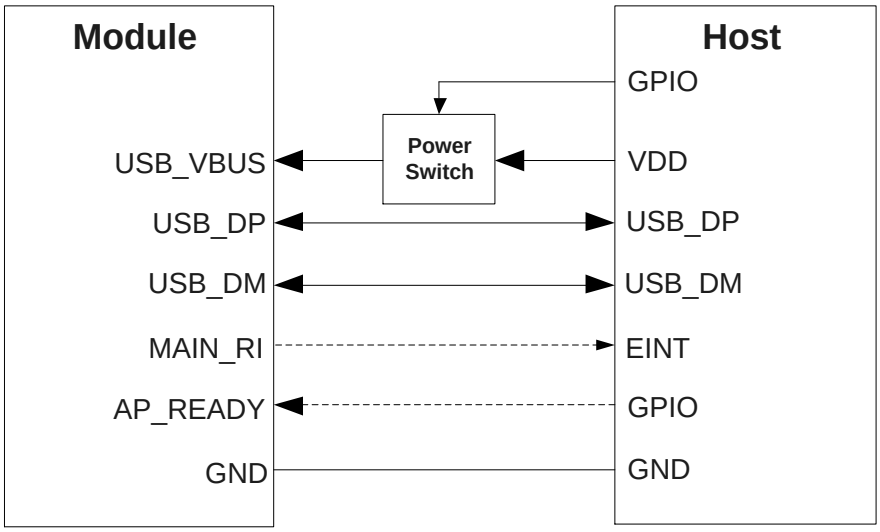



**Figure 7: Block Diagram of Application Without USB Suspend Function in Sleep Mode**

Restoring the power supply of USB_VBUS will wake up the module.

**NOTE**

Pay attention to the level matching shown in the dotted connection signal between the module and the MCU/host.

## 3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

**Hardware:**

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving the pin low can make the module enter airplane mode.

**Software:**

**AT+CFUN=<fun>** provides choices of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (Both (U)SIM and RF functions are disabled).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (RF function is disabled).

**NOTE**

For more details about AT command, see ***document [2]***.

## 3.4. Power Supply

### 3.4.1. Power Supply Pins

The module provides four VBAT pins dedicated to the connection with the external power supply.

**Table 8: VBAT and GND Pins**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| VBAT_BB | 32, 33 | PI | Power supply for the module's baseband part | It must be provided with sufficient current of at least 2.0 A. |
| VBAT_RF | 52, 53 | PI | Power supply for the module's RF part | It must be provided with sufficient current of at least 0.5 A. |
| GND | 3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102 | | | |

### 3.4.2. Reference Design for Power Supply

Power design for the module is essential. The power supply of the module should be able to provide sufficient current of at least 2.5 A. If the voltage difference between input and output is small, it is suggested to use an LDO; If there is a big voltage difference, a buck converter is recommended to use.

The following figure shows a reference design for +5 V input power source.

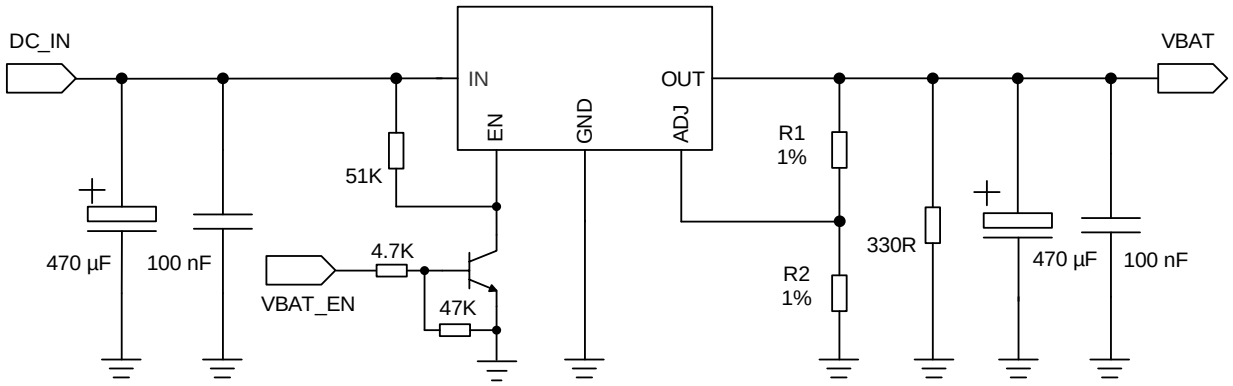



**Figure 8: Reference Design of Power Supply**

**NOTE**

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply. It is recommended to design a switch at the power supply.

### 3.4.3. Voltage Stability Requirements

The power supply range of the module is from 3.4 V to 4.5 V. Make sure the input voltage will never drop below 3.4 V.

To decrease voltage drop, a filter capacitor of about 100 µF with low ESR (ESR ≤ 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star configuration routing. The width of VBAT_BB trace should be not less than 2 mm; and the width of VBAT_RF trace should be not less than 1 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used.

The following figure shows the star configuration routing of the power supply.

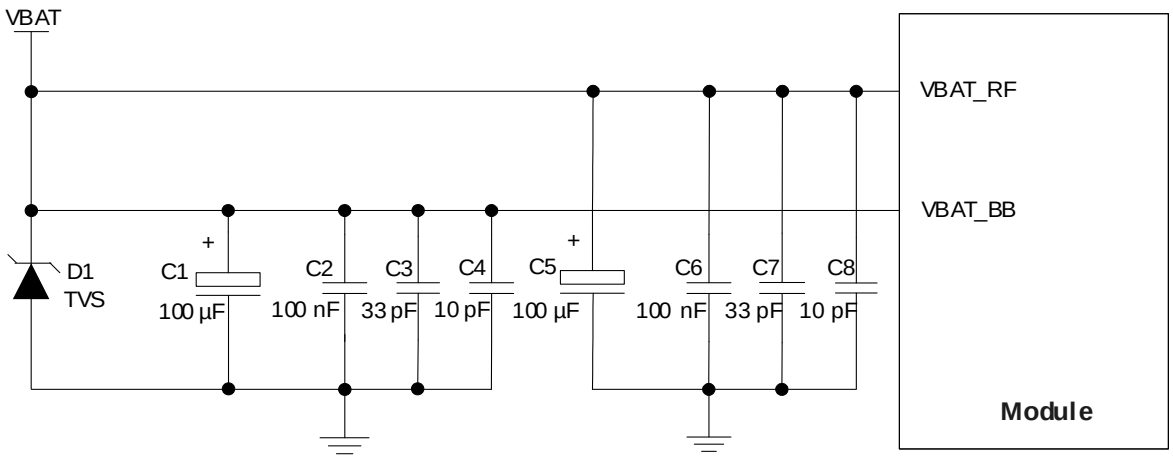



**Figure 9: Star Configuration of Power Supply**

### 3.4.4. Power Supply Voltage Monitoring

You can use **AT+CBC** to monitor and query the VBAT_BB voltage. For details, see ***document [2]***.

## 3.5. Turn On

### 3.5.1. Turn On the Module with PWRKEY

**Table 9: Pin Definition of PWRKEY**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| PWRKEY | 15 | DI | Turn on/off the module | VBAT power domain.<br>Active low. |

When the module is in power-off mode, it can be turned on to normal mode by driving the PWRKEY pin low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

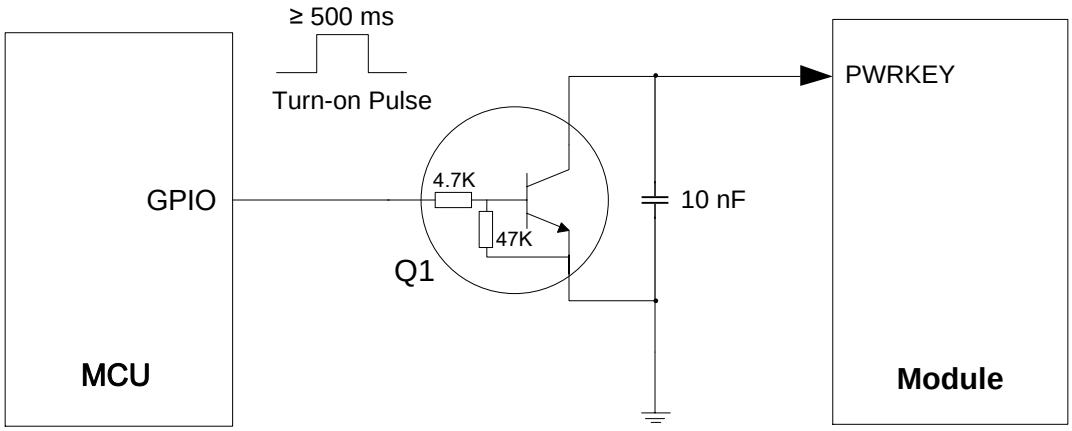



**Figure 10: Reference Circuit of Turning On the Module Using Driving Circuit**

The other way to control the PWRKEY is using a button directly. When pressing the button, electrostatic strike may be generated from finger. Therefore, an ESD device should be placed near the button for electrostatic protection. The reference circuit is as follows.

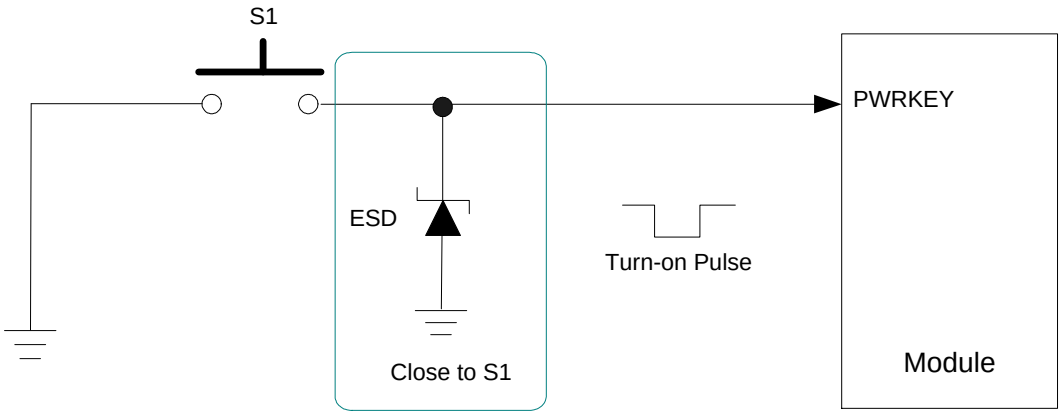



**Figure 11: Reference Circuit of Turning On the Module with Button**

The power-up scenario is illustrated in the following figure.

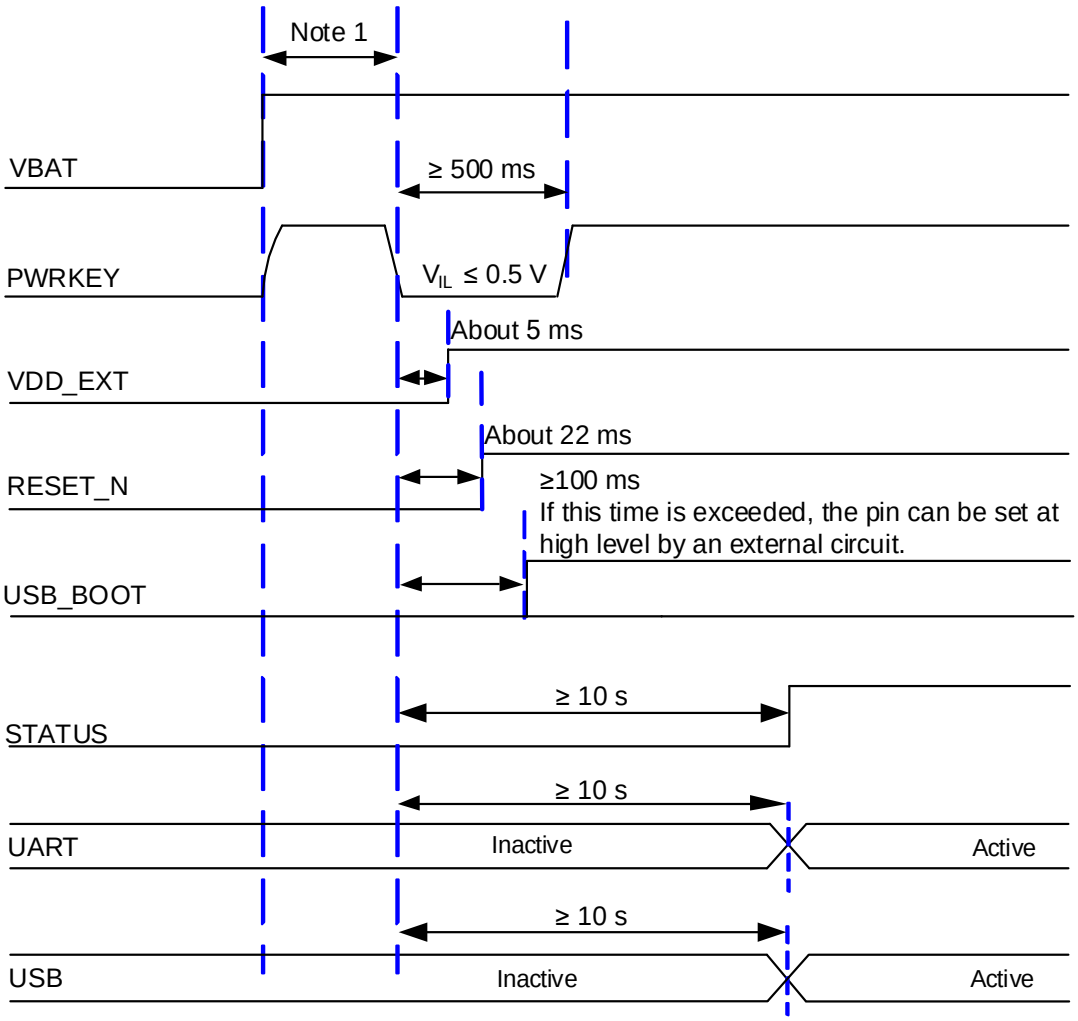



**Figure 12: Power-up Timing**

**NOTE**

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is not less than 450 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 4.7 kΩ resistor if module needs to be powered on automatically and shutdown is not needed.

## 3.6. Turn Off

The module can be normally turned off in the following ways:

- Control the PWRKEY pin.
- Send the **AT+QPOWD**. For details of the **AT+QPOWD**, see ***document [2]***.

### 3.6.1. Turn Off the Module with PWRKEY

Driving the PWRKEY low for at least 650 ms, and then the module will execute power-down procedure after the PWRKEY is released. The timing of power-down is illustrated in the following figure.

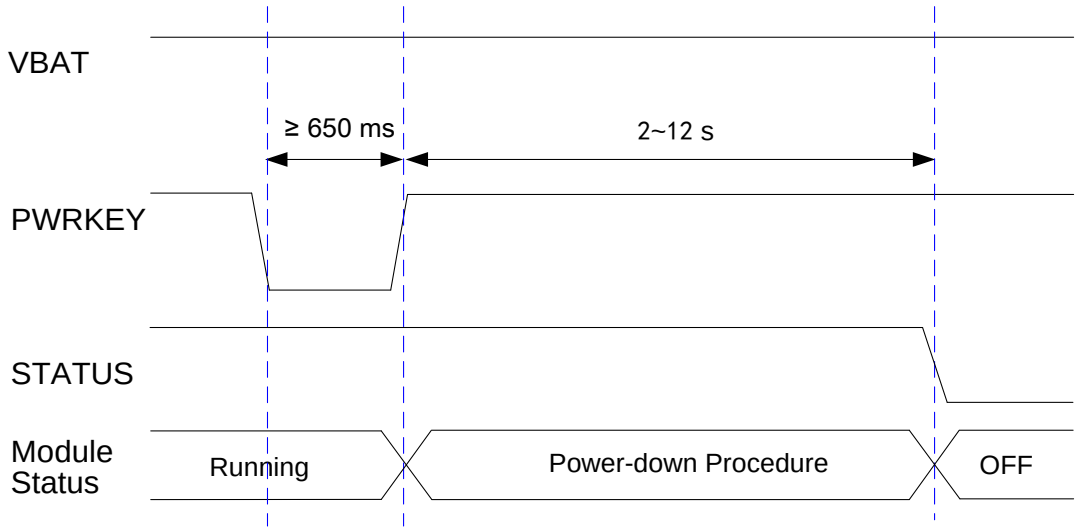



**Figure 13: Power-down Timing**

During the turn-off process, the module needs to log out from network. The logout time is related to the current network state, and it is measured to take about 2 to 12 s. Therefore, it is recommended to power off or restart the module after 12 s to ensure that the important software data is saved before the module is completely shut down.

### 3.6.2. Turn Off with AT Command

Execute **AT+QPOWD** to turn off the module, which has similar timing and effect as turning off the module through driving PWRKEY low.

**NOTE**

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

## 3.7. Reset

The module can be reset by driving RESET_N low for at least 300 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

**Table 10: Pin Definition of RESET_N**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| RESET_N | 17 | DI | Reset the module | 1.8 V power domain. Active low after turn-on.<br>A test point is recommended to be reserved. |

The recommended circuit is equal to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

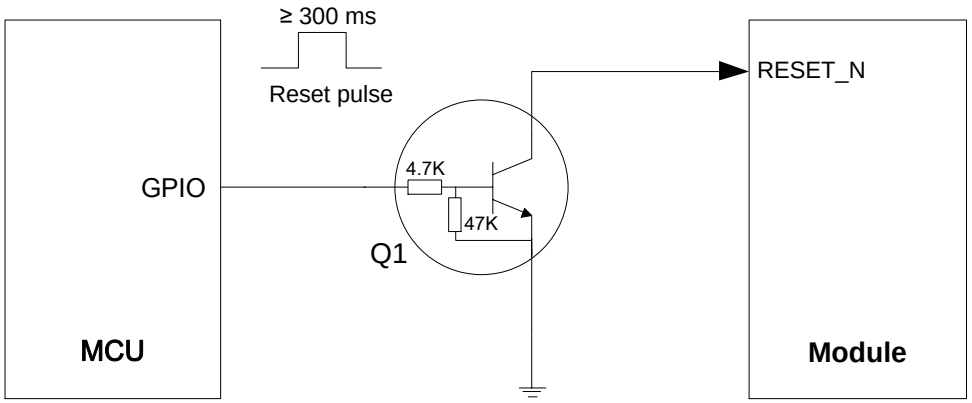



**Figure 14: Reference Circuit of RESET_N with Driving Circuit**

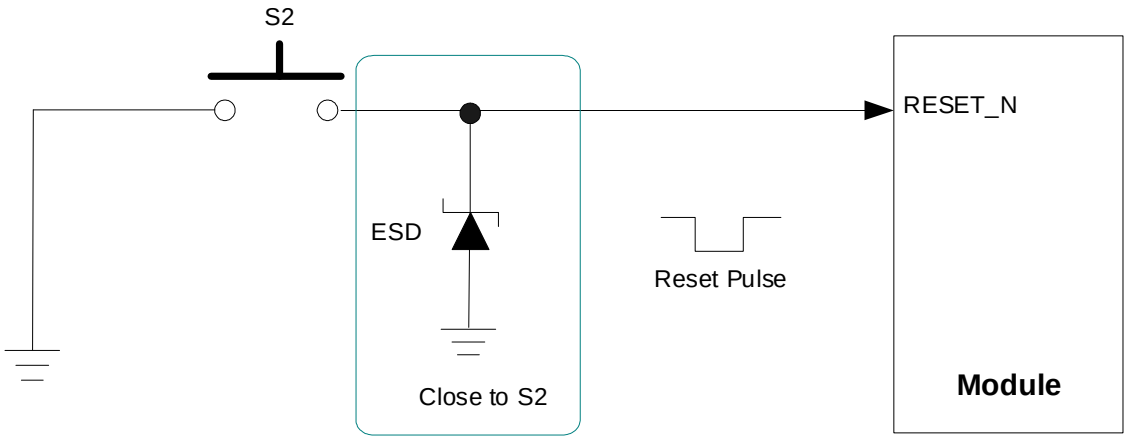



**Figure 15: Reference Circuit of RESET_N with Button**

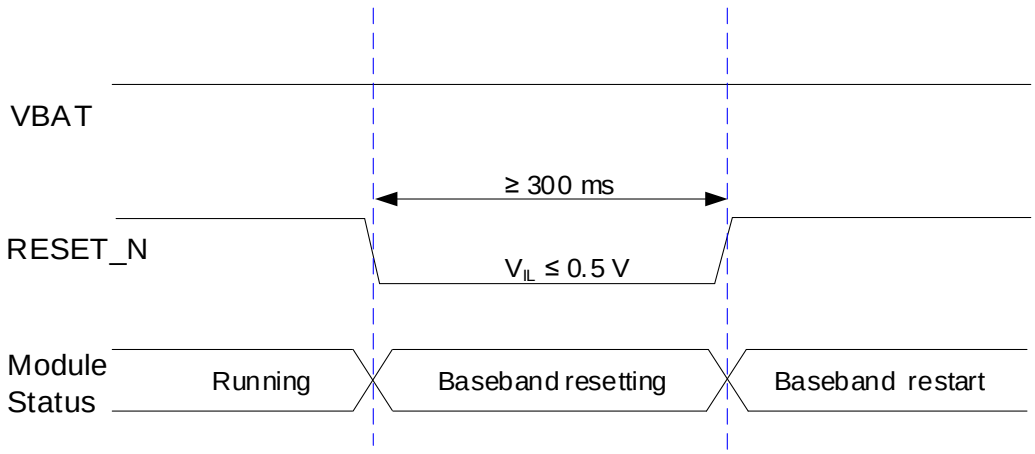



**Figure 16: Timing of Reset**

**NOTE**

1. RESET_N only resets the internal baseband chip of the module and does not reset the power management chip.
2. Ensure that the capacitance on PWRKEY and RESET_N does not exceed 10 nF.

# 4 Application Interfaces

## 4.1. USB Interface

The module provides one USB interface which complies with the USB 2.0 specifications and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface only supports USB slave mode and it can be used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging and firmware upgrade.

**Table 11: Pin Definition of USB Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| USB_VBUS | 8 | AI | USB connection detect | Typ. 5.0 V.<br>A test point must be reserved. |
| USB_DP | 9 | AIO | USB 2.0 differential data (+) | 90 Ω differential impedance.<br>USB 2.0 compliant.<br>Test points must be reserved. |
| USB_DM | 10 | AIO | USB 2.0 differential data (-) | |

Test points must be reserved for debugging and firmware upgrading in your designs.

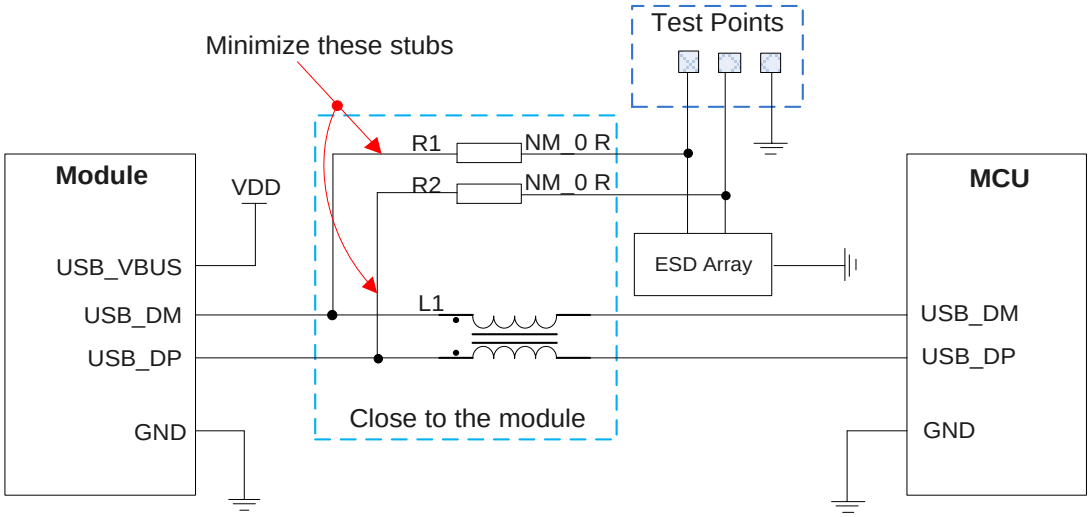



**Figure 17: Reference Design of USB 2.0 Interface**

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI spurious transmission. Meanwhile, it is also suggested to add R1 and R2 in series between the module and the test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, you should place L1, R1 and R2 close to the module, and keep the resistors close to each other. Moreover, keep extra stubs of trace as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- For USB 2.0 signal traces, length matching of differential data pair (USB_DP/USB_DM) should not exceed 1 mm.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on the same layer and with ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data traces. Typically, the stray capacitance should not exceed 2 pF for USB 2.0.
- If possible, reserve one 0 Ω resistor on USB_DP and USB_DM traces respectively.

For more details about the USB specifications, visit http://www.usb.org/home.

## 4.2. USB_BOOT Interface

USB_BOOT is for emergency download. You can pull up USB_BOOT to VDD_EXT or a 1.8 V external power before powering on the module, thus the module will enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

**Table 12: Pin Definition of USB_BOOT Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| USB_BOOT | 75 | DI | Forces the module to enter emergency download mode | 1.8 V power domain. Active high. A test point is recommended to be reserved. |

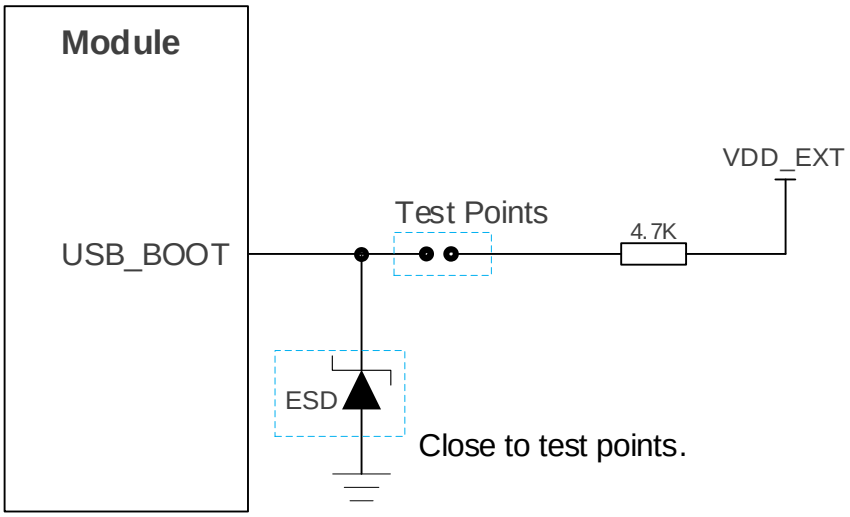



**Figure 18: Reference Circuit of USB_BOOT Interface**

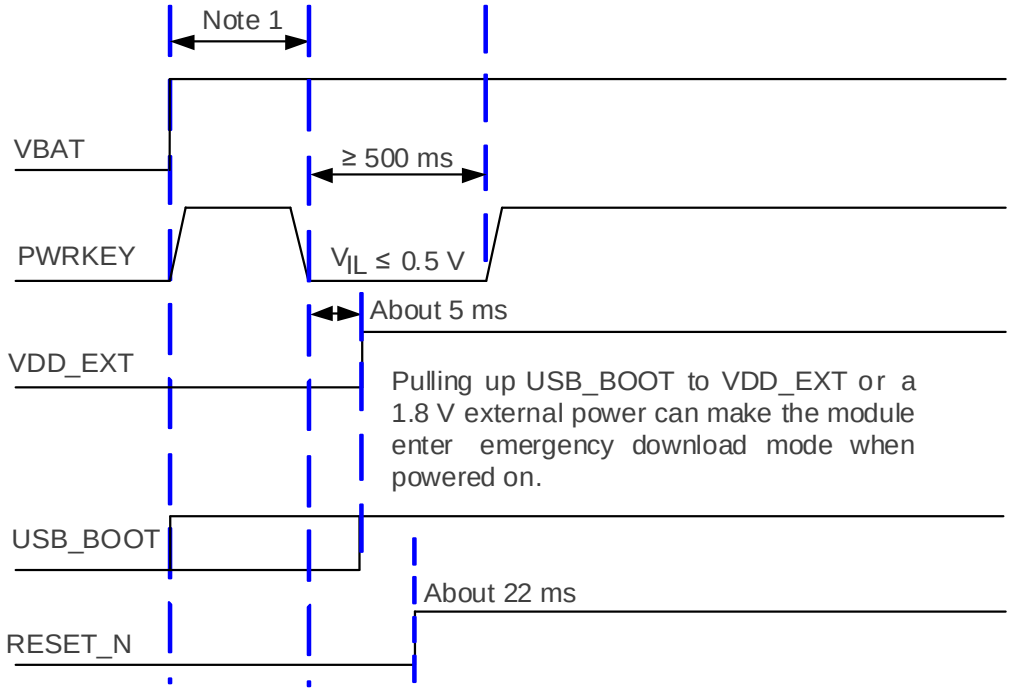



**Figure 19: Timing Sequence for Entering Emergency Download Mode**

**NOTE**

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time between powering up VBAT and pulling down PWRKEY pin is not less than 450 ms.
2. When using MCU to control module to enter the emergency download mode, please follow the above timing sequence. Directly connect the test points as shown in ***Figure 18*** can manually force the module into download mode.
3. If the module is turned on normally, the USB_BOOT pin is prohibited to be pulled up to high level until the module is powered on successfully.

## 4.3. (U)SIM Interface

The (U)SIM interface circuitry meets ETSI and IMT-2000 requirements. Both 1.8 V and 3.0 V (U)SIM cards are supported.

**Table 13: Pin Definition of (U)SIM Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| USIM_VDD | 43 | PO | (U)SIM card power supply | Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module. |
| USIM_DATA | 45 | DIO | (U)SIM card data | |
| USIM_CLK | 46 | DO | (U)SIM card clock | |
| USIM_RST | 44 | DO | (U)SIM card reset | |
| USIM_DET | 42 | DI | (U)SIM card hot-plug detect | 1.8 V power domain.<br>If unused, keep it open. |
| USIM_GND | 47 | - | Specified ground for (U)SIM card | Connect to GND of the (U)SIM card |

The module supports (U)SIM card hot-plug via the USIM_DET pin, and both low and high level detections are supported. By default, the function is disabled, and it can be configured via **AT+QSIMDET**. Please see ***document [2]*** for details about the command.

The reference circuit of the 8-pin (U)SIM interface is as follows.

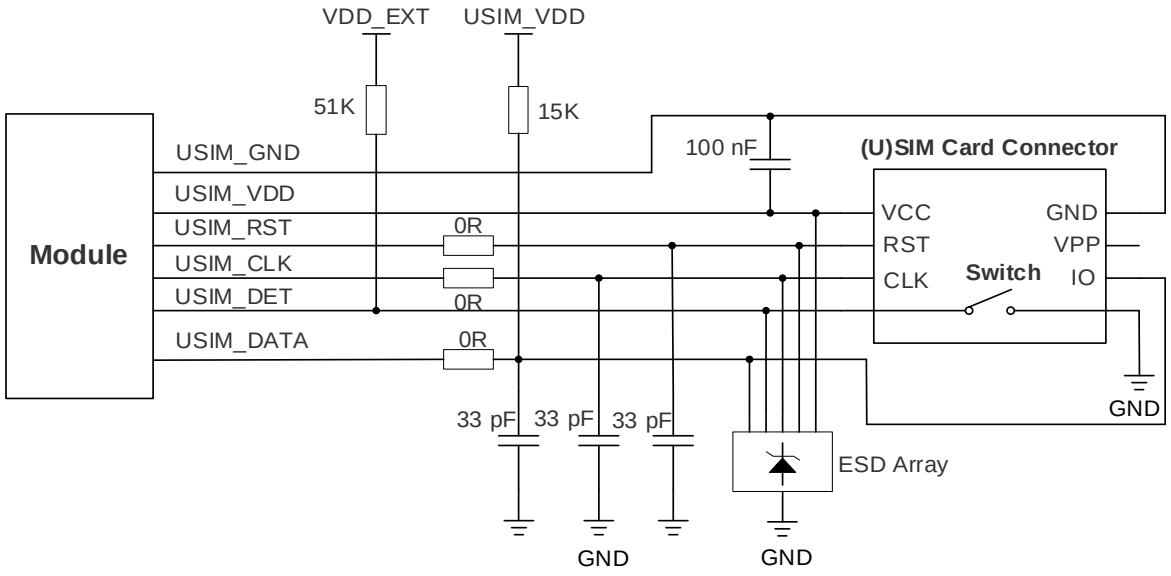



**Figure 20: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector**

If (U)SIM card detection function is not needed, keep USIM_DET unconnected.

A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

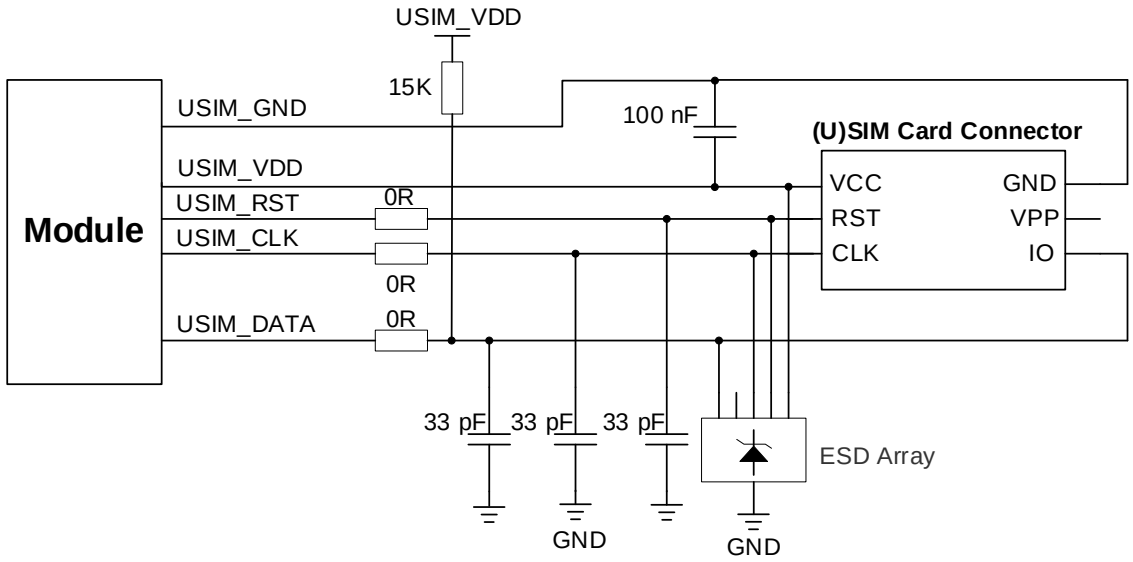



**Figure 21: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector**

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Place the (U)SIM card connector close to the module. Keep the trace length less than 200 mm if possible.

- Route (U)SIM card differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Ensure that the bypass capacitor between USIM_VDD and GND does not exceed 1 μF.
- Ensure the tracing between ground of the (U)SIM card connector and USIM_GND is short and wide. Keep the trace width of USIM_GND and USIM_VDD at least 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with ground surrounded.
- The (U)SIM peripheral circuit should be close to the (U)SIM card connector. In order to offer good ESD protection, it is recommended to add an ESD protection component whose parasitic capacitance should not exceed 15 pF. The 0 Ω resistors should be added in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors on the USIM_DATA, USIM_CLK and USIM_RST traces are used for filtering interference.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a 15 kΩ pull-up resistor near the (U)SIM card connector.

## 4.4. SDIO Interface

The module provides one SDIO interface which supports SD 3.0 protocol.

**Table 14: Pin Definition of SDIO Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| SDIO_VDD | 93 | PO | SDIO power supply | 1.8/2.85 V configurable output voltage. |
| SDIO_DATA0 | 11 | DIO | SDIO data bit 0 | 1.8/2.85 V power domain.<br>If unused, keep them open. |
| SDIO_DATA1 | 12 | DIO | SDIO data bit 1 | |
| SDIO_DATA2 | 13 | DIO | SDIO data bit 2 | |
| SDIO_DATA3 | 14 | DIO | SDIO data bit 3 | |
| SDIO_CMD | 66 | DIO | SDIO command | |
| SDIO_CLK | 65 | DO | SDIO clock | |
| SDIO_DET* | 83 | DI | SD card hot-plug detect | 1.8 V power domain.<br>If unused, keep it open. |

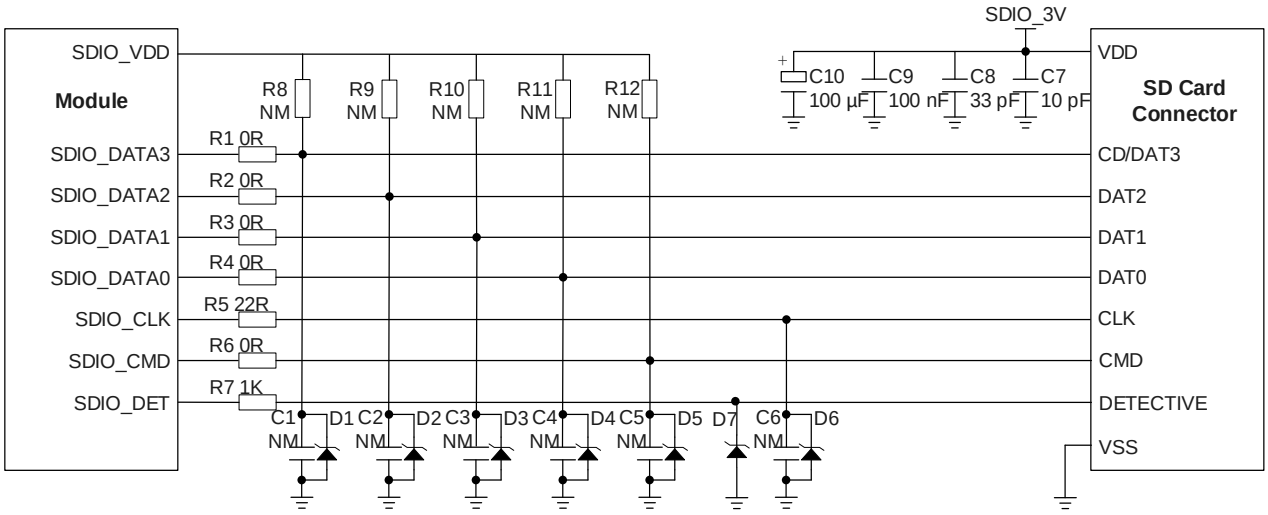



**Figure 22: Reference Circuit of SD Card Interface**

To ensure communication performance, the following conditions should be taken into considerations when designing SDIO interface:

- The voltage range of SDIO_3V is 2.7–3.6 V and it should be provided 200–800 mA current by an external power supply SDIO_VDD provides up to 50 mA current and can only be used for pull-up resistor of SDIO bus.
- To avoid the impact of jitter, pull up SDIO_CMD and SDIO_DATA[0:3] to SDIO_VDD with R8–R12. Resistance of these resistors can be 10–100 kΩ and the recommended value is 100 kΩ.
- In order to adjust the signal quality, it is recommended to add resistors R1–R7 in series between the module and the SDIO device. The recommended resistance of R5 and R7 is 22 Ω and 1 kΩ respectively, and the others is 0 Ω. The bypass capacitors C1–C6 are reserved and not mounted by default. The resistor R5 must be placed close to the module.
- Add an ESD protection component with capacitance value of not more than 8 pF near the SD card connector for better ESD protection.
- It is important to route SDIO signal traces at the inner-layer of the PCB and surround the traces with ground on that layer and ground planes above and below. The impedance of SDIO signal trace is 50 Ω ±10 %.
- Keep SDIO signal traces far away from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals and analog signals, as well as noise signals generated by clock, DC-DC, etc.
- It is recommended to keep the traces of SDIO_CLK and SDIO_DATA [0:3]/SDIO_CMD equal in length (the difference among them should be less than 1 mm).
- Keep the adjacent trace clearance twice the trace width and the load capacitance of SDIO bus less than 15 pF.

## 4.5. UART

The module provides two UART interfaces: the main UART interface and the debug UART interface. The following shows their features.

**Table 15: UART Information**

| Interface | Supported Baud Rate (bps) | Default Baud Rate (bps) | Function |
|---|---|---|---|
| Main UART | 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 | 115200 | Used for data transmission and AT command communication.<br>Supports RTS and CTS hardware flow control. |
| Debug UART | 115200 | 115200 | Used for the output of partial logs |

**Table 16: Pin Definition of Main UART Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| MAIN_CTS | 36 | DO | Clear to send signal from the module | Connect to MCU's CTS.<br>1.8 V power domain.<br>If unused, keep it open. |
| MAIN_RTS | 37 | DI | Request to send signal to the module | Connect to MCU's RTS.<br>1.8 V power domain.<br>If unused, keep it open. |
| MAIN_RXD | 34 | DI | Main UART receive | 1.8 V power domain.<br>If unused, keep them open. |
| MAIN_TXD | 35 | DO | Main UART transmit | |
| MAIN_DCD | 38 | DO | Main UART data carrier detect | |
| MAIN_RI | 39 | DO | Main UART ring indication | |
| MAIN_DTR | 30 | DI | Main UART data terminal ready | |
| DBG_RXD | 22 | DI | Debug UART receive | 1.8 V power domain.<br>Test points must be reserved. |
| DBG_TXD | 23 | DO | Debug UART transmit | |

The module provides a 1.8 V UART interface. A voltage-level translator should be used if the application is equipped with a 3.3 V UART interface. The voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

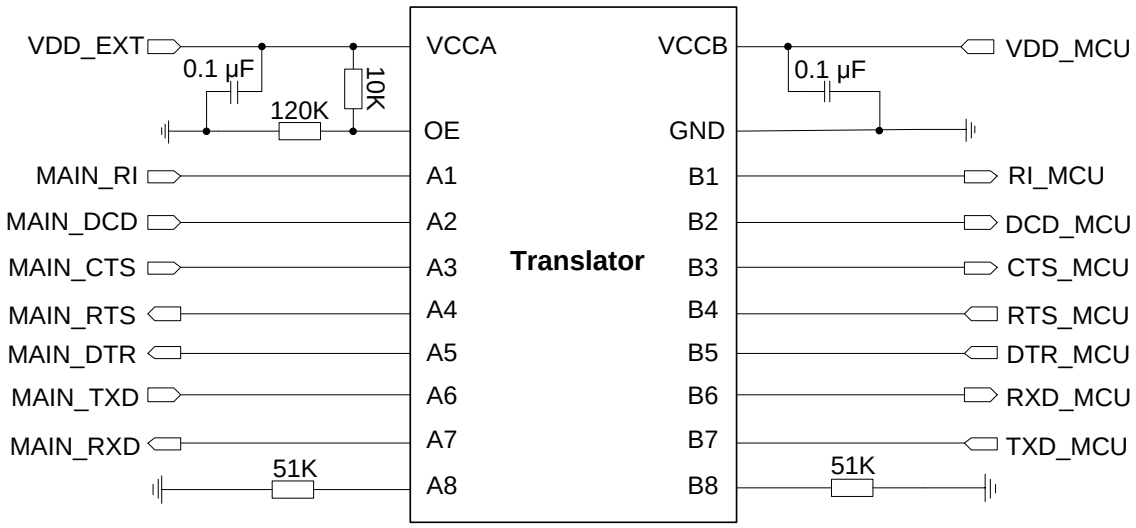



**Figure 23: Reference Design of UART with Level-shifting Chip**

Please visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, please refer to that shown in solid lines, but pay attention to the direction of connection.

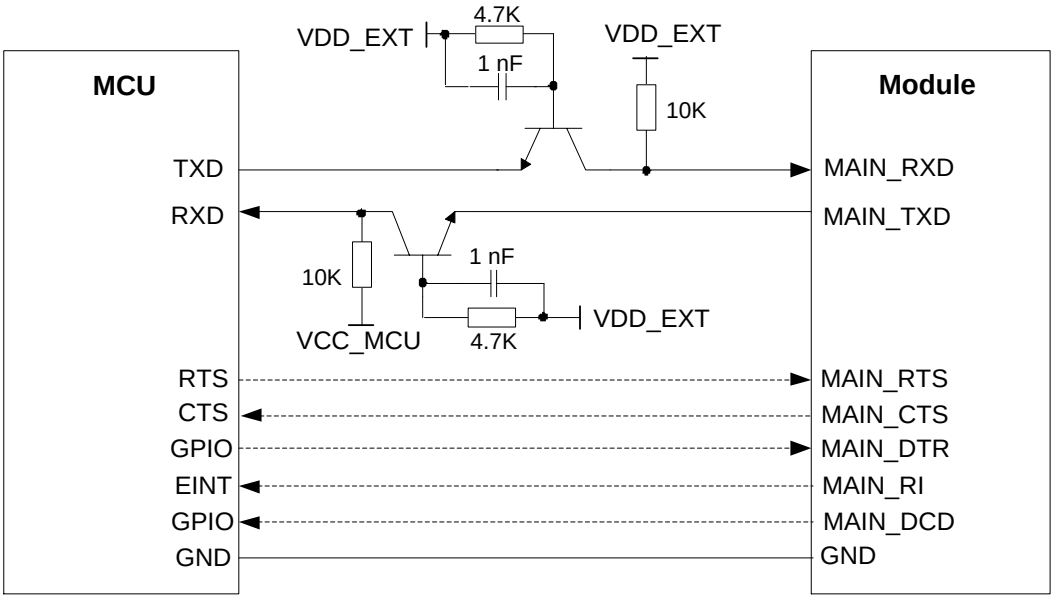



**Figure 24: Reference Design of UART with Transistor Level-shifting Circuit**

**NOTE**

1. Transistor level-shifting circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.

## 4.6. PCM and I2C Interfaces

The module provides one I2C interface and one Pulse Code Modulation (PCM) digital interface.

I2C interface complies with the I2C bus protocol specification (100/400 kHz). In applications related to the interface, the module can only be used as master device and does not support multi-host mode.

PCM interface supports short frame mode. In the applications related to the interface, the module can be used as both slave device* and master device.

In short frame mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and also supports 4069 kHz PCM_CLK at 16 kHz PCM_SYNC.

The module supports a 16-bit linear encoding format. The following figure shows the sequence diagram of short frame mode (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz).

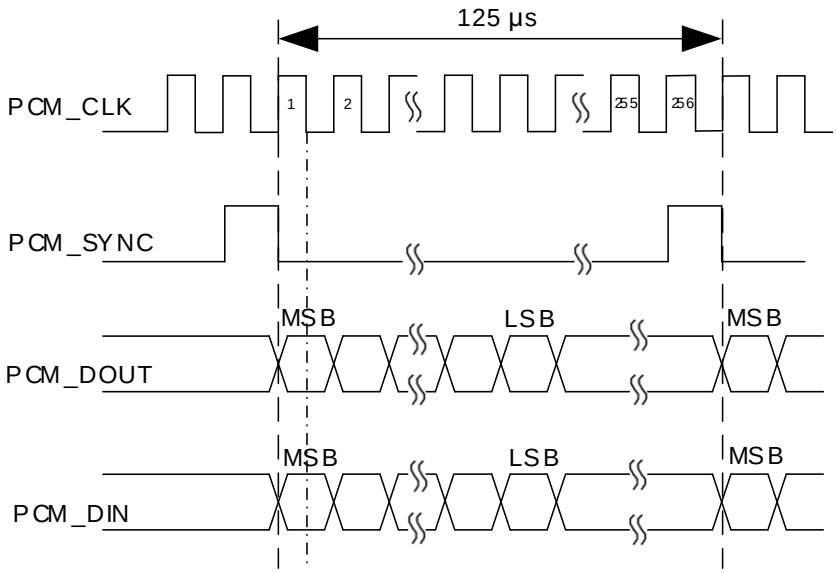



**Figure 25: Timing Sequence for Short Frame Mode**

**Table 17: Pin Definition of I2C Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| I2C_SCL | 40 | OD | I2C serial clock | An external 1.8 V pull-up resistor is needed.<br>If unused, keep them open. |
| I2C_SDA | 41 | OD | I2C serial data | |

**Table 18: Pin Definition of PCM Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| PCM_SYNC | 5 | DIO | PCM data frame sync | 1.8 V power domain.<br>When the module is used as the master device, the pins are in output state;<br>When the module is used as a slave device*, the pins are in input state.<br>If unused, keep them open. |
| PCM_CLK | 4 | DIO | PCM clock | |
| PCM_DIN | 6 | DI | PCM data input | If unused, keep them open. |
| PCM_DOUT | 7 | DO | PCM data output | |

The clock and mode of PCM can be configured by software, and the default configuration is short frame mode (PCM_CLK = 2048 kHz, PCM_SYNC = 8 kHz). For more details, see **AT+QDAI** in ***document [3]***.

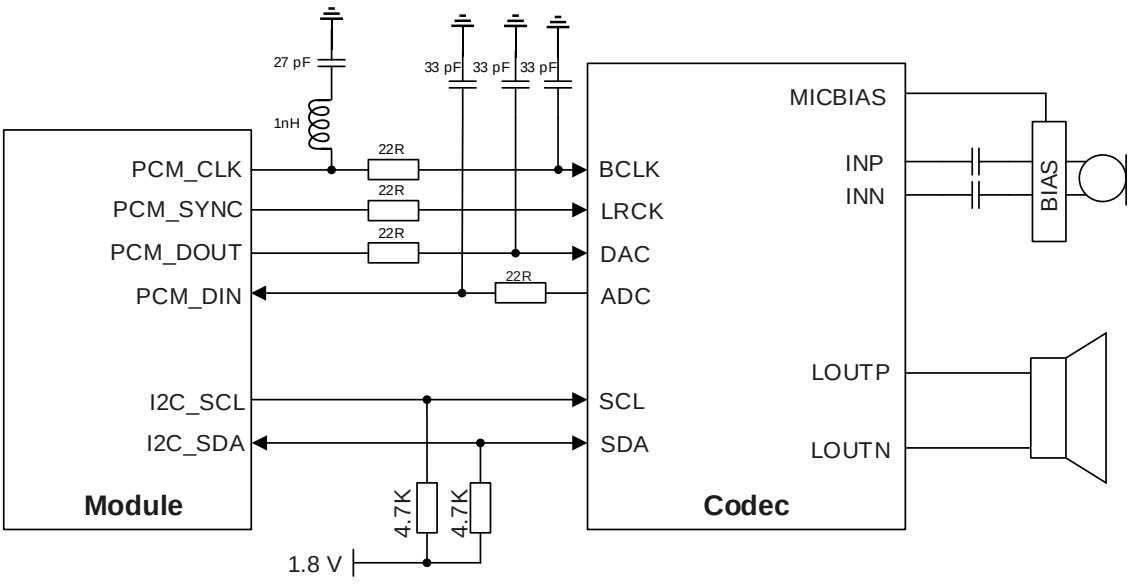



**Figure 26: Reference Design of PCM and I2C Interfaces**

**NOTE**

1. It is recommended to reserve the RC (R = 22 Ω, C = 33 pF) circuit on the PCM signal trace and the capacitor should be placed close to the module.
2. It is recommended to add a notch filter circuit near the module pin for PCM_CLK signal.

## 4.7. ADC Interface

The module provides two ADC interfaces. To improve the accuracy of ADC, the trace of ADC interface should be surrounded by ground.

**Table 19: Pin Definition of ADC Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| ADC0 | 24 | AI | General-purpose ADC interfaces | If unused, keep them open. |
| ADC1 | 2 | AI | | |

With **AT+QADC=<port>**, you can:

- **AT+QADC=0**: read the voltage value on ADC0
- **AT+QADC=1**: read the voltage value on ADC1

For more details about the AT command, see ***document [2]***.

**Table 20: Characteristics of ADC Interface**

| Parameters | Min. | Typ. | Max. | Units |
|---|---|---|---|---|
| ADC0 voltage range | 0 | - | VBAT_BB | V |
| ADC1 voltage range | 0 | - | VBAT_BB | V |
| ADC resolution | - | 12 | - | bits |

**NOTE**

1. The input voltage of every ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by

the VBAT.
3. If the ADC pin uses a voltage divider circuit input, the voltage divider resistance should not exceed 100 kΩ, otherwise the measurement accuracy of ADC would be significantly reduced.

## 4.8. SPI Interface

The module provides one SPI interface that supports master mode with a maximum clock frequency of 52 MHz.

**Table 21: Pin Definition of SPI Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| SPI_CLK | 26 | DO | SPI clock | Master mode only.<br>1.8 V power domain.<br>If unused, keep them open. |
| SPI_CS | 25 | DO | SPI chip select | |
| SPI_DIN | 27 | DI | SPI data input | |
| SPI_DOUT | 28 | DO | SPI data output | |

## 4.9. Control Signal

**Table 22: Pin Definition of Control Signal**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| W_DISABLE# | 18 | DI | Airplane mode control | 1.8 V power domain.<br>Pull-up by default.<br>In low voltage level, the module can enter airplane mode.<br>If unused, keep it open. |

### 4.9.1. W_DISABLE#

The module provides W_DISABLE# to enable or disable RF function. W_DISABLE# is pulled up by default. When W_DISABLE# is at high voltage level, you can send **AT+CFUN=<fun>** to set module's operating mode. Driving W_DISABLE# low will set the module into airplane mode.

**Table 23: W_DISABLE# AT Command Configuration Information**

| W_DISABLE# Level Status | AT Commands | RF Function Status | Module Operating Modes |
|---|---|---|---|
| High | **AT+CFUN=1** | Enabled | Full functionality mode |
| | **AT+CFUN=0** | Disabled | Minimum functionality mode |
| | **AT+CFUN=4** | Disabled | Airplane mode |
| Low | **AT+CFUN=0**<br>**AT+CFUN=1**<br>**AT+CFUN=4** | Disabled | Airplane mode |

**NOTE**

1. The execution of **AT+CFUN** does not affect GNSS function.
2. W_DISABLE# is a control function for airplane mode, which is disabled by default in software and can be enabled through **AT+QCFG="airplanecontrol",1**.

## 4.10. Indication Signal

**Table 24: Pin Definition of Indication Signal**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| STATUS | 20 | DO | Indicate the module's operation status | 1.8 V power domain.<br>If unused, keep them open. |
| NET_STATUS | 21 | DO | Indicate the module's network activity status | |
| SLEEP_IND | 1 | DO | Indicate the module's sleep mode | |

### 4.10.1. Network Status Indication

NET_STATUS pin can be used for indicating module’s the network activity status.

**Table 25: Network Status Indication Pin Level and Module Network Status**

| Pin Name | NET_STATUS Level Status | Module Network Status |
|---|---|---|
| NET_STATUS | Flicker slowly (200 ms high/1800 ms low) | Network searching |
| | Flicker slowly (1800 ms high/200 ms low) | Idle |
| | Flicker quickly (125 ms high/125 ms low) | Data transmission is ongoing |
| | Always high | Voice calling |

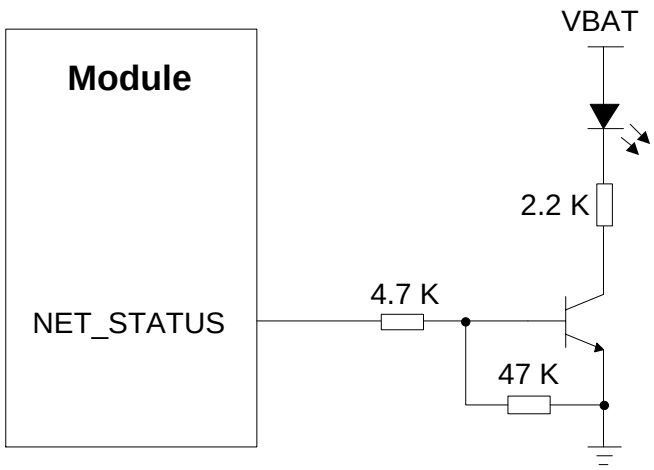



**Figure 27: Reference Design of Network Status Indication**

### 4.10.2. STATUS

The STATUS is used for indicating module's operation status. It will output high level when the module is turned on normally.

A reference circuit is shown as below:

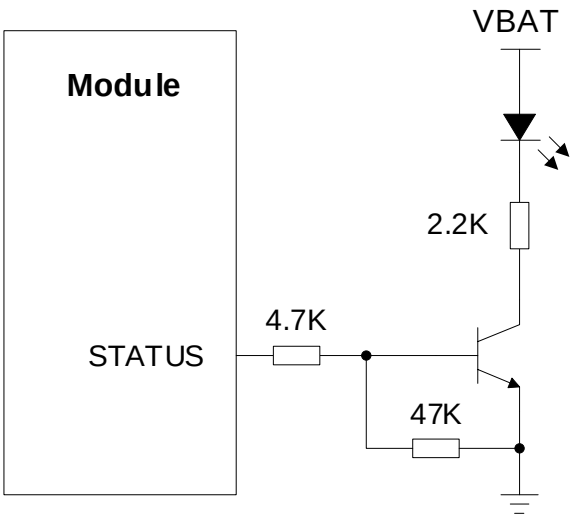



**Figure 28: Reference Design of STATUS**

**NOTE**

When the module is not powered by VBAT, STATUS cannot be used as a shutdown status indicator.

### 4.10.3. MAIN_RI

**AT+QCFG="risignaltype","physical"** can be used to configure the indication behavior for MAIN_RI. No matter on which port (main UART, USB AT port or USB modem port) a URC information is presented, the URC information will trigger the behavior of the MAIN_RI. For more details, see ***document [2]***.

**NOTE**

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The USB AT port is the URC output port by default. For more details, see ***document [2]***.

You can configure MAIN_RI behaviors flexibly. The default behaviors of the MAIN_RI is shown as below:

**Table 26: MAIN_RI Level and Module Status**

| Module Status | MAIN_RI Level Status |
|---|---|
| Idle | High |
| When a new URC returns | MAIN_RI outputs at least 120 ms low level. After the module outputs the data, the level status will then become high. |

Indication behavior for MAIN_RI can be configured via **AT+QCFG="urc/ri/ring"**. See ***document [2]*** for details.

# 5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

## 5.1. Cellular Network

### 5.1.1. RF Antenna Interface & Frequency Bands

**Table 27: Pin Description of RF Antenna Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| ANT_MAIN | 60 | AIO | Main antenna interface | 50 Ω characteristic impedance. |
| ANT_DRX | 56 | AI | Diversity antenna interface | |

**Table 28: Operating Frequency of EG950A-EL (Unit: MHz)**

| Operating Frequency | Transmit | Receive |
|---|---|---|
| WCDMA B1 | 1922–1978 | 2112–2168 |
| WCDMA B5 | 826–847 | 871–892 |
| WCDMA B8 | 882–913 | 927–958 |
| LTE-FDD B1 | 1920–1980 | 2110–2170 |
| LTE-FDD B3 | 1710–1785 | 1805–1880 |
| LTE-FDD B5 | 824–849 | 869–894 |
| LTE-FDD B7 | 2500–2570 | 2620–2690 |
| LTE-FDD B8 | 880–915 | 925–960 |

| | | |
|---|---|---|
| LTE-FDD B20 | 832–862 | 791–821 |
| LTE-FDD B28 | 703–748 | 758–803 |

**Table 29: Operating Frequency of EG950A-LA (Unit: MHz)**

| Operating Frequency | Transmit | Receive |
|---|---|---|
| WCDMA B1 | 1922–1978 | 2112–2168 |
| WCDMA B2 | 1852–1908 | 1932–1988 |
| WCDMA B4 | 1712–1753 | 2112–2153 |
| WCDMA B5 | 826–847 | 871–892 |
| WCDMA B8 | 882–913 | 927–958 |
| LTE-FDD B1 | 1920–1980 | 2110–2170 |
| LTE FDD B2 | 1850–1910 | 1930–1990 |
| LTE-FDD B3 | 1710–1785 | 1805–1880 |
| LTE FDD B4 | 1710–1755 | 2110–2155 |
| LTE-FDD B5 | 824–849 | 869–894 |
| LTE-FDD B7 | 2500–2570 | 2620–2690 |
| LTE-FDD B8 | 880–915 | 925–960 |
| LTE-FDD B28 | 703–748 | 758–803 |
| LTE-FDD B66 | 1710–1780 | 2110–2180 |

### 5.1.2. Tx Power

**Table 30: RF Output Power of EG950A-EL**

| Mode | Frequency Bands | Max. RF Output Power | Min. RF Output Power |
|---|---|---|---|
| WCDMA | B1/B5/B8 | 23 dBm ±2dB | < -49 dBm |
| LTE-FDD | B1/B3/B5/B7/B8/B20/B28 | 23 dBm ±2dB | < -39 dBm |

**Table 31: RF Output Power of EG950A-LA**

| Mode | Frequency Bands | Max. RF Output Power | Min. RF Output Power |
|---|---|---|---|
| WCDMA | B1/B2/B4/B5/B8 | 23 dBm ±2dB | < -49 dBm |
| LTE-FDD | B1/B2/B3/B4/B5/B7/B8/B28/B66 | 23 dBm ±2dB | < -39 dBm |

### 5.1.3. Rx Sensitivity

**Table 32: Conducted RF Receiver Sensitivity of EG950A-EL (Unit: dBm)**

| Frequency | Receiver Sensitivity (Typ.) | | | 3GPP (SIMO) |
|---|---|---|---|---|
| | Primary | Diversity | SIMO | |
| WCDMA B1 | -110.3 | - | - | -106.7 |
| WCDMA B5 | -111.5 | - | - | -104.7 |
| WCDMA B8 | -110.9 | - | - | -103.7 |
| LTE-FDD B1 | -98.3 | -98.8 | -101.3 | -96.3 |
| LTE-FDD B3 | -97.7 | -97.0 | -100.5 | -93.3 |
| LTE-FDD B5 | -98.9 | -99.6 | -102.6 | -94.3 |
| LTE-FDD B7 | -96.9 | -97.7 | -100.4 | -94.3 |
| LTE-FDD B8 | -98.9 | -99.3 | -101.8 | -93.3 |
| LTE-FDD B20 | -98.9 | -99.2 | -101.8 | -93.3 |
| LTE-FDD B28 | -98.9 | -97.9 | -101.5 | -94.8 |

**Table 33: Conducted RF Receiver Sensitivity of EG950A-LA (Unit: dBm)**

| Frequency | Receiver Sensitivity (Typ.) | | | 3GPP (SIMO) |
|---|---|---|---|---|
| | Primary | Diversity | SIMO | |
| WCDMA B1 | -109.5 | - | - | -106.7 dBm |
| WCDMA B2 | -108.8 | - | - | -104.7 dBm |
| WCDMA B4 | -109.5 | - | - | -106.7 dBm |

| | | | | |
|---|---|---|---|---|
| WCDMA B5 | -112.2 | - | - | -104.7 dBm |
| WCDMA B8 | -111.4 | - | - | -103.7 dBm |
| LTE-FDD B1 | -98.22 | -97.62 | -100.22 | -96.3 dBm |
| LTE FDD B2 | -97.52 | -96.32 | -99.62 | -94.3 dBm |
| LTE-FDD B3 | -97.42 | -96.32 | -100.12 | -93.3 dBm |
| LTE FDD B4 | -97.42 | -97.02 | -100.02 | -96.3 dBm |
| LTE-FDD B5 | -98.22 | -99.32 | -101.82 | -94.3 dBm |
| LTE-FDD B7 | -96.92 | -97.12 | -99.82 | -94.3 dBm |
| LTE-FDD B8 | -98.12 | -98.72 | -101.72 | -93.3 dBm |
| LTE-FDD B28 | -98.62 | -98.22 | -101.52 | -94.8 dBm |
| LTE-FDD B66 | -96.82 | -96.62 | -99.62 | -96.5 dBm |

### 5.1.4. Reference Design

The module provides two RF antenna interfaces for antenna connection. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (C1, R1, C2 and C3, R2, C4) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

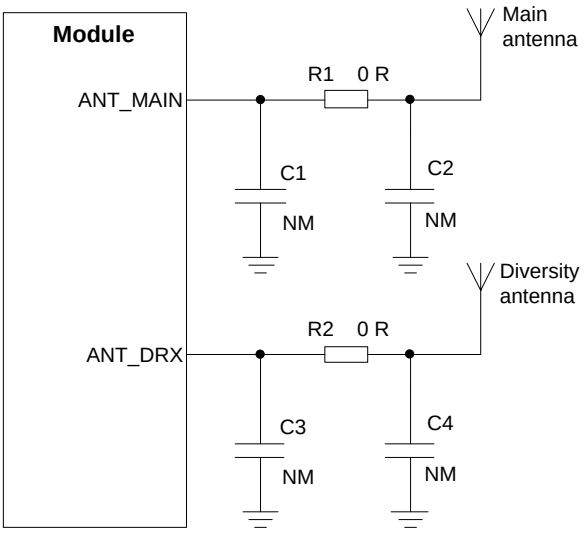



**Figure 29: Reference Design of Main Antenna and Diversity Antenna**

## 5.2. GNSS

GNSS information of the module is as follows:

- Supports GPS, GLONASS, BDS, QZSS positioning system.
- Supports NMEA 0183 protocol and outputs NMEA sentences via USB interface (data update rate for positioning: 1–5 Hz; 1 Hz by default).
- The module's GNSS function is OFF by default. It must be ON via **AT+QGPS**. For more details, see ***document [4]***.

### 5.2.1. Antenna Interface & Frequency Bands

**Table 34: Pin Definition of GNSS Antenna Interface**

| Pin Name | Pin No. | I/O | Description | Comment |
|---|---|---|---|---|
| ANT_GNSS | 49 | AI | GNSS antenna interface | 50 Ω characteristic impedance.<br>If unused, keep it open. |

**Table 35: GNSS Frequency (Unit: MHz)**

| Antenna Types | Frequency |
|---|---|
| GPS | 1575.42 ±1.023 (L1) |
| GLONASS | 1597.5–1605.8 (L1) |
| BDS | 1561.098 ±2.046 (B1I) |
| QZSS | 1575.42 ±1.023 (L1) |

**NOTE**

1. GNSS function is only supported by EG950A-EL module, and the function is optional. Only the module with built-in GNSS function has GNSS antenna interface.
2. An external LDO can be selected to supply power according to the active antenna requirements. If the module is designed with an active antenna, then VDD circuit is needed.

### 5.2.2. GNSS Performance

**Table 36: GNSS Performance**

| Parameters | Modes | Conditions | Typ. | Units |
|---|---|---|---|---|
| Sensitivity | Acquisition | Autonomous | -144 | dBm |
| | Reacquisition | | -157 | |
| | Tracking | | -161 | |
| TTFF | Cold start @ open sky | Autonomous | 35.47 | s |
| | Warm start @ open sky | | 31.53 | |
| | Hot start @ open sky | | 0.15 | |
| Accuracy | CEP-50 | Autonomous @ open sky | 1.69 | m |

**NOTE**

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

## 5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

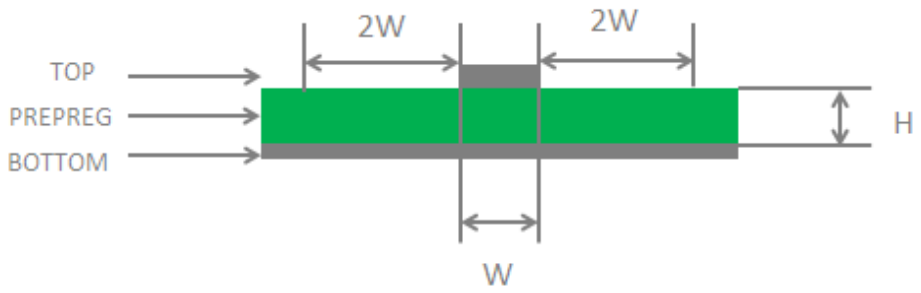



**Figure 30: Microstrip Design on a 2-layer PCB**

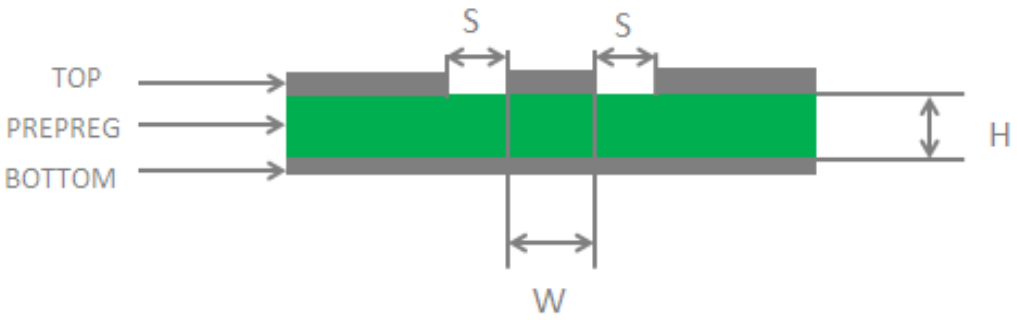



**Figure 31: Coplanar Waveguide Design on a 2-layer PCB**

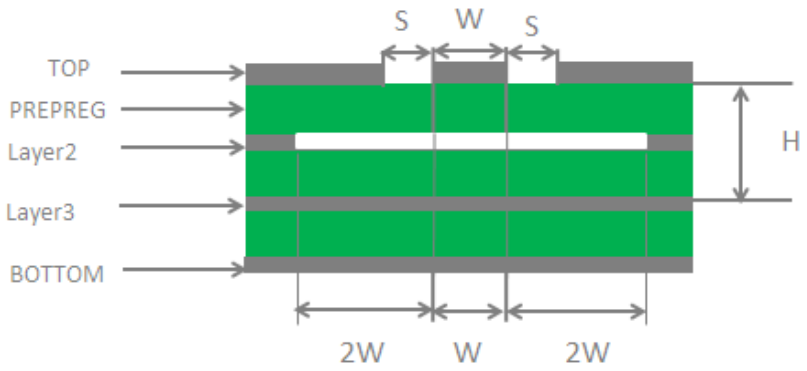



**Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)**

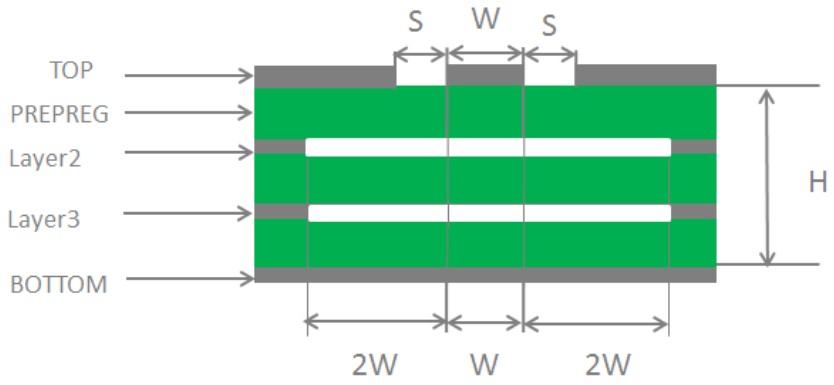



**Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)**

To ensure better RF performance and reliability, the following conditions should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between any traces on adjacent layers.

For more details about RF layout, see ***document [5]***.

## 5.4. Requirements for Antenna Design

**Table 37: Requirements for Antenna Design**

| Antenna Types | Requirements |
|---|---|
| GNSS | • **Frequency range:** L1 (1559–1609 MHz)<br>• RHCP or linear polarization<br>• VSWR: ≤ 2 |
| | • **For passive antenna application:**<br>Passive antenna gain: > 0 dBi |

| | |
|---|---|
| | ● **For active antenna application:**<br>Active antenna noise coefficient: < 1.5 dB<br>Active antenna gain: > 0 dBi<br>Active antenna embedded LNA gain: < 17 dB |
| UMTS/LTE [4] | ● VSWR: ≤ 2<br>● Efficiency: > 30 %<br>● Gain:<br>WCDMA Band 2,LTE Band 2: 1.590 dBi<br>WCDMA Band 4,LTE Band 4/66: 2.000 dBi<br>WCDMA Band 5,LTE Band 5: 2.530dBi<br>LTE Band 7: 3.000dBi<br>● Max input power: 50 W<br>● Input impedance: 50 Ω<br>● Vertical polarization<br>● **Cable insertion loss:**<br>**< 1 dB:** LB (< 1 GHz)<br>**< 1.5 dB:** MB (1–2.3 GHz)<br>**< 2 dB:** HB (> 2.3 GHz) |

## 5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

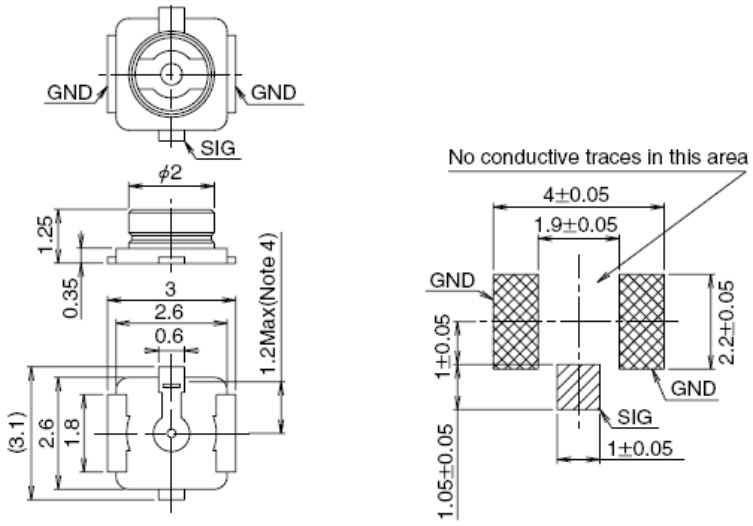



**Figure 34: Dimensions of the Receptacle (Unit: mm)**

[4] The performance parameters are recommended by Quectel and you are advised to confirm these parameters with antenna suppliers and adjust them according to the actual products, test results and certification requirements to ensure the overall wireless performance for your terminals.

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

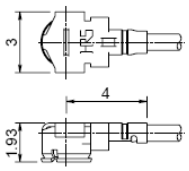
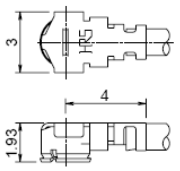
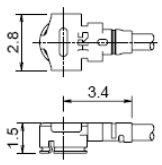
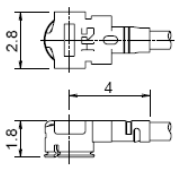
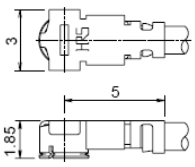
| Part No. | U.FL-LP-040 | U.FL-LP-066 | U.FL-LP(V)-040 | U.FL-LP-062 | U.FL-LP-088 |
|---|---|---|---|---|---|
| |  |  |  |  |  |
| Mated Height | 2.5mm Max. (2.4mm Nom.) | 2.5mm Max. (2.4mm Nom.) | 2.0mm Max. (1.9mm Nom.) | 2.4mm Max. (2.3mm Nom.) | 2.4mm Max. (2.3mm Nom.) |
| Applicable cable | Dia. 0.81mm Coaxial cable | Dia. 1.13mm and Dia. 1.32mm Coaxial cable | Dia. 0.81mm Coaxial cable | Dia. 1mm Coaxial cable | Dia. 1.37mm Coaxial cable |
| Weight (mg) | 53.7 | 59.1 | 34.8 | 45.5 | 71.7 |
| RoHS | YES | | | | |

**Figure 35: Specifications of Mated Plugs (Unit: mm)**

The following figure describes the space factor of the mated connector.

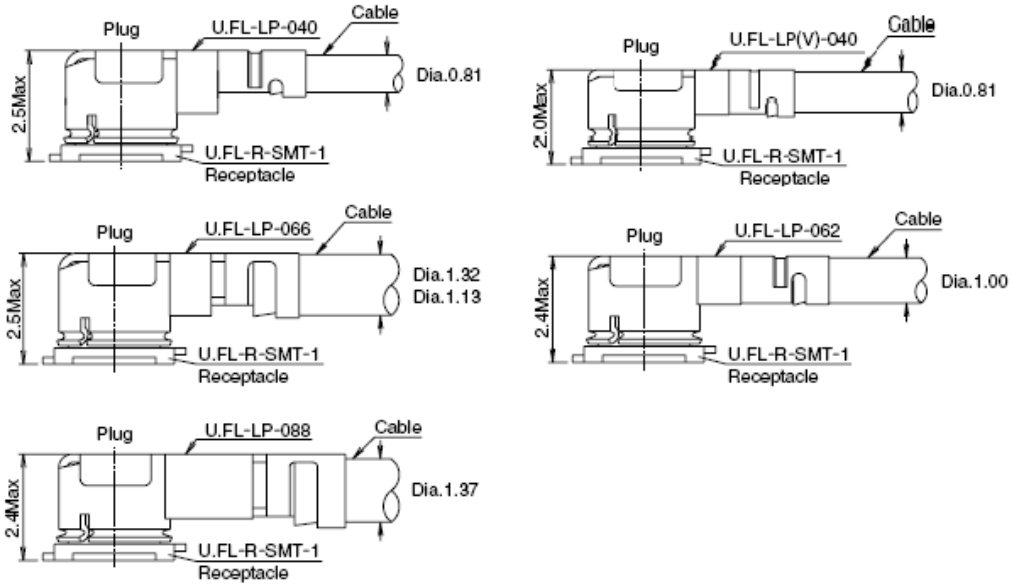



**Figure 36: Space Factor of the Mated Connectors (Unit: mm)**

For more details, visit http://www.hirose.com.

# 6 Electrical Characteristics & Reliability

## 6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

**Table 38: Absolute Maximum Ratings**

| Parameters | Min. | Max. | Units |
|---|---|---|---|
| Voltage at VBAT_RF & VBAT_BB | -0.3 | 5.5 | V |
| Voltage at USB_VBUS | -0.3 | 5.5 | V |
| Voltage at digital pins | -0.3 | 2.3 | V |
| Voltage at ADC0 | 0 | VBAT_BB | V |
| Voltage at ADC1 | 0 | VBAT_BB | V |
| Current at VBAT_BB | - | 2.0 | A |
| Current at VBAT_RF | - | 0.5 | A |

## 6.2. Power Supply Ratings

**Table 39: Module's Power Supply Ratings**

| Parameters | Descriptions | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| VBAT | VBAT_BB & VBAT_RF | The actual input voltage must be within this range | 3.4 | 3.8 | 4.5 | V |
| USB_VBUS | USB connection detection | | 3.0 | 5.0 | 5.25 | V |

## 6.3. Power Consumption

**Table 40: EG950A-EL Current Consumption**

| Description | Conditions | Typ. | Unit |
|---|---|---|---|
| Power-off | Power down | 9.65 | μA |
| Sleep State | **AT+CFUN=0** (USB disconnected) | 1.13 | mA |
| | WCDMA @ PF = 64 (USB disconnected) | 2.95 | |
| | WCDMA @ PF = 64 (USB suspended) | 3.22 | |
| | WCDMA @ PF = 128 (USB disconnected) | 2.42 | |
| | WCDMA @ PF = 256 (USB disconnected) | 2.11 | |
| | WCDMA @ PF = 512 (USB disconnected) | 1.92 | |
| | LTE-FDD @ PF = 32 (USB disconnected) | 2.83 | |
| | LTE-FDD @ PF = 64 (USB disconnected) | 2.10 | |
| | LTE-FDD @ PF = 64 (USB suspended) | 2.40 | |
| | LTE-FDD @ PF = 128 (USB disconnected) | 1.82 | |
| | LTE-FDD @ PF = 256 (USB disconnected) | 1.74 | |
| Idle State | WCDMA @ PF = 64 (USB disconnected) | 19.07 | mA |
| | WCDMA @ PF = 64 (USB connected) | 33.33 | |
| | LTE-FDD @ PF = 64 (USB disconnected) | 18.80 | |
| | LTE-FDD @ PF = 64 (USB connected) | 33.35 | |
| WCDMA Voice Communication（GNSS OFF） | WCDMA B1 @ 23.04 dBm | 577.00 | mA |
| | WCDMA B5 @ 22.59 dBm | 587.00 | |
| | WCDMA B8 @ 22.74 dBm | 564.00 | |
| WCDMA Data Transfer (GNSS OFF) | WCDMA B1 HSDPA @ 22.34 dBm | 550.00 | mA |
| | WCDMA B5 HSDPA @ 21.75 dBm | 562.00 | |

| | | | |
|---|---|---|---|
| | WCDMA B8 HSDPA @ 21.95 dBm | 547.00 | |
| | WCDMA B1 HSUPA @ 22.16 dBm | 511.00 | |
| | WCDMA B5 HSUPA @ 21.24 dBm | 544.00 | |
| | WCDMA B8 HSUPA @ 21.59 dBm | 543.00 | |
| LTE Data Transfer (GNSS OFF) | LTE-FDD B1 @ 23.92 dBm | 631.00 | mA |
| | LTE-FDD B3 @ 23.36 dBm | 655.00 | |
| | LTE-FDD B5 @ 22.89 dBm | 627.00 | |
| | LTE-FDD B7 @ 23.81 dBm | 825.00 | |
| | LTE-FDD B8 @ 23.49 dBm | 633.00 | |
| | LTE-FDD B20 @ 23.75 dBm | 573.00 | |
| | LTE-FDD B28 @ 23.28 dBm | 656.00 | |

**Table 41: EG950A-LA Current Consumption**

| Description | Conditions | Typ. | Unit |
|---|---|---|---|
| Power-off | Power down | 9.53 | μA |
| Sleep State | **AT+CFUN=0** (USB disconnected) | 1.12 | mA |
| | WCDMA @ PF = 64 (USB disconnected) | 3.11 | |
| | WCDMA @ PF = 64 (USB suspended) | 3.40 | |
| | WCDMA @ PF = 128 (USB disconnected) | 2.45 | |
| | WCDMA @ PF = 256 (USB disconnected) | 2.17 | |
| | WCDMA @ PF = 512 (USB disconnected) | 1.92 | |
| | LTE-FDD @ PF = 32 (USB disconnected) | 3.22 | |
| | LTE-FDD @ PF = 64 (USB disconnected) | 2.37 | |
| | LTE-FDD @ PF = 64 (USB suspended) | 2.63 | |
| | LTE-FDD @ PF = 128 (USB disconnected) | 2.14 | |

| | | | |
|---|---|---|---|
| | LTE-FDD @ PF = 256 (USB disconnected) | 1.90 | |
| Idle State | WCDMA @ PF = 64 (USB disconnected) | 18.89 | mA |
| | WCDMA @ PF = 64 (USB connected) | 33.65 | |
| | LTE-FDD @ PF = 64 (USB disconnected) | 18.45 | |
| | LTE-FDD @ PF = 64 (USB connected) | 33.22 | |
| WCDMA Voice Communication | WCDMA B1 @ 23.03 dBm | 617.00 | mA |
| | WCDMA B2 @ 23.10 dBm | 577.00 | |
| | WCDMA B4 @ 22.75 dBm | 495.00 | |
| | WCDMA B5 @ 22.68 dBm | 591.00 | |
| | WCDMA B8 @ 22.92 dBm | 592.00 | |
| WCDMA Data Transfer | WCDMA B1 HSDPA @ 22.33 dBm | 602.00 | mA |
| | WCDMA B2 HSDPA @ 22.53 dBm | 554.00 | |
| | WCDMA B4 HSDPA @ 22.01 dBm | 494.00 | |
| | WCDMA B5 HSDPA @ 22.01 dBm | 587.00 | |
| | WCDMA B8 HSDPA @ 22.18 dBm | 588.00 | |
| | WCDMA B1 HSUPA @ 21.67 dBm | 563.00 | |
| | WCDMA B2 HSUPA @ 21.73 dBm | 523.00 | |
| | WCDMA B4 HSUPA @ 20.98 dBm | 458.00 | |
| | WCDMA B5 HSUPA @ 21.20 dBm | 545.00 | |
| | WCDMA B8 HSUPA @ 20.61 dBm | 539.00 | |
| LTE Data Transfer | LTE-FDD B1 @ 23.69 dBm | 617.00 | mA |
| | LTE-FDD B2 @ 23.03 dBm | 550.00 | |
| | LTE-FDD B3 @ 23.82 dBm | 667.00 | |
| | LTE-FDD B4 @ 23.60 dBm | 560.00 | |
| | LTE-FDD B5 @ 23.82 dBm | 646.00 | |

| | | |
|---|---|---|
| | LTE-FDD B7 @ 23.02 dBm | 753.00 |
| | LTE-FDD B8 @ 23.84 dBm | 635.00 |
| | LTE-FDD B28 @ 23.60 dBm | 650.00 |
| | LTE-FDD B66 @ 23.83 dBm | 578.00 |

## 6.4. Digital I/O Characteristics

**Table 42: 1.8 V I/O Characteristics (Unit: V)**

| Parameters | Descriptions | Min. | Max. |
|---|---|---|---|
| VDD_EXT | I/O power supply | 1.67 | 1.93 |
| $V_{IH}$ | High-level input voltage | 0.7 × VDD_EXT | VDD_EXT + 0.2 |
| $V_{IL}$ | Low-level input voltage | -0.3 | 0.3 × VDD_EXT |
| $V_{OH}$ | High-level output voltage | VDD_EXT - 0.2 | VDD_EXT |
| $V_{OL}$ | Low-level output voltage | 0 | 0.2 |

**Table 43: SDIO Interface Low-voltage I/O Characteristics (Unit: V)**

| Parameters | Descriptions | Min. | Max. |
|---|---|---|---|
| SDIO_VDD | Power supply | 1.67 | 1.93 |
| $V_{IH}$ | High-level input voltage | 0.7 × SDIO_VDD | SDIO_VDD + 0.2 |
| $V_{IL}$ | Low-level input voltage | -0.3 | 0.3 × SDIO_VDD |
| $V_{OH}$ | High-level output voltage | SDIO_VDD - 0.2 | SDIO_VDD |
| $V_{OL}$ | Low-level output voltage | 0 | 0.2 |

**Table 44: SDIO Interface High-voltage I/O Characteristics (Unit: V)**

| Parameters | Descriptions | Min. | Max. |
|---|---|---|---|
| SDIO_VDD | Power supply | 2.7 | 3.05 |
| $V_{IH}$ | High-level input voltage | 2.0 | SDIO_VDD + 0.3 |
| $V_{IL}$ | Low-level input voltage | -0.3 | 0.8 |
| $V_{OH}$ | High-level output voltage | 2.4 | SDIO_VDD |
| $V_{OL}$ | Low-level output voltage | 0 | 0.4 |

**Table 45: (U)SIM Interface Low-voltage I/O Characteristics (Unit: V)**

| Parameters | Descriptions | Min. | Max. |
|---|---|---|---|
| USIM_VDD | Power supply | 1.67 | 1.93 |
| $V_{IH}$ | High-level input voltage | 0.8 × USIM_VDD | USIM_VDD |
| $V_{IL}$ | Low-level input voltage | -0.3 | 0.12 × USIM_VDD |
| $V_{OH}$ | High-level output voltage | 0.7 × USIM_VDD | USIM_VDD |
| $V_{OL}$ | Low-level output voltage | 0 | 0.15 × USIM_VDD |

**Table 46: (U)SIM Interface High-voltage I/O Characteristics (Unit: V)**

| Parameters | Descriptions | Min. | Max. |
|---|---|---|---|
| USIM_VDD | Power supply | 2.7 | 3.3 |
| $V_{IH}$ | High-level input voltage | 0.8 × USIM_VDD | USIM_VDD |
| $V_{IL}$ | Low-level input voltage | -0.3 | 0.12 × USIM_VDD |
| $V_{OH}$ | High-level output voltage | 0.7 × USIM_VDD | USIM_VDD |
| $V_{OL}$ | Low-level output voltage | 0 | 0.15 × USIM_VDD |

## 6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

**Table 47: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %; Unit: kV)**

| Tested Interfaces | Contact Discharge | Air Discharge |
|---|---|---|
| VBAT, GND | ±5 | ±10 |
| All Antenna Interfaces | ±5 | ±10 |
| Other Interfaces | ±0.5 | ±1 |

## 6.6. Operating and Storage Temperatures

**Table 48: Operating and Storage Temperatures (Unit: °C)**

| Parameter | Min. | Typ. | Max. |
|---|---|---|---|
| Operating Temperature Range [5] | -35 | +25 | +75 |
| Extended Operation Range [6] | -40 | - | +85 |
| Storage Temperature Range | -40 | - | +90 |

[5] Within this range, the module meets 3GPP specifications.
[6] Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as $P_{out}$, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

# 7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

## 7.1. Mechanical Dimensions

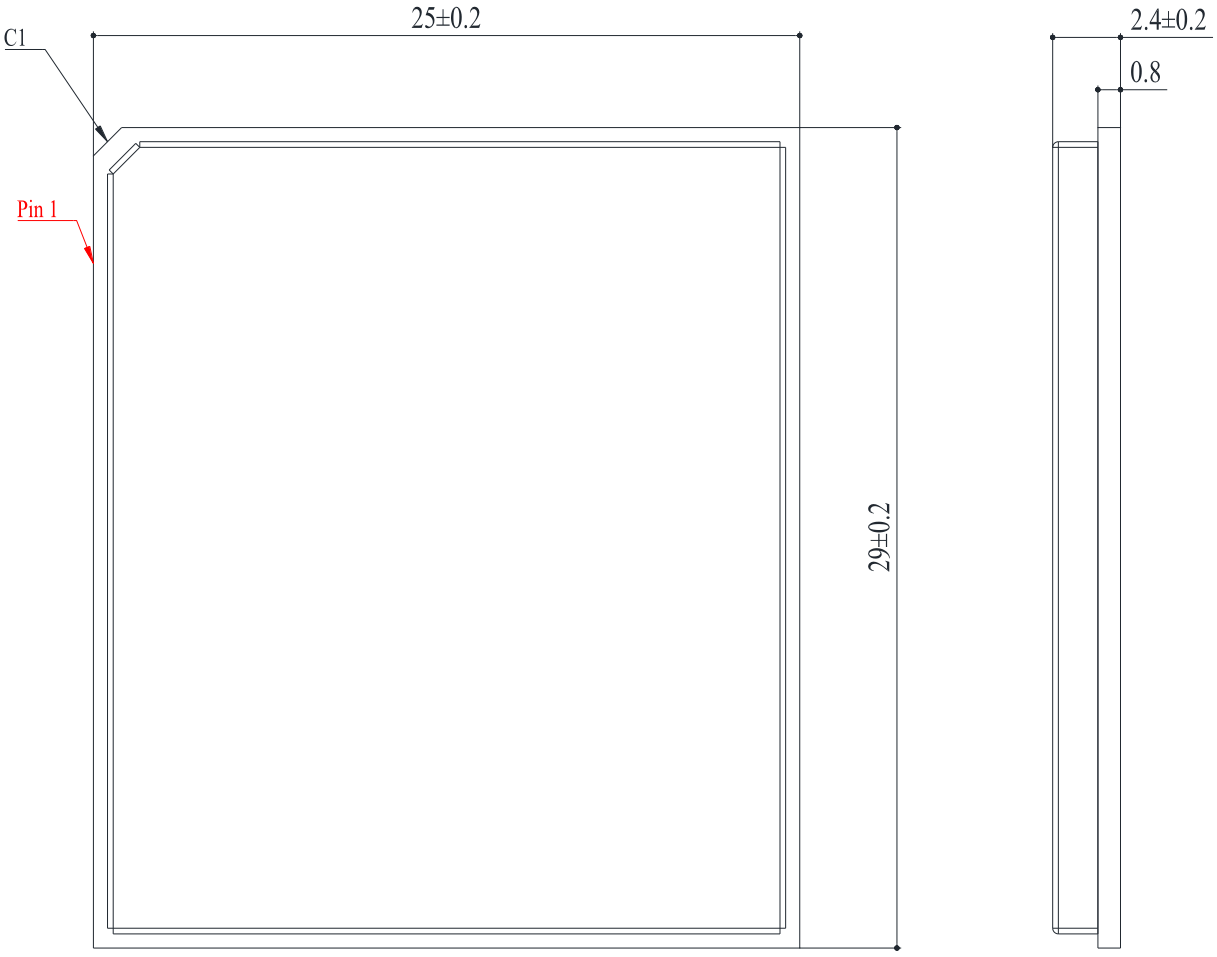



**Figure 37: Top and Side Dimensions**

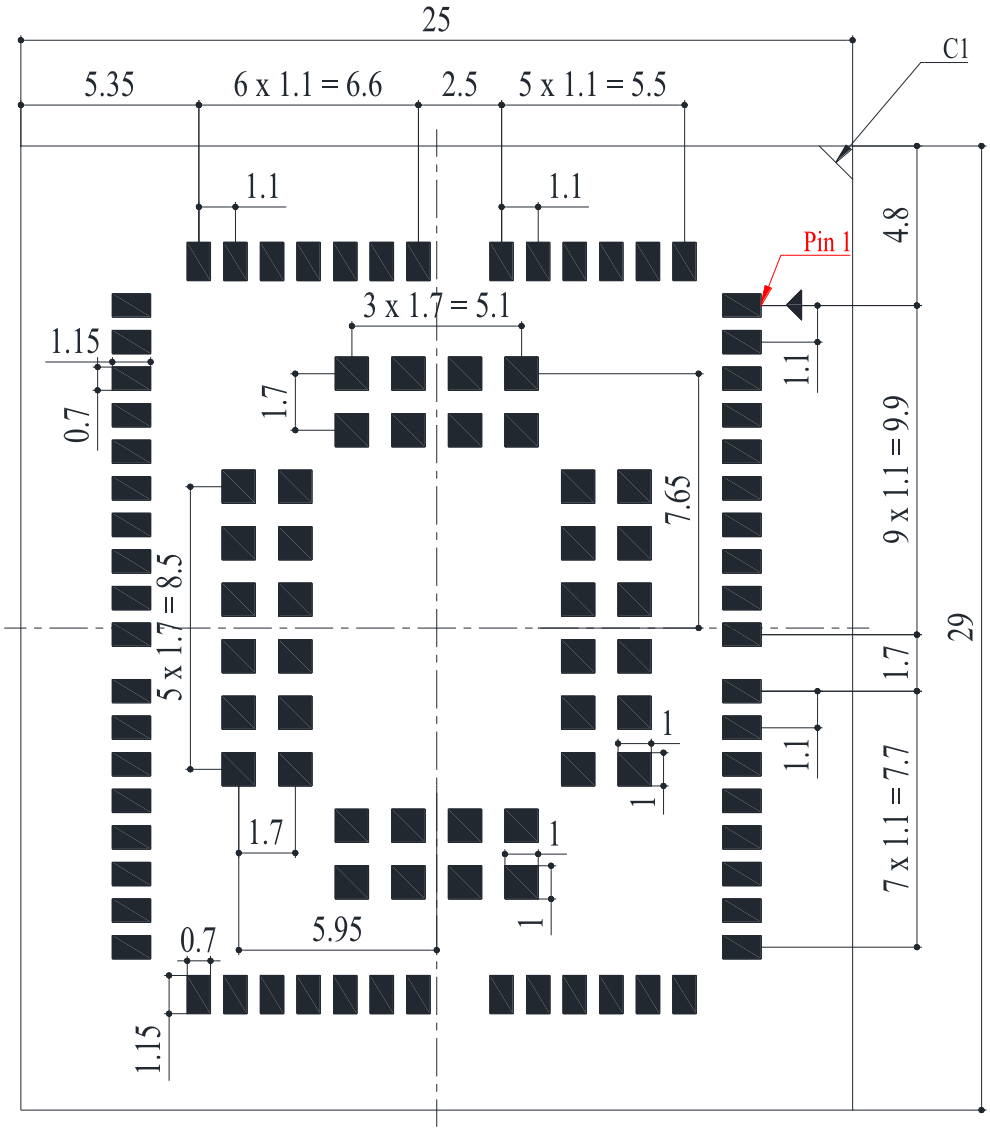



**Figure 38: Bottom Dimensions**

**NOTE**

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

## 7.2. Recommended Footprint

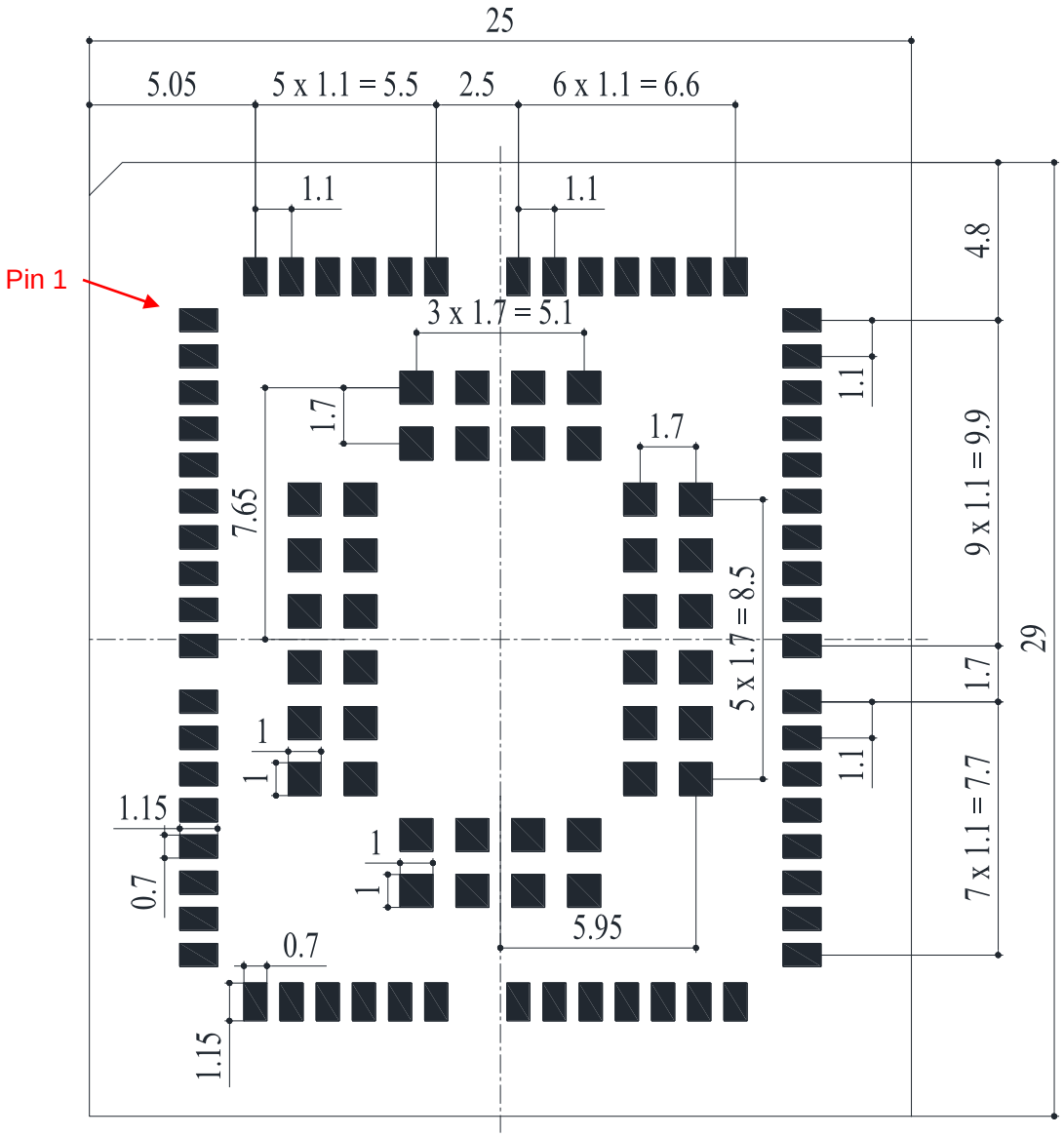



**Figure 39: Recommended Footprint (Top View)**

**NOTE**

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

## 7.3. Top and Bottom Views

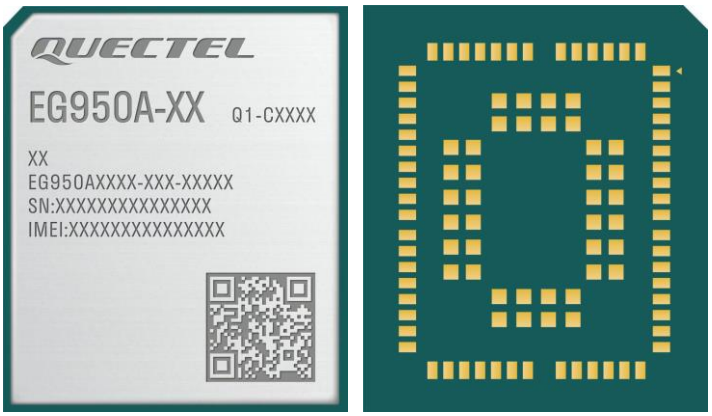



**Figure 40: Top & Bottom Views of the Module**

**NOTE**

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

# 8 Storage, Manufacturing & Packaging

## 8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended storage condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in recommended storage condition.

3. Floor life: 168 hours [7] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in recommended storage condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

**NOTE**

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

## 8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [6]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

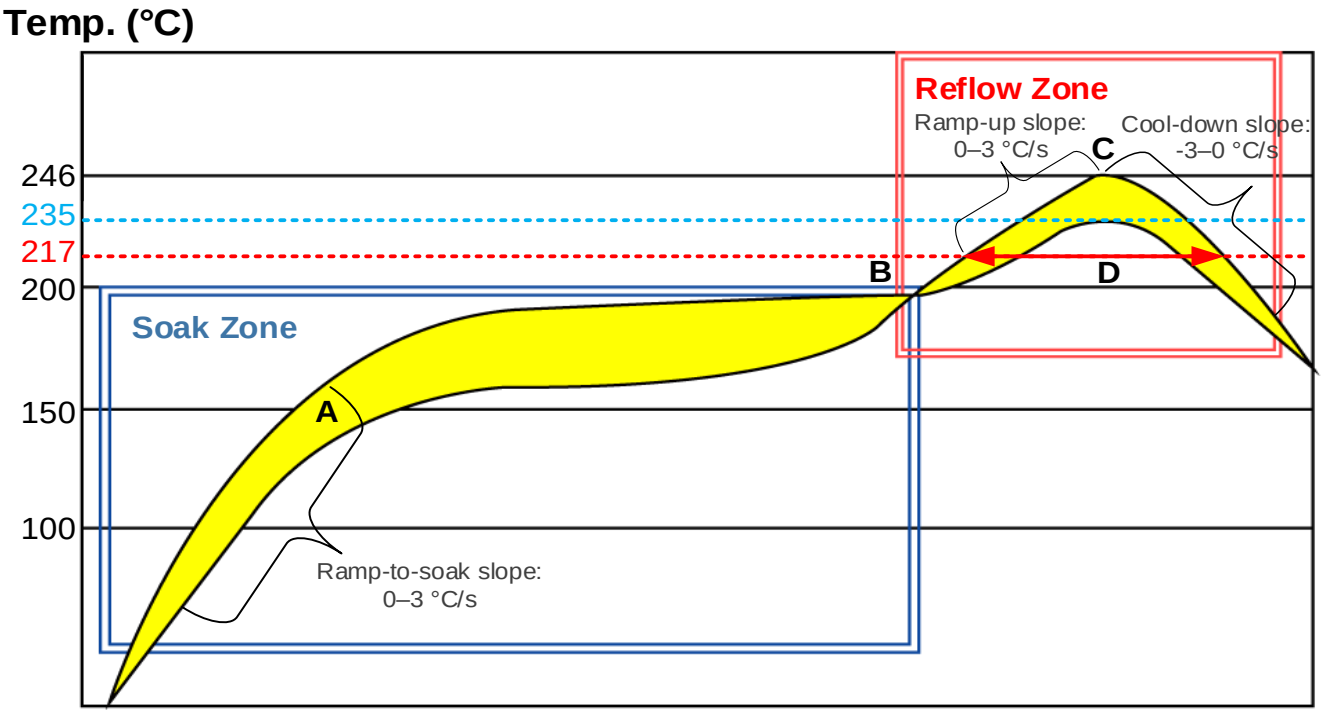



**Figure 41: Recommended Reflow Soldering Thermal Profile**

**Table 49: Recommended Thermal Profile Parameters**

| Factor | Recommended Value |
|---|---|
| **Soak Zone** | |
| Ramp-to-soak slope | 0–3 °C/s |
| Soak time (between A and B: 150 °C and 200 °C) | 70–120 s |
| **Reflow Zone** | |
| Ramp-up slope | 0–3 °C/s |
| Reflow time (D: over 217°C) | 40–70 s |
| Max temperature | 235–246 °C |
| Cool-down slope | -3–0 °C/s |
| **Reflow Cycle** | |
| Max reflow cycle | 1 |

**NOTE**

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, never wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

## 8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

### 8.3.1. Carrier Tape

Dimension details are as follow:

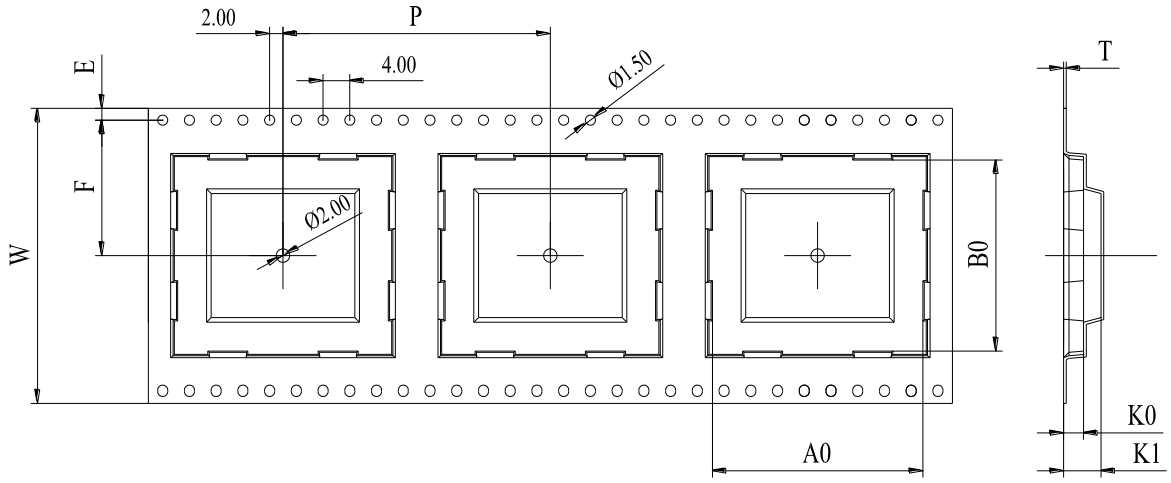



**Figure 42: Carrier Tape Dimension Drawing**

**Table 50: Carrier Tape Dimension Table (Unit: mm)**

| W | P | T | A0 | B0 | K0 | K1 | F | E |
|---|---|---|---|---|---|---|---|---|
| 44 | 32 | 0.35 | 25.5 | 29.5 | 3.2 | 5.8 | 20.2 | 1.75 |

### 8.3.2. Plastic Reel

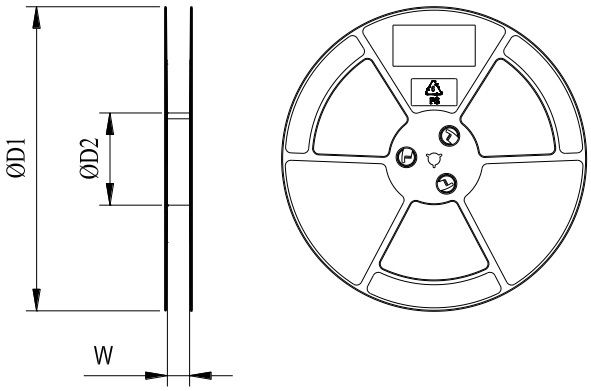



**Figure 43: Plastic Reel Dimension Drawing**

**Table 51: Plastic Reel Dimension Table (Unit: mm)**

| øD1 | øD2 | W |
|---|---|---|
| 330 | 100 | 44.5 |

### 8.3.3. Mounting Direction

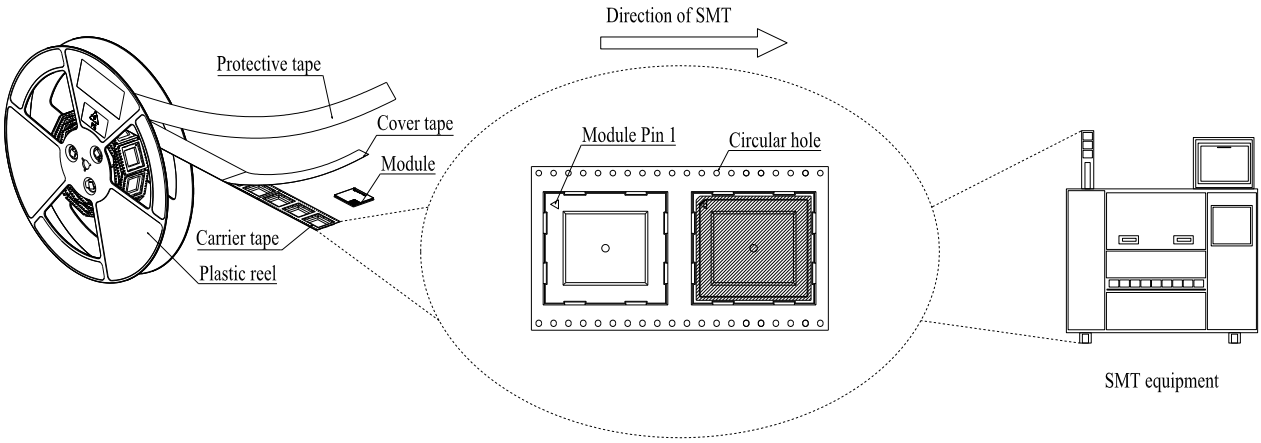
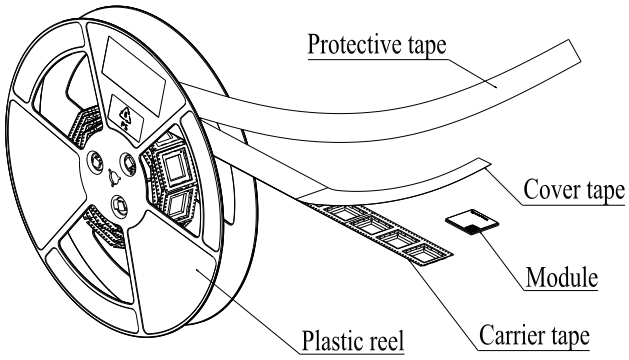


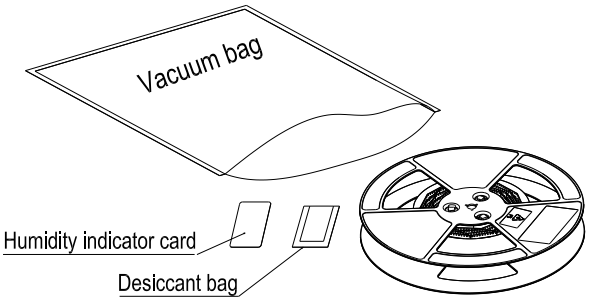

**Figure 44: Mounting Direction**

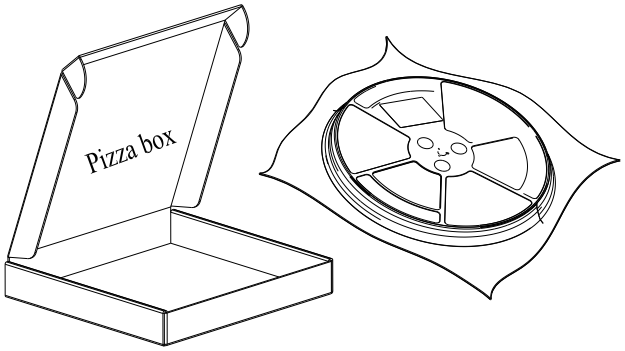
### 8.3.4. Packaging Process




Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.




Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

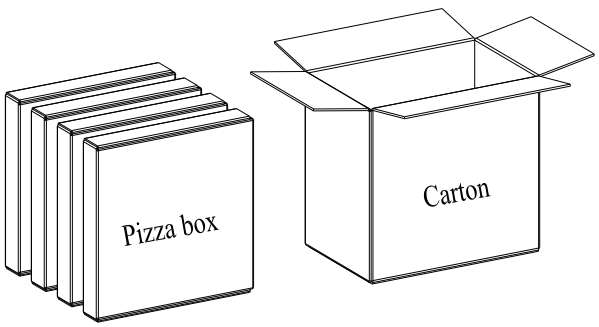



**Figure 45: Packaging Process**

# 9 Appendix References

**Table 52: Related Documents**

| Document Name |
|---|
| [1] Quectel_UMTS&LTE_EVB_User_Guide |
| [2] Quectel_LTE_Standard(A)_Series_AT_Commands_Manual |
| [3] Quectel_EC200x&EG912Y&EG91xN&EG950A_Series_Audio_Application_Note |
| [4] Quectel_EG915N&EG950A_Series_GNSS_Application_Note |
| [5] Quectel_RF_Layout_Application_Note |
| [6] Quectel_Module_SMT_Application_Note |

**Table 53: Terms and Abbreviations**

| Abbreviation | Description |
|---|---|
| AMR | Adaptive Multi-Rate |
| bps | Bytes per second |
| CHAP | Challenge Handshake Authentication Protocol |
| CS | Coding Scheme |
| CTS | Clear To Send |
| DRX | Discontinuous Reception |
| EFR | Enhanced Full Rate |
| ESD | Electrostatic Discharge |
| EVB | Evaluation Board |
| FDD | Frequency Division Duplexing |

| | |
|---|---|
| FR | Full Rate |
| FTP | File Transfer Protocol |
| FTPS | FTP over SSL |
| GLONASS | Global Navigation Satellite System (Russia) |
| GND | Ground |
| GNSS | Global Navigation Satellite System |
| GPS | Global Positioning System |
| HR | Half Rate |
| HSDPA | High Speed Downlink Packet Access |
| HTTP | Hypertext Transfer Protocol |
| HTTPS | Hypertext Transfer Protocol Secure |
| LGA | Land Grid Array |
| LTE | Long Term Evolution |
| MCU | Microcontroller Unit/Microprogrammed Control Unit |
| MMS | Multimedia Messaging Service |
| MO | Mobile Origination |
| MSB | Most Significant Bit |
| NMEA | National Marine Electronics Association |
| NTP | Network Time Protocol |
| PAP | Password Authentication Protocol |
| PCB | Printed Circuit Board |
| PCM | Pulse Code Modulation |
| PDU | Protocol Data Unit |
| PING | Packet Internet Groper |
| PPP | Point-to-Point Protocol |

| | |
|---|---|
| QAM | Quadrature Amplitude Modulation |
| QPSK | Quadrature Phase Shift Keying |
| QZSS | Quasi-Zenith Satellite System |
| RF | Radio Frequency |
| RoHS | Restriction of Hazardous Substances |
| RTS | Request To Send |
| SDIO | Secure Digital Input/Output Card |
| SMS | Short Message Service |
| SMTP | Simple Mail Transfer Protocol |
| SMTPS | Simple Mail Transfer Protocol Secure |
| SPI | Serial Peripheral Interface |
| SSL | Secure Sockets Layer |
| TCP | Transmission Control Protocol |
| TDD | Time Division Duplexing |
| UART | Universal Asynchronous Receiver/Transmitter |
| UDP | User Datagram Protocol |
| UMTS | Universal Mobile Telecommunications System |
| URC | Unsolicited Result Code |
| USB | Universal Serial Bus |
| (U)SIM | (Universal) Subscriber Identity Module |
| Vmax | Maximum Voltage |
| Vnom | Nominal Voltage |
| Vmin | Minimum Voltage |
| $V_{IL}$max | Maximum Low-level Input Voltage |
| VSWR | Voltage Standing Wave Ratio |

| | |
|---|---|
| WCDMA | Wideband Code Division Multiple Access |
| WLAN | Wireless Local Area Network |

FCC Certification Requirements.

According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.

And the following conditions must be met:

1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based time-averaging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.

2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.

3.A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2023EG950ALA.

4.To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

- ❒ WCDMA Band 2,LTE Band 2:≤1.590 dBi
- ❒ WCDMA Band 4,LTE Band 4/66:≤2.000 dBi
- ❒ WCDMA Band 5,LTE Band 5:≤2.530dBi
- ❒ LTE Band 7:≤3.000dBi

5. This module must not transmit simultaneously with any other antenna or transmitter

6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module:"Contains Transmitter Module FCC ID: XMR2023EG950ALA." or "Contains FCC ID: XMR2023EG950ALA." must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.