EG912U-GL Hardware Design

LTE Standard Module

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-08-04	Anla HUANGA	Creation of the document
1.0.0	2022-08-04	Anla HUANG/Nathan LIU	Preliminary

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1 Introduction

This document defines the EG912U-GL module and describes its air interfaces and hardware interfaces which relate to customers' applications.

It can help customers quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, customers can use this module to design and to set up mobile applications easily.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

The EG912U-GL is a wireless communication module, which supports LTE-FDD, LTE-TDD, GSM/GPRS network data connection. It provides voice function for your special applications and also supports GNSS. Related information and details are listed in the table below:

Table 2: Brief Introduction of the Module

Categories	
Packaging and Number of Pins	LGA; 126-pin
Dimensions	(25 ±0.2) mm × (29 ±0.2) mm × (2.4 ±0.2) mm
Weight	3.6 ±0.2 g
Wireless Network Functions	LTE/GSM/GNSS/Bluetooth/Wi-Fi Scan [1]

2.1. Frequency Bands and Functions

Table 3: Frequency Bands

Wireless Network Type	EG912U-GL
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B12/B13/ B17/B18/B19/B20/ B25/B26/B28/B66
LTE-TDD	B34/B38/B39/B40/B41
GSM	GSM850/EGSM900/DCS1800/PCS1900
GNSS [2]	GPS, GLONASS, BDS, Galileo, QZSS
Bluetooth and Wi-Fi Scan [1] (only for FCC ID: XMR2023EG912UGL)	Bluetooth 4.2 (BR/EDR + BLE) 2.4GHz 802.11b (Rx)

[1] EG912U-GL support Bluetooth and Wi-Fi Scan functions. Due to the shared antenna interface, the two functions cannot be used simultaneously. Bluetooth and Wi-Fi Scan functions are optional (both supported or not), please contact Quectel Technical Support for details.
[2] GNSS function is optional.

2.2. Key Features

Table 4: Key Features

Features	Description
Power Supply	● Supply voltage: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	● Class 4 for GSM850 ● Class 4 for EGSM900 ● Class 1 for DCS1800 ● Class 1 for PCS1900 ● Class 3 for LTE-FDD bands ● Class 3 for LTE-TDD bands
LTE Features	● Supports up to Cat 1 FDD/TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports uplink QPSK and 16QAM ● Supports downlink QPSK, 16QAM, and 64QAM ● Max. transmission data rates: FDD: 10 Mbps (DL)/5 Mbps (UL) TDD: 8.96 Mbps (DL)/3.1 Mbps (UL)
GSM Features	**GPRS:** ● Supports GPRS multi-slot class 12 ● Coding scheme: CS-1/CS-2/CS-3/CS-4 ● Max. transmission data rates: 85.6 kbps (DL)/85.6 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX/HTTPS/FTPS/SSL/FILE/MQTT/MMS protocols ● Support PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM card and ME; ME by default
(U)SIM Interfaces	● Supports USIM/SIM card: 1.8/3.0 V
USB Interface	● Compliant with USB 2.0 specification (slave mode only), with maximum transmission rate up to 480 Mbps ● Used for AT command communication, data transmission, software debugging, firmware upgrade ● Supports USB serial drivers for Windows 7/8/8.1/10, Linux 2.6–5.18, and Android 4.x–12.x
UART Interfaces	**Main UART** ● Used for AT command communication and data transmission ● Baud rates: up to 921600 bps; 115200 bps by default

	● Supports RTS and CTS hardware flow control **Debug UART** ● Used for log output ● Baud rate: 921600 bps ● Cannot be used as a general-purpose serial port **Auxiliary UART** The baud rate is the same as that of the Main UART
SPI Interface	● Supports one SPI interface (master mode only)
I2C Interface	● Supports one I2C interface
PCM Interface	● Supports one PCM interface (slave mode only)
Audio Features	● Supports one analog audio input and one analog audio output ● GSM: HR/FR/EFR/AMR/AMR-WB ● Supports echo cancellation and noise suppression
ADC Interfaces	● Supports two ADC Interfaces
Network Indication	● NET_STATUS used to indicate the network connectivity status
AT Commands	● Compliant with *3G PP TS 27.007* and *3G PP TS 27.005* ● Quectel enhanced AT commands
USB_BOOT Interface	● Supports one download control interface
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● Bluetooth and Wi-Fi Scan antenna interface (ANT_BT/WIFI_SCAN) ● GNSS antenna interface (ANT_GNSS [2]) ● 50 Ω impedance
Position Fixing	● Supports Wi-Fi Scan/GNSS [2]
Temperature Range	● Operating temperature range: -35 to +75 °C [3] ● Extended temperature range: -40 to +85 °C [4] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● Via USB interface and DFOTA
RoHS	● All hardware components are fully compliant with *EU RoHS Directive*

[3] Within operating temperature range, the module meets 3GPP specifications.
[4] Within extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Pin Assignment

The following figure illustrates the pin assignment of the module.

Figure 1: Pin Assignment (Top View)

NOTE

1. USB_BOOT cannot be pulled up before the module's startup.
2. Keep NC and RESERVED pins unconnected, and connect all GND pins to ground.
3. The module supports Dual SIM Single Standby. For details, please contact Quectel Technical

Support.

4. When using pins 18, 19, 30, 38, and 39, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

2.4. Pin Description

The following tables show the pin definition of the module.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current of 1 A at least.

VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 2.5 A.
VDD_EXT	29	PO	Provides 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	Power supply for external GPIO's pull-up circuits. Used with a 2.2 μF bypass capacitor. If unused, keep it open.
Power On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turns on/off the module	V_{IL}max = 0.5 V VBAT power domain	Active low.
RESET_N	17	DI	Resets the module		Active low. If unused, keep it open.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	20	DO	Indicates the module's operation status	1.8 V power domain	If unused, keep it open.
NET_STATUS	21	DO	Indicates the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.5 V Vnom = 5.0 V	If unused, keep it open.
USB_DP	9	AIO	USB differential data (+)		USB 2.0 compliant. Requires differential impedance of 90 Ω. If unused, keep them open.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	$I_O$max = 50 mA	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data		
USIM1_CLK	46	DO	(U)SIM1 card clock		
USIM1_RST	44	DO	(U)SIM1 card reset		
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain	If unused, keep it open. If unused, keep it open.
USIM1_GND	47	-	Ground		Specified ground for (U)SIM1 card
USIM2_VDD	87	PO	(U)SIM2 card power supply	$I_O$max = 50 mA	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	DIO	(U)SIM2 card data		
USIM2_CLK	84	DO	(U)SIM2 card clock		
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain	If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	36	DO	DTE clear to send signal to DCE	1.8 V power domain	Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	37	DI	DTE request to send signal to DCE		Connect to DTE's RTS. If unused, keep it

					open.
MAIN_RXD	34	DI	Main UART receive		If unused, keep them open.
MAIN_DCD	38	DO	Main UART data carrier detect		
MAIN_TXD	35	DO	Main UART transmit		
MAIN_RI	39	DO	Main UART ring indication		
MAIN_DTR	30	DI	Main UART data terminal ready		
Auxiliary UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain	If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain	If unused, keep them open.
DBG_TXD	23	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SCL	40	OD	I2C serial clock		External pull-up resistor is required. 1.8 V power domain only. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	5	DI	PCM data frame sync	1.8 V power domain	If unused, keep them open. Support slave mode only.
PCM_CLK	4	DI	PCM clock		
PCM_DIN	6	DI	PCM data input		

PCM_DOUT	7	DO	PCM data output		
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω impedance.
ANT_BT/ WIFI_SCAN	56	AIO	The shared interface for Bluetooth and Wi-Fi Scan		Bluetooth and Wi-Fi Scan cannot be used at the same time. Wi-Fi Scan antenna can only receive but not transmit. 50 Ω impedance. If unused, keep it open.
ANT_GNSS	49	AI	GNSS antenna interface		50 Ω impedance.
GRFC Antenna Tuner Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	76	DO	Generic RF Controller		If unused, keep them open.
GRFC2	77	DO			
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI_CLK	26	DO	SPI clock	1.8 V power domain	If unused, keep them open.
SPI_CS	25	DO	SPI chip select		
SPI_DIN	88	DI	SPI master mode input		
SPI_DOUT	64	DO	SPI master mode output		
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interfaces	Voltage range: 0 V to VBAT	If unused, keep them open.
ADC1	2	AI			
Analog Audio Interfaces					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
MIC_N	119	AI	Microphone analog input (-)		
MICBIAS	120	PO	Bias voltage output for microphone	Vmax = 3.0 V Vmin = 2.2 V Vnom = 2.2 V	
SPK_P	121	AO	Analog audio differential output (+)		
SPK_N	122	AO	Analog audio differential output (-)		
MIC_P	126	AI	Microphone analog input (+)		
USB_BOOT					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	75	DI	Control pin for module to enter the download mode	1.8 V power domain. V_{IL}min = -0.3 V V_{IL}max = 0.6 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	A circuit that enables the module to enter the download mode must be reserved. If unused, keep it open.Active high.
PSM Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_IND	1	DO	Indicates the module's power saving mode.		If unused, keep them open.
PSM_EINT	96	DI	External interrupt pin. Wakes up the module from PSM.		Pull this pin high externally to exit power saving mode. If unused, keep them open.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	18	DI	Airplane mode control	1.8 V power domain	Pulled up by default. When it is in low voltage

					level, the module can enter the airplane mode. If unused, keep it open.
AP_READY	19	DI	Application processor ready	1.8 V power domain	If unused, keep it open.
GND					
Pin Name	**Pin No.**				
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
RESERVED					
Pin Name	**Pin No.**				
RESERVED	11–14, 16, 51, 57, 63, 65, 66, 78, 92–95, 97–99, 103–118, 123–125				

NOTE

1. The functions of PSM and GRFC are under development and it is currently not recommended to use them. Please consult Quectel Technical Support for details.
2. When using pins 18, 19, 30, 38, and 39, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

2.5. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (UMTS&LTE EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

The following table briefly outlines the operating modes referred in the following chapters.

Table 7: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module remains registered on the network and is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode. In this mode, RF function will be invalid.	
Sleep Mode	In this mode, current consumption of the module is reduced to a low level. The module remains the ability to receive paging message, SMS, voice calls and TCP/UDP data from network normally.	
Power Down Mode	PMU shuts down the power supply. Software is not active and serial interfaces are not accessible. However, operating voltage connected to VBAT pins remain applied.	

NOTE

For more details about AT commands, see ***document [2]***.

3.2. Sleep Mode

The module is able to reduce its current consumption to an ultra-low value in the sleep mode. The

following chapters describe power saving procedures of the module.

3.2.1 UART Application Scenario

If the host communicates with module via UART interface, the following preconditions should be met to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive MAIN_DTR to high level.

The following figure shows the connection between the module and the host.

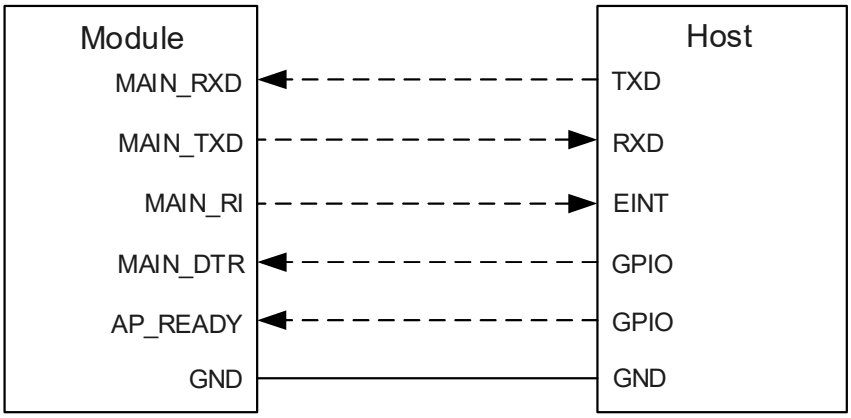


Figure 2: Sleep Mode Application via UART

- Driving MAIN_DTR low will wake up the module.
- When the module has a URC to report, the URC will trigger the behavior of MAIN_RI pin. See ***Chapter 4.10.3*** for details about MAIN_RI behaviors.

NOTE

When using AP_READY, MAIN_DTR, and MAIN_RI (pins 19, 30, and 39), please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.2.2. USB Application Scenario

3.2.2.1. USB Application with USB Remote Wakeup Function

If the host supports USB suspend/resume and remote wakeup function, three preconditions must be met to make the module enter the sleep mode:

- Execute **AT+QSCLK=1** command to enable the sleep mode.
- Ensure the MAIN_DTR is held at a high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure illustrates the connection between the module and the host.

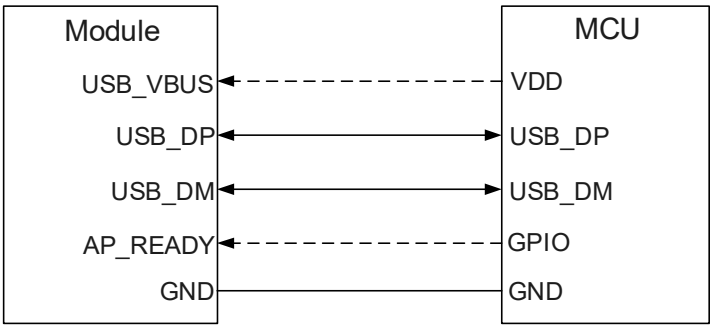


Figure 3: Sleep Mode Application with USB Remote Wakeup

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the module will send remote wake-up signals to USB bus to wake up the host.

NOTE

USB suspend is supported on Linux system but not on Windows system.

3.2.2.2. USB Application with USB Suspend/Resume and MAIN_RI Function

If the host supports USB suspend/resume, but does not support remote wake-up function, the MAIN_RI signal is needed to wake up the host.

In this case, three preconditions can make the module enter the sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure the MAIN_DTR is held at high level or keep it open.
- Ensure the host's USB bus, which is connected with the module's USB interface, enters suspend state.

The following figure illustrates the connection between the module and the host.

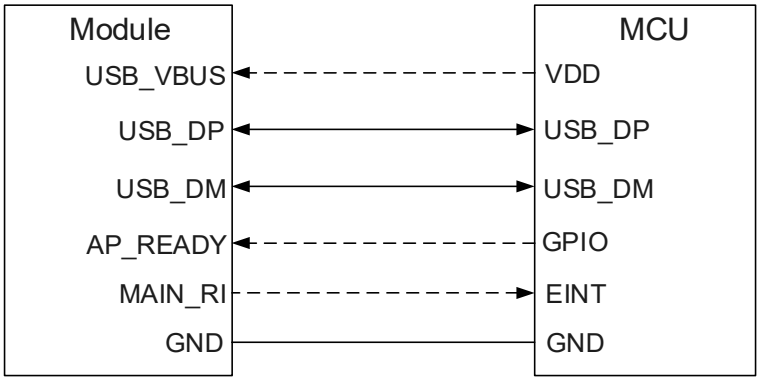


Figure 4: Sleep Mode Application with MAIN_RI

- You can wake up the module by sending data to it through USB.
- When the module has a URC to report, the URC will trigger the behaviors of MAIN_RI pin. See ***Chapter 4.10.3*** for details about MAIN_RI behaviors.

NOTE

USB suspend is supported on Linux system but not on Windows system.

3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, disconnect USB_VBUS with an external control circuit to make the module enter into sleep mode.

- Execute **AT+QSCLK=1** command to enable sleep mode.
- Ensure the MAIN_DTR is held at a high level or keep it open.
- Disconnect the USB_VBUS.

The following figure illustrates the connection between the module and the host.

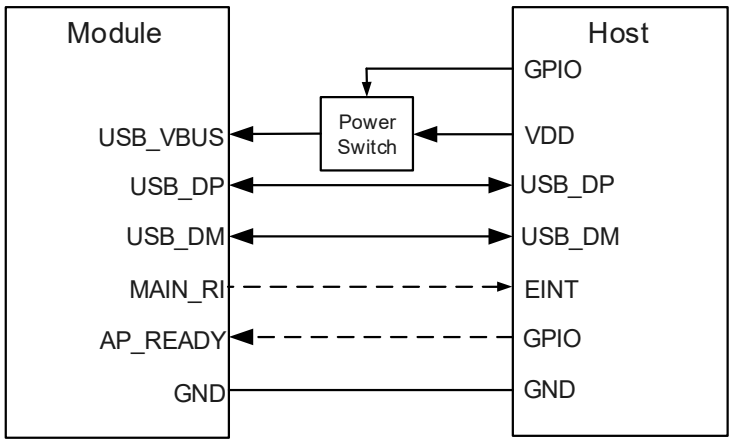


Figure 5: Sleep Mode Application without Suspend Function

You can wake up the module by turning on the power switch to supply power to USB_VBUS.

NOTE

1. Please pay attention to the level match shown in dotted line between the module and the host.
2. When using AP_READY, MAIN_DTR, and MAIN_RI (pins 19, 30, and 39), please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled and all AT commands related to it will be inaccessible. This mode can be set via the following ways.

3.3.1. Hardware

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode, which is disabled by default, can be enabled through **AT+QCFG="airplanecontrol",1**. When such a control function is enabled, you can drive it to low level to make the module enter airplane mode.

NOTE

When using W_DISABLE# (pin 18), please note that it will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before it can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

3.3.2. Software

AT+CFUN=<fun> provides the choice of functionality level through setting **<fun>** to 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality. Both RF function and (U)SIM functions are disabled.
- **AT+CFUN=1:** Full functionality (by default).
- **AT+CFUN=4:** RF function is disables (airplane mode).

NOTE

For more details about AT command, see ***document [2]***.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides 4 VBAT pins for connection with an external power supply.

- Two VBAT_RF pins for RF part.
- Two VBAT_BB pins for BB part.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32, 33	PI	Power supply for the module's baseband part	3.3	3.8	4.3	V
VBAT_RF	52, 53	PI	Power supply for the module's RF part	3.3	3.8	4.3	V

GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102

3.4.2. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of 3.0 A at least for the GSM or GSM & LTE and 2.0 A for the LTE only. If the voltage drops between input and output is not too high, it is suggested that an LDO should be used to supply power to the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure illustrates a reference design for +5 V input power source. The typical output of the power supply is about 3.8 V and the maximum load current is 3.0 A.

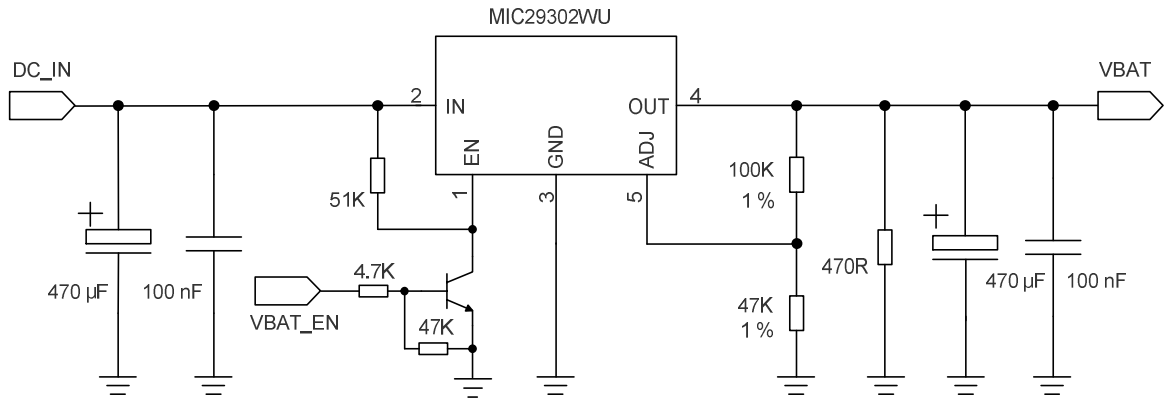


Figure 6: Reference Design of Power Supply

3.4.3. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Please make sure the input voltage never drops below 3.3 V.

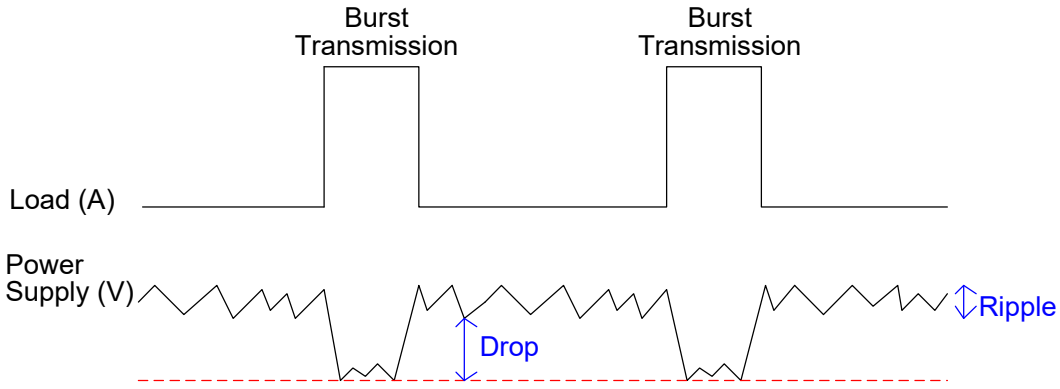


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 μF with low ESR (ESR = 0.7 Ω) should be used, and a multi-layer ceramic chip (MLCC) capacitor array should also be reserved due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to the VBAT_BB and VBAT_RF pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be no less than 2 mm; and the width of VBAT_RF trace should be no less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, in order to ensure the stability of power source, it is suggested that a TVS array of which reverse stand-off voltage is 4.7 V and peak pulse power is up to 2550 W should be used. The reference circuit is shown as below.

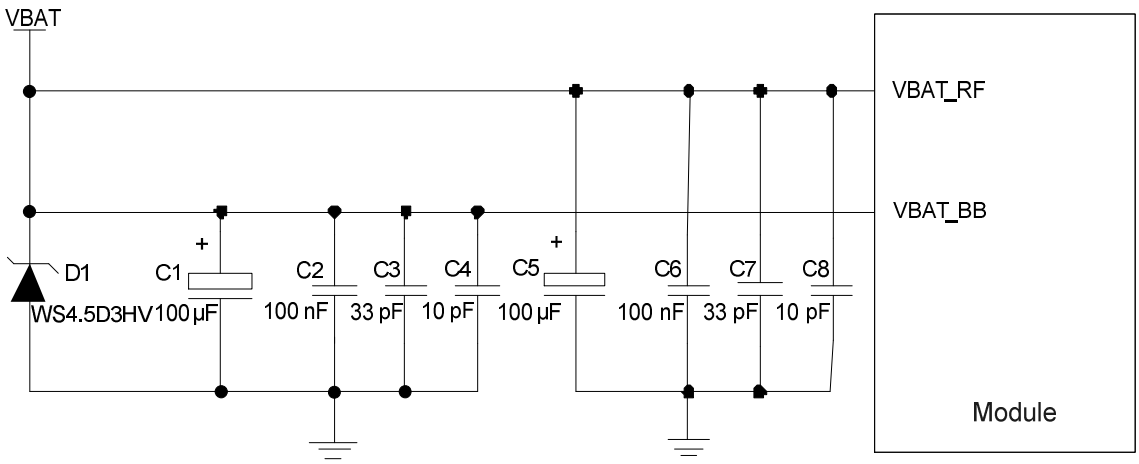


Figure 8: Power Supply

3.5. Turn On

3.5.1. Turn On with PWPKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turns on/off the module	VBAT power domain.

When the module is in power down mode, you can turn it on to normal mode by driving the PWRKEY pin low for at least 2 s. It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

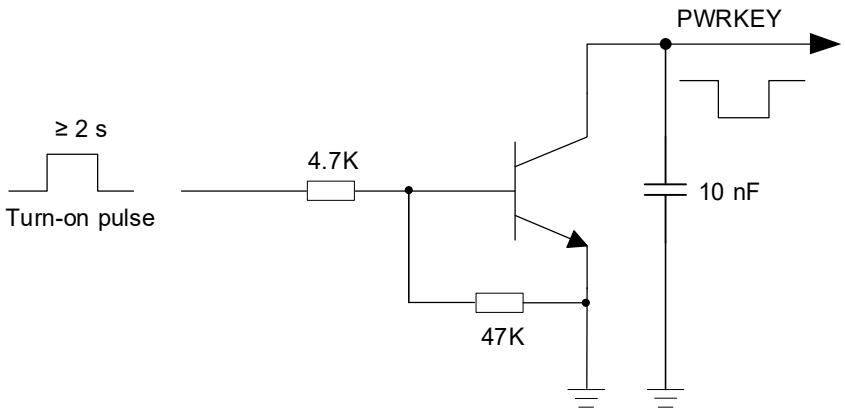


Figure 9: Turning on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When you are pressing the key, electrostatic strike may be generated from finger. Therefore, you must place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

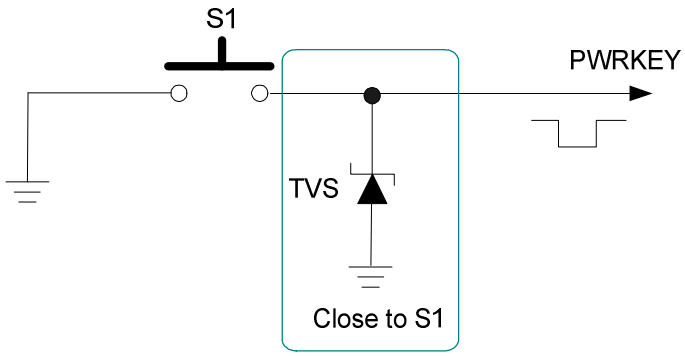


Figure 10: Turning on the Module Using Button

The power-up scenario is illustrated in the following figure.

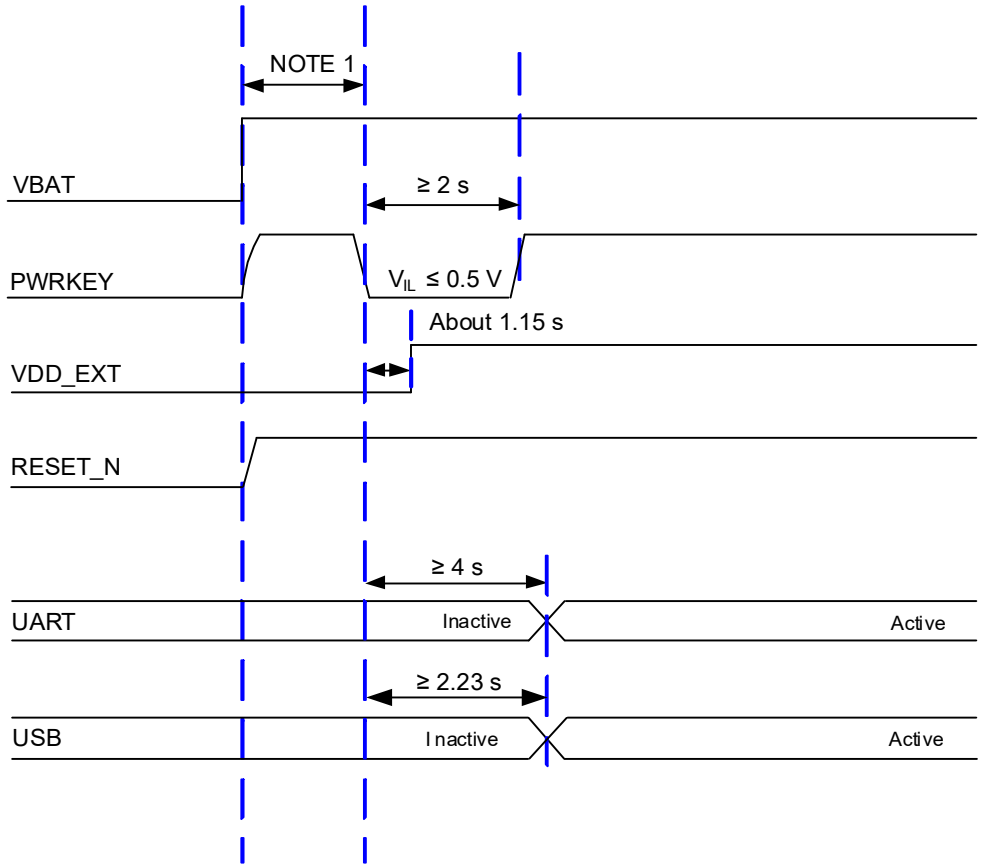


Figure 11: Power-up Timing

NOTE

1. Make sure that the VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin is no less than 30 ms.
2. PWRKEY can be pulled down directly to GND with a recommended 1 kΩ resistor if the module needs to be powered on automatically and shutdown is not needed.

3.6. Turn Off

The following procedures can be used to turn off the module:

- Use the PWRKEY pin.
- Use **AT+QPOWD**.

3.6.1. Turn Off with PWPKEY

Drive the PWRKEY pin low for at least 3 s and then release PWRKEY. After this, the module executes power-down procedure. The power-down scenario is illustrated in the following figure.

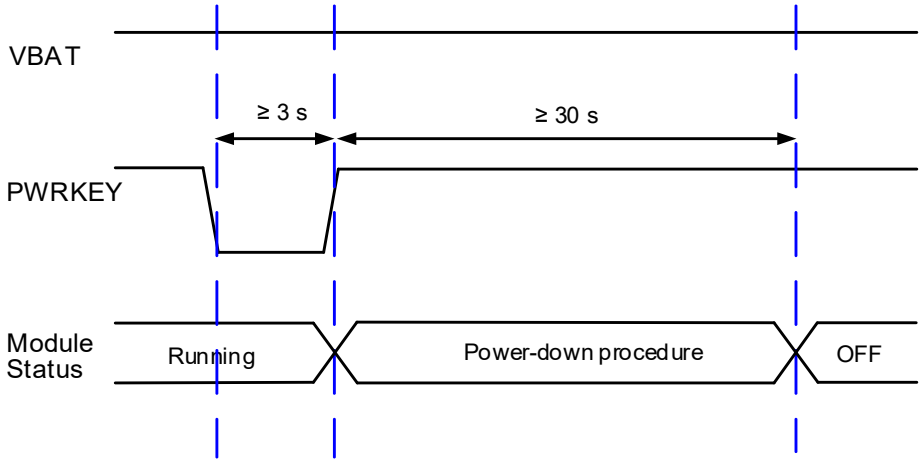


Figure 12: Timing of Turning off the Module

3.6.2. Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

Please refer to ***document [2]*** for details about **AT+QPOWD** command.

NOTE

1. To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.
2. When the PWRKEY pin has been kept pulled down directly to GND, the module will not boot automatically after being turned off with the AT command. In this case, it is necessary to forcibly disconnect the VBAT power supply and power on the module again. Therefore, we recommend to use a control circuit to drive the PWEKEY high/low to turn on/off the module instead of keeping the PWRKEY connected to GND.
3. When being turned off, the module will log out of the network. The time for logging out relates to its network status. Thus, please pay attention to the shutdown time in your design because the actual shutdown time varies according to the network status.

3.7. Reset

The RESET_N pin can be used to reset the module. The module can be reset by driving the RESET_N pin low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 10: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Resets the module	VBAT power domain. If unused, keep it open.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control the RESET_N.

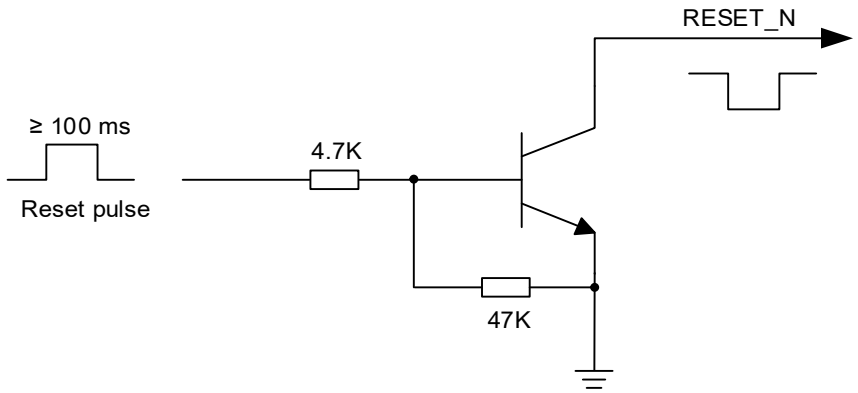


Figure 13: Reference Circuit of RESET_N by Using Driving Circuit

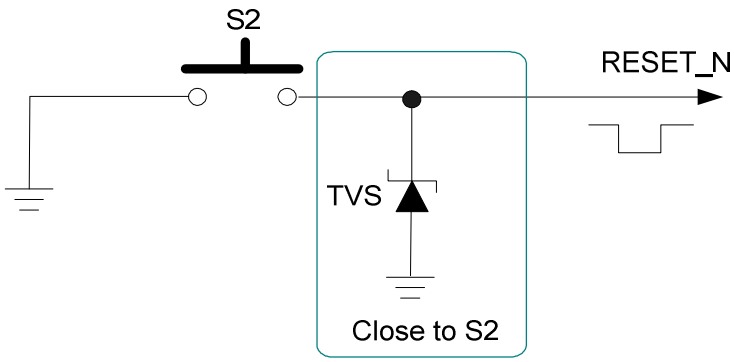


Figure 14: Reference Circuit of RESET_N by Using Button

The reset scenario is illustrated in the following figure.

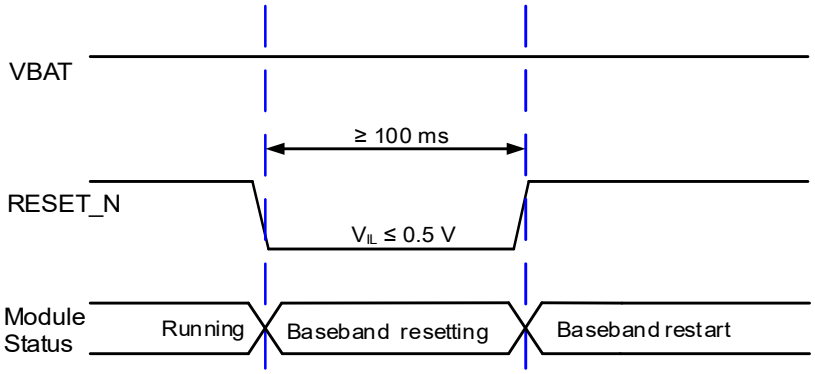


Figure 15: Timing of Resetting the Module

NOTE

1. Ensure that there is no large capacitance exceeding 10 nF on PWRKEY and RESET_N pins.
2. It is recommended to use RESET_N only when you fail to turn off the module with the **AT+QPOWD** or PWRKEY pin.

4 Application Interfaces

4.1. Analog Audio Interfaces

The module provides one analog audio input channel and one analog audio output channel. The pin definitions are shown in the following table.

Table 11: Pin Definition of Analog Audio Interfaces

Pin Name	Pin No.	I/O	Description
MIC_N	119	AI	Microphone analog input (-)
MICBIAS	120	PO	Bias voltage output for microphone
SPK_P	121	AO	Analog audio differential output (+)
SPK_N	122	AO	Analog audio differential output (-)
MIC_P	126	AI	Microphone analog input (+)

- AI channels are differential input channels, which can be applied for input of microphone (usually an electret microphone is used).
- AO channels are differential output channels, which can be applied for output of handset, earpiece and loudspeaker. (The module has no built-in PA, the analog audio output SPK can be directly used as handset function, and if connected with external PA, it can be used as loudspeaker function.)

4.1.1. Audio Interfaces Design Considerations

It is recommended to use the electret microphone with dual built-in capacitors (e.g., 10 pF and 33 pF) for filtering out RF interference, thus reducing TDD noise. The 33 pF capacitor is applied for filtering out RF interference when the module is transmitting at EGSM900. Without placing this capacitor, TDD noise could be heard. The 10 pF capacitor here is used for filtering out RF interference at DCS1800. Note that the resonant frequency point of a capacitor largely depends on the material and production technique. Therefore, you would have to discuss with your capacitor vendors to choose the most suitable capacitor for filtering out high-frequency noises.

The filter capacitors on the PCB board should be placed as close to the audio devices or audio interfaces as possible, and the traces should be as short as possible. They should go through the filter capacitors before arriving at other connection points.

To reduce radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Power traces should not be parallel with and also should be far away from the audio traces.

The differential audio traces must be routed according to the differential signal layout rule.

4.1.2. Microphone Interface Design

The microphone channel reference circuit is shown in the following figure.

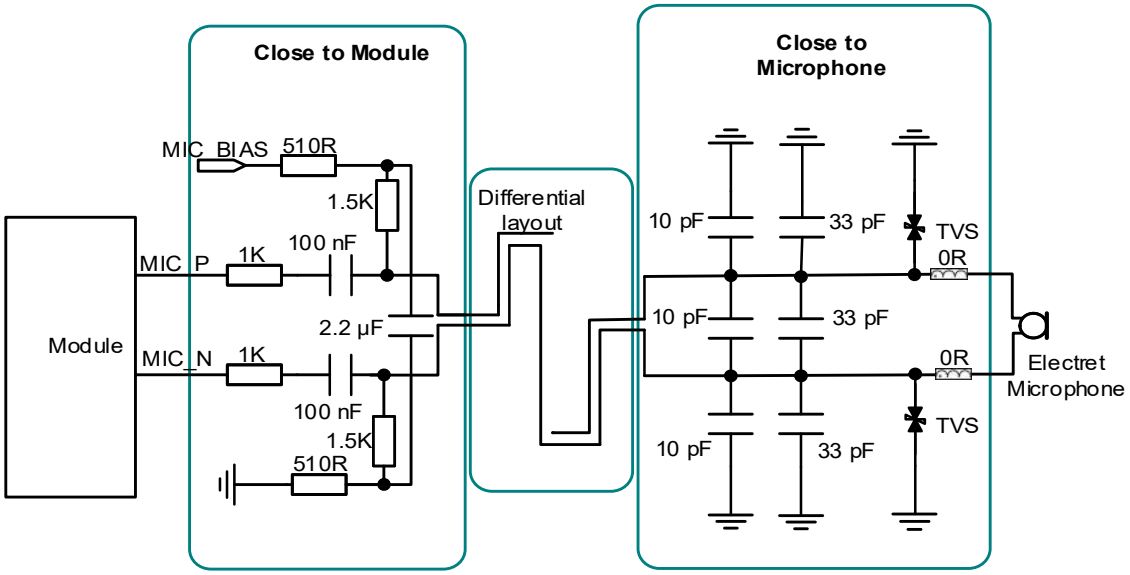


Figure 16: Reference Design for Microphone Interface

NOTE

MIC channel is sensitive to ESD, so it is not recommended to remove the ESD components used for protecting the MIC.

4.1.3. Earpiece Interface Design

The earpiece channel reference circuit is shown in the following figure:

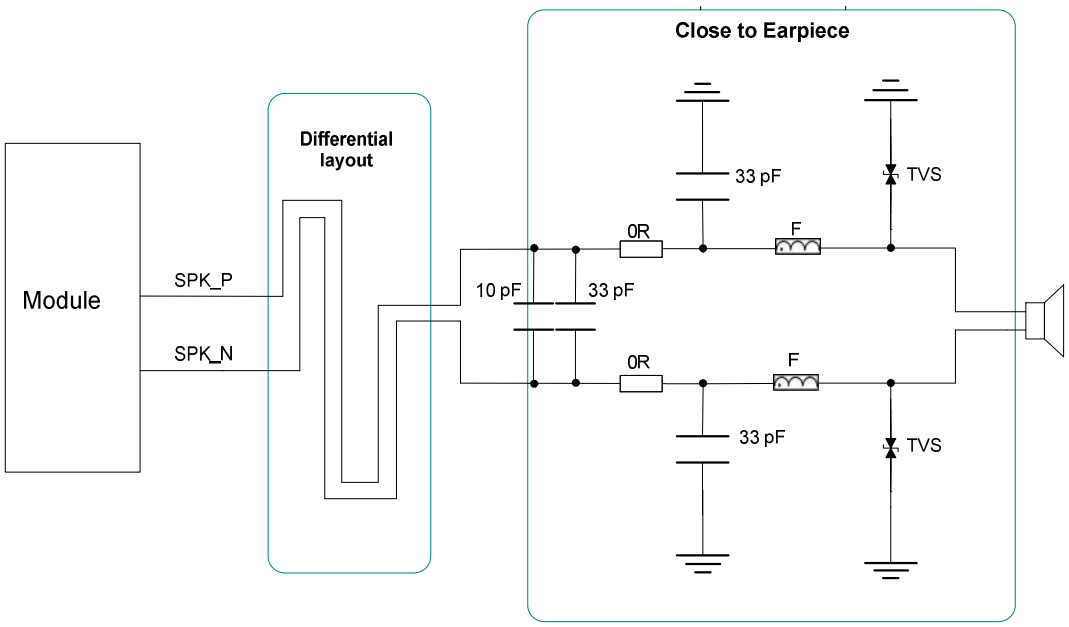


Figure 17: Reference Design for Earpiece Interface

4.2. USB Interface

The module provides an integrated Universal Serial Bus (USB) interface compliant with the USB 2.0 specification and supporting full-speed (12 Mbps) and high-speed (480 Mbps) modes. The USB interface can only serve as a slave device.

Table 12: Functions of USB Interface

Functions	
AT command communication	√
Data transmission	√
Software debugging	√
Firmware upgrade	√

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typ. 5.0 V Min. 3.5 V
USB_DP	9	AIO	USB differential data (+)	USB 2.0 compliant. Requires differential impedance of 90 Ω. If unused, keep them open.
USB_DM	10	AIO	USB differential data (-)	

For more details about the USB 2.0 specifications, visit http://www.usb.org/home.

Reserve test points for debugging and firmware upgrade in your design. The following figure shows a reference circuit of USB interface.

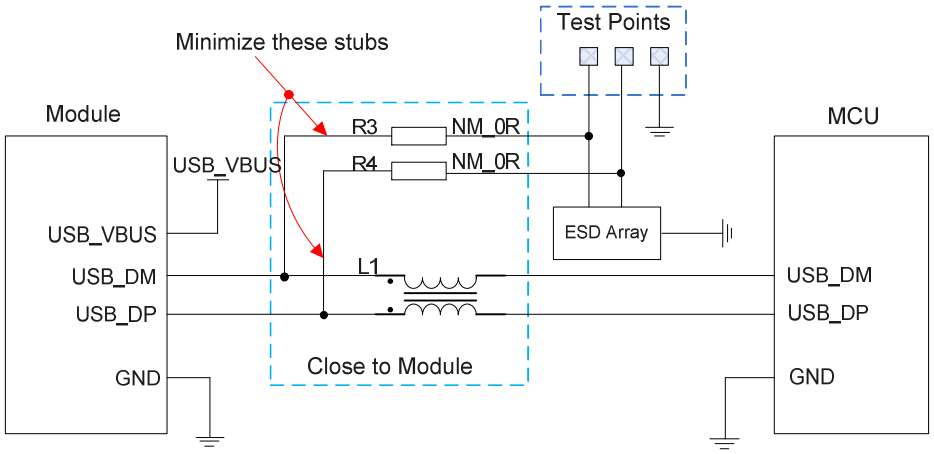


Figure 18: Reference Circuit of USB Application

A common mode choke L1 is recommended to be added in series between the module and your MCU to suppress EMI spurious transmission. Meanwhile, the 0 Ω resistors (R3 and R4) should be added in series between the module and the test points so as to facilitate debugging, and the resistors are not mounted by default. To ensure the signal integrity of USB data lines, L1, R3, and R4 must be placed close to the module, and resistors R3 and R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

When designing the USB interface, you should follow the following principles to meet USB 2.0 specification.

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under or near crystals, oscillators, magnetic devices, and RF signal traces. Route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on

that layer and ground planes above and below.

- Pay attention to the selection of the ESD component on the USB data line. Its stray capacitance should not exceed 2 pF and should be placed as close as possible to the USB connector.

4.3. USB_BOOT Interface

The module provides a USB_BOOT interface. Pull up USB_BOOT to VDD_EXT before powering on the module, which will enter the download mode when it is turned on. In this mode, the module supports firmware upgrade over USB interface.

Table 14: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	1.8 V power domain. Active high. A circuit that enables the module to enter the download mode must be reserved. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT interface.

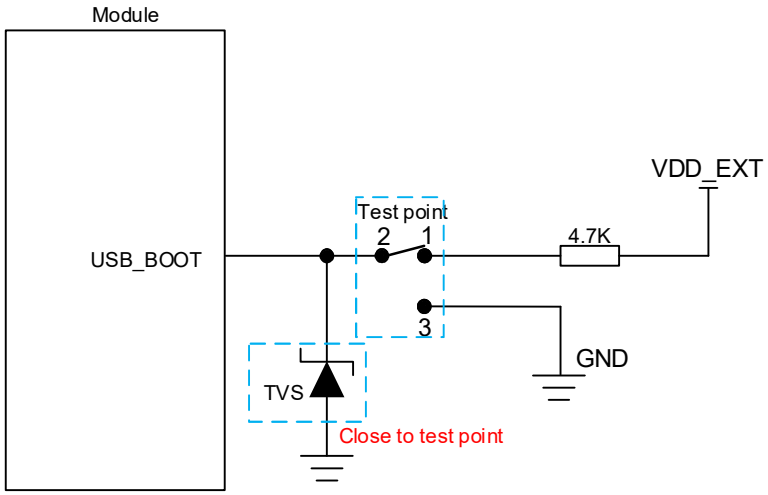


Figure 19: Reference Circuit of USB_BOOT Interface

4.4. (U)SIM Interfaces

The module provides two (U)SIM interfaces that supports Dual SIM Single Standby. The (U)SIM interfaces circuitry meets ETSI requirement and IMT-2000 specification. Either 1.8 V or 3.0 V (U)SIM card is supported.

Table 15: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM1_GND	47	-	Ground	Specified ground for (U)SIM1 card
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V (U)SIM card is supported and can be identified automatically by the module.
USIM2_DATA	86	IO	(U)SIM2 card data	
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open

The module supports (U)SIM card hot-plug via the USIM_DET pin and both high- and low-level detections are supported. By default, the function is disabled, and see **AT+QSIMDET** in ***document [2]*** for more details.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

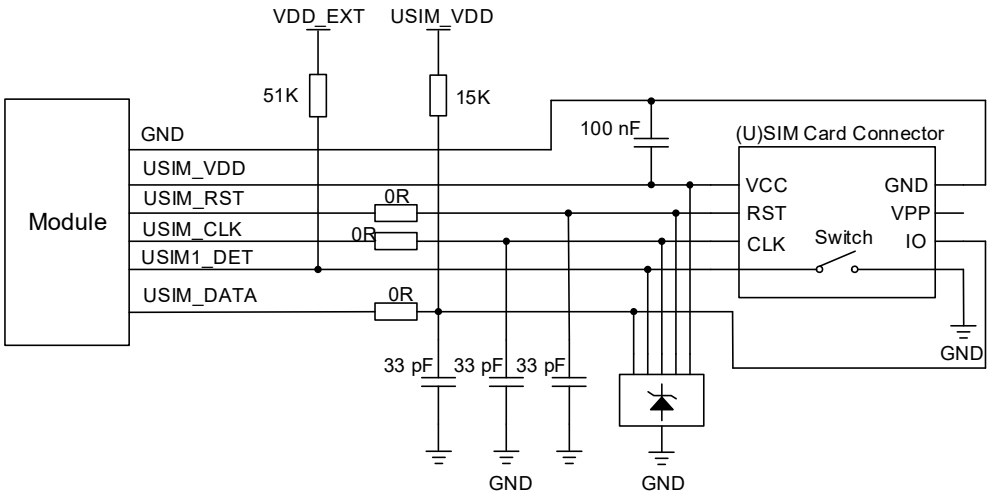


Figure 20: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, please keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

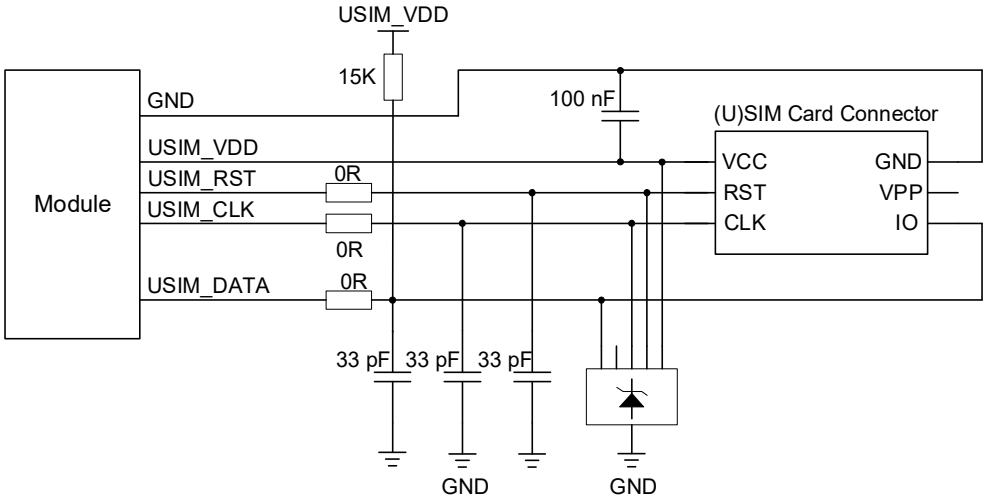


Figure 21: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in (U)SIM circuit design:

- Place (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Ensure the bypass capacitor between USIM_VDD and GND is less than 1 μF, and the capacitor should be close to the (U)SIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and

shield them with surrounded ground.

- To offer good ESD protection, it is recommended to add a TVS array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA can improve anti-jamming capability of the (U)SIM card. If the (U)SIM card traces are too long, or the interference source is relatively close, it is recommended to add a pull-up resistor near the (U)SIM card connector.

4.5. I2C and PCM Interfaces

The module provides one I2C interface and one pulse code modulation (PCM) interface. The PCM interface of the module only supports slave mode; therefore, the clock signal of the codec IC needs to be provided externally.

PCM interface supports the short frame mode and the module can be used as the slave mode only. In short frame mode, PCM_CLK = the number of channels × PCM_SYNC × 16 bit, where the number of channels supports 1~4 channels, but the module will only take the data on the first channel; PCM_SYNC is equal to the audio sampling rate, which supports 8~44.1kHz.

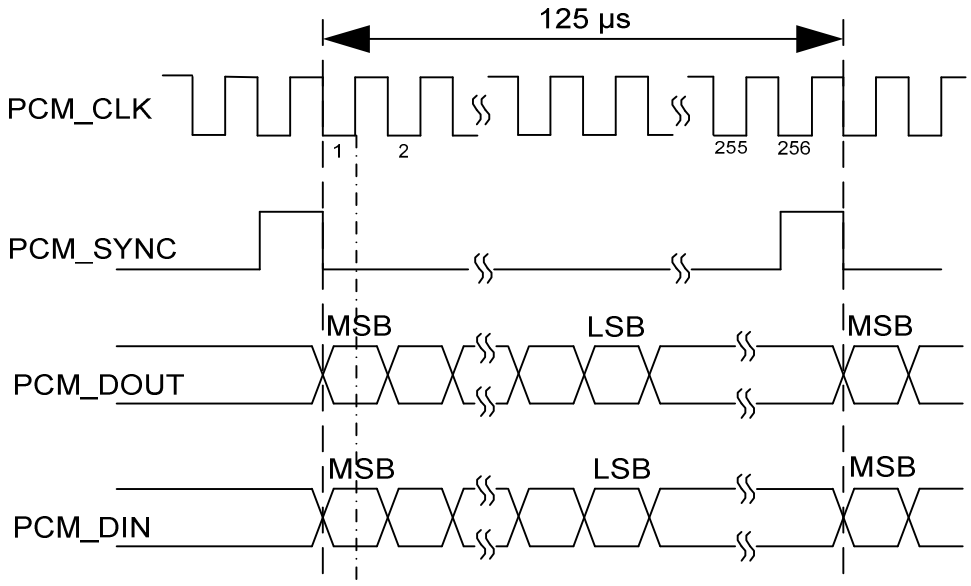


Figure 22: Timing of PCM mode

NOTE

The clocks of PCM_SYNC and PCM_CLK are provided by the codec of master device, but the provided PCM_SYNC frequency must be equal to the sampling frequency of the audio file played by the module.

Table 16: Pin Definition of I2C and PCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock	External pull-up resistor is required. 1.8 V power domain only. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data	
PCM_DIN	6	DI	PCM data input	1.8 V power domain. If unused, keep them open.
PCM_DOUT	7	DO	PCM data output	
PCM_SYNC	5	DI	PCM data frame sync	
PCM_CLK	4	DI	PCM clock	

The following figure shows a reference design of I2C and PCM interfaces with an external codec IC.

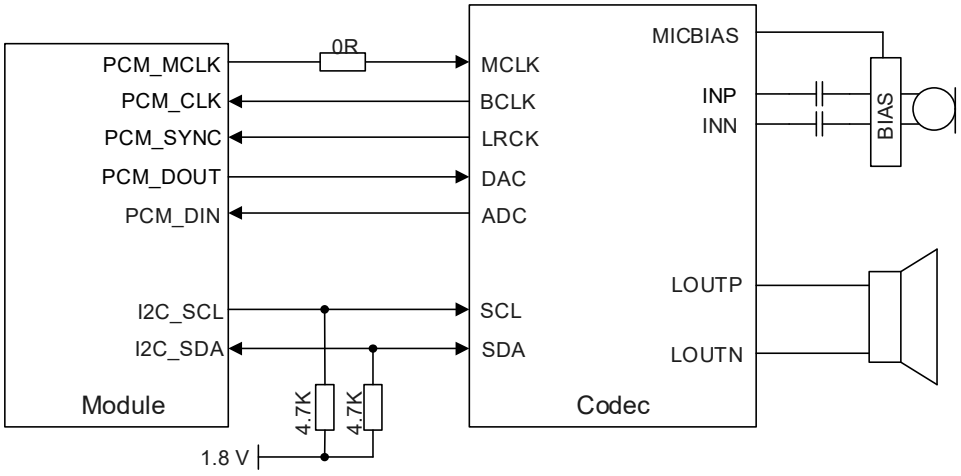


Figure 23: Reference Circuit of I2C and PCM Application with Audio Codec

NOTE

1. It is recommended to reserve an RC (R = 22 Ω, C = 22 pF) circuit on the PCM traces, especially for PCM_CLK.
2. The I2C interface supports simultaneous connection of multiple peripherals except for codec IC. In

other words, if a codec IC has been mounted on the I2C bus, no other peripherals can be mounted; if there is no codec IC on the bus, multiple peripherals can be mounted.

3. For PCM external Codec solution, it is recommended to use the clock solution provided by the module. However, if the pin 95 (configured as PCM_MCLK) provides the clock signal of audio Codec chip, it cannot be for other functions.

4.6. UART Interfaces

The module provides three UART interfaces: main UART, debug UART, and auxiliary UART. Their features are described as follows.

- Main UART interface supports baud rates of 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps, and 921600 bps, and the default setting is 115200 bps. It supports RTS and CTS hardware flow control. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 921600 bps baud rate. It is used for log output.
- Auxiliary UART: The baud rate is the same as that of the Main UART.

Table 17: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	DTE clear to send signal to DCE (connect to DTE's CTS)	1.8 V power domain. If unused, keep them open.
MAIN_RTS	37	DI	DTE request to send signal to DCE (connect to DTE's RTS)	
MAIN_RXD	34	DI	Main UART receive	
MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	

Table 18: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	1.8 V power domain.

DBG_TXD	23	DO	Debug UART transmit	If unused, keep them open.

Table 19: Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	27	DO	Auxiliary UART transmit	1.8 V power domain. If unused, keep them open.
AUX_RXD	28	DI	Auxiliary UART receive	

The module provides 1.8 V UART interfaces. Use a level shifter if the application is equipped with a 3.3 V UART interface. A level shifter TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

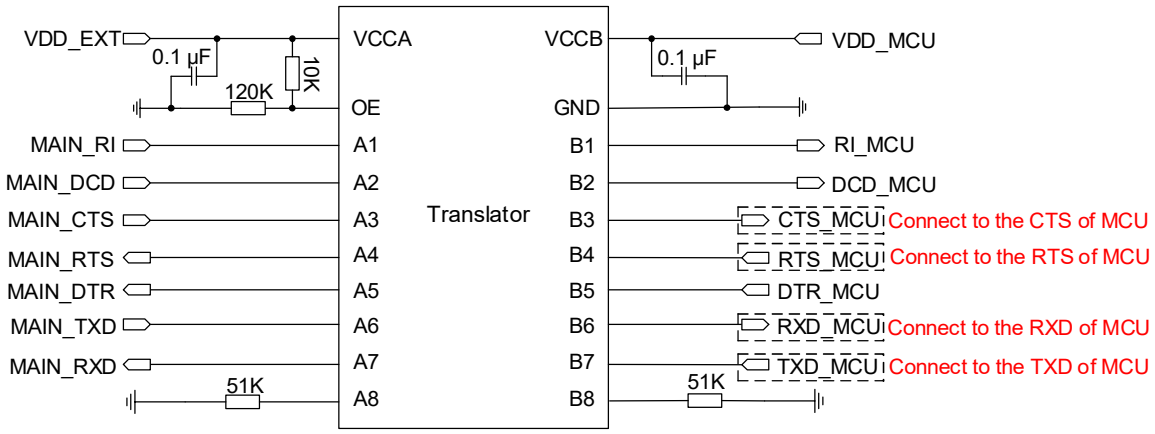


Figure 24: Reference Circuit with Translator Chip

Please visit http://www.ti.com for more information.

Another example with transistor circuit is shown as follows. For the design of circuits in dotted lines, please refer to that of the circuits in solid lines, but please pay attention to the direction of connection.

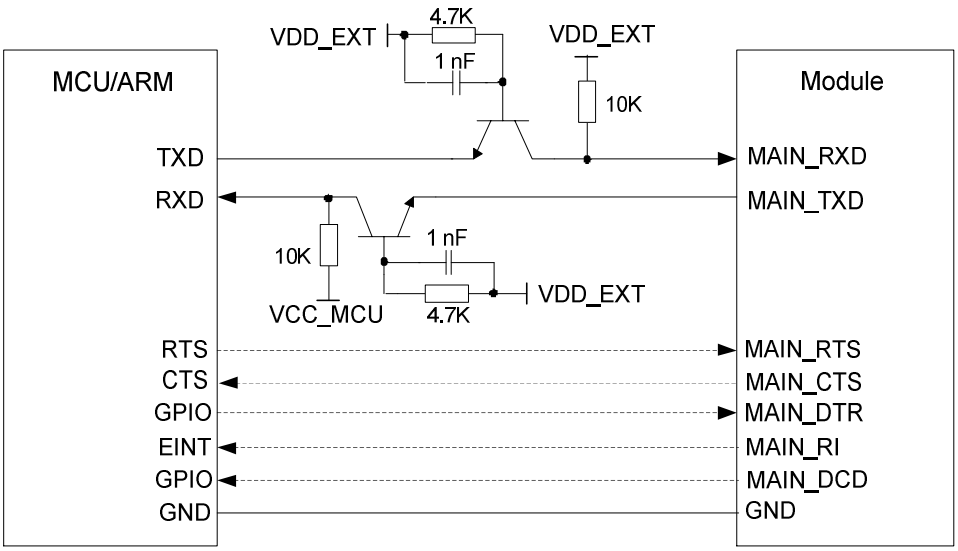


Figure 25: Reference Circuit with Transistor Circuit

NOTE

1. Transistor circuit solution is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.
3. When using pins 30, 38, and 39, please note that these pins will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

4.7. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. You can use **AT+QADC=0** and **AT+QADC=1** to read the voltage values on ADC0 and ADC1 respectively. See ***document [2]*** for more details.

To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 20: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment

ADC0	24	AI	General-purpose ADC interfaces	A 1 kΩ series resistor is required for use. If unused, keep them open.
ADC1	2	AI		

Table 21: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	VBAT	V
ADC1 Voltage Range	0	-	VBAT	V
ADC Resolution	-	12	-	bits

NOTE

1. The input voltage of ADC should not exceed its corresponding voltage range.
2. Do not supply any voltage to ADC pins when VBAT is removed.
3. Considering the difference of ADC voltage range among Quectel modules, when it is necessary to use ADC pins, it is strongly recommended to reserve the voltage divider circuit for better compatibility with other Quectel modules. The resistance of the divider must be less than 100 kΩ, otherwise the measurement accuracy of the ADC will be significantly reduced. When the divider circuit is not used, the ADC pins require 1 kΩ resistance in series.

4.8. SPI Interface

The module provides an SPI interface that only supports master mode. It has a working voltage of 1.8 V and a maximum clock frequency of 25 MHz.

Table 22: Pin Definition of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	1.8 V power domain. If unused, keep them open.
SPI_CS	25	DO	SPI chip select	
SPI_DIN	88	DI	SPI master mode input	
SPI_DOUT	64	DO	SPI master mode output	

NOTE

When the 4-wire SPI interface is connected to NOR Flash, it supports basic flash read, write, erase, and other operations, but you need to perform wear leveling. It does not support file system and can only be used for storage purpose.

4.9. PSM Interface*

The module supports power saving mode (PSM). It enters the PSM through the following AT commands when working normally.

- **AT+CFUN=4:** Enter airplane mode.
- **AT+QSCLK=3:** Enable PSM.
- **AT+CFUN=1:** Exit airplane mode.

Pulling up the PSM_EINT pin externally or setting the timer by software will enable the module to exit PSM.

Table 23: Pin Definition of PSM Interface

Pin Name	Pin No.	I/O	Description
PSM_IND	1	DO	Indicates the module's power saving mode.
PSM_EINT	96	DI	External interrupt pin. Wakes up the module from PSM.

4.10. Indication Signals

Table 24: Pin Definition of Indication Signals

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicates the module's operation status	1.8 V power domain. If unused, keep them open.
MAIN_RI	39	DO	Main UART ring indication	
NET_STATUS	21	DO	Indicates the module's network activity status	

4.10.1. NET_STATUS

The network indication pin NET_STATUS can drive the network status indicator. The following table describes its pin definition and working states in different network status.

Table 25: Pin Definition of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
NET_STATUS	21	DO	Indicates the module's network activity status	V_{OH}min = 1.35 V V_{OL}max = 0.45 V	1.8 V power domain. If unused, keep it open.

Table 26: Working States of Network Connection Status/Activity Indication

Pin Name	State	Network Status
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker quickly (234 ms high/266 ms low)	Registered on network and idle
	Flicker rapidly (63 ms low /62 ms high)	Data transfer is ongoing
	Always high	Voice calling

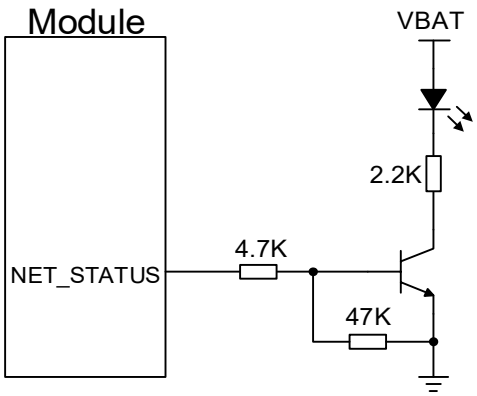


Figure 26: Reference Circuit of Network Status Indication

4.10.2. STATUS

The STATUS pin is an open drain output for indicating the module's operation status. It will output high level when module is powered on successfully.

Table 27: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicates the module's operation status	1.8 V power domain. If unused, keep it open.

A reference circuit is shown as below.

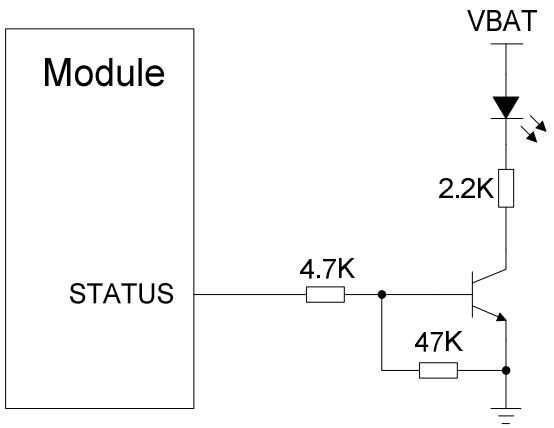


Figure 27: Reference Circuit of STATUS

4.10.3. MAIN_RI

You can configure MAIN_RI behaviors with **AT+QCFG="risignaltype","physical"**. No matter on which port a URC is presented, the URC will trigger the behaviors of MAIN_RI.

MAIN_RI behavior can be configured flexibly. The default behaviors of the MAIN_RI are shown as below.

Table 28: Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.

URC	MAIN_RI outputs 120 ms low pulse when a new URC returns.

The MAIN_RI behaviors can be changed via **AT+QCFG="urc/ri/ring"**. See ***document [2]*** for details.

NOTE

1. The URC can be output via UART port, USB AT port, and USB modem port, which can be set by **AT+QURCCFG**. The default setting is USB AT port.
2. When using AP_READY and MAIN_RI (pins 19 and 39), please note that they will have a period of variable level state (not controllable by software) after the module is powered on: first high level (3 V) for 2 s and then low level (0 V) for 1.2 s, before they can be configured as 1.8 V input or output. Please evaluate whether the unstable output state on power-up meets your application design requirements based on the specific usage scenario and circuit design.

5 Antenna Interfaces

The module provides a main antenna interface, a Wi-Fi Scan/Bluetooth antenna interface and a GNSS antenna interface. The antenna ports have an impedance of 50 Ω.

5.1. Main Antenna and Bluetooth/Wi-Fi Scan Antenna Interfaces

5.1.1. Pin Definition

Table 29: Pin Definition of RF Antennas

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance.
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_BT/WIFI_SCAN	56	AIO	The shared interface for Bluetooth and Wi-Fi Scan	Bluetooth and Wi-Fi Scan cannot be used simultaneously; Wi-Fi Scan can only receive but not transmit. 50 Ω impedance. If unused, keep it open.

5.1.2. Operating Frequency

Table 30: Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)
GSM850	824–849	869–894
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
PCS1900	1850–1910	1930–1990

LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B2	1850–1910	1930-1990
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B4	1710–1755	2110–2155
LTE-FDD B5	824–849	869–894
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B12	699–716	729–746
LTE-FDD B13	777–787	746–756
LTE-FDD B17	704–716	734–746
LTE-FDD B18	815–830	860–875
LTE-FDD B19	830–845	875–890
LTE-FDD B20	832–862	791–821
LTE-FDD B25	1850–1915	1930–1995
LTE-FDD B26	814–850	859–894
LTE-FDD B28	703–748	758–803
LTE-FDD B66	1710–1780	2110–2180
LTE-TDD B34	2010–2025	2010–2025
LTE-TDD B38	2570–2620	2570–2620
LTE-TDD B39	1880–1920	1880–1920
LTE-TDD B40	2300–2400	2300–2400
LTE-TDD B41	2496–2690	2496–2690

5.1.3. Reference Design of Antenna Interfaces

A reference design of ANT_MAIN pin and ANT_BT/WIFI_SACN pin are shown as below. A π-type matching circuit should be reserved for better RF performance. The capacitors are not mounted by default.

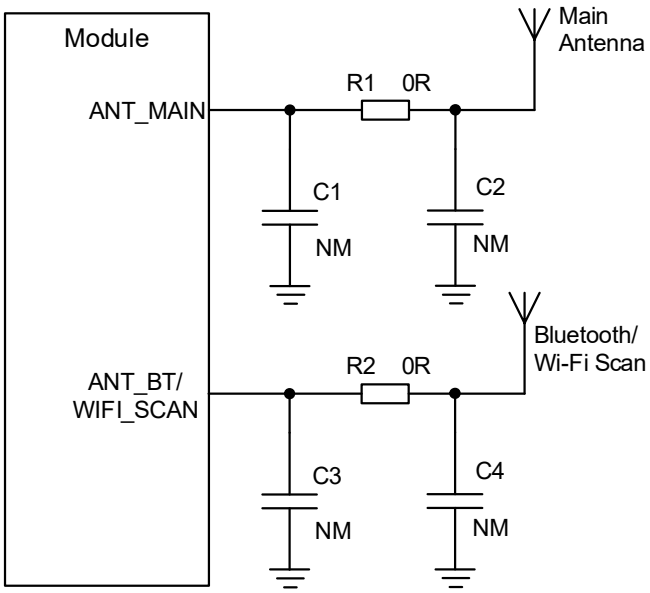


Figure 28: Reference Circuit of RF Antennas

5.2. GNSS Antenna Interface

The following tables list the pin definition and frequency characteristics of the GNSS antenna interface respectively.

Table 31: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 32: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS (Compass)	1561.098 ±2.046	MHz

QZSS	1575.42	MHz

A reference design of GNSS antenna is shown as below:

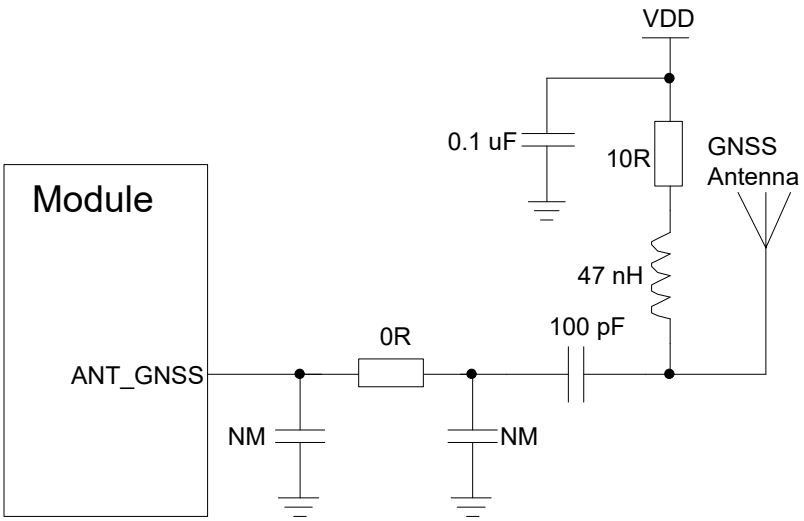


Figure 29: Reference Circuit of GNSS Antenna

NOTE

1. An external LDO can be selected to supply power according to the active antenna requirement.
2. The VDD circuit is not needed if you select a passive antenna.

5.2.1. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between the RF traces and the ground (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

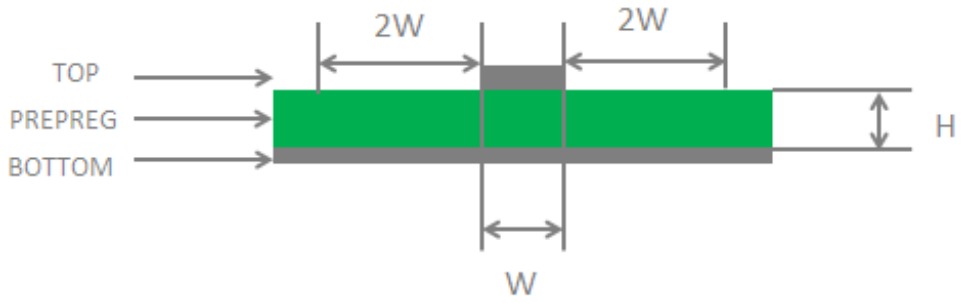


Figure 30: Microstrip Design on a 2-layer PCB

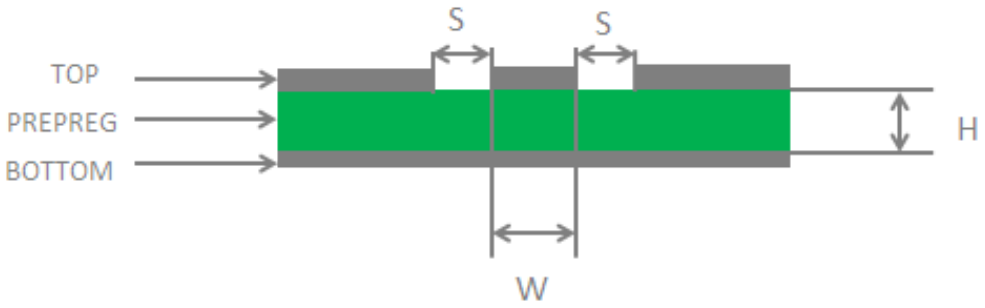


Figure 31: Coplanar Waveguide Design on a 2-layer PCB

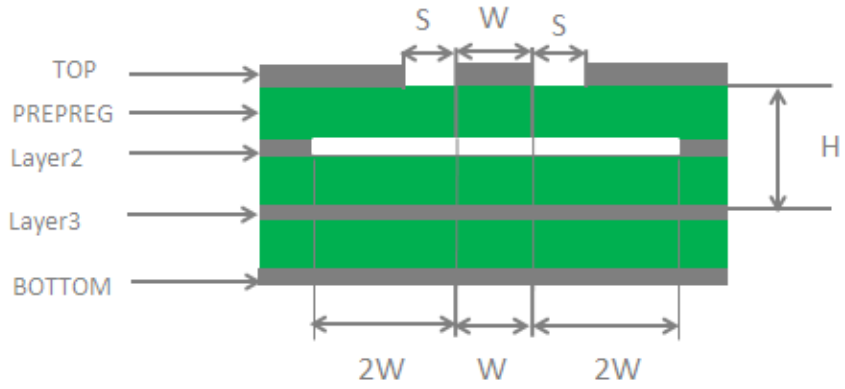


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

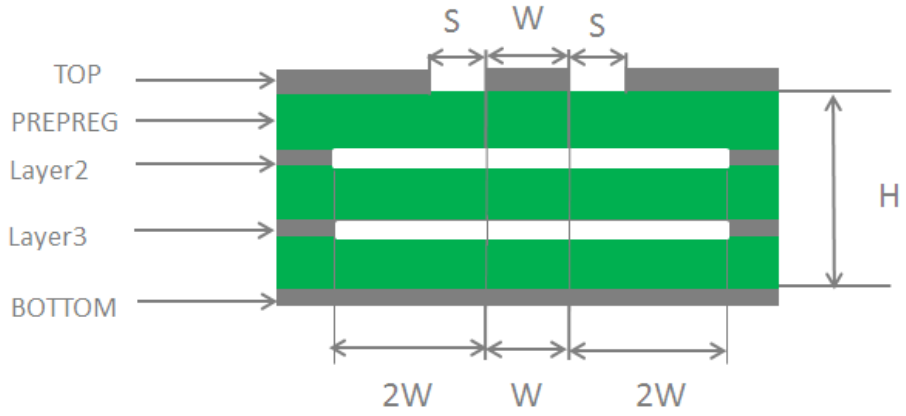


Figure 33: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.3. Antenna Installation

5.3.1. Antenna Design Requirement

Table 33: Requirements for Antenna Design

Type	Requirements
GSM/LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < **1 dB:** LB (< 1 GHz) < **1.5 dB:** MB (1–2.3 GHz) < **2 dB:** HB (> 2.3 GHz)

5.3.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

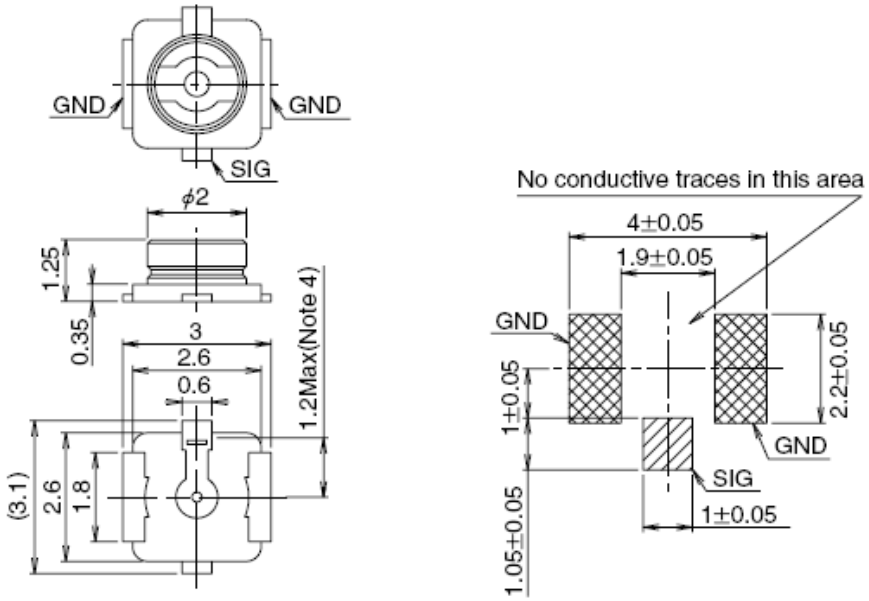


Figure 34: Dimensions of Receptacle (Unit: mm)

U.FL-LP serial mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

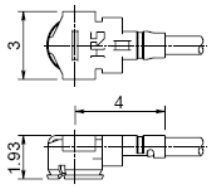
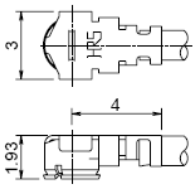
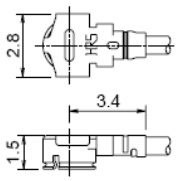
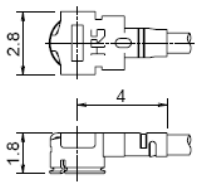
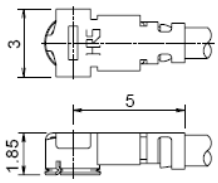
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 35: Specifications of Mated Plugs

The following figure describes the space factor of mated connector.

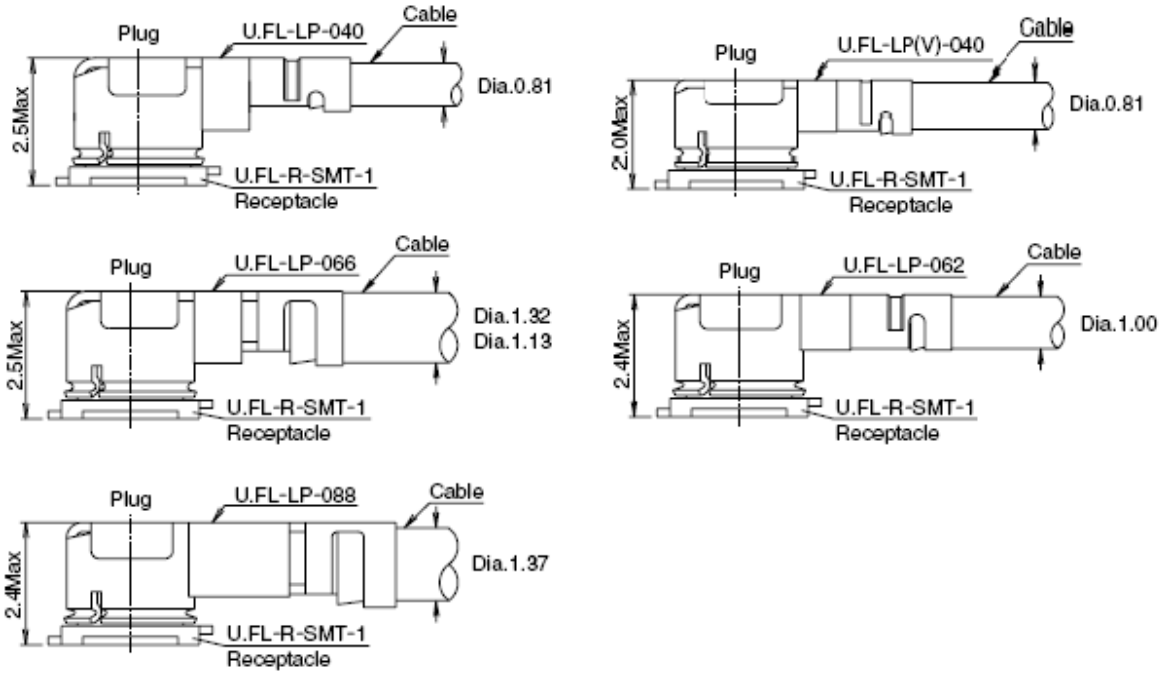


Figure 36: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://hirose.com.

6 Reliability, Radio, and Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 34: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.0	A
Peak Current of VBAT_RF	-	2.5	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT	V
Voltage at ADC1	0	VBAT	V

6.2. Power Supply Ratings

Table 35: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must be kept between the minimum	3.3	3.8	4.3	V

		and maximum values.				
	Voltage drop during transmitting burst	Maximum power control level at EGSM900	-	-	400	mV
I_{VBAT}	Peak supply current (during transmission slot)	Maximum power control level at EGSM900	-	1.7	2.5	A
USB_VBUS	USB connection detection	-	3.5	5.0	5.25	V

6.3. Power Consumption

Table 36: Current Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	34	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.4	mA
	AT+CFUN=0 (USB connected)	2.5	mA
	AT+CFUN=4 (USB disconnected)	1.5	mA
	AT+CFUN=4 (USB connected)	2.6	mA
	EGSM900 @ DRX = 2 (USB disconnected)	2.3	mA
	EGSM900 @ DRX = 5 (USB disconnected)	1.8	mA
	EGSM900 @ DRX = 5 (USB connected)	3.3	mA
	EGSM900 @ DRX = 9 (USB disconnected)	1.6	mA
	DCS1800 @ DRX = 2 (USB disconnected)	2.3	mA
	DCS1800 @ DRX = 5 (USB disconnected)	1.8	mA
	DCS1800 @ DRX = 5 (USB connected)	3.3	mA
	DCS1800 @ DRX = 9 (USB disconnected)	1.6	mA
	LTE-FDD @ PF = 32 (USB disconnected)	2.9	mA
	LTE-FDD @ PF = 64 (USB disconnected)	2.1	mA

	LTE-FDD @ PF = 64 (USB connected)	3.6	mA
	LTE-FDD @ PF = 128 (USB disconnected)	1.7	mA
	LTE-FDD @ PF = 256 (USB disconnected)	1.5	mA
	LTE-TDD @ PF = 32 (USB disconnected)	3.0	mA
	LTE-TDD @ PF = 64 (USB disconnected)	2.1	mA
	LTE-TDD @ PF = 64 (USB connected)	3.6	mA
	LTE-TDD @ PF = 128 (USB disconnected)	1.7	mA
	LTE-TDD @ PF = 256 (USB disconnected)	1.5	mA
Idle state	EGSM900 @ DRX = 5 (USB disconnected)	14.1	mA
	EGSM900 @ DRX = 5 (USB connected)	30	mA
	LTE-FDD @ PF = 64 (USB disconnected)	14.2	mA
	LTE-FDD @ PF = 64 (USB connected)	30.2	mA
	LTE-TDD @ PF = 64 (USB disconnected)	14.3	mA
	LTE-TDD @ PF = 64 (USB connected)	30.2	mA
LTE data transmission	LTE-FDD B1 @ 23.20 dBm	635	mA
	LTE-FDD B2 @ 22.24 dBm	604	mA
	LTE-FDD B3 @ 23.20 dBm	634	mA
	LTE-FDD B4 @ 22.80 dBm	694	mA
	LTE-FDD B5 @ 22.01 dBm	622	mA
	LTE-FDD B7 @ 22.62 dBm	919	mA
	LTE-FDD B8 @ 23.21 dBm	710	mA
	LTE-FDD B12 @ 24.13 dBm	656	mA
	LTE-FDD B13 @ 23.39 dBm	605	mA
	LTE-FDD B17 @ 23.53 dBm	649	mA
	LTE-FDD B18 @ 22.33 dBm	608	mA
	LTE-FDD B19 @ 22.05 dBm	596	mA

	LTE-FDD B20 @ 23.01 dBm	652	mA
	LTE-FDD B25 @ 22.62 dBm	624	mA
	LTE-FDD B26 @ 23.17 dBm	658	mA
	LTE-FDD B28 @ 23.43 dBm	666	mA
	LTE-FDD B66 @ 22.45 dBm	732	mA
	LTE-TDD B34 @ 22.91 dBm	274	mA
	LTE-TDD B38 @ 23.19 dBm	407	mA
	LTE-TDD B39 @ 23.41 dBm	255	mA
	LTE-TDD B40 @ 23.71 dBm	394	mA
	LTE-TDD B41 @ 23.71 dBm	384	mA
GPRS data transmission	GSM850 4DL/1UL @ 32.95 dBm	234	mA
	GSM850 3DL/2UL @ 30.94 dBm	338	mA
	GSM850 2DL/3UL @ 29.02 dBm	396	mA
	GSM850 1DL/4UL @ 27.03 dBm	417	mA
	EGSM900 4DL/1UL @ 32.27 dBm	230	mA
	EGSM900 3DL/2UL @ 31.01 dBm	378	mA
	EGSM900 2DL/3UL @ 29.20 dBm	447	mA
	EGSM900 1DL/4UL @ 27.41 dBm	488	mA
	DCS1800 4DL/1UL @ 30.95 dBm	189	mA
	DCS1800 3DL/2UL @ 28.76 dBm	272	mA
	DCS1800 2DL/3UL @ 26.64 dBm	310	mA
	DCS1800 1DL/4UL @ 24.35 dBm	322	mA
	PCS1900 4DL/1UL @ 30.17 dBm	168	mA
	PCS1900 3DL/2UL @ 28.08 dBm	238	mA
	PCS1900 2DL/3UL @ 26.13 dBm	276	mA
	PCS1900 1DL/4UL @ 24.10 dBm	288	mA

GSM voice call	GSM850 PCL = 5 @ 32.88 dBm	239	mA
	GSM850 PCL = 12 @ 18.87 dBm	90	mA
	GSM850 PCL = 19 @ 4.77 dBm	63	mA
	EGSM900 PCL = 5 @ 32.72 dBm	257	mA
	EGSM900 PCL = 12 @ 19.35 dBm	99	mA
	EGSM900 PCL = 19 @ 4.82 dBm	64	mA
	DCS1800 PCL = 0 @ 30.35 dBm	188	mA
	DCS1800 PCL = 7 @ 16.39 dBm	80	mA
	DCS1800 PCL = 15 @ 1.29 dBm	61	mA
	PCS1900 PCL = 0 @ 30.06 dBm	172	mA
	PCS1900 PCL = 7 @ 16.01 dBm	78	mA
	PCS1900 PCL = 15 @ 1.29 dBm	61	mA

6.4. Tx Power

Table 37: RF Output Power (Unit: dBm)

Parameters	Max. RF Output Power	Receiver Sensitivity
GSM850	33 dBm ±2 dB	NA
EGSM900	33 dBm ±2 dB	NA
DCS1800	30 dBm ±2 dB	NA
PCS1900	30 dBm ±2 dB	NA
LTE FDD	23 dBm ±2 dB	NA
LTE TDD	23 dBm ±2 dB	NA
BR	6 dBm	-89
EDR (8-DPSK)	6 dBm	-90

BLE	6 dBm	-89

6.5. Rx Sensitivity

Table 38: Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)	3GPP (SIMO)
	Primary	
GSM850	-108.6	-102.0
EGSM900	-108.4	-102.0
DCS1800	-108.1	-102.0
PCS1900	-108.3	-102.0
LTE-FDD B1 (10 MHz)	-98.2	-96.3
LTE-FDD B2 (10 MHz)	-98.9	-94.3
LTE-FDD B3 (10 MHz)	-99.0	-93.3
LTE-FDD B4 (10 MHz)	-98.2	-96.3
LTE-FDD B5 (10 MHz)	-99.3	-94.3
LTE-FDD B7 (10 MHz)	-96.3	-94.3
LTE-FDD B8 (10 MHz)	-99.2	-93.3
LTE-FDD B12 (10 MHz)	-98.0	-93.3
LTE-FDD B13 (10 MHz)	-99.1	-93.3
LTE-FDD B17 (10 MHz)	-97.5	-93.3
LTE-FDD B18 (10 MHz)	-99.0	-96.3
LTE-FDD B19 (10 MHz)	-99.5	-96.3
LTE-FDD B20 (10 MHz)	-98.9	-93.3
LTE-FDD B25 (10 MHz)	-98.3	-92.8

LTE-FDD B26 (10 MHz)	-98.9	-93.8
LTE-FDD B28 (10 MHz)	-99.4	-94.8
LTE-FDD B66 (10 MHz)	-98.1	-96.5
LTE-TDD B34 (10 MHz)	-99.0	-96.3
LTE-TDD B38 (10 MHz)	-99.0	-96.3
LTE-TDD B39 (10 MHz)	-99.7	-96.3
LTE-TDD B40 (10 MHz)	-99.2	-96.3
LTE-TDD B41 (10 MHz)	-98.6	-94.3

6.6. Digital I/O Characteristic

Table 39: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.26	2.0	V
V_{IL}	Input low voltage	-0.3	0.6	V
V_{OH}	Output high voltage	1.35	-	V
V_{OL}	Output low voltage	-	0.45	V

Table 40: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V
V_{IH}	Input high voltage	1.26		V
V_{IL}	Input low voltage	-	0.6	V
V_{OH}	Output high voltage	1.35	-	V
V_{OL}	Output low voltage	-	0.45	V

Table 41: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.05	V
V_{IH}	Input high voltage	1.95	-	V
V_{IL}	Input low voltage	-	1.0	V
V_{OH}	Output high voltage	2.55	-	V
V_{OL}	Output low voltage	-	0.45	V

6.7. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective component to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatics discharge characteristics of the module.

Table 42: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.8. Operating and Storage Temperatures

Table 43: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit

Operating Temperature Range [5]	-35	+25	+75	ºC
Extended Operation Range [6]	-40	+25	+85	ºC
Storage Temperature Range	-40	+25	+90	ºC

[5] Within operating temperature range, the module is 3GPP compliant.
[6] Within extended temperature range, the module remains the ability to establish and maintain a voice, SMS, data transmission, etc. There is no unrecoverable malfunction. There are also no effects on radio spectrum and no harm to radio network. Only one or more parameters like P_{out} might reduce in their value and exceed the specified tolerances. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

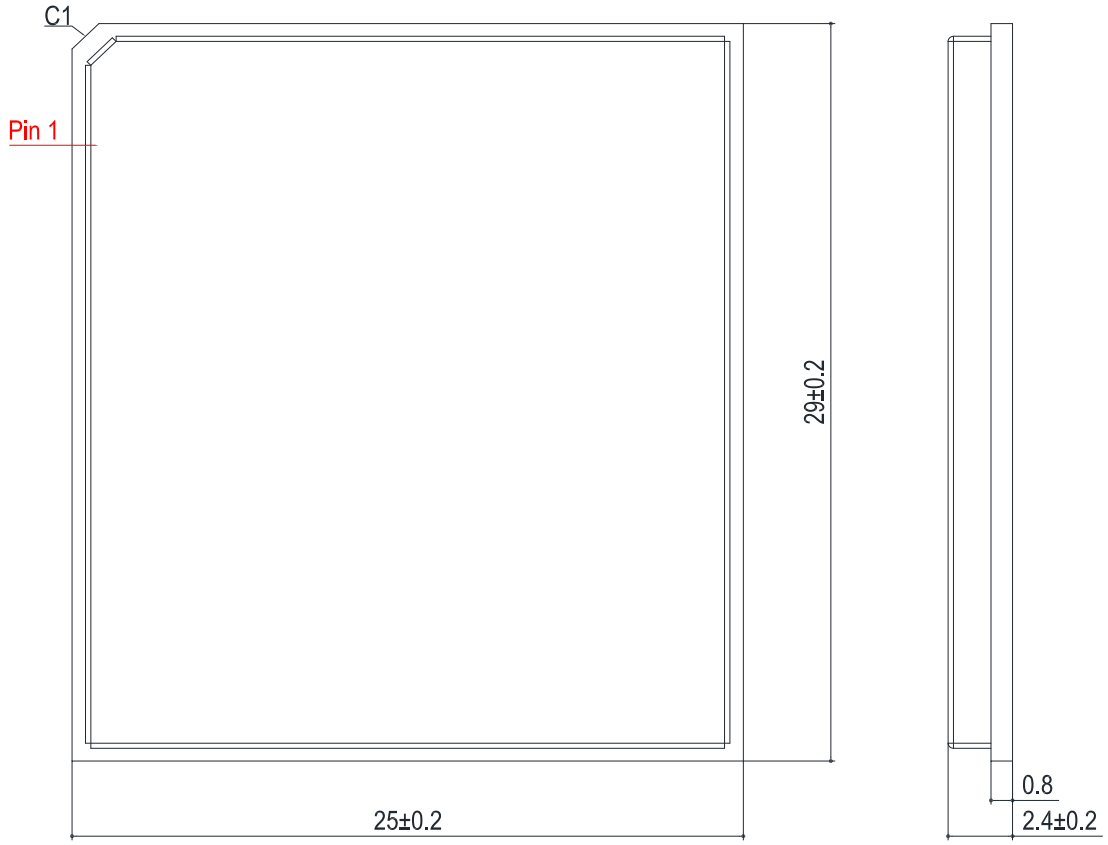


Figure 37: Module Top and Side Dimensions (Unit: mm)

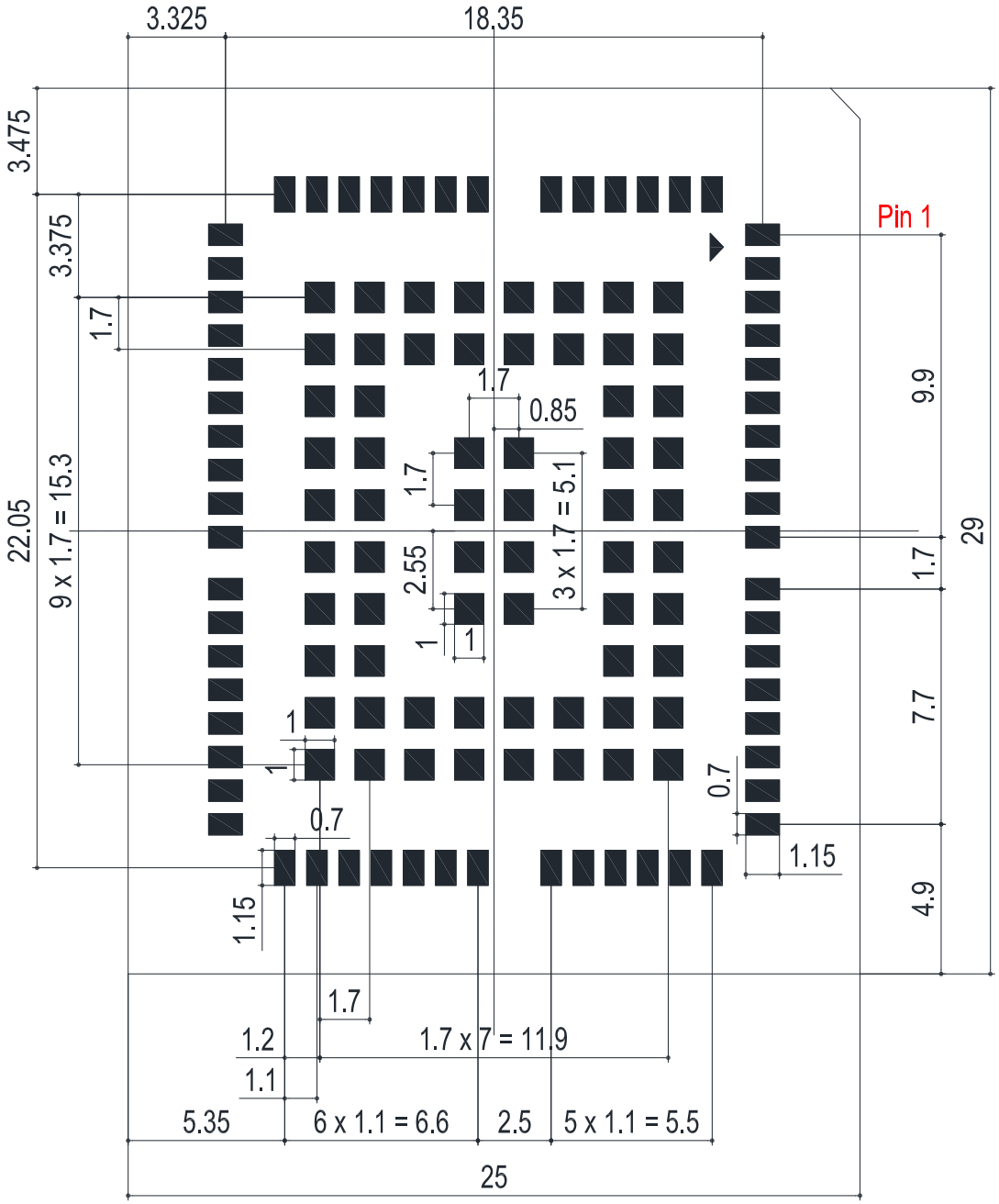


Figure 38: Bottom Dimension (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

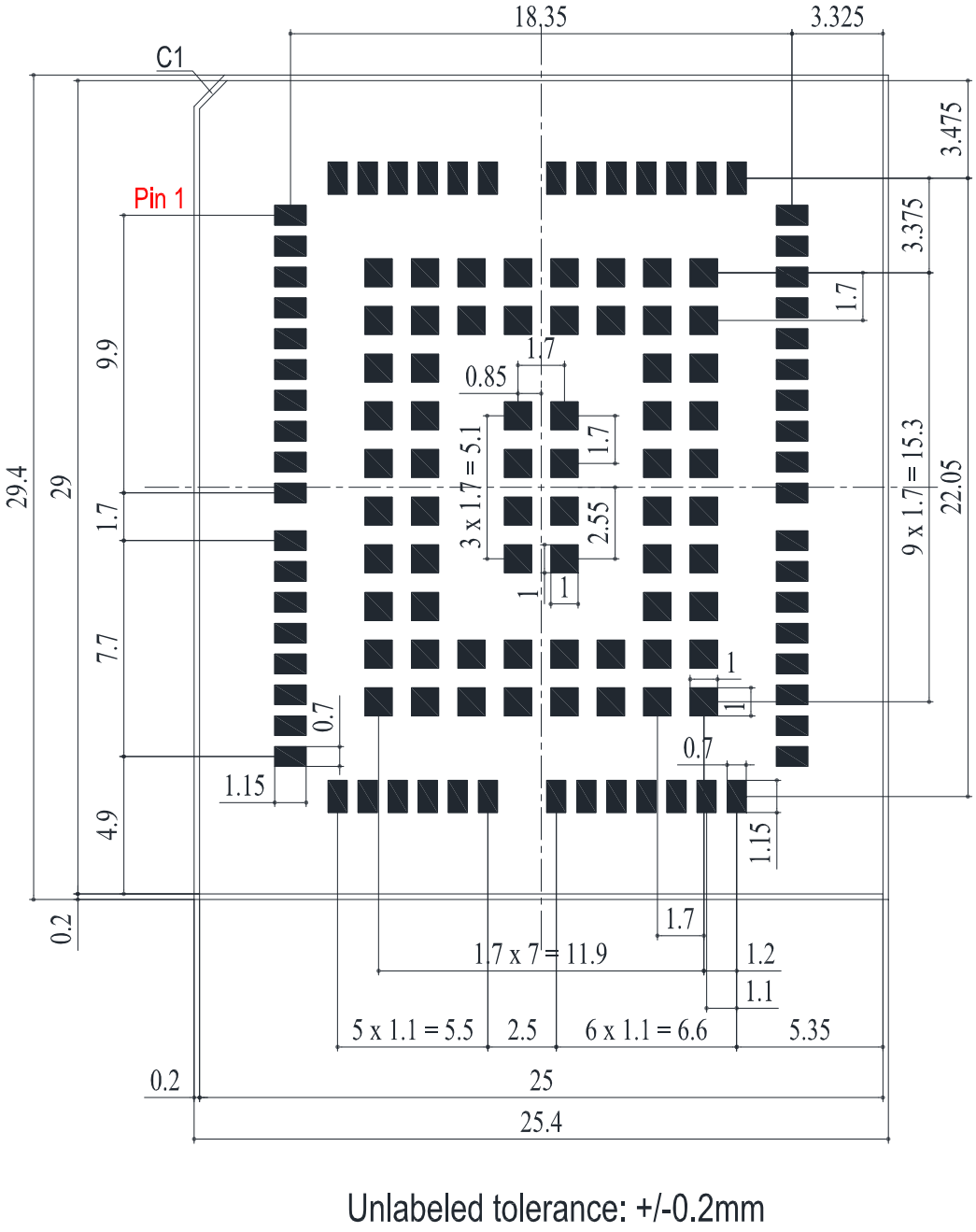


Figure 39: Recommended Footprint (Top View)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

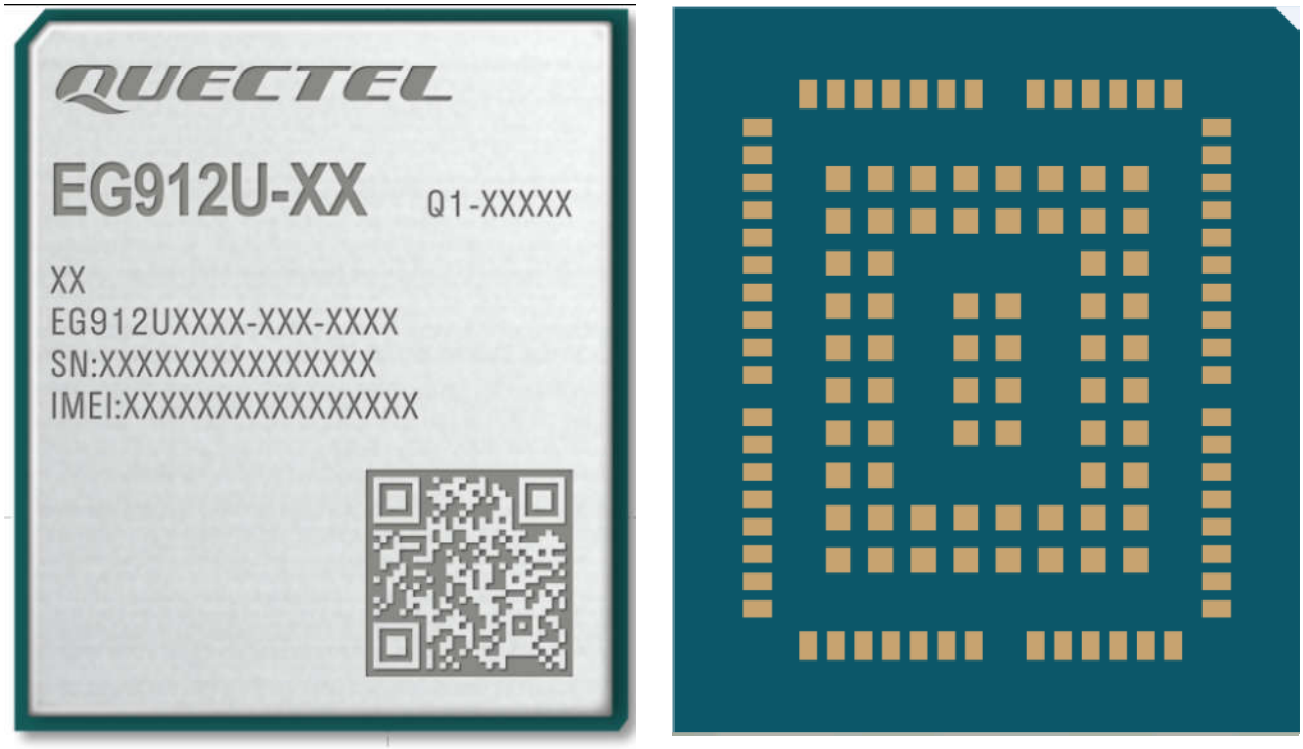


Figure 40: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing, and Packaging

8.1. Storage Conditions

Module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [7] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[7] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [4]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

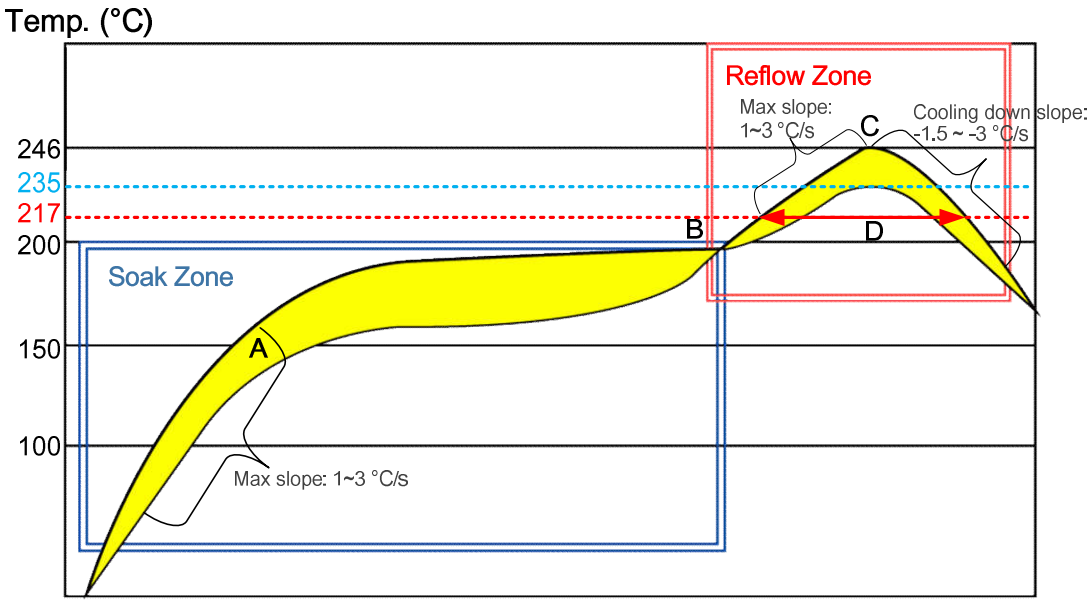


Figure 41: Recommended Reflow Soldering Thermal Profile

Table 44: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

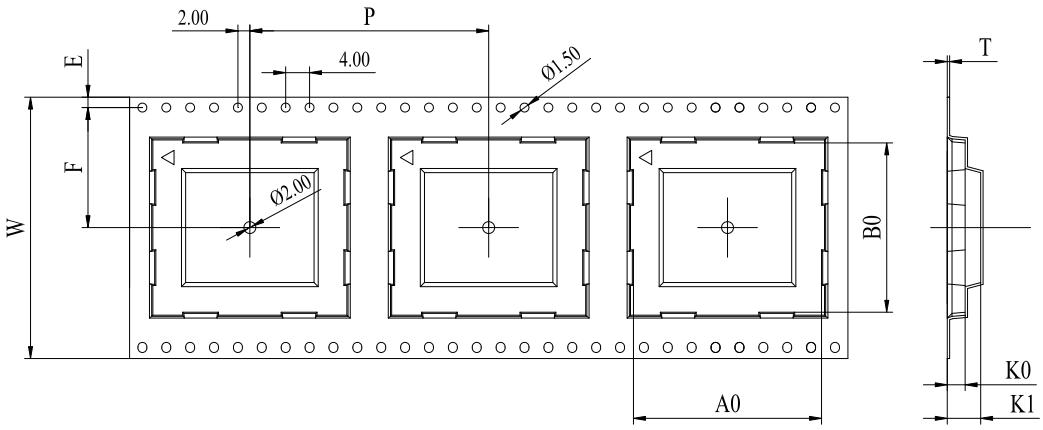


Figure 42: Carrier Tape Dimension Drawing

Table 45: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	25.5	29.5	3.2	5.8	20.2	1.75

8.3.2. Plastic Reel

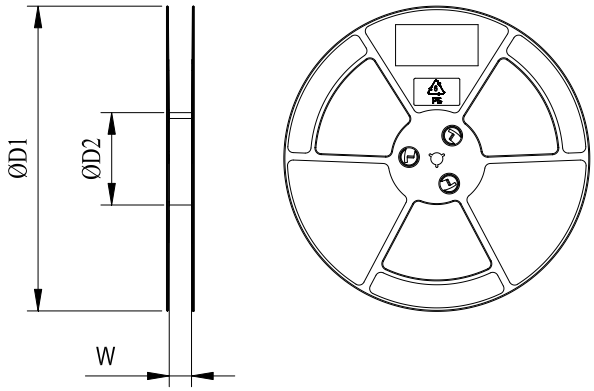
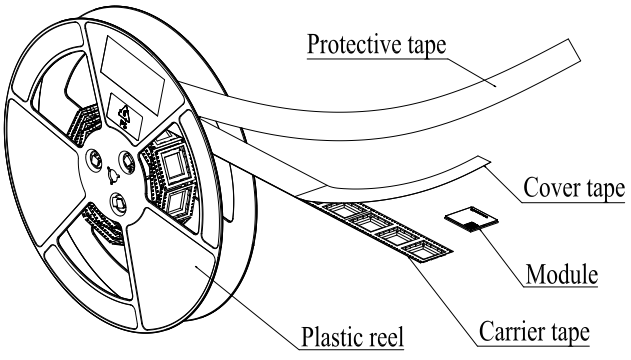


Figure 43: Plastic Reel Dimension Drawing

Table 46: Plastic Reel Dimension Table (Unit: mm)

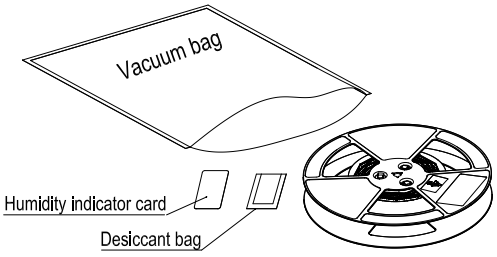
øD1	øD2	W
330	100	44.5

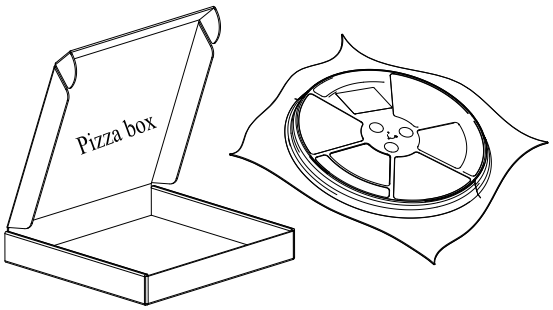
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 cartoon box and seal it. 1 cartoon box can pack 1000 modules.

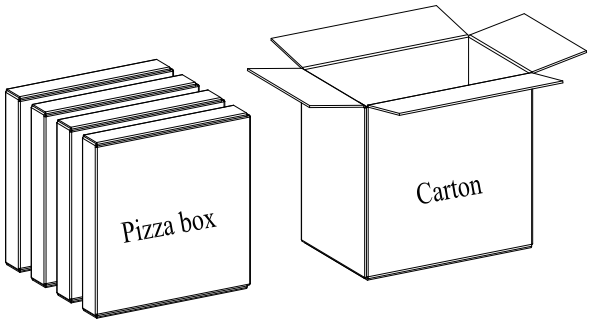


Figure 44: Packaging Process

9 Appendix References

Table 47: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC200U&EG912U-GL_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_SMT_User_Guide

Table 48: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AP	Application Processor
bps	Bits Per Second
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DCE	Data Communications Equipment
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception

DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HR	Half Rate
I/O	Input/Output
LB	Low Band
LGA	Land Grid Array
LTE	Long Term Evolution
MB	Middle Band
MCU	Microcontroller Unit
MT	Mobile Terminated
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
QAM	Quadrature Amplitude Modulation

QPSK	Quadrature Phase Shift Keying
RI	Ring Indicator
RF	Radio Frequency
Rx	Receive
SIMO	Single Input Multiple Output
SMS	Short Message Service
SPI	Serial Peripheral Interface
TDD	Time Division Duplexing
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage Value
Vnom	Nominal Voltage Value
Vmin	Minimum Voltage Value
$V_{IH}max$	Maximum High-level Input Voltage
$V_{IH}min$	Minimum High-level Input Voltage
$V_{IL}max$	Maximum Low-level Input Voltage
$V_{IL}min$	Minimum Low-level Input Voltage
$V_{I}max$	Absolute Maximum Input Voltage
$V_{I}min$	Absolute Minimum Input Voltage

$V_{OH}max$	Maximum High-level Output Voltage
$V_{OH}min$	Minimum High-level Output Voltage
$V_{OL}max$	Maximum Low-level Output Voltage
$V_{OL}min$	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio

Hereby, [Quectel Wireless Solutions Co., Ltd.] declares that the radio equipment type [EG912U-GL] is in compliance with Directive 2014/53/EU. The full text of the EU declaration of conformity is available at the following internet address: http://www.quectel.com/support/technical.htm

The device could be used with a separation distance of 20cm to the human body.

FCC

OEM/Integrators Installation Manual

Important Notice to OEM integrators

1. This module is limited to OEM installation ONLY.
2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b).
3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations
4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part
15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s).
The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application.

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the

final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR2023EG912UGL2”
The FCC ID can be used only when all FCC compliance requirements are met.

Antenna Installation

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.
(3) Only antennas of the same type and with equal or less gains as shown below may be used with this module. Other types of antennas and/or higher gain antennas may require additional authorization for operation.

Antenna type	GSM Peak Gain (dBi)	LTE Peak Gain (dBi)	Bluetooth Peak Gain (dBi)
Dipole for WWAN Folded Dipole for BT	GSM850: 2.53 GSM1900: 1.59	B2: 1.59 B4: 2.00 B5: 2.53 B7: 3.00 B12: 3.95 B13: 4.45 B17: 3.95 B25: 1.59 B26: 2.53 B38: 3.00 B41: 3.00 B66: 2.00	BT: 0.47

Note: Bluetooth only for FCC ID: XMR2023EG912UGL

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC/IC authorization is no longer considered valid and the FCC ID/IC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC/IC authorization.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant

to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27, part 90, 15.247 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.
As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.