BG770A-GL&BG773A-GL
Hardware Design

LPWA Module Series

Version: 1.2.1

Date: 2022-06-10

Status: Preliminary

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-01-28	Lex LI/ Ben JIANG	Creation of the document
1.0	2021-11-03	Arvin WU/ Ben JIANG	First official release
1.1	2022-02-16	Arvin WU/ Ben JIANG	1. Reserved pins 2, 3, 34 & 35 (previously for PCM) and pins 5 & 37 (previously for I2C), therefore deleted all information involving voice/VoLTE functionality throughout the document. Added the description of wake-up the module from PSM by driving PWRKEY low (Chapter 3.4.2). 2. Added the figure of power supply limits during burst transmission (Figure 4). 3. Added the method of waking up the module from PSM through driving PWRKEY low (Chapter 3.4.2). 4. Updated the minimum power supply current to 0.8 A (Chapter 3.5.2). 5. Updated the power-up timing and added the restart timing (Chapter 3.6.1). 6. Updated the power-down timing (Chapter 3.6.2). 7. Updated the truth table of GRFC interfaces (Table 24). 8. Updated the data of power consumption (Table 34). 9. Updated the recommended maximum slope parameter for reflow zone (Chapter 8.2).
1.2.0	2022-05-16	Lex LI/ Ben JIANG	Preliminary: 1. Added the sub-model of BG773A-GL. 2. Updated the max. UL and DL rate of 3GPP Rel-13 Cat M1 and Cat NB1 and 3GPP Rel-14 Cat M1 and Cat NB2 (Chapter 2.2). 3. Added the XTRA enabled data in the state of cold start, warm start and hot start @ open sky (Table 25).

1.2.1	2022-06-10	Lex LI/ Ben JIANG	Preliminary: Added the note description about USB interface, MAIN_RI and AP_READY.

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1 Introduction

This document defines BG770A-GL and BG773A-GL modules and describes their air interface and hardware interfaces which connect to your applications.

This document helps you quickly understand the interface specifications, electrical and mechanical details, as well as other related information of the module. To facilitate application designs, it also includes some reference designs for your reference. The document, coupled with application notes and user guides, makes it easy to design and to set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

2.1. Frequency Bands and Functions

BG770A-GL/BG773A-GL module is an embedded IoT (LTE Cat M1, LTE Cat NB1/Cat NB2) wireless communication module. It provides data connectivity on LTE-FDD network, and supports half-duplex operation in LTE network. It also provides GNSS functionality to meet your specific application demands.

BG770A-GL/BG773A-GL module is based on an architecture in which WWAN (LTE) and GNSS Rx chains share certain hardware blocks. However, the module does not support concurrent operation of WWAN and GNSS. The solution adopted in the module is a form of coarse time-division multiplexing (TDM) between WWAN and GNSS Rx chains. Given the relaxed latency requirements of most LPWA applications, time-division sharing of resources can be made largely transparent to applications. For more details, see ***document [1]***.

BG770A-GL/BG773A-GL is an industrial grade module for industrial and commercial applications only.

Table 2: Frequency Bands and GNSS Types of BG770A-GL & BG773A-GL Modules

Module	Supported Bands	Power Class	GNSS
BG770A-GL/ BG773A-GL	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/ B25/B26/B27/B28/B66 **Cat NB1/NB2** [1]**:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/ B20/B25/B28/B66	Power Class 3 (23 dBm ± 2.7 dB)	GPS, GLONASS

With a compact profile of 14.9 mm × 12.9 mm × 1.9 mm, BG770A-GL/BG773A-GL can meet almost all requirements for M2M applications such as smart metering, tracking system, security, wireless POS, etc. It is especially suitable for size and weight sensitive applications such as smart watch and other wearable devices.

[1] LTE Cat NB2 is backward compatible with LTE Cat NB1.

BG770A-GL/BG773A-GL is an SMD type module which can be embedded into applications through its 94 LGA pins. It supports internet service protocols like TCP, UDP and PPP. Extended AT commands have been developed for you to use these internet service protocols easily.

2.2. Key Features

Table 3: Key Features of BG770A-GL & BG773A-GL Modules

Features	Details
Power Supply [2]	● VBAT_BB: 2.2–4.35 V, typ. 3.3 V ● VBAT_RF: 3.1–4.2 V, typ. 3.3 V
Transmitting Power	Class 3 (23 dBm ± 2.7 dB) for LTE HD-FDD bands
LTE Features	● Supports 3GPP Rel-13 (LTE Cat M1/Cat NB1) and 3GPP Rel-14 (LTE Cat NB1/Cat NB2) ● Supports 1.4 MHz RF bandwidth for LTE Cat M1 ● Supports 200 kHz RF bandwidth for LTE Cat NB1/Cat NB2 **Rel-13:** ● Cat M1: Max. 300 kbps (DL)/375 kbps (UL) ● Cat NB1: 27.2 kbps (DL)/62.5 kbps (UL) **Rel-14:** ● Cat M1: Max. 588 kbps (DL)/1119 kbps (UL) ● Cat NB2: Max. 127 kbps (DL)/158 kbps (UL)
Internet Protocol Features	● Supports PPP/TCP/UDP/SSL/DTLS/FTP(S)/HTTP(S)/NITZ/PING/NIDD/MQTT/NTP/LwM2M/CoAP protocols ● Supports PAP and CHAP for PPP connections
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USIM Interface	Supports 1.8 V external USIM/eSIM card only
USB Interface* [3]	● Complies with USB 2.0 specification ● Supports full speed mode only
UART Interfaces	**Main UART:** ● Used for data transmission and AT command communication ● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit)

[2] When the module starts up normally, in order to ensure full function mode, the minimum power supply voltage should be higher than 3.1 V.
[3] USB interface is under developed on BG773A-GL, while it can be used on BG770A-GL.

	● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for firmware upgrade, software debugging, log output and NMEA sentences output. ● 115200 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **Auxiliary UART:** ● Used for RF calibration and log output ● 921600 bps baud rate by default ● The default frame format is 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control
GNSS	GPS, GLONASS
AT Commands	● *3GPP TS 27.007* and *3GPP TS 27.005* AT commands ● Quectel enhanced AT commands
Network Status Indication	One NET_STATUS pin for network connectivity status indication
Antenna Interfaces	● Main antenna interface (ANT_MAIN) ● GNSS antenna interface (ANT_GNSS)
Physical Characteristics	● Dimensions: (14.9 ±0.2) mm × (12.9 ±0.2) mm × (1.9 ±0.2) mm ● Package: LGA ● Weight: approx. 0.8 g
Temperature Range	● Operating temperature range: -35 °C to +75 °C [4] ● Extended temperature range: -40 °C to +85 °C [5] ● Storage temperature range: -40 °C to +90 °C
Firmware Upgrade	● Debug UART interface ● DFOTA ● USB* [3]
RoHS	All hardware components are fully compliant with EU RoHS directive

[4] Within the operating temperature range, the module meets 3GPP specifications.
[5] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The following figure shows a block diagram of BG770A-GL & BG773A-GL and illustrates the major functional parts.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

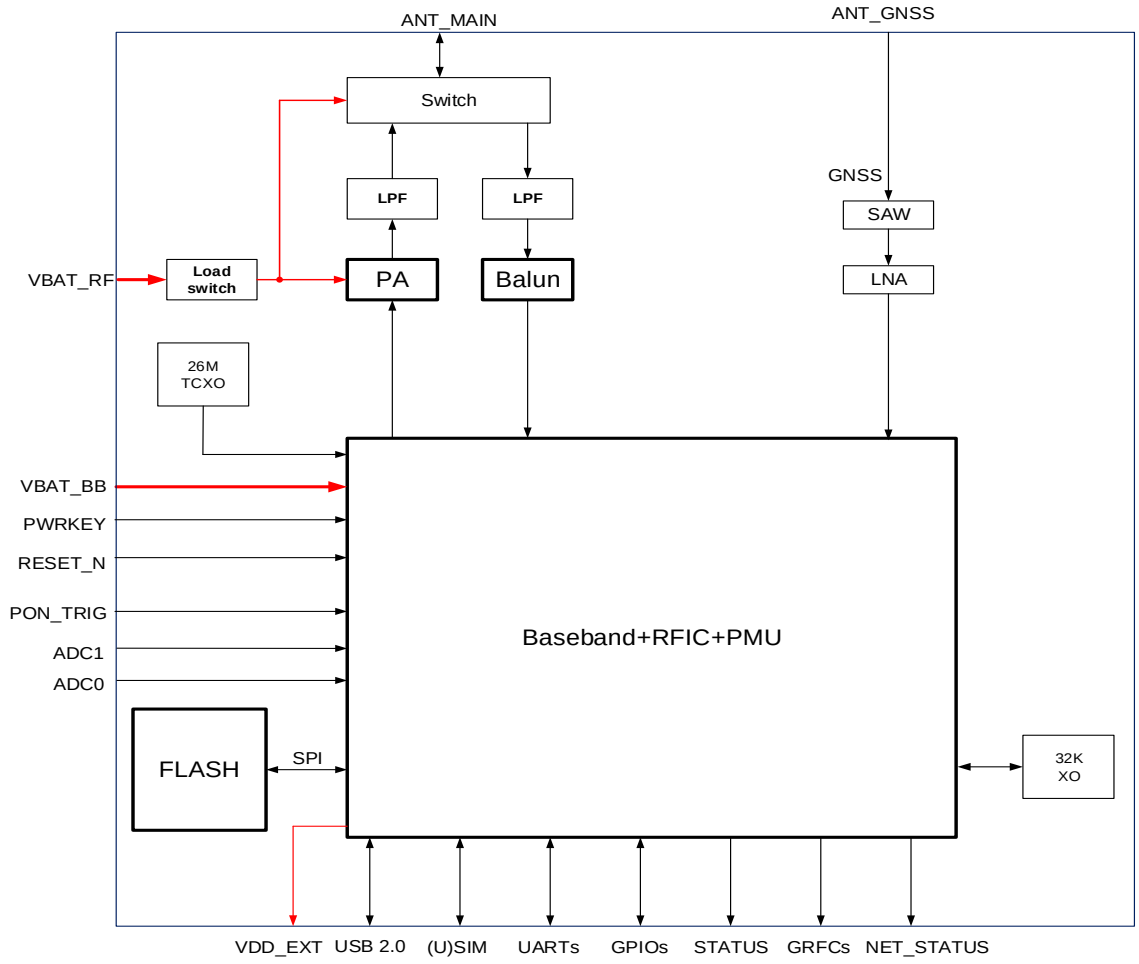


Figure 1: Functional Diagram of BG770A-GL

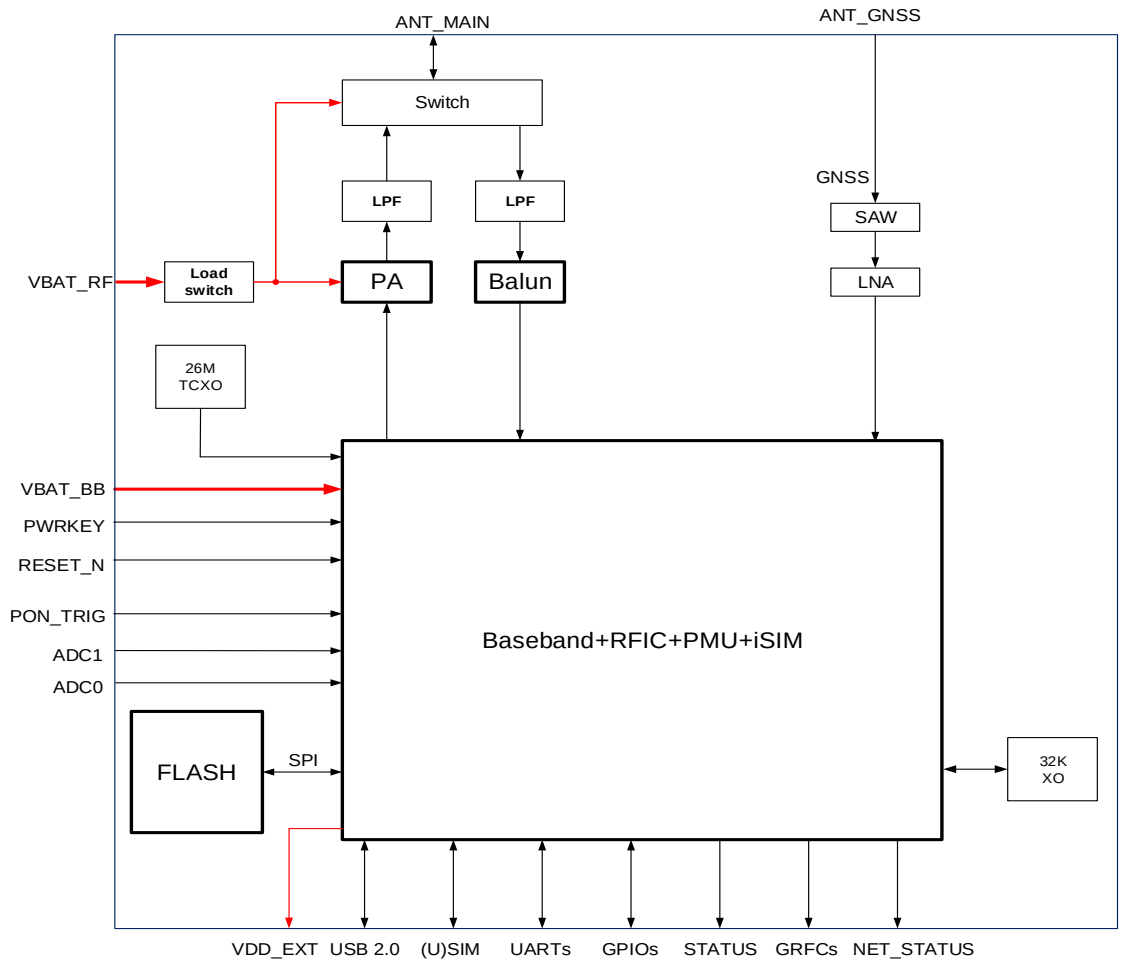


Figure 2: Functional Diagram of BG773A-GL

2.4. EVB Kit

To facilitate application development with BG770A-GL and BG773A-GL conveniently, Quectel supplies the evaluation board (UMTS&LTE EVB), USB to RS-232 converter cable, USB data cable, earphone, antennas and other peripherals to control or test the module. For more details, see ***document [2]***.

3 Application Interfaces

BG770A-GL and BG773A-GL is equipped with 94 LGA pins for connection to cellular application platforms. The subsequent chapters provide detailed description of interfaces listed below:

- Power supply
- PON_TRIG
- USIM interface
- USB interface*
- UART interfaces
- Indication signals
- ADC interfaces
- GPIO interfaces
- GRFC interfaces

NOTE

USB interface is under developed on BG773A-GL, while it can be used on BG770A-GL.

3.1. Pin Assignment

The following figure shows the pin assignment of BG770A-GL and BG773A-GL.

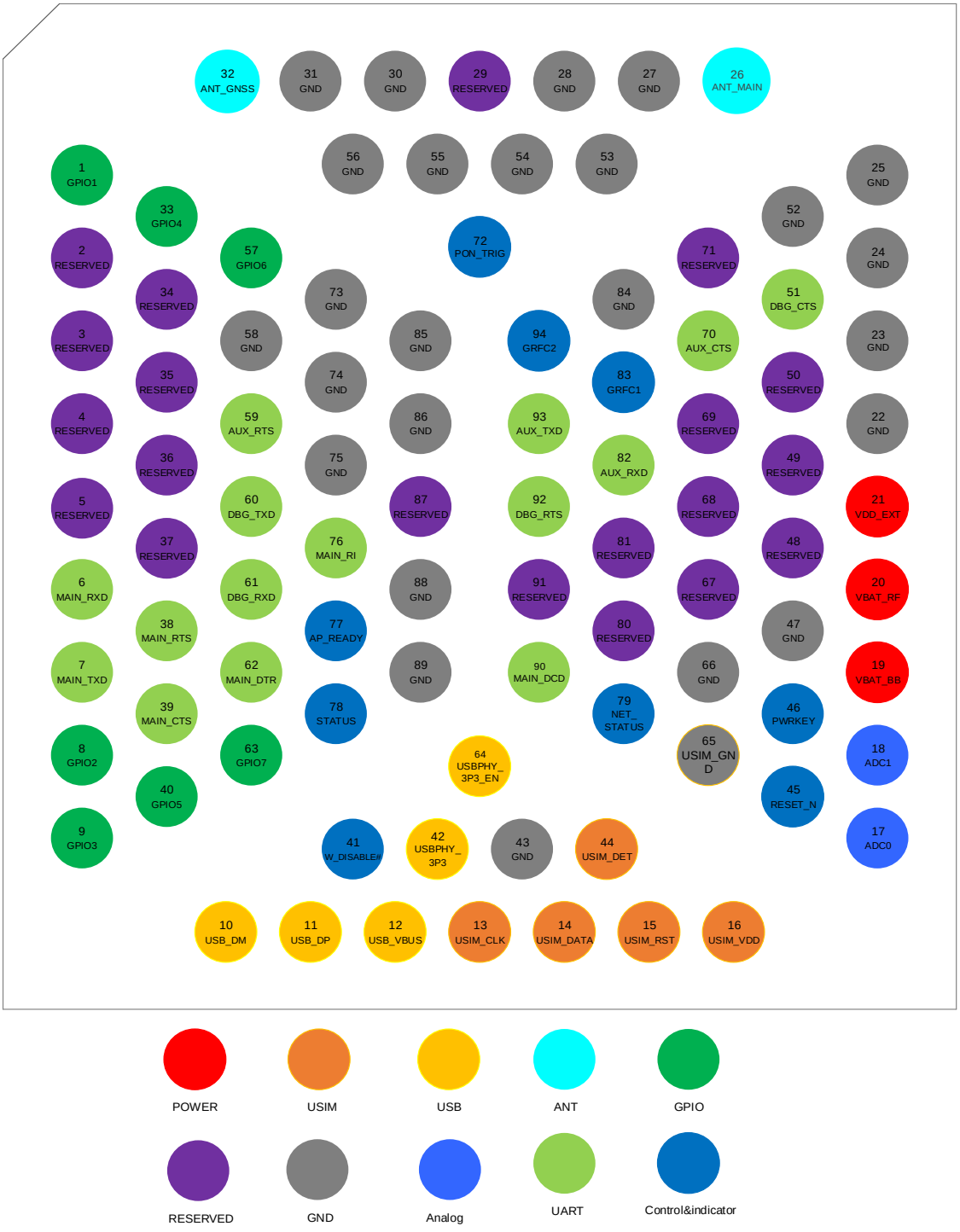


Figure 3: Pin Assignment (Top View)

NOTE

1. ADC input voltage must not exceed 1.8 V.
2. The input voltage range of USB_VBUS is 1.19–2.0 V.
3. Keep all RESERVED pins and unused pins unconnected.
4. Connect GND pins to ground in the design.

3.2. Pin Description

The following tables show the pin definition of BG770A-GL and BG773A-GL.

Table 4: Definition of I/O Parameters

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	19	PI	Power supply for the module's baseband part	Vmax = 4.35 V Vmin = 2.2 V Vnom = 3.3 V	See NOTE 1.
VBAT_RF	20	PI	Power supply for the module's RF part	Vmax = 4.2 V Vmin = 3.1 V Vnom = 3.3 V	See NOTE 1.

VDD_EXT	21	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	If this pin is unused, keep it open.
GND	22–25, 27, 28, 30, 31, 43, 47, 52–56, 58, 66, 73–75, 84–86, 88, 89				
Turn on/off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	46	DI	Turn on/off the module	V_{IL}max = 0.3 V V_{IH}min = 1.0 V	Internally pulled up with a 470 kΩ resistor.
Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	45	DI	Reset the module	V_{IL}max = 0.3 V V_{IH}min = 1.3 V	Internally pulled up with a 470 kΩ resistor.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	78	DO	Indicate the module's operation status	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain. If these pins are unused, keep them open.
NET_STATUS	79	DO	Indicate the module's network activity status		
USB Interface* [6]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	12	AI	USB connection detect	V_{IH}max = 2.0 V V_{IH}min = 1.19 V	1.8 V power domain.
USB_DP	11	AIO	USB differential data (+)	Vmax = 4.1 V Vmin = -0.2 V	Compliant with USB 2.0 standard specification. Require differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)		
USBPHY_3P3	42	PI	Power supply for USB PHY circuit	Vmax = 3.6 V Vnom = 3.3 V Vmin = -0.2 V	
USBPHY_3P3_EN	64	DO	External LDO enable control for USB	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain.

[6] USB interface is under developed on BG773A-GL, while it can be used on BG770A-GL.

USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DET	44	DI	USIM card hot-plug detect	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If this pin is unused, keep it open.
USIM_VDD	16	PO	USIM card power supply	Vmax = 1.9 V Vmin = 1.7 V	Supports 1.8 V USIM card only.
USIM_RST	15	DO	USIM card reset	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain.
USIM_DATA	14	DIO	USIM card data	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain.
USIM_CLK	13	DO	USIM card clock	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain.
USIM_GND	65		Specified ground for USIM card		
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	62	DI	Main UART data terminal ready	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If these pins are unused, keep them open.
MAIN_RXD	6	DI	Main UART receive		
MAIN_TXD	7	DO	Main UART transmit		
MAIN_CTS	39	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
MAIN_RTS	38	DI	DTE request to send signal from DCE (Connects to DTE's RTS)	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_DCD	90	DO	Main UART data carrier detect	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	

MAIN_RI* [7]	76	DO	Main UART ring indication		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	61	DI	Debug UART receive	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. It is recommended to reserve test points for these four pins.
DBG_TXD	60	DO	Debug UART transmit	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
DBG_CTS	51	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)		
DBG_RTS	92	DI	DTE request to send signal from DCE (Connects to DTE's RTS)	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Auxiliary UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
AUX_TXD	93	DO	Auxiliary UART transmit	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain. If these pins are unused, keep them open.
AUX_RXD	82	DI	Auxiliary UART receive	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
AUX_CTS	70	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
AUX_RTS	59	DI	DTE request to send signal from DCE (Connects to DTE's RTS)	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

[7] MAIN_RI is under developed on BG773A-GL, while it can be used on BG770A-GL.

ANT_MAIN	26	AIO	Main antenna interface		50 Ω impedance.
ANT_GNSS	32	AI	GNSS antenna interface		50 Ω impedance. If this pin is unused, keep it open.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	1	DIO	General-purpose input/output	V_{OL}max = 0.36 V V_{OH}min = 1.44 V V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If these pins are unused, keep them open.
GPIO2	8	DIO			
GPIO3	9	DIO			
GPIO4	33	DIO			
GPIO5	40	DIO			
GPIO6	57	DIO			
GPIO7	63	DIO			
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	17	AI	General-purpose ADC interface	Voltage range: 0–1.8 V	If these pins are unused, keep them open.
ADC1	18	AI	General-purpose ADC interface	Voltage range: 0–1.8 V	
Other Interface Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	41	DI	Airplane mode control	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. When this pin is at low level, the module enters airplane mode. If this pin is unused, keep it open.
AP_READY* [8]	77	DI	Application processor ready	V_{IL}min = -0.2 V V_{IL}max = 0.54 V	1.8 V power domain. If this pin is unused,

[8] AP_READY is under developed on BG773A-GL, while it can be used on BG770A-GL.

				V_{IH}min = 1.26 V V_{IH}max = 2.0 V	keep it open.
PON_TRIG	72	DI	Used for main UART function control and for entering/exiting e-I-DRX, PSM, sleep and power off modes	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. No internal pull up/down resistors by default.
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	83	DO	Generic RF controller	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain. If these pins are unused, keep them open.
GRFC2	94	DO	Generic RF controller		
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	2–5, 29, 34–37, 48–50, 67–69, 71, 80, 81, 87, 91				Keep these pins open.

NOTE

1. When the module starts up normally, in order to ensure full function mode, the minimum power supply voltage should be higher than 3.1 V. For every VBAT transition/re-insertion from 0 V, VBAT slew rate is less than 25 mV/μs. In order to ensure that the module can start normally, pull down PWRKEY to turn on the module after VBAT remains stable for at least 100 ms.
2. The input voltage range of USB_VBUS is 1.19–2.0 V.
3. USBPHY_3P3 and USBPHY_3P3_EN pins are used for USB PHY circuits.
4. ADC input voltage must not exceed 1.8 V.
5. Keep all RESERVED pins and unused pins unconnected.

3.3. Operating Modes

The table below briefly summarizes the various operating modes of BG770A-GL/BG773A-GL.

Table 6: Overview of Operating Modes

Mode	Details	
Normal Operation	Connected	The module is connected to network. Its power consumption varies with the network setting and data transfer rate.
	Idle	The module remains registered on network, and is ready to send and receive data. In this mode, the software is active.
Extended Idle Mode DRX (e-I-DRX)	The module and the network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module into airplane mode where the RF function is invalid.	
Minimum Functionality Mode	**AT+CFUN=0** can set the module into a minimum functionality mode without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Sleep Mode	The module retains the ability to receive paging message, SMS and TCP/UDP data from the network normally. In this mode, the current consumption is reduced to a low level.	
Power OFF Mode	The module's power supply is shut down by its power management unit. In this mode, the software is inactive, the serial interfaces are inaccessible, while the operating voltage (connected to VBAT_BB and VBAT_RF) remains applied.	
Power Saving Mode (PSM)	PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. The current consumption is reduced to a minimized level.	
Recovery Mode	The module can burn firmware with an empty serial flash, or recover from firmware malfunction. For more details, see ***Chapter 3.4.5***.	

NOTE

During e-I-DRX, it is recommended to use main UART interface for data communication, as the use of USB interface* will increase power consumption.

3.4. Power Saving

3.4.1. Airplane Mode

When BG770A-GL/BG773A-GL module enters airplane mode, the RF function will be disabled, and all AT commands correlative with RF function will be inaccessible. This mode can be set as follows:

Hardware:

W_DISABLE# is pulled up by default. Driving it low will let the module enter airplane mode.

Software:

AT+CFUN=<fun> provides choice of the functionality level, through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).
- **AT+CFUN=4**: Airplane mode. RF function is disabled.

NOTE

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled with **AT+QCFG="airplanecontrol"**. For details of the command, see ***document [3]***.
2. The execution of **AT+CFUN=<fun>** may affect GNSS function. Since the module does not support concurrent operation of WWAN and GNSS, the GNSS function can be used when **<fun>**=0 or 4, but cannot be used when **<fun>**=1.

3.4.2. Power Saving Mode (PSM)

BG770A-GL/BG773A-GL module minimizes its power consumption by entering PSM. The mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. Therefore, in PSM the module cannot immediately respond to user requests.

When the module wants to use PSM, it shall request an Active Time value during every Attach and TAU procedures. If the network supports PSM use, it will it will allocate an Active Time value to the module to confirm PSM use. If the module wants to change the Active Time value, the module consequently requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via **AT+QPSMS**. In this case, driving PON_TRIG low will set the module to PSM.

Any of the following methods can wake up the module from PSM:

- Drive PON_TRIG high and keeping it high, will wake up the module from PSM.
- When the TAU timer expires, the module wakes up from PSM automatically. In this case, the main UART interface is inaccessible until PON_TRIG is pulled up.
- Driving PWRKEY low to wake up the module from PSM. In this case, the main UART interface is inaccessible until PON_TRIG is pulled up.

NOTE

1. PON_TRIG is not pulled up/down internally by default.
2. PON_TRIG must be pulled up after executing any PSM wake-up event, otherwise the main UART will be inaccessible. In any case, the main UART interface is inaccessible until PON_TRIG is pulled up.
3. See ***document [4]*** for details about **AT+QPSMS**.

3.4.3. Extended Idle Mode DRX (e-I-DRX)

The module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transfers, and in particular, they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what were requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

If e-I-DRX is supported by the network, perform the steps below in sequence to let the module enter e-I-DRX mode, in which case the main UART interface is inaccessible.

1. Send **AT+QPSMS=0** to disable PSM mode.
2. Send **AT+CEDRXS=1** to enable e-I-DRX mode.
3. Send **AT+QSCLK=2** to enable sleep mode.
4. Drive MAIN_DTR high.
5. Drive PON_TRIG low.

NOTE

1. See ***document [4]*** for details about the above AT commands.
2. Follow the steps for exiting sleep mode to exit e-I-DRX.

3.4.4. Sleep Mode

BG770A-GL and BG773A-GL can reduce its power consumption to a lower value during the sleep mode. The following sub-chapters describe the power saving procedure.

3.4.4.1. UART Application Scenario

If the host communicates with the module via the main UART interface, perform the steps below in sequence to make the module enter sleep mode, in which case the main UART interface is not accessible.

1. Send **AT+CFUN=0** to set the module to minimum function mode. [9]
2. Drive MAIN_DTR low.
3. Execute **AT+QSCLK=2** to enable sleep mode.
4. Drive MAIN_DTR high.
5. Drive PON_TRIG low.

When the module is in sleep mode, perform the steps below in sequence to let the module exit sleep mode.

1. Drive PON_TRIG high.
2. Drive MAIN_DTR low.
3. Execute **AT+QSCLK=0** to disable sleep mode.
4. Send **AT+CFUN=1** to set the module into full function mode. [9]
5. Drive MAIN_DTR high.

The following figure shows the connection between the module and the host.

[9] After setting the module to minimum functionality with **AT+CFUN=0**, you can test the lowest power consumption of the module after the module enters sleep mode. If you need to keep the RF function on after the module enters sleep mode, there is no need to send any **AT+CFUN** command.

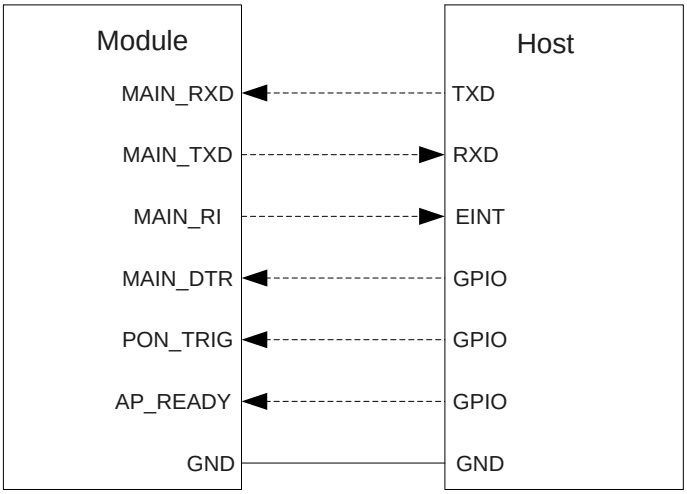


Figure 4: Sleep Mode Application via UART Interface

- When the module has a URC to report, MAIN_RI* will wake up the host. See ***Chapter 3.12.3*** for details about MAIN_RI* behavior.
- After the module is turned on, MAIN_DTR is internally pulled up by default.
- AP_READY* will detect the sleep state of the host (it can be configured to detect high or low voltage level). See **AT+QCFG="apready"** in ***document [3]*** for details.

3.4.5. Recovery Mode

BG770A-GL/BG773A-GL provides the recovery mode for firmware upgrade in emergency cases. Recovery mode can force the baseband chip of the module to upgrade firmware via debug UART interface.

The following preconditions can set the module to recovery mode.

1. Short-circuit DBG_TXD and DBG_RXD pins.
2. Drive PWRKEY low to turn on the module. In this case the module will enter recovery mode.
3. After the module enters recovery mode, disconnect the connection between DBG_TXD and DBG_RXD.
4. Upgrade firmware via debug UART interface.

NOTE

1. In the design, it is recommended to reserve all the test points of the debug UART interface, and keep DBG_TXD close to DBG_RXD.
2. Ensure that VBAT remains stable for at least 100 ms before pulling down PWRKEY.

3.5. Power Supply

3.5.1. Power Supply Pins

BG770A-GL/BG773A-GL provides two VBAT pins for connection with an external power supply.

The following table shows the details of VBAT_BB and VBAT_RF pins and ground pins.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_BB	19	Power supply for the module's baseband part	2.2	3.3	4.35	V
VBAT_RF	20	Power supply for the module's RF part	3.1	3.3	4.2	V
GND	22–25, 27, 28, 30, 31, 47, 52–56, 58, 66, 73–75, 84–86, 88, 89		-	-	-	-

NOTE

When the module starts up normally, in order to ensure full function mode, the minimum power supply voltage should be higher than 3.1 V. For every VBAT transition/re-insertion from 0 V, VBAT slew rate is less than 25 mV/μs. In order to ensure that the module can start normally, pull down PWRKEY to turn on the module after VBAT remains stable for at least 100 ms.

3.5.2. Voltage Stability Requirements

The power supply range of VBAT_BB is 2.2–4.35 V, and that of VBAT_RF is 3.1–4.2 V. When the module starts up normally, to ensure normal operation mode, the minimum power supply voltage should be higher than 3.1 V.

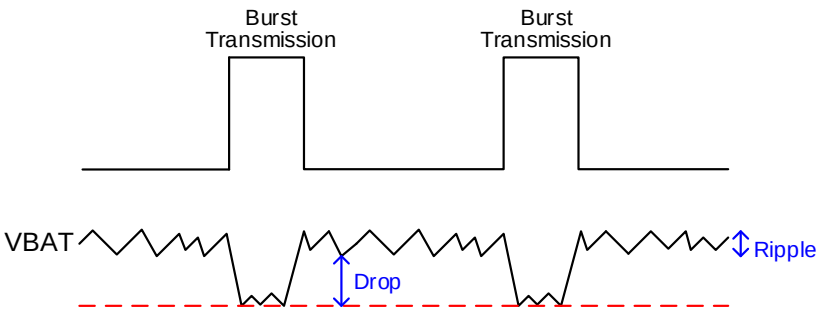


Figure 5: Power Supply Limits During Burst Transmission

To decrease voltage drop, a bypass capacitor of about 100 µF with low ESR should be used, and a multi-layer ceramic chip capacitor (MLCC) array should also be reserved due to its low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) for composing the MLCC array, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT trace should be no less than 1 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to ensure power supply stability, it is suggested to use two TVS components with low leakage current and suitable reverse stand-off voltage, and also it is recommended to place them as close to the VBAT pins as possible. The following figure shows the star structure of the power supply.

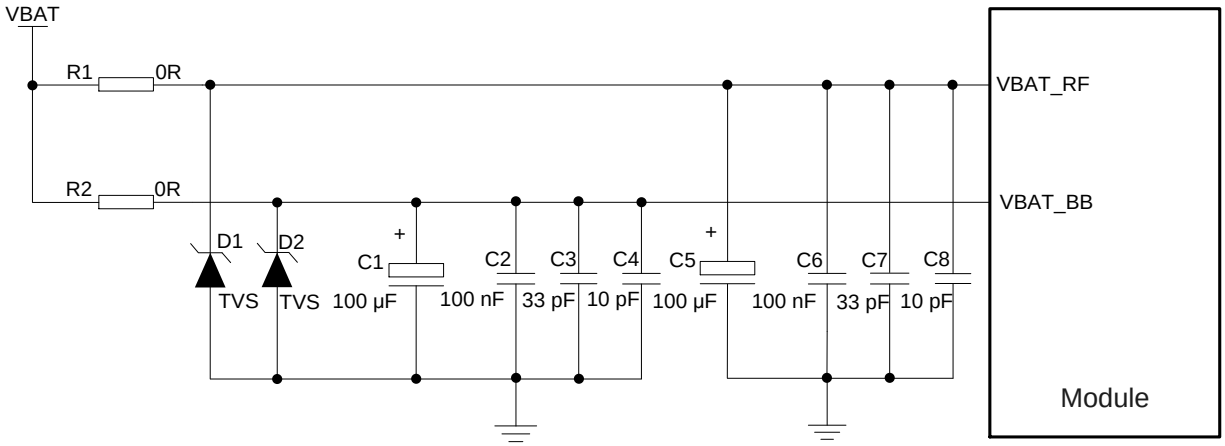


Figure 6: Star Structure of the Power Supply

Power design for a module is critical to its performance. The power supply of the module should be able to provide sufficient current of at least 0.8 A, so it is recommended to select a DC-DC converter chip or an LDO chip with ultra-low leakage current and current output no less than 1.0 A for the power supply design.

3.5.3. Power Supply Voltage Monitoring

AT+CBC can be used to monitor the VBAT voltage value. For more details, see ***document [4]***.

3.6. Turn On and off Scenarios

3.6.1. Turn On with PWRKEY

The following table shows the pin definition of PWRKEY.

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	46	DI	Turn on/off the module	Internally pulled up with a 470 kΩ resistor.

When the module is in turn-off mode, driving PWRKEY low for 500–1000 ms and then releasing it will turn on the module. It is recommended to use an open drain/collector driver to control the PWRKEY.

A simple reference design is illustrated in the following figure.

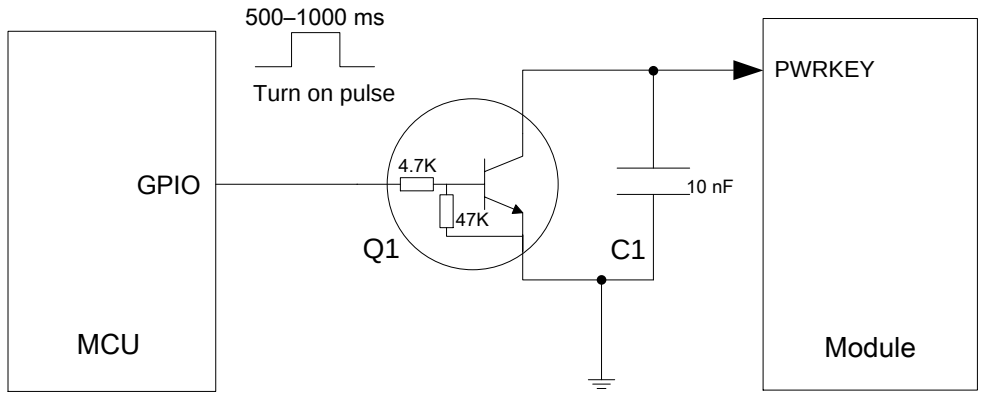


Figure 7: Turn On the Module with Driving Circuit

Another way to control the PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may generate from fingers. Therefore, a TVS component is indispensable to be placed nearby the button for ESD protection. A reference design is shown in the following figure.

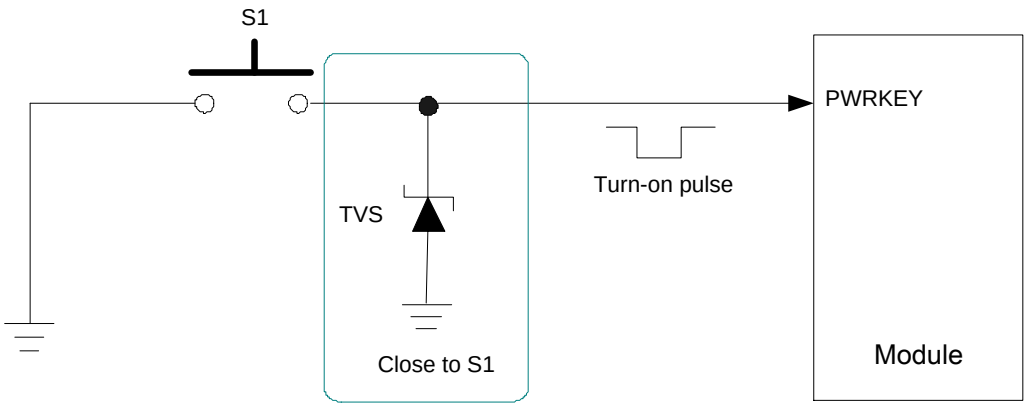


Figure 8: Turn On the Module with a Button

The power-up timing of the module varies with the VBAT stable duration before you drive PWRKEY low.

1) Drive PON_TRIG high and then drive PWRKEY low when VBAT is stable for 100–200 ms, the module will be turned on immediately, and in this case, the power-up timing is shown below.

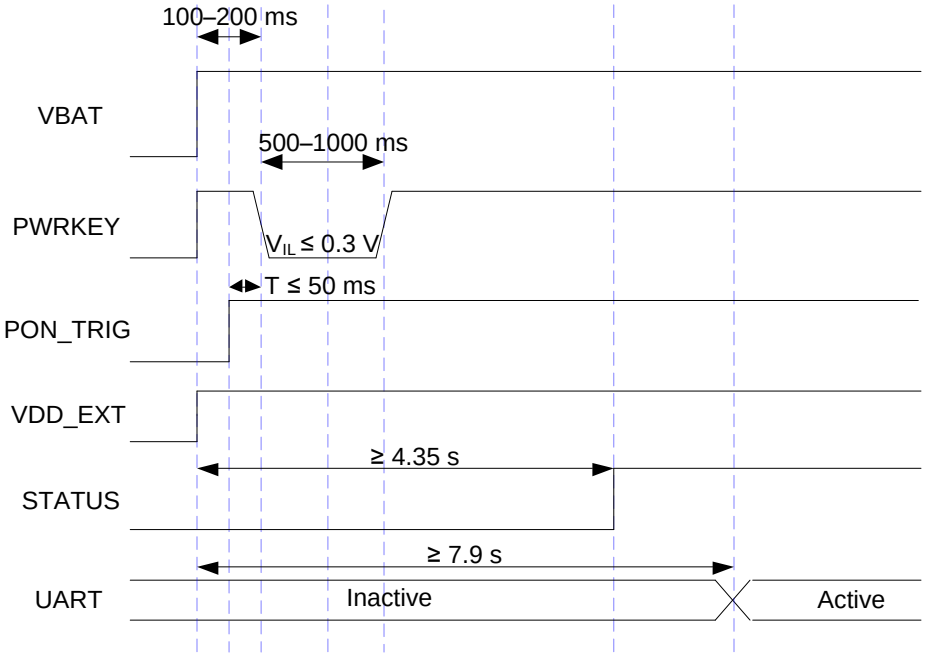


Figure 9: Power-up Timing (After VBAT is Stable for 100–200 ms)

NOTE

1. Ensure that VBAT is stable for 100–200 ms before pulling down PWRKEY.
2. Before you turn on the module by driving PWRKEY low for 500–1000 ms, drive PON_TRIG high, otherwise, the main UART interface will be inaccessible.

2) Drive PON_TRIG high and then drive PWRKEY low when VBAT is stable for more than 250 ms, the module will also be turned on immediately, and in this case, the power-up timing is shown below.

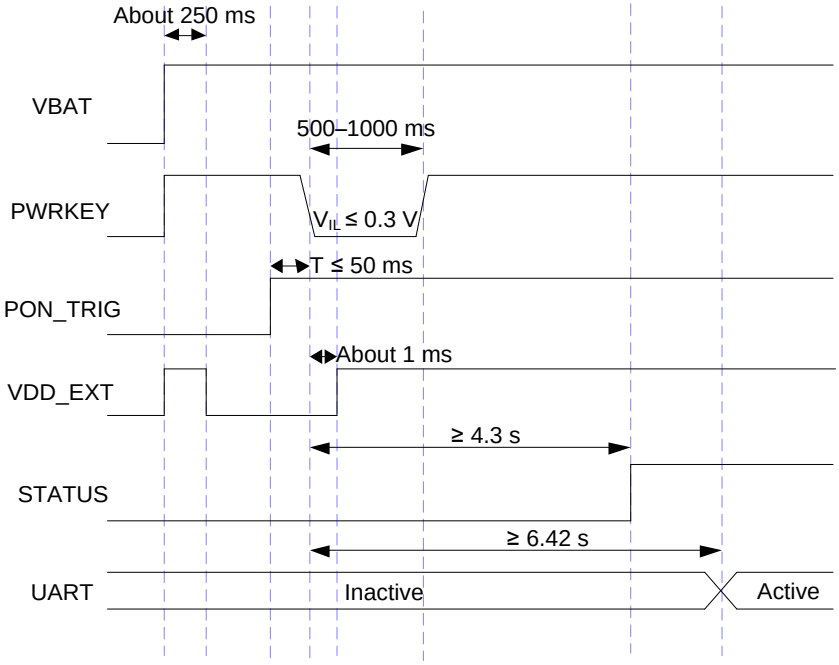


Figure 10: Power-up Timing (After VBAT is Stable for more than 250 ms)

After the module is turned off with the PWRKEY and PON_TRIG solution (see ***Chapter 3.6.2.1***) or the AT command and PON_TRIG solution (see ***Chapter 3.6.2.2***), VBAT will keep powered on all the time until the main power supply is disconnected. In this case, drive PON_TRIG high and then drive PWRKEY low will restart the module, and the restart timing is shown below.

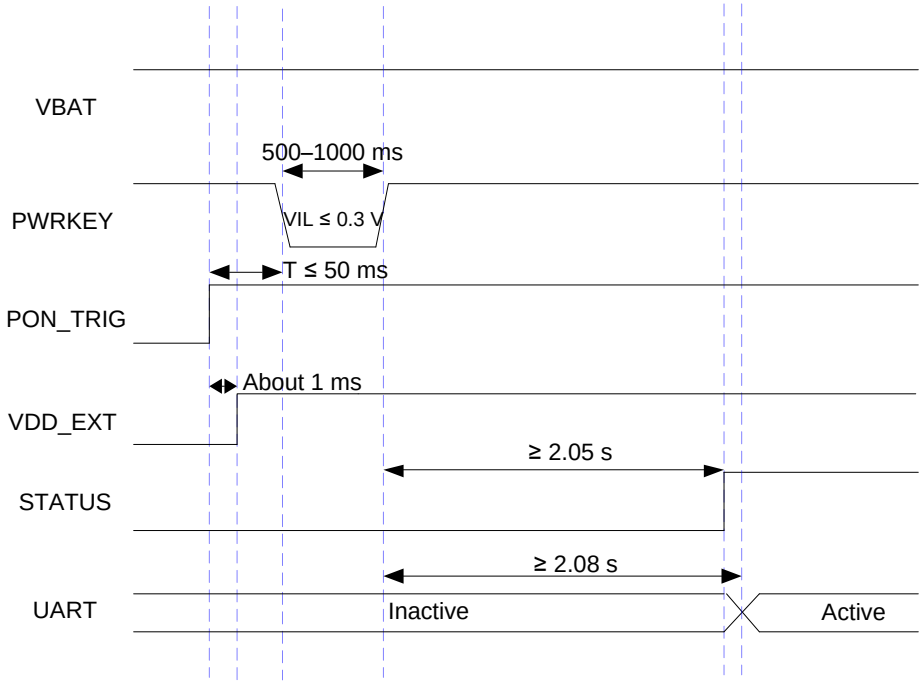


Figure 11: Restart Timing

NOTE

1. After VBAT is powered on, the module requires an internal program loading time of about 250 ms.
2. Before you turn on or restart the module by driving PWRKEY low, drive PON_TRIG high; otherwise the main UART interface will be inaccessible.

3.6.2. Turn Off

After the module is turned off or enters PSM, do not pull up any I/O pin lest it cause additional power consumption and possibly damage pins on the module.

Either of the following methods can be used to turn off the module normally:

- Turn off the module with PWRKEY and PON_TRIG.
- Turn off the module with **AT+QPOWD** and PON_TRIG.

3.6.2.1. Turn Off with PWRKEY and PON_TRIG

When the module is powered on, drive PWRKEY low for 650–1500 ms before you release it, and then pull down PON_TRIG within 200 ms, after which the module will execute a power-down procedure.

The power-down timing is illustrated in the following figure.

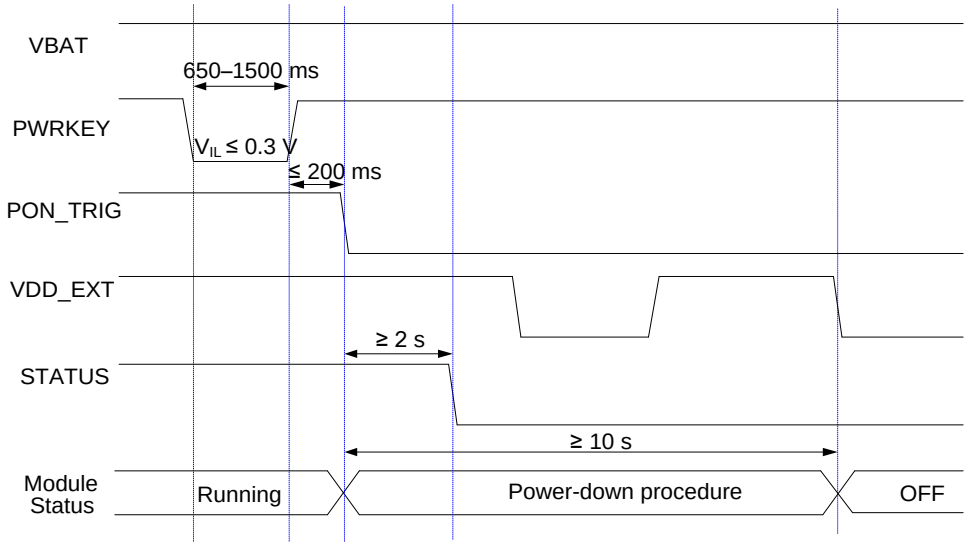


Figure 12: Power-down Timing (PWRKEY & PON_TRIG)

3.6.2.2. Turn Off with AT Command and PON_TRIG

Similar to PWRKEY, the module can be turned off safely with **AT+QPOWD**. After the **AT+QPOWD** is sent, pull down PON_TRIG within 200 ms, then the module will execute the power-down procedure.

See ***document [4]*** for details about **AT+QPOWD**.

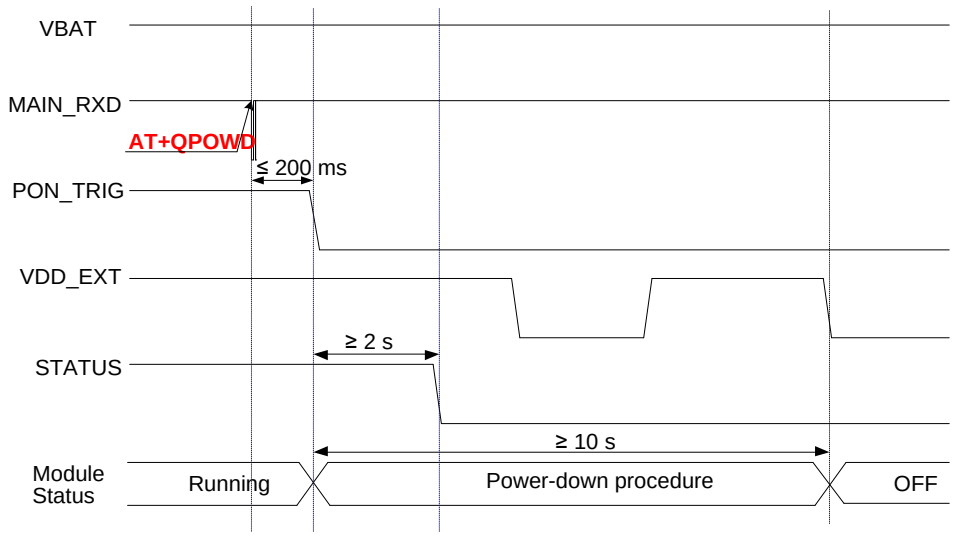


Figure 13: Power-down Timing (AT Command & PON_TRIG)

NOTE

1. To avoid internal flash data damage, do not switch off the power supply while the module is working normally. The power supply can be cut off only after the module is shut down with PWRKEY & PON_TRIG or AT command & PON_TRIG.
2. When turning off the module with AT command, keep PWRKEY at a high level after executing power-off command. Otherwise, the module will be turned on again after turned off.

3.7. Reset

The module can be reset by driving RESET_N low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description
RESET_N	45	DI	Reset the module. Internally pulled up with a 470 kΩ resistor.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or button can be used to control RESET_N.

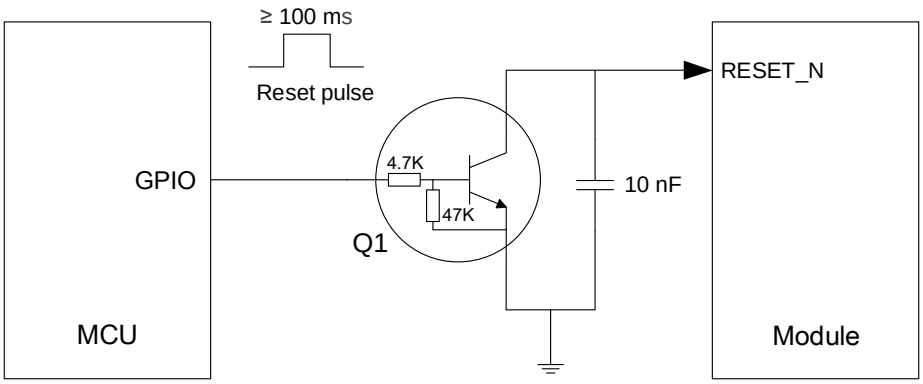


Figure 14: Reference Design of RESET_N with Driving Circuit

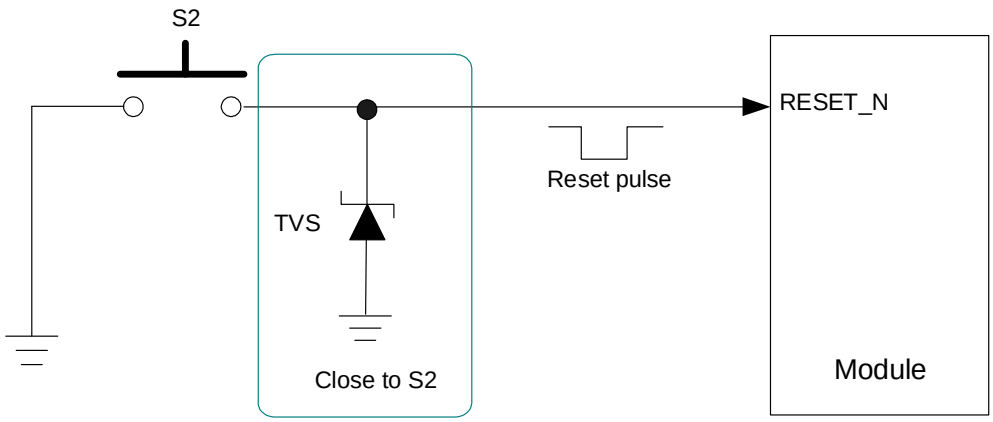


Figure 15: Reference Design of RESET_N with Button

The reset timing is illustrated in the following figure.

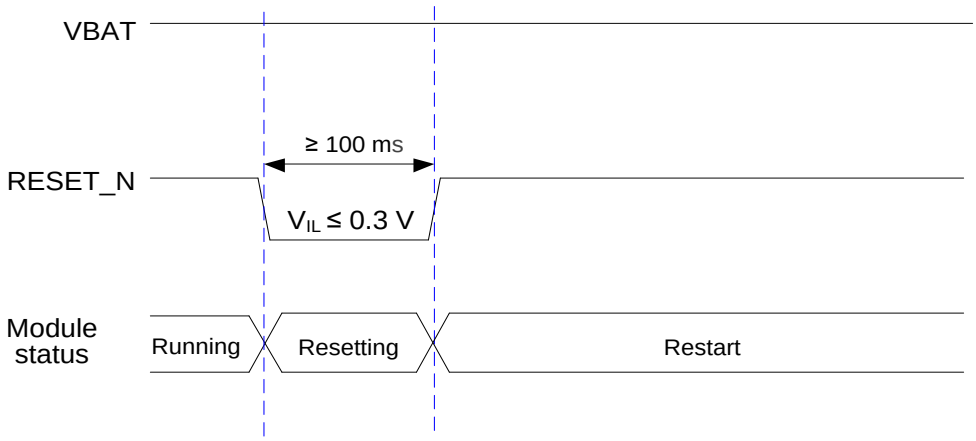


Figure 16: Reset Timing

NOTE

Ensure that there is no large capacitance on RESET_N pin.

3.8. PON_TRIG

BG770A-GL & BG773A-GL provides one PON_TRIG pin. Drive PON_TRIG high and remain it high, the module will wake up from PSM. PON_TRIG is not pulled up/down internally by default.

Table 10: Pin Definition of PON_TRIG

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	72	DI	Used for main UART function control and for entering/exiting e-I-DRX, PSM, sleep and power off modes	1.8 V power domain. No internal pull up/down resistors by default.

PON_TRIG can realize the following functions:

- Make the module enter or exit e-I-DRX, PSM mode and sleep mode.
- Enable/disables the main UART interface communication function.
- Turns on/off the module.

PON_TRIG must be designed to allow for external control. A reference design is shown in the following figure.

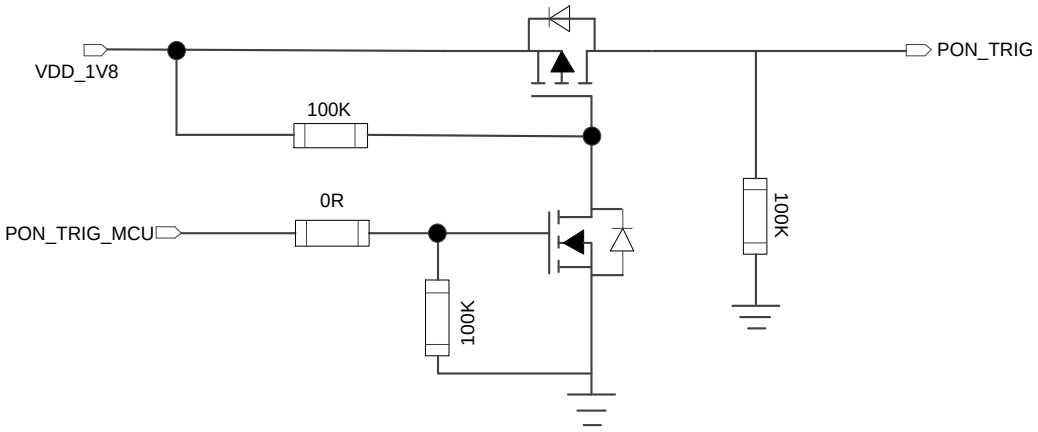


Figure 17: Reference Design of PON_TRIG

NOTE

VDD_1V8 is powered by an external LDO.

The use of PON_TRIG is illustrated below.

- PON_TRIG is not pulled up/down internally by default. Before the module is turned on, PON_TRIG must be pulled up. Otherwise, the main UART will be inaccessible.
- When the module is powered on, pull down PON_TRIG within 200 ms after sending **AT+QPOWED** or driving PWRKEY low, after which the module will execute a power-down procedure. For more details, see ***Chapter 3.6.2***.
- After sending **AT+QPSMS** to enable PSM, driving PON_TRIG low will set the module to PSM. Drive PON_TRIG high and remain it high, the module will wake up from PSM. In this case, PON_TRIG must remain high, otherwise the module will re-enter PSM.
- Pull down PON_TRIG and keep it low in e-I-DRX, PSM, sleep or power off mode. In other cases, pull high PON_TRIG and keep it high to make sure the main UART is accessible. For details about PON_TRIG use in e-I-DRX and sleep modes, see ***Chapter 0*** and ***Chapter 3.4.4***, respectively.

3.9. USIM Interface

BG770A-GL supports 1.8 V USIM card only. The USIM interface circuitry meets ETSI and IMT-2000 requirements.

Since BG773A-GL supports integrated iSIM, which can improve the security of the device and minimize the PCB area. If you need to enable iSIM function, the external USIM card circuit design is not required. For more details about iSIM function, please contact with local network service providers.

Table 11: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	44	DI	USIM card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM_VDD	16	PO	USIM card power supply	Only 1.8 V USIM card is supported.
USIM_RST	15	DO	USIM card reset	1.8 V power domain.
USIM_DATA	14	DIO	USIM card data	1.8 V power domain.
USIM_CLK	13	DO	USIM card clock	1.8 V power domain.
USIM_GND	65		Specified ground for USIM card	

BG770A-GL supports USIM card hot-plug via USIM_DET, and both high-and low-level detections are supported. The function is disabled by default, and see **AT+QSIMDET** in ***document [4]*** for more details.

The following figure shows a reference design of USIM interface with an 8-pin USIM card connector.

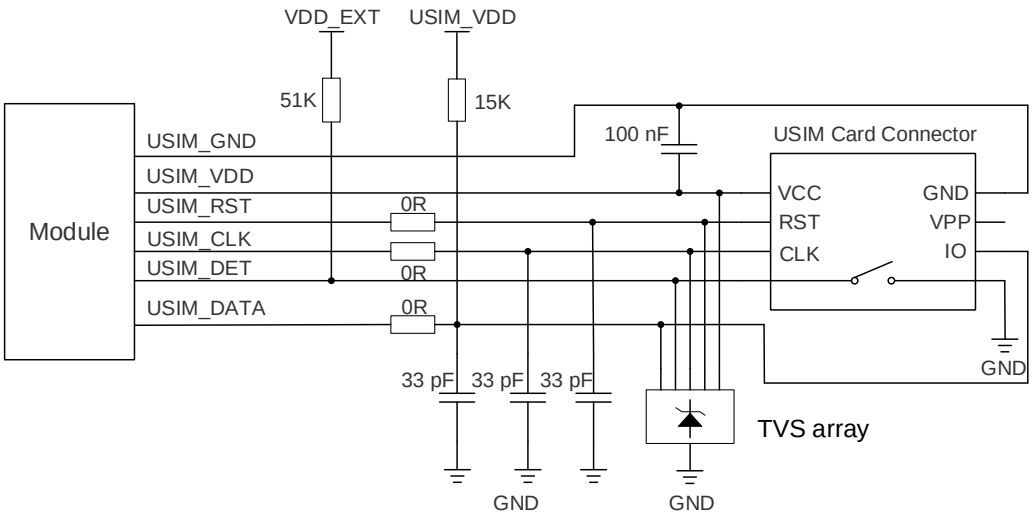


Figure 18: Reference Design of USIM Interface with an 8-Pin USIM Card Connector

If USIM card detection function is not needed, keep USIM_DET unconnected. A reference design for USIM interface with a 6-pin USIM card connector is illustrated in the following figure.

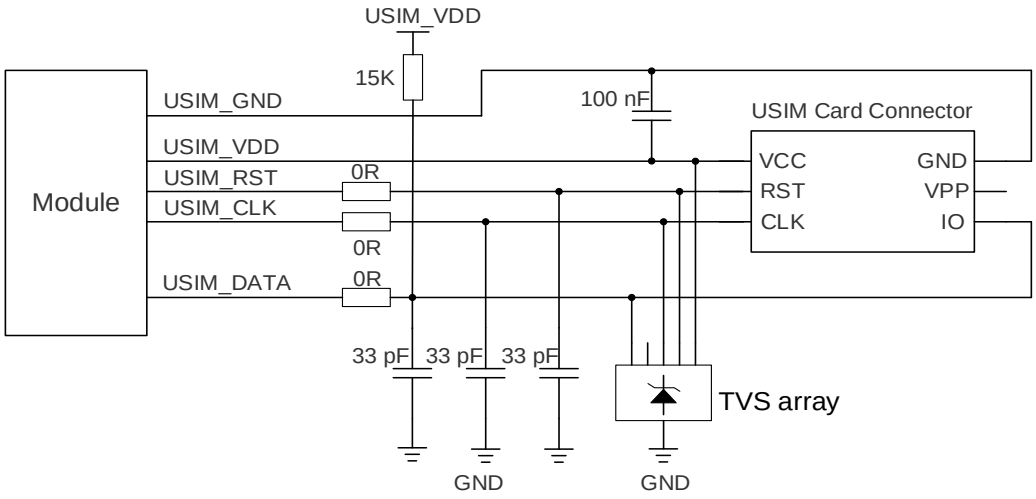


Figure 19: Reference Design of USIM Interface with a 6-Pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, follow the criteria below in USIM circuit design:

- Place the USIM card connector as close as possible to the module with a trace shorter than 200 mm.
- Keep USIM card signals away from RF and power supply traces.
- Ensure a short and wide ground trace between the module and the USIM card connector. Keep the ground and USIM_VDD traces at least 0.5 mm wide to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND is less than 1 μF, and place it as close to USIM card connector as possible. If the system ground plane is complete, USIM_GND can be directly connected to the system ground.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep their traces away from each other and shield them with ground. USIM_RST should also be shielded with ground.
- To offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 15 pF. It is recommended to reserve 0 Ω series resistors for the USIM signals of the module to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Note that the USIM peripheral circuit should be close to the USIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability, and should be placed close to the USIM card connector.

3.10. USB Interface*

BG770A-GL/BG773A-GL provides one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports full speed mode only.

The following table shows the pin definition of USB interface.

Table 12: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	12	AI	USB connection detect	Input range: 1.19–2.0 V
USB_DP	11	AIO	USB differential data (+)	Require differential impedance of 90 Ω
USB_DM	10	AIO	USB differential data (-)	
USBPHY_3P3	42	PI	Power supply for USB PHY circuit	Typ. 3.3 V
USBPHY_3P3_EN	64	DO	External LDO enable control for USB	1.8 V power domain
GND	43		Ground	

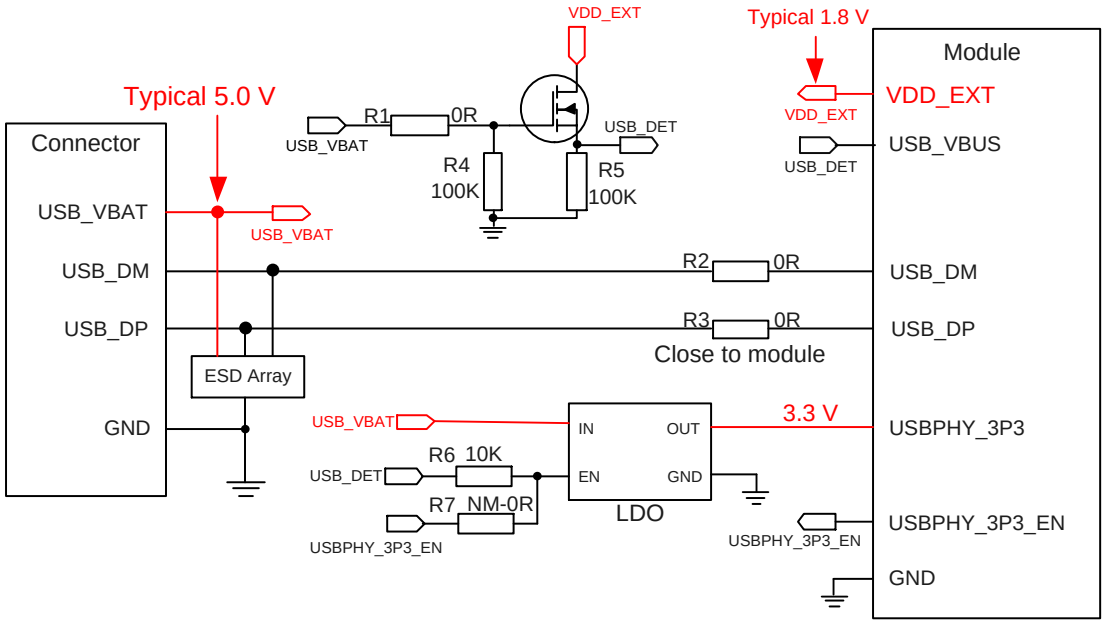


Figure 20: Reference Design of USB Interface

To ensure the integrity of USB data signals, resistors R2 and R3 should be placed close to the module, and also these resistors should be placed close to each other. The extra stubs of trace must be as short as possible.

To meet USB 2.0 specification, comply with the following principles while designing the USB interface.

- It is important to route the USB signal traces as a differential pair with ground. The impedance of USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices and RF signal traces. It is

important to route the USB differential traces in inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.

- Junction capacitance of the ESD protection conponents might cause influences on USB data traces, so pay attention to the device selection. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection conponents as close to the USB connector as possible.

For more details about USB 2.0 specification, visit http://www.usb.org/home.

NOTE

1. The input voltage range of USB_VBUS is 1.19–2.0 V.
2. After the module is turned off or enters PSM, do not pull up any USB interface pin lest it cause additional power consumption and potentially damage pins on the module.
3. When using the UMTS&LTE EVB board to test the USB interface function of the module, see ***document [5]***.
4. USB interface is under developed on BG773A-GL, while it can be used on BG770A-GL.

3.11. UART Interfaces

The module provides three UART interfaces: main UART interface, debug UART interface and auxiliary UART interface. Features of them are illustrated below:

- The main UART interface supports 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates, and the default is 115200 bps. It is used for data transmission and AT command communication, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- The debug UART interface supports 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates, and the default is 115200 bps. It is used for firmware upgrade, software debugging, log and NMEA sentences output, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).
- The auxiliary UART interface supports 921600 bps baud rate by default. It is used for RF calibration and log output, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).

The following tables show the pin definition of three UART interfaces.

Table 13: Pin Definition of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	62	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep these pins open.
MAIN_RXD	6	DI	Main UART receive	
MAIN_TXD	7	DO	Main UART transmit	
MAIN_CTS	39	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	
MAIN_RTS	38	DI	DTE request to send signal from DCE (Connects to DTE's RTS)	
MAIN_DCD	90	DO	Main UART data carrier detect	
MAIN_RI*	76	DO	Main UART ring indication	

NOTE

1. **AT+IPR** can be used to set the baud rate of the main UART interface, and **AT+IFC** can be used to enable/disable the hardware flow control (the function is disabled by default). See ***document [4]*** for more details about these AT commands.
2. MAIN_RI is under developed on BG773A-GL, while it can be used on BG770A-GL.

Table 14: Pin Definition of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	60	DO	Debug UART transmit	It is recommended to add test points in the design.
DBG_RXD	61	DI	Debug UART receive	
DBG_CTS	51	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	
DBG_RTS	92	DI	DTE request to send signal from DCE (Connects to DTE's RTS)	

Table 15: Pin Definition of Auxiliary UART Interface

Pin Name	Pin No.	I/O	Description	Comment
AUX_TXD	93	DO	Auxiliary UART transmit	1.8 V power domain.

AUX_RXD	82	DI	Auxiliary UART receive	If unused, keep these pins open.
AUX_CTS	70	DO	DTE clear to send signal from DCE (Connects to DTE's CTS)	
AUX_RTS	59	DI	DTE request to send signal from DCE (Connects to DTE's RTS)	

The module provides 1.8 V UART interfaces. A voltage-level translator should be used if your application is equipped with a 3.3 V UART interface. It is recommended to use a level shifting chip without internal pull-up. The voltage-level translator TXB0108PWR provided by Texas Instruments is recommended. The following figure shows a reference design of the main UART interface:

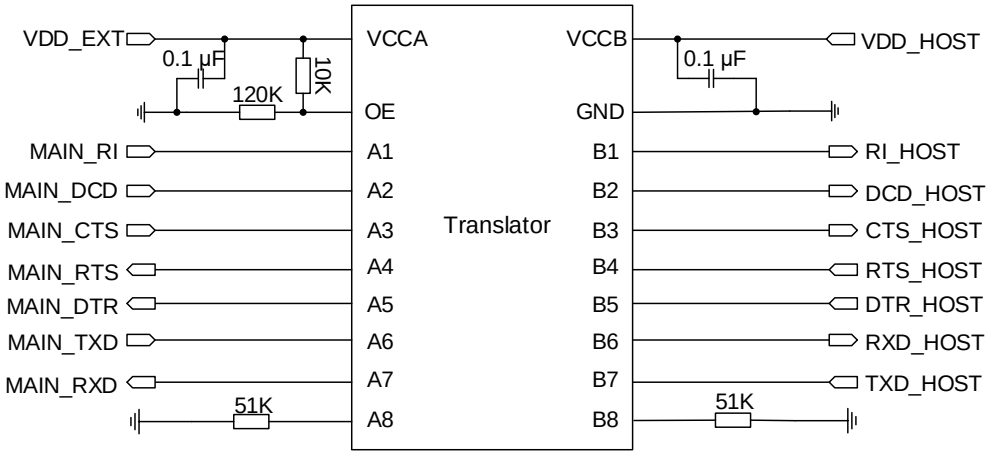


Figure 21: Main UART Reference Design (Translator Chip)

Visit http://www.ti.com for more information.

Another example with transistor translation circuit is shown as below. For the design of circuits in dotted lines, see that of circuits in solid lines, but pay attention to the direction of connection.

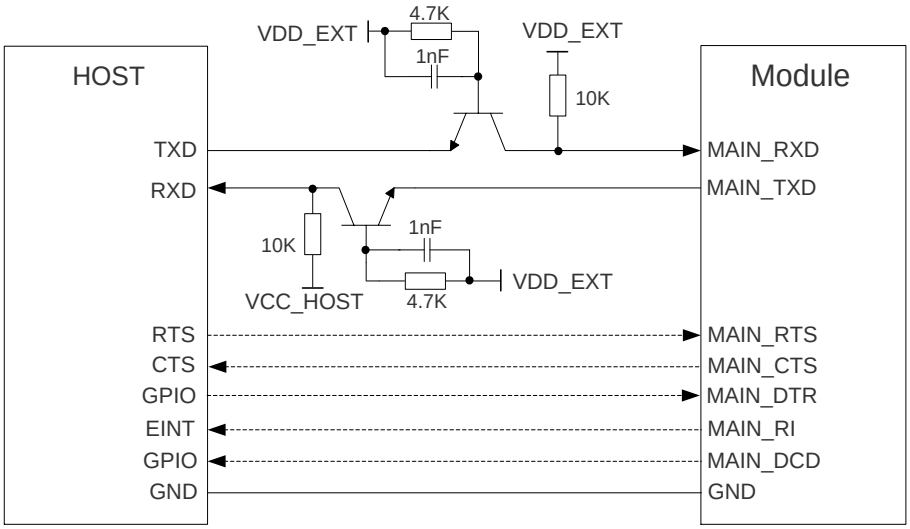


Figure 22: Main UART Reference Design (Transistor Circuit)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. The main UART interface should be disconnected in PSM and power off modes lest it cause additional power consumption and potentially damage pins on the module.
3. It is recommended to use a level-shifting chip without internal pull-up, such as TXB0108PWR, for level-shifting.
4. Please note that the module's CTS is connected to the host's CTS, and the module's RTS is connected to the host's RTS.

3.12. Indication Signals

3.12.1. Network Status Indication

BG770A-GL/BG773A-GL provides one network status indication pin: NET_STATUS. The pin is used to drive a network status indication LED. The following tables describe the pin definition and logic level changes of NET_STATUS in different network activity status.

Table 16: Pin Definition of NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	79	DO	Indicate the module's network activity status	1.8 V power domain. If the pin is unused, keep it open.

Table 17: Working State of NET_STATUS

Pin Name	Logic Level Changes	Network Status
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing

A reference design is shown in the following figure.

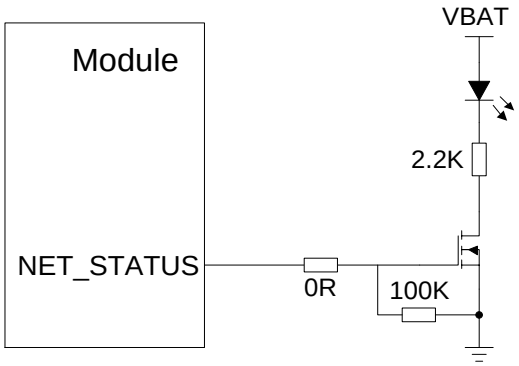


Figure 23: Reference Design of NET_STATUS

3.12.2. STATUS

The STATUS pin indicates the operation status of BG770A-GL/BG773A-GL. It outputs high level when the module powers on.

Table 18: Pin Definition of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	78	DO	Indicate the module's operation status	1.8 V power domain

The following figure shows a reference design of STATUS.

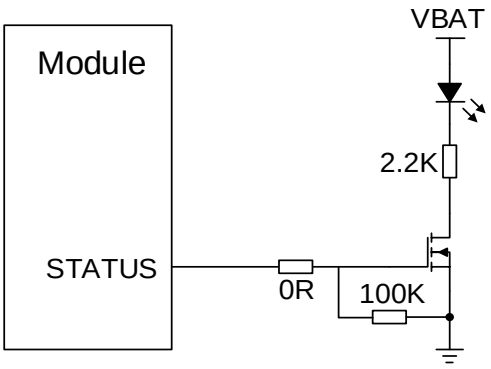


Figure 24: Reference Design of STATUS

3.12.3. MAIN_RI*

AT+QCFG="risignaltype","physical" can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI.
The default behaviors of MAIN_RI are shown as below.

Table 19: Default Behaviors of MAIN_RI

State	Response
Idle	MAIN_RI remains at a high level.
URC	MAIN_RI outputs a 120 ms low pulse when a new URC is returned.

The default MAIN_RI behaviors can be configured flexibly by **AT+QCFG="urc/ri/ring"**. For more details about **AT+QCFG**, see ***document [3]***.

NOTE

1. A URC can be outputted from the main UART (default), auxiliary UART or EMUX ports through configuring URC indication option with **AT+QURCCFG**. See ***document [4]*** for details about the AT command.
2. MAIN_RI is under developed on BG773A-GL, while it can be used on BG770A-GL.

3.13. ADC Interfaces

The module provides two analog-to-digital converter (ADC) interfaces. **AT+QADC=0** can be used to read the voltage value on ADC0 pin. **AT+QADC=1** be used to read the voltage value on ADC1 pin. For more details about the AT command, see ***document [4]***.

To improve the accuracy of ADC voltage values, the traces of ADC should be surrounded with ground.

Table 20: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description
ADC0	17	AI	General-purpose ADC interface
ADC1	18	AI	General-purpose ADC interface

The following table describes the characteristics of ADC interfaces.

Table 21: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
Voltage Range	0	-	1.8	V
Resolution	6	-	12	bit

NOTE

1. ADC input voltage must not exceed 1.8 V.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.
3. It is recommended to use resistor divider circuit for ADC application, and the divider's resistor accuracy should be no less than 1 %.
4. After the module is turned off or enters PSM, do not pull up any pin of ADC interfaces lest it cause additional power consumption and potentially damage pins on the module.

3.14. GPIO Interfaces

The module provides seven general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"** command can be used to configure the status of GPIO pins. For more details about the AT command, see ***document [3]***.

Table 22: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description
GPIO1	1	DIO	General-purpose input/output
GPIO2	8	DIO	General-purpose input/output
GPIO3	9	DIO	General-purpose input/output
GPIO4	33	DIO	General-purpose input/output
GPIO5	40	DIO	General-purpose input/output
GPIO6	57	DIO	General-purpose input/output
GPIO7	63	DIO	General-purpose input/output

3.15. GRFC Interfaces

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 23: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comments
GRFC1	83	DO	Generic RF controller	1.8 V power domain. If these pins are unused, keep them open.
GRFC2	94	DO	Generic RF controller	

Table 24: Truth Table of GRFC Interfaces

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)
Low	Low	880–2200
Low	High	791–879.9
High	Low	698–790.9

4 GNSS

4.1. General Description

BG770A-GL/BG773A-GL supports GPS and GLONASS satellite systems using dedicated hardware accelerators in a power and cost-efficient manner.

The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via debug UART interface by default.

By default, BG770A-GL/BG773A-GL GNSS engine is switched off. It has to be switched on via AT command. The module does not support concurrent operation of WWAN and GNSS. For more details about GNSS engine technology and configurations, see ***document [1]***.

4.2. GNSS Performance

The following table shows the GNSS performance of BG770A-GL/BG773A-GL.

Table 25: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Acquisition	Autonomous	-145	dBm
	Reacquisition	Autonomous	-153	dBm
	Tracking	Autonomous	-158	dBm
TTFF (GNSS)	Cold start @ open sky	Autonomous	29.42	s
		XTRA enabled	16.14	s
	Warm start @ open sky	Autonomous	28.38	s
		XTRA enabled	3.57	s

	Hot start @ open sky	Autonomous	1.07	s
		XTRA enabled	2.10	s
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	1.41	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing cold start command.

4.3. Layout Guidelines

The following layout guidelines should be taken into account in application designs.

- Maximize the distance between the GNSS antenna and the main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector and SD card should be kept away from antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for ANT_GNSS trace.

Refer to ***Chapter 5*** for GNSS antenna reference design and antenna installation information.

5 Antenna Interfaces

BG770A-GL/BG773A-GL includes a main antenna interface and a GNSS antenna interface. The impedance of antenna ports is 50 Ω.

5.1. Main Antenna Interface

5.1.1. Pin Definition

The pin definition of the main antenna interface is shown below.

Table 26: Pin Definition of Main Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	26	AIO	Main antenna interface	50 Ω impedance

5.1.2. Operating Frequency

Table 27: BG770A-GL & BG773A-GL Operating Frequency

3GPP Band	Transmit	Receive	Unit
LTE HD-FDD B1	1920–1980	2110–2170	MHz
LTE HD-FDD B2	1850–1910	1930–1990	MHz
LTE HD-FDD B3	1710–1785	1805–1880	MHz
LTE HD-FDD B4	1710–1755	2110–2155	MHz
LTE HD-FDD B5	824–849	869–894	MHz
LTE HD-FDD B8	880–915	925–960	MHz
LTE HD-FDD B12	699–716	729–746	MHz

LTE HD-FDD B13	777–787	746–756	MHz
LTE HD-FDD B17 [10]	704–716	734–746	MHz
LTE HD-FDD B18	815–830	860–875	MHz
LTE HD-FDD B19	830–845	875–890	MHz
LTE HD-FDD B20	832–862	791–821	MHz
LTE HD-FDD B25	1850–1915	1930–1995	MHz
LTE HD-FDD B26 [11]	814–849	859–894	MHz
LTE HD-FDD B27 [11]	807–824	852–869	MHz
LTE HD-FDD B28	703–748	758–803	MHz
LTE HD-FDD B66	1710–1780	2110–2180	MHz

5.1.3. Reference Design

A reference design of main antenna interface is shown as below. It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

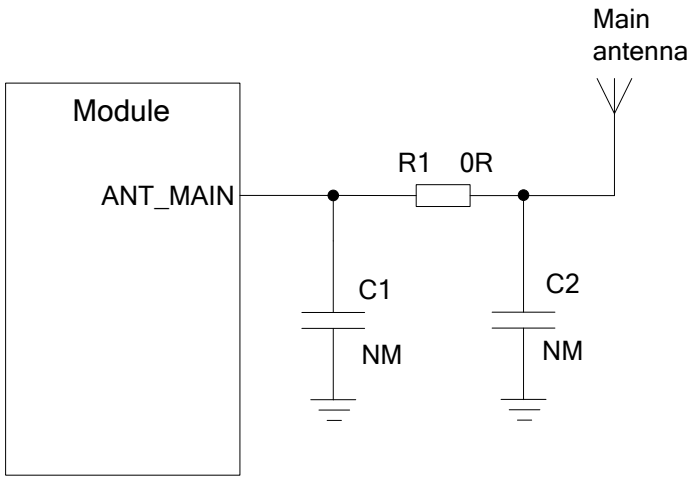


Figure 25: Reference Design of Main Antenna Interface

[10] LTE HD-FDD B17 is supported in Cat NB1/Cat NB2 only.
[11] LTE HD-FDD B26 and B27 are supported in Cat M1 only.

5.2. GNSS Antenna Interface

The following tables show the pin definition and frequency specification of GNSS antenna interface.

5.2.1. Pin Definition

Table 28: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	32	AI	GNSS antenna interface	50 Ω impedance If this pin is unused, keep it open.

5.2.2. GNSS Operating Frequency

Table 29: GNSS Operating Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz

5.2.3. Reference Design

A reference design of GNSS antenna interface is shown as below.

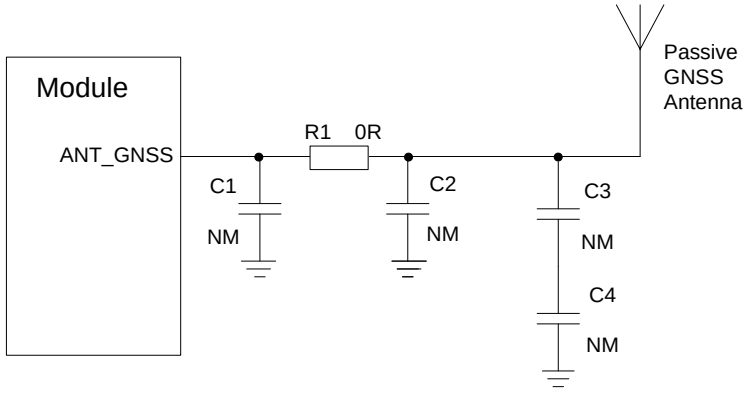


Figure 26: Reference Design of GNSS Antenna Interface

NOTE

The module is designed with a built-in LNA, and supports passive GNSS antenna only. Active antenna and external LNA are not supported.

5.3. RF Routing Guidelines

For users' PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

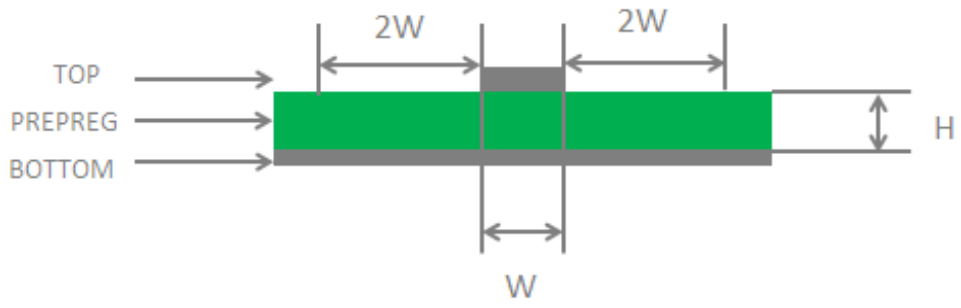


Figure 27: Microstrip Design on a 2-layer PCB

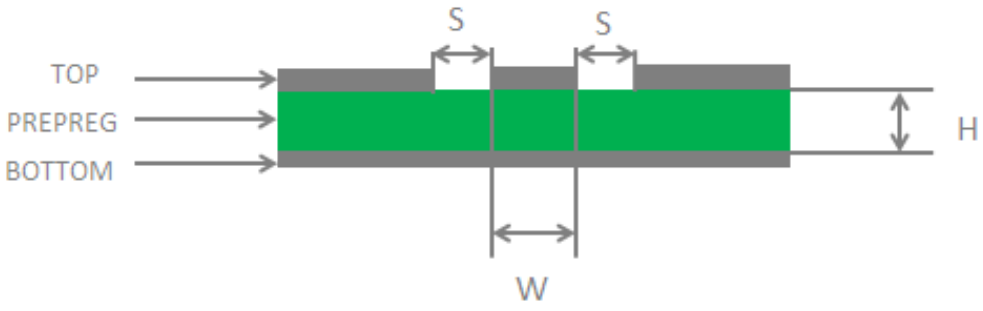


Figure 28: Coplanar Waveguide Design on a 2-layer PCB

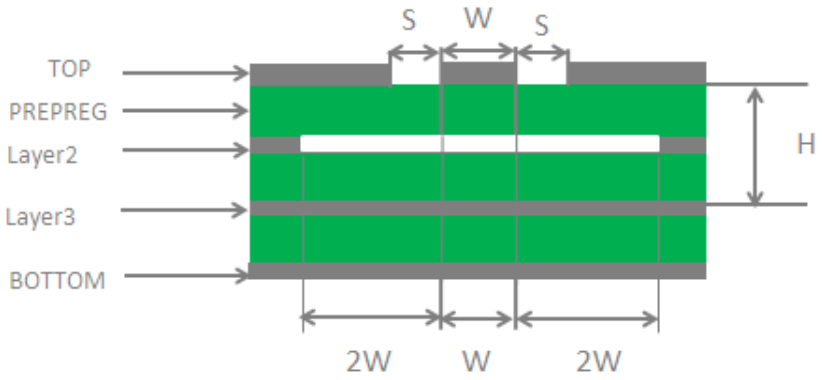


Figure 29: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

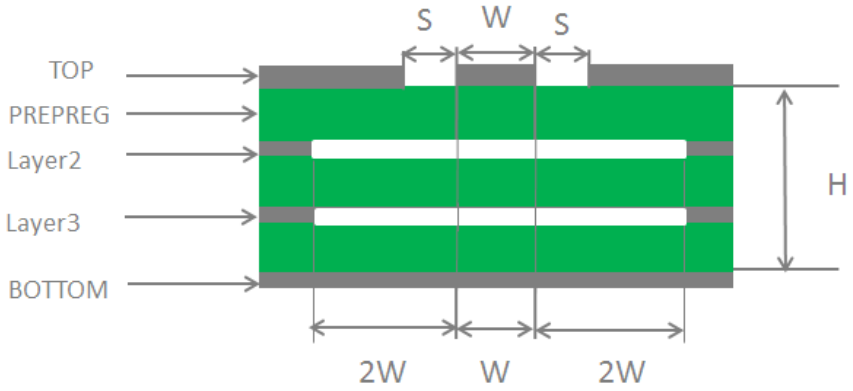


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [6]***.

5.4. Antenna Installation

5.4.1. Antenna Design Requirements

The following table shows the requirements on the main antenna and the GNSS antenna.

Table 30: Antenna Design Requirements

Antenna Type	Requirements
GNSS	Must be a passive antenna Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi
LTE	VSWR: ≤ 2 Efficiency: > 30 % Max. Input Power: 50 W Input Impedance: 50 Ω Cable Insertion Loss: **< 1 dB:** LB (< 1 GHz) **< 1.5 dB:** MB (1–2.3 GHz)

5.4.2. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connectors provided by Hirose.

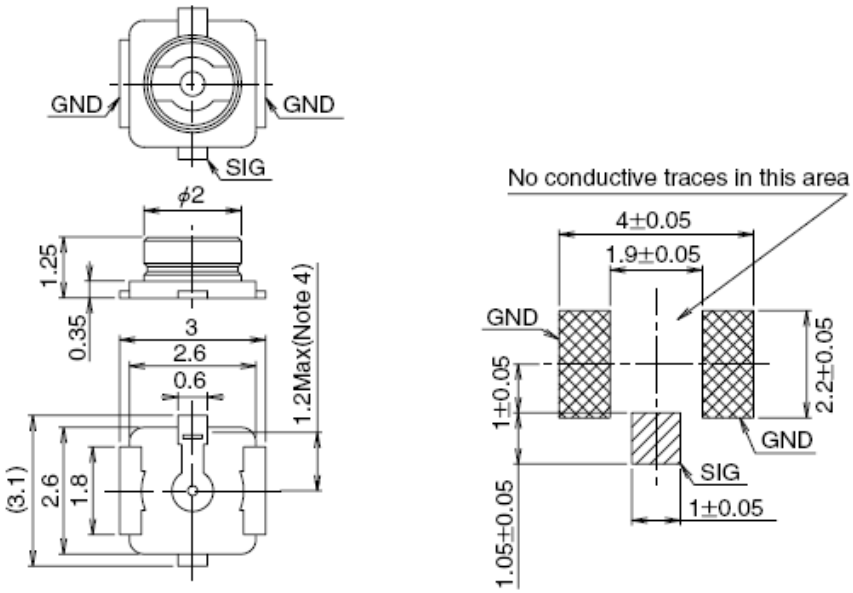


Figure 31: Dimensions of the Receptacle (Unit: mm)

The mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

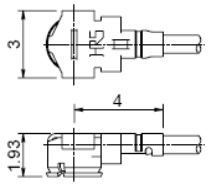
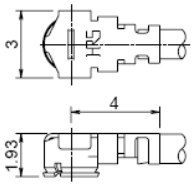
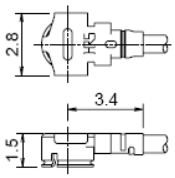
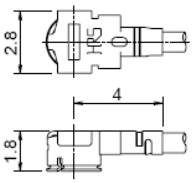
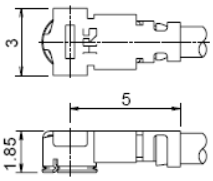
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 32: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

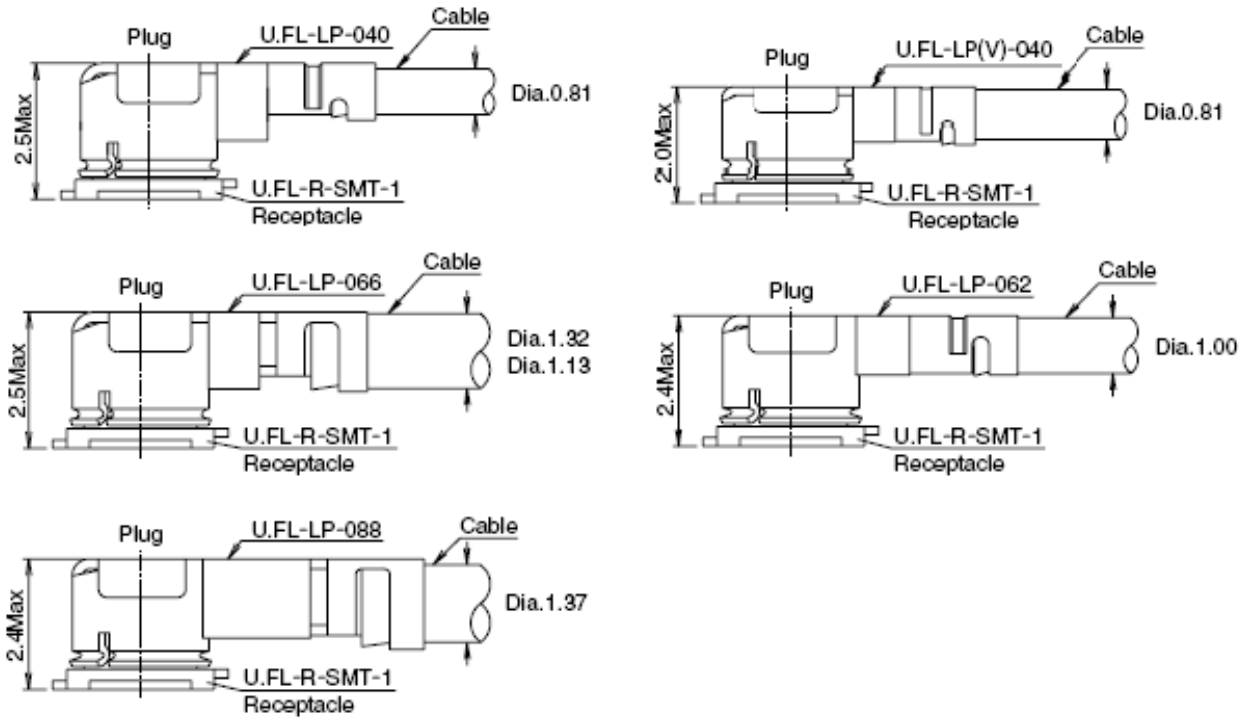


Figure 33: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 31: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_BB	-0.2	4.5	V
VBAT_RF	-0.2	4.5	V
USB_VBUS	1.19	2.0	V
Voltage at Digital Pins	-0.3	2.0	V

6.2. Power Supply Ratings

Table 32: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT_BB [12]	Power supply for the module's baseband part	The actual input voltages must be kept between the minimum and maximum values.	2.2	3.3	4.35	V

[12] When the module starts up normally, to ensure full function mode, the minimum power supply voltage should be higher than 3.1 V.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT_RF [12]	Power supply for the module's RF part	The actual input voltages must be kept between the minimum and maximum values.	3.1	3.3	4.2	V
USBPHY_3P3	Power supply for USB PHY circuit	-	-	3.3	-	V
USB_VBUS	USB connection detect	-	1.19	-	2.0	V

6.3. Operating and Storage Temperatures

Table 33: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [13]	-35	+25	+75	ºC
Extended Temperature Range [14]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

6.4. Power Consumption

The following table shows the power consumption of BG770A-GL & BG773A-GL.

Table 34: BG770A-GL Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Avg.	Max.	Unit
Leakage	Power-off @ USB/UART disconnected	1.4	-	μA
PSM	PSM @ USB/UART disconnected	1.4	-	μA

[13] Within the operating temperature range, the module meets 3GPP specifications.
[14] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

Rock Bottom	**AT+CFUN=0** @ Sleep mode	45	-	μA
Sleep Mode (USB/UART disconnected)	LTE Cat M1 DRX = 1.28 s	1.1	-	mA
	LTE Cat NB1 DRX = 1.28 s	2.2	-	mA
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 1.28 s, DRX = 1.28 s	0.06	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 1.28 s, DRX = 1.28 s	0.05	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.07	-	mA
	LTE Cat NB1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	0.16	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.12	-	mA
Idle State (USB/UART disconnected)	LTE Cat M1 DRX = 1.28 s	16.5	-	mA
	LTE Cat NB1 DRX = 1.28 s	17.0	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	16.0	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	16.0	-	mA
LTE Cat M1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 23.40 dBm	182.51	500.65	mA
	LTE HD-FDD B2 @ 23.14 dBm	184.77	528.46	mA
	LTE HD-FDD B3 @ 23.27 dBm	175.89	477.22	mA
	LTE HD-FDD B4 @ 23.29 dBm	175.88	486.06	mA
	LTE HD-FDD B5 @ 23.23 dBm	193.09	554.42	mA
	LTE HD-FDD B8 @ 23.48 dBm	214.80	653.30	mA
	LTE HD-FDD B12 @ 23.56 dBm	233.99	716.10	mA
	LTE HD-FDD B13 @ 23.19 dBm	200.37	566.59	mA

	LTE HD-FDD B18 @ 23.36 dBm	192.28	545.62	mA
	LTE HD-FDD B19 @ 23.45 dBm	193.63	555.78	mA
	LTE HD-FDD B20 @ 23.25 dBm	197.74	581.05	mA
	LTE HD-FDD B25 @ 23.58 dBm	184.45	524.71	mA
	LTE HD-FDD B26 @ 23.10 dBm	192.68	559.21	mA
	LTE HD-FDD B27 @ 23.06 dBm	191.86	559.27	mA
	LTE HD-FDD B28A @ 23.40 dBm	229.53	682.16	mA
	LTE HD-FDD B28B @ 23.39 dBm	228.11	686.99	mA
	LTE HD-FDD B66 @ 22.87. dBm	177.39	498.33	mA
LTE Cat NB1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 23.19 dBm	168.42	543.91	mA
	LTE HD-FDD B2 @ 23.42 dBm	169.30	548.95	mA
	LTE HD-FDD B3 @ 23.38 dBm	165.42	539.46	mA
	LTE HD-FDD B4 @ 23.32 dBm	165.64	528.80	mA
	LTE HD-FDD B5 @ 23.24 dBm	185.75	592.76	mA
	LTE HD-FDD B8 @ 23.40 dBm	196.19	659.33	mA
	LTE HD-FDD B12 @ 23.17 dBm	219.43	740.62	mA
	LTE HD-FDD B13 @ 23.25 dBm	189.37	612.65	mA
	LTE HD-FDD B17 @ 23.26 dBm	216.57	747.99	mA
	LTE HD-FDD B18 @ 23.43 dBm	181.85	596.65	mA
	LTE HD-FDD B19 @ 23.32 dBm	184.30	580.59	mA
	LTE HD-FDD B20 @ 23.41 dBm	189.34	606.56	mA
	LTE HD-FDD B25 @ 23.48 dBm	168.63	545.30	mA
	LTE HD-FDD B28 @ 23.28 dBm	221.81	748.14	mA
	LTE HD-FDD B66 @ 23.01 dBm	164.18	530.24	mA

Table 35: BG773A-GL Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Avg.	Max.	Unit
Leakage	Power-off @ USB/UART disconnected	1.4	-	μA
PSM	PSM @ USB/UART disconnected	1.4	-	μA
Rock Bottom	**AT+CFUN=0** @ Sleep mode	TBD	-	μA
Sleep Mode (USB/UART disconnected)	LTE Cat M1 DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 DRX = 1.28 s	TBD	-	mA
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 1.28 s, DRX = 1.28 s	TBD	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 1.28 s, DRX = 1.28 s	TBD	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
Idle State (USB/UART disconnected)	LTE Cat M1 DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 DRX = 1.28 s	TBD	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	TBD	-	mA
LTE Cat M1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 23.40 dBm	TBD	TBD	mA
	LTE HD-FDD B2 @ 23.14 dBm	TBD	TBD	mA
	LTE HD-FDD B3 @ 23.27 dBm	TBD	TBD	mA
	LTE HD-FDD B4 @ 23.29 dBm	TBD	TBD	mA

	LTE HD-FDD B5 @ 23.23 dBm	TBD	TBD	mA
	LTE HD-FDD B8 @ 23.48 dBm	TBD	TBD	mA
	LTE HD-FDD B12 @ 23.56 dBm	TBD	TBD	mA
	LTE HD-FDD B13 @ 23.19 dBm	TBD	TBD	mA
	LTE HD-FDD B18 @ 23.36 dBm	TBD	TBD	mA
	LTE HD-FDD B19 @ 23.45 dBm	TBD	TBD	mA
	LTE HD-FDD B20 @ 23.25 dBm	TBD	TBD	mA
	LTE HD-FDD B25 @ 23.58 dBm	TBD	TBD	mA
	LTE HD-FDD B26 @ 23.10 dBm	TBD	TBD	mA
	LTE HD-FDD B27 @ 23.06 dBm	TBD	TBD	mA
	LTE HD-FDD B28A @ 23.40 dBm	TBD	TBD	mA
	LTE HD-FDD B28B @ 23.39 dBm	TBD	TBD	mA
	LTE HD-FDD B66 @ 22.87. dBm	TBD	TBD	mA
LTE Cat NB1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 23.19 dBm	TBD	TBD	mA
	LTE HD-FDD B2 @ 23.42 dBm	TBD	TBD	mA
	LTE HD-FDD B3 @ 23.38 dBm	TBD	TBD	mA
	LTE HD-FDD B4 @ 23.32 dBm	TBD	TBD	mA
	LTE HD-FDD B5 @ 23.24 dBm	TBD	TBD	mA
	LTE HD-FDD B8 @ 23.40 dBm	TBD	TBD	mA
	LTE HD-FDD B12 @ 23.17 dBm	TBD	TBD	mA
	LTE HD-FDD B13 @ 23.25 dBm	TBD	TBD	mA
	LTE HD-FDD B17 @ 23.26 dBm	TBD	TBD	mA
	LTE HD-FDD B18 @ 23.43 dBm	TBD	TBD	mA
	LTE HD-FDD B19 @ 23.32 dBm	TBD	TBD	mA
	LTE HD-FDD B20 @ 23.41 dBm	TBD	TBD	mA

	LTE HD-FDD B25 @ 23.48 dBm	TBD	TBD	mA
	LTE HD-FDD B28 @ 23.28 dBm	TBD	TBD	mA
	LTE HD-FDD B66 @ 23.01 dBm	TBD	TBD	mA

Table 36: BG770A-GL GNSS Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Typ.	Unit
Searching (**AT+CFUN=0**)	Cold start @ Instrument	49.04	mA
	Hot start @ Instrument	50.17	mA
	Lost state @ Instrument	49.31	mA
Tracking (**AT+CFUN=0**)	Instrument environment @ Passive antenna	49.58	mA
	Half sky @ Real network, Passive antenna	48.37	mA

Table 37: BG773A-GL GNSS Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Typ.	Unit
Searching (**AT+CFUN=0**)	Cold start @ Instrument	TBD	mA
	Hot start @ Instrument	TBD	mA
	Lost state @ Instrument	TBD	mA
Tracking (**AT+CFUN=0**)	Instrument environment @ Passive antenna	TBD	mA
	Half sky @ Real network, Passive antenna	TBD	mA

6.5. Digital I/O Characteristic

Table 38: 1.8 V Digital I/O Requirements – (U)SIM

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V

V_{IH}	Input high voltage	1.26	2.0	V
V_{IL}	Input low voltage	-0.2	0.54	V
V_{OH}	Output high voltage	1.44	2.0	V
V_{OL}	Output low voltage	-0.2	0.36	V

Table 39: 1.8 V Digital I/O Requirements – Others

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.26	2.0	V
V_{IL}	Input low voltage	-0.2	0.54	V
V_{OH}	Output high voltage	1.44	2.0	V
V_{OL}	Output low voltage	-0.2	0.36	V

6.6. Tx Power

Table 40: BG770A-GL & BG773A-GL Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17 [15]/B18/ B19/B20/B25/B26 [16]/B27 [16]/B28/B66	23 dBm ±2.7 dB	< -39 dBm

[15] LTE HD-FDD B17 is supported in Cat NB1/Cat NB2 only.
[16] LTE HD-FDD B26 and B27 are supported in Cat M1 only.

6.7. Rx Sensitivity

Table 41: BG770A-GL & BG773A-GL Conducted RF Receiving Sensitivity

Frequency Band	Primary	Diversity	Receiving Sensitivity (dBm)	
			Cat M1/3GPP	Cat NB1[17]/3GPP
LTE HD-FDD B1			-106.6/-102.3	-115.3/-107.5
LTE HD-FDD B2			-106.2/-100.3	-114.3/-107.5
LTE HD-FDD B3			-106.2/-99.3	-114/-107.5
LTE HD-FDD B4			-106.6/-102.3	-114/-107.5
LTE HD-FDD B5			-106.8/-100.8	-115/-107.5
LTE HD-FDD B8			-107/-99.8	-115/-107.5
LTE HD-FDD B12			-106.4/-99.3	-114.3/-107.5
LTE HD-FDD B13			-106.4/-99.3	-114.6/-107.5
LTE HD-FDD B17 [15]	Supported	-	-	-114.6/-107.5
LTE HD-FDD B18			-107.2/-102.3	-115.3/-107.5
LTE HD-FDD B19			-107/-102.3	-115.3/-107.5
LTE HD-FDD B20			-106.6/-99.8	-114.6/-107.5
LTE HD-FDD B25			-106.4/-100.3	-114.3/-107.5
LTE HD-FDD B26 [18]			-107/-100.3	-
LTE HD-FDD B27 [18]			-107.2/-100.8	-
LTE HD-FDD B28			-106.6/-100.8	-114.6/-107.5
LTE HD-FDD B66			-106.8/-101.8	-114.9/-107.5

[17] LTE Cat NB1 receiving sensitivity without repetitions.
[18] LTE HD-FDD B26 and B27 are supported in Cat M1 only.

6.8. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly, and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

The following table shows the electrostatic discharge characteristics of BG770A-GL/BG773A-GL module.

Table 42: Electrostatic Discharge Characteristics (Temperature: 25 ºC, Relative Humidity: 45 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±6	kV
Main/GNSS Antenna Interface	±5	±8	kV

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Top and Side Dimensions

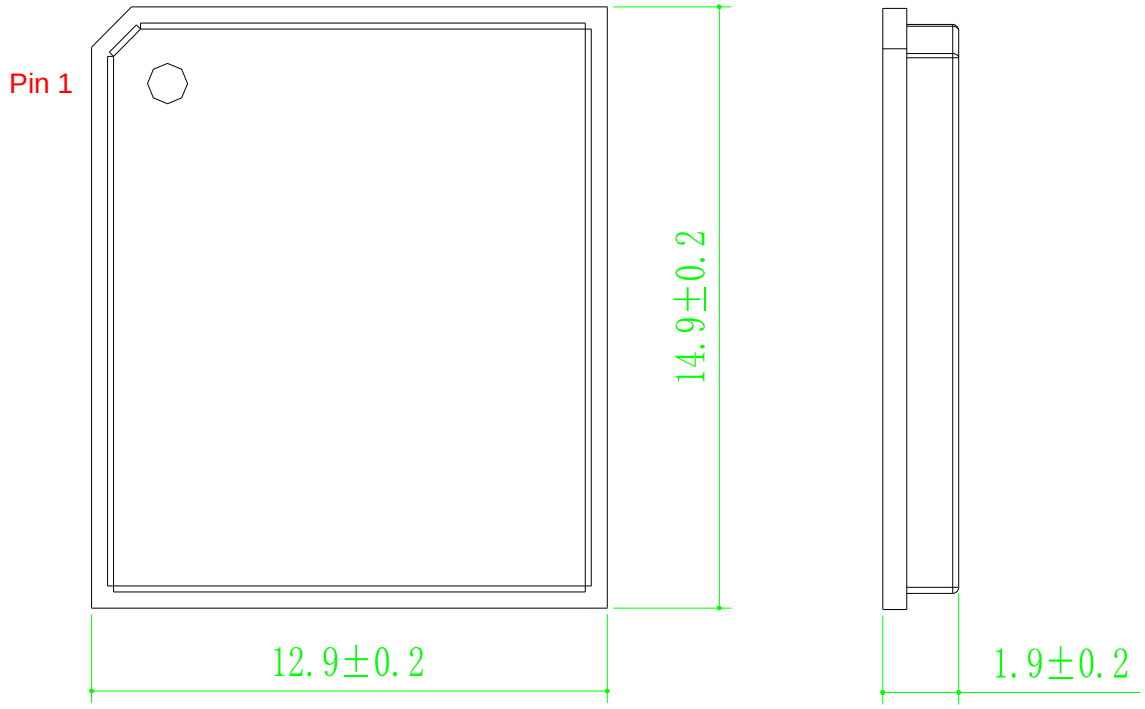


Figure 34: Module Top and Side Dimensions

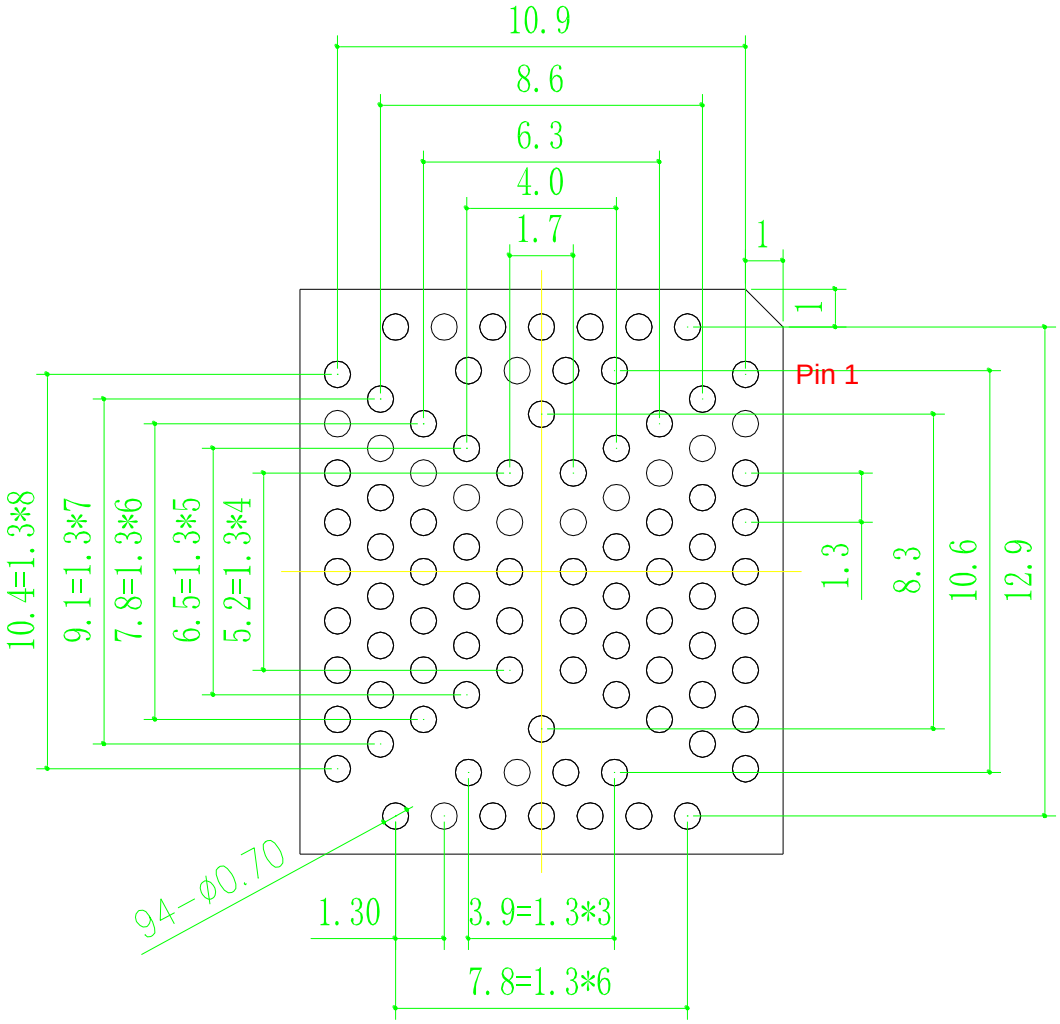


Figure 35: Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

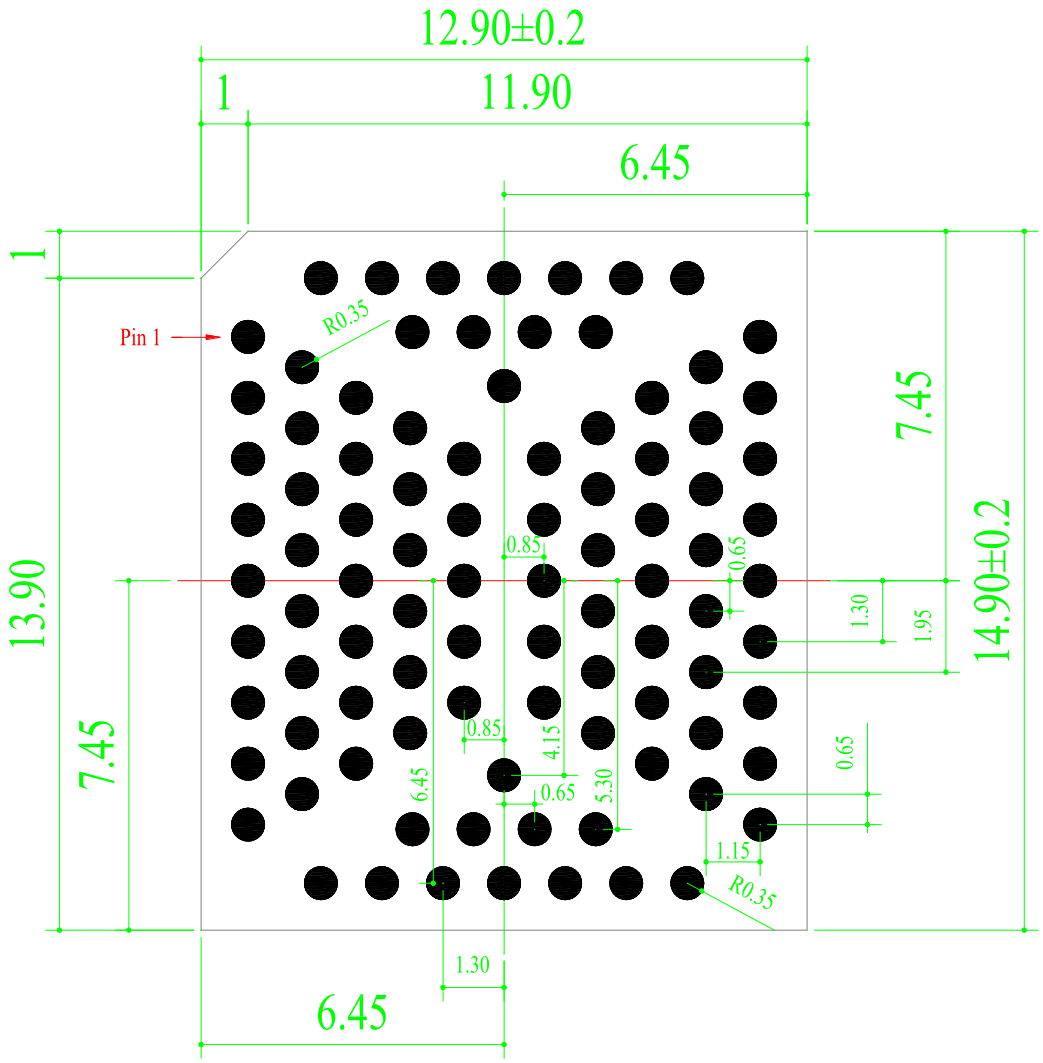


Figure 36: Recommended Footprint (Top View)

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. All RESERVED pins must be kept open.
3. For stencil design requirements of the module, see ***document [7]***.

7.3. Top and Bottom Views

Figure 37: Top and Bottom Views of BG770A-GL and BG773A-GL

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, refer to the module received from Quectel.

8 Storage, Manufacturing and Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [19] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[19] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.10–0.13 mm. For more details, see ***document [7]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

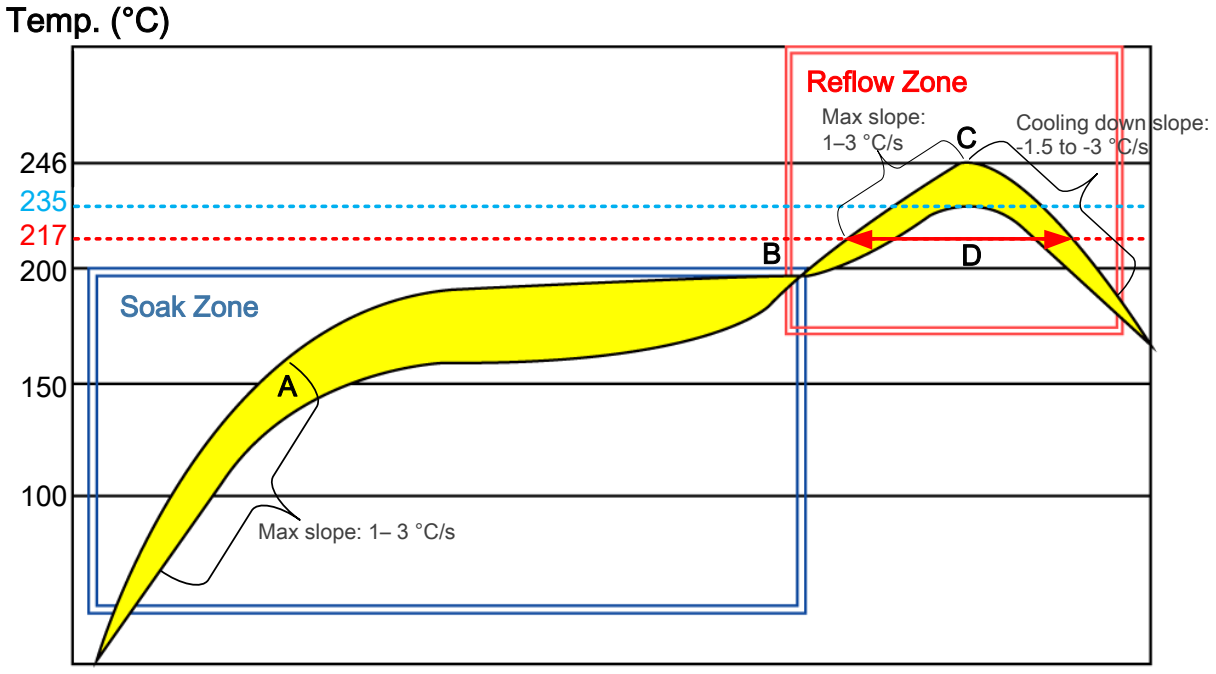


Figure 38: Recommended Reflow Soldering Thermal Profile

Table 43: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to 3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If the module requires conformal coating, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [7]***.

8.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

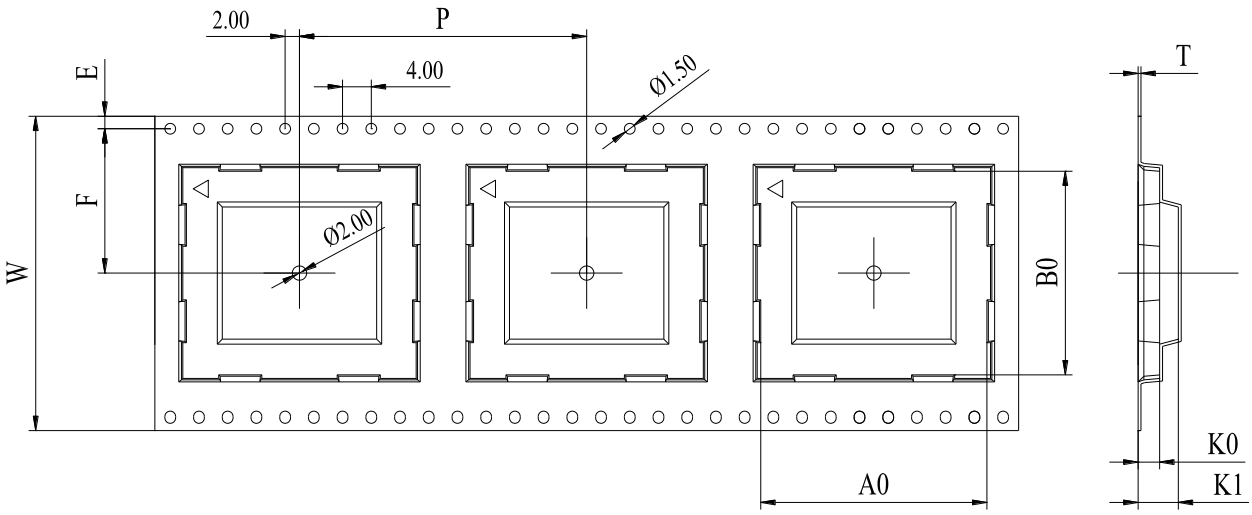


Figure 39: Carrier Tape Dimension Drawing

Table 44: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	20	0.35	13.3	15.3	2.35	5.35	14.2	1.75

8.3.2. Plastic Reel

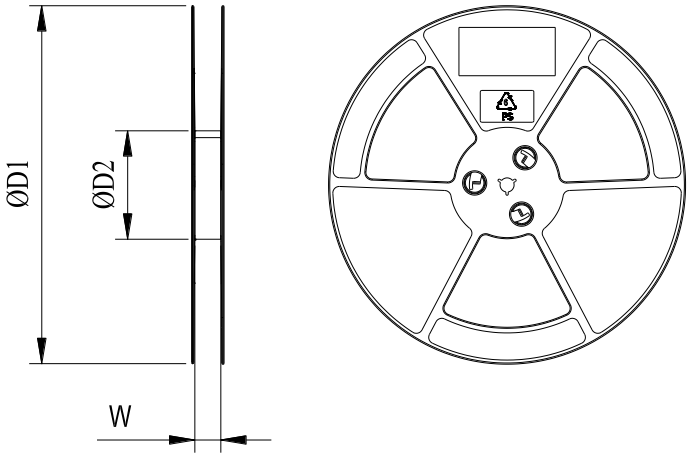
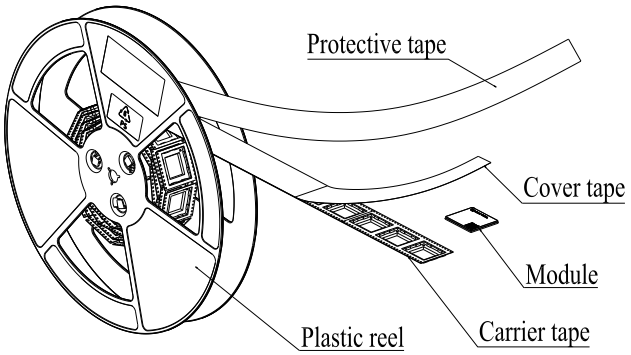


Figure 40: Plastic Reel Dimension Drawing

Table 45: Plastic Reel Dimension Table (Unit: mm)

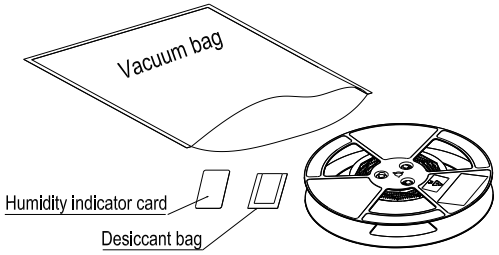
øD1	øD2	W
330	100	32.5

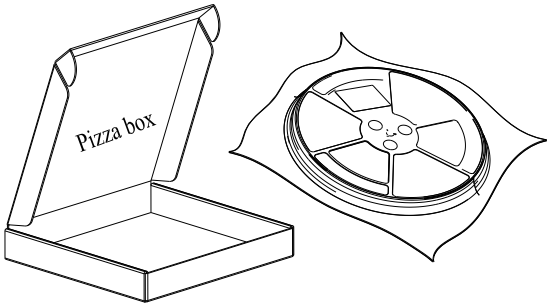
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 500 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 2000 modules.

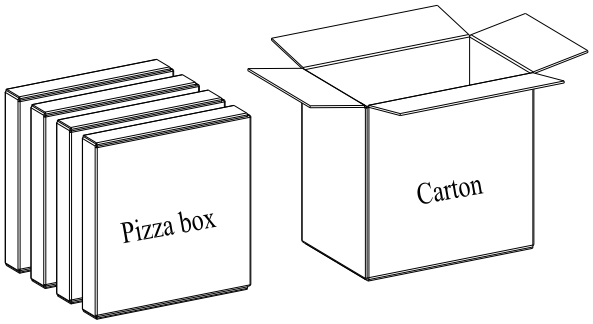


Figure 41: Packaging Process

9 Appendix References

Table 46: Related Documents

Document Name
[1] Quectel_BG770A-GL&BG95xA-GL_GNSS_Application_Note
[2] Quectel_UMTS&LTE_EVB_User_Guide
[3] Quectel_BG770A-GL&BG95xA-GL_QCFG_AT_Commands_Manual
[4] Quectel_BG770A-GL&BG95xA-GL_AT_Commands_Manual
[5] Quectel_BG770A-GL_TE-A_User_Guide
[6] Quectel_RF_Layout_Application_Note
[7] Quectel_Module_Secondary_SMT_Application_Note

Table 47: Terms and Abbreviations

Abbreviation	Description
3GPP	3rd Generation Partnership Project
ADC	Analog to Digital Converter
Balun	Balanced to Unbalanced
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CoAP	Constrained Application Protocol
CTS	Clear to Send
DFOTA	Delta Firmware Upgrade Over the Air
DL	Downlink

DRX	Discontinuous Reception
EGSM	Extended GSM (Global System for Mobile Communications)
e-I-DRX	Extended Idle Mode Discontinuous Reception
EPC	Evolved Packet Core
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplex
FTP(S)	FTP over SSL
GNSS	Global Navigation Satellite System
GLONASS	Global Navigation Satellite System (Russia)
GPIO	General-purpose Input/Output
GPS	Global Positioning System
GRFC	Generic RF Controller
HD	Half Duplex
HSS	Home Subscriber Server
I2C	Inter-Integrated Circuit
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LPWA	Low-Power Wide-Area (Network)
LTE	Long Term Evolution
LwM2M	Lightweight M2M
ME	Mobile Equipment

MLCC	Multi-layer Ceramic Chip
MO	Mobile Originated
MOQ	Minimum Order Quantity
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Levels
MT	Mobile Terminated
NITZ	Network Identity and Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDU	Protocol Data Unit
PHY	Physical
PING	Packet Internet Groper
PMU	Power Management Unit
POS	Point of Sale
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
RTS	Request to Send
SAW	Surface Acoustic Wave

SMD	Surface Mount Device
SMS	Short Message Service
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TDM	Time-division Multiplexing
TLS	Transport Layer Security
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UE	User Equipment
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
VSWR	Voltage Standing Wave Ratio
WWAN	Wireless Wide Area Network