EG92 Series

Hardware Design

LTE Standard Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2023-07-21	Thor LEI/Woping WANG/ Kai YU/Gavin LU	Creation of the document
0.1	2023-07-21	Thor LEI/Woping WANG/ Kai YU/Gavin LU	Draft

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1 Introduction

This document describes the EG92 series module features, performance, and air interfaces and hardware interfaces connected to your applications. The document provides a quick insight into interface specifications, RF performance, electrical and mechanical specifications, and other module information, as well.

This document is applicable to the following modules:

- EG92-EU
- EG92-NA

2 Product Overview

The module is an SMD module with compact packaging, which is engineered to meet most of the demands of M2M and IoT applications, for instance:

- Smart metering
- Wearable devices
- Environmental monitoring
- Asset tracking
- Fleet
- Management
- Security and alarm systems

Table 1: Brief Introduction

Item	Description
Packaging type	LGA
Pin counts	102 pins
Dimensions	(26.5 ±0.2) mm x (22.5 ±0.2) mm x (2.3 ±0.2) mm
Weight	3.8 g
Models	• EG92-EU • EG92-NA

2.1. Frequency Bands and Functions

Table 2: Frequency Bands and Functions

Technology	EG92-EU	EG92-NA
LTE-FDD	B1/B3/B7/B8/B20/B28	B2/B4/B5/B12/B13/B66/B71
WCDMA	B1/B8	-
GSM	EGSM900/DCS1800	-
GNSS	GPS, GLONASS, BDS, Galileo, QZSS	

2.2. Key Features

Table 3: Key Features

Feature	Capability
Supply Voltage	● 3.3–4.3 V ● Typ.: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USB Interface	● One USB interface ● Complies with USB 2.0 specification (slave mode only) ● Data rate: up to 480 Mbps ● Use: AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade and voice over USB ● USB serial drivers under Windows 7/8/8.1/10/11, Linux 2.6–6.5 and Android 4.x–13.x systems
(U)SIM Interfaces	1.8 V and 3.0 V
UARTs	● Two UART **Main UART:** ● Use: AT command communication and data transmission ● Baud rate: 921600 bps ● RTS and CTS hardware flow control **Debug UART:**

	● Use: Linux console and log output ● Baud rate: 115200 bps
Audio Features	● One digital audio interface ● GSM: HR, FR, EFR, AMR and AMR-WB ● WCDMA: AMR and AMR-WB ● LTE: AMR and AMR-WB ● Echo cancellation and noise suppression
PCM Interface	● Use: audio data transmission between the module and the external codec ● 16-bit linear data format ● Long and short frame synchronization ● Master and slave modes (but must be in master mode for long frame synchronization)
SPI	● One SPI ● Master mode only ● One-to-one connection, without chip selection ● Clock rate: up to 50 MHz
Network Indication	**NET_STATUS:** ● Use: network connectivity status indication
AT Commands	● Complies with the AT commands defined in *3GPP TS 27.007* and *3GPP TS 27.005* ● Complies with Quectel enhanced AT commands
Rx-diversity	LTE and WCDMA Rx-diversity
Antenna Interfaces	● One main antenna interface (ANT_MAIN) ● One Rx-diversity antenna interface (ANT_DRX) ● One GNSS antenna interface (ANT_GNSS) ● 50 Ω characteristic impedance
Transmitting Power	● LTE-FDD: Class 3 (23 dBm ±2 dB) ● WCDMA: Class 3 (23 dBm ±2 dB) ● DCS1800 8-PSK: Class E2 (26 dBm ±3 dB) ● EGSM900 8-PSK: Class E2 (27 dBm ±3 dB) ● DCS1800: Class 1 (30 dBm ±2 dB) ● EGSM900: Class 4 (33 dBm ±2 dB)
LTE Features	● Complies with 3GPP Rel-8 specification ● Max. LTE category: Cat 1 ● 1.4/3/5/10/15/20 MHz RF bandwidths ● Modulations: – DL: QPSK, 16QAM and 64QAM – UL: QPSK, 16QAM ● LTE-FDD max. data rates: 10 Mbps (DL)/5 Mbps (UL)
UMTS Features	● Complies with 3GPP Rel-8 specification ● DC-HSDPA, HSPA+, HSDPA, HSUPA and WCDMA ● Modulations: QPSK, 16QAM and 64QAM ● Max. data rates:

	– DC-HSDPA: 42 Mbps (DL) – HSUPA: 5.76 Mbps (UL) – WCDMA: 384 kbps (DL/UL)
GSM Features	**GPRS:** ● GPRS multi-slot class 33 (33 by default) ● Coding scheme: CS 1–4 ● Max. data rates: 107 kbps (DL)/85.6 kbps (UL) **EDGE:** ● EDGE multi-slot class 33 (33 by default) ● Coding scheme: GMSK and 8-PSK ● DL coding schemes: MCS 1–9 ● UL coding schemes: MCS 1–9 ● Max. data rates: 296 kbps (DL)/236.8 kbps (UL)
GNSS Features	● GPS, GLONASS, BDS, Galileo and QZSS ● Complies with NMEA 0183 protocol ● The data update rate is 1 Hz by default and 10 Hz maximally
Internet Protocol Features	● Complies with TCP, UDP, PPP, NTP, NITZ, FTP, HTTP, PING, QMI, CMUX, HTTPS, FTPS, SSL, FILE, MQTT, MMS, SMTP and SMTPS protocols ● PAP and CHAP for PPP connections
Temperature Ranges	● Normal operating temperature [1]: -35 °C to +75 °C ● Extended operating temperature [2]: -40 °C to +85 °C ● Storage temperature: -40 °C to +90 °C
Firmware Upgrade	● USB 2.0 interface ● DFOTA
RoHS	All hardware components are fully Complies with EU RoHS directive

[1] Within this range, the module's performance complies with 3GPP requirements.
[2] Within this range, the module retains the ability to establish and maintain functions such as voice and SMS, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's performance will comply with 3GPP requirements again.

2.3. Pin Description

Table 4: Parameter Definition

Parameters	Descriptions
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current, etc.

Table 5: Pin Definition

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
VBAT_BB	32, 33	PI	Power supply for the module's BB part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A. A test point is recommended to be reserved.
VBAT_RF	52, 53	PI	Power supply for the module's RF part		It must be provided with sufficient current up to 1.8 A in a burst transmission. A test point is recommended to be reserved.
VDD_EXT	29	PO	Provide 1.8 V for	Vnom = 1.8 V	Power supply for

			external circuit	$I_O$max = 50 mA	external GPIO's pull-up circuits. A test point is recommended to be reserved.
GND	3, 31, 47, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
PWRKEY	15	DI	Turn on/off the module		The output voltage is 0.8 V because of the diode drop in the baseband chipset. A test point is recommended to be reserved.
RESET_N	17	DI	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	1.8 V power domain. A test point is recommended to be reserved if unused.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
STATUS	20	DO	Indicate the module's operation status	VDD_EXT	If unused, keep it open.
NET_STATUS	21	DO	Indicate the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.0 V Vnom = 5.0 V	A test point must be reserved.
USB_DP	9	AIO	USB 2.0 differential data (+)		Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB 2.0 differential data (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**

				$I_O$max = 50 mA **Low-voltage:** Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.7 V **High-voltage:** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V	
USIM1_VDD	43	PO	(U)SIM1 card power supply		Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	DIO	(U)SIM1 card data	USIM1_VDD	
USIM1_CLK	46	DO	(U)SIM1 card clock		
USIM1_RST	44	DO	(U)SIM1 card reset		
USIM1_DET	42	DI	(U)SIM1 card hot-plug detect	VDD_EXT	If unused, keep it open.
				$I_O$max = 50 mA **Low-voltage:** Vmax = 1.9 V Vnom = 1.8 V Vmin = 1.7 V **High-voltage:** Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V	
USIM2_VDD	87	PO	(U)SIM2 card power supply		Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_DATA	86	DIO	(U)SIM2 card data	USIM2_VDD	If unused, keep them open.
USIM2_CLK	84	DO	(U)SIM2 card clock		
USIM2_RST	85	DO	(U)SIM2 card reset		
USIM2_DET	83	DI	(U)SIM2 card hot-plug detect	VDD_EXT	
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
MAIN_CTS	36	DO	Clear to send signal to the module	VDD_EXT	If unused, keep it open. Connect to the MCU's CTS.
MAIN_RTS	37	DI	Request to send signal		If unused, keep it open.

			from the module		Connect to the MCU's RTS.
MAIN_RXD	34	DI	Main UART receive		If unused, keep them open.
MAIN_DCD	38	DO	Main UART data carrier detect		
MAIN_TXD	35	DO	Main UART transmit		
MAIN_RI	39	DO	Main UART ring indication		
MAIN_DTR	30	DI	Main UART data terminal ready		Pulled up by default. The pin can wake up the module in the low level. If unused, keep it open.
Debug UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
DBG_RXD	22	DI	Debug UART receive	VDD_EXT	Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
I2C_SCL	40	OD	I2C serial clock (for external codec)	VDD_EXT	Externally pulled up to 1.8 V. If unused, keep them open.
I2C_SDA	41	OD	I2C serial data (for external codec)		
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
PCM_SYNC	5	DIO	PCM data frame sync	VDD_EXT	Master mode: output. Slave mode: input. If unused, keep it open.
PCM_CLK	4	DIO	PCM clock		
PCM_DIN	6	DI	PCM data input		If unused, keep them open.
PCM_DOUT	7	DO	PCM data output		
RF Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface		50 Ω impedance.

ANT_DRX	56	AI	Diversity antenna interface		50 Ω impedance. If unused, keep them open.
ANT_GNSS	49	AI	GNSS antenna interface		
Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
GRFC1	76	DO	Generic RF Controller		If unused, keep them open.
GRFC2	77	DO	Generic RF Controller		
SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
SPI_CLK	26	DO	SPI clock	VDD_EXT	Master mode only. If unused, keep them open.
SPI_DIN	28	DI	SPI data input		
SPI_DOUT	27	DO	SPI data output		
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0.3 V to VBAT_BB	If unused, keep it open.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristic**	**Comment**
USB_BOOT	75	DI	Force the module into emergency download mode	VDD_EXT	Cannot be pulled up before startup. A test point is recommended to be reserve.
W_DISABLE#	18	DI	Airplane mode control		Pulled up by default. If unused, keep it open.
AP_READY	19	DI	Application processor ready		If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**				
RESERVED	1, 2, 11–14, 16, 25, 51, 57, 63–66, 78, 88, 92–99				

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. BOOT_CONFIG pins (SPI_CLK, USB_BOOT, PCM_CLK, PCM_SYNC, GRFC1) cannot be pulled up before startup.

2.4. EVB Kit

Quectel supplies an evaluation board (UMTS&LTE EVB) with accessories to develop or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 6: Operating Modes Overview

Modes	Descriptions	
Full Functionality Mode	Idle	The module remains registered on the network but has no data interaction with the network. In this mode, the software is active.
	Voice/Data	The module is connected to the network. In this mode, the power consumption is decided by network settings and data rates.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to the minimum functionality mode without removing the power supply. In this mode, both (U)SIM card and RF function are disabled.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# can set the module to airplane mode. In this mode, RF function is disabled and all relevant AT commands are inaccessible.	
Sleep Mode	The module can still receive paging, SMS, voice call and TCP/UDP data from the network. In this mode, the power consumption is minimized.	
Shutdown Mode	PMU shuts down the power supply. In this mode, software is not active. However, the voltage supply (for VBAT_RF and VBAT_BB) remains connected.	

NOTE

For more details about **AT+CFUN**, see ***document [2]***.

3.2. Sleep Mode

With DRX technology, power consumption of the module will be reduced to a minimal level.

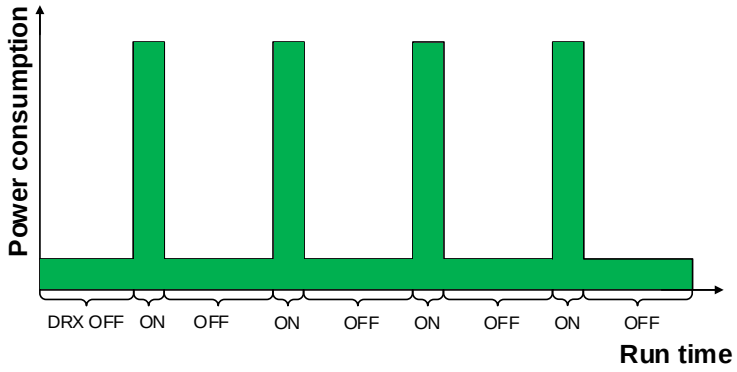


Figure 1: Module Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.2.1. UART Application Scenario

If the module communicates with the MCU via main UART, both the following preconditions should be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.

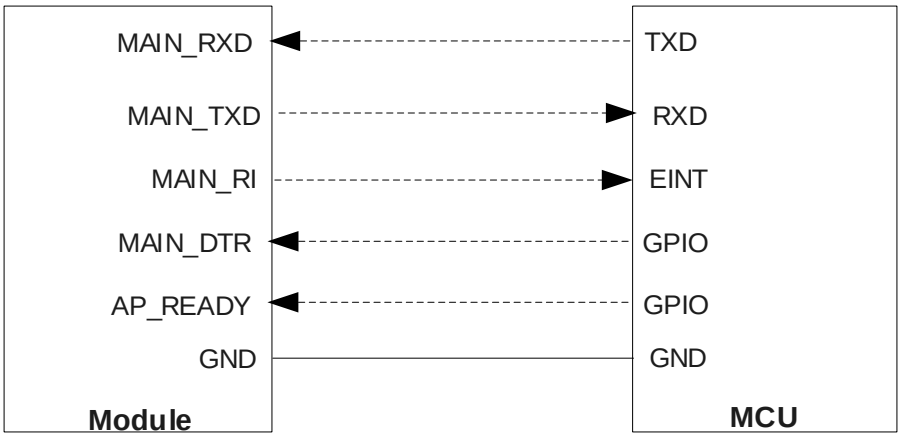


Figure 2: Block Diagram of UART Application in Sleep Mode

- Drive MAIN_DTR low with the MCU will wake up the module.
- When the module has a URC to report, MAIN_RI signal will wake up the MCU. See ***Chapter 4.8.3*** for details about MAIN_RI.

3.2.2. USB Application Scenarios

For the two situations ('USB application with USB remote wakeup function' and USB application with USB suspend/resume and RI function') below, three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure the host's USB bus, which is connected to the module's USB interface, enters suspend state.

Sending data to the module through USB will wake up the module.

3.2.2.1. USB Application with USB Suspend/Resume and USB Remote Wakeup Function

The host supports USB suspend/resume and remote wakeup function.

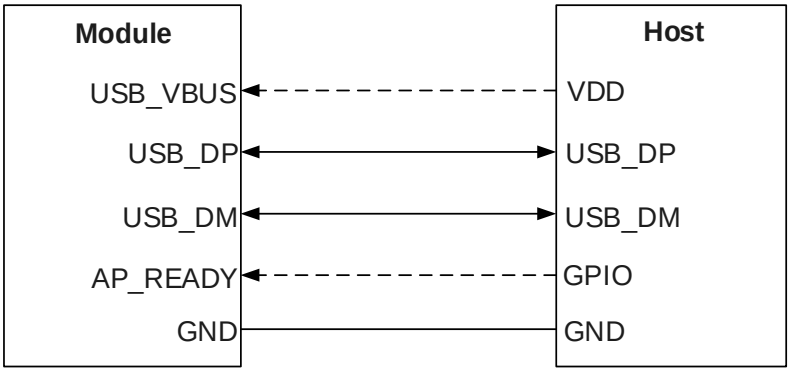


Figure 3: Block Diagram of Application with USB Remote Wakeup Function in Sleep Mode

When the module has a URC to report, the module will send remote wake-up signals through USB bus to wake up the host.

3.2.2.2. USB Application with USB Suspend/Resume and RI Function

If the host supports USB suspend/resume, but does not support remote wakeup function, the MAIN_RI signal is needed to wake up the host.

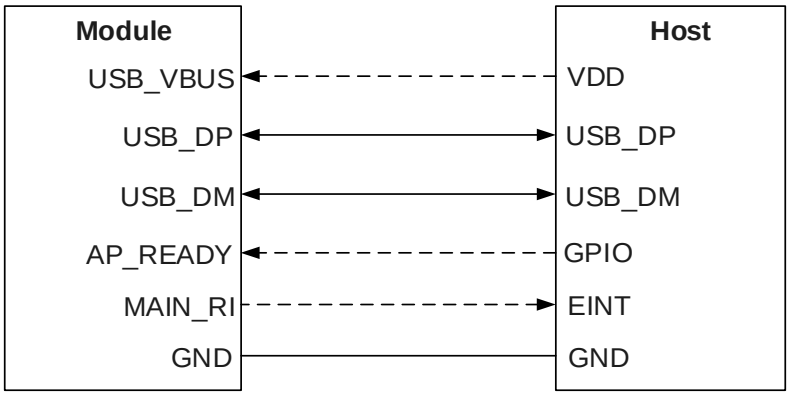


Figure 4: Block Diagram of Application with RI Function in Sleep Mode

When the module has a URC to report, the module will wake up the host through MAIN_RI signal.

3.2.2.3. USB Application without USB Suspend Function

If the host does not support USB suspend function, the following three preconditions must be met to set the module to sleep mode:

- Execute **AT+QSCLK=1**.
- Ensure MAIN_DTR is held high or is kept unconnected.
- Ensure USB_VBUS is disconnected via the external control circuit.

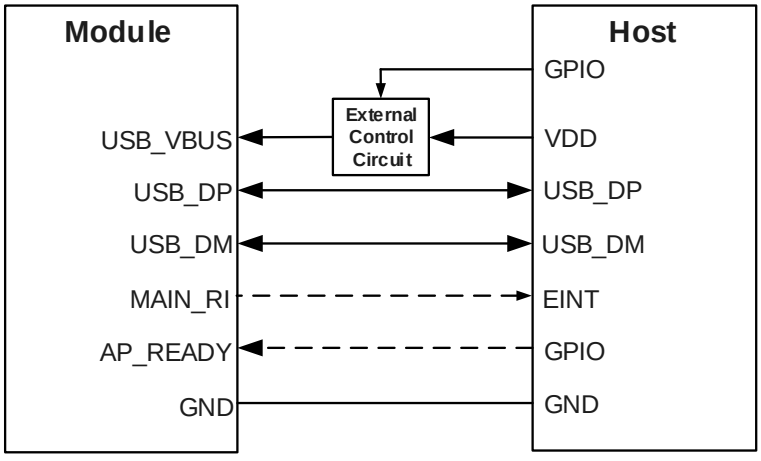


Figure 5: Block Diagram of Application without USB Suspend Function in Sleep Mode

Restore the power supply of USB_VBUS will wake up the module.

NOTE

1. Pay attention to the level match shown in the dotted line between the module and the host. See ***document [4]*** for more details about EG92 series module power management application.
2. For details of **AT+QSCLK**, see ***document [2]***.

3.3. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. The following ways can be used to let the module enter airplane mode.

Hardware:

The W_DISABLE# pin is pulled up by default. Its control function for airplane mode is disabled by default, and **AT+QCFG="airplanecontrol",1** can be used to enable the function. Driving the pin low after its control function for airplane mode is enabled by AT command, which can make the module enter the airplane mode.

Software:

AT+CFUN=<fun> provides the choice of the functionality level through setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality mode (disable (U)SIM and RF functions).
- **AT+CFUN=1:** Full functionality mode (by default).
- **AT+CFUN=4:** Airplane mode (disable RF function).

NOTE

1. The execution of **AT+CFUN** does not affect GNSS function.
2. For details of **AT+QCFG**, see ***document [3]***.

3.4. Power Supply

3.4.1. Power Supply Interface

The module has four VBAT pins dedicate to connecting with the external power supply.

Table 7: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32, 33	Power supply for the module's BB part	3.3	3.8	4.3	V
VBAT_RF	52, 53	Power supply for the module's RF part	3.3	3.8	4.3	V
GND	3, 31, 47, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102					

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power supply design. The power supply of the module should be able to provide sufficient current of 2.0 A at least. If the voltage difference between input voltage and the supply voltage is small, it is suggested to use an LDO; if the voltage difference is big, a buck converter is recommended.

The following figure shows a reference design for +5 V input power supply. The designed output of the power supply is about 3.8 V.

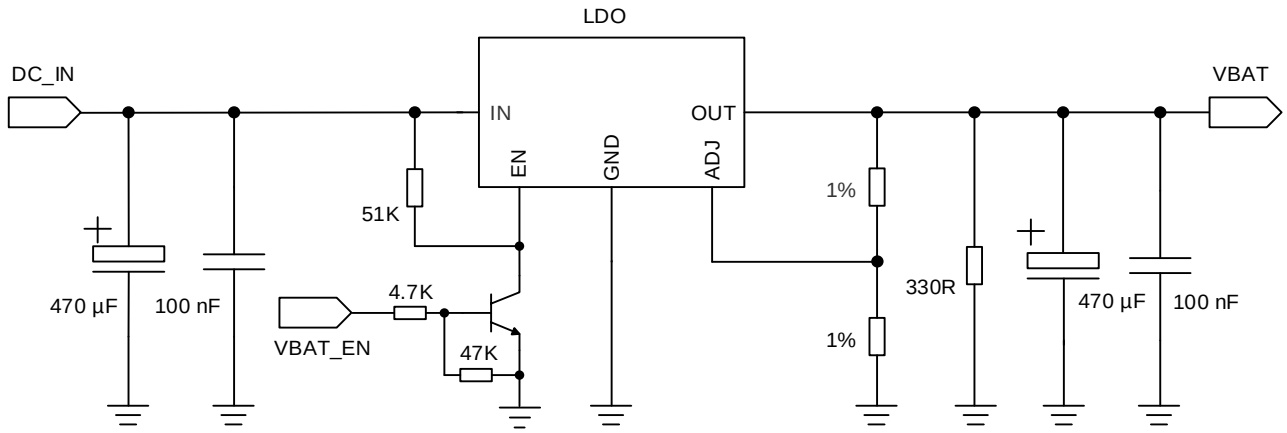


Figure 6: Reference Design of Power Input

NOTE

To avoid corrupting the data in the internal flash, do not cut off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.

3.4.3. Requirements for Voltage Stability

The power supply range of the module is from 3.3 V to 4.3 V. Ensure the input voltage never drops below 3.3 V.

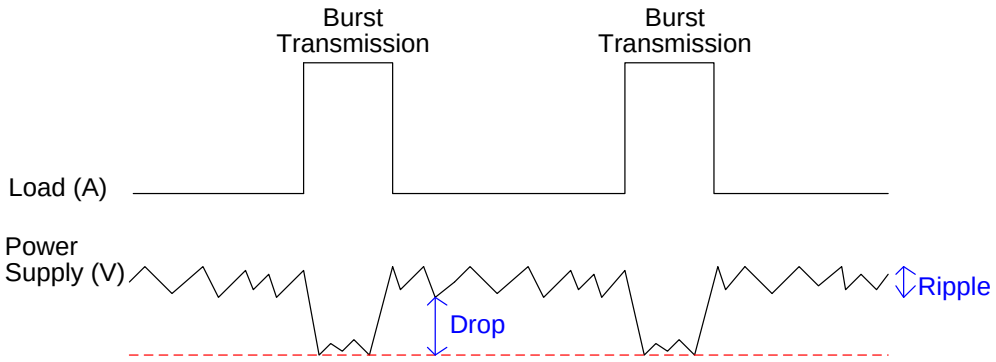
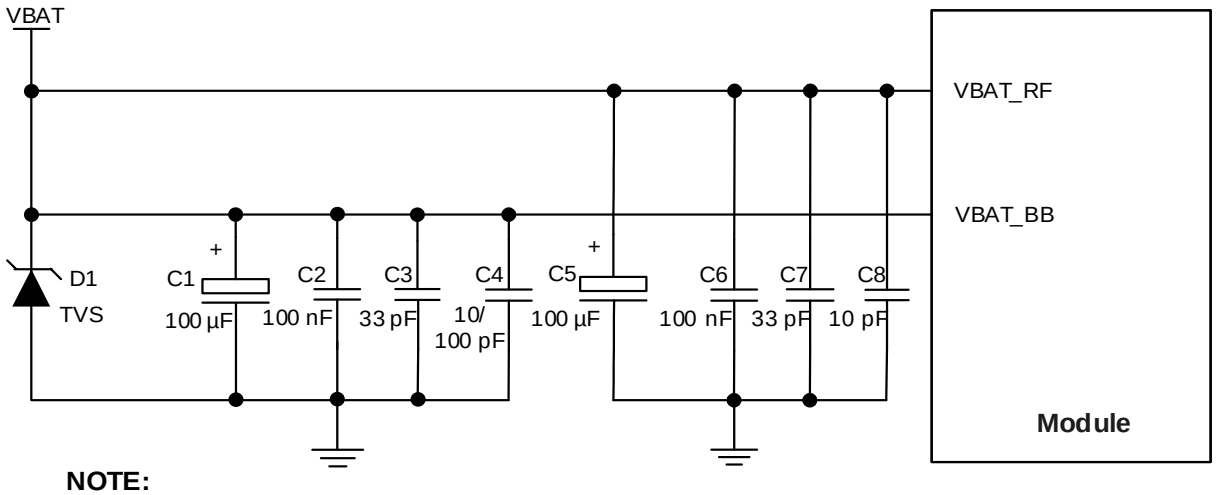


Figure 7: Power Supply Limits During Burst Transmission

To decrease the voltage drop, use a bypass capacitor of about 100 μF with low ESR (ESR ≤ 0.7 Ω), and reserve a multi-layer ceramic chip (MLCC) capacitor array with ultra-low ESR. Use three ceramic capacitors (100 nF, 33 pF, 10/100 pF [3] for VBAT_BB and 100 nF, 33 pF, 10 pF for VBAT_RF) for composing the MLCC array, and place these capacitors close to the VBAT pins. The main power supply from an external application should be a single voltage source and can be expanded to two sub paths routed as the star configuration. The width of VBAT_BB trace and VBAT_RF trace should be at least 1 mm and 2 mm respectively. As per design rules, the longer the VBAT trace is, the wider it should be.

To avoid the ripple and surge and ensure the stability of the power supply to the module, add a TVS component with VRWM = 4.5 V, low clamping V_c and high reverse peak pulse current I_{pp} near the power supply.

[3] For EG92-EU, the capacitance value is 10 pF. For EG92-NA, the capacitance value is 100 pF.



NOTE:
For EG92-EU, the capacitance value of C4 is 10 pF.
For EG92-NA, the capacitance value of C4 is 100 pF.

Figure 8: Reference Design of Power Supply

3.4.4. Power Supply Voltage Monitoring

You can use **AT+CBC** to monitor and query the VBAT_BB voltage. For details, see ***document [2]***.

3.5. Turn-On

3.5.1. Turn-On with PWRKEY

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	The output voltage is 0.8 V because of the diode drop in the baseband chipset. A test point is recommended to be reserved.

When the module is in turn-off state, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control the PWRKEY. After STATUS outputs high-level voltage, the PWRKEY can be released.

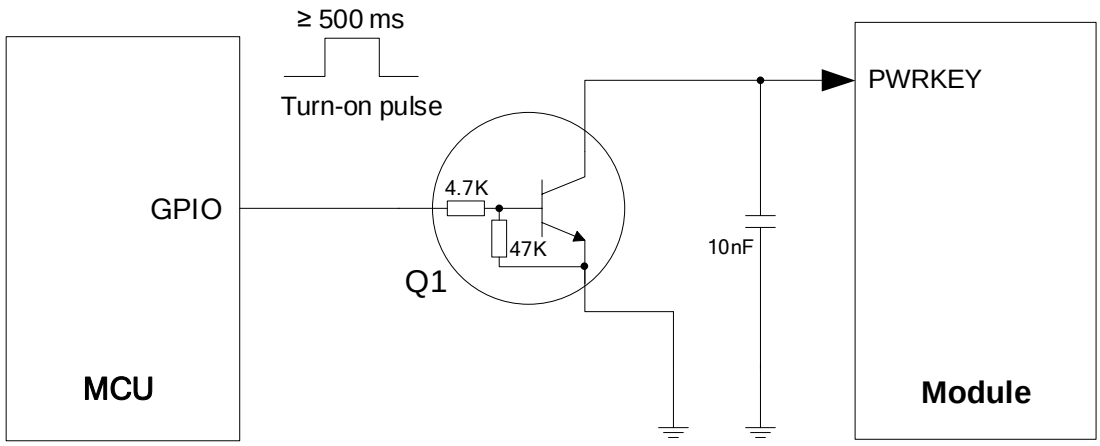


Figure 9: Reference Design of Turn-On with Driving Circuit

The module can also be turned on by pressing the PWRKEY button. A ESD component should be placed near the button for protection against ESD, since static electricity may be generated by the finger touching.

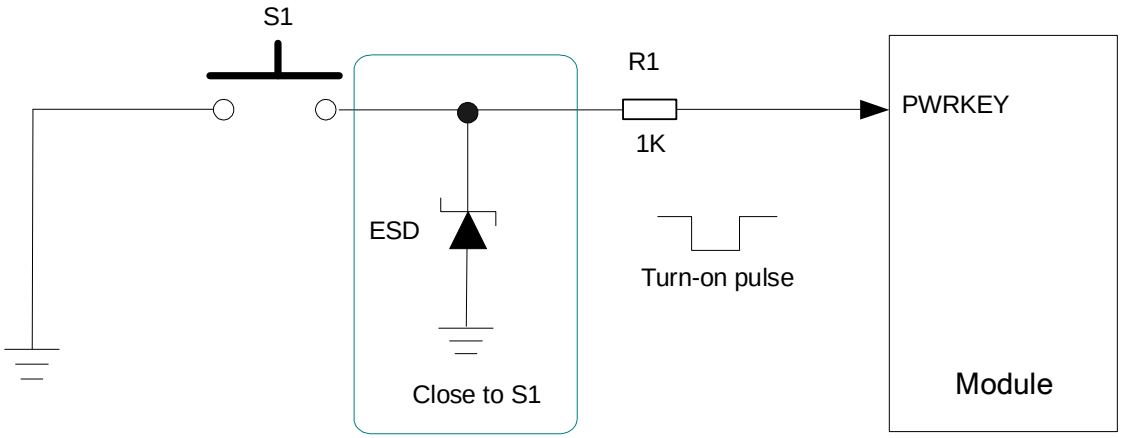


Figure 10: Reference Design of Turn-On with Keystroke

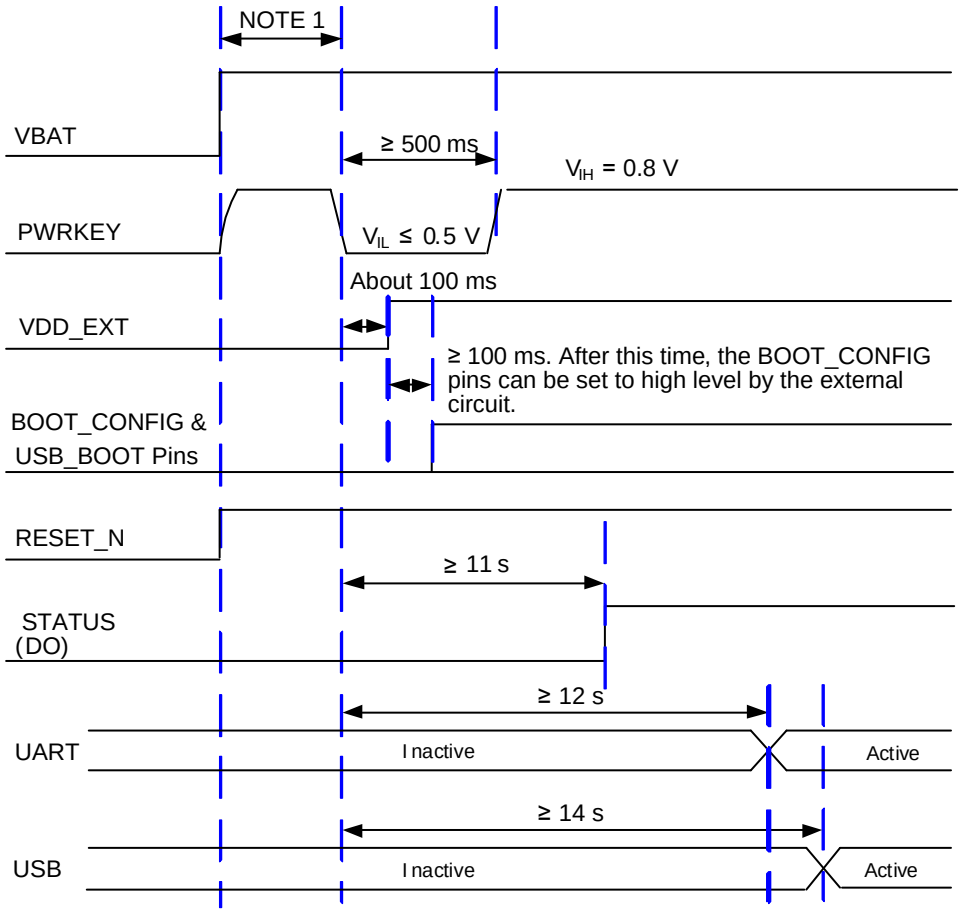


Figure 11: Timing of Turn-On with PWRKEY

NOTE

1. Ensure that VBAT is stable for at least 30 ms before driving the PWRKEY low.
2. If the module needs to turn on automatically but does not need turn-off function, PWRKEY can be driven low directly to ground with a recommended 10 kΩ resistor.
3. BOOT_CONFIG pins (SPI_CLK, USB_BOOT, PCM_CLK, PCM_SYNC, GRFC1) cannot be pulled up before startup.

3.6. Turn-Off

3.6.1. Turn-Off with PWRKEY

Drive PWRKEY low for at least 650 ms and then release it to turn off the module.

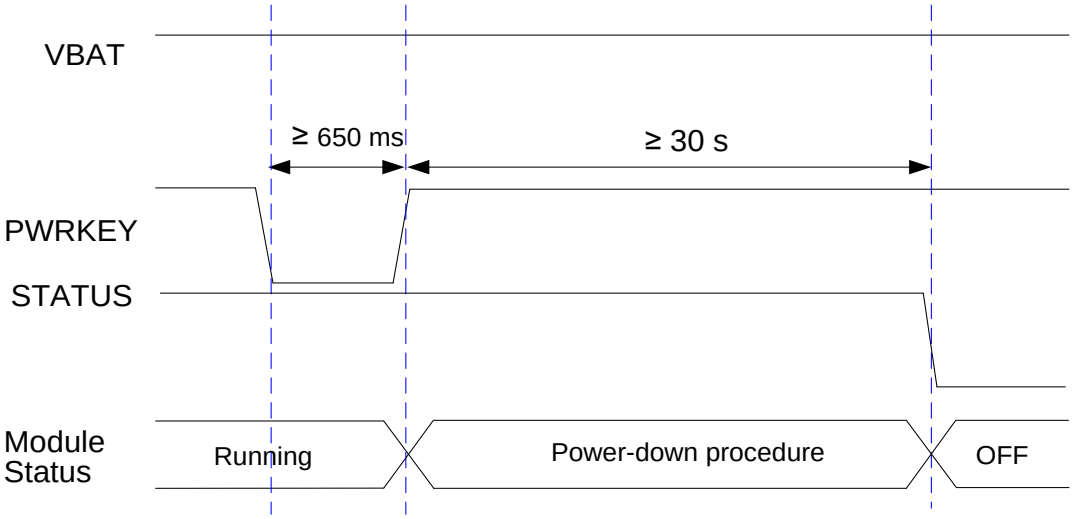


Figure 12: Timing of Turn-Off with PWRKEY

3.6.2. Turn-Off with AT Command

To turn off the module, you can also execute **AT+QPOWD**, which has similar timing and effect as turning off the module through driving PWRKEY low. See ***document [2]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply to turn off the module when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off the module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise, the module will be turned on automatically again after successful turn-off.

3.7. Reset

Drive RESET_N low for at least 150-460 ms and then release it to reset the module. RESET_N signal is sensitive to interference, consequently it is recommended to route the trace as short as possible and surround it with ground.

Table 9: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	17	DI	Reset the module	1.8 V power domain. A test point is recommended to be reserved if unused.

The recommended circuit for reset function is similar to the PWRKEY control circuit. You can use an open drain/collector driver or a button to control RESET_N.

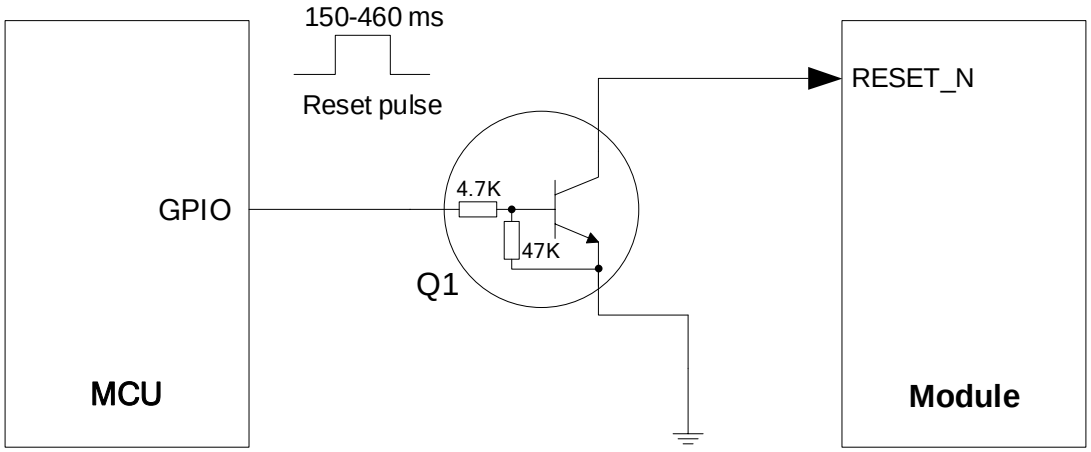


Figure 13: Reference Design of Reset with Driving Circuit

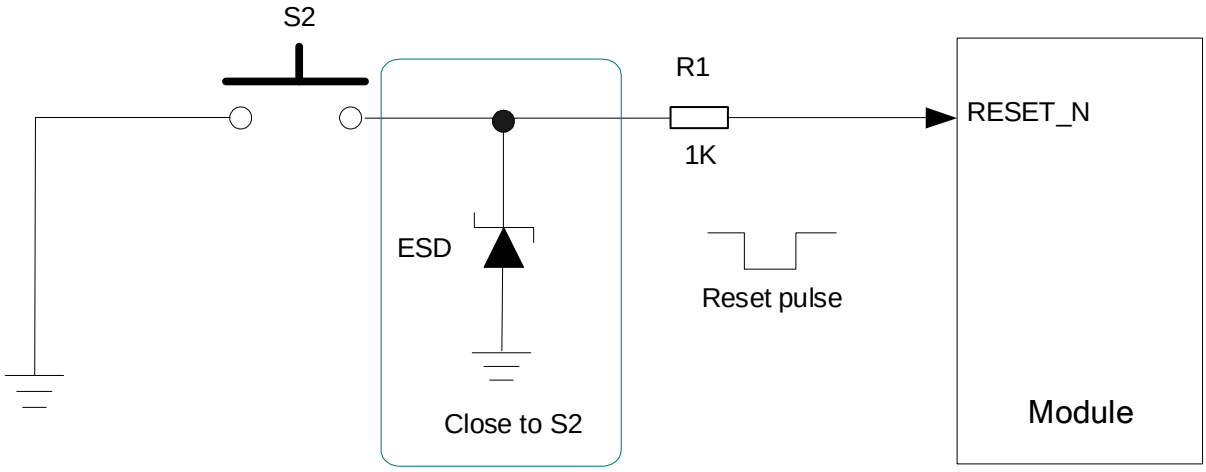


Figure 14: Reference Design of Reset with Button

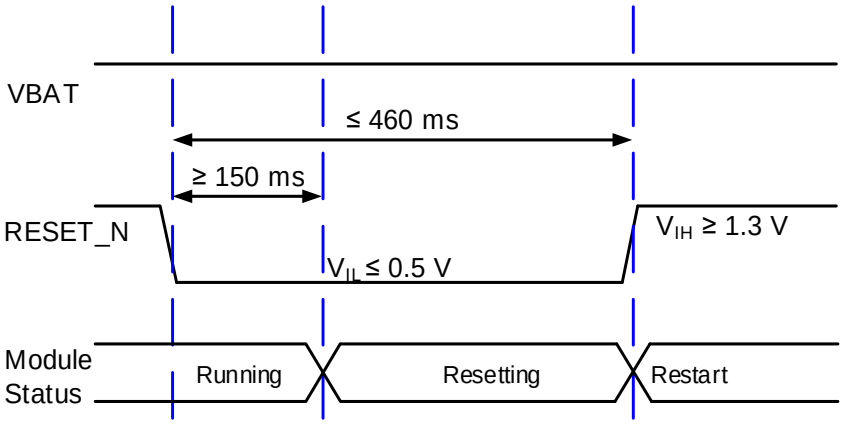


Figure 15: Timing of Reset

NOTE

1. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
2. Ensure the capacitance on PWRKEY and RESET_N is no more than 10 nF.

4 Application Interfaces

4.1. USB Interface

The module contains one integrated Universal Serial Bus (USB) interface which complies with the USB 2.0 specification and supports high-speed (480 Mbps) and full-speed (12 Mbps) modes. The USB interface can only serve as the slave device.

USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output,
software debugging, firmware upgrade and voice over USB.

Table 10: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Test point must be reserved.
USB_DP	9	AIO	USB 2.0 differential data (+)	Require differential impedance of 90 Ω. Test points must be reserved.
USB_DM	10	AIO	USB 2.0 differential data (-)	

USB 2.0 interface can be used for firmware upgrade and test points must be reserved for debugging in your designs.

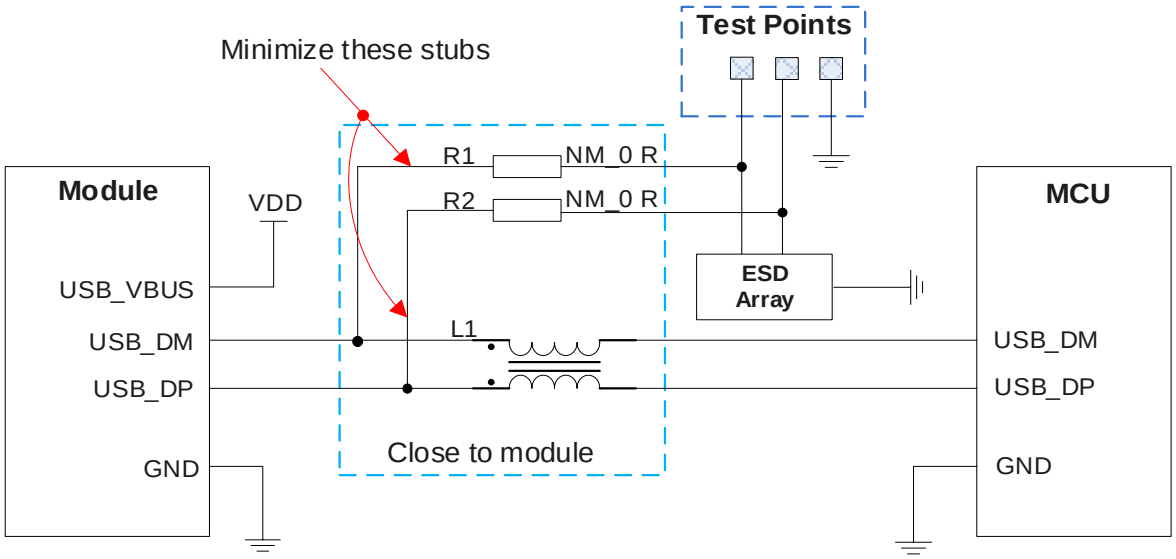


Figure 16: Reference Design of USB Interface

It is recommended to add a common-mode choke L1 in series between MCU and the module to suppress EMI spurious transmission. Meanwhile, it is also suggested to add R1 and R2 in series between the module and test points for debugging. These resistors are not mounted by default. To ensure the signal integrity of USB 2.0 data transmission, you should place L1, R1 and R2 close to the module, and keep these resistors close to each other. Moreover, keep extra stubs of trace as short as possible.

To ensure performance, you should follow the following principles when designing USB interface:

- Route USB signal traces as differential pairs with surrounded ground. The impedance of USB differential trace is 90 Ω.
- Route USB differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Pay attention to the impact caused by stray capacitance of the ESD protection component on USB data lines. Typically, the stray capacitance should be less than 2 pF for USB .
- If possible, reserve two 0 Ω resistors on USB_DP and USB_DM traces respectively.

For more details about the USB specifications, visit http://www.usb.org/home.

4.2. USB_BOOT

The module has a USB_BOOT for emergency download. Pulling up USB_BOOT to VDD_EXT before turning on the module, and then the module will enter emergency download mode. In this mode, the module supports firmware upgrade over USB interface.

Table 11: Pin Definition of USB_BOOT

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	75	DI	Force the module into emergency download mode	Cannot be pulled up before startup. A test point is recommended to be reserve.

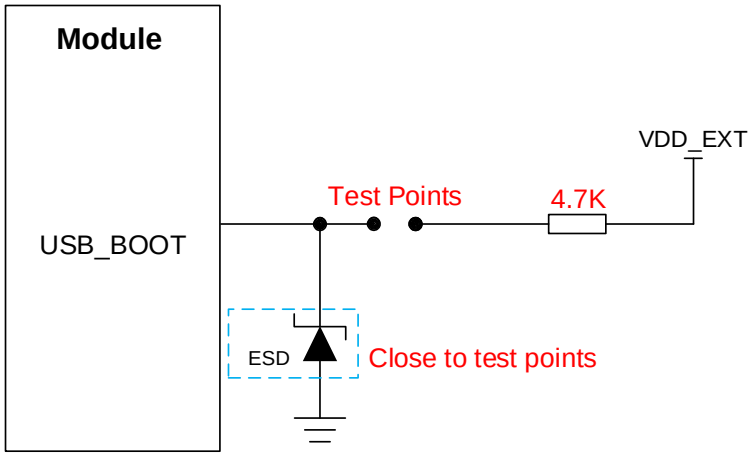


Figure 17: Reference Design of USB_BOOT

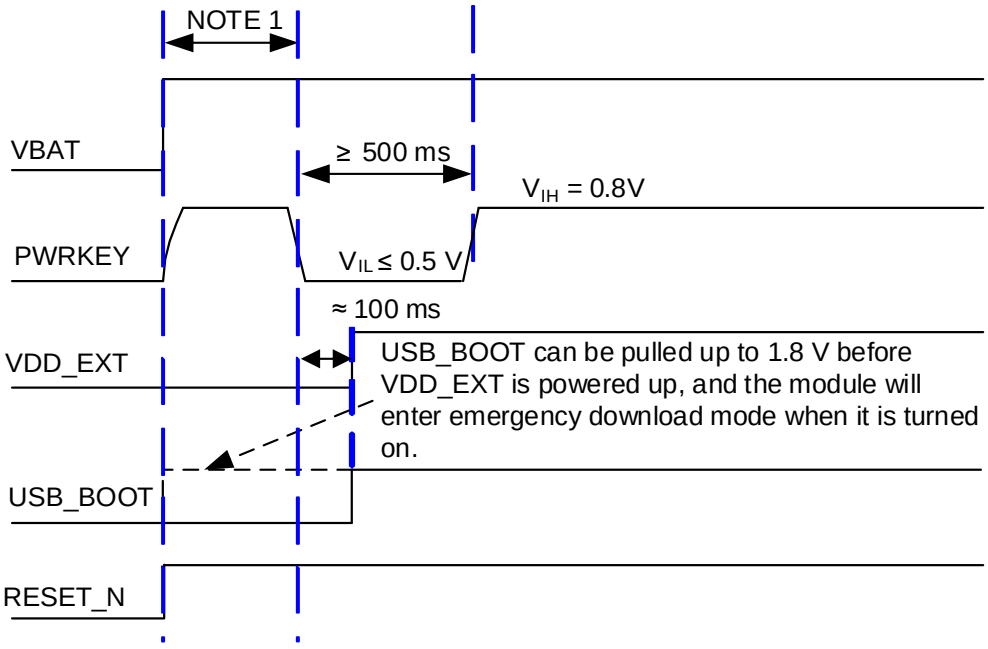


Figure 18: Timing of Entering Emergency Download Mode

NOTE

1. Ensure VBAT is stable before driving PWRKEY low. The time period between powering VBAT up and driving PWRKEY low shall be at least 30 ms.
2. Follow the above timing when using MCU control the module to enter the emergency download mode. Do not pull up USB_BOOT to 1.8 V before powering up VBAT.
3. If you need to manually force the module to enter emergency download mode, directly connect the test points shown in ***Figure 17***.

4.3. (U)SIM Interface

The (U)SIM interface meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported. and only one (U)SIM card can work at a time. The (U)SIM1 and (U)SIM2 cards can be switched by **AT+QDSIM**. For more details, see ***document [5]***.

Table 12: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	43	PO	(U)SIM1 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	45	DIO	(U)SIM1 card data	
USIM1_CLK	46	DO	(U)SIM1 card clock	
USIM1_RST	44	DO	(U)SIM1 card reset	
USIM1_DET	42	DI	(U)SIM1 card hot-swap detect	If unused, keep it open.
USIM2_VDD	87	PO	(U)SIM2 card power supply	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM2_DATA	86	DIO	(U)SIM2 card data	If unused, keep them open.
USIM2_CLK	84	DO	(U)SIM2 card clock	
USIM2_RST	85	DO	(U)SIM2 card reset	
USIM2_DET	83	DI	(U)SIM2 card detect	If unused, keep it open.

The module supports (U)SIM card hot-swap via the USIM_DET, and both high-level and low-level detections are supported. Hot-swap function is disabled by default and you can use **AT+QSIMDET** to

configure this function. See ***document [2]*** for more details.

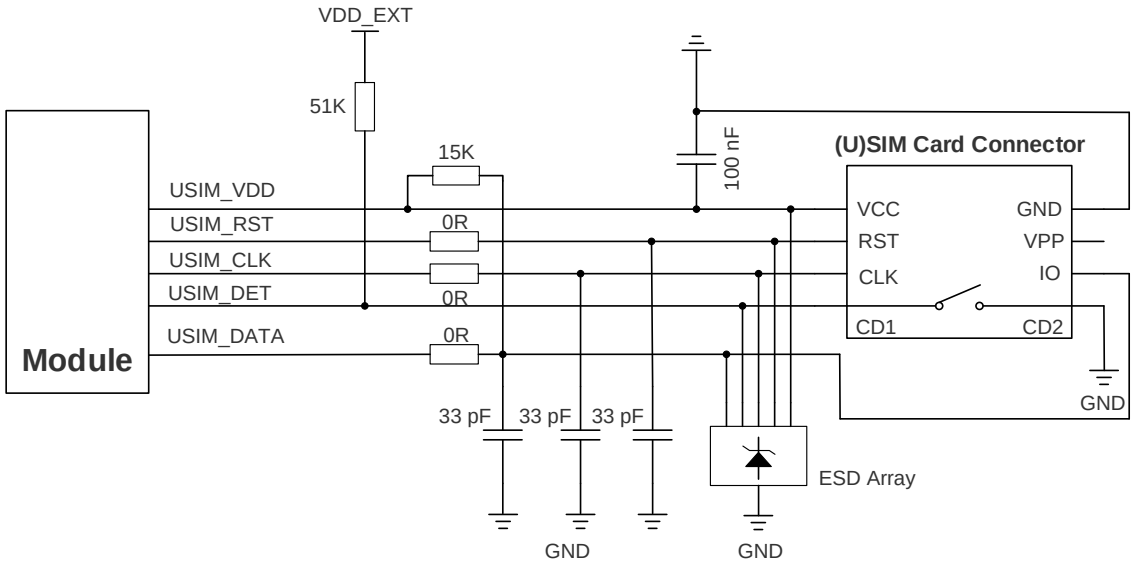


Figure 19: Reference Design of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the function of (U)SIM card hot-swap is not needed, keep USIM_DET unconnected.

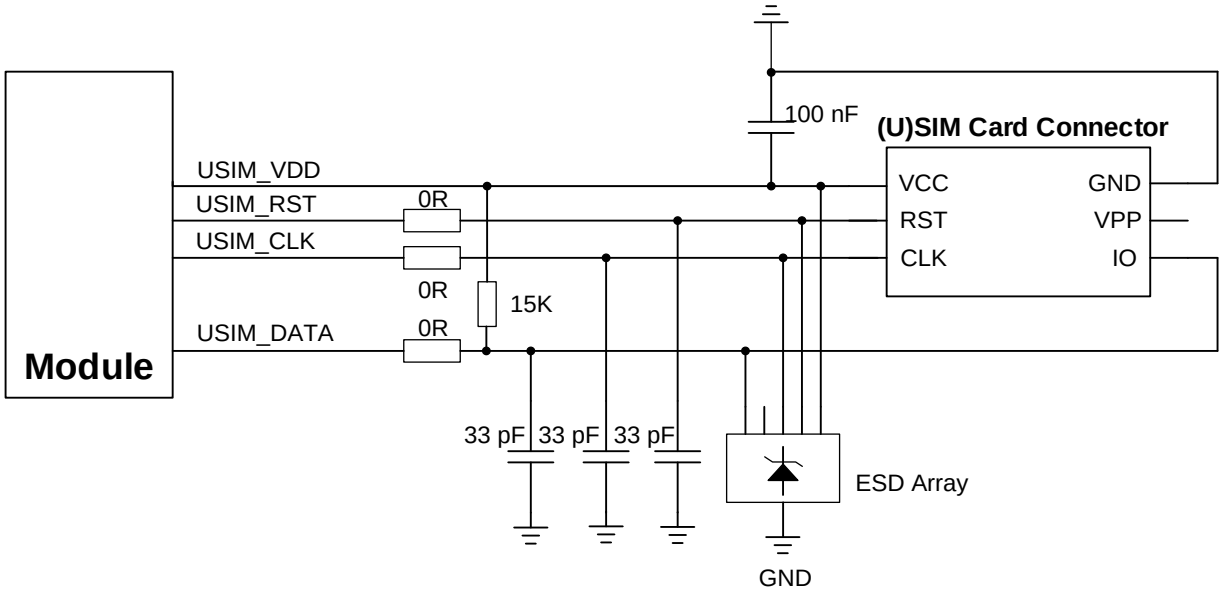


Figure 20: Reference Design of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, you should follow the principles below in the (U)SIM circuit design:

- Place the (U)SIM card connector close to the module. Keep the trace length less than 200 mm if possible.

- Route (U)SIM card differential traces at the inner-layer of the PCB, and surround the traces with ground on that layer and ground planes above and below. For signal traces, provide clearance from power supply traces, crystal-oscillators, magnetic devices, sensitive signals like RF signals, analog signals, and noise signals generated by clock, DC-DC, etc.
- Ensure the tracing between the (U)SIM card connector and the module is short and wide. Keep the trace width of ground and USIM_VDD at least 0.5 mm to keep the same electric potential.
- To avoid cross talk between USIM_DATA and USIM_CLK, keep the traces away from each other and shield them with surrounded ground.
- To offer better ESD protection, you can add a ESD array of which the parasitic capacitance should be less than 15 pF. Add 0 Ω resistors in series between the module and the (U)SIM card connector to facilitate debugging. Additionally, add 33 pF capacitors in parallel among USIM_DATA, USIM_CLK and USIM_RST signal traces to filter out RF interference.
- For USIM_DATA, it is recommended to add a 15 kΩ pull-up resistor near the (U)SIM card connector to improve the anti-jamming capability of the (U)SIM card.

4.4. UART

The module has two UART:

Table 13: UART Information

UART Types	Supported Baud Rates (bps)	Default Baud Rates (bps)	Functions
Main UART	4800/9600/19200/38400/ 57600/115200/230400/ 460800/921600	115200	• Data transmission • AT command communication
Debug UART	115200	115200	Linux console and log output

Table 14: Pin Definition of Main UART

Pin Name	Pin No.	I/O	Description	Comment
MAIN_CTS	36	DO	Main UART clear to send	If unused, keep it open. Connect to the MCUl's CTS.
MAIN_RTS	37	DI	Main UART request to send	If unused, keep it open. Connect to the MCU's RTS.
MAIN_RXD	34	DI	Main UART receive	If unused, keep it open.

MAIN_DCD	38	DO	Main UART data carrier detect	
MAIN_TXD	35	DO	Main UART transmit	
MAIN_RI	39	DO	Main UART ring indication	
MAIN_DTR	30	DI	Main UART data terminal ready	Pulled up by default. The pin can wake up the module in the low level. If unused, keep it open.

Table 15: Pin Definition of Main UART

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	22	DI	Debug UART receive	If unused, keep it open. Test points must be reserved.
DBG_TXD	23	DO	Debug UART transmit	

The module has 1.8 V UART. You can use a voltage-level translator between the module and MCU's UART if the MCU is equipped with a 3.3 V UART.

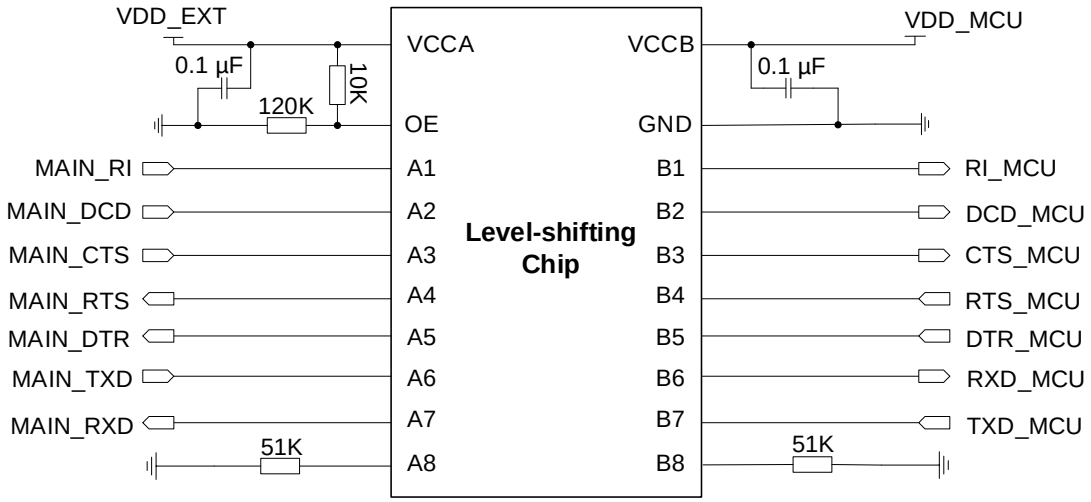


Figure 21: Reference Design of UART with a Voltage-level Translator

Another example of transistor circuit is shown as below. For the design of input/output circuits in dotted lines, see that shown in solid lines, but pay attention to the direction of the connection.

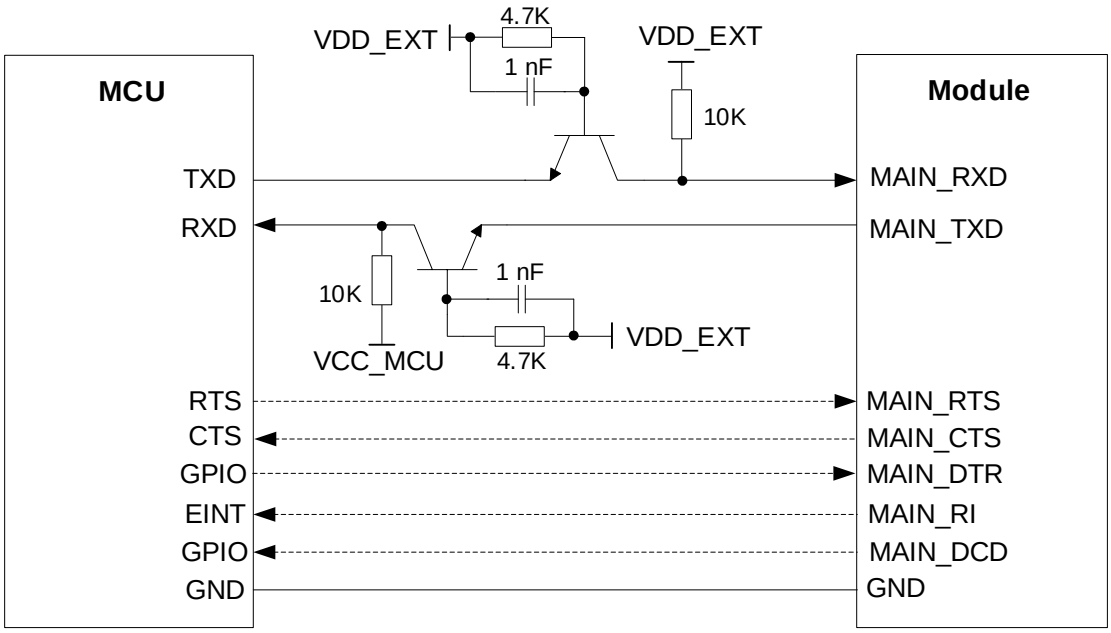


Figure 22: Reference Design of UART with Transistor Circuit

NOTE

1. Transistor circuit above is not suitable for applications with baud rates exceeding 460 kbps.
2. Please note that the module's CTS is connected to the MCU's CTS, and the module's RTS is connected to the MCU's RTS.

4.5. PCM and I2C Interfaces

The module has one PCM interfaces and one I2C interfaces.

The PCM interface supports the following modes:

- Short frame mode: the module works as both the slave and the master device
- Long frame mode: the module works as the master device only

The module supports 16-bit linear encoding format. The following figures are the short frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 2048 kHz) and the long frame mode timing diagram (PCM_SYNC = 8 kHz, PCM_CLK = 256 kHz).

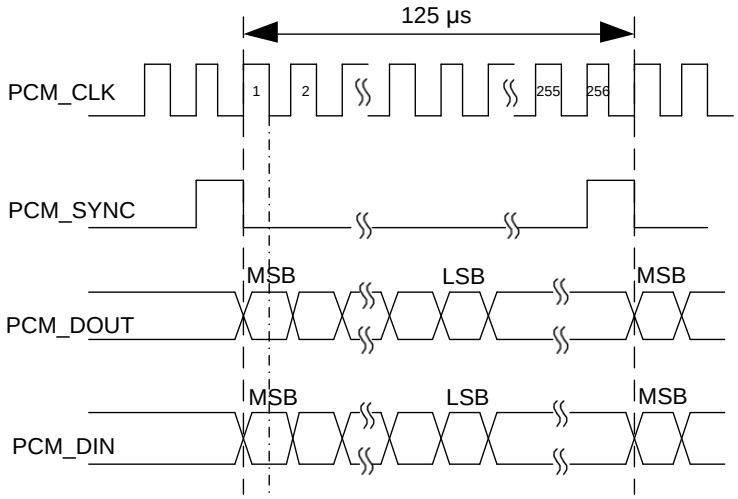


Figure 23: Timing of Short Frame Mode

In short frame mode, data is sampled on the falling edge of PCM_CLK and transmitted on the rising edge. The PCM_SYNC falling edge represents the MSB. In this mode, PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM_SYNC operates at 8 kHz, and also supports 4096 kHz when PCM_SYNC operates at 16 kHz.

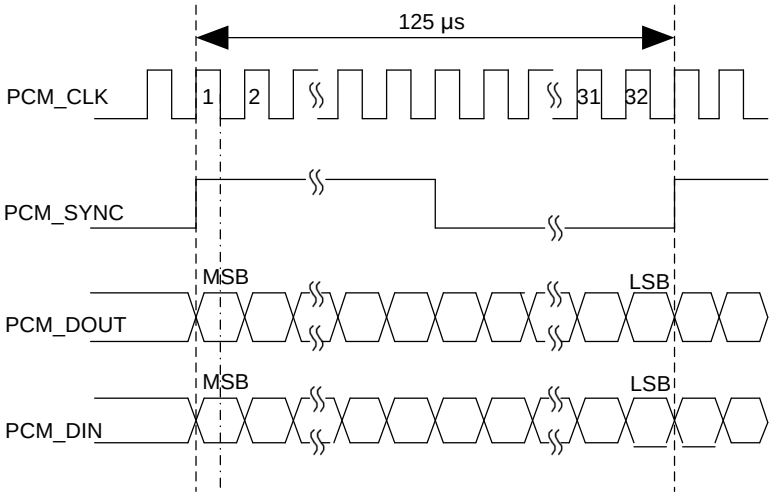


Figure 24: Timing of Long Frame Mode

In long frame mode, data is also sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. But in this mode, the PCM_SYNC rising edge represents the MSB. PCM_CLK supports 256 kHz, 512 kHz, 1024 kHz and 2048 kHz when PCM_SYNC reaches 8 kHz with a 50 % duty cycle.

The clock and mode of PCM can be configured by **AT+QDAI**, and the default configuration is short frame mode (PCM_CLK = 2048 kHz, PCM_SYNC = 8 kHz). For details, see ***document [2]*** about AT command.

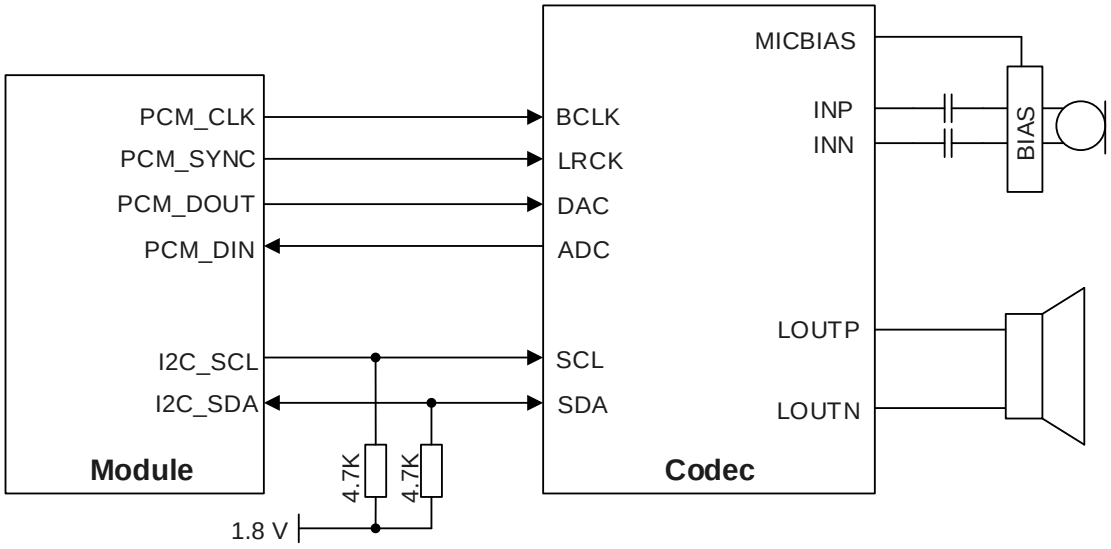


Figure 25: Reference Design of PCM and I2C Interfaces

Table 16: Pin Definition of PCM Interface

Pin Name	Pin No.	I/O	Description	Comment
PCM_SYNC	5	DIO	PCM data frame sync	Master mode: output. Slave mode: input. If unused, keep it open.
PCM_CLK	4	DIO	PCM clock	
PCM_DIN	6	DI	PCM data input	If unused, keep it open.
PCM_DOUT	**7**	DO	PCM data output	If unused, keep it open.

Table 17: Pin Definition of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C_SCL	40	OD	I2C serial clock (for external codec)	Externally pulled up to 1.8 V. If unused, keep it open.
I2C_SDA	41	OD	I2C serial data (for external codec)	

4.6. ADC Interface

The module has one ADC interface. To improve the accuracy of ADC, the trace of ADC interface should be surrounded by ground.

Table 18: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	If unused, keep it open.

With **AT+QADC=0**, you can read the voltage value on ADC0. For more details about the AT command, see ***document [2]***.

Table 19: Characteristics of ADC Interface

Parameters	Min.	Typ.	Max.	Units
ADC0 Voltage Range	0.3	-	VBAT_BB	V
ADC Resolution	-	-	15	bits

NOTE

1. The input voltage of every ADC interface should not exceed its corresponding voltage range.
2. It is prohibited to directly supply any voltage to ADC interface when the module is not powered by the VBAT.
3. It is recommended to use resistor divider circuit for ADC interface application.

4.7. SPI

The module has one SPI which only supports master mode with a maximum clock frequency up to 50 MHz.

Table 20: Pin Definition of SPI

Pin Name	Pin No.	I/O	Description	Comment
SPI_CLK	26	DO	SPI clock	Master mode only. If unused, keep it open.
SPI_DIN	28	DI	SPI master-in salve-out	
SPI_DOUT	27	DO	SPI master-out slave-in	

The module has 1.8 V SPI interfaces. A voltage-level translator should be used between the module and the host if the application is equipped with a 3.3 V processor or device interface. The following figure shows a reference design:

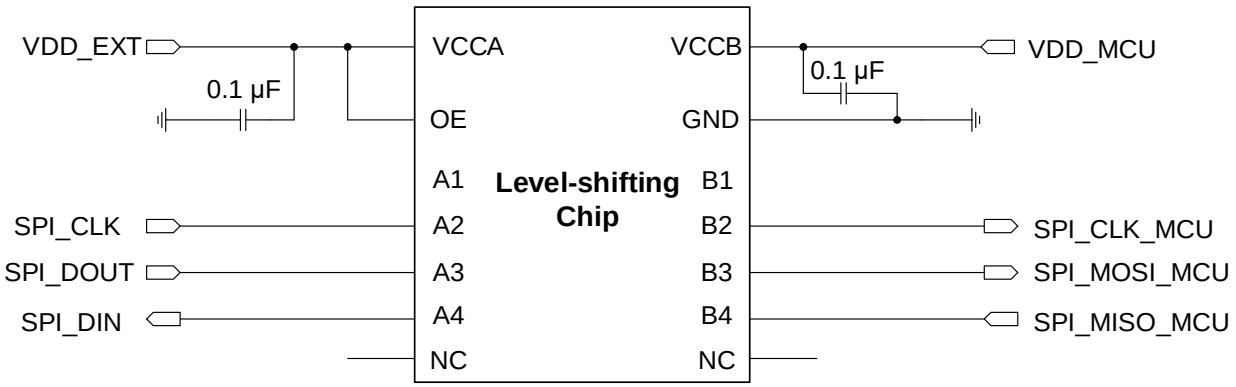


Figure 26: Reference Design of SPI with a Level-Shifting Chip

4.8. Indication Signal

Table 21: Pin Definition of Indication Signal

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	If unused, keep it open.
NET_STATUS	21	DO	Indicate the module's network activity status	If unused, keep it open.

4.8.1. Network Status Indication

The module has one network status indication pin: the NET_STATUS for the module’s network operation status indication. NET_STATUS can drive corresponding LED.

Table 22: Network Status Indication Pin Level and Module Network Status

Pin Name	Level Status	Module Network Status
NET_STATUS	Flicker slowly (200 ms high/1800 ms low)	Network searching
	Flicker slowly (1800 ms high/200 ms low)	Idle

	Flicker quickly (125 ms high/125 ms low)	Data transmission is ongoing
	Always high	Voice calling

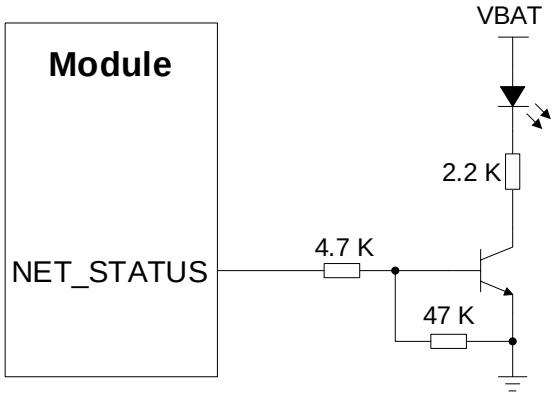


Figure 27: Reference Design of Network Status Indication

4.8.2. STATUS

The STATUS is used for indicating module's operation status. It will output high level when the module is turned on.

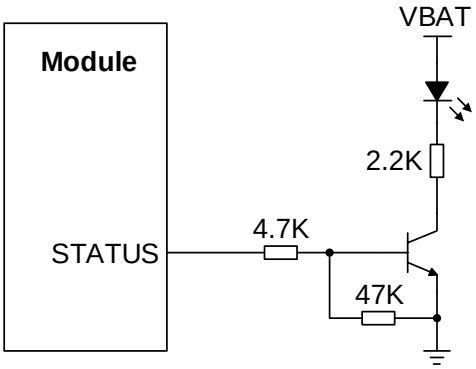


Figure 28: Reference Design of STATUS

4.8.3. MAIN_RI

AT+QCFG= "risignaltype", "physical" can be used to configure the indication behavior for MAIN_RI. No matter on which port (main UART, USB AT port or USB modem port) a URC information is presented,

the URC information will trigger the behavior of the MAIN_RI.

NOTE

The **AT+QURCCFG** allows you to set the main UART, USB AT port or USB modem port as the URC information output port. The USB AT port is the URC output port by default. See ***document [2]*** for details.

You can configure MAIN_RI behaviors flexibly. The default behaviors of the MAIN_RI are shown as below:

Table 23: MAIN_RI Level and Module Status

Module Status	MAIN_RI Level Status
Idle	High
When a new URC information returns	MAIN_RI outputs at least 120 ms low level. After the module outputs the data, the level status will then become high.

Indication behavior for MAIN_RI can be configured via **AT+QCFG="urc/ri/ring"**. See ***document [3]*** for details.

5 RF Specifications

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 24: Pin Definition of Cellular Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance.
ANT_DRX	56	AI	Diversity antenna interface	50 Ω impedance. If unused, keep it open.

NOTE

Only passive antennas are supported.

Table 25: Operating Frequency of EG92-NA (Unit: MHz)

Operating Frequency	Transmit	Receive
LTE-FDD B2	1850~1910	1930~1990
LTE-FDD B4	1710~1755	2110~2155
LTE-FDD B5	824~849	869~894
LTE-FDD B12	699~716	729~746
LTE-FDD B13	777~787	746~756

LTE-FDD B66	1710~1780	2110~2200
LTE-FDD B71	663~698	617~652

Table 26: Operating Frequency of EG92-EU (Unit: MHz)

Operating Frequency	Transmit	Receive
EGSM900	880–915	925–960
DCS1800	1710–1785	1805–1880
WCDMA B1	1920–1980	2110–2170
WCDMA B8	880–915	925–960
LTE-FDD B1	1920–1980	2110–2170
LTE-FDD B3	1710–1785	1805–1880
LTE-FDD B7	2500–2570	2620–2690
LTE-FDD B8	880–915	925–960
LTE-FDD B20	832–862	791–821
LTE-FDD B28	703–748	758–803

5.1.2. Antenna Tuner Control Interface

The module can use GRFC (generic RF control) interfaces to control external antenna tuner.

Table 27: Pin Definition of GRFC Interface

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	76	DO	Generic RF Controller	If unused, keep them open.
GRFC2	77	DO	Generic RF Controller	

Table 28: Truth Table of GRFC Interfaces for EG92-NA (Unit: MHz)

GRFC1 Level	GRFC2 Level	Frequency Range	Bands
Low	Low	699–756	LTE: B12/B13
Low	High	824–894	LTE: B5
High	Low	663–652	LTE: B71
High	High	1710–2180	LTE: B2/B4/B66

Table 29: Truth Table of GRFC Interfaces for EG92-EU (Unit: MHz)

GRFC1 Level	GRFC2 Level	Frequency Range	Bands
Low	Low	703–803	LTE B28
Low	High	791–862	LTE B20
High	Low	880–960	• LTE: B8 • WCDMA: B8 • GSM900
High	High	1710–2690	• LTE: B1/B3/B7 • WCDMA: B1 • DCS1800

5.1.3. Transmitting Power

Table 30: RF Transmitting Power

Frequency	Max. Tx Power	Min. Tx Power
EGSM900	33 dBm ±2 dB	5 dBm ±5 dB
DCS1800	30 dBm ±2 dB	0 dBm ±5 dB
EGSM900 (8-PSK)	27 dBm ±3 dB	5 dBm ±5 dB
DCS1800 (8-PSK)	26 dBm ±3 dB	0 dBm ±5 dB
WCDMA bands	23 dBm ±2 dB	< -49 dBm
LTE bands	23 dBm ±2 dB	< -39 dBm

NOTE

For GPRS transmission on 4 uplink timeslots, the maximum output power reduction is 4.0 dB. The design conforms to *3GPP TS 51.010-1* ***subclause 13.16***

5.1.4. Receiver Sensitivity

Table 31: Conducted RF Receiver Sensitivity of EG92-NA (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [4]	
LTE-FDD B2	-97.5 dBm	-98.5 dBm	-101.1 dBm	-94.3dBm
LTE-FDD B4	-97.2 dBm	-98.4 dBm	-100.2 dBm	-96.3dBm
LTE-FDD B5	-98.8 dBm	-99.4 dBm	-101.5 dBm	-94.3dBm
LTE-FDD B12	-97.8 dBm	-98.1 dBm	-100.2 dBm	-93.3dBm
LTE-FDD B13	-97.8 dBm	-98.2 dBm	-100.3 dBm	-93.3dBm
LTE-FDD B66	-97.2 dBm	-98.5 dBm	-100.2 dBm	-96.5dBm
LTE-FDD B71	-97.8 dBm	-98.8 dBm	-100.3 dBm	-94.2dBm

Table 31: Conducted RF Receiver Sensitivity of EG92-EU (Unit: dBm)

Frequency	Receiver Sensitivity (Typ.)			3GPP Requirements (SIMO)
	Primary	Diversity	SIMO [5]	
EGSM900	-109.4	-	-	-102
DCS1800	-109	-	-	-102
WCDMA B1	-109.2	-111	-	-106.7
WCDMA B8	-110	-111.2	-	-103.7
LTE-FDD B1	-97.5	-99.4	-101	-96.3
LTE-FDD B3	-98	-99	-100.5	-93.3

[4] For the SIMO receiving sensitivity, LTE bands are tested with 2 Rx antennas.
[5] For the SIMO receiving sensitivity, LTE bands are tested with 2 Rx antennas.

LTE-FDD B7	-96.6	-98.1	-99.5	-94.3
LTE-FDD B8	-98.5	-99.7	-102	-93.3
LTE-FDD B20	-98.5	-97	-100.4	-93.3
LTE-FDD B28	-98.6	-99.8	-102.5	-94.8

5.1.5. Reference Design

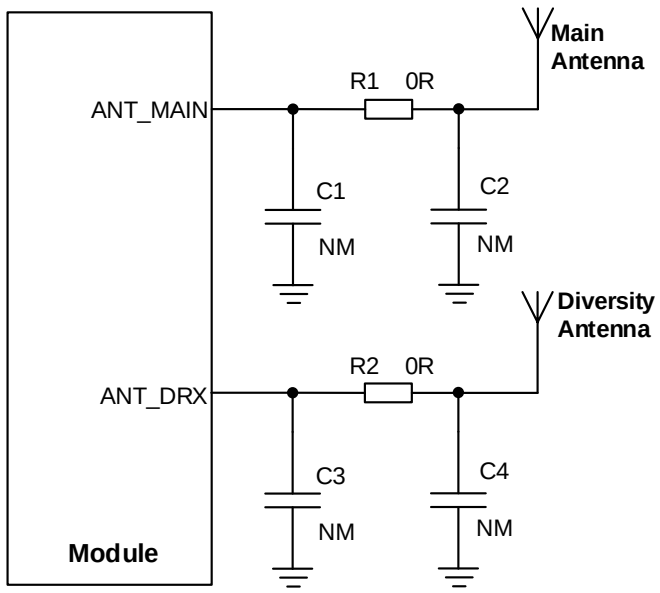


Figure 29: Reference Design of Main Antenna and Diversity Antenna

NOTE

1. To improve receiver sensitivity, ensure that the clearance among antennas is appropriate.
2. Use a π-type matching circuit for all the antenna interfaces for better RF performance and for the ease of debugging.
3. Capacitors are not mounted by default.
4. Place the π-type matching components (R1, C1, C2 and R2, C3, C4) to antennas as close as possible.

5.2. GNSS

GNSS information of the module is as follows:

- Supports GPS, GLONASS, BDS, Galileo and QZSS positioning system.
- Supports NMEA 0183 protocol and outputs NMEA sentences via USB interface (data update rate for positioning: 1–10 Hz, 1 Hz by default).
- The module's GNSS function is OFF by default. It must be ON via AT commands.

For more details about GNSS technology and configurations, see ***document [6]***.

5.2.1. Antenna Interface & Frequency Bands

Table 32: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 33: GNSS Frequency (Unit: MHz)

Antenna Types	Frequency
GPS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)
GLONASS	1597.5–1605.8 (L1)
BDS	1561.098 ±2.046 (B1I)
Galileo	1575.42 ±2.046 (E1) 1176.45 ±10.23 (E5a)
QZSS	1575.42 ±1.023 (L1) 1176.45 ±10.23 (L5)

5.2.2. GNSS Performance

Table 34: GNSS Performance

Parameters	Modes	Conditions	Typ.	Units
Sensitivity	Acquisition	Autonomous	-146	dBm
	Reacquisition		-157	
	Tracking		-157	
TTFF	Cold start @ open sky	Autonomous	35	s

		XTRA start	12	
	Warm start @ open sky	Autonomous	26	
		XTRA start	3.7	
	Hot start @ open sky	Autonomous	2	
		XTRA start	3.4	
Accuracy	CEP-50	Autonomous @ open sky	2.5	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock of navigation signals (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock of navigation signals within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position of navigation signals successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

5.2.3.1. GNSS Active Antenna

GNSS active antenna connection reference circuit is shown in the figure below.

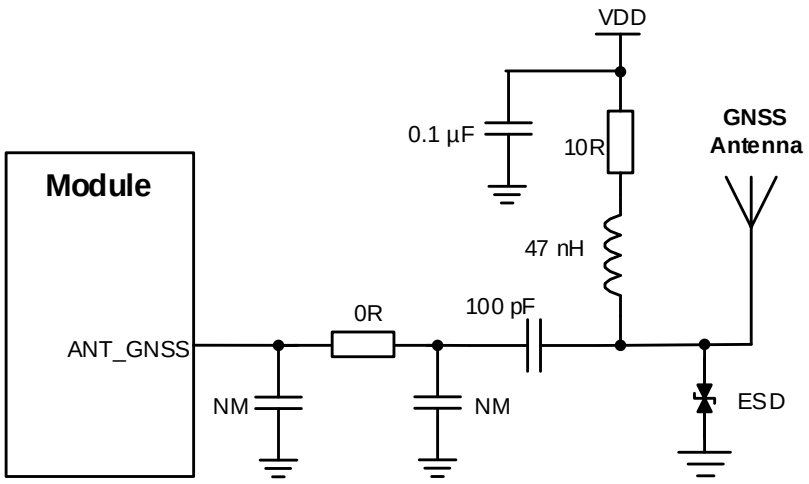


Figure 30: Reference Design of GNSS Active Antenna

The power supply voltage range of the external active antenna is 2.8–4.3 V, and the typical value is 3.3 V.

5.2.3.2. GNSS Passive Antenna

GNSS passive antenna connection reference circuit is shown in the figure below.

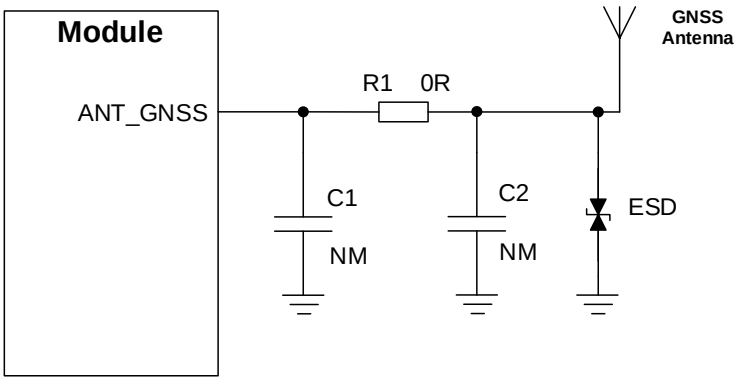


Figure 31: Reference Design of GNSS Passive Antenna

It is recommended to reserve a π-type matching circuit in the peripheral circuit design for Bluetooth antenna interface for better RF performance. Components (R1, C1 and C2) of the π-type matching circuit shall be placed as close to the antenna as possible. C1andC2are not mounted by default. Only a 0 Ω resistor is mounted on R1. Keep the characteristic impedance for RF trace as 50 Ω when routing and keep the trace as short as possible.

NOTE

1. You can select an external LDO according to the active antenna types. If you design the module with a passive antenna, you will not need the VDD circuit.
2. Junction capacitance of ESD protection components on the antenna interface should not exceed 0.05 pF.
3. It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB

structures.

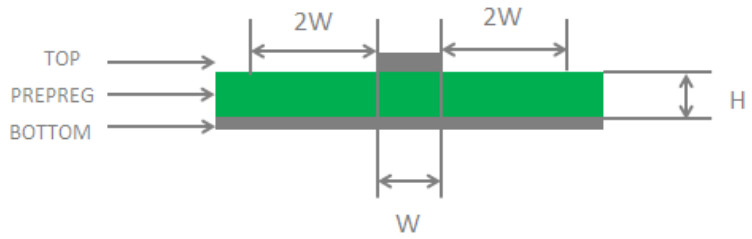


Figure 32: Microstrip Design on a 2-layer PCB

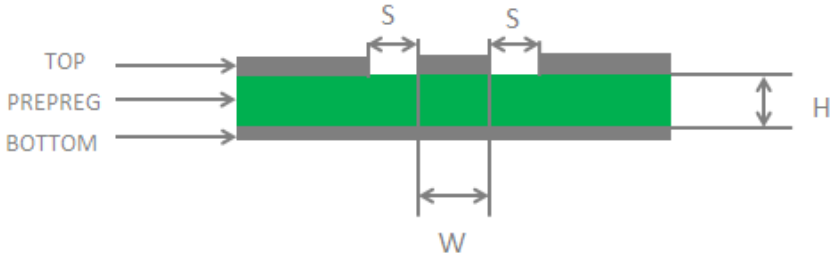


Figure 33: Coplanar Waveguide Design on a 2-layer PCB

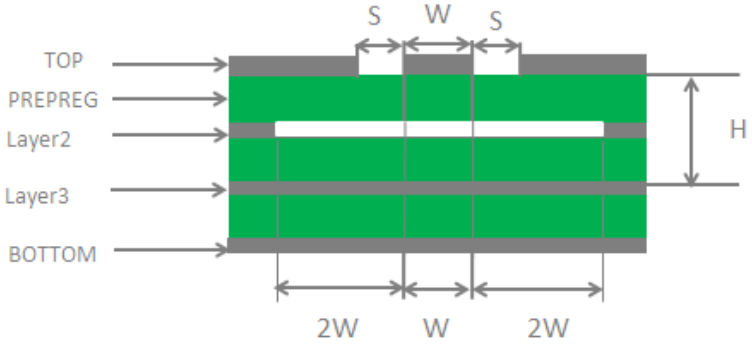


Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

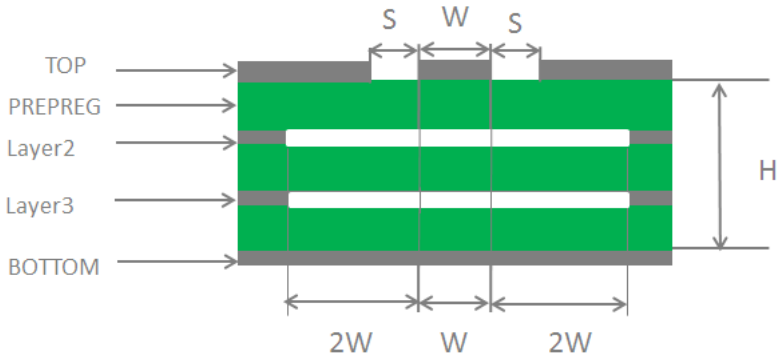


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [7]***.

5.4. Requirements for Antenna Design

Table 35: Requirements for Antenna Design

Antenna Types	Requirements
GNSS	**Frequency range:** ● L1: 1559–1609 MHz ● L5: 1166–1187 MHz RHCP or linear polarization VSWR: ≤ 2 (Typ.)

	For passive antenna application: Passive antenna gain: > 0 dBi
	For active antenna application: Active antenna noise coefficient: < 1.5 dB Active antenna gain: > 0 dBi Active antenna embedded LNA gain: < 17 dB
GSM, WCDMA, LTE-FDD	VSWR: ≤ 2 Efficiency: > 30 % Gain: 1 dBi Max input power: 50 W Input impedance: 50 Ω Vertical polarization **Cable insertion loss:** ● < 1 dB: LB (< 1 GHz) ● < 1.5 dB: MB (1–2.3 GHz) ● < 2 dB: HB (> 2.3 GHz)

5.5. RF Connector Recommendation

If the RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT receptacle provided by Hirose.

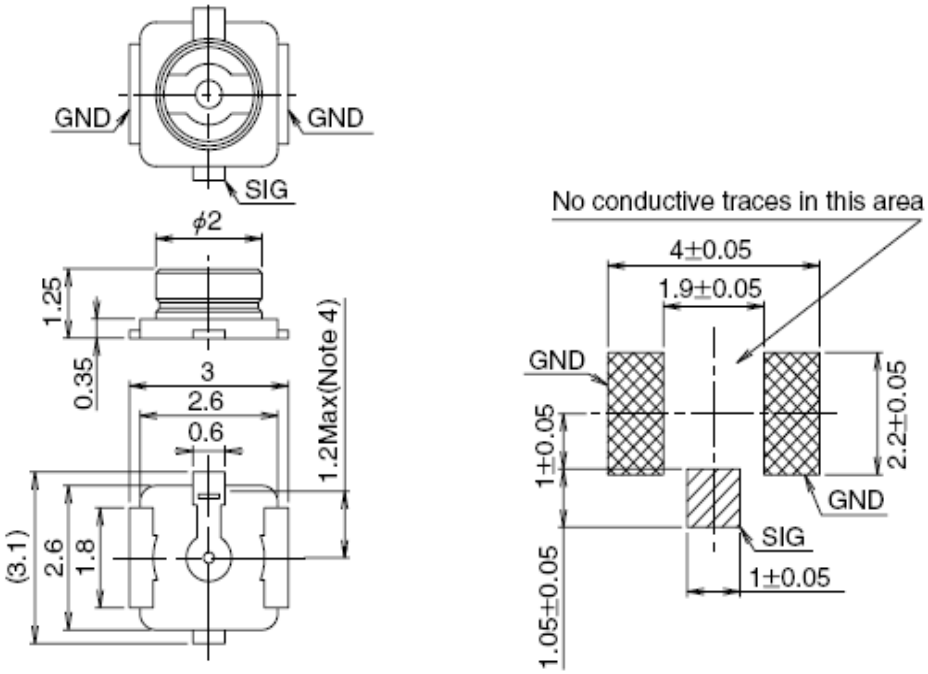


Figure 36: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

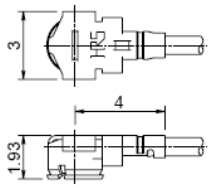
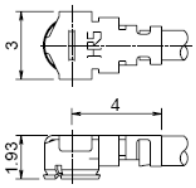
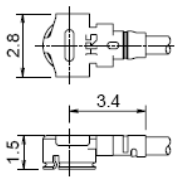
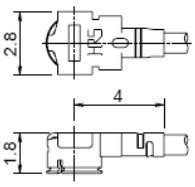
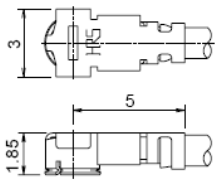
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 37: Specifications of Mated Plugs (Unit: mm)

The following figure describes the space factor of the mated connector.

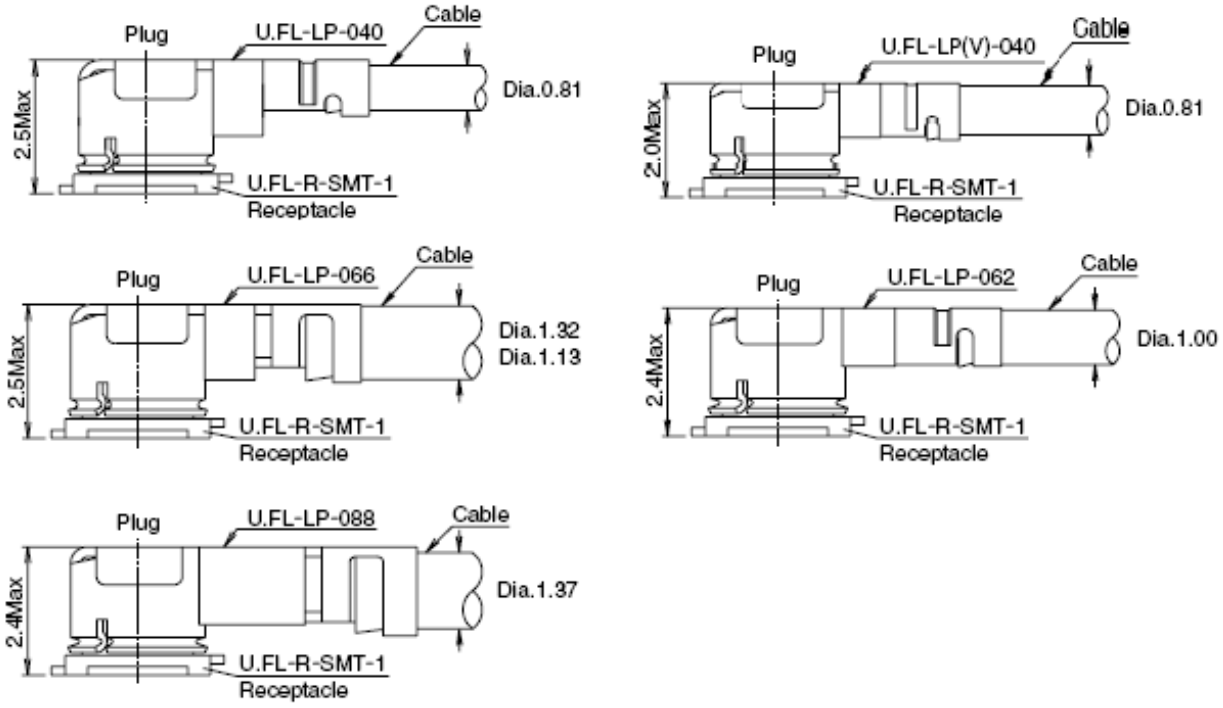


Figure 38: Space Factor of the Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Table 36: Absolute Maximum Ratings

Parameters	Min.	Max.	Units
Voltage at VBAT_RF & VBAT_BB	-0.3	4.7	V
Voltage at USB_VBUS	-0.3	5.5	V
Voltage at digital pins	-0.3	2.3	V
Voltage at ADC0	0	VBAT_BB	V
Current at VBAT_BB	-	0.8	A
Current at VBAT_RF	-	1.8	A

6.2. Power Supply Ratings

Table 37: Module's Power Supply Ratings

Parameters	Descriptions	Conditions	Min.	Typ.	Max.	Units
VBAT	VBAT_BB & VBAT_RF	The actual input voltage must be within this range	3.3	3.8	4.3	V
	Voltage drops during burst transmission	At maximum power control level	-	-	400	mV
I_{VBAT}	Peak power consumption	At maximum power control level	-	-	2.0	A

USB_VBUS	USB connection detection	-	3.0	5.0	5.25	V

6.3. Power Consumption

The power consumption of EG92 series will be provided in future version of this document.

6.4. Digital I/O Characteristics

Table 38: VDD_EXT I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	0.65 × VDD_EXT	VDD_EXT + 0.2
V_{IL}	Low-level input voltage	-0.3	0.35 × VDD_EXT
V_{OH}	High-level output voltage	VDD_EXT - 0.45	VDD_EXT
V_{OL}	Low-level output voltage	0	0.45

Table 39: (U)SIM Low/High-voltage I/O Characteristics (Unit: V)

Parameters	Descriptions	Min.	Max.
V_{IH}	High-level input voltage	0.8 x USIM_VDD	USIM_VDD
V_{IL}	Low-level input voltage	-0.3	0.12 x USIM_VDD
V_{OH}	High-level output voltage	0.8 x USIM_VDD	USIM_VDD
V_{OL}	Low-level output voltage	0	0.4

6.5. ESD

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the

development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 40: ESD Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %; Unit: kV)

Test Points	Contact Discharge	Air Discharge
VBAT & GND	±5	±10
All Antenna Interfaces	±4	±8
Other Interfaces	±0.5	±1

6.6. Operating and Storage Temperatures

Table 41: Operating and Storage Temperatures (Unit: °C)

Parameters	Min.	Typ.	Max.
Normal Operating Temperature [6]	-35	+25	+75
Extended Operating Temperature [7]	-40	-	+85
Storage Temperature	-40	-	+90

[6] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module's performance complies with 3GPP requirements.

[7] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module retains the ability to establish and maintain functions such as voice and SMS, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as P_{out}, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's performance will comply with 3GPP requirements again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

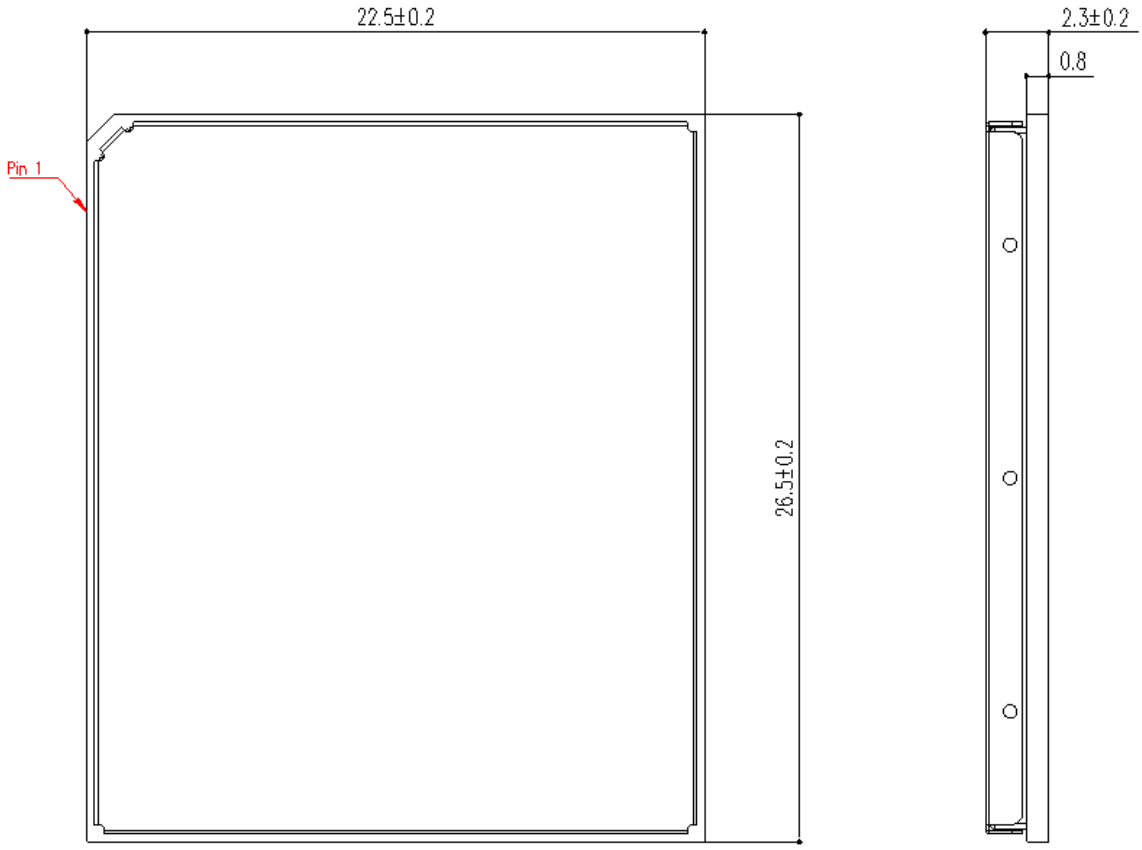


Figure 39: Top and Side Dimensions

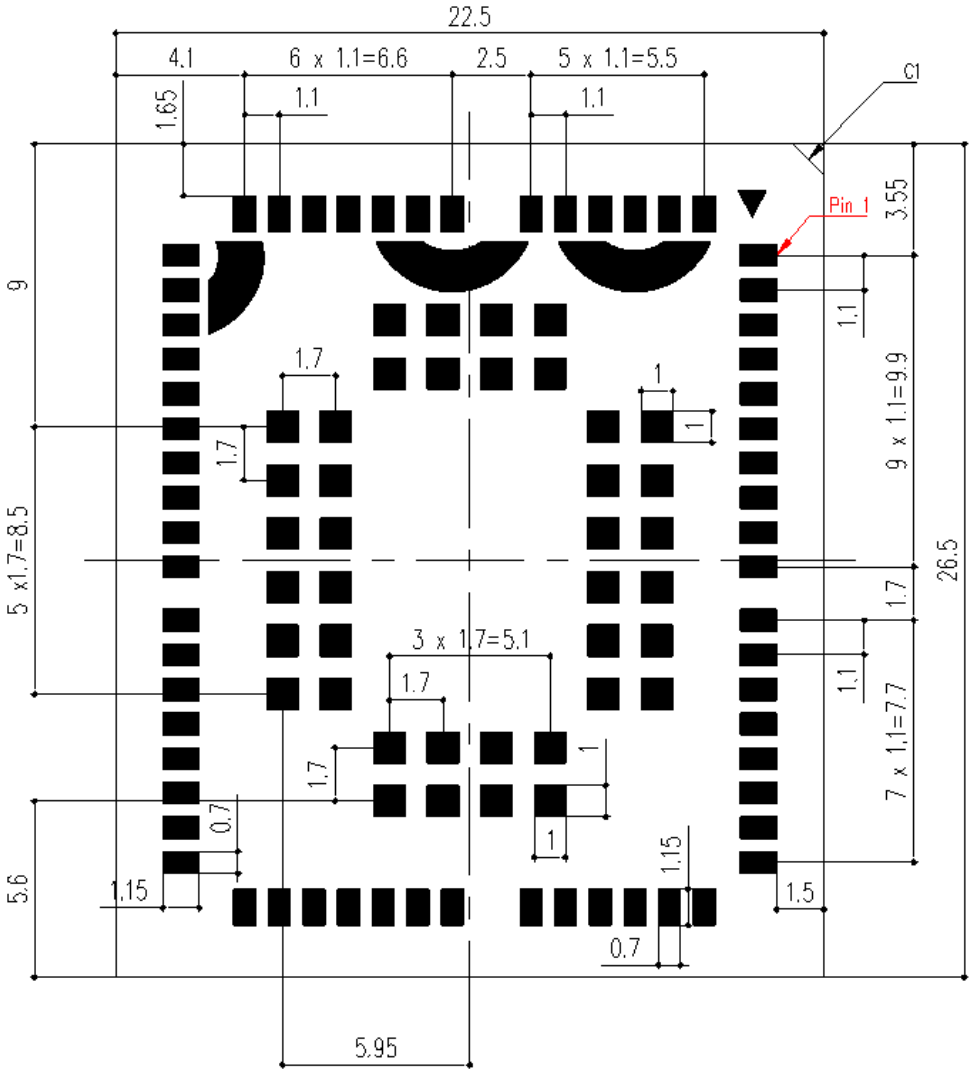


Figure 40: Bottom Dimensions

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

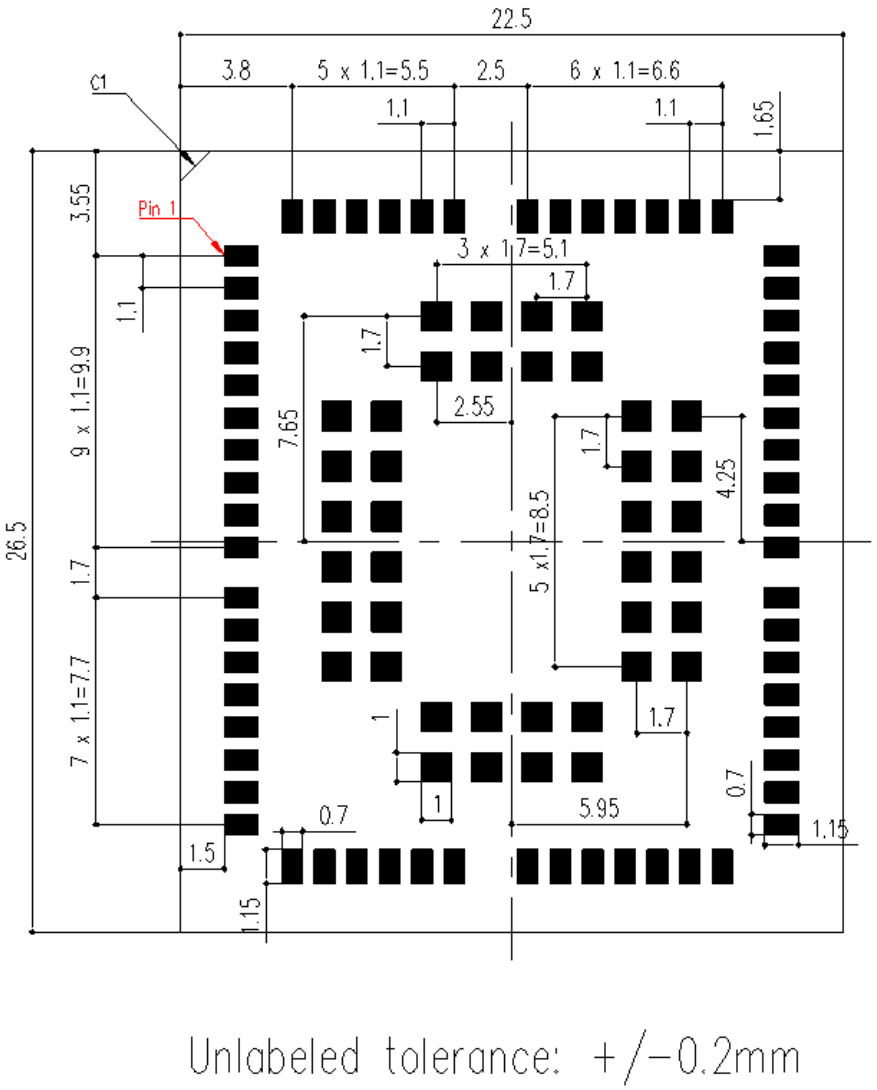


Figure 41: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

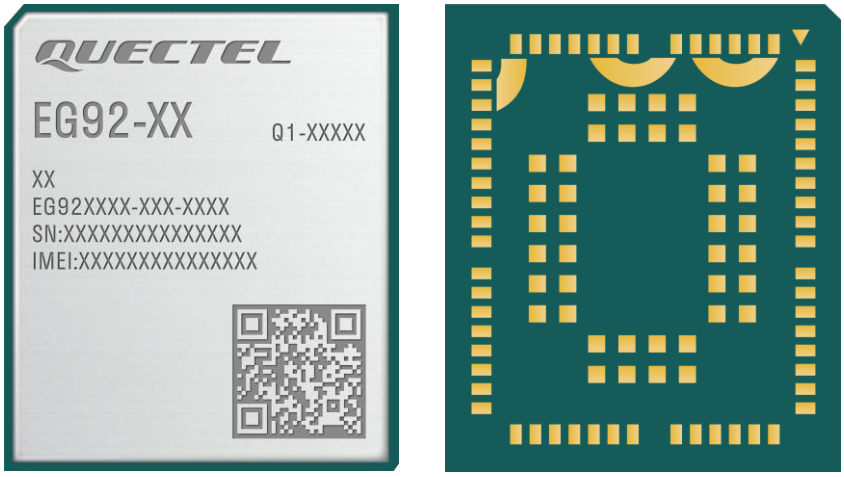


Figure 42: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended storage condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in recommended storage condition.

3. Floor life: 168 hours [8] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in recommended storage condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[8] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.18 mm. For more details, see ***document [9]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below:

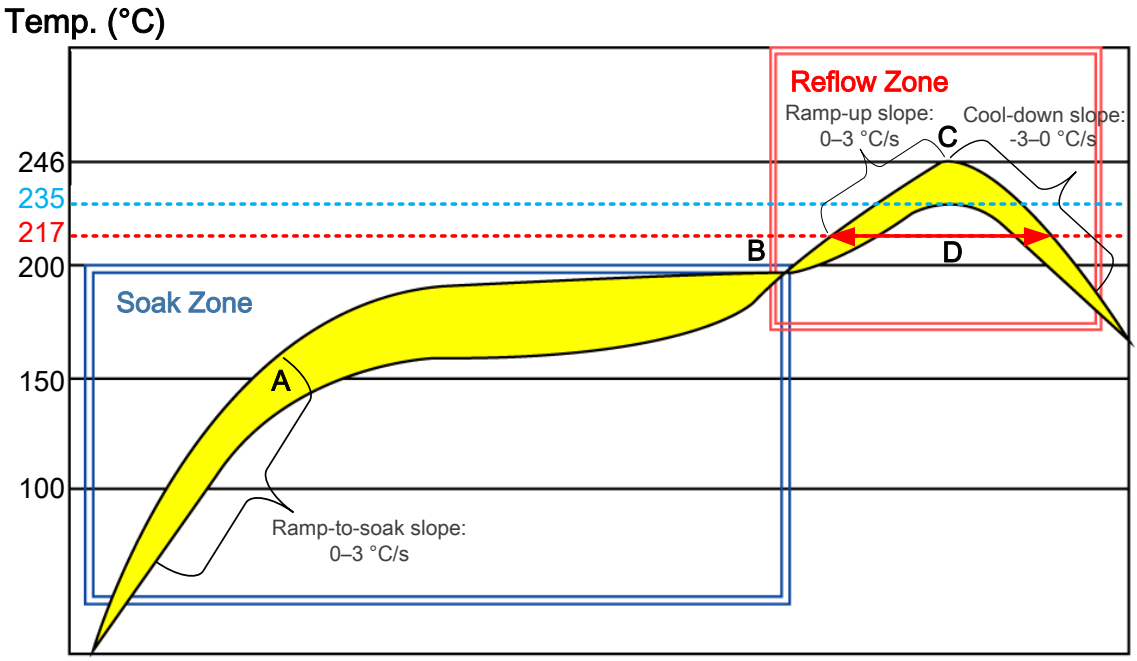


Figure 43: Recommended Reflow Soldering Thermal Profile

Table 42: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s
Reflow Cycle	
Max Reflow Cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. If a conformal coating is necessary for the module, do not use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
3. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
4. Due to the complexity of the SMT process, contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective wave soldering, ultrasonic soldering) that is not mentioned in ***document [9]***.

8.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

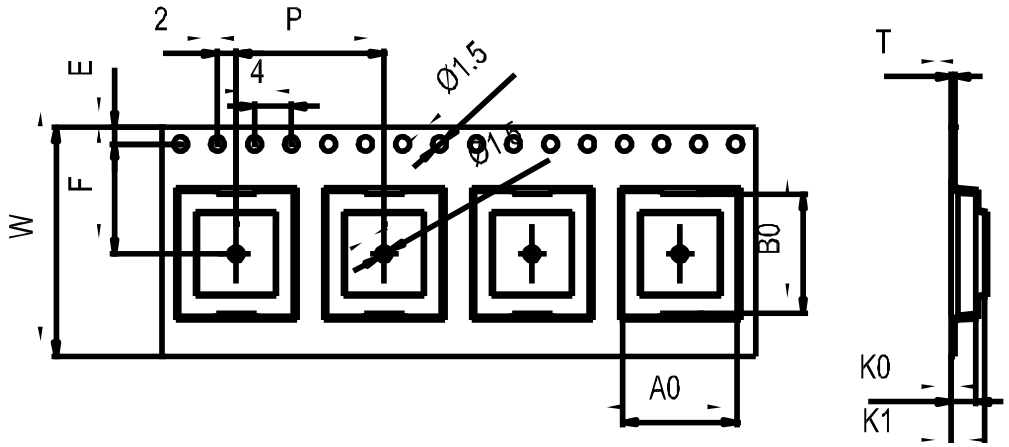


Figure 44: Carrier Tape Dimension Drawing

Table 43: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	22.8	26.8	3.1	6.9	20.2	1.75

8.3.2. Plastic Reel

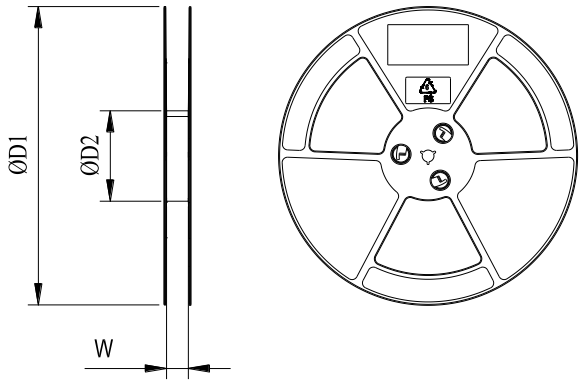


Figure 45: Plastic Reel Dimension Drawing

Table 44: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	44.5

8.3.3. Mounting Direction

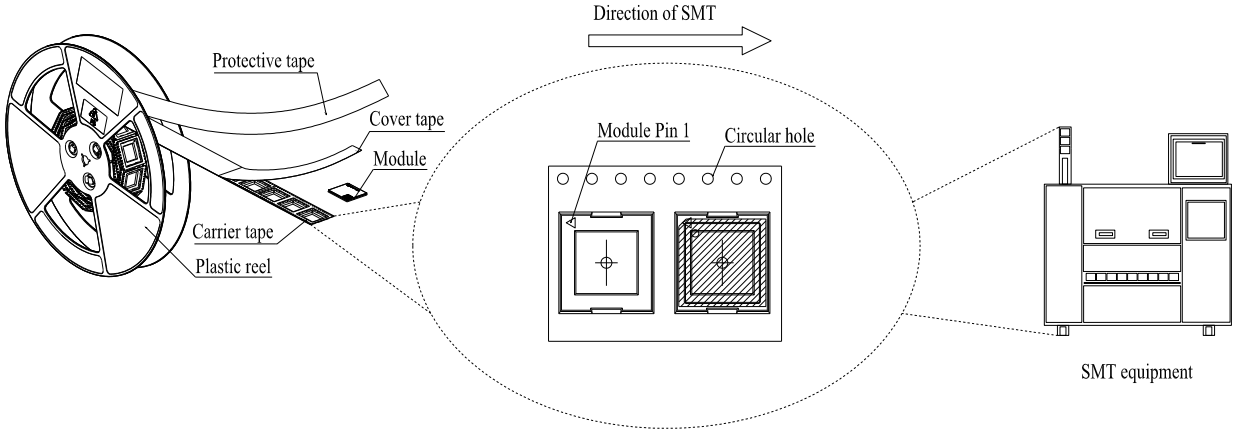
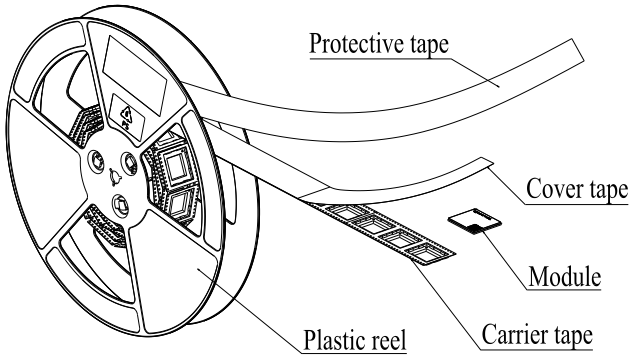


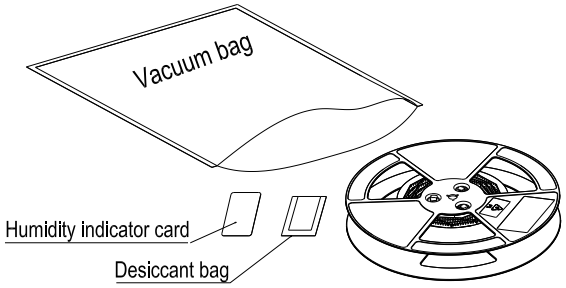
Figure 46: Mounting Direction

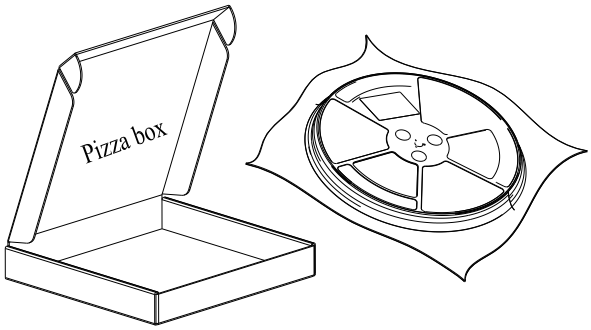
8.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into the pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

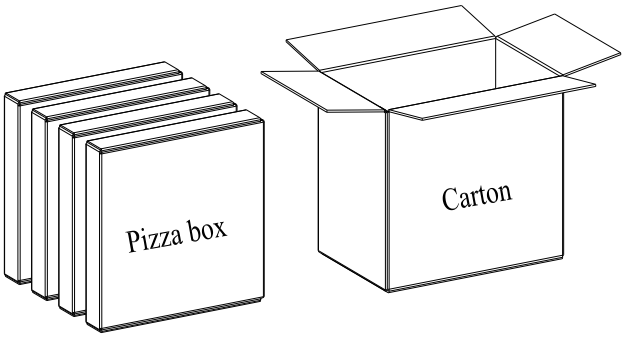


Figure 47: Packaging Process

9 Appendix References

Table 45: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EC2x&EG2x-G(L)&EG9x&EM05_Series_AT_Commands_Manual
[3] Quectel_EC2x&EG2x&EG9x&EM05_Series_QCFG_AT_Commands_Manual
[4] Quectel_EC2x&EG2x&EG9x_Series_Power_Management_Application_Note
[5] Quectel_EG9x_Series_AT+QDSIM_Command_Manual
[6] Quectel_EC2x&EG2x&EG9x&EM05_Series_GNSS_Application_Note
[7] Quectel_RF_Layout_Application_Note
[8] Quectel_EC2x&EG2x&EG9x&EM05_Series_Software_Thermal_Management_Guide
[9] Quectel_Module_SMT_Application_Note

Table 46: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
bps	Bits Per Second
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CTS	Clear To Send
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access

DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
DRX	Diversity Receive
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HR	Half Rate
HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
I2C	Inter-Integrated Circuit
I/O	Input/Output
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array

LNA	Low Noise Amplifier
LTE	Long Term Evolution
MB	Middle Band
MCU	Microcontroller Unit
MO	Mobile Originated
MT	Mobile Terminated
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RHCP	Right Hand Circularly Polarized
Rx	Receive
SIMO	Single Input Multiple Output
SMD	Surface Mount Device
SMS	Short Message Service
SPI	Serial Peripheral Interface
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink

UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access

OEM/Integrators Installation Manual

Important Notice to OEM integrators 1. This module is limited to OEM installation ONLY. 2. This module is limited to installation in mobile or fixed applications, according to Part 2.1091(b). 3. The separate approval is required for all other operating configurations, including portable configurations with respect to Part 2.1093 and different antenna configurations 4. For FCC Part 15.31 (h) and (k): The host manufacturer is responsible for additional testing to verify compliance as a composite system. When testing the host device for compliance with Part 15 Subpart B, the host manufacturer is required to show compliance with Part 15 Subpart B while the transmitter module(s) are installed and operating. The modules should be transmitting and the evaluation should confirm that the module's intentional emissions are compliant (i.e. fundamental and out of band emissions). The host manufacturer must verify that there are no additional unintentional emissions other than what is permitted in Part 15 Subpart B or emissions are complaint with the transmitter(s) rule(s). The Grantee will provide guidance to the host manufacturer for Part 15 B requirements if needed.

Important Note

notice that any deviation(s) from the defined parameters of the antenna trace, as described by the instructions, require that the host product manufacturer must notify to Quectel that they wish to change the antenna trace design. In this case, a Class II permissive change application is required to be filed by the USI, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by a Class II permissive change application

End Product Labeling

When the module is installed in the host device, the FCC ID label must be visible through a window on the final device or it must be visible when an access panel, door or cover is easily re-moved. If not, a second label must be placed on the outside of the final device that contains the following text: “Contains FCC ID: XMR202307EG92NA”. The FCC ID can be used only when all FCC compliance requirements are met.

Antenna

(1) The antenna must be installed such that 20 cm is maintained between the antenna and users,
(2) The transmitter module may not be co-located with any other transmitter or antenna.

In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed

Technology	Frequency Range (MHz)	Antenna Type	Max Peak Gain (dBi)
LTE Band 2	1850 ~ 1910	Dipole	9.9
LTE Band 4	1710 ~ 1755		9.9
LTE Band 5	824 ~ 849		7.3
LTE Band 12	699 ~ 716		6.5
LTE Band 13	777 ~ 787		7.0
LTE Band 66	1710 ~ 1780		9.9
LTE Band 71	663~698		6.3

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual

Federal Communication Commission Interference Statement

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:
- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

List of applicable FCC rules

This module has been tested and found to comply with part 22, part 24, part 27 requirements for Modular Approval.
The modular transmitter is only FCC authorized for the specific rule parts (i.e., FCC transmitter rules) listed on the grant, and that the host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. If the grantee markets their product as being Part 15 Subpart B compliant (when it also contains unintentional-radiator digital circuity), then the grantee shall provide a notice stating that the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

This device is intended only for OEM integrators under the following conditions: (For module device use)

1) The antenna must be installed such that 20 cm is maintained between the antenna and users, and
2) The transmitter module may not be co-located with any other transmitter or antenna.

As long as 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.