SC690A Series

Hardware Design

Smart Module Series

Version: 1.0.0

Date: 2021-12-07

Status: Preliminary

At Quectel, our aim is to provide timely and comprehensive services to our customers. If you require any assistance, please contact our headquarters:

Quectel Wireless Solutions Co., Ltd.
Building 5, Shanghai Business Park Phase III (Area B), No.1016 Tianlin Road, Minhang District, Shanghai 200233, China
Tel: +86 21 5108 6236
Email: info@quectel.com

Or our local offices. For more information, please visit:
http://www.quectel.com/support/sales.htm.

For technical support, or to report documentation errors, please visit:
http://www.quectel.com/support/technical.htm.
Or email us at: support@quectel.com.

Legal Notices

We offer information as a service to you. The provided information is based on your requirements and we make every effort to ensure its quality. You agree that you are responsible for using independent analysis and evaluation in designing intended products, and we provide reference designs for illustrative purposes only. Before using any hardware, software or service guided by this document, please read this notice carefully. Even though we employ commercially reasonable efforts to provide the best possible experience, you hereby acknowledge and agree that this document and related services hereunder are provided to you on an “as available” basis. We may revise or restate this document from time to time at our sole discretion without any prior notice to you.

Use and Disclosure Restrictions

License Agreements

Documents and information provided by us shall be kept confidential, unless specific permission is granted. They shall not be accessed or used for any purpose except as expressly provided herein.

Copyright

Our and third-party products hereunder may contain copyrighted material. Such copyrighted material shall not be copied, reproduced, distributed, merged, published, translated, or modified without prior written consent. We and the third party have exclusive rights over copyrighted material. No license shall be granted or conveyed under any patents, copyrights, trademarks, or service mark rights. To avoid ambiguities, purchasing in any form cannot be deemed as granting a license other than the normal non-exclusive, royalty-free license to use the material. We reserve the right to take legal action for noncompliance with abovementioned requirements, unauthorized use, or other illegal or malicious use of the material.

Trademarks

Except as otherwise set forth herein, nothing in this document shall be construed as conferring any rights to use any trademark, trade name or name, abbreviation, or counterfeit product thereof owned by Quectel or any third party in advertising, publicity, or other aspects.

Third-Party Rights

This document may refer to hardware, software and/or documentation owned by one or more third parties ("third-party materials"). Use of such third-party materials shall be governed by all restrictions and obligations applicable thereto.

We make no warranty or representation, either express or implied, regarding the third-party materials, including but not limited to any implied or statutory, warranties of merchantability or fitness for a particular purpose, quiet enjoyment, system integration, information accuracy, and non-infringement of any third-party intellectual property rights with regard to the licensed technology or use thereof. Nothing herein constitutes a representation or warranty by us to either develop, enhance, modify, distribute, market, sell, offer for sale, or otherwise maintain production of any our products or any other hardware, software, device, tool, information, or product. We moreover disclaim any and all warranties arising from the course of dealing or usage of trade.

Privacy Policy

To implement module functionality, certain device data are uploaded to Quectel's or third-party's servers, including carriers, chipset suppliers or customer-designated servers. Quectel, strictly abiding by the relevant laws and regulations, shall retain, use, disclose or otherwise process relevant data for the purpose of performing the service only or as permitted by applicable laws. Before data interaction with third parties, please be informed of their privacy and data security policy.

Disclaimer

a) We acknowledge no liability for any injury or damage arising from the reliance upon the information.
b) We shall bear no liability resulting from any inaccuracies or omissions, or from the use of the information contained herein.
c) While we have made every effort to ensure that the functions and features under development are free from errors, it is possible that they could contain errors, inaccuracies, and omissions. Unless otherwise provided by valid agreement, we make no warranties of any kind, either implied or express, and exclude all liability for any loss or damage suffered in connection with the use of features and functions under development, to the maximum extent permitted by law, regardless of whether such loss or damage may have been foreseeable.
d) We are not responsible for the accessibility, safety, accuracy, availability, legality, or completeness of information, advertising, commercial offers, products, services, and materials on third-party websites and third-party resources.

Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Revision	Date	Author	Description
-	2021-12-07	Mary SHEN/Kevin ZHOU	Creation of the document
1.0.0	2021-12-07	Mary SHEN/Kevin ZHOU	Preliminary

Contents

Table Index

Figure Index

1 Introduction

This document defines the SC690A series and describes its air interfaces and hardware interfaces which relate to your applications.

It can help you quickly understand interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application notes and user guides, you can use this module to design and to set up mobile applications easily.

FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain, and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2022SC690ANA
4. This module must not transmit simultaneously with any other antenna or transmitter
5. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.
For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093
If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.
For this device, OEM integrators must be provided with labeling instructions of finished products.
Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:
A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).
For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible;

then an additional permanent label referring to the enclosed module: “Contains Transmitter Module FCC ID: XMR2022SC690ANA” or “Contains FCC ID: XMR2022SC690ANA” must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user’s manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes, or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user’s authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier’s Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user’s manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN

"This device complies with Industry Canada’s licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d’Industrie Canada applicables aux appareils radio exempts de licence. L’exploitation est autorisée aux deux conditions suivantes:

1) l’appareil ne doit pas produire de brouillage; 2) l’utilisateur de l’appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d’en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled

to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word “Contains” or similar wording expressing the same meaning, as follows: “Contains IC: 10224A-22SC690ANA” or “where: 10224A-22SC690ANA is the module’s certification number”.

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC: 10224A-22SC690ANA " ou "où: 10224A-22SC690ANA est le numéro de certification du module".

i. the device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems;

ii. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the bands 5250-5350 MHz and 5470-5725 MHz shall be such that the equipment still complies with the e.i.r.p. limit;

iii. for devices with detachable antenna(s), the maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits as appropriate;

iv. Omnidirectional antenna is recommended

CE Statement

Regulatory Conformance

Hereby, we (Quectel Wireless Solutions Co., Ltd.) declares that the radio equipment type SC690A series are in compliance

with Directive 2014/53/EU.

RF exposure

This equipment complies with CE radiation exposure limits set forth for an uncontrolled environment.

This equipment should be installed and operated with minimum distance of 20 cm between the radiator and your body.

This device may be operated in all member states of the EU.

Observe national and local regulations where the device is used.

This device is restricted to indoor use only when operating in the 5150 to 5350 MHz,frequency range in the following countries:

AT	BE	BG	HR	CY	CZ	DK	
EE	FI	FR	DE	EL	HU	IE	
IT	LV	LT	LU	MT	NL	PL	
PT	RO	SK	SI	ES	SE	UK	

UK Regulations

Regulations 2017 (SI 2017/1206)

Declaration of Conformity

Quectel Wireless Solutions Co., Ltd. hereby declares that this WCDMA / LTE with Bluetooth, Wi-Fi and GNSS functions, SC690A series are in compliance with the essential requirements and other relevant provisions of the UK Radio Equipment Regulations 2017 (SI 2017/1206).

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of such model is currently unavailable.

2 Product Overview

The module is a series of smart LTE modules based on Android operating system and provides industrial grade performance. It supports multiple audio and video codecs, built-in high performance Adreno™ GPU 610 graphics processing unit and multiple audio and video input/output interfaces as well as abundant GPIO interfaces. Its general features are listed below:

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	LCC + LGA; 323
Dimensions	44 mm × 43 mm × 2.85 mm
Weight	12.24 g
Wireless network functions	LTE-FDD
Wi-Fi & Bluetooth functions	Wi-Fi 802.11a/b/g/n/ac & BT 5.1
GNSS functions	GNSS
Variants	SC690A-NA, SC690A-EM

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	SC690A-NA	SC690A-EM
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/B17/ B25/B26/B66	B1/B3/B7/B8/B20/B28
LTE-TDD	-	-
WCDMA	-	B1/B3/B8

GSM	-	-
GNSS	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz Galileo: 1573.5–1577.5MHz	GPS: 1575.42 ±1.023 MHz GLONASS: 1597.5–1605.8 MHz BeiDou: 1561.098 ±2.046 MHz Galileo: 1573.5–1577.5MHz
Wi-Fi	2402–2482 MHz; 5180–5825 MHz	2402–2482 MHz; 5180–5825 MHz
Bluetooth	2402–2480 MHz	2402–2480 MHz

2.2. Key Features

Table 4: Key Features

Features	Details
Application Processors	Quad-core Kryo 260 64-bit CPU @ 2.0 GHz： ● Gold cluster: Kryo cores at 2 GHz with 1 MB L2 cache ● Silver cluster: Kryo cores at 1.8 GHz with 512 KB L2 cache
Modem DSP	Hexagon DSP, dual-HVX at 1.0 GHz
GPU	Adreno GPU610 at 950 MHz, 3D graphics accelerator with 64-bit addressing
Memory	● 64 GB eMMC + 4 GB LPDDR4X SDRAM (default) ● 32 GB eMMC + 3 GB LPDDR4X SDRAM (optional)
Operating System	Android 11/12
Power Supply	● Supply voltage: 3.55–4.4 V ● Typical supply voltage: 3.8 V
LCM Interfaces	● Supports one group of 4-lane MIPI_DSI, up to 1.5 Gbps/lane. ● Supports FHD+ (1080 × 2520) @ 60 fps.
Camera Interfaces	● Supports 3 groups of 4-lane MIPI_CSI, up to 2.5 Gbps/lane ● Supports 3 cameras (4-lane + 4-lane + 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane + 1-lane) ● Supports triple ISP ● Up to 25 MP with dual ISP
Video Codec	● EVS, EVRC, EVRC-B, EVRC-WB ● G.711 and G7.729A/AB ● GSM-FR, GSM-EFR and GSM-HR ● AMR-NB, AMR-WB ● Video encoding and decoding: up to 1080P at 60 fps

Audio Interfaces	**Audio Inputs** 3 analog microphone inputs 2 digital microphone inputs **Audio Outputs** Class AB stereo headphone output Class AB earpiece differential output Class AB LINE_OUT output
Audio Codec	Supports MP3; AAC; HE AAC v1, v2; FLAC; APE; ALAC; AIFF
(U)SIM Interface	● 2 (U)SIM interfaces ● Supports USIM/SIM card: 1.8/2.95 V ● Supports Dual SIM Dual Standby (supported by default)
I2C Interface	5 I2C interfaces, used for peripherals such as TP, camera, sensor, etc.
ADC Interfaces	● 1 generic ADC interface ● Supports up to 15-bit resolution
Real Time Clock	Supported
USB Interface	● Compliant with USB 3.1 and 2.0 specifications, with transmission rates up to 5 Gbps on USB 3.1 Gen1 and 480 Mbps on USB 2.0 ● Supports USB OTG ● Used for AT command communication, data transmission, software debugging, firmware upgrade.
SD Card Interface	● Supports SD 3.0 protocol ● Supports SD card hot-plug ● Supports 1.8/2.95 V SD card
UART Interfaces	**UART5:** ● Supports RTS and CTS hardware flow control **UART1:** ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for debugging ● Default baud rate: 115200 bps
Vibrator drive interface	Drive ERM vibrator
Flashlight Interface	2 high current flash and torch LED driver: ● 1 A for flash mode and 300 mA for torch mode by default ● Maximum 1.5 A combined
Charging Interface	Used for battery voltage detection, fuel gauge, battery temperature detection
Bluetooth Features	Supports *Bluetooth 5.1* Supports BR/EDR/BLE
GNSS Features	GPS/GLONASS/BeiDou/Galileo
Antenna Interface	● ANT_MAIN

	● ANT_DRX ● ANT_WIFI/BT ● ANT_GNSS
Transmitting Power	● WCDMA: Class 3 (24 dBm + 1/ -3 dB) ● LTE-FDD: Class 3 (23 dBm ±2 dB)
LTE Features	● Supports 3GPP Rel-10 Cat 4 FDD ● Supports 1.4 to 20 MHz RF bandwidth ● Supports DL 2 × 2 MIMO ● Supports uplink QPSK, 16QAM and 64QAM modulation ● Supports downlink QPSK, 16QAM modulation ● FDD: Max 150 Mbps (DL)/ 50 Mbps (UL)
UMTS Features	● Supports 3GPP Rel-8/DC-HSDPA/HSPA+/HSDPA/HSUPA/ WCDMA ● Supported modulation: QPSK/16QAM/64QAM ● DC-HSDPA: Max 42 Mbps (DL) ● DC-HSUPA: Max 5.76 Mbps (UL) ● WCDMA: Max 384 kbps (DL)/384 kbps (UL)
WLAN Features	● 2.4 GHz; 5 GHz, ● Supports 802.11a/b/g/n/ac, maximally up to 433 Mbps ● Supports AP and STA modes
Temperature Range	● Operating temperature range [1]: -35 to +75 °C ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	Use USB interface
RoHS	All hardware components are fully compliant with EU RoHS directive

[1] Within operating temperature range, the module is 3GPP compliant.

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR4X + EMMC flash
- Radio frequency
- Peripheral interface
  -- USB interfaces
  -- (U)SIM interfaces
  -- UART interfaces
  -- SD card interface
  -- I2C interfaces
  -- ADC interfaces
  -- LCM (MIPI) interfaces
  -- TP (touch panel) interfaces
  -- Camera (MIPI) interfaces
  -- Audio interfaces

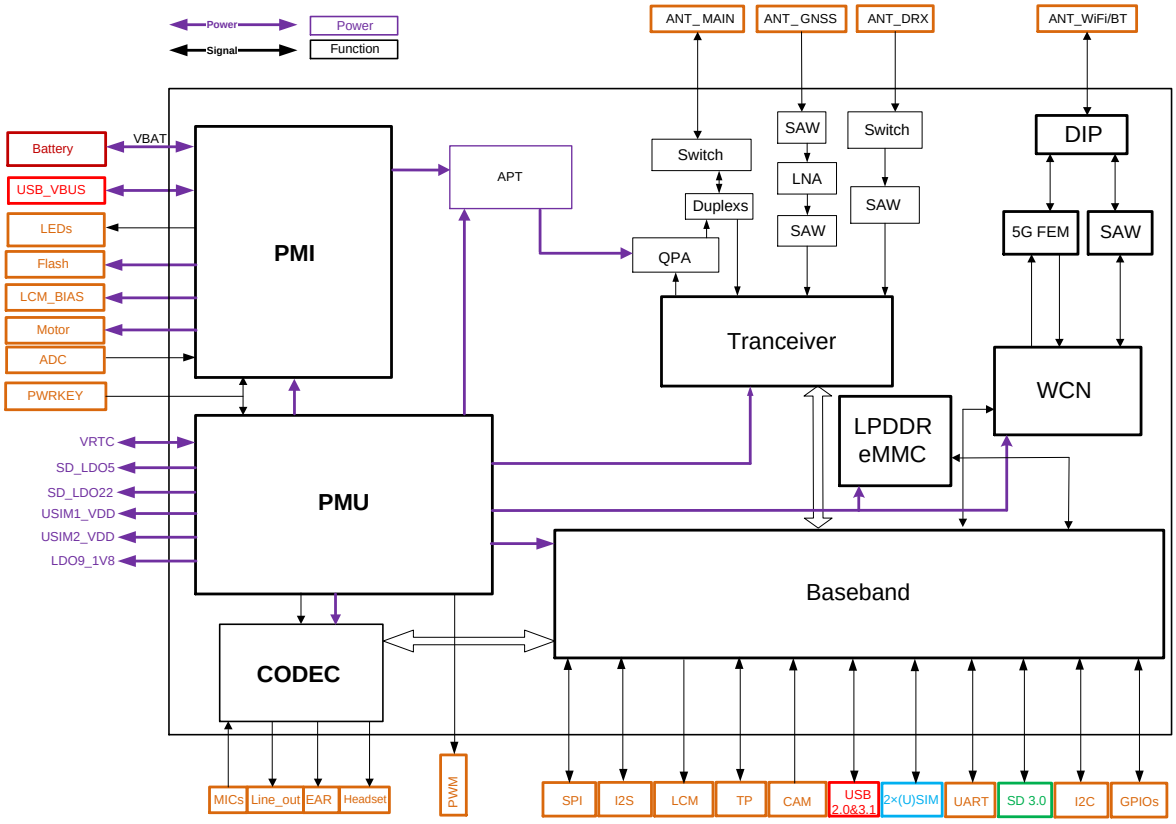


Figure 1: Functional Diagram

2.4. Pin Assignment

The following figure illustrates the pin assignment of the module.

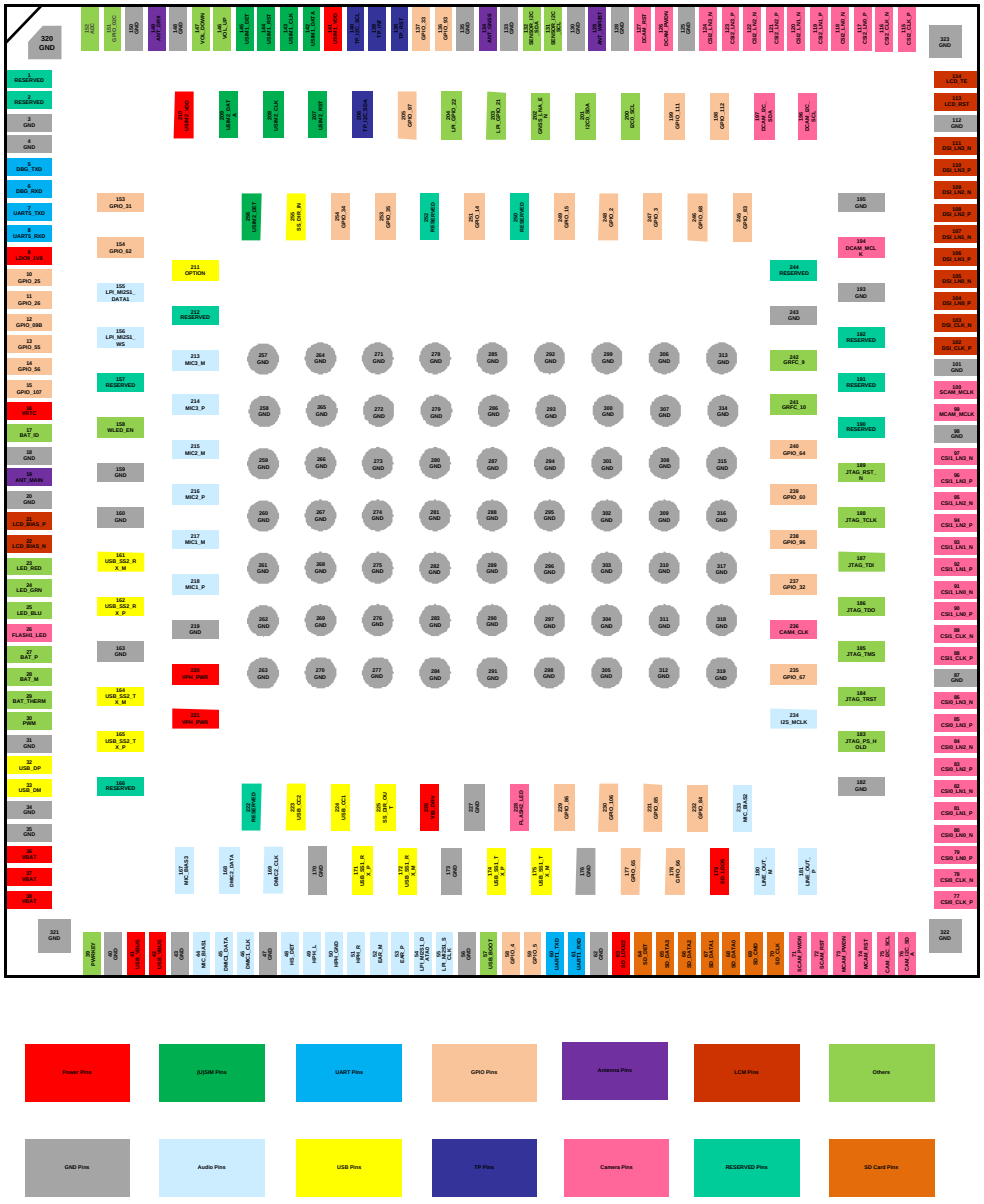


Figure 2: Pin Assignment (Top View)

NOTE

Keep all RESERVED and unused pins open.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output
PIO	Power Input/Output
PU	Pull Up
PD	Pull Down

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	36, 37, 38	PIO	Power supply for the module	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	It must be able to provide sufficient current up to 3.0 A.

					It is suggested to use a TVS to increase voltage surge withstand capability.
LDO9_1V8	9	PO	1.8 V output	Vnom = 1.8 V $I_O$max = 300 mA	Power supply for external GPIO's pull up circuits and level shift circuit.
VPH_PWR	220, 221	PO	Power supply for peripherals	Vmax = 4.4 V Vmin = 3.55 V Vnom = 3.8 V	
VRTC	16	PIO	Power supply for RTC	Vmax = 3.2 V V_I = 2.0–3.25 V	
GND	3, 4, 18, 20, 31, 34, 35, 40, 43, 47, 56, 62, 87, 98, 101, 112, 125, 128,130, 133, 135, 148, 150, 159, 160, 163, 170, 173, 176, 182, 193, 195, 219, 227, 243, 257–323				
Analog Audio Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MIC_BIAS1	44	AO	Microphone bias output voltage 1	Vmin = 1.0 V Vmax = 2.85 V	
MIC_BIAS2	233	AO	Microphone bias output voltage 2		
MIC_BIAS3	167	AO	Microphone bias output voltage 3		
MIC1_P	218	AI	Microphone input for channel 1 (+)		
MIC1_M	217	AI	Microphone input for channel 1 (-)		
MIC2_P	216	AI	Microphone input for channel 2 (+)		Used for headset mic by default.
MIC2_M	215	AI	Microphone input for channel 2 (-)		
MIC3_P	214	AI	Microphone input for channel 3 (+)		
MIC3_M	213	AI	Microphone input for channel 3 (-)		
EAR_P	53	AO	Earpiece output (+)		
EAR_M	52	AO	Earpiece output (-)		
LINE_OUT_P	181	AO	Aux amplifier output (+)		

LINE_OUT_M	180	AO	Aux amplifier output (-)		
HPH_R	51	AO	Headphone right channel output		
HPH_L	49	AO	Headphone left channel output		
HPH_GND	50	AI	Headphone reference ground		
HS_DET	48	AI	Headset hot-plug detect		Pulled up internally.
DMIC Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DMIC1_DATA	45	DIO	Digital microphone 1 data		1.8 V power domain
DMIC1_CLK	46	DO	Digital microphone 1 clock		
DMIC2_DATA	168	DIO	Digital microphone 2 data		
DMIC2_CLK	169	DO	Digital microphone 2 clock		
LED Driver Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LED_RED	23	AO	Current source for the red LED.		Sources up to 12 mA max per channel.
LED_GRN	24	AO	Current source for the green LED.		
LED_BLU	25	AO	Current source for the blue LED.		
USB Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	41, 42	PIO	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.	Vmax = 10 V Vmin = 4 V Vnom = 5.0 V	USB On-The-Go (OTG) supports up to 1.0 A.
USB_DM	33	AIO	USB 2.0 differential data (-)		USB 2.0 standard compliant. 90 Ω differential impedance.
USB_DP	32	AIO	USB 2.0 differential data (+)		

USB_SS1_RX_P	171	AI	USB 3.1 Channel 1 super-speed receive (+)		
USB_SS1_RX_M	172	AI	USB 3.1 Channel 1 super-speed receive (-)		
USB_SS1_TX_P	174	AO	USB 3.1 Channel 1 super-speed transmit (+)		
USB_SS1_TX_M	175	AO	USB 3.1 Channel 1 super-speed transmit (-)		USB 3.1 Gen1 standard compliant. 90 Ω differential impedance.
USB_SS2_RX_M	161	AI	USB 3.1 Channel 2 super-speed receive (-)		
USB_SS2_RX_P	162	AI	USB 3.1 Channel 2 super-speed receive (+)		
USB_SS2_TX_M	164	AO	USB 3.1 Channel 2 super-speed transmit (-)		
USB_SS2_TX_P	165	AO	USB 3.1 Channel 2 super-speed transmit (+)		
USB_CC1	224	AI	USB Type-C detect 1		
USB_CC2	223	AI	USB Type-C detect 2		
SS_DIR_IN	255	AI	CC status detect		USB PHY port select.
SS_DIR_OUT	225	AO	CC status output		
OPTION	211	AI	USB mode select		Select either micro-USB mode or Type-C mode.
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	141	PO	(U)SIM1 card power supply		Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM1_DATA	142	DIO	(U)SIM1 card data		

USIM1_CLK	143	DO	(U)SIM1 card clock		
USIM1_RST	144	DO	(U)SIM1 card reset		
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect		Active Low. Require external pull-up to 1.8 V. If unused, keep this pin open. Disabled by default, and can be enabled through software configuration.
USIM2_VDD	210	PO	(U)SIM2 card power supply		Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM2_DATA	209	DIO	(U)SIM2 card data		
USIM2_CLK	208	DO	(U)SIM2 card clock		
USIM2_RST	207	DO	(U)SIM2 card reset		
USIM2_DET	256	DI	(U)SIM2 card detect		Active Low. Need external pull-up to 1.8 V. If unused, keep this pin open. Disabled by default, and can be enabled through software configuration.
SD Card Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SD_CLK	70	DO	SD card clock		
SD_CMD	69	DIO	SD card command		
SD_DATA0	68	DIO	SDIO data bit 0		
SD_DATA1	67	DIO	SDIO data bit 1		
SD_DATA2	66	DIO	SDIO data bit 2		
SD_DATA3	65	DIO	SDIO data bit 3		

SD_DET	64	DI	SD card hot-plug detect		Active low.
SD_LDO22	63	PO	SD card power supply	Vnom = 2.95 V $I_O$max = 600 mA	
SD_LDO5	179	PO	1.8/2.95 V output power for SD card pull-up circuits	Vnom = 1.8/2.95 V $I_O$max = 50 mA	
Touch Panel Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
TP_RST	138	DO	TP reset		1.8 V power domain.
TP_INT	139	DI	TP interrupt		
TP_I2C_SCL	140	OD	TP I2C clock		
TP_I2C_SDA	206	OD	TP I2C data		
LCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
LCD_BIAS_P	21	PO	LCD display bias (+)	Vnom = 5.5 V Vmin = 4.0 V Vmax = 6.0 V	Positive LCD regulated output.
LCD_BIAS_N	22	PO	LCD display bias (-).	Vnom = -5.5 V Vmin = -6.0 V Vmax = -4.0 V	Negative LCD regulated output.
PWM	30	DO	PWM output		1.8 V power domain.
WLED_EN	158	DO	LCD backlight enable		1.8 V power domain.
LCD_RST	113	DO	LCD reset		1.8 V power domain. Active low.
LCD_TE	114	DI	LCD tearing effect		1.8 V power domain.
DSI_CLK_P	102	AIO	LCD MIPI clock (+)		
DSI_CLK_N	103	AIO	LCD MIPI clock (-)		
DSI_LN0_P	104	AIO	LCD MIPI lane 0 data (+)		
DSI_LN0_N	105	AIO	LCD MIPI lane 0 data (-)		

DSI_LN1_P	106	AIO	LCD MIPI lane 1 data (+)		
DSI_LN1_N	107	AIO	LCD MIPI lane 1 data (-)		
DSI_LN2_P	108	AIO	LCD MIPI lane 2 data (+)		
DSI_LN2_N	109	AIO	LCD MIPI lane 2 data (-)		
DSI_LN3_P	110	AIO	LCD MIPI lane 3 data (+)		
DSI_LN3_N	111	AIO	LCD MIPI lane 3 data (-)		
Camera Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
CSI0_CLK_P	77	AIO	MIPI clock of rear camera (+)		
CSI0_CLK_N	78	AIO	MIPI clock of rear camera (-)		
CSI0_LN0_P	79	AIO	MIPI lane 0 data of rear camera (+)		
CSI0_LN0_N	80	AIO	MIPI lane 0 data of rear camera (-)		
CSI0_LN1_P	81	AIO	MIPI lane 1 data of rear camera (+)		
CSI0_LN1_N	82	AIO	MIPI lane 1 data of rear camera (-)		
CSI0_LN2_P	83	AIO	MIPI lane 2 data of rear camera (+)		
CSI0_LN2_N	84	AIO	MIPI lane 2 data of rear camera (-)		
CSI0_LN3_P	85	AIO	MIPI lane 3 data of rear camera (+)		
CSI0_LN3_N	86	AIO	MIPI lane 3 data of rear camera (-)		
CSI1_CLK_P	88	AIO	MIPI clock of front camera (+)		
CSI1_CLK_N	89	AIO	MIPI clock of front camera (-)		
CSI1_LN0_P	90	AIO	MIPI lane 0 data of front camera (+)		
CSI1_LN0_N	91	AIO	MIPI lane 0 data of front camera (-)		

CSI1_LN1_P	92	AIO	MIPI lane 1 data of front camera (+)	
CSI1_LN1_N	93	AIO	MIPI lane 1 data of front camera (-)	
CSI1_LN2_P	94	AIO	MIPI lane 2 data of front camera (+)	
CSI1_LN2_N	95	AIO	MIPI lane 2 data of front camera (-)	
CSI1_LN3_P	96	AIO	MIPI lane 3 data of front camera (+)	
CSI1_LN3_N	97	AIO	MIPI lane 3 data of front camera (-)	
CSI2_CLK_P	115	AIO	MIPI clock of depth camera (+)	
CSI2_CLK_N	116	AIO	MIPI clock of depth camera (-)	
CSI2_LN0_P	117	AIO	MIPI lane 0 data of depth camera (+)	
CSI2_LN0_N	118	AIO	MIPI lane 0 data of depth camera (-)	
CSI2_LN1_P	119	AIO	MIPI lane 1 data of depth camera (+)	
CSI2_LN1_N	120	AIO	MIPI lane 1 data of depth camera (-)	
CSI2_LN2_P	121	AIO	MIPI lane 2 data of depth camera (+)	
CSI2_LN2_N	122	AIO	MIPI lane 2 data of depth camera (-)	
CSI2_LN3_P	123	AIO	MIPI lane 3 data of depth camera (+)	
CSI2_LN3_N	124	AIO	MIPI lane 3 data of depth camera (-)	
SCAM_MCLK	100	DO	Master clock of front camera	1.8 V power domain.
SCAM_RST	72	DO	Reset of front camera	
SCAM_PWDN	71	DO	Power down of front camera	
MCAM_MCLK	99	DO	Master clock of rear camera	
MCAM_RST	74	DO	Reset of rear camera	
MCAM_PWDN	73	DO	Power down of rear camera	

DCAM_MCLK	194	DO	Master clock of depth camera		
DCAM_RST	127	DO	Reset of depth camera		
DCAM_PWDN	126	DO	Power down of depth camera		
CAM4_MCLK	236	DO	Master clock of fourth camera		
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras		1.8 V power domain.
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras		1.8 V power domain.
DCAM_I2C_SDA	197	OD	I2C data of depth camera		1.8 V power domain.
DCAM_I2C_SCL	196	OD	I2C clock of depth camera		1.8 V power domain.
Flash Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
FLASH1_LED	26	AO	Flash/torch driver output		Support flash and torch modes. 2 × 1.5 A (maximum 1.5 A combined)
FLASH2_LED	228	AO	Flash/torch driver output		
Keypad Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	39	DI	Turn on/off the module		Pull up to 1.8 V internally. Active low.
VOL_UP	146	DI	Volume up		If unused, keep this pin open.
VOL_DOWN	147	DI	Volume down		If unused, keep this pin open.
UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_TXD	5	DO	Debug UART transmit.		1.8 V power domain.
DBG_RXD	6	DI	Debug UART receive.		

UART5_TXD	7	DO	UART5 transmit		
UART5_RXD	8	DI	UART5 receive		
UART1_TXD	60	DO	UART1 transmit		
UART1_RXD	61	DI	UART1 receive		
I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor		1.8 V power domain.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor		
I2C0_SCL	200	OD	I2C clock for external device		
I2C0_SDA	201	OD	I2C data for external device		
I2S Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2S_MCLK	234	DO	I2S master clock		1.8 V power domain.
LPI_MI2S1_SCLK	55	DO	LPI I2S1 serial clock		
LPI_MI2S1_WS	156	DO	LPI I2S1 word select		
LPI_MI2S1_DATA0	54	DIO	LPI I2S1 data channel 0		
LPI_MI2S1_DATA1	155	DIO	LPI I2S1 data channel 1		
RF Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_GNSS	134	AI	GNSS antenna interface		50 Ω impedance
ANT_MAIN	19	AIO	Main antenna interface		50 Ω impedance
ANT_DRX	149	AI	Diversity antenna interface		50 Ω impedance
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface		50 Ω impedance

Antenna Tuner Control Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC_10	241	DIO	Generic RF controller		
GRFC_9	242	DIO	Generic RF controller		
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC	152	AI	General-purpose ADC interface		Maximum input voltage: 1.875 V.
Charging Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
BAT_P	27	AI	Battery voltage detect (+)		Cannot be kept open.
BAT_M	28	AI	Battery voltage detect (-)		Cannot be kept open.
BAT_THERM	29	AI	Battery temperature detect		Internally pulled up. Externally connected to GND via a 10 kΩ NTC resistor. Maximum input voltage: 1.875 V.
BAT_ID	17	AI	Battery type detect		Maximum input voltage: 1.875 V. If unused, keep this pin open.
Vibration Motor Driver Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIB_DRV	226	PO	Vibration motor driver output control	Vmin = 1.504 V Vmax = 3.544 V Imax = 300 mA	
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

USB_BOOT	57	DI	Force the module into emergency download mode		Pulled up to LDO9_1V8 during power-up will force the module into emergency download mode.
GNSS_LNA_EN	202	DO	GNSS LNA enable control		If unused, keep this pin open.
JTAG Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
JTAG_PS_HOLD	183	DO	JTAG power-supply hold		1.8 V power domain
JTAG_TRST	184	DI	JTAG reset		
JTAG_TCLK	188	DI	JTAG clock input		
JTAG_TMS	185	DI	JTAG mode-select input		
JTAG_TDO	186	DO	JTAG data output		
JTAG_TDI	187	DI	JTAG data input		
JTAG_RST_N	189	DI	JTAG reset for debug		
Reserved Interface					
Pin Name	**Pin No.**				**Comment**
RESERVED	1, 2, 157, 166, 190, 191, 192, 212, 222, 244, 250, 252				Keep these pins open.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO_2	248	DIO	General-purpose input/output		1.8 V power domain.
GPIO_3	247	DIO	General-purpose input/output		
GPIO_4	58	DIO	General-purpose input/output		
GPIO_5	59	DIO	General-purpose input/output		
GPIO_14	251	DIO	General-purpose input/output		

GPIO_15	249	DIO	General-purpose input/output	
GPIO_25	10	DIO	General-purpose input/output	
GPIO_26	11	DIO	General-purpose input/output	
GPIO_31	153	DIO	General-purpose input/output	
GPIO_32	237	DIO	General-purpose input/output	
GPIO_33	137	DIO	General-purpose input/output	
GPIO_34	254	DIO	General-purpose input/output	
GPIO_35	253	DIO	General-purpose input/output	
GPIO_55	13	DIO	General-purpose input/output	
GPIO_56	14	DIO	General-purpose input/output	
GPIO_60	239	DIO	General-purpose input/output	
GPIO_62	154	DIO	General-purpose input/output	
GPIO_64	240	DIO	General-purpose input/output	
GPIO_65	177	DIO	General-purpose input/output	
GPIO_66	178	DIO	General-purpose input/output	1.8 V power domain.
GPIO_67	235	DIO	General-purpose input/output	
GPIO_68	246	DIO	General-purpose input/output	
GPIO_83	245	DIO	General-purpose input/output	
GPIO_84	232	DIO	General-purpose input/output	
GPIO_85	231	DIO	General-purpose input/output	
GPIO_86	229	DIO	General-purpose input/output	
GPIO_93	136	DIO	General-purpose input/output	

GPIO_96	238	DIO	General-purpose input/output		
GPIO_97	205	DIO	General-purpose input/output		
GPIO_106	230	DIO	General-purpose input/output		
GPIO_107	15	DIO	General-purpose input/output		
GPIO_111	199	DIO	General-purpose input/output		
GPIO_112	198	DIO	General-purpose input/output		
LPI_GPIO_21	203	DIO	General-purpose input/output		Only used for audio and sensor, cannot be used as ordinary GPIO port
LPI_GPIO_22	204	DIO	General-purpose input/output		
GPIO_09B	12	DO	General-purpose output of PM1		PMU's GPIO Used for enabling some power only.
GPIO_02C	151	DIO	General-purpose input/output of PM2		Power domain: 1.8 V or VPH_PWR

2.6. EVB

To help you to develop applications with the module conveniently, Quectel supplies an evaluation board (EVB), USB data cable, earphone, antenna, and other peripherals to control or to test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Power Supply

3.1.1. Power Supply Pins

The module provides 3 VBAT pins, and 2 VPH_PWR pins. VBAT pins must be connected to an external power supply to power the module. VPH_PWR pins are used to power other devices.

3.1.2. Battery Charge and Management

The module can recharge batteries. The battery charger in the module supports trickle charging, constant current charging and constant voltage charging modes, which optimize the charging procedure for Li-ion batteries.

- **Trickle charging:** When the battery voltage is below 2.1 V, a 75 mA trickle charging current is applied to the battery.
- **Pre-charge mode:** When the battery voltage is charged up and is between 2.1 V and 3.0 V (the maximum pre-charge voltage is 2.4–3.0 V programmable, 3.0 V by default), the system will enter into pre-charge mode. The charging current is 450 mA (100–450 mA programmable, 450 mA by default).
- **Constant current mode (CC mode):** When the battery is increased to 3 V, the system will switch to CC mode. The maximum charging current is 3000 mA when an adapter is used for battery charging, and the maximum charging current is 500 mA for USB charging.
- **Constant voltage mode (CV mode):** When the battery voltage reaches the final value 4.35 V, the system will switch to CV mode and the charging current will decrease gradually. When the battery level reaches 100 %, the charging is completed.

Table 7: Pin Definition of Charging Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	PIO	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.	USB On-The-Go (OTG) supports up to 1.0 A.

VBAT	36, 37, 38	PIO	Power supply for the module	It must be able to provide sufficient current up to 3.0 A. It is suggested to use a TVS to increase voltage surge withstand capability.
BAT_P	27	AI	Battery voltage detect (+)	Cannot be kept open.
BAT_M	28	AI	Battery voltage detect (-)	Cannot be kept open.
BAT_THERM	29	AI	Battery temperature detect	Internally pulled up. Externally connected to GND via a 10 kΩ NTC resistor. Maximum input voltage: 1.875 V.
BAT_ID	17	AI	Battery type detect	Maximum input voltage: 1.875 V. If unused, keep this pin open.

The module supports battery temperature detection in the condition that the battery integrates a thermistor (10 kΩ 1 % NTC thermistor with a B-constant of 4050 by default; and the thermistor is connected to BAT_THERM pin, or there will be malfunctions such as battery charging failure, battery level display error, etc.

A reference design for the battery charging circuit is shown below.

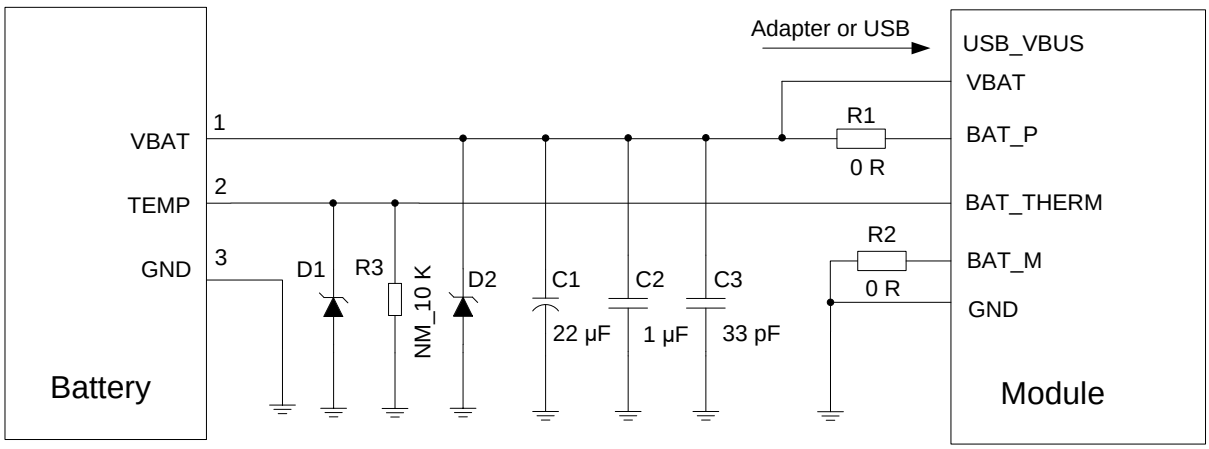


Figure 3: Reference Design for Battery Charging Circuit

Mobile devices such as mobile phones and handheld POS systems are powered by batteries. When different batteries are utilized, the charging and discharging curve must be modified correspondingly to achieve the best effect.

If the thermistor is not available in the battery, or an adapter is utilized for powering the module, then there is only a need for connecting VBAT and GND. In this case, the system may mistakenly judge that

the battery temperature is abnormal, which will cause battery charging failure. To avoid this, BAT_THERM should be connected to GND via a 10 kΩ resistor. If BAT_THERM is unconnected, the system will be unable to detect the battery, and the battery will not be charged.

BAT_P/M must be connected. Otherwise, the module will have trouble in voltage detection, as well as associated power on/off issues and battery charging/discharging issues.

3.1.3. Reference Design for Power Supply

The power design for the module is very important, as the performance of the module largely depends on the power source. The power supply of the module should be able to provide sufficient current of at least 3 A. If the voltage drop between the input and output is not too big, it is suggested to use an LDO to supply power for the module. If there is a big voltage difference between the input source and the desired output (VBAT), a buck converter is recommended.

The following figure shows a reference design for +5V input power source. The designed output of the power supply is about 3.8 V and the maximum rated current is 5 A.

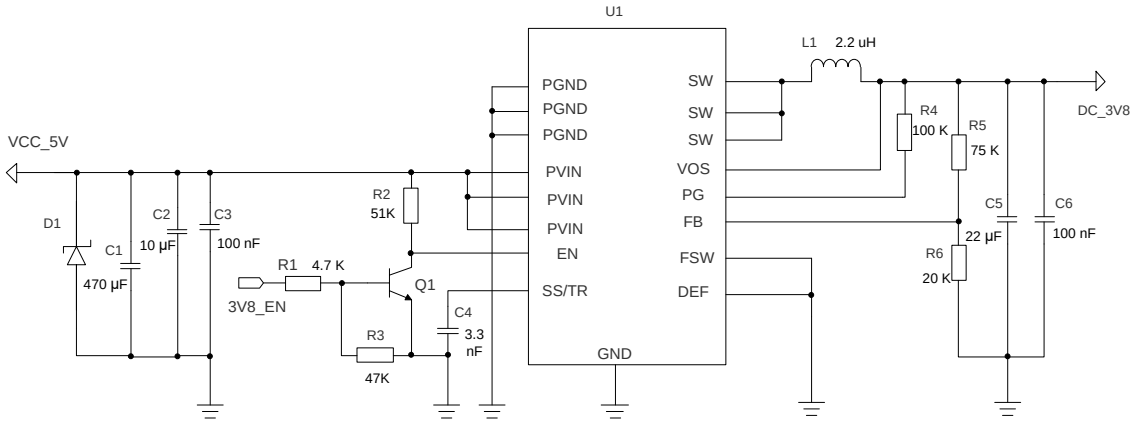


Figure 4: Reference Circuit of Power Supply

NOTE

To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.

3.1.4. Requirements for Voltage Stability

The power supply range of the module is from 3.55 V to 4.4 V, and the recommended value is 3.8 V. The power supply performance, such as load capacity, voltage ripple, etc. directly influences the module's performance and stability. Under ultimate conditions, the module may have a transient peak current of

up to 3 A. If the power supply capability is not sufficient, there will be voltage drops, and if the voltage drops below 3.1 V, the module will power off automatically. Therefore, ensure that the input voltage never drops below 3.1 V.

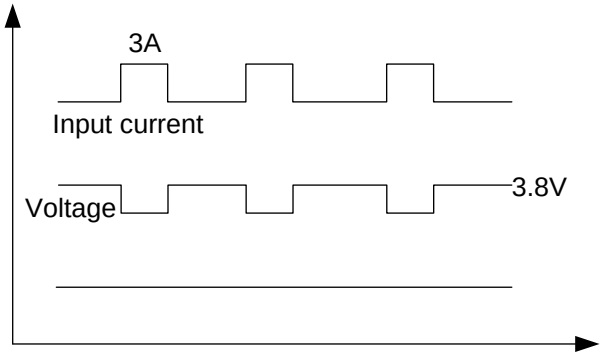


Figure 5: Voltage Drop Sample

To prevent the voltage from dropping below 3.1 V, use a bypass capacitor of about 100 µF with low ESR (ESR = 0.7 Ω), and reserve a multi-layer ceramic chip capacitor (MLCC) array due to its ultra-low ESR. It is recommended to use three ceramic capacitors (100 nF, 33 pF, 10 pF) to compose the MLCC array, and place these capacitors close to VBAT pins. Additionally, add a 4.7 µF capacitor in parallel. The width of VBAT trace should be no less than 3 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to get a stable power source, it is suggested to use a 2000 W TVS and place it as close to the VBAT pins as possible to enhance surge protection.

The following figure shows the structure of the power supply.

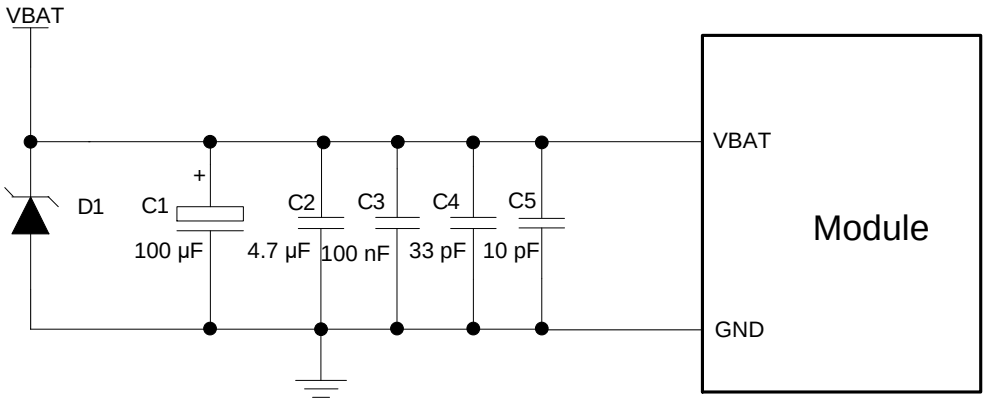


Figure 6: Structure of Power Supply

3.2. Turn on

Table 8: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	39	DI	Turn on/off the module	Pull up to 1.8 V internally. Active low.

The module can be turned on by driving the PWRKEY pin to a low level for at least 1.6 s. PWRKEY pin is pulled to 1.8 V internally.

It is recommended to use an open drain/collector driver to control the PWRKEY. A simple reference circuit is illustrated in the following figure.

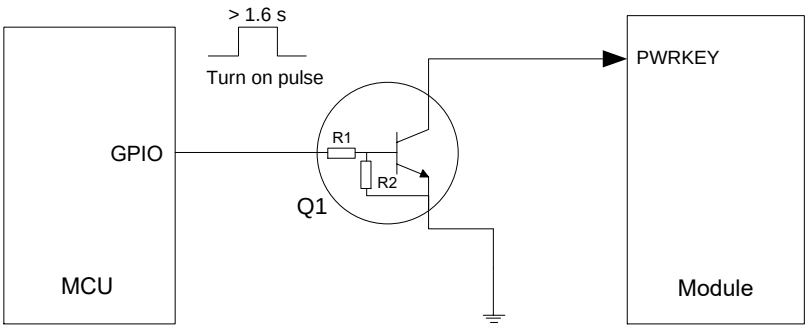


Figure 7: Turn on the Module Using Driving Circuit

The other way to control the PWRKEY is by using a button directly. A TVS component is indispensable to be placed nearby the button for ESD protection. A reference circuit is shown in the following figure.

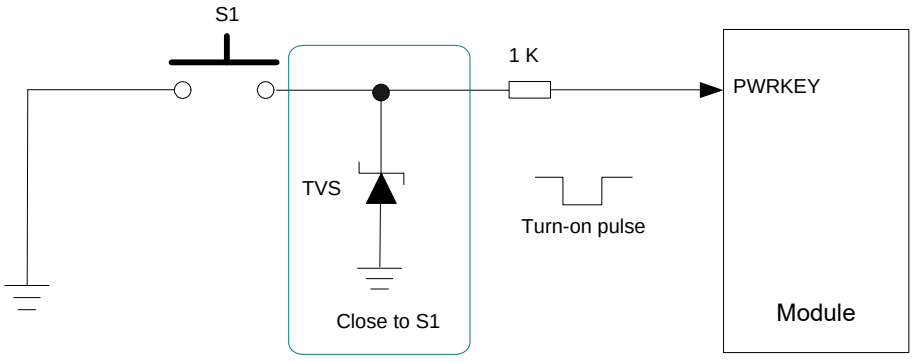


Figure 8: Turn on the Module Using Keystroke

The turning on the scenario is illustrated in the following figure.

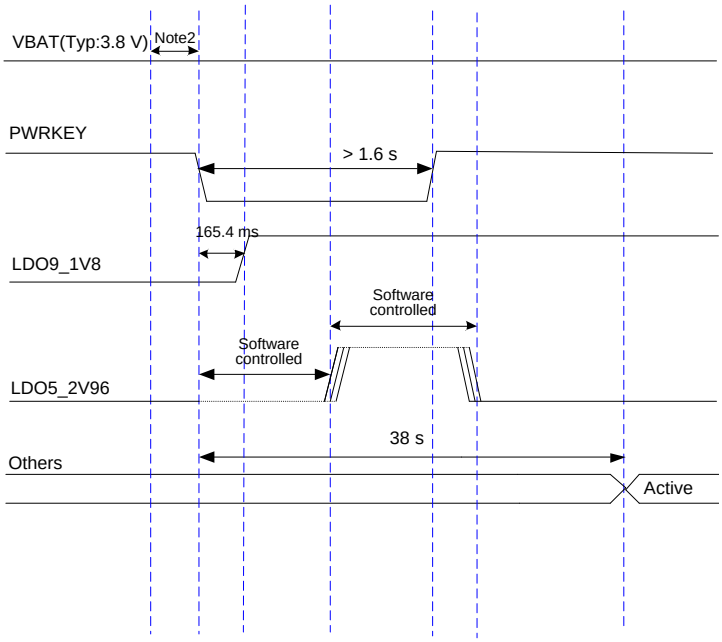


Figure 9: Timing of Turning on Module

NOTE

1. When the module is powered on for the first time, its timing of turning on may be different from that shown above.
2. Ensure that VBAT is stable before pulling down the PWRKEY pin. It is recommended to wait until VBAT to be stable at 3.8 V for at less 30 ms before pulling down PWRKEY. Additionally, PWRKEY cannot be pulled down all the time.

3.3. Turn off

Set the PWRKEY pin low for at least 1 s, and then choose to turn off the module when the prompt window comes up.

The other way to turn off the module is to drive PWRKEY to a low level for at least 8 s. The module will execute the forced shutdown. The forced power-down scenario is illustrated in the following figure.

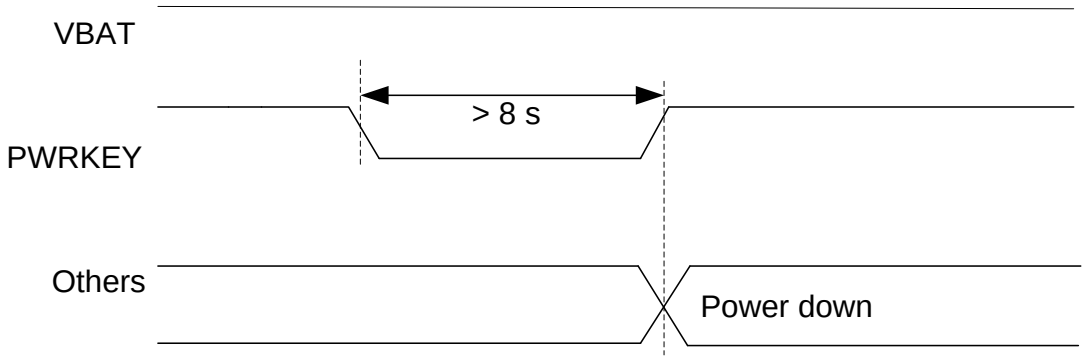


Figure 10: Timing of Turning off Module

3.4. VRTC Interface

The RTC (Real Time Clock) can be powered by an external power source through VRTC when the module is powered down and there is no power supply for the VBAT. The external power source can be a capacitor according to application demands. The following figure shows the reference circuit when an external battery is utilized for powering RTC.

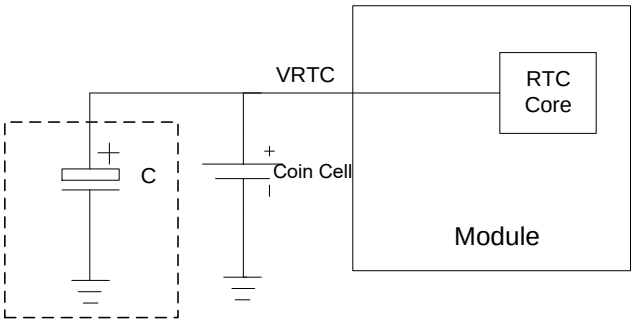


Figure 11: RTC Powered by Coin Cell

- When VBAT is disconnected, the recommended input voltage range for VRTC is 2.0–3.25 V and the recommended typical value is 3.0 V.
- When powered by VBAT, the RTC error is 50 ppm. When powered by VRTC, the RTC error is about 200 ppm.
- If a rechargeable battery is used, ESR of the battery should be less than 2 kΩ.
- If RTC function is not needed, it is recommended to connect a 0.1 μF capacitor to VRTC.

3.5. Power Output

The module supports output of regulated voltages for peripheral circuits. During application, it is recommended to connect a 33 pF and a 10 pF capacitor in parallel to suppress high-frequency noise.

Table 9: Power Description

Pin Name	Default Voltage (V)	Drive Current (mA)	Standby
LDO9_1V8	1.8	300	Keeps ON
SD_LDO5	1.8/2.95	50	-
SD_LDO22	2.95	600	-
USIM1_VDD	1.8/2.95	50	-
USIM2_VDD	1.8/2.95	50	-
VPH_PWR	VBAT	2000	Keeps ON

4 Application Interfaces

4.1. USB Interfaces

The module provides one USB interface(s): USB Type-C. The USB interface complies with the USB 3.1 Gen1 and USB 2.0 specifications, and supports SuperSpeed (5 Gbps) for USB 3.1 Gen1, High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) for USB 2.0. The USB interface supports USB OTG function, and is used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 10: Functions of the USB Interface

Functions	
Data communication with external AP	√
AT command communication	√
Data transmission	√
GNSS NMEA output	-
Software debugging	√
Firmware upgrade	√
Voice over USB	-

NOTE

“ √ ” means supported; “-” means not supported.

Table 11: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	41, 42	PIO	Charging power input. Power supply for OTG device. USB/adaptor insertion detection.	USB On-The-Go (OTG) supports up to 1.0 A.
USB_DM	33	AIO	USB 2.0 differential data (-)	USB 2.0 standard compliant. 90 Ω differential impedance.
USB_DP	32	AIO	USB 2.0 differential data (+)	
USB_SS1_RX_P	171	AI	USB 3.1 Channel 1 super-speed receive (+)	Compliant with USB 3.1 Gen1 specification. 90 Ω differential impedance.
USB_SS1_RX_M	172	AI	USB 3.1 Channel 1 super-speed receive (-)	
USB_SS1_TX_P	174	AO	USB 3.1 Channel 1 super-speed transmit (+)	
USB_SS1_TX_M	175	AO	USB 3.1 Channel 1 super-speed transmit (-)	
USB_SS2_RX_M	161	AI	USB 3.1 Channel 2 super-speed receive (-)	
USB_SS2_RX_P	162	AI	USB 3.1 Channel 2 super-speed receive (+)	
USB_SS2_TX_M	164	AO	USB 3.1 Channel 2 super-speed transmit (-)	
USB_SS2_TX_P	165	AO	USB 3.1 Channel 2 super-speed transmit (+)	
USB_CC1	224	AI	USB Type-C detect 1	
USB_CC2	223	AI	USB Type-C detect 2	
SS_DIR_IN	255	AI	CC status detect	USB PHY port select.
SS_DIR_OUT	225	AO	CC status output	
OPTION	211	AI	USB mode select	Select either micro-USB mode or Type-C mode.

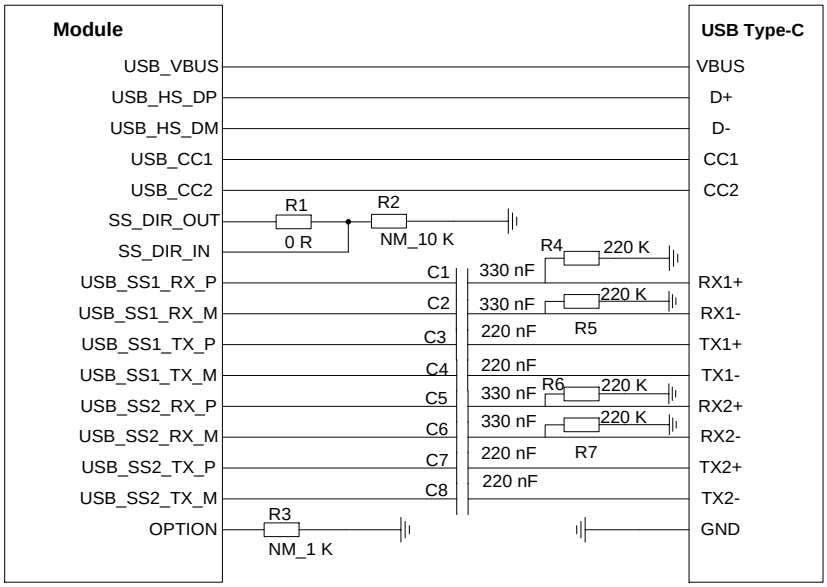


Figure 12: USB Type-C Interface Reference Design

To ensure USB performance, please comply with the following principles while designing USB interface.

- It is important to route the USB signal traces as differential pairs with total grounding. The impedance of USB differential trace is 90 Ω.
- Pay attention to the influence of junction capacitance of ESD protection devices on USB data traces. Typically, the capacitance value should be less than 2 pF for USB 2.0 and less than 0.5 pF for USB 3.1 Gen1.
- Do not route signal traces under crystals, oscillators, magnetic devices, and RF signal traces. It is important to route the USB differential traces in inner-layer with ground shielding on not only upper and lower layers but also right and left sides.
- Keep the ESD protection devices as close as possible to the USB connector.
- Ensure the trace length difference between USB_DM/DP and that between USB 3.1 Gen1 RX/TX differential pairs do not exceed 0.7 mm.
- If micro USB is supported, R1 = NM, R2 = 10 K, R3 = 1 K. If USB Type-C is supported, R2/R3 = NM, R1 = 0 R.

Table 12: USB Trace Length Inside the Module

Pin No.	Signal	Length (mm)	Length Difference (DP-DM)
33	USB_DM	38.16	-0.22
32	USB_DP	38.38	

171	USB_SS1_RX_P	26.12	0.32
172	USB_SS1_RX_M	25.80	
174	USB_SS1_TX_P	25.53	0.02
175	USB_SS1_TX_M	25.51	
161	USB_SS2_RX_M	30.25	-0.33
162	USB_SS2_RX_P	30.58	
164	USB_SS2_TX_M	35.50	0.25
165	USB_SS2_TX_P	35.25	

4.2. UART Interfaces

The module provides 3 UART interfaces:

- **UART5:** 4-wire UART interface, hardware flow control supported.
- **UART1:** 4-wire UART interface, hardware flow control supported.
- **Debug UART :** 2-wire UART interface; used for debugging by default.

Pin definition of the UART interfaces is here as follows:

Table 13: Pin Definition of UART Interfaces

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	5	DO	Debug UART transmit.	1.8 V power domain.
DBG_RXD	6	DI	Debug UART receive.	
UART5_TXD	7	DO	UART5 transmit	
UART5_RXD	8	DI	UART5 receive	
GPIO_15	249	DO	General-purpose input/output	Can be multiplexed into UART5_RTS.
GPIO_14	251	DI	General-purpose input/output	Can be multiplexed into UART5_CTS.
UART1_TXD	60	DO	UART1 transmit	

UART1_RXD	61	DI	UART1 receive	
GPIO_4	58	DI	General-purpose input/output	Can be multiplexed into UART1_CTS.
GPIO_5	59	DO	General-purpose input/output	Can be multiplexed into UART1_RTS.

UART5 is a 4-wire UART interface with 1.8 V power domain. A level translator chip should be used if your application is equipped with a 3.3 V UART interface. A level translator chip is recommended. The following figure shows a reference design.

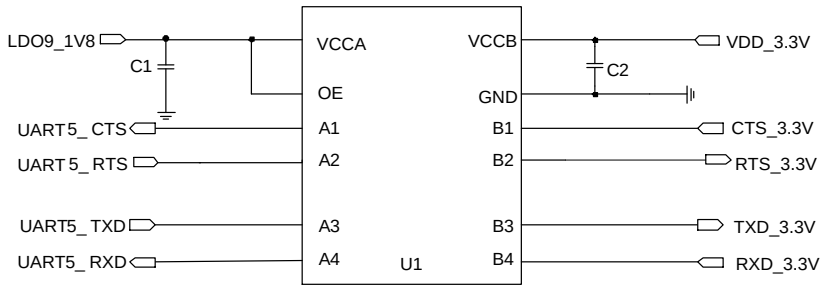


Figure 13: Reference Circuit with Level Translator Chip (for UART5)

The following figure is an example of connection between the module and PC. A voltage level translator and an RS-232 level translator chip are recommended to be added between the module and PC, as shown below:

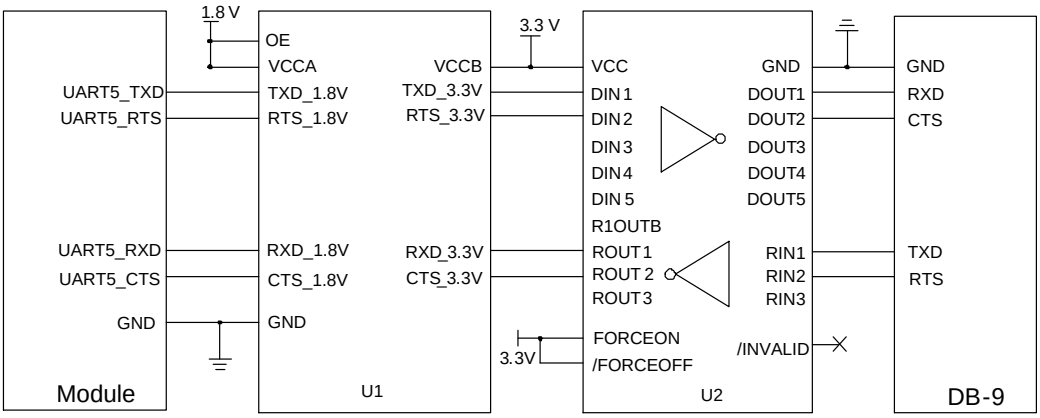


Figure 14: RS-232 Level Match Circuit (for UART5)

NOTE

The reference circuit of debug UART and UART1 is similar to that of UART5.

4.3. (U)SIM Interfaces

The module provides two (U)SIM interfaces which meet ETSI and IMT-2000 requirements. Dual SIM Dual Standby is supported by default. Either 1.8 V or 2.95 V (U)SIM card is supported, and the (U)SIM interfaces are powered by the dedicated low dropout regulators in the module.

Table 14: Pin Definition of (U)SIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	141	PO	(U)SIM1 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM1_DATA	142	DIO	(U)SIM1 card data	
USIM1_CLK	143	DO	(U)SIM1 card clock	
USIM1_RST	144	DO	(U)SIM1 card reset	
USIM1_DET	145	DI	(U)SIM1 card hot-plug detect	Active Low. Require external pulled up to 1.8 V. If unused, keep this pin open. Disabled by default, and can be enabled through software configuration.
USIM2_VDD	210	PO	(U)SIM2 card power supply	Either 1.8 V or 2.95 V (U)SIM card is supported.
USIM2_DATA	209	DIO	(U)SIM2 card data	
USIM2_CLK	208	DO	(U)SIM2 card clock	
USIM2_RST	207	DO	(U)SIM2 card reset	
USIM2_DET	256	DI	(U)SIM2 card detect	Active Low. Require external pulled up to 1.8 V. If unused, keep this pin open. Disabled by default, and can be enabled through software configuration.

The module supports (U)SIM card hot-plug via the USIM_DET pin, which is disabled by default and can be enabled through software configuration. A reference circuit for (U)SIM interface with an 8-pin (U)SIM card connector is shown below.

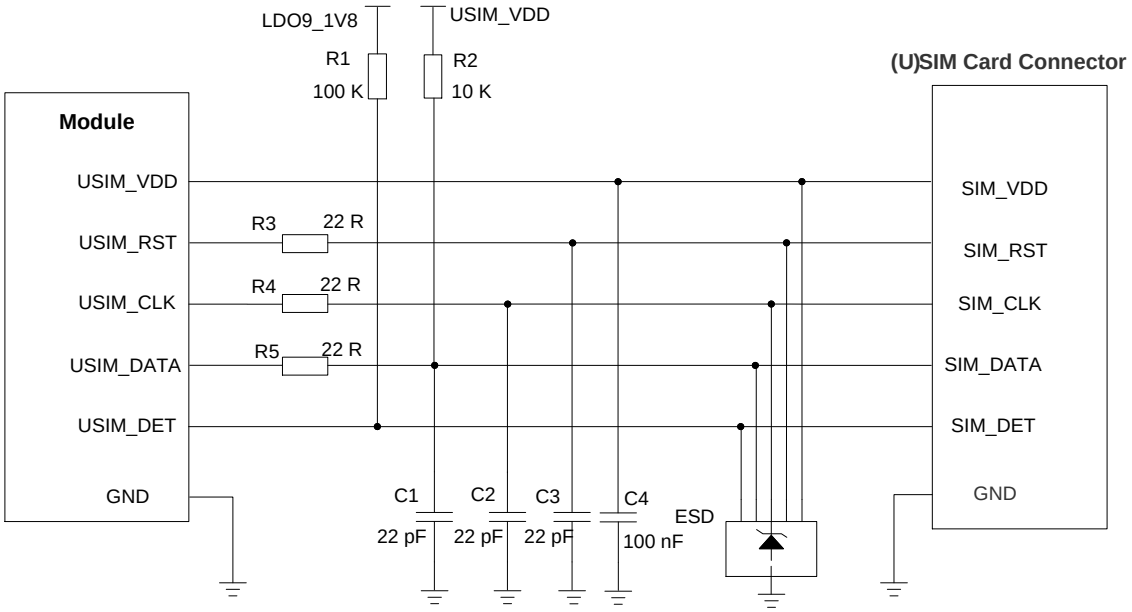


Figure 15: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Keep (U)SIM card connector as close as possible to the module. Keep the trace length as less than 200 mm as possible.
- Keep (U)SIM card signal traces away from RF and VBAT traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- For better ESD protection, it is recommended to add a TVS diode array with a parasitic capacitance not exceeding 50 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection.
- The pull-up resistor on USIM_DATA trace improves anti-jamming capability and should be placed close to the (U)SIM card connector.
- Add 22 pF capacitors parallel on USIM_DATA, USIM_CLK and USIM_RST signal traces to filter RF interference, and place them as close to the (U)SIM card connector as possible.

4.4. SD Card Interface

The module supports SD 3.0 specifications. The pin definition of the SD card interface is shown below.

Table 15: Pin Definition of SD Card Interface

Pin Name	Pin No.	I/O	Description	Comment
SD_CLK	70	DO	SD card clock	
SD_CMD	69	DIO	SD card command	
SD_DATA0	68	DIO	SDIO data bit 0	
SD_DATA1	67	DIO	SDIO data bit 1	
SD_DATA2	66	DIO	SDIO data bit 2	
SD_DATA3	65	DIO	SDIO data bit 3	
SD_DET	64	DI	SD card hot-plug detect	Active low.
SD_LDO22	63	PO	SD card power supply	
SD_LDO5	179	PO	1.8/2.95 V output power for SD card pull-up circuits	

A reference circuit for SD card interface is shown below.

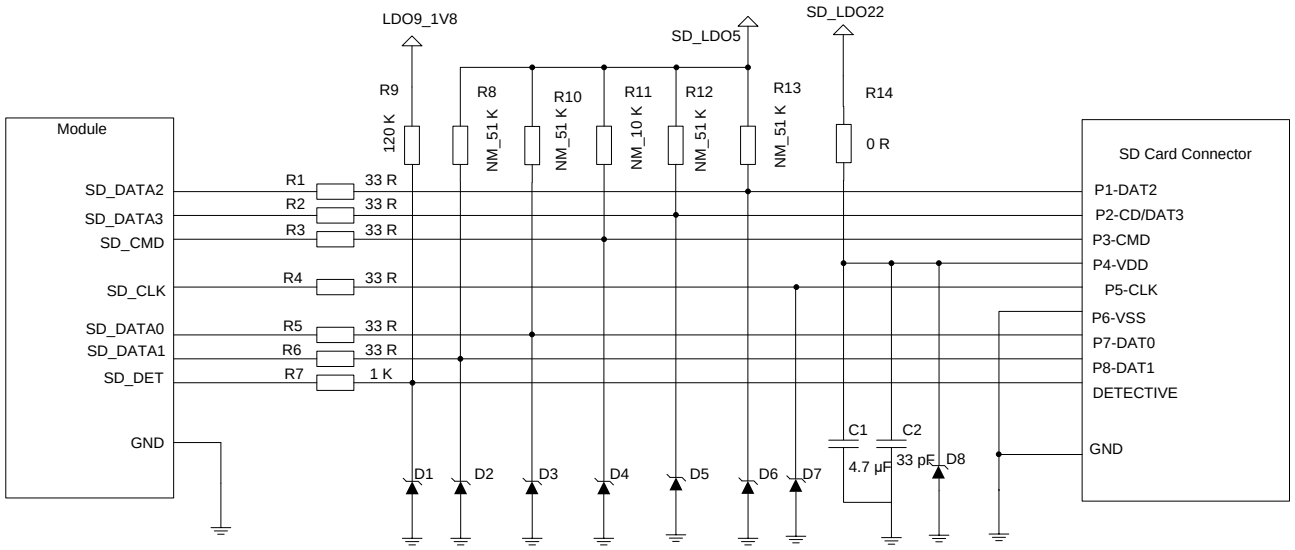


Figure 16: Reference Circuit for SD Card Interface

SD_LDO22 is a peripheral driver power supply for SD card. The maximum drive current is 600 mA. Because of the high drive current, it is recommended that the trace width is 0.5 mm or above. To ensure the stability of drive power, add a 4.7 μF and a 33 pF capacitor in parallel near the SD card connector.

SD_CMD, SD_CLK, SD_DATA0, SD_DATA1, SD_DATA2 and SD_DATA3 are all high-speed signal traces. In PCB design, control the characteristic impedance of them as 50 Ω, and do not cross them with other traces. It is recommended to route these traces on the inner layer of PCB, and keep them of the same length. Additionally, SD_CLK needs separate ground shielding.

Layout guidelines:

- Control impedance to 50 Ω ±10 %, and add ground shielding.
- The trace length difference between SD_CLK and other traces like SD_CMD and SD_DATA should be less than 1 mm.

Table 16: SD Card Signal Trace Length Inside the Module

Pin No.	Signal	Length (mm)
70	SD_CLK	48.98
69	SD_CMD	48.82
68	SD_DATA0	48.42
67	SD_DATA1	48.54
66	SD_DATA2	48.60
65	SD_DATA3	50.34

4.5. GPIO Interfaces

The module has abundant GPIO interfaces with power domain of 1.8 V. The pin definition is listed below.

Table 17: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO_2	248	DIO	General-purpose input/output	

GPIO_3	247	DIO	General-purpose input/output	1.8 V power domain.
GPIO_4	58	DIO	General-purpose input/output	
GPIO_5	59	DIO	General-purpose input/output	
GPIO_14	251	DIO	General-purpose input/output	
GPIO_15	249	DIO	General-purpose input/output	
GPIO_25	10	DIO	General-purpose input/output	
GPIO_26	11	DIO	General-purpose input/output	
GPIO_31	153	DIO	General-purpose input/output	
GPIO_32	237	DIO	General-purpose input/output	
GPIO_33	137	DIO	General-purpose input/output	
GPIO_34	254	DIO	General-purpose input/output	
GPIO_35	253	DIO	General-purpose input/output	
GPIO_55	13	DIO	General-purpose input/output	
GPIO_56	14	DIO	General-purpose input/output	
GPIO_60	239	DIO	General-purpose input/output	
GPIO_62	154	DIO	General-purpose input/output	
GPIO_64	240	DIO	General-purpose input/output	
GPIO_65	177	DIO	General-purpose input/output	
GPIO_66	178	DIO	General-purpose input/output	1.8 V power domain.
GPIO_67	235	DIO	General-purpose input/output	
GPIO_68	246	DIO	General-purpose input/output	
GPIO_83	245	DIO	General-purpose input/output	

GPIO_84	232	DIO	General-purpose input/output	
GPIO_85	231	DIO	General-purpose input/output	
GPIO_86	229	DIO	General-purpose input/output	
GPIO_93	136	DIO	General-purpose input/output	
GPIO_96	238	DIO	General-purpose input/output	
GPIO_97	205	DIO	General-purpose input/output	
GPIO_106	230	DIO	General-purpose input/output	
GPIO_107	15	DIO	General-purpose input/output	
GPIO_111	199	DIO	General-purpose input/output	
GPIO_112	198	DIO	General-purpose input/output	
LPI_GPIO_21	203	DIO	General-purpose input/output	Only used for audio and sensor.
LPI_GPIO_22	204	DIO	General-purpose input/output	
GPIO_09B	12	DO	General-purpose output of PM1	PMU's GPIO Used for enabling some power only.
GPIO_02C	151	DIO	General-purpose input/output of PM2	Power domain: 1.8 V or VPH_PWR

4.6. I2C Interfaces

The module provides up to five I2C Interfaces. All I2C interfaces are open drain signals and therefore you must pull them up externally. The reference power domain is 1.8 V. The SENSOR_I2C interface only supports sensors of the DSP architecture. The CAM_I2C interface supports connection with video output related devices.

Table 18: Pin Definition of I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	131	OD	I2C clock for external sensor	1.8 V power domain.
SENSOR_I2C_SDA	132	OD	I2C data for external sensor	
I2C0_SCL	200	OD	I2C clock for external device	
I2C0_SDA	201	OD	I2C data for external device	
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras	
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras	
DCAM_I2C_SCL	196	OD	I2C clock of depth camera	
DCAM_I2C_SDA	197	OD	I2C data of depth camera	
TP_I2C_SCL	140	OD	TP I2C clock	
TP_I2C_SDA	206	OD	TP I2C data	

4.7. I2S Interfaces

The module provides two I2S interfaces, which are low-power I2S. Data signals of both interfaces can be configured as input or output, and the reference power domain of the interfaces is 1.8 V. LPI_MI2S0 interface is multiplexed from DMIC interface*.

Table 19: Pin Definition of I2S Interfaces

Pin Name	Pin No.	I/O	Description	Comment
I2S_MCLK	234	DO	I2S master clock	1.8 V power domain.
LPI_MI2S1_SCLK	55	DO	LPI I2S1 serial clock	
LPI_MI2S1_WS	156	DO	LPI I2S1 word select	
LPI_MI2S1_DATA0	54	DIO	LPI I2S1 data channel 0	
LPI_MI2S1_DATA1	155	DIO	LPI I2S1 data channel 1	
LPI_MI2S0_CLK	46	DO	LPI I2S0 serial clock	

LPI_MI2S0_WS	45	DO	LPI I2S0 word select
LPI_MI2S0_DATA0	169	DIO	LPI I2S0 data channel 0
LPI_MI2S0_DATA1	168	DIO	LPI I2S0 data channel 1

4.8. ADC Interface

The module provides one analog-to-digital converter (ADC) interface which support up to 15-bit resolution, and the pin definition is shown below.

Table 20: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC	152	AI	General-purpose ADC interface	Maximum input voltage: 1.875 V.

4.9. LCM Interfaces

The module provides an LCM interface, which is MIPI_DSI standard compliant. The interface supports high-speed differential data transmission and supports FHD+ display (1080 × 2520 @ 60 fps). The maximum rate up to 1.5 Gbps/lane. The pin definition of the LCM interface is shown below.

Table 21: Pin Definition of LCM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
LCD_BIAS_P	21	PO	LCD display bias (+)	Positive LCD regulated output.
LCD_BIAS_N	22	PO	LCD display bias (-).	Negative LCD regulated output.
PWM	30	DO	PWM output	1.8 V power domain.
WLED_EN	158	DO	LCD backlight enable	1.8 V power domain.
LCD_RST	113	DO	LCD reset	1.8 V power domain. Active low.
LCD_TE	114	DI	LCD tearing effect	1.8 V power domain.

DSI_CLK_P	102	AIO	LCD MIPI clock (+)
DSI_CLK_N	103	AIO	LCD MIPI clock (-)
DSI_LN0_P	104	AIO	LCD MIPI lane 0 data (+)
DSI_LN0_N	105	AIO	LCD MIPI lane 0 data (-)
DSI_LN1_P	106	AIO	LCD MIPI lane 1 data (+)
DSI_LN1_N	107	AIO	LCD MIPI lane 1 data (-)
DSI_LN2_P	108	AIO	LCD MIPI lane 2 data (+)
DSI_LN2_N	109	AIO	LCD MIPI lane 2 data (-)
DSI_LN3_P	110	AIO	LCD MIPI lane 3 data (+)
DSI_LN3_N	111	AIO	LCD MIPI lane 3 data (-)

The following figures show the reference design for LCM interface.

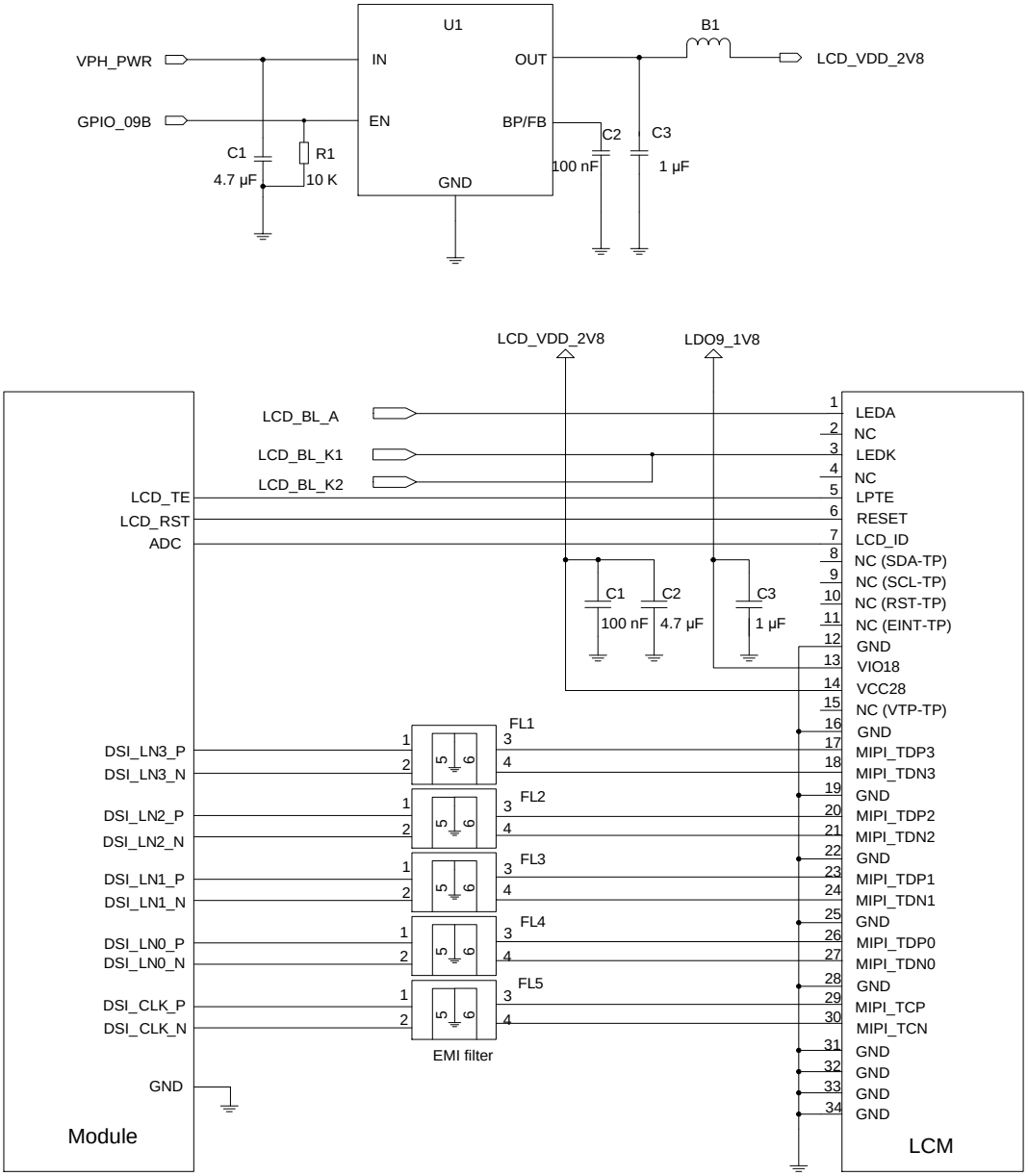


Figure 17: Reference Circuit Design for LCM Interface

MIPI are high speed signal lines. It is recommended to add common-mode filters in series near the LCM connector to improve protection against electromagnetic radiation interference.

It is recommended to read the LCM ID register through MIPI when compatible design with other displays is required. If several LCMs share the same IC, it is recommended that LCM module factory should burn an OTP register to distinguish different screens. You can also connect the LCD_ID pin of LCM to the ADC pin of the module, but please note that the output voltage of LCD_ID should not exceed the voltage range of the ADC pin.

You can design external backlight drive circuit for LCM according to actual requirement. The reference designs are shown in the figures below, in which PWM is used for backlight brightness adjustment.

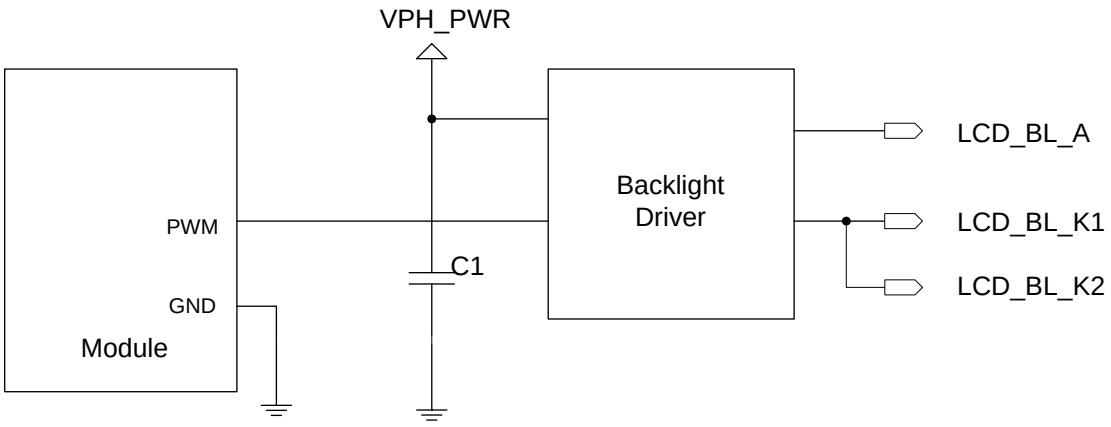


Figure 18: LCM External Backlight Driver Reference Circuit

NOTE

LCM is powered by LCD_VDD_2V8, which is an external LDO power supply.

4.10. Touch Panel Interface

The module provides one I2C interface for connection with touch panel (TP), and provides the corresponding power supply and interrupt pins. The pin definition of touch panel interfaces is illustrated below.

Table 22: Pin Definition of Touch Panel Interfaces

Pin Name	Pin No.	I/O	Description	Comment
TP_RST	138	DO	TP reset	1.8 V power domain.
TP_INT	139	DI	TP interrupt	
TP_I2C_SCL	140	OD	TP I2C clock	
TP_I2C_SDA	206	OD	TP I2C data	

A reference design for TP interface is shown below.

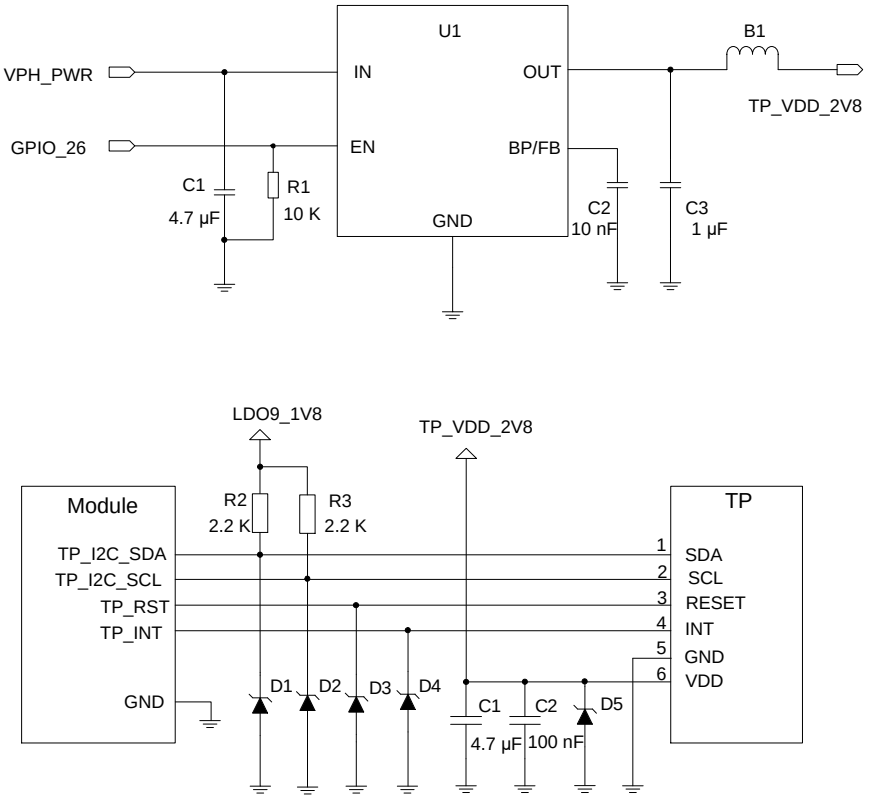


Figure 19: Reference Circuit Design for TP Interface

NOTE

TP is powered by TP_VDD_2V8, which is an external LDO power supply.

4.11. Camera Interfaces

Based on the standard MIPI CSI video input interface, the module supports 3 cameras (4-lane + 4-lane+ 4-lane) or 4 cameras (4-lane + 4-lane + 2-lane+ 1-lane), and the maximum pixel of the camera can be up to 25 MP. The video and photo quality are determined by various factors such as the camera sensor, camera lens quality, etc.

Table 23: Pin Definition of Camera Interfaces

Pin Name	Pin No.	I/O	Description	Comment
CSI0_CLK_P	77	AIO	MIPI clock of rear camera (+)	
CSI0_CLK_N	78	AIO	MIPI clock of rear camera (-)	
CSI0_LN0_P	79	AIO	MIPI lane 0 data of rear camera (+)	
CSI0_LN0_N	80	AIO	MIPI lane 0 data of rear camera (-)	
CSI0_LN1_P	81	AIO	MIPI lane 1 data of rear camera (+)	
CSI0_LN1_N	82	AIO	MIPI lane 1 data of rear camera (-)	
CSI0_LN2_P	83	AIO	MIPI lane 2 data of rear camera (+)	
CSI0_LN2_N	84	AIO	MIPI lane 2 data of rear camera (-)	
CSI0_LN3_P	85	AIO	MIPI lane 3 data of rear camera (+)	
CSI0_LN3_N	86	AIO	MIPI lane 3 data of rear camera (-)	
CSI1_CLK_P	88	AIO	MIPI clock of front camera (+)	
CSI1_CLK_N	89	AIO	MIPI clock of front camera (-)	
CSI1_LN0_P	90	AIO	MIPI lane 0 data of front camera (+)	
CSI1_LN0_N	91	AIO	MIPI lane 0 data of front camera (-)	
CSI1_LN1_P	92	AIO	MIPI lane 1 data of front camera (+)	
CSI1_LN1_N	93	AIO	MIPI lane 1 data of front camera (-)	
CSI1_LN2_P	94	AIO	MIPI lane 2 data of front camera (+)	
CSI1_LN2_N	95	AIO	MIPI lane 2 data of front camera (-)	
CSI1_LN3_P	96	AIO	MIPI lane 3 data of front camera (+)	
CSI1_LN3_N	97	AIO	MIPI lane 3 data of front camera (-)	
CSI2_CLK_P	115	AIO	MIPI clock of depth camera (+)	
CSI2_CLK_N	116	AIO	MIPI clock of depth camera (-)	
CSI2_LN0_P	117	AIO	MIPI lane 0 data of depth camera (+)	
CSI2_LN0_N	118	AIO	MIPI lane 0 data of depth camera (-)	

CSI2_LN1_P	119	AIO	MIPI lane 1 data of depth camera (+)	
CSI2_LN1_N	120	AIO	MIPI lane 1 data of depth camera (-)	
CSI2_LN2_P	121	AIO	MIPI lane 2 data of depth camera (+)	
CSI2_LN2_N	122	AIO	MIPI lane 2 data of depth camera (-)	
CSI2_LN3_P	123	AIO	MIPI lane 3 data of depth camera (+)	
CSI2_LN3_N	124	AIO	MIPI lane 3 data of depth camera (-)	
SCAM_MCLK	100	DO	Master clock of front camera	1.8 V power domain.
SCAM_RST	72	DO	Reset of front camera	
SCAM_PWDN	71	DO	Power down of front camera	
MCAM_MCLK	99	DO	Master clock of rear camera	
MCAM_RST	74	DO	Reset of rear camera	
MCAM_PWDN	73	DO	Power down of rear camera	
DCAM_MCLK	194	DO	Master clock of depth camera	
DCAM_RST	127	DO	Reset of depth camera	
DCAM_PWDN	126	DO	Power down of depth camera	
CAM4_MCLK	236	DO	Master clock of fourth camera	
CAM_I2C_SCL	75	OD	I2C clock of front and rear cameras	1.8 V power domain.
CAM_I2C_SDA	76	OD	I2C data of front and rear cameras	1.8 V power domain.
DCAM_I2C_SDA	197	OD	I2C data of depth camera	1.8 V power domain.
DCAM_I2C_SCL	196	OD	I2C clock of depth camera	1.8 V power domain.

The following is a reference circuit design for three-camera applications.

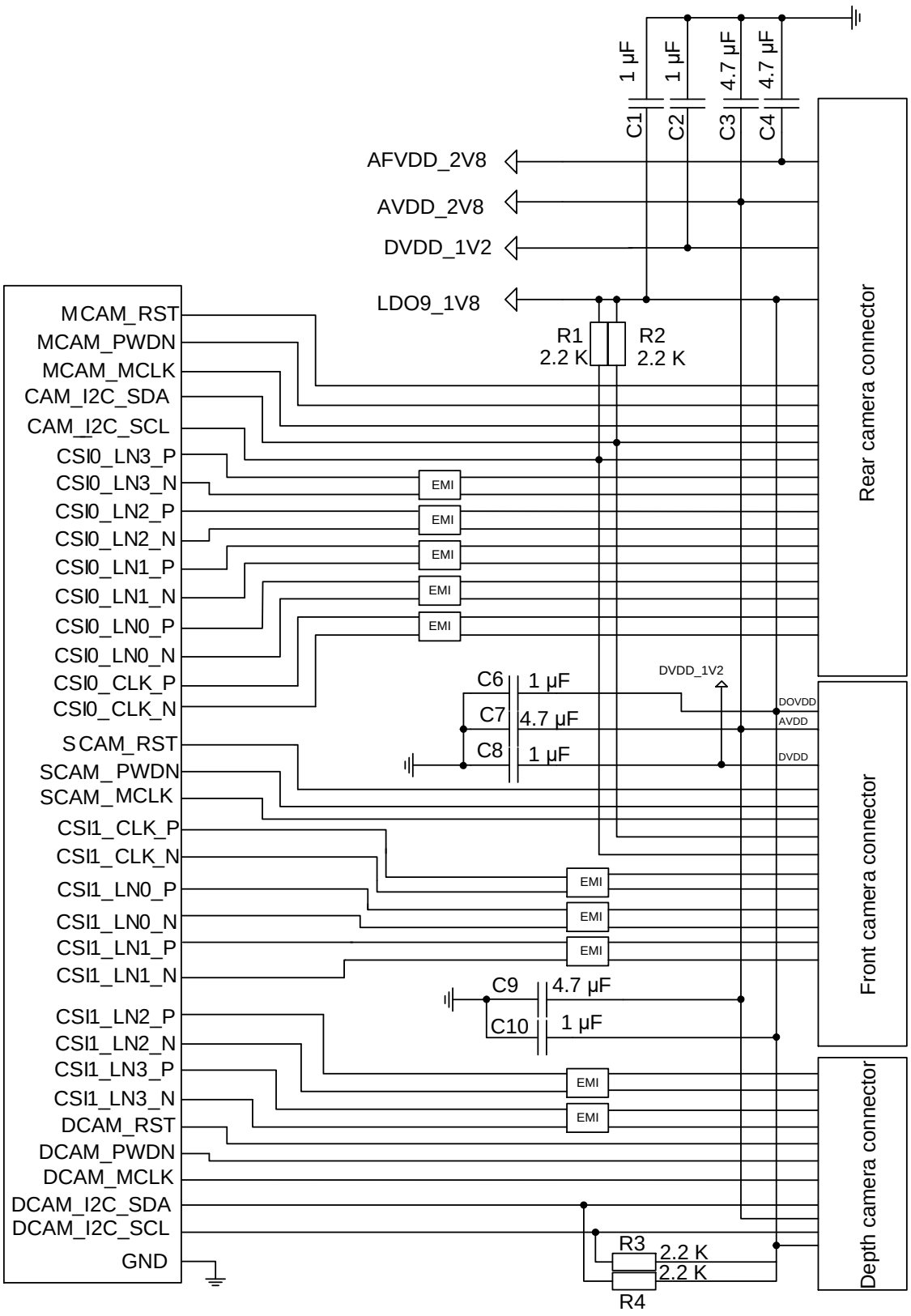


Figure 20: Reference Circuit Design for Three-Camera Applications

NOTE

CSI0 is used for rear camera, CSI1 for front camera and depth camera. Refer to the reference circuit of CSI0 for that of CSI2.

The camera interfaces are powered by an external power supply. The reference circuit design is as follows:

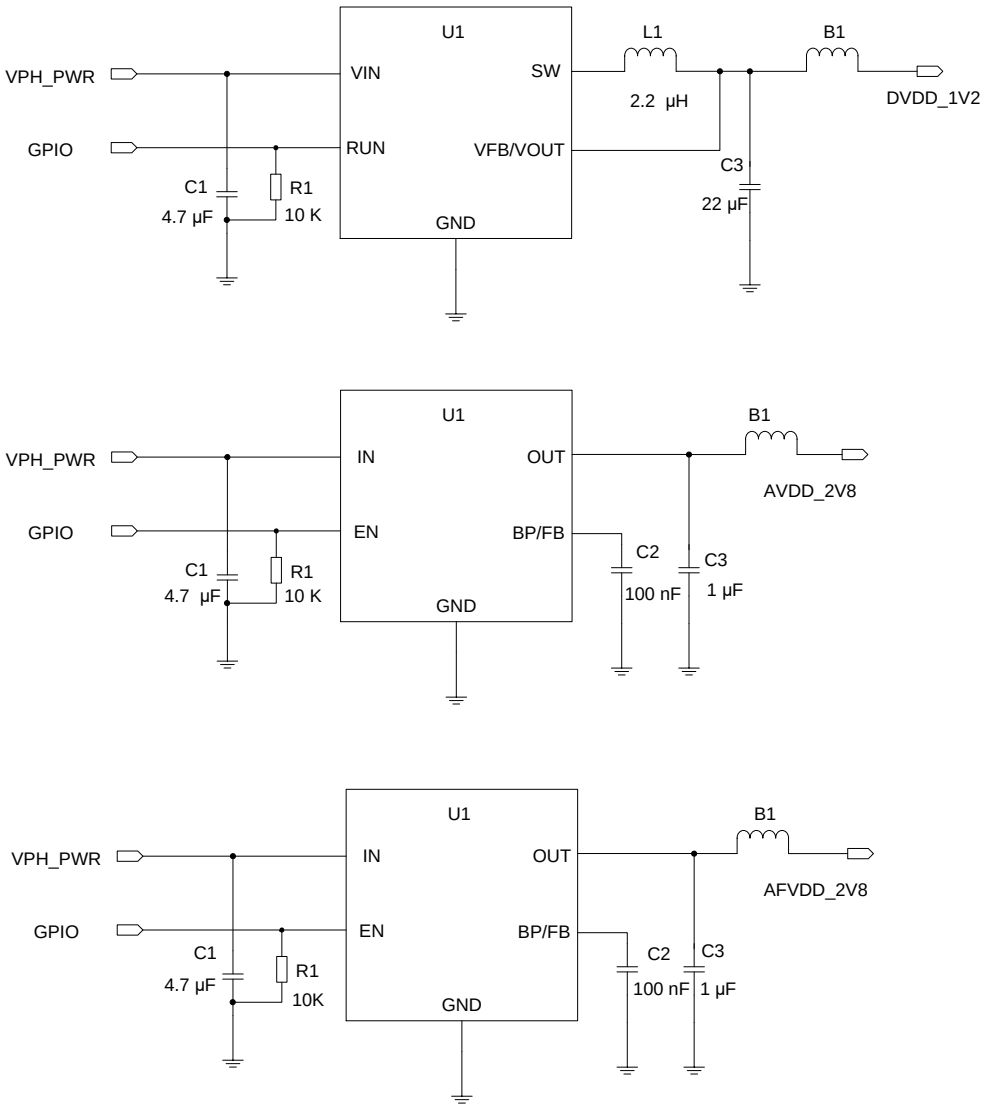


Figure 21: Reference Circuit Design for Camera Power Supply

- Special attention should be paid to the pin definition of LCM/camera connectors. Ensure the module and the connectors are correctly connected.
- MIPI is high speed signal traces, supporting maximum data rate up to 2.5 Gbps. The differential

impedance should be controlled to 85 Ω. Additionally, it is recommended to route the trace on the inner layer of PCB, and do not cross it with other traces. For the same group of DSI or CSI signals, all the MIPI traces should keep the same length. To avoid crosstalk, a distance of 1.5 times the trace width among MIPI signal traces is recommended. During impedance matching, do not connect GND on different planes to ensure impedance consistency.

- It is recommended to select a low capacitance TVS for ESD protection and the recommended parasitic capacitance should be below 1 pF.
- Route MIPI traces according to the following rules:

  a) The total trace length should not exceed 150 mm;
  b) Control the differential impedance to 85 Ω ±10 %;
  c) Control intra-pair length difference within 0.7 mm;
  d) Control inter-pair length difference within 1.4 mm.

Table 24: MIPI Trace Length Inside the Module

Pin Name	Pin No	Length (mm)	Length Difference (P-N)
DSI_CLK_N	103	50.71	0.35
DSI_CLK_P	102	50.37	
DSI_LN0_N	105	50.28	-0.30
DSI_LN0_P	104	50.58	
DSI_LN1_N	107	50.32	0.32
DSI_LN1_P	106	50.00	
DSI_LN2_N	109	50.20	-0.29
DSI_LN2_P	108	50.49	
DSI_LN3_N	111	50.43	0.27
DSI_LN3_P	110	50.16	
CSI0_CLK_N	78	20.54	0.28
CSI0_CLK_P	77	20.26	
CSI0_LN0_N	80	20.75	0.00
CSI0_LN0_P	79	20.74	
CSI0_LN1_N	82	20.79	0.35

CSI0_LN1_P	81	20.45	
CSI0_LN2_N	84	20.84	0.20
CSI0_LN2_P	83	20.65	
CSI0_LN3_N	86	21.17	0.16
CSI0_LN3_P	85	21.01	
CSI1_CLK_N	89	13.17	0.06
CSI1_CLK_P	88	13.10	
CSI1_LN0_N	91	12.82	0.00
CSI1_LN0_P	90	12.82	
CSI1_LN1_N	93	12.97	0.29
CSI1_LN1_P	92	12.68	
CSI1_LN2_N	95	12.82	-0.17
CSI1_LN2_P	94	12.99	
CSI1_LN3_N	97	13.02	0.34
CSI1_LN3_P	96	12.6	
CSI2_CLK_N	116	29.77	0.23
CSI2_CLK_P	115	29.54	
CSI2_LN0_N	118	29.65	0.25
CSI2_LN0_P	117	29.40	
CSI2_LN1_N	120	29.64	0.28
CSI2_LN1_P	119	29.36	
CSI2_LN2_N	122	29.37	-0.16
CSI2_LN2_P	121	29.53	
CSI2_LN3_N	124	29.76	0.31
CSI2_LN3_P	123	29.45	

4.12. Sensor Interfaces

The module supports communication with sensors via I2C interface, and it supports various sensors such as acceleration sensor, gyroscopic sensor, compass, light sensor, temperature sensor, etc.

Table 25: Pin Definition of Sensor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
SENSOR_I2C_SCL	131	OD	I2C clock signal of external sensor	1.8 V power domain.
SENSOR_I2C_SDA	132	OD	I2C data signal of external sensor	1.8 V power domain.
GPIO_35	253	DI	Can be multiplexed into ALPS_INT, used as light sensor interrupt	
GPIO_34	254	DI	Can be multiplexed into MAG_INT, used as geomagnetic sensor interrupt	
GPIO_33	137	DI	Can be multiplexed into GYRO_INT, used as gyroscopic sensor interrupt	
GPIO_32	237	DI	Can be multiplexed into ACCEL_INT, used as acceleration sensor interrupt	

4.13. Flash Interfaces

The module supports 2 flash LED drivers, with maximal output current up to 1.5 A per channel. The default output current is 1000 mA in flash mode and 300 mA in torch mode.

Table 26: Pin Definition of Flash Interfaces

Pin Name	Pin No.	I/O	Description	Comment
FLASH1_LED	26	AO	Flash/torch driver output	Support flash and torch modes. 2 × 1.5 A (maximum 1.5 A combined)
FLASH2_LED	228	AO	Flash/torch driver output	

A reference circuit design is shown below.

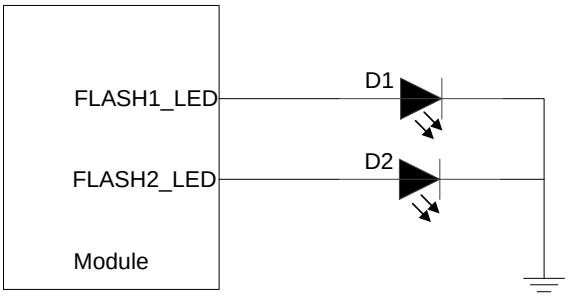


Figure 26: Reference Circuit Design for Flashlight Interfaces

4.14. Keypad Interfaces

The module supports three keypads: PWRKEY for turning module on/off and VOL_UP and VOL_DOWN to adjust the volume.

Table 27: Pin Definition of Keypad Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	39	DI	Turn on/off the module	Pull up to 1.8 V internally. Active low.
VOL_UP	146	DI	Volume up	If unused, keep this pin open.
VOL_DOWN	147	DI	Volume down	If unused, keep this pin open.

4.15. Vibration Driver Motor Interfaces

The module supports eccentric rotating machines (ERM). The pin definition of vibrator drive interface is listed below.

Table 28: Pin Definition of Vibration Driver Motor Interfaces

Pin Name	Pin No.	I/O	Description	Comment
VIB_DRV	226	PO	Vibration motor driver	

	output control

The vibrator is driven by an exclusive circuit, and a reference circuit design is shown below.

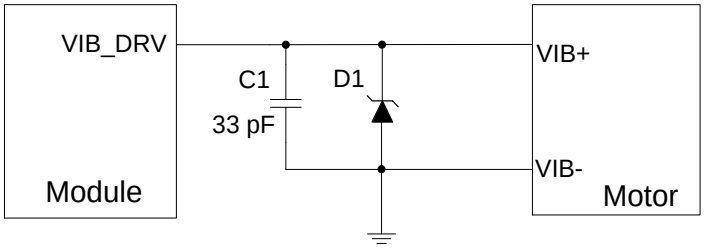


Figure 22: Reference Circuit for Vibrator Connection

4.16. JTAG Interface

Table 29: Pin Definition of JTAG Interface

Pin Name	Pin No.	I/O	Description	Comment
JTAG_PS_HOLD	183	DO	JTAG power-supply hold	
JTAG_TRST	184	DI	JTAG reset	
JTAG_TCLK	188	DI	JTAG clock input	
JTAG_TMS	185	DI	JTAG mode-select input	
JTAG_TDO	186	DO	JTAG data output	
JTAG_TDI	187	DI	JTAG data input	
JTAG_RST_N	189	DI	JTAG reset for debug	

4.17. LED Driver Interface

The following is the pin definition of LED driver interfaces.

Table 30: Pin Definition of LED Driver Interface

Pin Name	Pin No.	I/O	Description	Comment
LED_RED	23	AO	Current source for the red LED.	Sources up to 12 mA max per channel.
LED_GRN	24	AO	Current source for the green LED.	
LED_BLU	25	AO	Current source for the blue LED.	

A reference circuit design for LED interfaces is shown below.

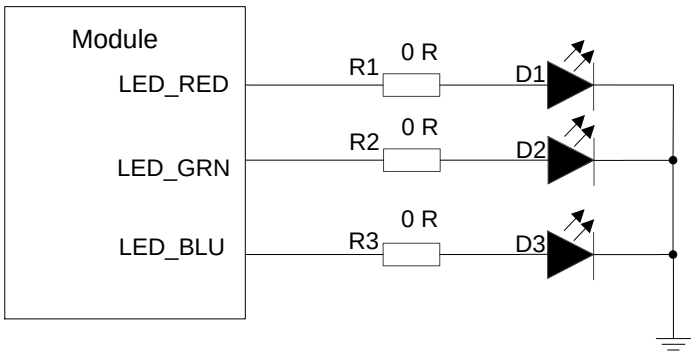


Figure 23: Reference Circuit Design for LED Interfaces

4.18. Audio Interfaces

The module provides three pairs of analog input/output channels and two digital input/output channels. channels. The following table shows the pin definition.

Table 31: Pin Definition of Audio Interfaces

Pin Name	Pin No.	I/O	Description	Comment
DMIC1_DATA	45	DIO	Digital microphone 1 data	

DMIC1_CLK	46	DO	Digital microphone 1 clock	
DMIC2_DATA	168	DIO	Digital microphone 2 data	
DMIC2_CLK	169	DO	Digital microphone 2 clock	
MIC_BIAS1	44	AO	Microphone bias output voltage 1	
MIC_BIAS2	233	AO	Microphone bias output voltage 2	
MIC_BIAS3	167	AO	Microphone bias output voltage 3	
MIC1_P	218	AI	Microphone input for channel 1 (+)	Used for ECM microphone by default. MIC1_P require pulled up to MIC_BIAS1.
MIC1_M	217	AI	Microphone input for channel 1 (-)	
MIC2_P	216	AI	Microphone input for channel 2 (+)	Used for headset microphone by default. MIC2_P require pulled up to MIC_BIAS2.
MIC2_M	215	AI	Microphone input for channel 2 (-)	
MIC3_P	214	AI	Microphone input for channel 3 (+)	Used for MEMS microphone by default. MIC3_P require pulled up to MIC_BIAS3.
MIC3_M	213	AI	Microphone input for channel 3 (-)	
EAR_P	53	AO	Earpiece output (+)	
EAR_M	52	AO	Earpiece output (-)	
LINE_OUT_P	181	AO	Aux amplifier output (+)	
LINE_OUT_M	180	AO	Aux amplifier output (-)	
HPH_R	51	AO	Headphone right channel output	
HPH_L	49	AO	Headphone left channel output	
HPH_GND	50	AI	Headphone reference ground	
HS_DET	48	AI	Headset hot-plug detect	Pulled up internally.

- The module offers five audio input/output channels, including two digital channels and three analog channels.
- The output voltage range of MIC_BIAS is programmable between 1.0 V and 2.85 V, and the maximum output current is 3 mA.
- The earpiece interface uses differential output.
- LINE_OUT for audio external speaker amplifier.
- The headset interface features stereo left and right channel output, and headset insert detection function is supported.

4.18.1. Reference Circuit Design for Microphone Interfaces

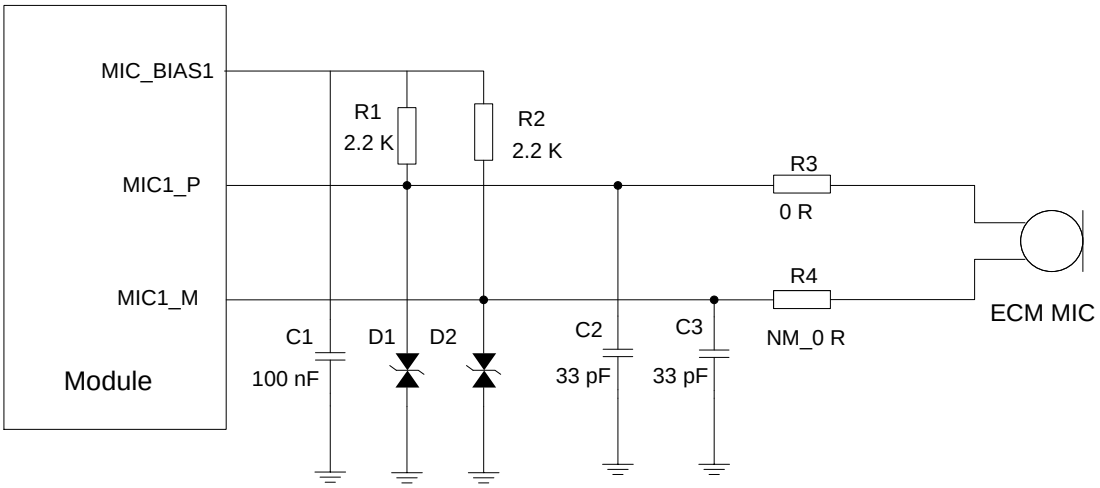


Figure 24: Reference Circuit Design for ECM Microphone Interfaces

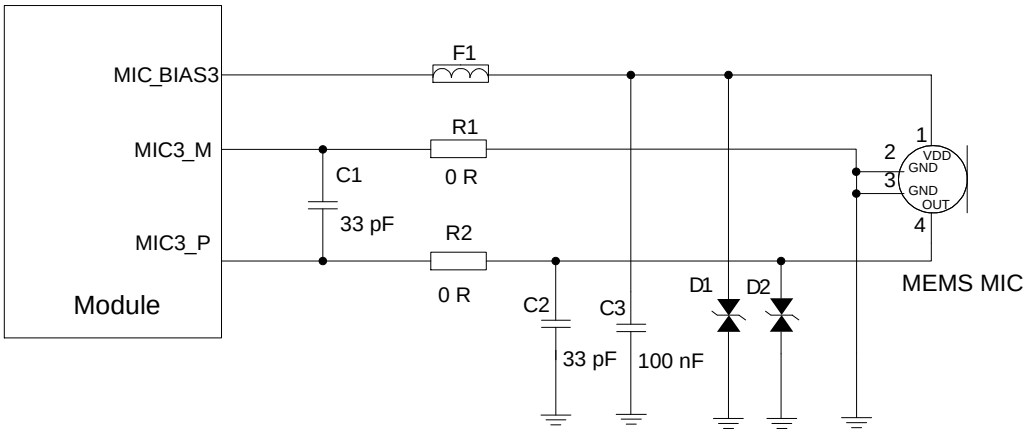


Figure 25: Reference Circuit Design for MEMS Microphone Interfaces

4.18.2. Reference Circuit Design for Receiver Interface

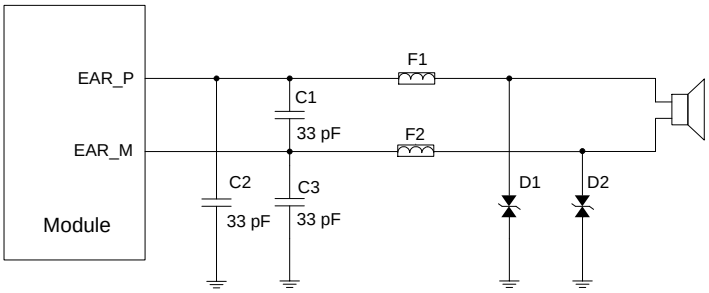


Figure 26: Reference Circuit Design for Receiver Interface

4.18.3. Reference Circuit Design for Headset Interface

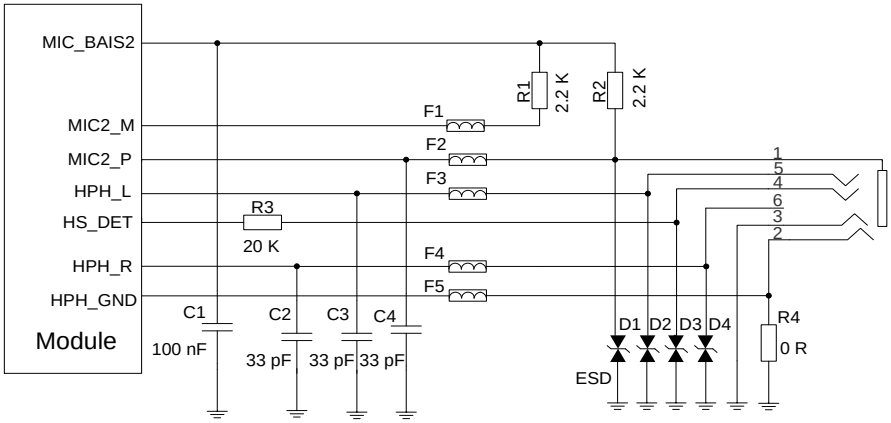


Figure 27: Reference Circuit Design for Headset Interface

4.18.4. Reference Circuit Design for Loudspeaker Interface

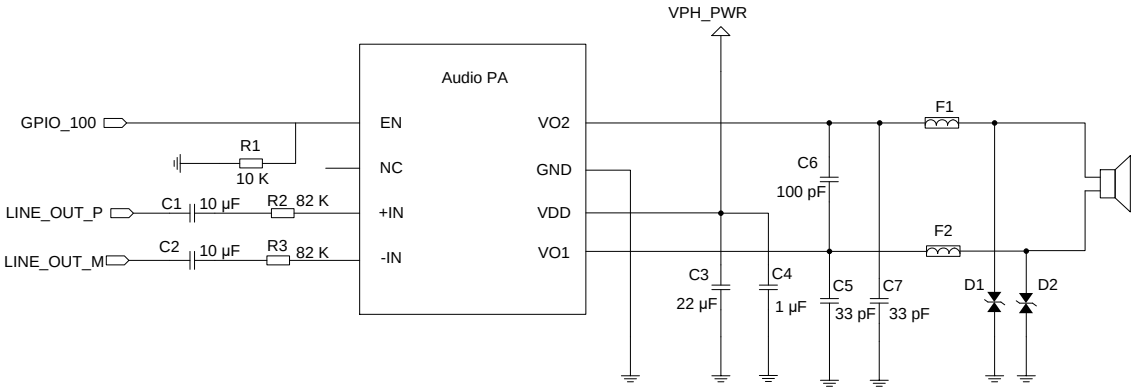


Figure 28: Reference Circuit Design for Loudspeaker Interface

4.18.5. Audio Interfaces Design Considerations

To decrease radio or other signal interference, RF antennas should be placed away from audio interfaces and audio traces. Additionally, keep power traces far away from the audio traces and do not route them in parallel.

The differential audio traces must be routed according to the differential signal layout rule.

4.19. Emergency Download Interface

USB_BOOT is an emergency download interface. Pull up to LDO9_1V8 during power-up will force the module to enter emergency download mode. There is an emergency option when start-up failures or operational abnormalities occur. For firmware upgrade and debugging in the future, please reverse the following reference circuit design.

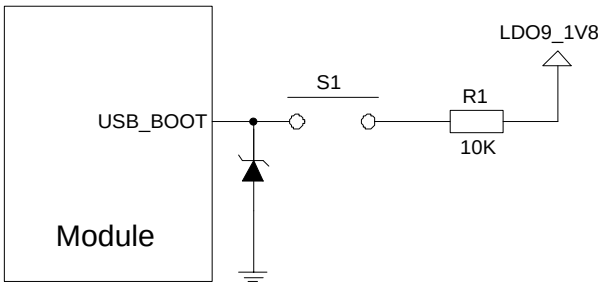


Figure 29: Reference Circuit Design for Emergency Download Interface

5 RF Specifications

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 32: Pin Definition of Cellular Network Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	19	AIO	Main antenna interface	50 Ω impedance
ANT_DRX	149	AI	Diversity antenna interface	50 Ω impedance

NOTE

Only passive antennas are supported.

Table 33: Operating Frequency of SC690A-NA

Operating Frequency	Receive (MHz)	Transmit (MHz)
LTE-FDD B2	1930–1990	1850–1910
LTE-FDD B4	2110–2155	1710–1755
LTE-FDD B5	869–894	824–849
LTE-FDD B7	2620–2690	2500–2570
LTE-FDD B12	729–746	699–716
LTE-FDD B13	746–756	777–787
LTE-FDD B14	758–768	788–798

LTE-FDD B17	734–746	704–716
LTE-FDD B25	1930–1995	1850–1915
LTE-FDD B26	859–894	814–849
LTE-FDD B66	2110–2200	1710–1780

Table 34: Operating Frequency of SC690A-EM

Operating Frequency	Receive (MHz)	Transmit (MHz)
WCDMA B1	2110–2170	1920–1980
WCDMA B3	1805–1880	1710–1785
WCDMA B8	925–960	880–915
LTE-FDD B1	2110–2170	1920–1980
LTE-FDD B3	1805–1880	1710–1785
LTE-FDD B7	2620–2690	2500–2570
LTE-FDD B8	925–960	880–915
LTE-FDD B20	791–821	832–862
LTE-FDD B28	758–803	703–748

5.1.2. Tx Power

The following table shows the RF output power of the module.

Table 35: Tx Power

Frequency	Max.	Min.
WCDMA bands	24 dBm +1/-3 dB	<-49 dBm
LTE-FDD bands	23 dBm ±2 dB	<-39 dBm

5.1.3. Reference Design

The module provides main and Rx-diversity RF antenna interfaces for antenna connection.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

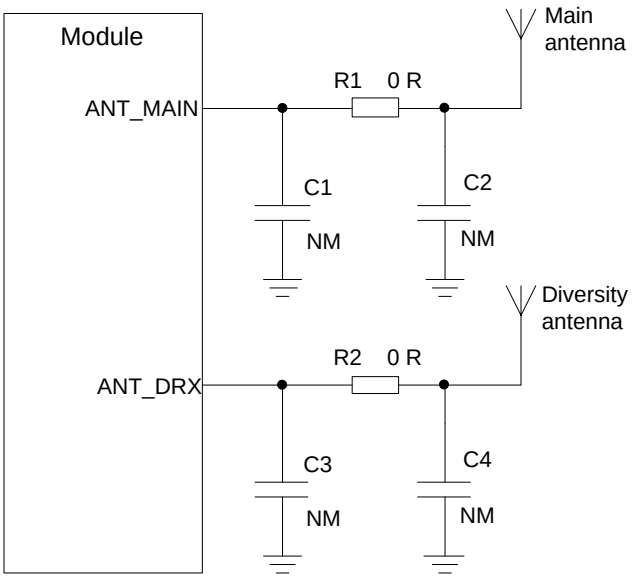


Figure 30: Reference Circuit for RF Antenna Interfaces

5.2. GNSS

The module integrates the IZat™ GNSS engine (Gen 8) which supports multiple positioning and navigation systems including GPS, GLONASS, BeiDou and so on. With an embedded LNA, the module provides greatly improved positioning accuracy.

5.2.1. Antenna Interface & Frequency Bands

The following table shows the pin definition, frequency, and performance of GNSS antenna interface.

Table 36: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	134	AI	GNSS antenna interface	50 Ω impedance

Table 37: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	
BeiDou	1561.098 ±2.046	
Galileo	1573.5–1577.5	

5.2.2. Reference Design

5.2.2.1. Recommended Circuit for Passive Antenna

GNSS antenna interface supports passive ceramic antennas and other types of passive antennas. A reference circuit design is given below.

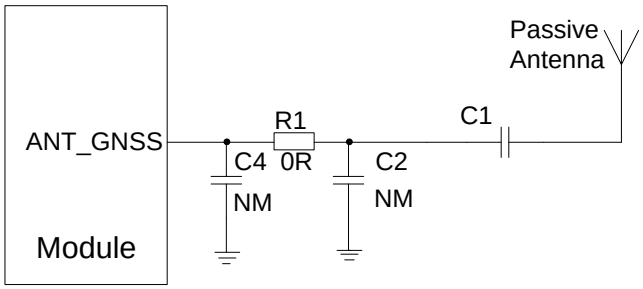


Figure 31: Reference Circuit Design for GNSS Passive Antenna

NOTE

When the passive antenna is placed far away from the module (that is, the antenna trace is long), it is recommended to add an external LNA circuit for better GNSS receiving performance, and the LNA should be placed close to the antenna.

5.2.2.2. Recommended Circuit for Active Antenna

The active antenna is powered by a 56 nH inductor through the antenna's signal path. The common power supply voltage ranges from 3.3 V to 5.0 V. Although featuring low power consumption, the active antenna still requires stable and clean power supplies. It is recommended to use high-performance LDO as the power supply. A reference design of the GNSS active antenna is shown below.

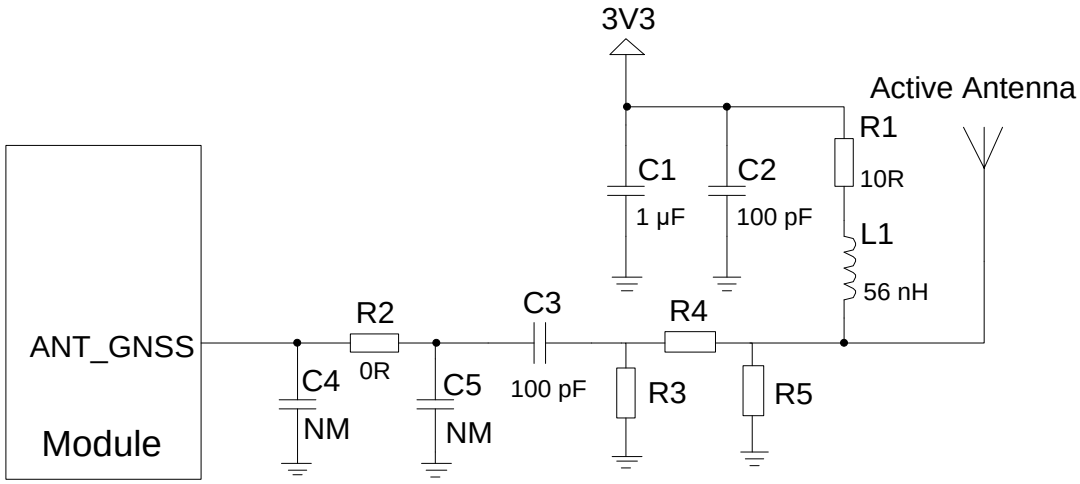


Figure 32: Reference Circuit Design for GNSS Active Antenna

NOTE

When using external active antennas or external LNA circuits, we recommend reserving type π attenuation networks (R3, R4, R5) to improve GNSS reception performance.

5.2.2.3. GNSS RF Design Guidelines

Improper design of antenna and layout may cause reduced GNSS receiving sensitivity, longer GNSS positioning time, or reduced positioning accuracy. To avoid these, please follow the reference design rules as below:

- Maximize the distance between the GNSS RF part and the GPRS RF part (including trace routing and antenna layout) to avoid mutual interference.

- In user systems, GNSS RF signal lines and RF components should be placed far away from high-speed circuits, switched-mode power supplies, power inductors, the clock circuit of single-chip microcomputers, etc.
- For applications with a harsh electromagnetic environment or with high requirement on ESD protection, it is recommended to add ESD protection diodes for the antenna interface. Only diodes with ultra-low junction capacitance such as 0.5 pF can be selected. Otherwise, it will influence the impedance characteristic of RF circuit loop or cause attenuation of bypass RF signals.
- Control the impedance of either feeder line or PCB trace to 50 Ω, and keep the trace length as short as possible.

5.3. Wi-Fi/Bluetooth

The module provides a shared antenna interface ANT_WIFI/BT for Wi-Fi and Bluetooth functions. The interface impedance is 50 Ω. You can connect external antennas such as PCB antenna, sucker antenna and ceramic antenna to the module via these interfaces to achieve Wi-Fi and Bluetooth functions.

Table 38: Pin Definition of Wi-Fi/Bluetooth Application Interfaces

Pin Name	Pin No.	GPIO No.	Default Status	Comment
ANT_WIFI/BT	129	AIO	Wi-Fi/Bluetooth antenna interface	50 Ω impedance

Table 39: Wi-Fi/Bluetooth Frequency

Type	Frequency	Unit
802.11a/b/g/n/ac	2402–2482 5180–5825	MHz
Bluetooth 5.1	2402–2480	MHz

5.3.1. Wi-Fi Overview

The module supports 2.4 GHz/5 GHz double-band WLAN wireless communication based on IEEE 802.11a/b/g/n/ac standard protocols. The maximum data rate is up to 433 Mbps. The features are as below:

- Support Wake-on-WLAN (WoWLAN)
- Support ad hoc mode
- Support WAPI SMS4 hardware encryption

- Support AP mode
- Support Wi-Fi Direct
- Support MCS 0-7 for HT20 and HT40
- Support MCS 0~8 for VHT20
- Support MCS 0~9 for VHT40和VHT80

The following table lists the Wi-Fi transmitting and receiving performance of the module.

Table 40: Wi-Fi Transmitting Performance

	Standard	Rate	Output Power
2.4 GHz	802.11b	1 Mbps	16 dBm ±2.5 dB
	802.11b	11 Mbps	16 dBm ±2.5 dB
	802.11g	6 Mbps	16 dBm ±2.5 dB
	802.11g	54 Mbps	14 dBm ±2.5 dB
	802.11n HT20	MCS0	15 dBm ±2.5 dB
	802.11n HT20	MCS7	13 dBm ±2.5 dB
	802.11n HT40	MCS0	14 dBm ±2.5 dB
	802.11n HT40	MCS7	13 dBm ±2.5 dB
5 GHz	802.11a	6 Mbps	15 dBm ±2.5 dB
	802.11a	54 Mbps	13 dBm ±2.5 dB
	802.11n HT20	MCS0	14 dBm ±2.5 dB
	802.11n HT20	MCS7	12 dBm ±2.5 dB
	802.11n HT40	MCS0	14 dBm ±2.5 dB
	802.11n HT40	MCS7	12 dBm ±2.5 dB
	802.11ac VHT20	MCS0	14 dBm ±2.5 dB
	802.11ac VHT20	MCS8	13 dBm ±2.5 dB
	802.11ac VHT40	MCS0	13 dBm ±2.5 dB
	802.11ac VHT40	MCS9	12 dBm ±2.5 dB

	802.11ac VHT80	MCS0	13 dBm ±2.5 dB
	802.11ac VHT80	MCS9	12 dBm ±2.5 dB

Table 41: Wi-Fi Receiving Performance

	Standard	Rate	Sensitivity
2.4 GHz	802.11b	1 Mbps	-96
	802.11b	11 Mbps	-88
	802.11g	6 Mbps	-90
	802.11g	54 Mbps	-74
	802.11n HT20	MCS0	-90
	802.11n HT20	MCS7	-71
	802.11n HT40	MCS0	-89
	802.11n HT40	MCS7	-70
5 GHz	802.11a	6 Mbps	-88
	802.11a	54 Mbps	-73
	802.11n HT20	MCS0	-88
	802.11n HT20	MCS7	-68
	802.11n HT40	MCS0	-86
	802.11n HT40	MCS7	-67
	802.11ac VHT20	MCS0	-89 dBm
	802.11ac VHT20	MCS8	-67 dBm
	802.11ac VHT40	MCS0	-87 dBm
	802.11ac VHT40	MCS9	-62 dBm
	802.11ac VHT80	MCS0	-83 dBm
	802.11ac VHT80	MCS9	-58 dBm

NOTE

The product conforms to the IEEE specifications.

5.3.2. Bluetooth Overview

The module supports Bluetooth 5.1 (BR/EDR+BLE) specification, as well as GFSK, 8-DPSK, Π/4-DQPSK modulation modes.

- Maximally support up to 7 wireless connections.
- Maximally support up to 3.5 PICONETs at the same time.
- Support one SCO (Synchronous Connection Oriented) or eSCO connection.

The BR/EDR channel bandwidth is 1 MHz, and can accommodate 79 channels. The BLE channel bandwidth is 2 MHz, and can accommodate 40 channels.

Table 42: Bluetooth Data Rate and Version

Version	Data rate	Maximum Application Throughput
1.2	1 Mbit/s	> 80 Kbit/s
2.0+EDR	3 Mbit/s	> 80 Kbit/s
3.0+HS	24 Mbit/s	Reference 3.0 + HS
4.0	24 Mbit/s	Reference 4.0 LE
5.0	48 Mbit/s	Reference 5.0 LE
5.1	TBD	TBD

Referenced specifications are listed below:

- Bluetooth Radio Frequency TSS and TP Specification 1.2/2.0/2.0 + EDR/2.1/2.1+ EDR/3.0/3.0 + HS, August 6, 2009
- Bluetooth Low Energy RF PHY Test Specification, RF-PHY.TS/4.0.0, December 15, 2009
- Bluetooth 5.0 RF-PHY Cover Standard: RF-PHY.TS.5.0.0, December 06, 2016

The following table lists the Bluetooth transmitting and receiving performance of the module.

Table 43: Bluetooth Transmitting and Receiving Performance

Transmitter Performance			
Packet Types	DH5	2-DH5	3-DH5
Transmitting Power	7 ±2.5 dBm	6 ±2.5 dBm	6 ±2.5 dBm
Receiver Performance			
Packet Types	DH5	2-DH5	3-DH5
Receiving Sensitivity	-91 dBm	-91 dBm	-85 dBm

5.3.3. Reference Design

A reference circuit design for Wi-Fi/Bluetooth antenna interface is shown as below. C1 and C2 are not mounted and a 0 Ω resistor is mounted on R1 by default.

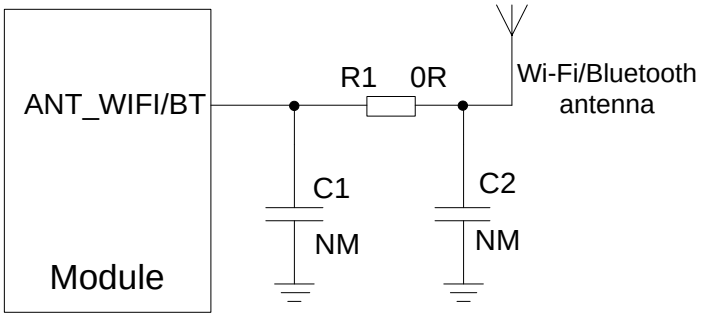


Figure 33: Reference Circuit Design for Wi-Fi/Bluetooth Antenna

5.4. Reference Design of RF Routing

For user's PCB, the characteristic impedance of all RF traces should be controlled as 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the distance between signal layer and reference ground (H), and the clearance between RF trace and ground (S). Microstrip line or coplanar waveguide line is typically used in RF layout for characteristic impedance control. The following are reference designs of microstrip line or coplanar waveguide line with different PCB structures..

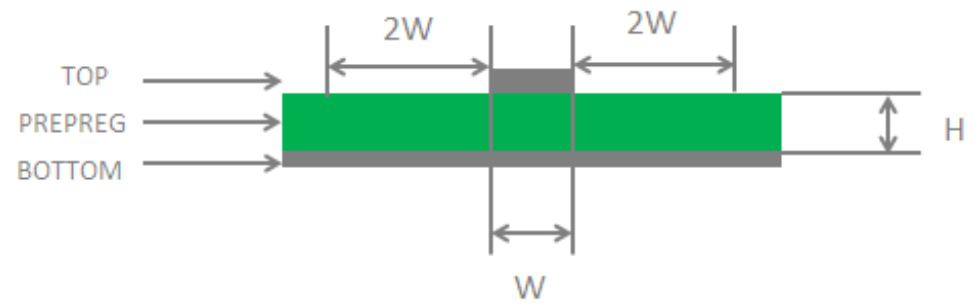


Figure 34: Microstrip Design on a 2-layer PCB

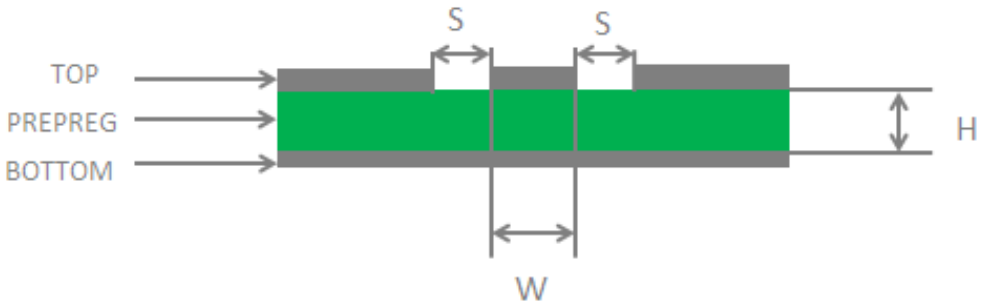


Figure 35: Coplanar Waveguide Design on a 2-layer PCB

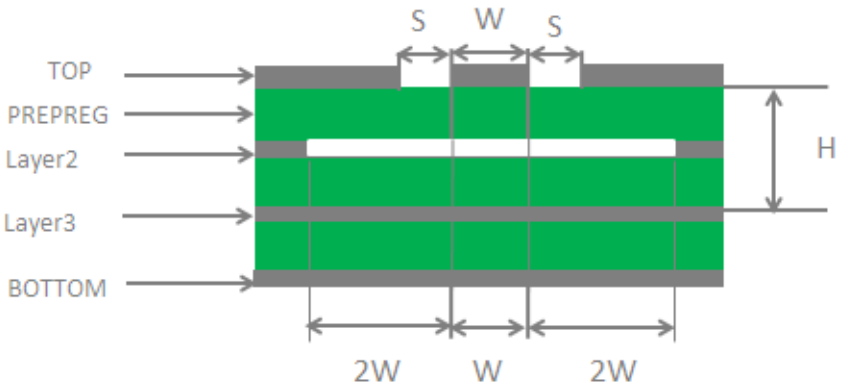


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

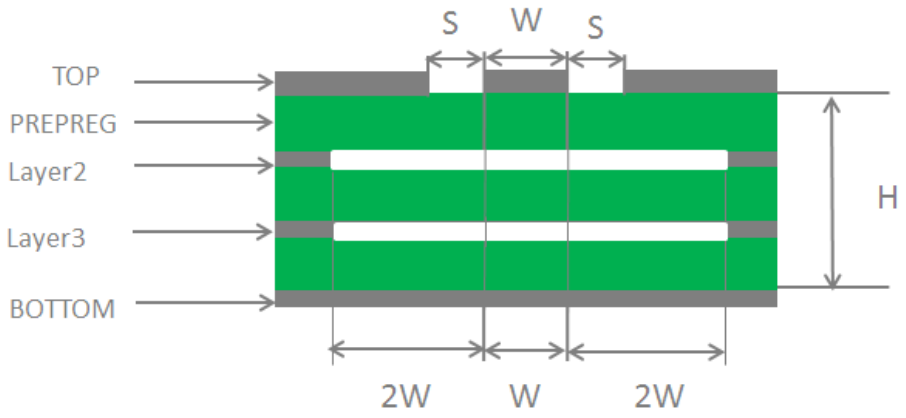


Figure 37: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- Design the GND pins adjacent to RF pins as thermal relief pads, and fully connect them to ground. Keep the distance between the RF pins and the RF connector as short as possible. Change all the right-angle traces to curved ones and the recommended trace angle is 135°.
- Reserve clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, ground vias around RF traces and the reference ground improves RF performance. The distance between the ground vias and RF traces should be more than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers

For more details about RF layout, see ***document [3]***.

5.5. Requirements for Antenna Design

Table 44: Requirements for Antenna Design

Antenna Type	Requirements
GNSS	Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi Active antenna noise figure: < 1.5 dB Active antenna gain: > -2 dBi

	Active antenna embedded LNA gain: 17 dB
GSM/EVDO/CDMA/UMTS/TD-SCDMA/LTE	VSWR: ≤ 2 Efficiency: > 30 % Gain: 1 dBi Max input power: 50 W Input impedance: 50 Ω Polarization: Vertical Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)
Wi-Fi/Bluetooth	VSWR: ≤ 2 Gain: 1 dBi Max Input Power: 50 W Input Impedance: 50 Ω Polarization Type: Vertical Cable Insertion Loss: < 1 dB

NOTE

It is recommended to use a passive GNSS antenna when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.6. RF Connector Recommendation

If you use RF connector for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by *HIROSE*.

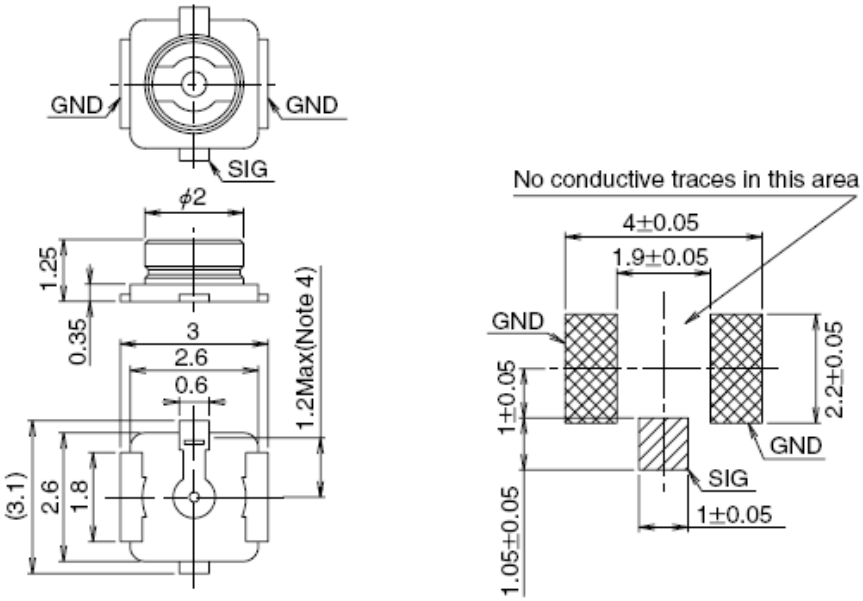


Figure 38: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP serial connectors listed in the following figure can be used to match the U.FL-R-SMT.

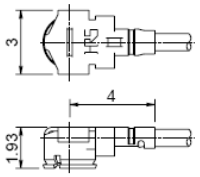
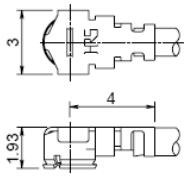
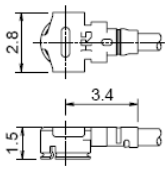
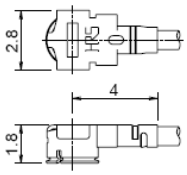
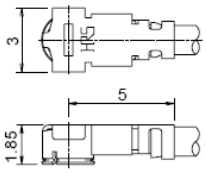
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 39: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

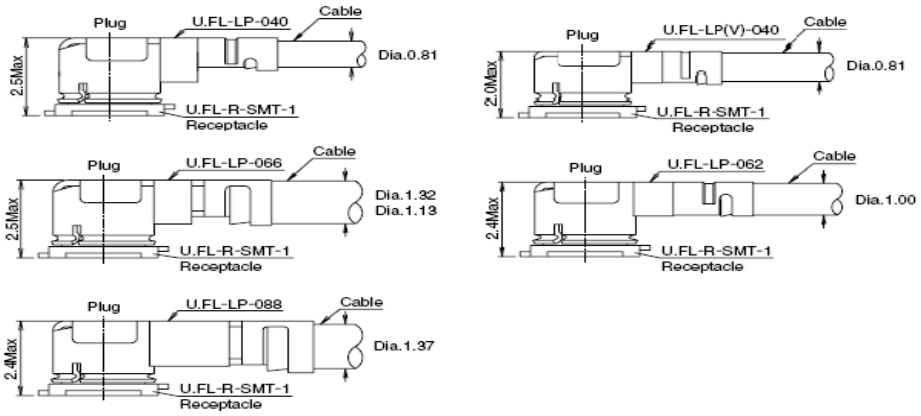


Figure 40: Space Factor of Mated Connector (Unit: mm)

For more details, visit http://www.hirose.com.

6 Electrical Characteristics & Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 45: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	4.75	V
USB_VBUS	-0.3	16	V
Peak Current of VBAT	-	3	A
Voltage on Digital Pins	-0.3	2.09	V

6.2. Power Supply Ratings

Table 46: The Module's Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB	The actual input voltages must stay between the minimum and maximum values.	3.55	3.8	4.4	V
USB_VBUS	USB connection detection		3.6	-	10	V

6.3. Power Consumption

Table 47: SC690A-NA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	90	μA
LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
LTE data transfer	LTE-FDD B2 @ max power	TBD	mA
	LTE-FDD B4 @ max power	TBD	mA
	LTE-FDD B5 @ max power	TBD	mA
	LTE-FDD B7 @ max power	TBD	mA
	LTE-FDD B12 @ max power	TBD	mA
	LTE-FDD B13 @ max power	TBD	mA
	LTE-FDD B14 @ max power	TBD	mA

	LTE-FDD B17 @ max power	TBD	mA
	LTE-FDD B25 @ max power	TBD	mA
	LTE-FDD B26 @ max power	TBD	mA
	LTE-FDD B66 @ max power	TBD	mA

Table 48: SC690A-EM Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	79	μA
WCDMA data transfer (GNSS OFF)	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
	Sleep (USB disconnected) @ DRX = 9	TBD	mA
LTE-FDD supply current	Sleep (USB disconnected) @ DRX = 5	TBD	mA
	Sleep (USB disconnected) @ DRX = 6	TBD	mA
	Sleep (USB disconnected) @ DRX = 7	TBD	mA
	Sleep (USB disconnected) @ DRX = 8	TBD	mA
LTE data transfer	LTE-FDD B1 @ max power	TBD	mA
	LTE-FDD B3 @ max power	TBD	mA
	LTE-FDD B7 @ max power	TBD	mA
	LTE-FDD B8 @ max power	TBD	mA
	LTE-FDD B20 @ max power	TBD	mA
WCDMA data transfer	B1 (HSDPA) @ max power	TBD	mA
	B3 (HSDPA) @ max power	TBD	mA
	B8 (HSDPA) @ max power	TBD	mA

	B1 (HSUPA) @ max power	TBD	mA
	B3 (HSUPA) @ max power	TBD	mA
	B8 (HSUPA) @ max power	TBD	mA

6.4. Digital I/O Characteristic

Table 49: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.17	2.1	V
V_{IL}	Input low voltage	-0.3	0.63	V
V_{OH}	Output high voltage	1.35	1.8	V
V_{OL}	Output low voltage	0	0.45	V

Table 50: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V
V_{IH}	Input high voltage	1.26	2.1	V
V_{IL}	Input low voltage	-0.3	0.36	V
V_{OH}	Output high voltage	1.44	1.8	V
V_{OL}	Output low voltage	0	0.4	V

Table 51: (U)SIM 2.95 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.1	V
V_{IH}	Input high voltage	2.065	3.25	V

V_{IL}	Input low voltage	-0.3	0.59	V
V_{OH}	Output high voltage	2.36	2.95	V
V_{OL}	Output low voltage	0	0.4	V

6.5. ESD

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective component to the ESD sensitive interfaces and points in the product design of the module.

Table 52: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±5	±10	kV
Other Interfaces	±0.25	-	kV

6.6. Operating and Storage Temperatures

Table 53: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [2]	-35	+25	+75	°C
Storage temperature range	-40	-	+90	°C

[2] Within operating temperature range, the module is 3GPP compliant.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

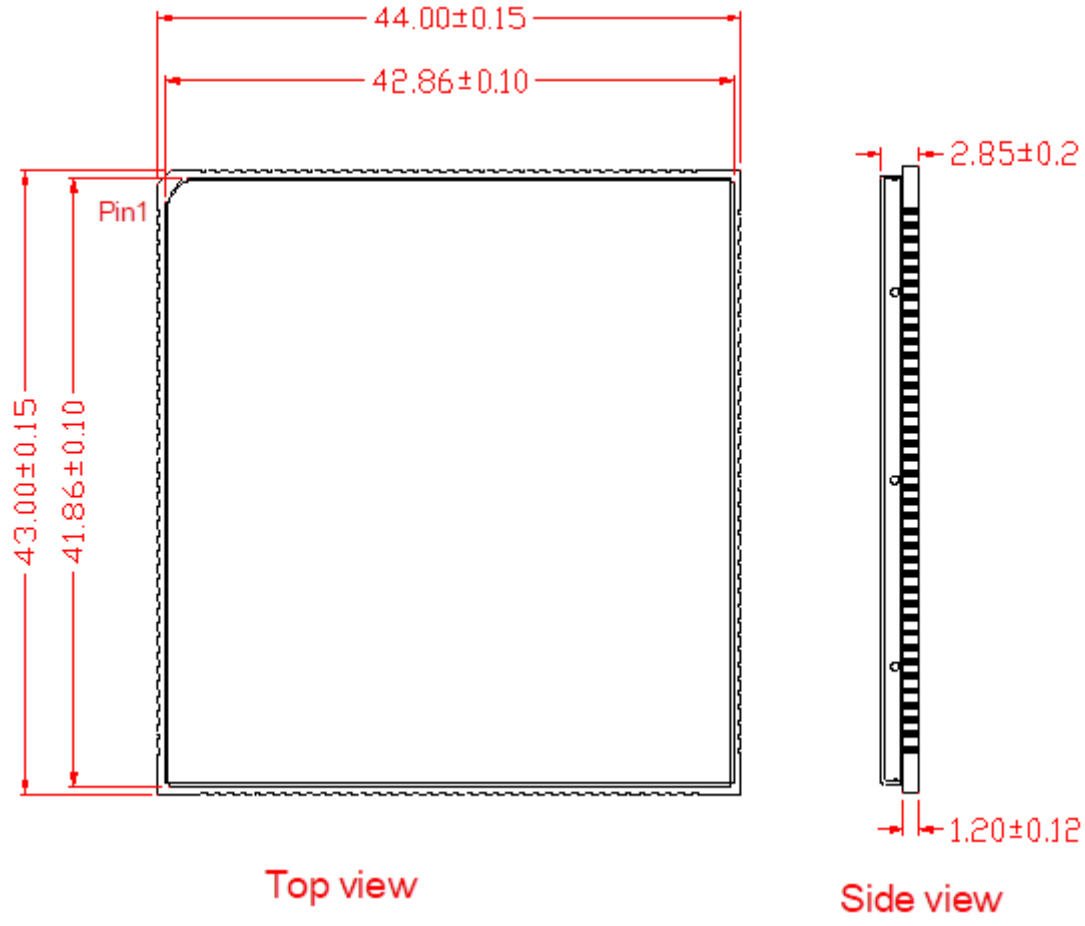


Figure 41: Module Top and Side Dimensions (Unit: mm)

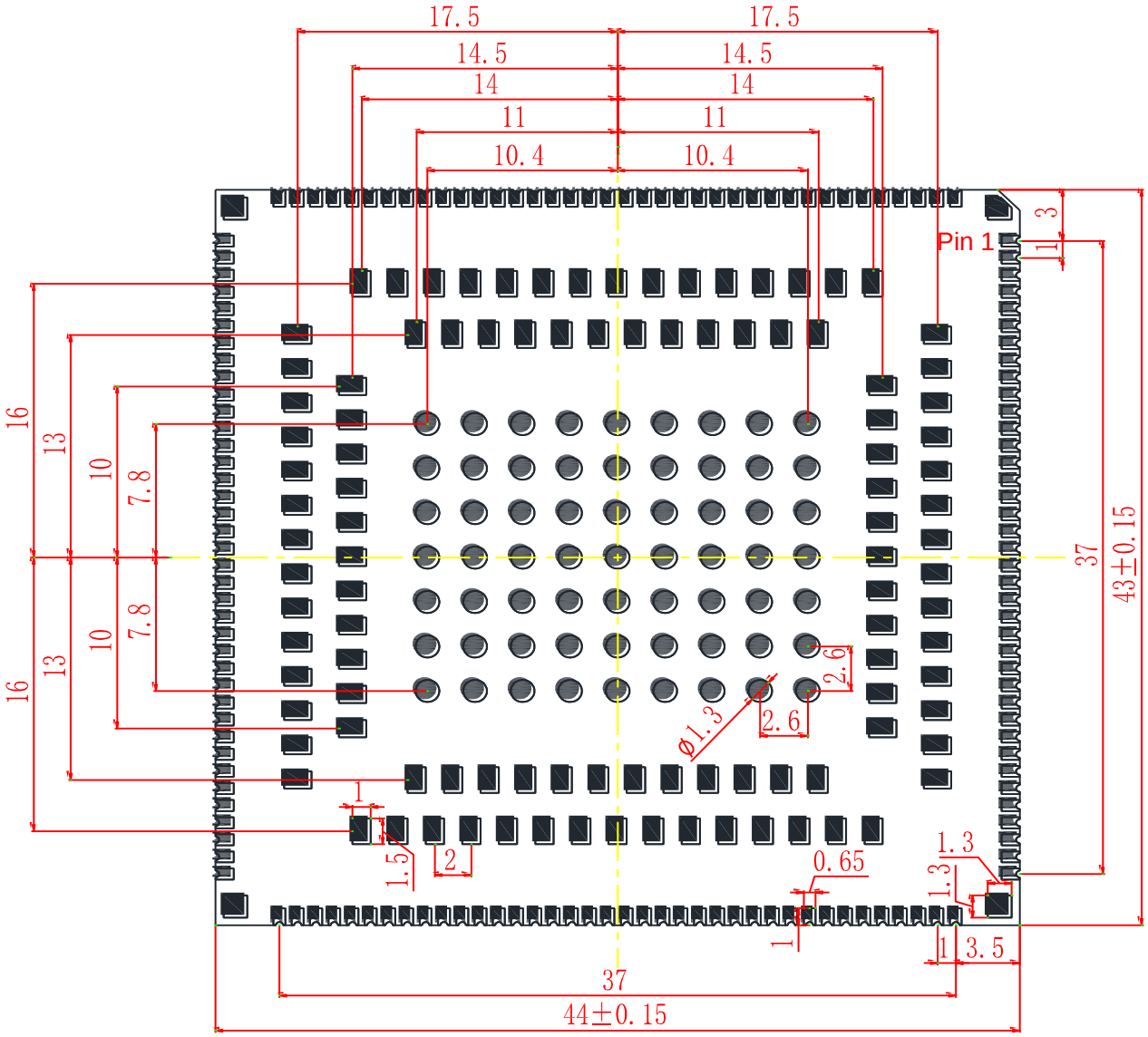


Figure 42: Module Bottom Dimensions (TOP View, Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

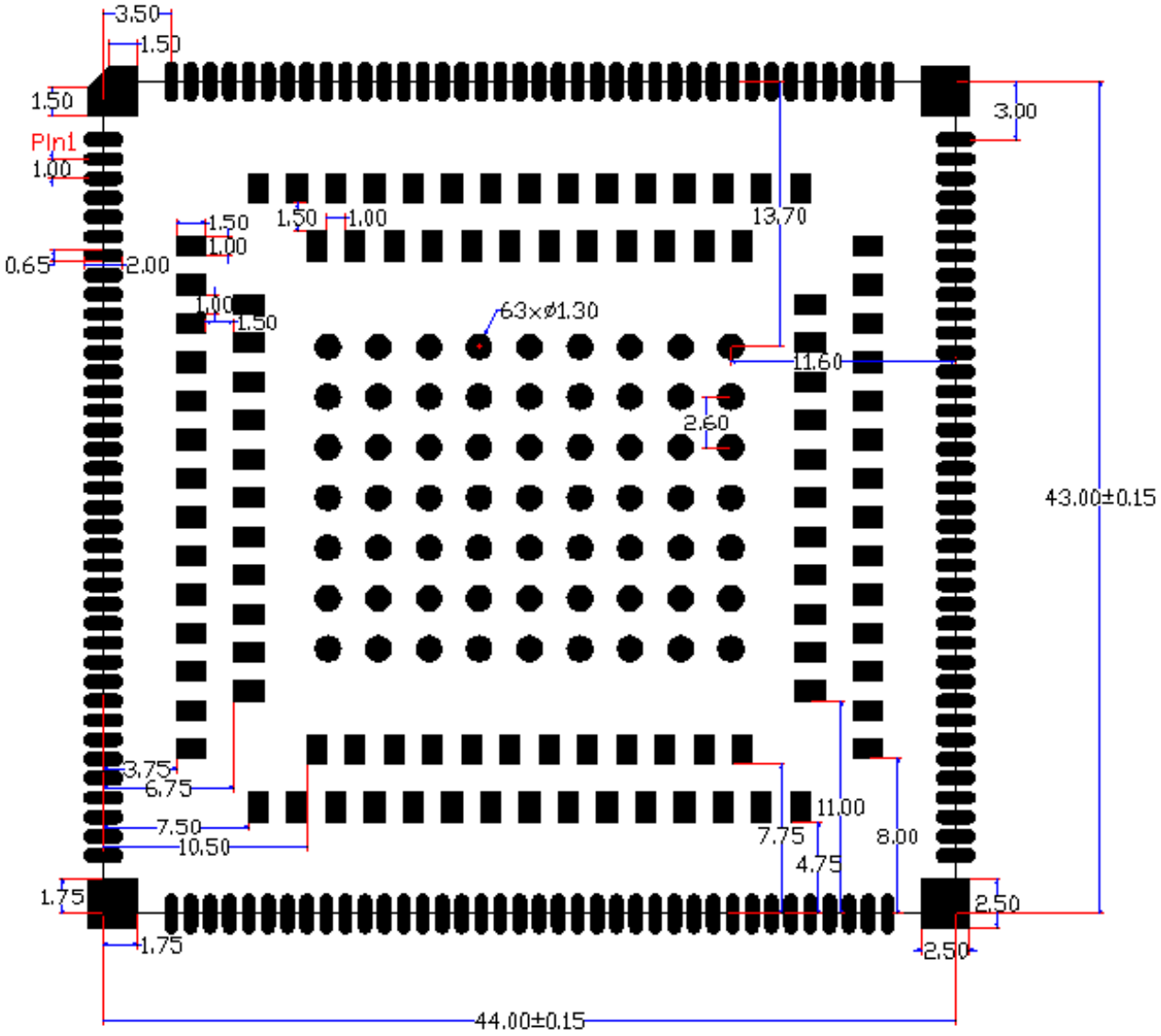


Figure 43: Recommended Footprint (TOP View)

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm.

7.3. Top and Bottom Views

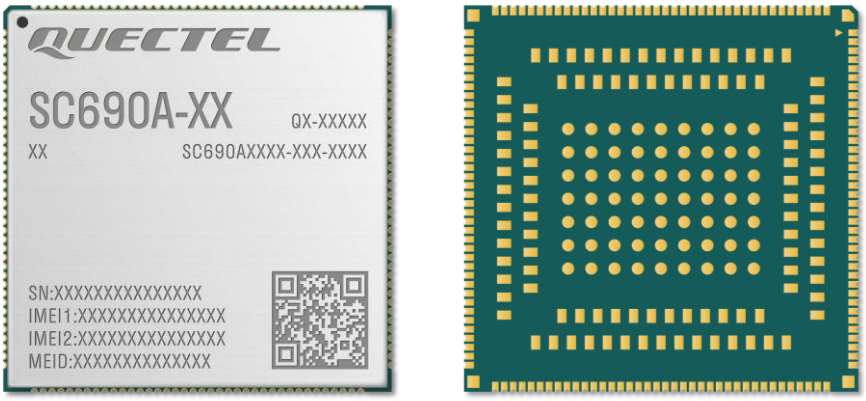


Figure 44: Top & Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. The storage life (in vacuum-sealed packaging) is 12 months in recommended storage condition.

3. The floor life of the module is 168 hours [4] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in recommended storage condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

[4] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.18–0.20mm. For more details, see ***document [4]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

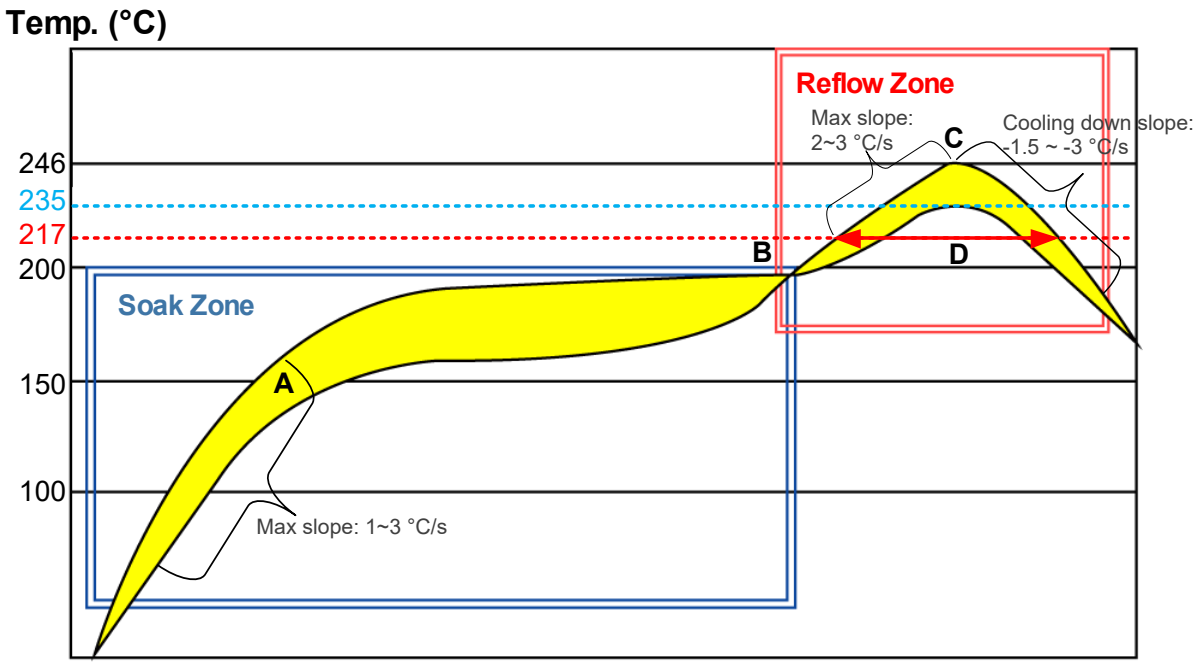


Figure 45: Recommended Reflow Soldering Thermal Profile

Table 54: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	2–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

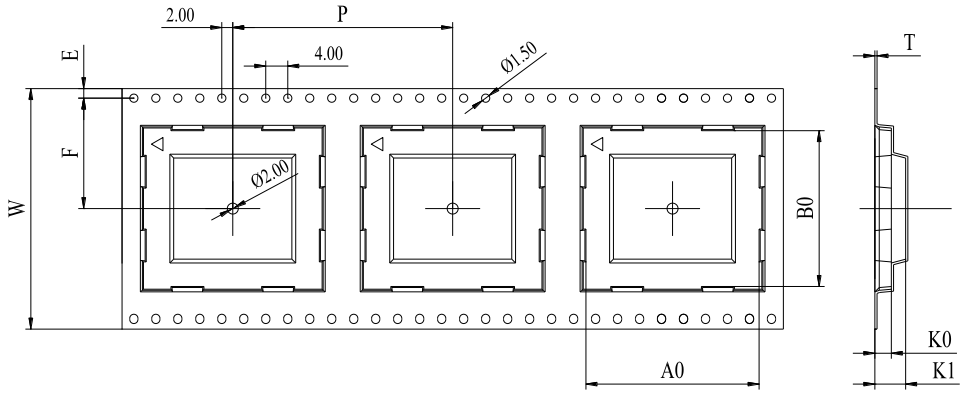


Figure 46: Carrier Tape Dimension Drawing

Table 55: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.35	44.5	43.5	4.1	5.4	34.2	1.75

8.3.2. Plastic Reel

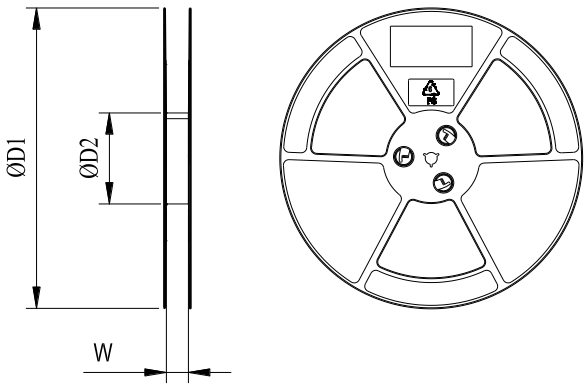
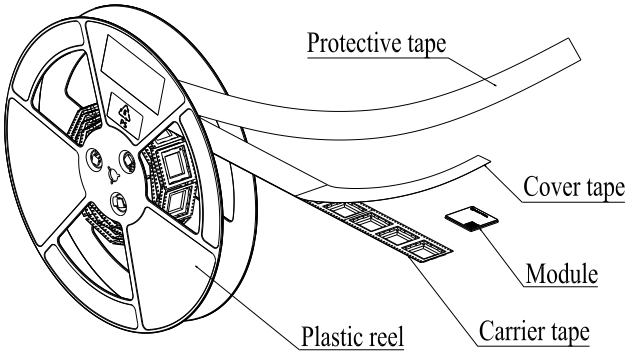


Figure 47: Plastic Reel Dimension Drawing

Table 56: Plastic Reel Dimension Table (Unit: mm)

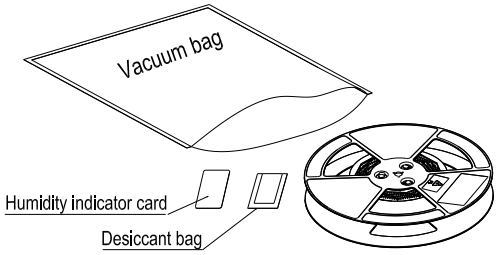
øD1	øD2	W
380	180	72.5

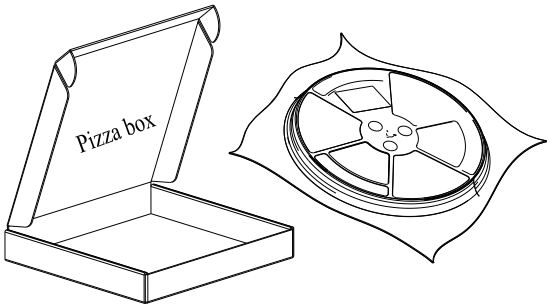
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 800 modules.

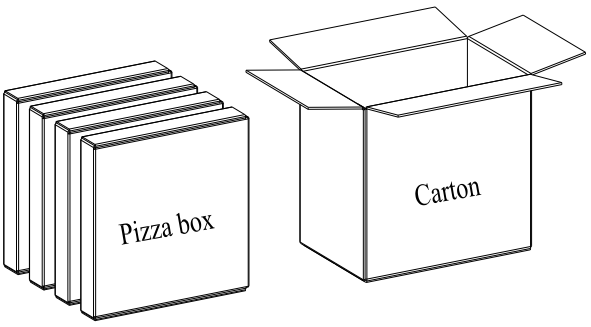


Figure 48: Packaging Process

9 Appendix References

Table 57: Related Documents

Document Name
[1] Quectel_Smart_EVB-G2_User_Guide
[2] Quectel_SC690A_Series_GPIO_Configuration
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Secondary_SMT_ User_Guide
[5] Quectel_SC690A_Series_Reference_Design

Table 58: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AMR-WB	Adaptive Multi-Rate Wideband
AON	Active Optical Network
AP	Application Processor
bps	Bits Per Second
BPSK	Binary Phase Shift Keying
BW	Bandwidth
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CS	Coding Scheme
CSD	Circuit Switched Data

CS2	Commercial Sample II
CTS	Clear To Send
DAI	Digital Audio Interface
DCE	Data Communications Equipment
DC-HSDPA	Dual-carrier High Speed Downlink Packet Access
DDR	Double Data Rate
DFOTA	Delta Firmware Upgrade Over The Air
DL	Downlink
DRX	Discontinuous Reception
DRX	Diversity Receive
DTE	Data Terminal Equipment
DTR	Data Terminal Ready
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
FDD	Frequency Division Duplex
FEM	Front-End Module
FR	Full Rate
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
GRFC	General RF Control
HB	High Band
HPUE	High Power User Equipment
HR	Half Rate

HSDPA	High Speed Downlink Packet Access
HSPA	High Speed Packet Access
HSUPA	High Speed Uplink Packet Access
IC	Integrated Circuit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
I/O	Input/Output
Inorm	Normal Current
LAA	License Assisted Access
LB	Low Band
LED	Light Emitting Diode
LGA	Land Grid Array
LMHB	Low/Middle/High Band
LNA	Low Noise Amplifier
LTE	Long Term Evolution
MAC	Media Access Control
MB	Middle Band
MCU	Microcontroller Unit
MDC	Management Data Clock
MDIO	Management Data Input/Output
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MS	Mobile Station
MT	Mobile Terminated

NR	New Radio
NSA	Non-Stand Alone
PA	Power Amplifier
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCM	Pulse Code Modulation
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical Layer
PMIC	Power Management Integrated Circuit
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
QZSS	Quasi-Zenith Satellite System
RI	Ring Indicator
RF	Radio Frequency
RGMII	Reduced Gigabit Media Independent Interface
RHCP	Right Hand Circularly Polarized
Rx	Receive
SA	Stand Alone
SCS	Sub-Carrier Space
SD	Secure Digital
SIMO	Single Input Multiple Output

SMD	Surface Mount Device
SMS	Short Message Service
SoC	System on a Chip
STB	Set Top Box
TDMA	Time Division Multiple Access
TD-SCDMA	Time Division-Synchronous Code Division Multiple Access
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UHB	Ultra High Band
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{I}max	Absolute Maximum Input Voltage
V_{I}min	Absolute Minimum Input Voltage

V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WWAN	Wireless Wide Area Network