EG065K Series

Hardware Design

LTE-A Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for your failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2021-03-19	David WANG/ Alex WANG	Creation of the document
1.0	2022-03-04	David WANG/ Elliot CAO/ Robinson SHEN/ Haibo LV/ Jacen HUANG	First official release

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Table Index

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1 Introduction

This document defines the EG065K series module and describes its air interfaces and hardware interfaces which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

This document is applicable to the following modules:

- EG065K-NA

FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2022EG065KNA
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain (dBi)	IC Max Antenna Gain (dBi)
LTE BAND 2	7.50	7.50
LTE BAND 4	4.50	4.50
LTE BAND 5	8.91	8.91
LTE BAND 7	7.50	7.50
LTE BAND 12	8.20	8.20
LTE BAND 13	8.66	8.66

LTE BAND 14	8.73	8.73
LTE BAND 25	7.50	7.50
LTE BAND 26(814-824)	8.86	NA
LTE BAND 26(824-849)	8.91	8.91
LTE BAND 30	-0.32	-0.32
LTE BAND 66	4.50	4.50

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products.

Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR2022EG065KNA" or "Contains FCC ID: XMR2022EG065KNA" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without

a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device." or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement."

Déclaration sur l'exposition aux rayonnements RF

L'autre utilisé pour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows:

"Contains IC: 10224A-22EG065KNA" or "where: 10224A-22EG065KNA is the module's certification number".

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte.

L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, précédé du mot «Contient» ou d'un libellé semblable exprimant la même signification, comme suit:

"Contient IC: 10224A-22EG065KNA " ou "où: 10224A-22EG065KNA est le numéro de certification du module".

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

The module is a SMD type module which is engineered to meet the demanding requirements in M2M applications, such as body camera, portable device, etc. Related information and details are listed in the table below.

Table 2: Brief Introduction of the Module

Categories	
Packaging	LGA
Pins in total	230
Dimensions	(28.0 ±0.2) mm × (31.0 ±0.2) mm × (2.4 ±0.2) mm
Weight	Approx. 5.3 g
Wireless technologies	LTE-A
Variants	EG065K-NA, EG065K-EA

2.1. Frequency Bands and Functions

Table 3: Wireless Network Type

Wireless Network Type	EG065K-NA	EG065K-EA
LTE-FDD	B2/B4/B5/B7/B12/B13/B14/ B25/B26/B30/B66	B1/B2/B3/B4/B5/B7/B8/ B20/B28
LTE-TDD	-	B40

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● Supply voltage: 3.3–4.5 V ● Typical supply voltage: 3.8 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interfaces	Supports dual USIM/SIM card: 1.8 V, 3.0 V
USB Interface	● Compliant with USB 2.0 specifications, with transmission rates up to 480 Mbps on USB 2.0 ● Used for AT command communication, data transmission, software debugging and firmware upgrade ● USB serial driver: Windows 7/8/8.1/10, Linux 2.6–5.15, Android 4.x–12.x
UART Interface	**Debug UART:** ● Used for Linux console and log output ● Baud rate: 115200 bps
Network Indication	NET_MODE and NET_STATUS to indicate network connectivity status
AT Commands	Compliant with *3GPP TS 27.007*, *3GPP TS 27.005* and Quectel enhanced AT commands
Rx-diversity	LTE
Antenna Interfaces	● Main antenna interfaces: ANT_MAIN1 and ANT_MAIN2 ● Diversity antenna interfaces: ANT_DIV1 and ANT_DIV2 ● 50 Ω impedance
Transmitting Power	● LTE-FDD B30: Class 3 (22.3 dBm ±2 dB) ● LTE-FDD other bands: Class 3 (23.5 dBm ±2 dB) ● LTE-TDD: Class 3 (23.5 dBm ±2 dB)
LTE Features	● Supports *3GPP Rel-12* Cat 6 FDD and TDD ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth ● Supports DL 2 × 2 MIMO ● Supports uplink QPSK, 16QAM and 64QAM modulation ● Supports downlink QPSK, 16QAM and 64QAM modulation ● FDD: Max. 300 Mbps (DL)/ 75 Mbps (UL)

	• TDD: Max. 250 Mbps (DL)/ 45 Mbps (UL) [1]
Internet Protocol Features	• Supports QMI/MBIM/NITZ/HTTP/HTTPS/FTP/LwM2M*/PING* • Supports PAP and CHAP for PPP connections
Temperature Range	• Operating temperature range [2]: -30 °C to 75 °C • Extended temperature range [3]: -40 °C to 85 °C • Storage temperature range: -40 °C to 90 °C
Firmware Upgrade	• USB interface • DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive.

2.3. Functional Diagram

[1] LTE-TDD is only supported by EG065K-EA.
[2] To meet this operating temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this operation temperature range, the module can meet 3GPP specifications.
[3] To meet this extended temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are impervious, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR2 SDRAM + NAND flash
- Radio frequency
- Peripheral interfaces

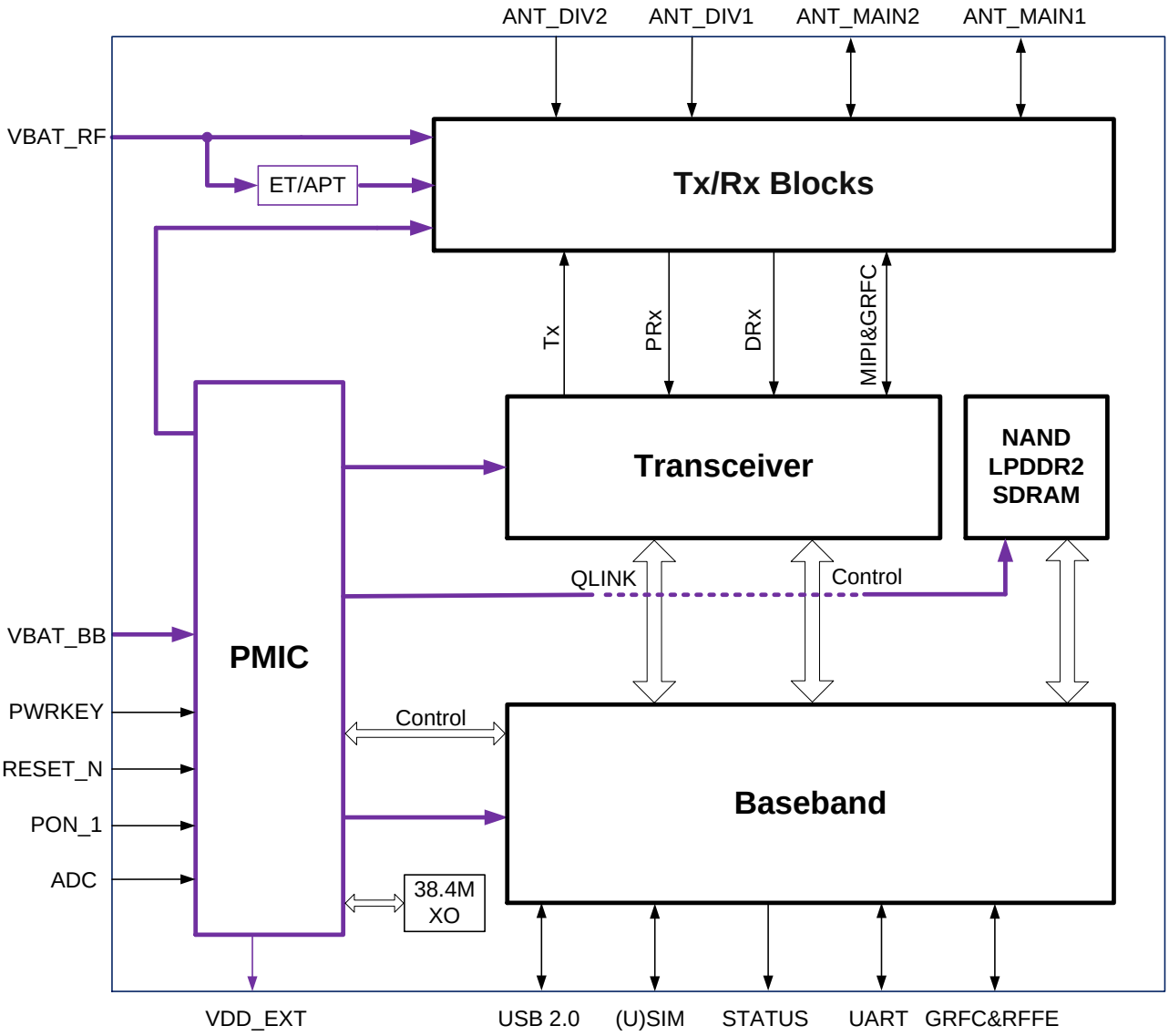


Figure 1: Functional Diagram

2.4. Pin Assignment

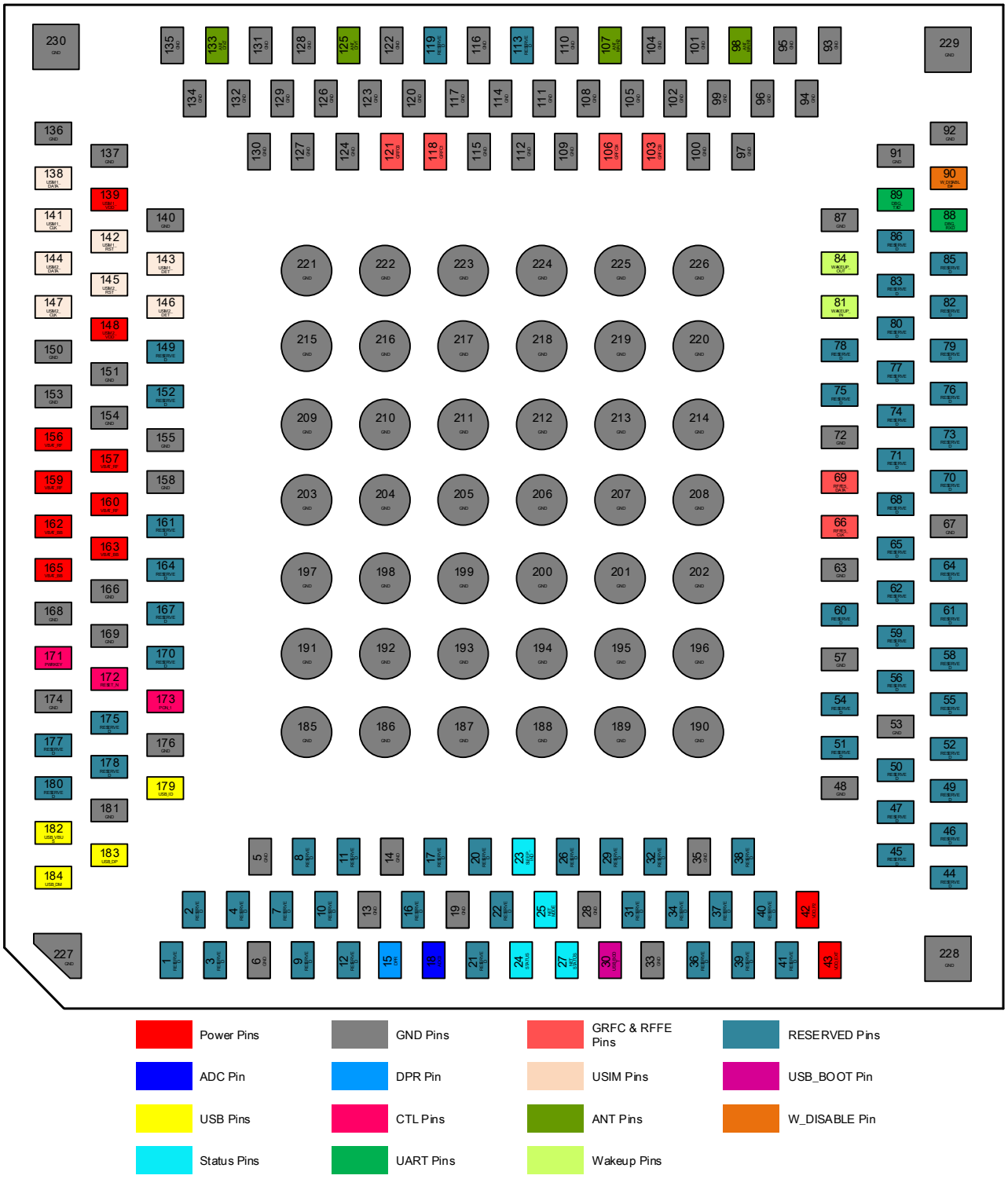


Figure 2: Pin Assignment (Top View)

NOTE

Keep all RESERVED and unused pins unconnected.

2.5. Pin Description

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output

Table 6: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	162, 163, 165	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	156, 157, 159, 160	PI	Power supply for the module's RF part	Vmax = 4.5 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1.2 A in a transmitting burst.
VDD_EXT	43	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	-
VDD_P2	42	PI	SD card IO power supply	**For high-voltage**: Vmax = 3.05 V	Reserved for SDIO interface.

				Vmin = 2.7 V Vnom = 2.85 V **For low-voltage**: Vmax = 1.95 V Vmin = 1.65V Vnom = 1.8 V	If unused, connect VDD_P2 to VDD_EXT.
GND	5, 6, 13, 14, 19, 28, 33, 35, 48, 53, 57, 63, 67, 72, 87, 91–97, 99–102, 104, 105, 108–112, 114–117, 120, 122–124, 126–132, 134–137, 140, 150, 151, 153–155, 158, 166, 168, 169, 174, 176, 181, 185–230				Ground
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	171	DI	Turn on/off the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Internally pulled up to 1.8 V. Active low.
RESET_N	172	DI	Reset the module		
PON_1	173	DI	Turn on the module automatically when it is pulled high	V_{IH}max = VBAT + 0.5 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Pull it up to 1.8–4.5 V. If unused, pull it down to GND.
Indication Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	25	DO	Indicate the module's network registration mode	1.8 V	If unused, keep these pins open.
NET_STATUS	27	DO	Indicate the module's network activity status		
STATUS	24	DO	Indicate the module's operation status		
SLEEP_IND	23	DO	Indicate the module's sleep mode		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	182	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.3 V Vnom = 5.0 V	For USB Connection detection only, not power supply.
USB_ID*	36	DI	USB ID detect	1.8 V	-

USB_DP	183	AIO	USB differential data (+)	-	Requires differential impedance of 90 Ω. USB 2.0 compliant.
USB_DM	184	AIO	USB differential data (-)	-	
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	139	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.75 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	138	DIO	(U)SIM1 card data	1.8/3.0 V	-
USIM1_CLK	141	DO	(U)SIM1 card clock	1.8/3.0 V	-
USIM1_RST	142	DO	(U)SIM1 card reset	1.8/3.0 V	-
USIM1_DET	143	DI	(U)SIM1 card hot–plug detect	1.8 V	If unused, keep it open.
USIM2_VDD	148	PO	(U)SIM2 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.75 V	Either 1.8 V or 3.0 V is supported by the module automatically. If (U)SIM2 interface is unused, keep it open.
USIM2_DATA	144	DIO	(U)SIM2 card data	1.8/3.0 V	If (U)SIM2 interface is unused, keep these pins open.
USIM2_CLK	147	DO	(U)SIM2 card clock	1.8/3.0 V	
USIM2_RST	145	DO	(U)SIM2 card reset	1.8/3.0 V	
USIM2_DET	146	DI	(U)SIM2 card hot-plug detect	1.8 V	If (U)SIM2 interface is unused, keep it open.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	88	DI	Debug UART receive	1.8 V	If unused, keep these pins open.
DBG_TXD	89	DO	Debug UART transmit	1.8 V	

Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN1	98	AIO	Main antenna interface LTE LMB_TRX ● For EG065K-NA, LMB includes B2/B4/B5/B12/B13/B14/B25/B26/B66 ● For EG065K-EA, LMB includes B1/B2/B3/B4/B5/B8/B20/B28	-	50 Ω impedance
ANT_MAIN2	107	AIO	Main antenna interface LTE HB_TRX ● For EG065K-NA, HB includes B7/B30 ● For EG065K-EA, HB includes B7/B40	-	
ANT_DIV1	125	AI	Diversity antenna interface LTE MHB_DRX ● For EG065K-NA, MHB includes B2/B4/B7/B25/B30/B66 ● For EG065K-EA, MHB includes B1/B2/B3/B4/B7/B40	-	
ANT_DIV2	133	AI	Diversity antenna interface LTE LB_DRX ● For EG065K-NA, LB includes B5/B12/B13/B14/B26 ● For EG065K-EA, LB includes B5/B8/B20/B28	-	
RFFE Antenna Tuner Control Interface					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RFFE5_CLK	66	DO	Used for external MIPI IC control	1.8 V	If unused, keep these pins open.
RFFE5_DATA	69	DIO	Used for external MIPI IC control		
GRFC Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC33	103	DO	Generic RF controller	1.8 V	If unused, keep these pins open.
GRFC34	106	DO	Generic RF controller		
GRFC1	118	DO	Generic RF controller		
GRFC6	121	DO	Generic RF controller		
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	18	AI	General-purpose ADC interface	Voltage range: 0–1.875 V	If unused, keep it open.
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	30	DI	Force the module into emergency download mode	1.8 V	Active high. If unused, keep it open.
DPR	15	DI	Dynamic power reduction	1.8 V	Active low.
W_DISABLE#	90	DI	Airplane mode control	1.8 V	Pulled up by default. At low voltage level, the module will enter airplane mode. If unused, keep it open.
WAKEUP_IN	81	DI	Wake up the module	1.8 V	Pulled up by default. Low level wakes up the module. If unused, keep it open.
WAKE_ON_WWAN	84	DO	Wake up the host	1.8 V	Pulled down by default.

		High level wakes up the host. If unused, keep it open.
RESERVED Pins		
Pin Name	**Pin No.**	**Comment**
RESERVED	1–4, 7–12, 16, 17, 20–22, 26, 29, 31, 32, 34, 36–41, 44–47, 49–52, 54–56, 58–62, 64, 65, 68, 70, 71, 73–80, 82, 83, 85, 86, 113, 119, 149, 152, 161, 164, 167, 170, 175, 177, 178, 180	Keep these pins open.

2.6. EVB

To help you develop applications with the module, Quectel supplies an evaluation board (EVB), USB data cable, earphone, antenna, and other peripherals to control or to test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 7: Overview of Operating Modes

Mode	Details	
Normal Operation	Idle	Software is active. The module has registered on the network and ready to send and receive data.
	Data	Network connected. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command sets the module to a minimum functionality mode. In this case, both RF function and (U)SIM card will be invalid.	
Airplane Mode	**AT+CFUN=4** command or driving W_DISABLE# pin low can set the module to airplane mode. In this case, RF function will be invalid.	
Sleep Mode	In this mode, power consumption of the module will be reduced to the minimal level. In this mode, the module can still receive paging message, SMS and TCP/UDP data from network.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is inactive, all interfaces are inaccessible, and the operating voltage (connected to VBAT_BB and VBAT_RF) remains applied.	

See details of **AT+CFUN=0** and **AT+CFUN=4** in ***document [2].***

3.2. Sleep Mode

DRX can reduce the module's power consumption to a minimum value during sleep mode. The diagram below illustrates the relationship between the DRX run time and the power consumption of the module in this mode.

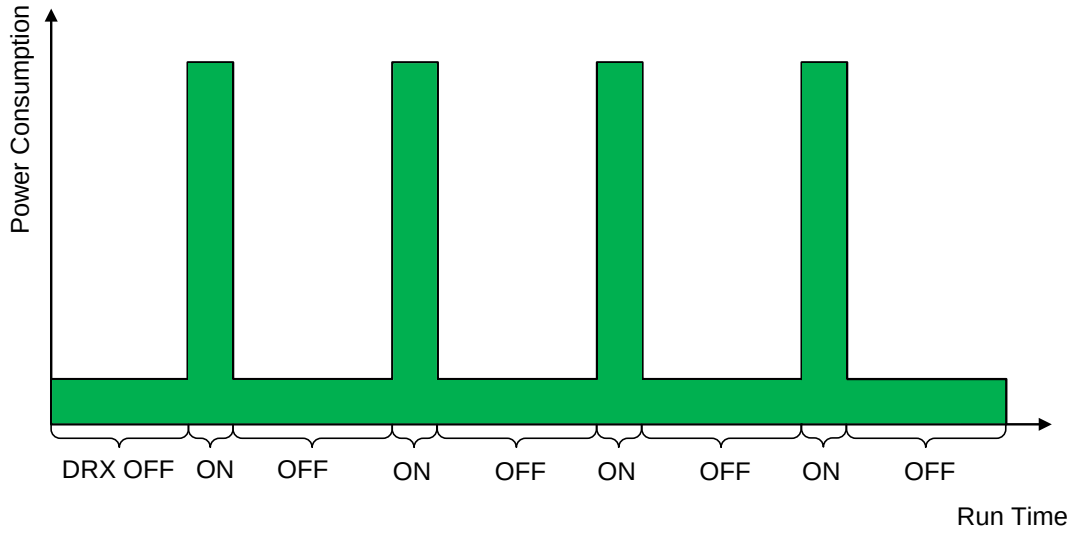


Figure 3: DRX Run Time and Power Consumption in Sleep Mode

3.2.1. USB Application Scenarios

3.2.1.1. USB Application with USB Remote Wakeup Function

In this scenario, two preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1** command.
- The host's USB, which connects to the module's USB interface, enters suspend state.

See details of **AT+QSCLK=1** command in ***document [2]***.

The host supports USB suspend/resume and remote wakeup function. The figure below illustrates the connection between the module and the host.

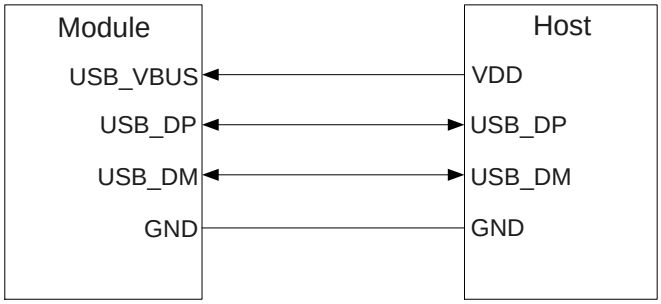


Figure 4: Sleep Mode Application with USB Remote Wakeup

The module and the host will be woken up in the following conditions:

- Sending data to the module through USB will wake up the module.
- When the module has a URC to report, the module will send remote wake-up signals to host's USB to wake up the host.

3.2.1.2. USB Application Without USB Suspend Function

In this scenario, two preconditions must be met to set the module into sleep mode:

- Execute **AT+QSCLK=1** command.
- Disconnect the USB_VBUS power supply.

See details of **AT+QSCLK=1** command in ***document [2]***.

If the host does not support USB suspend function, USB_VBUS should be disconnected through an external control circuit to set the module enter sleep mode. Turning on the power switch and supplying power to USB_VBUS will wake up the module. The figure illustrates the connection between the module and the host.

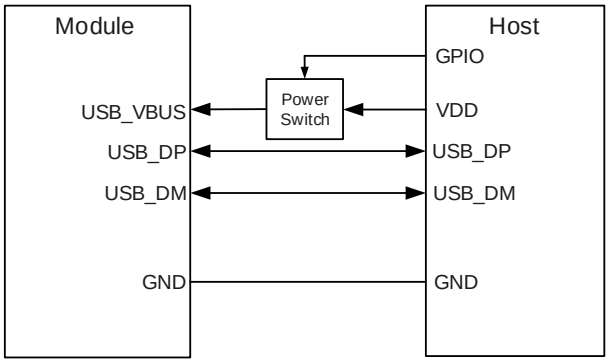


Figure 5: Sleep Mode Application without Suspend Function

3.3. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands related to it will be inaccessible. This mode can be set via hardware or software methods, see ***Chapter 4.7*** for details.

3.4. Power Supply

3.4.1. Power Supply Pins

The module provides 7 VBAT pins dedicated for the connection with the external power supply. There are 2 separate voltage domains for VBAT.

Table 8: Pin Definition of Power Supply

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
VBAT_BB	162, 163, 165	PI	Power supply for the module's baseband part	Vmax = 4.5 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 0.8 A.
VBAT_RF	156, 157, 159, 160	PI	Power supply for the module's RF part	Vmax = 4.5 V Vmin = 3.3 V Vnom = 3.8 V	It must be provided with sufficient current up to 1.2 A in a transmitting burst.
VDD_EXT	43	PO	Provide 1.8 V for external circuit	Vnom = 1.8 V $I_O$max = 50 mA	-
VDD_P2	42	PI	SD card IO power Supply	**For high-voltage**: Vmax = 3.05 V Vnom = 2.85 V Vmin = 2.7 V **For low-voltage**: Vmax = 1.95 V Vnom = 1.8 V Vmin = 1.65 V	Reserved for SDIO interface. If unused, connect VDD_P2 to VDD_EXT.
GND	5, 6, 13, 14, 19, 28, 33, 35, 48, 53, 57, 63, 67, 72, 87, 91–97, 99–102, 104, 105, 108–112, 114–117, 120, 122–124, 126–132, 134–137, 140, 150, 151, 153–155, 158, 166, 168, 169, 174, 176, 181, 185–230				

3.4.2. Reference Design for Power Supply

The performance of the module largely depends on the power source. The power supply of the module should provide sufficient current of 2.0 A at least. If the voltage drops between input and output are not too high, it is suggested that an LDO should be used to supply power to the module. If there is a big voltage difference between input and the desired output VBAT, a buck converter is preferred as the power supply.

The following figure shows a reference design for +5 V input power source. In this design, output of the power supply is about 3.8 V and the maximum load current is 3 A.

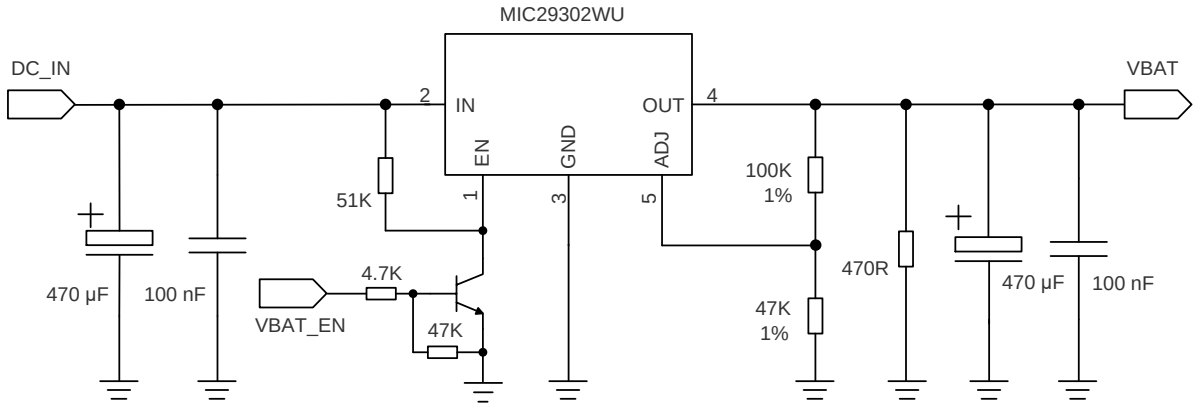


Figure 6: Reference Design of Power Supply

NOTE

To avoid damaging internal flash, do not switch off power supply when the module works normally. Only after the module is shut down with PWRKEY or AT command can the power supply be cut off.

3.4.3. Power Supply Monitoring

The **AT+CBC** command can be used to monitor the voltage of VBAT_BB. For more details, see ***document [2]***.

3.4.4. Voltage Stability Requirements

The power supply of the module ranges from 3.3 V to 4.5 V. Please ensure the input voltage never drops below 3.3 V.

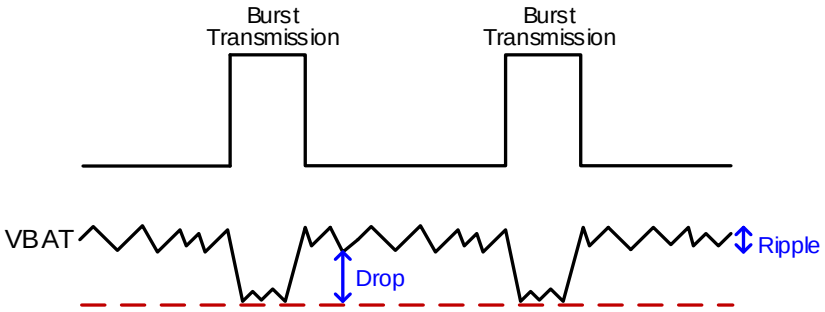


Figure 7: Power Supply Limits during Burst Transmission

To decrease voltage drop, one bypass capacitor of about 100 μF with low ESR and one multi-layer ceramic chip (MLCC) capacitor array for its ultra-low ESR should be used for VBAT_BB/RF. It is recommended to use 4 ceramic capacitors (100 nF, 6.8 nF, 220 pF, 68 pF) for composing the MLCC array for VABT_BB and 6 ceramic capacitors (100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for composing the MLCC array for VABT_RF, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source which can supply power along two sub paths with star structure. The width of VBAT_BB trace should be no less than 1 mm, and the width of VBAT_RF trace should be no less than 1.5 mm. In principle, the longer the VBAT trace is, the wider it will be.

In addition, to ensure the stability of the power supply, it is necessary to add a high-power TVS component at the front end of the power supply. The star structure of the power supply is shown as below.

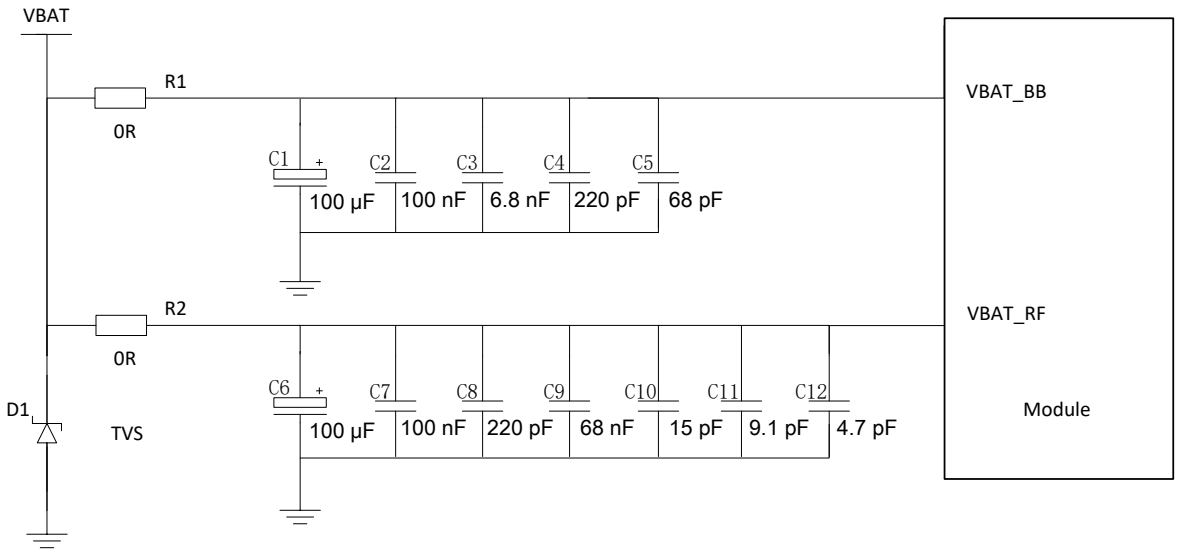


Figure 8: Star Structure of the Power Supply

3.5. Turn On

3.5.1. Turn On with PWRKEY

Table 9: Pin Definition of PWRKEY

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PWRKEY	171	DI	Turn on/off the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Internally pulled up to 1.8 V. Active low.

When the module is in power-off mode, it can be turned on and enter normal operation mode by driving PWRKEY low for at least 500 ms. It is recommended to use an open drain/collector driver to control PWRKEY. After STATUS outputs a high level, PWRKEY can be released.

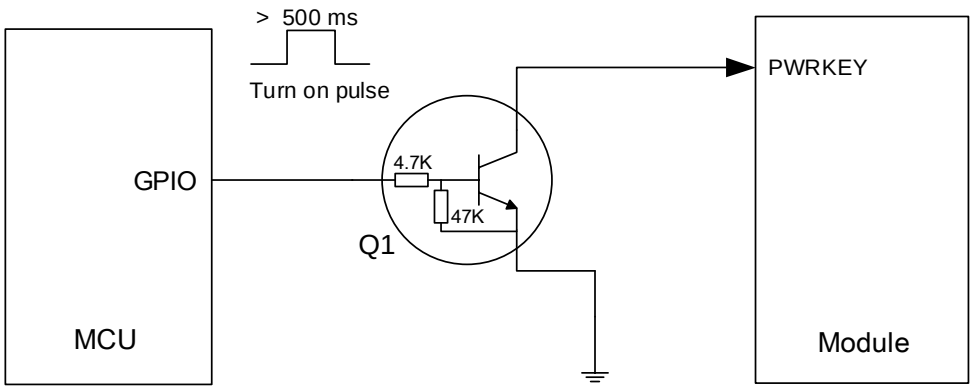


Figure 9: Reference Circuit of Turning On the Module with Driving Circuit

Another way to control PWRKEY is by using a button directly. When pressing the button, an electrostatic strike may generate from your finger. Therefore, a TVS component shall be placed near the button for ESD protection.

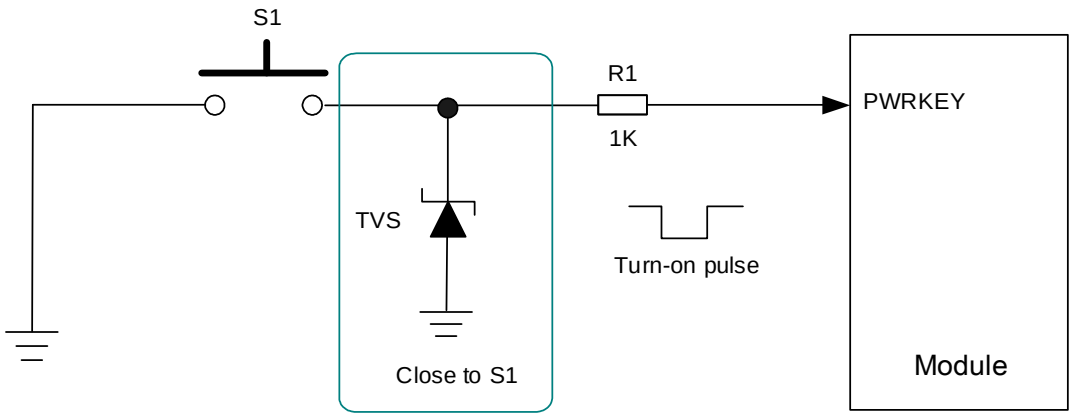


Figure 10: Reference Circuit of Turning On the Module with Button

The power-up scenario is illustrated in the following figure.

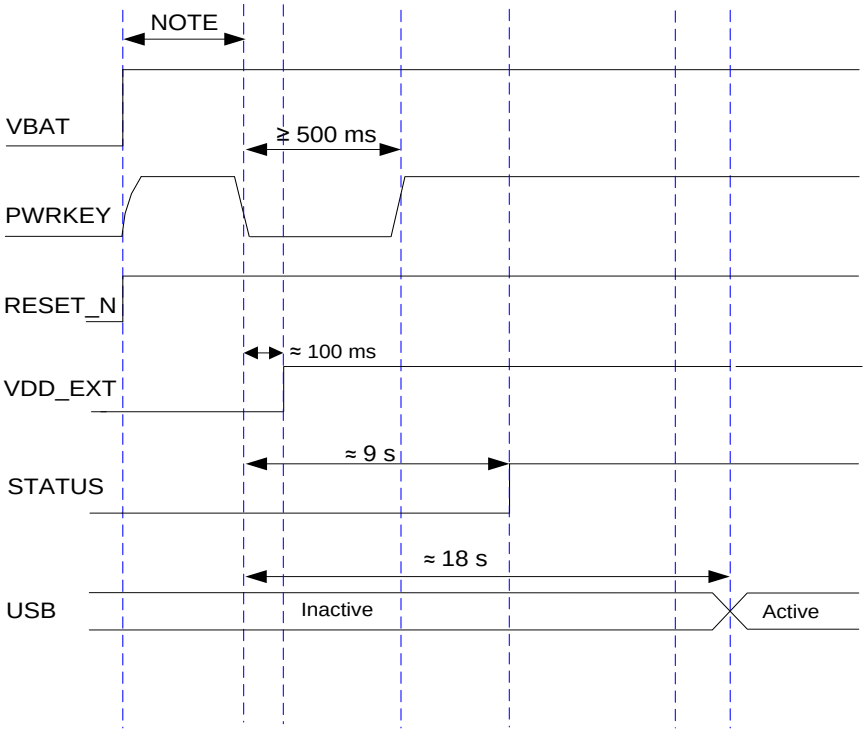


Figure 11: Power-Up Timing

NOTE

1. Please ensure that VBAT is stable for at least 60 ms before pulling down PWRKEY.
2. If the module needs to be powered on automatically and power-off is not needed, PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor.

3. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

3.5.2. Turn On with PON_1

Table 10: Pin Description of PON_1

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
PON_1	173	DI	Turn on the module automatically when it is pulled high	V_{IH}max = VBAT + 0.5 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Pull it up to 1.8–4.5 V. If unused, pull it down to GND.

3.6. Turn Off

Normally, there are two approaches to turn off the module:

- Driving PWRKEY low for at least 800 ms.
- Executing **AT+QPOWD** command.

3.6.1. Turn Off with PWRKEY

Drive PWRKEY low for at least 800 ms, then the module will execute a power-down procedure after PWRKEY is released.

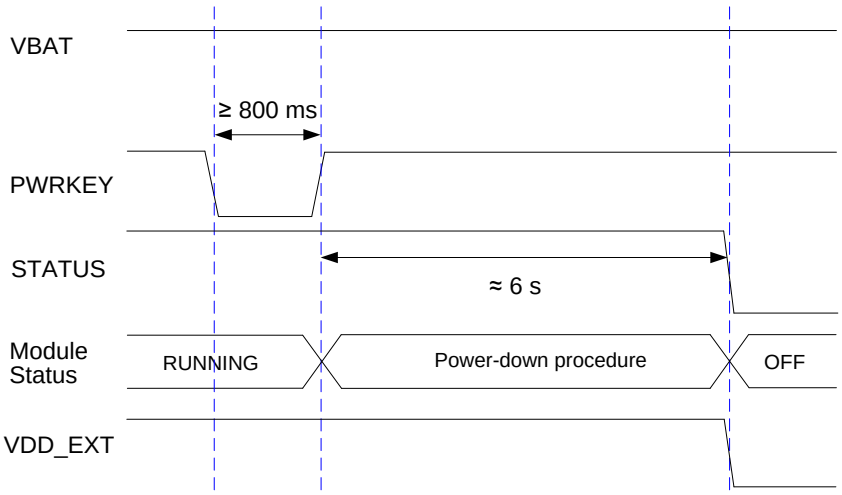


Figure 12: Power-Down Timing

3.6.2. Turn Off with AT Command

It is also safe to turn off the module with command **AT+QPOWD**, which is similar to turn off the module via PWRKEY. See ***document [2]*** for details about **AT+QPOWD** command.

NOTE

1. To avoid damaging internal flash, do not switch off the power supply when the module works normally. Only after the module is power off by PWRKEY or AT command can the power supply cut off.
2. When turning off module with **AT+QPOWD**, keep PWRKEY at a high level after the execution of power-off command. Otherwise, the module will be turned on again after successful turn-off.

3.7. RESET_N

The module can be reset by driving RESET_N low for at least 250–600 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: Pin Definition of RESET_N

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESET_N	172	DI	Reset the module	V_{IH}max = 2.1 V V_{IH}min = 1.3 V V_{IL}max = 0.5 V	Internally pulled up to 1.8 V. Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver can be used to control RESET_N.

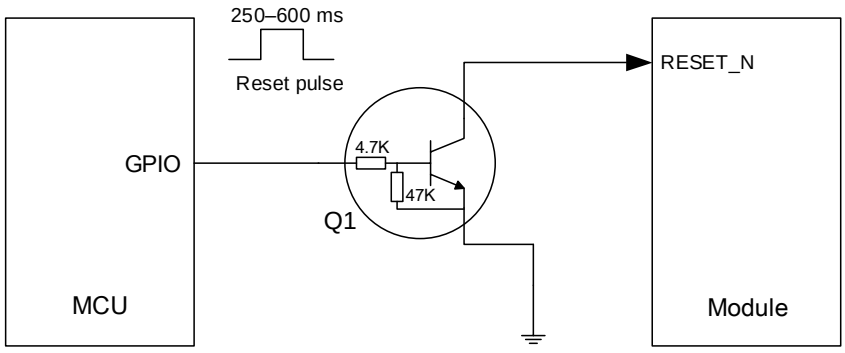


Figure 13: Reference Circuit of RESET_N with Driving Circuit

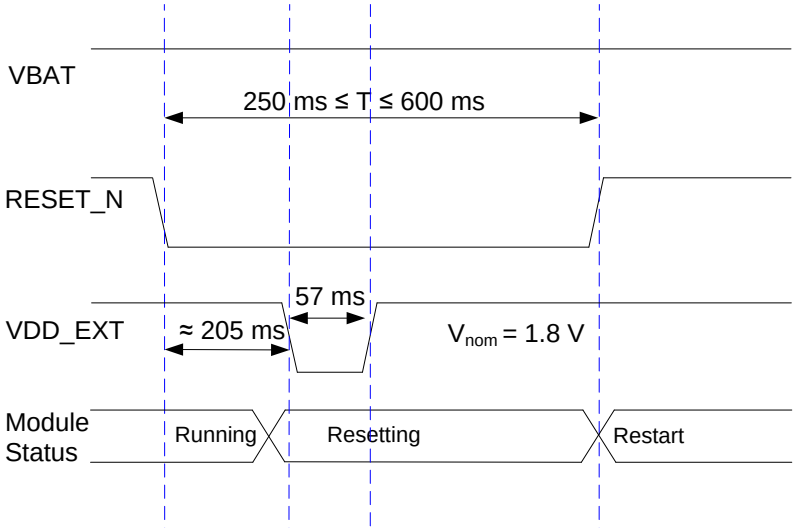


Figure 14: Reset Timing

NOTE

1. Reset the module with RESET_N only when it fails to be turned off with **AT+QPOWD** or PWRKEY. See ***document [2]*** for details about **AT+QPOWD**.
2. Ensure that there is no large capacitance on PWRKEY and RESET_N pins.

4 Application Interfaces

The module is equipped with 230 LGA pins that can connect to cellular application platform. The following interfaces are described in details in subsequent chapters:

- USB interface
- USB_BOOT interface
- (U)SIM interfaces
- UART interface
- ADC interface
- Indication interfaces
- W_DISABLE#
- DPR

4.1. USB Interface

The module provides one integrated Universal Series Bus (USB) interface. The USB interface complies with the USB 2.0 specifications, and supports high speed (480 Mbps) and full speed (12 Mbps) for USB 2.0.

Table 12: Functions of USB Interface

Functions	USB High-Speed Interface	USB Full-Speed Interface
AT command communication	√	√
Data transmission	√	√
Software debugging	√	√
Firmware upgrade	√	√

Table 13: Pin Definition of USB Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_VBUS	182	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.3 V Vnom = 5.0 V	For USB connection detection only, not power supply.
USB_ID*	36	DI	USB ID detect	1.8 V	-
USB_DP	183	AIO	USB differential data (+)	-	Requires differential impedance of 90 Ω. USB 2.0 compliant.
USB_DM	184	AIO	USB differential data (-)	-	

It is recommended to reserve test points for software debugging and firmware upgrade in your designs. Below is a reference design of USB 2.0 interface.

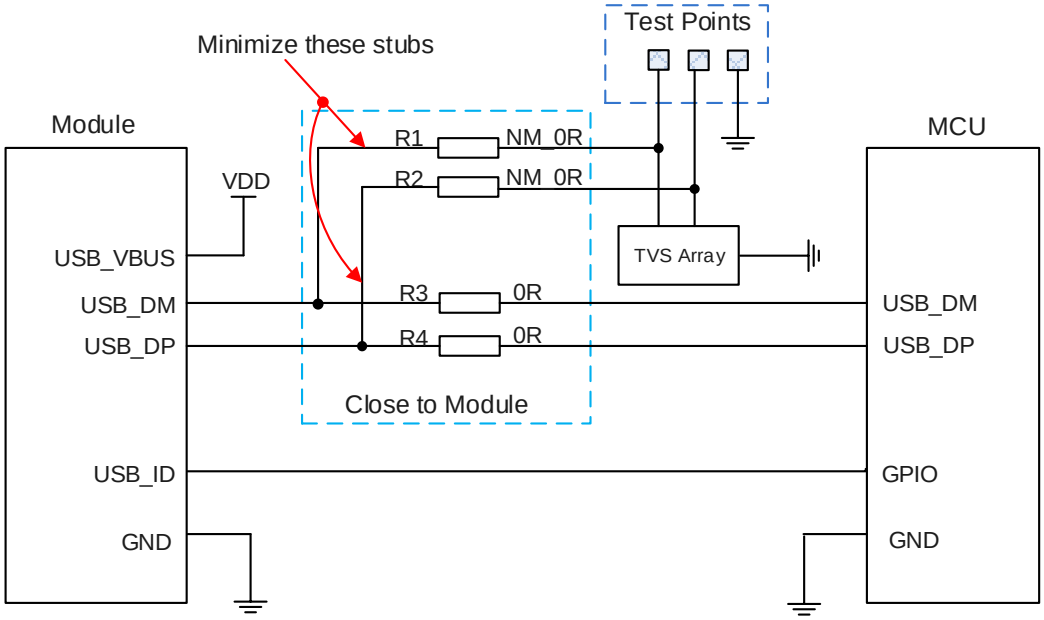


Figure 15: Reference Circuit of USB Interface

To ensure the signal integrity of USB data lines, R1, R2, R3 and R4 should be placed close to the module and close to each other as well. The extra stubs of trace must be as short as possible.

To meet the USB specifications, the following principles should be complied with when designing the USB interface.

- It is vital to route the USB signal traces as a differential pair with ground surrounded. The impedance of USB 2.0 differential traces is 90 Ω.
- For USB 2.0 signal traces, length matching within the differential data pair should be less than 2 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, and RF signal traces. It is important to route the USB differential traces in inner-layers of the PCB, and surround the traces with ground on the same layer and with ground planes on adjacent layers above and below.
- Pay attention to the selection of the ESD protection device since the device's junction capacitance may cause influences on USB data traces. Typically, the stray capacitance should be less than 2.0 pF for USB 2.0.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces respectively.

For more details about the USB specifications, please visit http://www.usb.org/home.

4.2. USB_BOOT Interface

Table 14: Pin Definition of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USB_BOOT	30	DI	Force the module into emergency download mode	1.8 V	Active high. If unused, keep it open.

The module provides a USB_BOOT pin. You can pull up USB_BOOT to VDD_EXT before powering on the module, then the module will enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB 2.0 interface.

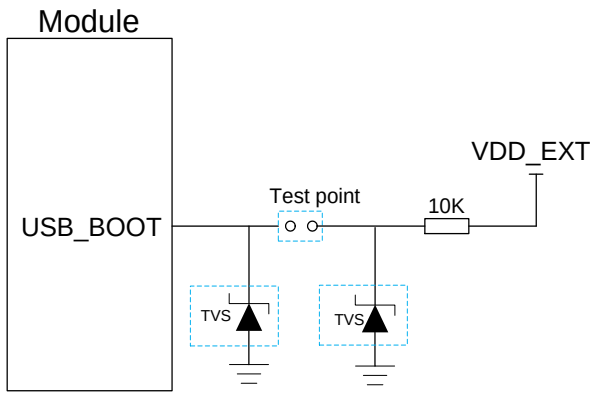


Figure 16: Reference Circuit of USB_BOOT Interface

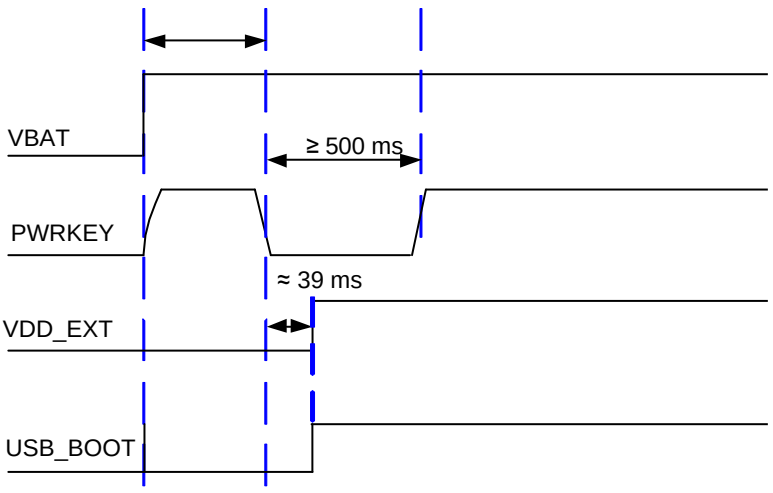


Figure 17: Timing Sequence for Entering Emergency Download Mode

NOTE

1. Ensure that VBAT is stable before pulling down PWRKEY. It is recommended that the time between powering up VBAT and pulling down PWRKEY is not less than 60 ms.
2. When using MCU to control the module to enter emergency download mode, please follow the above timing sequence. It is not recommended to pull up USB_BOOT to 1.8 V before powering up VBAT. Directly connecting the test points as shown in ***Figure 16*** can manually force the module to enter emergency download mode.

4.3. (U)SIM Interfaces

The (U)SIM interface circuitry meets *ETSI* and *IMT-2000* requirements. Both Class B (3.0 V) and Class C (1.8 V) (U)SIM cards are supported, and dual-SIM single-standby function is supported.

Table 15: Pin Definition of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
USIM1_VDD	139	PO	(U)SIM1 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.75 V	Either 1.8 V or 3.0 V is supported by the module automatically.
USIM1_DATA	138	DIO	(U)SIM1 card data	1.8/3.0 V	-
USIM1_CLK	141	DO	(U)SIM1 card clock	1.8/3.0 V	-
USIM1_RST	142	DO	(U)SIM1 card reset	1.8/3.0 V	-
USIM1_DET	143	DI	(U)SIM1 card hot-plug detect	1.8 V	If unused, keep it open.
USIM2_VDD	148	PO	(U)SIM2 card power supply	$I_O$max = 50 mA **For 1.8 V (U)SIM:** Vmax = 1.9 V Vmin = 1.7 V **For 3.0 V (U)SIM:** Vmax = 3.05 V Vmin = 2.75 V	Either 1.8 V or 3.0 V is supported by the module automatically. If (U)SIM2 interface is unused, keep it open.
USIM2_DATA	144	DIO	(U)SIM2 card data	1.8/3.0 V	If (U)SIM2 interface is

USIM2_CLK	147	DO	(U)SIM2 card clock	1.8/3.0 V	unused, keep these pins open.
USIM2_RST	145	DO	(U)SIM2 card reset	1.8/3.0 V	
USIM2_DET	146	DI	(U)SIM2 card hot-plug detect	1.8 V	If (U)SIM2 interface is unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM_DET pin. The function supports low-level and high-level detections. In the default software configuration, the USIM_DET pin is at low level when a (U)SIM card is inserted. You can change the software configuration with **AT+QSIMDET**.

See ***document [2]*** for details about **AT+QSIMDET** command.

Normally Closed (U)SIM Card Connector:

- When the (U)SIM card is absent, CD is short-circuited to ground and USIM_DET is at low level.
- When the (U)SIM card is inserted, CD is open from ground and USIM_DET is at high level.

The following figure shows a reference design of (U)SIM interface with a normally closed (NC) (U)SIM card connector.

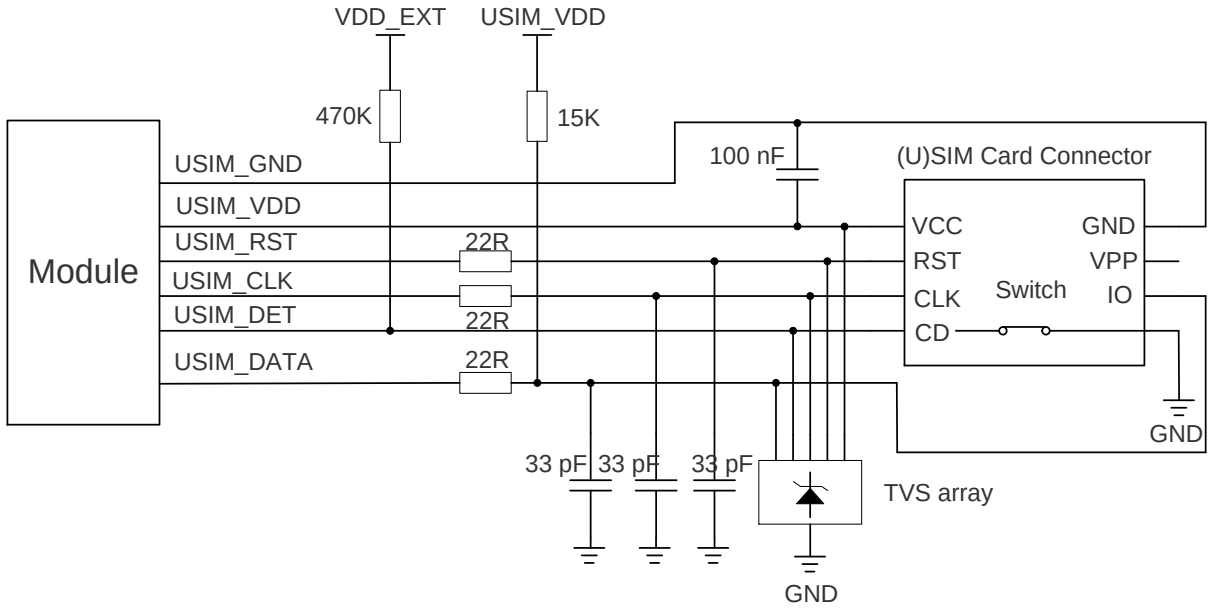


Figure 18: Reference Circuit of Normally Closed (U)SIM Card Connector

Normally Open (U)SIM Card Connector:

- When the (U)SIM card is absent, CD is open from ground and USIM_DET is at high level.
- When the (U)SIM card is inserted, CD is short-circuited to ground and USIM_DET is at low level.

If (U)SIM card detection function is not needed, keep USIM_DET open.

The following figure shows a reference design of (U)SIM interface with a normally open (NO) (U)SIM card connector.

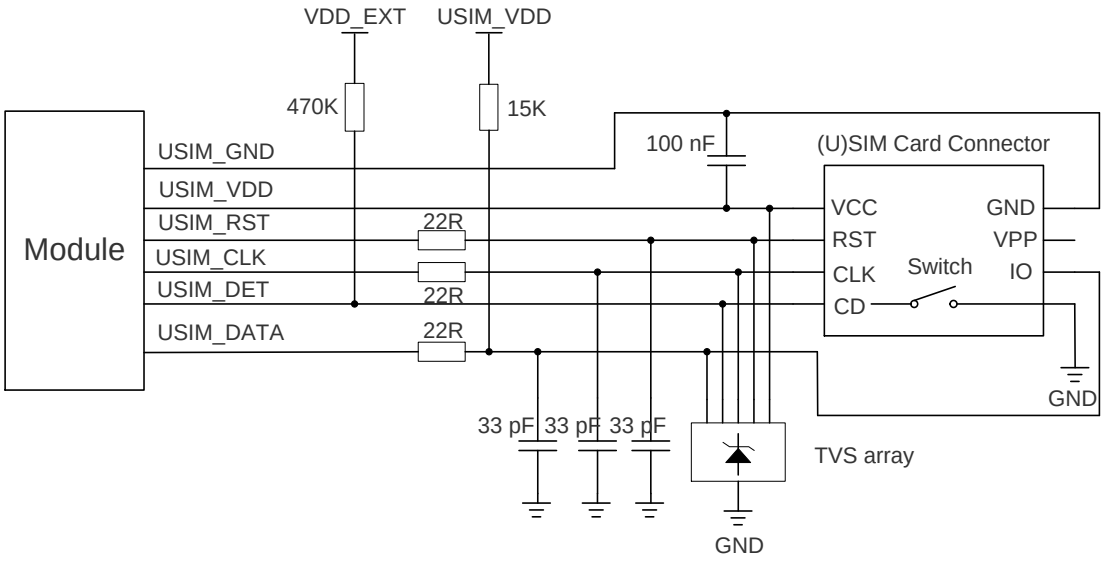


Figure 19: Reference Circuit of Normally Open (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, please follow the criteria below in (U)SIM circuit design.

- Keep (U)SIM card connector as close as possible to the module. Keep the trace length as short as possible, 200 mm at most.
- Keep (U)SIM card signal traces away from RF and VBAT traces.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with ground surrounded.
- For better ESD protection, it is recommended to add a TVS array with a parasitic capacitance not exceeding 50 pF. The 22 Ω resistors should be added in series between the module and the (U)SIM card connector to suppress EMI spurious transmission and enhance ESD protection. The 33 pF capacitors are used to filter out RF interference.
- The pull-up resistor on USIM_DATA trace improves anti-jamming capability and should be placed close to the (U)SIM card connector.
- (U)SIM card hot-plug function is supported by default.

4.4. UART Interface

Table 16: UART Information

UART Interface	Supported Baud Rate (Unit: bps)	Default Baud Rate (Unit: bps)	Function
Debug UART	115200	115200	Linux console and log output

Table 17: Pin Definition of UART Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_RXD	88	DI	Debug UART receive	1.8 V	If unused, keep these pins open.
DBG_TXD	89	DO	Debug UART transmit	1.8 V	

The following figure illustrates the reference design for UART interface connection between the module and AP.

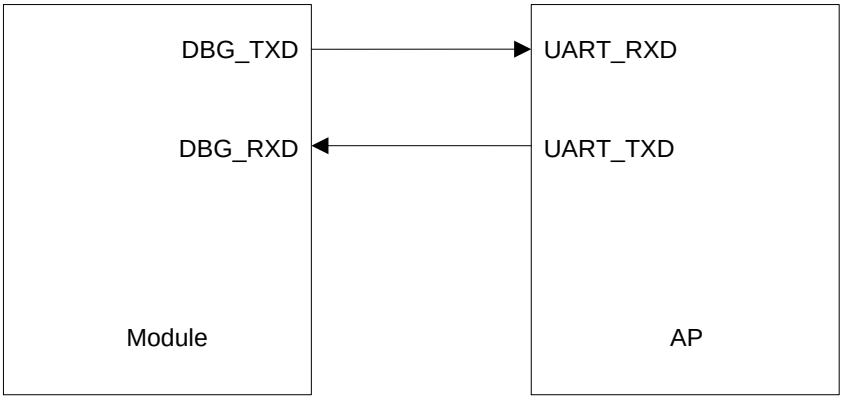


Figure 20: UART Interface Connection

The module provides 1.8 V UART interface. A level shift circuit should be used if the application is equipped with a 3.3 V UART interface.

An example with translator chip is shown as below.

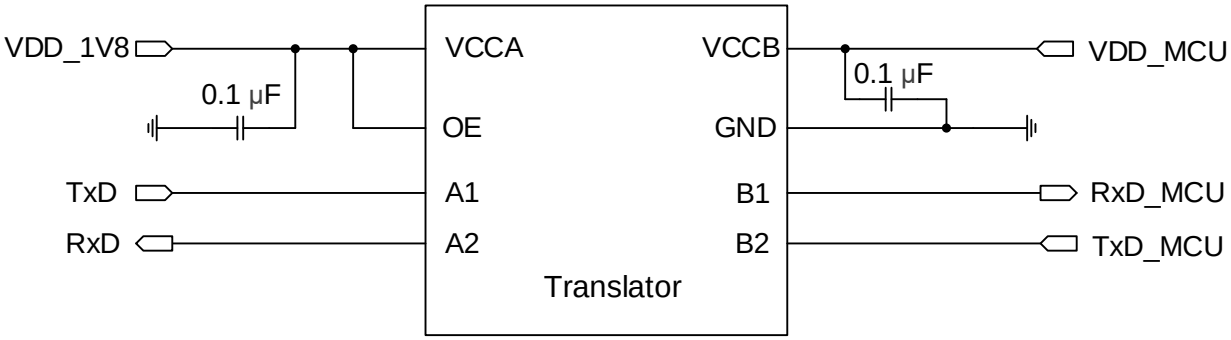


Figure 21: Reference Circuit with Translator Chip

Another example with transistor circuit is shown as below.

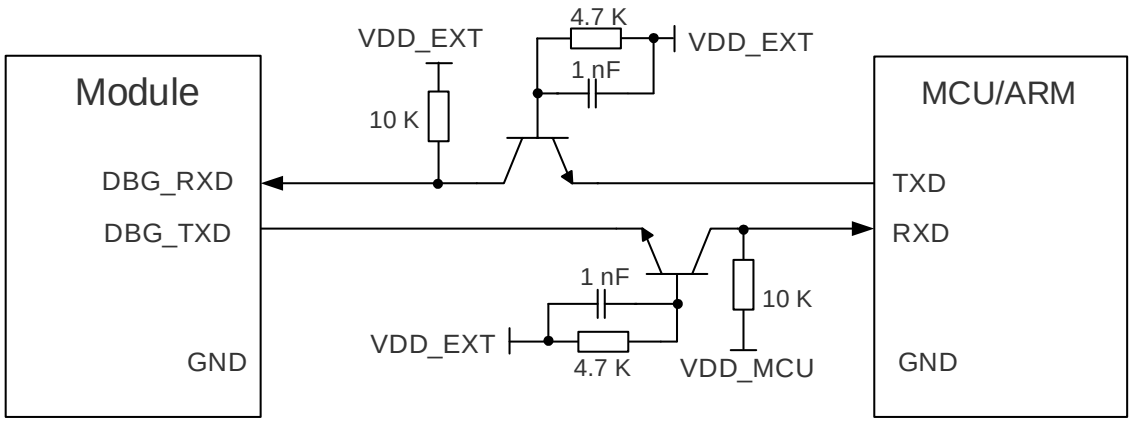


Figure 22: Reference Circuit with Transistor Circuit

4.5. ADC Interface

The module provides one Analog-to-Digital Converter (ADC) interface. To improve the accuracy of the ADC interface, the interface trace should be surrounded by ground.

Table 18: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
ADC0	18	AI	General-purpose ADC interface	Voltage range: 0–1.875 V	If unused, keep it open.

The voltage value on the ADC interface can be read via **AT+QADC=<port>** command. For more details about the AT command, see ***document [2]***.

The resolution of the ADC interface is up to 14 bits. The following table describes the characteristics of the ADC interface.

Table 19: Characteristics of ADC Interface

Characteristics	Min.	Typ.	Max.	Unit
Voltage Range	0	-	1.875	V
Input Resistance	10	-	-	MΩ
Resolution	-	14	-	bits
Sample Rate	-	4.8	-	MHz

NOTE

1. The input voltage of ADC0 should not exceed its corresponding voltage range.
2. It is prohibited to supply any voltage to ADC0 when VBAT is removed.
3. It is recommended to use voltage divider circuit for ADC0 application.

4.6. Indication Interfaces

Table 20: Pin Definition of Indication Interfaces

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
STATUS	24	DO	Indicate the module's operation status	1.8 V	If unused, keep these pins open.
SLEEP_IND	23	DO	Indicate the module's sleep mode		
NET_MODE	25	DO	Indicate the module's network registration mode		
NET_STATUS	27	DO	Indicate the module's network activity status		

4.6.1. STATUS

The STATUS pin is an output pin, indicating the module's operation status. It will output high level when module is powered on successfully. A reference circuit is shown as below.

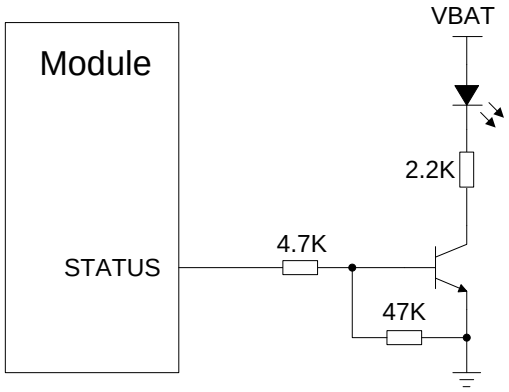


Figure 23: Reference Circuit of STATUS

4.6.2. SLEEP_IND

The SLEEP_IND pin is an output pin, indicating the module's sleep mode. It will output high level when module enters sleep mode. A reference circuit is shown as below.

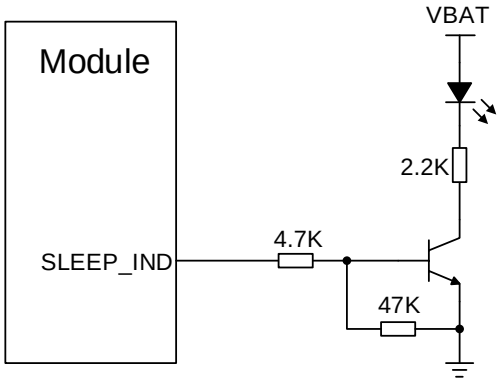


Figure 24: Reference Circuit of SLEEP_IND

4.6.3. Network Status Indication

The module provides two network indication pins: NET_MODE and NET_STATUS which can drive network status indication LEDs. The following tables describe logic level changes of NET_MODE and NET_STATUS in different network status.

Table 21: Working State of the Network Status Indication Pins

Pin Name	Status	Description
NET_MODE	Always High	Registered on LTE network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing

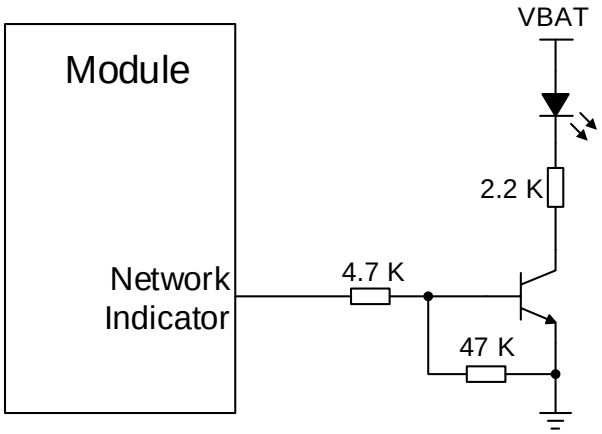


Figure 25: Reference Circuit of Network Status Indication

4.7. W_DISABLE#

The module provides pin W_DISABLE# to enable or disable airplane mode through hardware operation. W_DISABLE# is pulled up by default, and driving it low will set the module to airplane mode.

Table 22: Pin Definition of W_DISABLE#

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
W_DISABLE#	90	DI	Airplane mode control	1.8 V	Pulled up by default. At low voltage level, the module will enter airplane mode.

	If unused, keep it open.

The RF function can also be enabled or disabled through software AT commands. See ***document [2]*** for details of **AT+CFUN=<fun>**.

Table 23: RF Function Status

W_DISABLE# Level	AT Commands	RF Function Status
High Level	**AT+CFUN=1**	Enabled
High Level	**AT+CFUN=0** **AT+CFUN=4**	Disabled
Low Level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled

4.8. DPR

The module provides a DPR (Dynamic Power Reduction) pin for SAR (Specific Absorption Rate) detection. The signal is sent by a host system proximity sensor to the module to provide an input trigger, which will reduce the output power in radio transmission.

Table 24: Pin Definition of DPR

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DPR	15	DI	Dynamic power reduction	1.8 V	Active low.

Table 25: Function of DPR

DPR Level	Function
High/Floating	Max transmitting power will NOT be backed off
Low	Max transmitting power will be backed off

5 RF Specifications

5.1. Antenna Interfaces & Frequency Bands

Table 26: Pin Definition of Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN1	98	AIO	Main antenna interface LTE LMB_TRX ● For EG065K-NA, LMB includes B2/B4/B5/B12/B13/B14/B25/B26/B66 ● For EG065K-EA, LMB includes B1/B2/B3/B4/B5/B8/B20/B28	50 Ω impedance.
ANT_MAIN2	107	AIO	Main antenna interface LTE HB_TRX ● For EG065K-NA, HB includes B7/B30 ● For EG065K-EA, HB includes B7/B40	
ANT_DIV1	125	AI	Diversity antenna interface LTE MHB_DRX ● For EG065K-NA, MHB includes B2/B4/B7/B25/B30/B66 ● For EG065K-EA, MHB includes B1/B2/B3/B4/B7/B40	
ANT_DIV2	133	AI	Diversity antenna interface LTE LB_DRX ● For EG065K-NA, LB includes B5/B12/B13/B14/B26 ● For EG065K-EA, LB includes B5/B8/B20/B28	

NOTE

Only passive antennas are supported.

Table 27: Operating Frequency of EG065K-NA

Operating Frequency	Transmit (MHz)	Receive (MHz)
B2	1850–1910	1930–1990
B4	1710–1755	2110–2155
B5	824–849	869–894
B7	2500–2570	2620–2690
B12	699–716	729–746
B13	777–787	746–756
B14	788–798	758–768
B25	1850–1915	1930–1995
B26	814–849	859–894
B30	2305–2315	2350–2360
B66	1710–1780	2110–2200

Table 28: Operating Frequency of EG065K-EA

Operating Frequency	Transmit (MHz)	Receive (MHz)
B1	1920–1980	2110–2170
B2	1850–1910	1930–1990
B3	1710–1785	1805–1880
B4	1710–1755	2110–2155
B5	824–849	869–894
B7	2500–2570	2620–2690
B8	880–915	925–960
B20	832–862	791–821
B28	703–748	758–803
B40	2300–2400	2300–2400

5.1.1. Tx Power

Table 29: Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE-FDD B30	22.3 dBm ±2 dB	< -40 dBm
LTE-FDD other bands	23.5 dBm ±2 dB	< -40 dBm
LTE-TDD bands		

5.1.2. Rx Sensitivity

Table 30: Rx Sensitivity of EG065K-NA

Frequency (10 MHz)	Rx Sensitivity (Typ.)			3GPP (SIMO) (dBm)
	Primary (dBm)	Diversity (dBm)	SIMO (dBm)	
LTE-FDD B2	-98	-99	-101	-94.3
LTE-FDD B4	-97.5	-99	-100.5	-96.3
LTE-FDD B5	-97.5	-100.3	-101	-94.3
LTE-FDD B7	-97	-97.3	-100	-94.3
LTE-FDD B12	-98	-101	-102.3	-93.3
LTE-FDD B13	-97.5	-100.3	-102	-93.3
LTE-FDD B14	-96.5	-100	-101.5	-93.3
LTE-FDD B25	-98	-98.3	-101	-92.8
LTE-FDD B26	-97.5	-100	-101	-93.8
LTE-FDD B30	-97.3	-97	-99.5	-95.3
LTE-FDD B66	-97.5	-98.5	-100.5	-95.8

Table 31: Rx Sensitivity of EG065K-EA

Frequency (10 MHz)	Rx Sensitivity (Typ.)			3GPP (SIMO) (dBm)
	Primary (dBm)	Diversity (dBm)	SIMO (dBm)	
LTE-FDD B1	-96.5	-98.5	-100	-96.3
LTE-FDD B2	-97.5	-98	-100	-94.3
LTE-FDD B3	-96.7	-98	-100	-93.3
LTE-FDD B4	-97.3	-98.5	-100.2	-96.3
LTE-FDD B5	-97	-100.5	-102	-94.3
LTE-FDD B7	-97.3	-98.5	-100	-94.3
LTE-FDD B8	-96.2	-99.5	-102	-93.3
LTE-FDD B20	-98	-98	-101	-93.3
LTE-FDD B28	-98	-99.5	-101.5	-94.8
LTE-TDD B40	-96.5	-98.2	-99.5	-96.3

5.1.3. Reference Design

The module provides four RF antenna interfaces for antenna connection.

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1, R2, R3, R4, C1, C2, C3, C4, C5, C6, C7 and C8) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

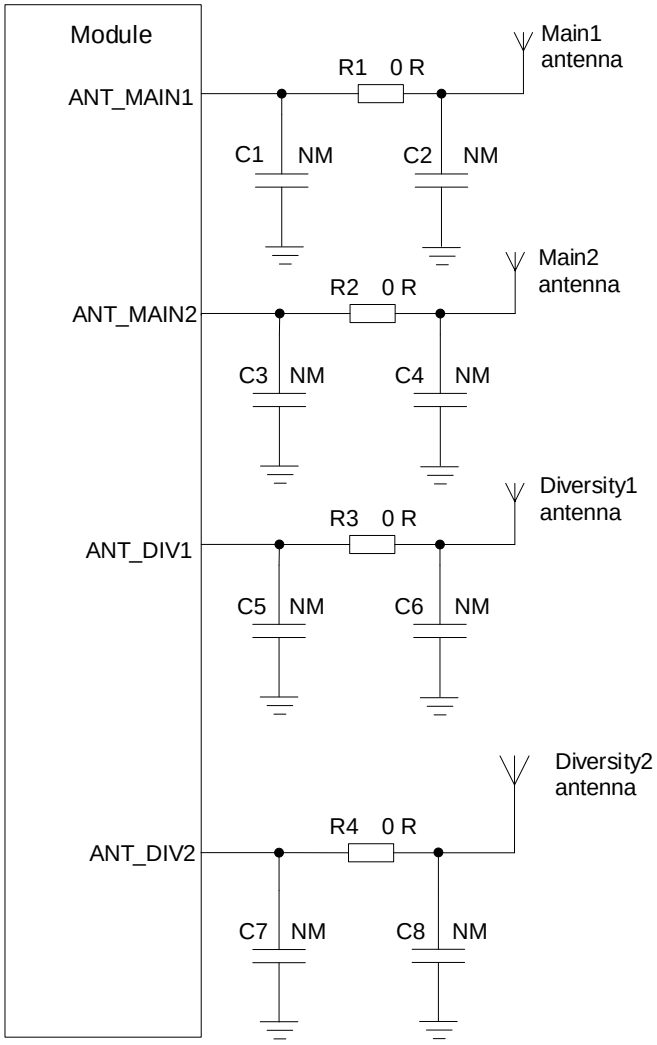


Figure 26: Reference Circuit for RF Antenna Interfaces

5.1.4. Antenna Tuner Control Interfaces

5.1.4.1. Antenna Tuner Control Interface Through RFFE

Table 32: Pin Definition of Antenna Tuner Control Interface Through RFFE

Pin Name	Pin No.	I/O	Description	Comment
RFFE5_CLK	66	DO	Used for external MIPI IC control	If unused, keep these pins open.
RFFE5_DATA	69	DIO	Used for external MIPI IC control	

5.1.4.2. Antenna Tuner Control Interfaces Through GRFC

Table 33: Pin Definition of Antenna Tuner Control Interfaces Through GRFC

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
GRFC1	118	DO	Generic RF controller	1.8 V	If unused, keep these pins open.
GRFC6	121	DO	Generic RF controller		
GRFC33	103	DO	Generic RF controller		
GRFC34	106	DO	Generic RF controller		

Table 34: Truth Table of GRFC Interfaces for EG065K-NA

GRFC6 Level	GRFC1 Level	GRFC34 Level	GRFC33 Level	Band
High	Low	High	Low	B12
High	High	High	High	B13
Low	High	Low	High	B14
Low	Low	Low	Low	B5
Low	Low	Low	Low	B26
Low	Low	Low	Low	B4
Low	Low	Low	Low	B25
Low	Low	Low	Low	B2
Low	Low	Low	Low	B66
Low	Low	Low	Low	B30
Low	Low	Low	Low	B7

Table 35: Truth Table of GRFC Interfaces for EG065K-EA

GRFC6 Level	GRFC1 Level	GRFC34 Level	GRFC33 Level	Band
High	Low	High	Low	B28

High	High	High	High	B20
Low	High	Low	High	B5
Low	Low	Low	Low	B8
Low	Low	Low	Low	B3
Low	Low	Low	Low	B4
Low	Low	Low	Low	B2
Low	Low	Low	Low	B1
Low	Low	Low	Low	B40
Low	Low	Low	Low	B7

NOTE

"Low" means "V_{OL}", and "High" means "V_{OH}".

5.2. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

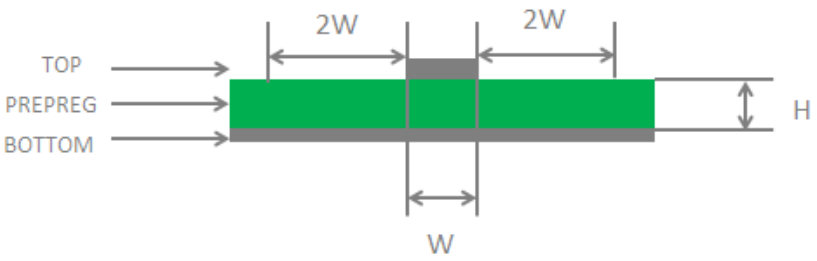


Figure 27: Microstrip Design on a 2-layer PCB

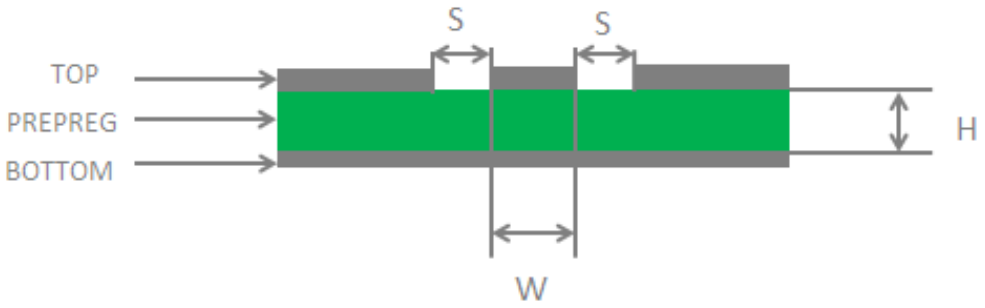


Figure 28: Coplanar Waveguide Design on a 2-layer PCB

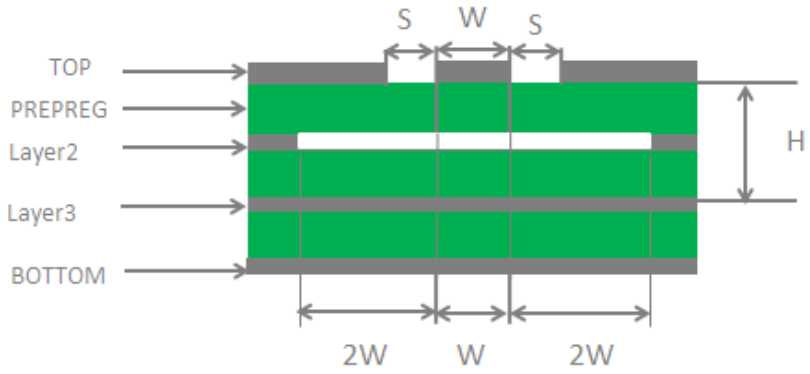


Figure 29: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

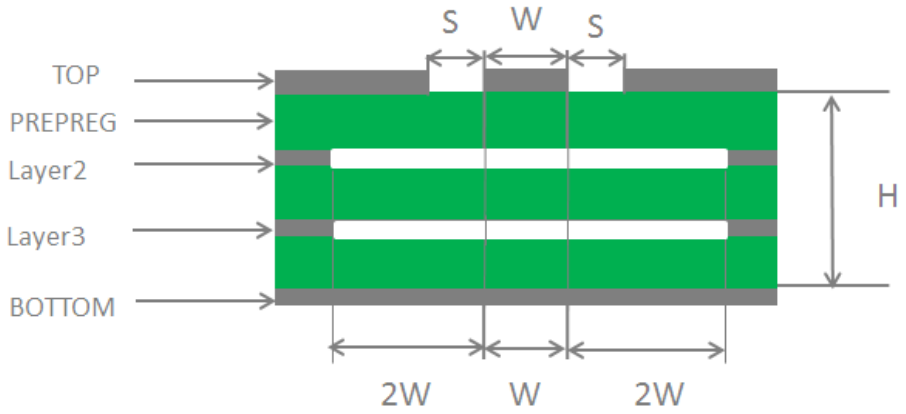


Figure 30: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be

fully connected to ground.

- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be no less than two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.3. Antenna Design Requirements

Table 36: Requirements for Antenna Design

Antenna Type	Requirements
LTE	VSWR: ≤ 2 Efficiency: > 30 % Max input power: 50 W Input impedance: 50 Ω Cable insertion loss: < 1 dB (699–960 MHz) Cable insertion loss: < 1.5 dB (1710–2200 MHz) Cable insertion loss: < 2 dB (2300–2690 MHz)

NOTE

It is recommended to use passive GNSS antennas when LTE B13 or B14 is supported, as the use of active antenna may generate harmonics which will affect the GNSS performance.

5.4. RF Connector Recommendation

The recommended receptacle dimensions are illustrated as below.

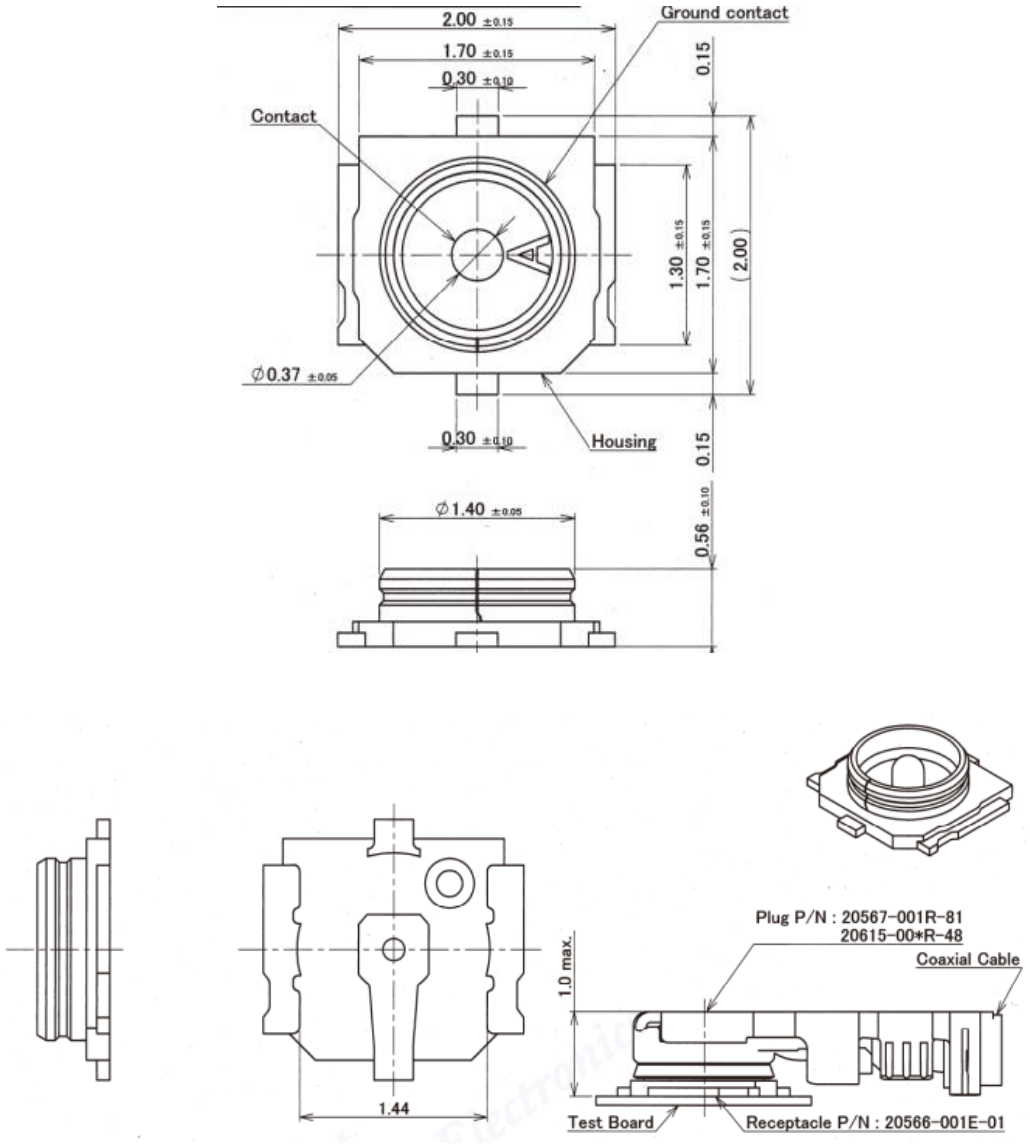


Figure 31: Dimensions of the Receptacles (Unit: mm)

The following figure shows the specifications of mating plugs using ø0.81 mm coaxial cables.

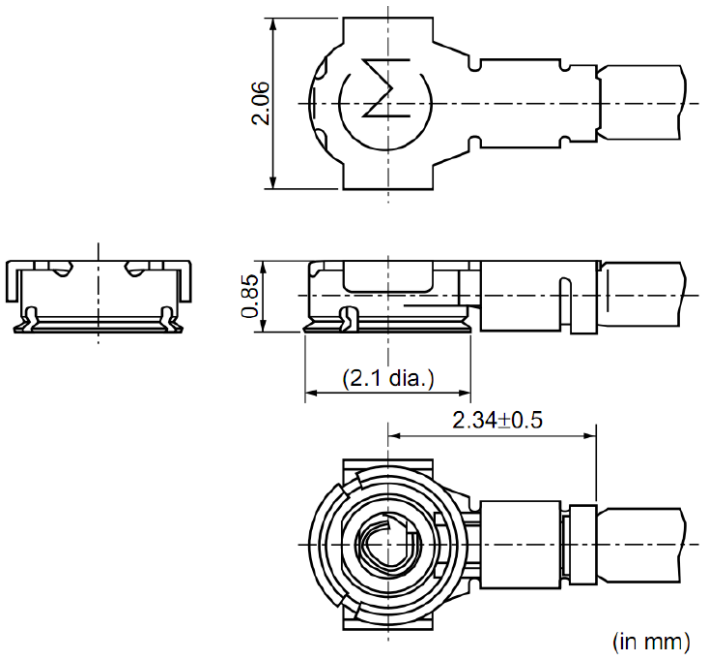


Figure 32: Specifications of Mating Plugs Using ø0.81 mm Coaxial Cables (Unit: mm)

For more details, please visit https://www.i-pex.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 37: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	0.8	A
Peak Current of VBAT_RF	-	1.2	A
Voltage on Digital Pins	-0.3	2.3	V
Voltage at ADC0	-	1.875	V

6.2. Power Supply Ratings

Table 38: Module Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must stay between the minimum and maximum values.	3.3	3.8	4.5	V
USB_VBUS	USB connection detection	-	3.3	5.0	5.25	V

6.3. Power Consumption

Table 39: EG065K-NA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	26	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.46	mA
	LTE-FDD @ DRX = 0.32 s	5.16	mA
	LTE-FDD @ DRX = 0.64 s	3.93	mA
	LTE-FDD @ DRX = 0.64 s, USB Suspend	4.23	mA
	LTE-FDD @ DRX = 1.28 s	3.09	mA
	LTE-FDD @ DRX = 2.56 s	2.56	mA
Idle state	LTE-FDD @ DRX = 0.64 s	12.77	mA
	LTE-FDD @ DRX = 0.64 s, USB Active	29.24	mA
LTE data transfer	LTE-FDD B2 CH900 @ 23.5 dBm	545	mA
	LTE-FDD B4 CH2175 @ 23.5 dBm	545	mA
	LTE-FDD B5 CH2525 @ 23.5 dBm	590	mA
	LTE-FDD B7 CH3100 @ 23.5 dBm	760	mA
	LTE-FDD B12 CH5095 @ 23.5 dBm	590	mA
	LTE-FDD B13 CH5230 @ 23.5 dBm	660	mA
	LTE-FDD B14 CH5330 @ 23.5 dBm	630	mA
	LTE-FDD B25 CH8365 @ 23.5 dBm	550	mA
	LTE-FDD B26 CH8865 @ 23.5 dBm	645	mA
	LTE-FDD B30 CH9820 @ 22.3 dBm	601	mA
	LTE-FDD B66 CH66786 @ 23.5 dBm	560	mA

Table 40: EG065K-EA Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	26	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	1.43	mA
	LTE-FDD @ DRX = 0.32 s	4.75	mA
	LTE-FDD @ DRX = 0.64 s	3.36	mA
	LTE-FDD @ DRX = 0.64 s, USB Suspend	3.69	mA
	LTE-FDD @ DRX = 1.28 s	2.66	mA
	LTE-FDD @ DRX = 2.56 s	2.24	mA
	LTE-TDD @ DRX = 0.32 s	4.77	mA
	LTE-TDD @ DRX = 0.64 s	3.25	mA
	LTE-TDD @ DRX = 0.64 s, USB Suspend	3.56	mA
	LTE-TDD @ DRX = 1.28 s	2.53	mA
	LTE-TDD @ DRX = 2.56 s	2.16	mA
Idle state	LTE-FDD @ DRX = 0.64 s	12.58	mA
	LTE-FDD @ DRX = 0.64 s, USB Active	19.03	mA
	LTE-TDD @ DRX = 0.64 s	12.38	mA
	LTE-TDD @ DRX = 0.64 s, USB Active	18.95	mA
LTE data transfer	LTE-FDD B1 CH300 @ 23.5 dBm	655	mA
	LTE-FDD B2 CH900 @ 23.5 dBm	610	mA
	LTE-FDD B3 CH1575 @ 23.5 dBm	620	mA
	LTE-FDD B4 CH2175 @ 23.5 dBm	595	mA
	LTE-FDD B5 CH2525 @ 23.5 dBm	620	mA
	LTE-FDD B7 CH3100 @ 23.5 dBm	710	mA
	LTE-FDD B8 CH3625 @ 23.5 dBm	650	mA
	LTE-FDD B20 CH6300 @ 23.5 dBm	650	mA

	LTE-FDD B28 CH9435 @ 23.5 dBm	650	mA
	LTE-TDD B40 CH39150 @ 23.5 dBm	390	mA

6.4. Digital I/O Characteristics

Table 41: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.2	2.0	V
V_{IL}	Input low voltage	-0.3	0.6	V
V_{OH}	Output high voltage	1.35	1.8	V
V_{OL}	Output low voltage	0	0.45	V

Table 42: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V
V_{IH}	Input high voltage	1.26	-	V
V_{IL}	Input low voltage	-	0.36	V
V_{OH}	Output high voltage	1.45	-	V
V_{OL}	Output low voltage	-	0.4	V

Table 43: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.75	3.05	V
V_{IH}	Input high voltage	2.0	-	V
V_{IL}	Input low voltage	-	0.57	V

V_{OH}	Output high voltage	2.3	-	V
V_{OL}	Output low voltage	-	0.4	V

6.5. ESD Protection

If the static electricity generated by various ways discharges to the module, the module maybe damaged to a certain extent. Thus, please take proper ESD countermeasures and handling methods. For example, wearing anti-static gloves during the development, production, assembly and testing of the module; adding ESD protective components to the ESD sensitive interfaces and points in the product design.

Table 44: Electrostatics Discharge Characteristics (25 °C, 45 % Relative Humidity)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
All Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operating and Storage Temperatures

Table 45: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-30	25	75	°C
Extended Operating Temperature Range [5]	-40	-	85	°C
Storage temperature range	-40	-	90	°C

[4] To meet this operating temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this operation temperature range, the module can meet 3GPP specifications.

[5] To meet this extended temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this extended temperature range, the module remains the ability to establish and maintain functions such as voice, SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are impervious, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal ICs always work within in the recommended operating temperature.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the heatsink should be larger than the module to cover the module completely.
  - Choose the heatsink with adequate fins to dissipate heat.
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module.
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

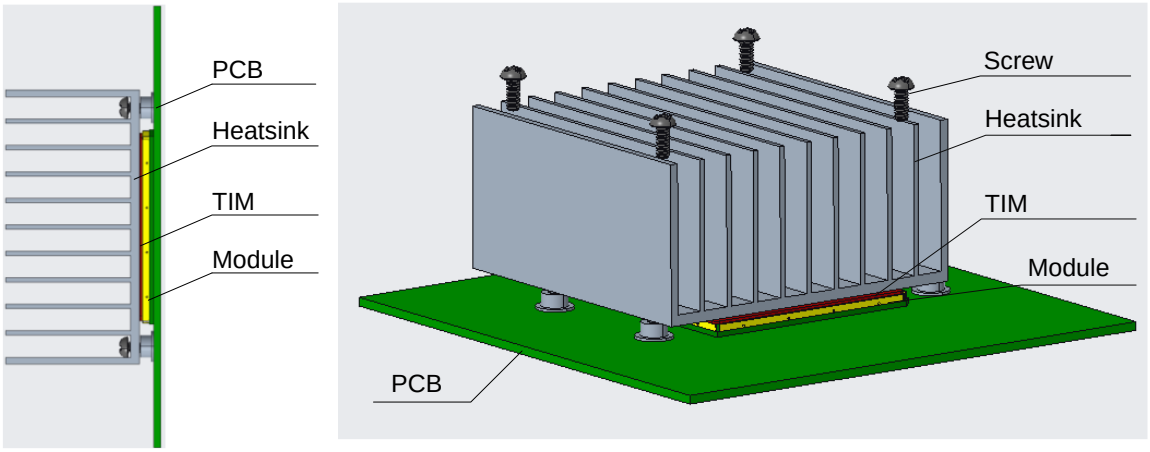


Figure 33: Placement and Fixing of Heatsink

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

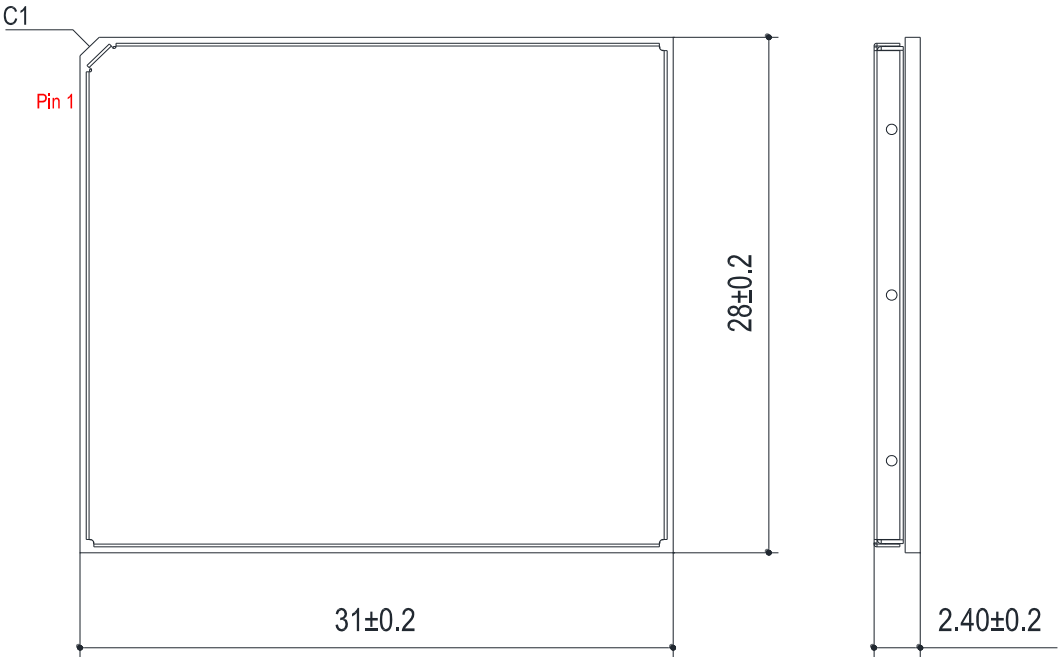


Figure 34: Module Top and Side Dimensions (Unit: mm)

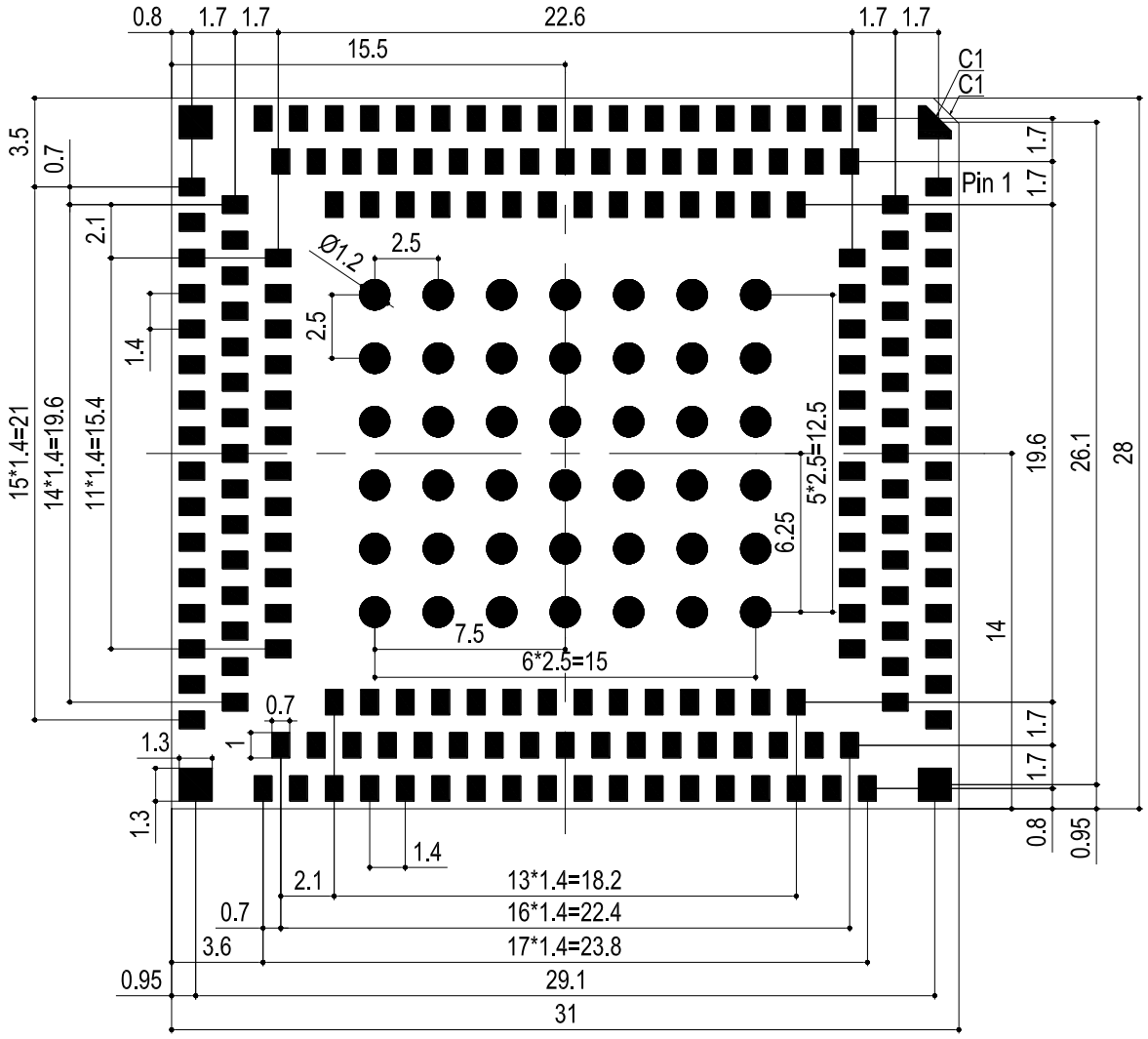


Figure 35: Module Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

7.2. Recommended Footprint

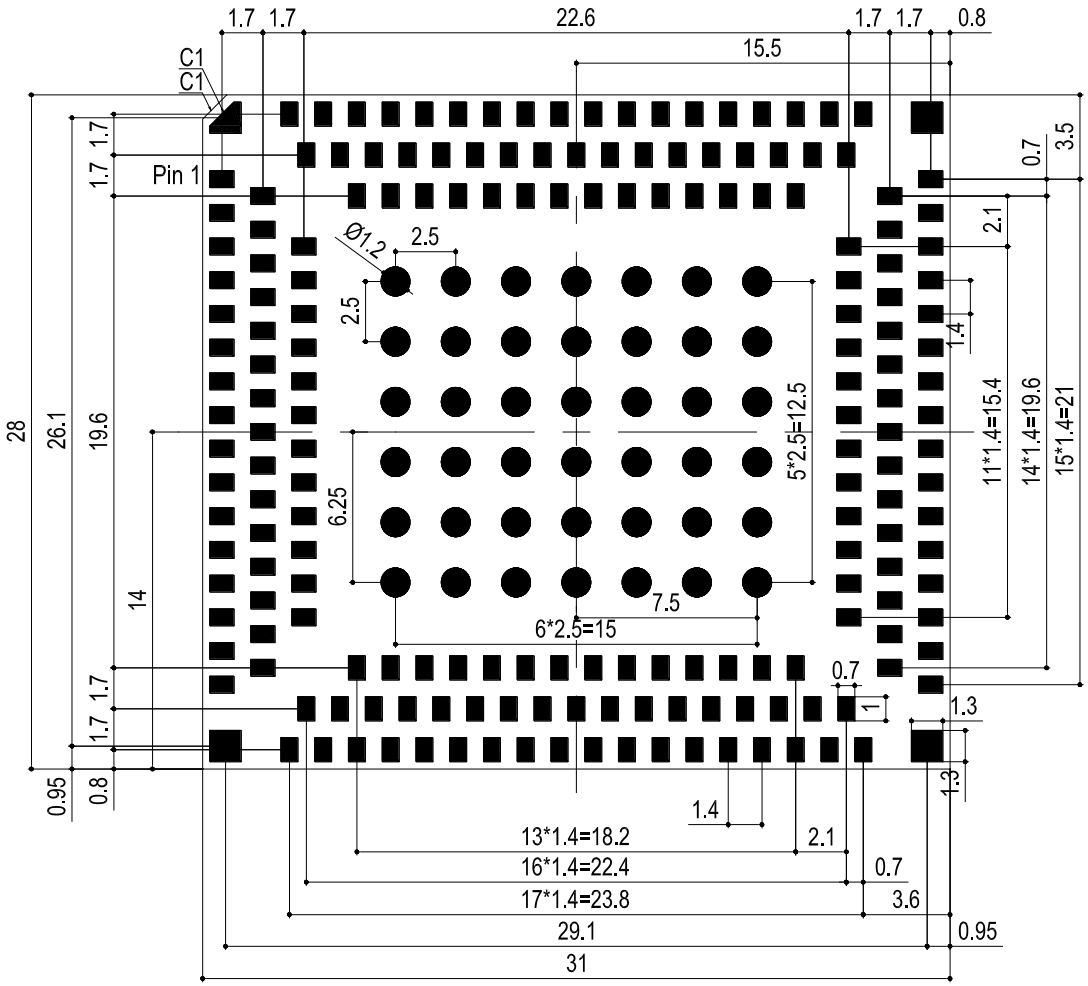


Figure 36: Recommended Footprint (Top View, Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

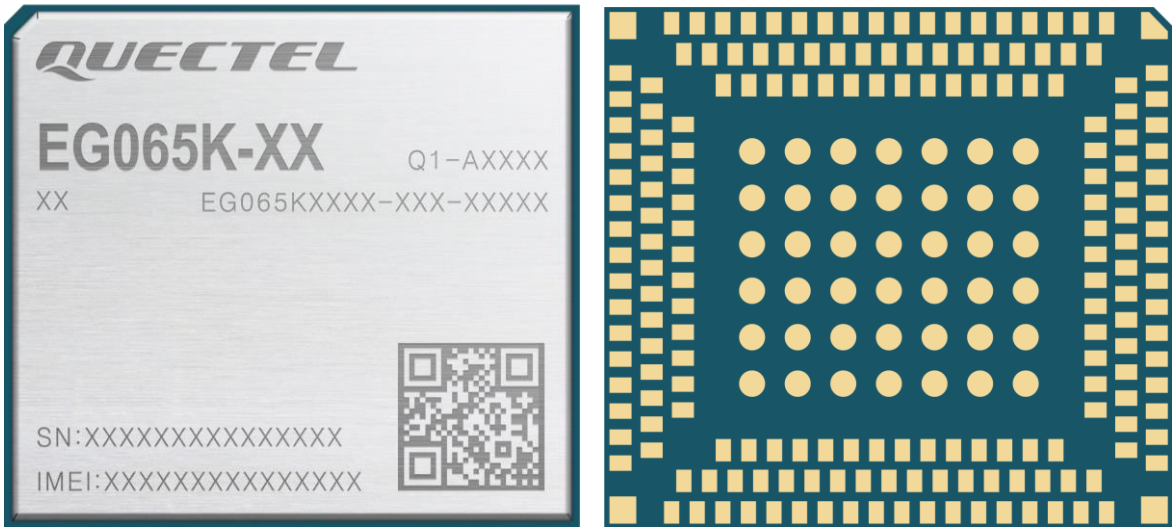


Figure 37: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, see the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed package. MSL of the module is rated as 3, and its storage restrictions are shown as below.

1. Recommended Storage Condition: The temperature should be 23 ±5 °C and the relative humidity should be 35%–60%.

2. The storage life (in vacuum-sealed packaging) is 12 months in Recommended Storage Condition.

3. The floor life of the module is 168 hours [6] in a plant where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g. a drying cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement above occurs;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - All modules must be soldered to PCB within 24 hours after the baking, otherwise they should be put in a dry environment such as in a drying oven.

NOTE

[6] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours after the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.15 mm. For more details, see ***document [4]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

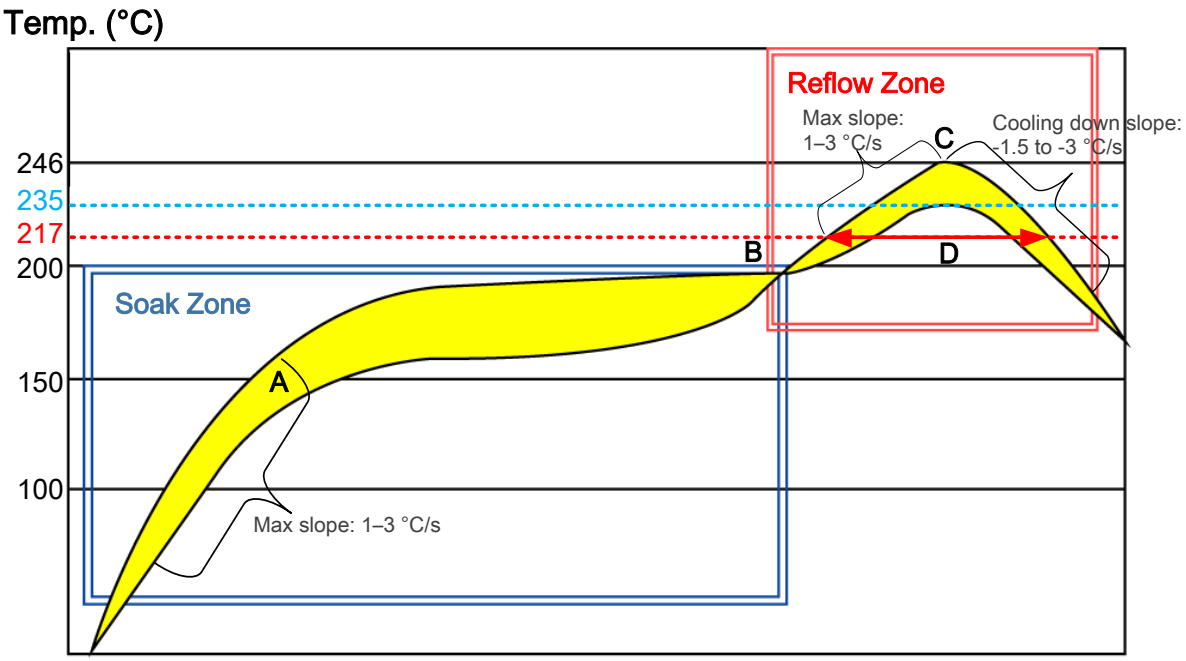


Figure 38: Recommended Reflow Soldering Thermal Profile

Table 46: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

The module adopts carrier tape packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

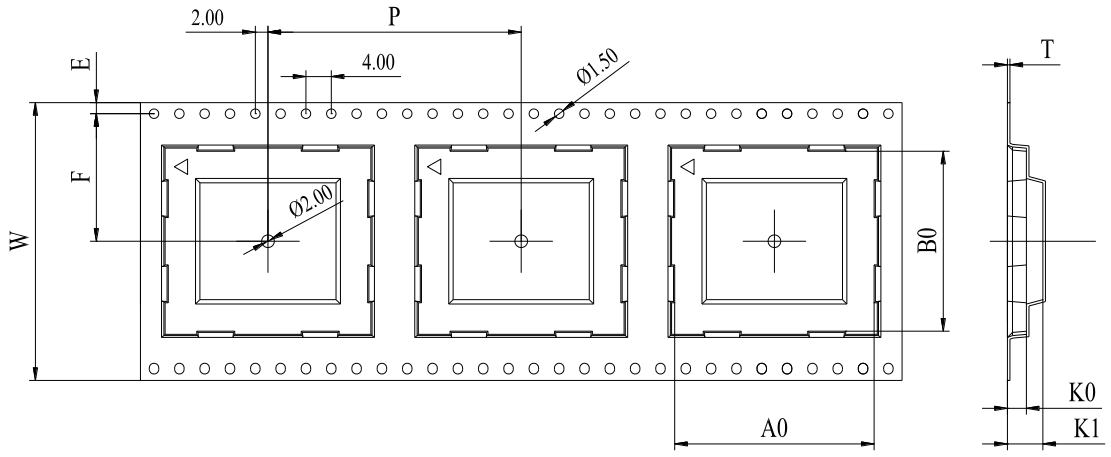


Figure 39: Carrier Tape Dimension Drawing

Table 47: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	40	0.4	31.5	28.5	3.0	5.6	20.2	1.75

8.3.2. Plastic Reel

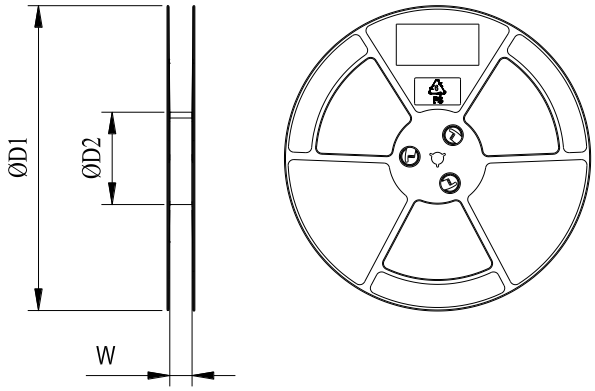
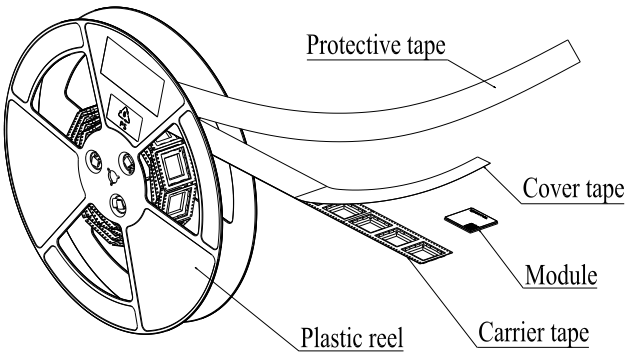


Figure 40: Plastic Reel Dimension Drawing

Table 48: Plastic Reel Dimension Table (Unit: mm)

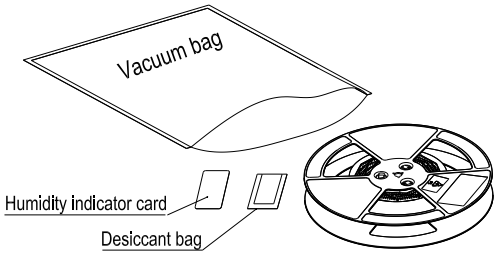
øD1	øD2	W
330	100	44.5

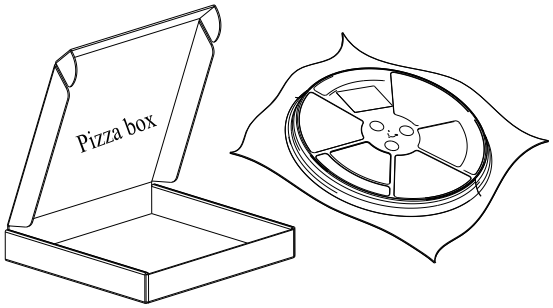
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 1000 modules.

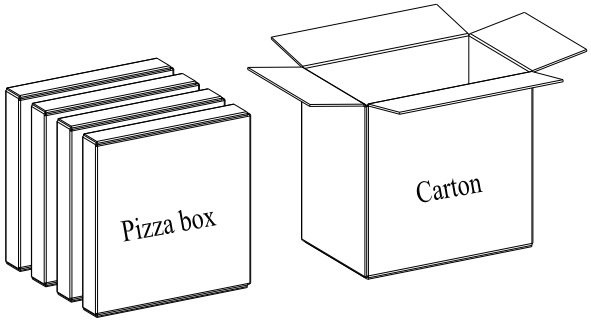


Figure 41: Packaging Process

9 Appendix References

Table 49: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_EG06xK&Ex120K&EM060K_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Secondary_SMT_Application_Note

Table 50: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
APT	Average Power Tracking
bps	bit(s) per second
CHAP	Challenge-Handshake Authentication Protocol
DFOTA	Delta Firmware Upgrade Over-The-Air
DL	Downlink
DRX	Discontinuous Reception
DRx	Diversity Receive
ESD	Electrostatic Discharge
ET	Envelope Tracking
FDD	Frequency Division Duplex
FTP	File Transfer Protocol

GRFC	General RF Control
HB	High Band
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IC	Integrated Circuit
I/O	Input/Output
LB	Low Band
LGA	Land Grid Array
LPDDR	Low-Power Double Data Rate
LTE	Long-Term Evolution
LwM2M	Lightweight M2M
MB	Middle Band
MBIM	Mobile Broadband Interface Model
MCU	Microcontroller Unit
MHB	Middle/High Band
MIMO	Multiple Input Multiple Output
MIPI	Mobile Industry Processor Interface
M2M	Machine to Machine
NITZ	Network Identity and Time Zone
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMIC	Power Management Integrated Circuit

PPP	Point-to-Point Protocol
PRx	Primary Receive
QAM	Quadrature Amplitude Modulation
QMI	Qualcomm Message Interface
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
Rx	Receive
SD	Secure Digital
SMD	Surface Mount Device
SMS	Short Message Service
TDD	Time Division Duplex
TRX	Transmit & Receive
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USB	Universal Serial Bus
(U)SIM	Universal Subscriber Identity Module
VBAT	Voltage at Battery (Pin)
Vmax	Maximum Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage

VSWR	Voltage Standing Wave Ratio
XO	Crystal Oscillator