EG060K-GT Hardware Design

LTE-A Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for your failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-08-18	Elliot CAO/ Lewis PENG/ Jacen HUANG	Creation of the document
1.0.0	2022-08-18	Elliot CAO/ Nancy SHAO/ Jacen HUANG	Preliminary

Contents

Table Index

Figure Index

1 Introduction

This document defines EG060K-GT module and describes its air and hardware interfaces which connects to your applications.

With this document, you can quickly understand the module's interfaces, electrical and mechanical specifications, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Marks

Table 1: Special Marks

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.
[…]	Brackets ([…]) used after a pin enclosing a range of numbers indicate all pins of the same type. For example, SDIO_DATA [0:3] refers to all four SDIO pins: SDIO_DATA0, SDIO_DATA1, SDIO_DATA2, and SDIO_DATA3.

The device could be used with a separation distance of 20cm to the human body.
Product Marketing Name：Quectel EG060K-GT
FCC Certification Requirements.
According to the definition of mobile and fixed device is described in Part 2.1091(b), this device is a mobile device.
And the following conditions must be met:
1. This Modular Approval is limited to OEM installation for mobile and fixed applications only. The antenna installation and operating configurations of this transmitter, including any applicable source-based timeaveraging duty factor, antenna gain and cable loss must satisfy MPE categorical Exclusion Requirements of 2.1091.
2. The EUT is a mobile device; maintain at least a 20 cm separation between the EUT and the user's body and must not transmit simultaneously with any other antenna or transmitter.
3. A label with the following statements must be attached to the host end product: This device contains FCC ID: XMR2022EG060KGT
4. To comply with FCC regulations limiting both maximum RF output power and human exposure to RF

radiation, maximum antenna gain (including cable loss) must not exceed:

radiation, maximum antenna gain (including cable loss) must not exceed: Operating Band	FCC Max Antenna Gain（dBi）
LTE B41	8.00
LTE B48	-1.00

5. This module must not transmit simultaneously with any other antenna or transmitter
6. The host end product must include a user manual that clearly defines operating requirements and conditions that must be observed to ensure compliance with current FCC RF exposure guidelines.

For portable devices, in addition to the conditions 3 through 6 described above, a separate approval is required to satisfy the SAR requirements of FCC Part 2.1093

If the device is used for other equipment that separate approval is required for all other operating configurations, including portable configurations with respect to 2.1093 and different antenna configurations.

For this device, OEM integrators must be provided with labeling instructions of finished products. Please refer to KDB784748 D01 v07, section 8. Page 6/7 last two paragraphs:

A certified modular has the option to use a permanently affixed label, or an electronic label. For a permanently affixed label, the module must be labeled with an FCC ID - Section 2.926 (see 2.2 Certification (labeling requirements) above). The OEM manual must provide clear instructions explaining to the OEM the labeling requirements, options and OEM user manual instructions that are required (see next paragraph).

For a host using a certified modular with a standard fixed label, if (1) the module's FCC ID is not visible when installed in the host, or (2) if the host is marketed so that end users do not have straightforward commonly used methods for access to remove the module so that the FCC ID of the module is visible; then an additional permanent label referring to the enclosed module: "Contains Transmitter Module FCC ID: XMR2022EG060KGT" or "Contains FCC ID: XMR2022EG060KGT" must be used. The host OEM user manual must also contain clear instructions on how end users can find and/or access the module and the FCC ID.

The final host / module combination may also need to be evaluated against the FCC Part 15B criteria for unintentional radiators in order to be properly authorized for operation as a Part 15 digital device.

The user's manual or instruction manual for an intentional or unintentional radiator shall caution the user that changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment. In cases where the manual is provided only in a form other than paper, such as on a computer disk or over the Internet, the information required by this section may be included in the manual in that alternative form, provided the user can reasonably be expected to have the capability to access information in that form.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

To ensure compliance with all non-transmitter functions the host manufacturer is responsible for ensuring compliance with the module(s) installed and fully operational. For example, if a host was previously authorized as an unintentional radiator under the Supplier's Declaration of Conformity procedure without a transmitter certified module and a module is added, the host manufacturer is responsible for ensuring

that the after the module is installed and operational the host continues to be compliant with the Part 15B unintentional radiator requirements.

Manual Information To the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

IC Statement

IRSS-GEN

"This device complies with Industry Canada's licence-exempt RSSs. Operation is subject to the following two conditions: (1) This device may not cause interference; and (2) This device must accept any interference, including interference that may cause undesired operation of the device."The transmitter module may not be co-located with any other transmitter orantenna. or "Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radi o exempts de licence.L'exploitation est autoris ée a ux deux conditions suivantes :

1) l'appareil ne doit pas produire de brouillage; 2) l'utilisateur de l'appareil doit accepter tout brouill age radioélectrique subi, même si le brouillage est susc eptible d'en compromettre le fonctionnement." Déclarat ion sur l'exposition aux rayonnements RF

L'autre utilisépour l'émetteur doit être installé pour fournir une distance de séparation d'au moins 20 cm de toutes les personnes et ne doit pas être colocalisé ou fonctionner conjointement avec une autre antenne ou un autre émet teur.

The host product shall be properly labeled to identify the modules within the host product.

The Innovation, Science and Economic Development Canada certification label of a module shall be clearly visible at all times when installed in the host product; otherwise, the host product must be labeled to display the Innovation, Science and Economic Development Canada certification number for the module, preceded by the word "Contains" or similar wording expressing the same meaning, as follows: "Contains IC: 10224A-2022EG060GT" or "where: 10224A-2022EG060GT is the module's certification number".

Le produit hôte doit être correctement étiqueté pour identifier les modules dans le produit hôte. L'étiquette de certification d'Innovation, Sciences et Développement économique Canada d'un module doit être clairement visible en tout temps lorsqu'il est installédans le produit hôte; sinon, le produit hôte doit porter une étiquette indiquant le numéro de certification d'Innovation, Sciences et Développement économique Canada pour le module, préc édé du mot «Contient» ou d'un libellés emblable exprimant la même signification, comme suit:

"Contient IC: 10224A-2022EG060GT " ou "où: 10224A-2022EG060GT est le numéro de certification du module".

2 Product Overview

The module is an LTE-TDD wireless communication module with receive diversity. It provides data connectivity on LTE-TDD networks. The module supports embedded operating systems such as Windows, Linux and Android. It also provides GNSS to meet specific application demands.

2.1. Frequency Bands and Functions

Table 2: Frequency Bands and Functions

Frequency Bands and Functions	EG060K-GT
LTE-TDD (with Rx-diversity)	B41/B48
2CA	CA_41A-41A, , CA_41C, CA_48C
GNSS	GPS, GLONASS, BDS, Galileo

With a compact profile of 37.0 mm × 39.5 mm × 2.8 mm, the module meets most of requirements for M2M applications such as security, 4G router, CPE, wireless POS terminal, mobile computing device, PDA phone, and tablet PC. The module is an SMD type module and can be embedded in applications through its 299 LGA pins.

2.2. Key Features

Table 3: Key Features

Feature	Details
Power Supply	● Supply voltage range: 3.3–4.4 V ● Typical supply voltage: 3.8 V
Transmitting Power	Class 3 (23 dBm ±2 dB)*
LTE Features	● Supports 3GPP Rel-12 LTE-TDD ● Supports CA Category - Supports up to Cat 6 ● Supports 1.4/3/5/10/15/20 MHz RF bandwidth LTE-TDD: Max. 226 Mbps (DL)/28 Mbps (UL)
MCP	4 Gb NAND + 4 Gb LPDDR2
Internet Protocol Features	Supports QMI/MBIM/NITZ/HTTP/HTTPS/FTP/LwM2M*/PING* protocols
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
USIM Interfaces	● Supports USIM card: 1.8/3.0 V ● Supports Dual USIM Single Standby
Audio Features	● Provides one digital audio interface: PCM interface ● LTE: AMR/AMR-WB ● Supports echo cancellation and noise suppression
PCM Interface	● Used for audio function with an external codec or SLIC ● Supports 16-bit linear data format ● Supports long and short frame synchronization ● Supports master and slave modes, but the module must work as master in long frame synchronization
USB Interface	● Complies with USB 3.0 and 2.0 specifications, with max. transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 ● Used for AT command communication, data transmission, firmware upgrade, software debugging, GNSS NMEA sentence output. ● Supports USB serial drivers for: Windows 7/8/8.1/10/11, Linux 2.6–5.18, Android 4.x–12.x
UART Interfaces	**Main UART interface:** ● Used for AT command communication and data transmission ● Baud rate reaches up to 921600 bps, 115200 bps by default ● Supports RTS and CTS hardware flow control **Debug UART interface:** ● Used for Linux console and log output ● 115200 bps baud rate **Bluetooth UART interface*:** ● Multiplexed from SPI interface ● Used for Bluetooth communication ● 115200 bps baud rate
SPI Interface	● Works in master mode only ● Max. clock frequency rate: 50 MHz

PCIe Interface	● Complies with *PCI Express Base Specification Revision 2.0* ● Supports 5 Gbps per lane ● Used for data transmission ● RC mode only
eSIM	Optional
Rx-diversity	Supports LTE Rx-diversity
GNSS Features	● Supports GPS, GLONASS, BDS, and Galileo ● Protocol: NMEA 0183 ● Data update rate: 1 Hz
AT Commands	● Complies with *3GPP TS 27.007* and *3GPP TS 27.005* ● Quectel enhanced AT commands
Network Indication	Two pins (NET_MODE and NET_STATUS) indicate network connectivity status
Antenna Interfaces	● ANT [0:1] ● ANT_GNSS ● 50 Ω impedance
Physical Characteristics	● Dimensions: (37.0 ±0.2) mm × (39.5 ±0.2) mm × (2.8 ±0.2) mm ● Package: LGA ● Weight: approx. 9.1 g
Temperature Range	● Operating temperature range: -30 to +75 °C [1] ● Extended temperature range: -40 to +85 °C [2] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	● USB 2.0 ● DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of the module and illustrates the major functional parts.

- Power management
- Baseband
- LPDDR2 SDRAM + NAND flash
- Radio frequency
- Peripheral interfaces

1 To meet this operating temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module can meet 3GPP specifications.
2 To meet this extended temperature range, you need to ensure effective thermal dissipation, for example, by adding passive or active heatsinks, heat pipes, vapor chambers, etc. Within this range, the module remains the ability to establish and maintain functions such as SMS, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.
*FCC LTE Band48(22 dBm ±2 dB) ISED LTE Band48(3550-3650)(22 dBm ±2 dB) ISED LTE Band48(3650-3700)(15 dBm ±2 dB)

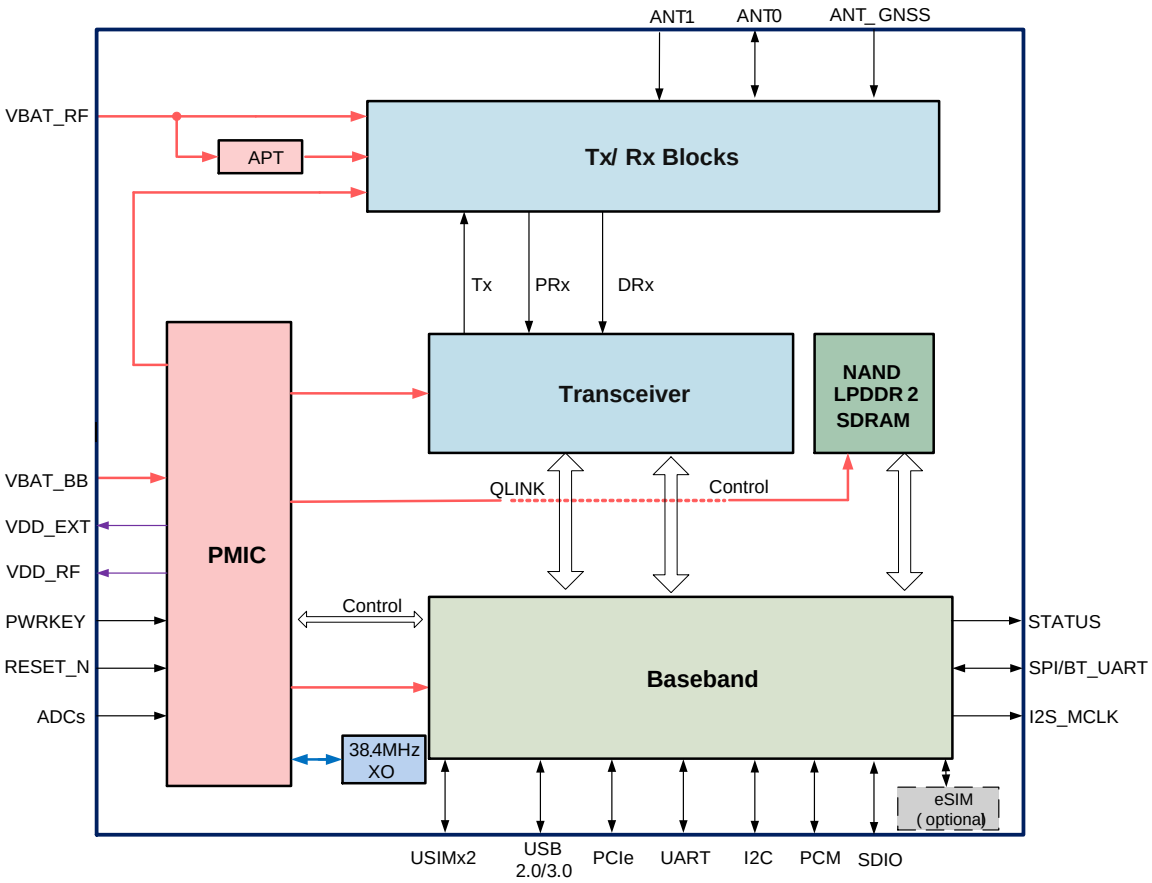


Figure 1: Functional Diagram

2.4. Pin Assignment

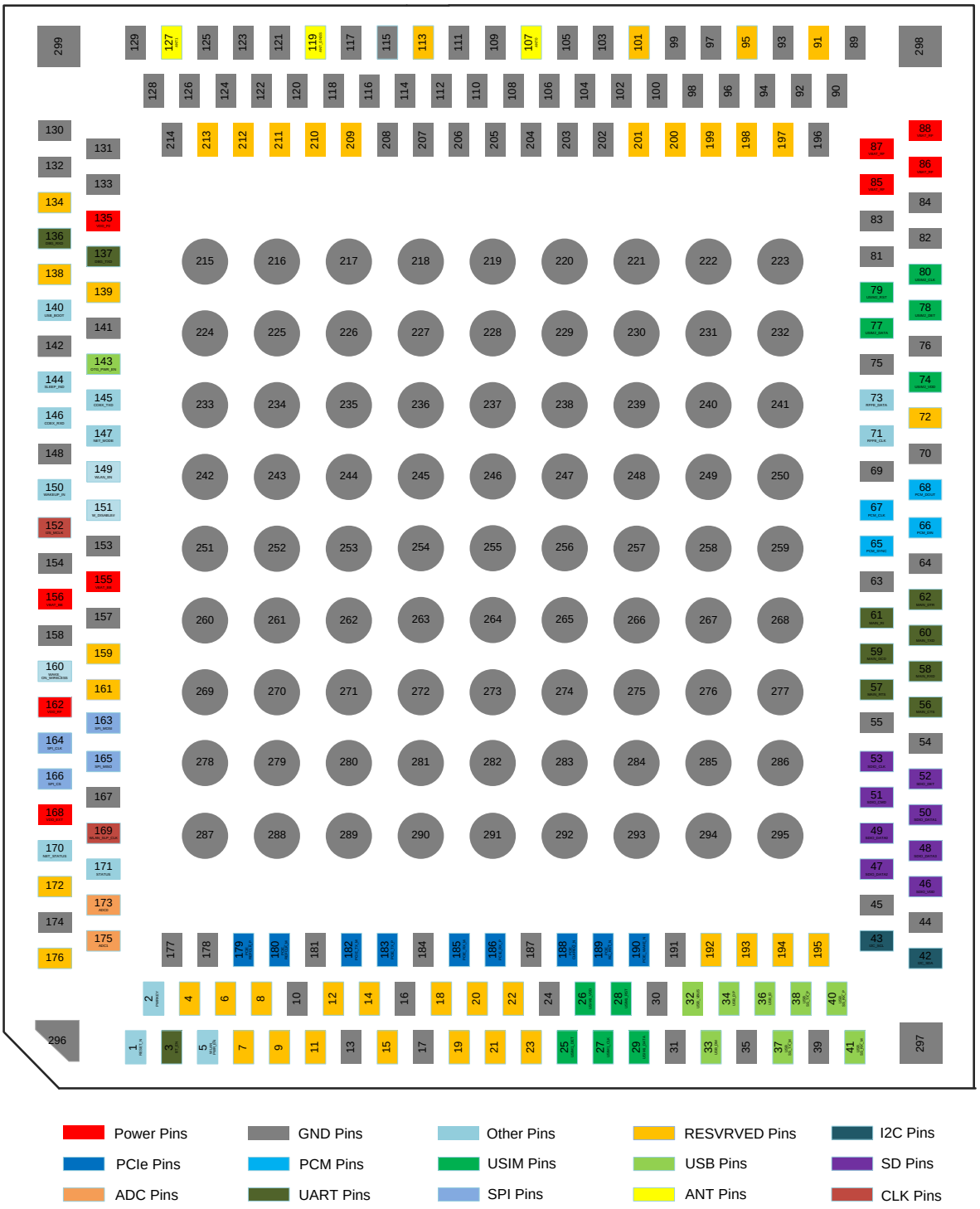


Figure 2: Pin Assignment (Top View)

NOTE

1. Keep all RESERVED pins and unused pins unconnected.
2. GND pins should be connected to ground in the design.

2.5. Pin Description

Table 4: I/O Parameters Definition

Type	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics includes power domain, rate current etc.

Table 5: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	155, 156	PI	Power supply for the module's baseband part.	Vmax = 4.4 V Vmin = 3.3 V Vnom = 3.8 V	Sufficient current up to 1 A is requisite.
VBAT_RF	85–88	PI	Power supply for the module's RF part.		A transmitting burst requires a sufficient current up to 1.5 A.
VDD_EXT	168	PO	Provide 1.8 V for external circuit.	Vnom = 1.8 V $I_O$max = 50 mA	

VDD_RF	162	PO	Provide 2.85 V for external RF circuit.	Vnom = 2.7 V $I_O$max = 120 mA	If unused, keep it open.
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114–118, 120–126, 128–133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202–208, 214–299				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	1	DI	Reset the module	V_{IH}min = 1.17 V V_{IL}max = 0.54 V	Pulled up to 1.8 V internally. Active low.
PWRKEY	2	DI	Turn on/off the module		
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NET_MODE	147	DO	Indicate the module's network registration mode	VDD_EXT	If unused, keep them open.
NET_STATUS	170	DO	Indicate the module's network activity status	VDD_EXT	
STATUS	171	DO	Indicate the module's operation status	VDD_EXT	
SLEEP_IND	144	DO	Indicates the module's sleep indication	VDD_EXT	
USIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_DET	25	DI	USIM1 card hot-plug detect	USIM1_VDD	If unused, keep it open.
USIM1_VDD	26	PO	USIM1 card power supply	**High-voltage:** Vmin = 3.05 V Vnom = 2.85 V Vmax = 2.7 V **Low-Voltage:** Vmin = 1.95 V Vnom = 1.8 V Vmax = 1.65 V	
USIM1_CLK	27	DO	USIM1 card clock	USIM1_VDD	
USIM1_RST	28	DO	USIM1 card reset	USIM1_VDD	
USIM1_DATA	29	DIO	USIM1 card data	USIM1_VDD	
USIM2_VDD	74	PO	USIM2 card power supply	**High-voltage:** Vmin = 3.05 V Vnom = 2.85 V Vmax = 2.7 V	If USIM2 interface is unused, keep it open.

				Low-Voltage: Vmin = 1.95 V Vnom = 1.8 V Vmax = 1.65 V	
USIM2_DATA	77	DIO	USIM2 card data	USIM2_VDD	If USIM2 interface is unused, keep it open.
USIM2_DET	78	DI	USIM2 card hot-plug detect	USIM2_VDD	If USIM2 interface is unused, keep it open.
USIM2_RST	79	DO	USIM2 card reset	USIM2_VDD	If USIM2 interface is unused, keep them open.
USIM2_CLK	80	DO	USIM2 card clock	USIM2_VDD	
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	32	DI	USB connection detect	-	Detection threshold: Vmin = 3.3 V Vnom = 5 V Vmax = 5.25 V
USB_DM	33	AIO	USB 2.0 differential data (-)		Comply with USB 2.0 specifications. Require differential impedance of 90 Ω.
USB_DP	34	AIO	USB 2.0 differential data (+)		
USB_SS_TX_M	37	AO	USB 3.0 super-speed transmit (-)		Comply with USB 3.0 specifications. Require differential impedance of 90 Ω.
USB_SS_TX_P	38	AO	USB 3.0 super-speed transmit (+)		
USB_SS_RX_P	40	AI	USB 3.0 super-speed receive (+)		
USB_SS_RX_M	41	AI	USB 3.0 super-speed receive (-)		
USB_ID*	36	DI	USB ID detect	VDD_EXT	If unused, keep them open.
OTG_PWR_EN*	143	DO	OTG power control	VDD_EXT	
SDIO Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VDD_P2	135	PI	Power input for SDIO interface	-	If a SD card is used, connect VDD_P2 to SDIO_VDD. If unused, connect VDD_P2 to VDD_EXT.
SDIO_VDD	46	PO	**SD card application**: SDIO pull up power source **eMMC* application**: Keep it open as used for eMMC*	**High-voltage:** Vmin = 3.05 V Vnom = 2.85 V Vmax = 2.7 V **Low-Voltage:** Vmin = 1.95 V Vnom = 1.8 V	Cannot work as SD card power supply. SD card must be powered by an external power supply.

				Vmax = 1.65 V	
SDIO_DATA0	49	DIO	SDIO data bit 0	SDIO_VDD	If unused, keep them open.
SDIO_DATA1	50	DIO	SDIO data bit 1		
SDIO_DATA2	47	DIO	SDIO data bit 2		
SDIO_DATA3	48	DIO	SDIO data bit 3		
SDIO_CMD	51	DIO	SDIO command		
SDIO_CLK	53	DO	SDIO clock		
SDIO_DET	52	DI	SD card detect	VDD_EXT	If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_CTS	56	DI	CTS: DTE clear to send signal from DCE	VDD_EXT	Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	57	DO	RTS: DTE request to send signal to DCE	VDD_EXT	Connect to DTE's RTS. If unused, keep it open.
MAIN_RXD	58	DI	Main UART receive	VDD_EXT	If unused, keep this pin open.
MAIN_DCD	59	DO	Main UART data carrier detect	VDD_EXT	
MAIN_TXD	60	DO	Main UART transmit	VDD_EXT	
MAIN_RI	61	DO	Main UART ring indication	VDD_EXT	
MAIN_DTR	62	DI	Main UART data terminal ready	VDD_EXT	Pulled up by default. Pulling low will awaken the module. If unused, keep it open. Sleep mode control.
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	136	DI	Debug UART receive	VDD_EXT	If unused, keep them open.
DBG_TXD	137	DO	Debug UART transmit	VDD_EXT	
SPI Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**

SPI_MOSI	163	DO	SPI master output slave input	VDD_EXT	If unused, keep it open. It can be multiplexed into BT_TXD*.
SPI_CLK	164	DO	SPI clock	VDD_EXT	If unused, keep it open. It can be multiplexed into BT_CTS*.
SPI_MISO	165	DI	SPI master input slave output	VDD_EXT	If unused, keep it open. It can be multiplexed into BT_RXD*.
SPI_CS	166	DO	SPI chip select	VDD_EXT	If unused, keep it open. It can be multiplexed into BT_RTS*.
PCM and I2C Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C_SDA	42	OD	I2C serial data (for an external codec)	VDD_EXT	An external pull-up resistor is requisite. If unused, keep them open.
I2C_SCL	43	OD	I2C serial clock (for an external codec)	VDD_EXT	
PCM_SYNC	65	DIO	PCM data frame sync	VDD_EXT	Output signal in master mode. Input signal in slave mode. If unused, keep it open.
PCM_DIN	66	DI	PCM data input	VDD_EXT	If unused, keep it open.
PCM_CLK	67	DIO	PCM clock	VDD_EXT	Output signal in master mode. Input signal in slave mode. If unused, keep it open.
PCM_DOUT	68	DO	PCM data output	VDD_EXT	If unused, keep it open.
I2S_MCLK	152	DO	Clock output for codec	VDD_EXT	Provide a digital clock output for an external codec. If unused, keep it open.
Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT0	107	AIO	Main antenna interface		50 Ω impedance
ANT1	127	AI	Diversity antenna interface		50 Ω impedance If unused, keep them open.
ANT_GNSS	119	AI	GNSS antenna interface		
WLAN Control Interface*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_PWR_EN	5	DO	WLAN power supply enable	VDD_EXT	If unused, keep them open.

			control		
COEX_TXD	145	DO	LTE/WLAN coexistence transmit	VDD_EXT	
COEX_RXD	146	DI	LTE/WLAN coexistence receive	VDD_EXT	
WLAN_EN	149	DO	WLAN function enable control	VDD_EXT	Active high. If unused, keep it open.
WAKE_ON_WIRELESS	160	DI	Awaken the host (the module) via an external Wi-Fi module	VDD_EXT	Active low. If unused, keep it open.
WLAN_SLP_CLK	169	DO	WLAN sleep clock	VDD_EXT	If unused, keep it open.
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	173	AI	General-purpose ADC interface	0–1.875 V	If unused, keep them open.
ADC1	175	AI			
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	179	AO	PCIe reference clock (+)		Require differential impedance of 95 Ω. If unused, keep them open.
PCIE_REFCLK_M	180	AO	PCIe reference clock (-)		
PCIE_TX_M	182	AO	PCIe transmission (-)		
PCIE_TX_P	183	AO	PCIe transmission (+)		
PCIE_RX_M	185	AI	PCIe receiving (-)		
PCIE_RX_P	186	AI	PCIe receiving (+)		
PCIE_CLKREQ_N	188	DI	PCIe clock request	VDD_EXT	Input signal in master mode. If unused, keep it open.
PCIE_RC_RST_N	189	DO	PCIe RC reset	VDD_EXT	Output signal in master mode. If unused, keep it open.
PCIE_WAKE_N	190	DI	PCIe wake up	VDD_EXT	Input signal, in master mode only. If unused, keep it open.
Antenna Tuner Control Interfaces* (RFFE Interface)					

Pin Name	Pin Name	I/O	Description	DC Characteristics	Comment
RFFE_CLK	71	DO	RFFE serial interface for external tuner control	VDD_EXT	If unused, keep them open.
RFFE_DATA	73	DIO			
Other Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	140	DI	Force the module into emergency download mode	VDD_EXT	Active high If unused, keep it open.
BT_EN*	3	DO	Bluetooth function enable control	VDD_EXT	If unused, keep it open.
WAKEUP_IN	150	DI	Sleep mode control	VDD_EXT	Pulled up by default. Low level awakens the module. If unused, keep it open.
W_DISABLE#	151	DI	Airplane mode control	VDD_EXT	Pulled up by default. In low level, the module will enter airplane mode. If unused, keep it open.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	4, 6–9, 11, 12, 14, 15, 18–23, 72, 91, 95,101,113, 134, 138, 139, 159, 161, 172, 176, 192–195, 197–201, 209–213				Keep these pins unconnected.

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (UMTS & LTE EVB R2.0) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

Table 6: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice/Data	Network is connected. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** command sets the module to minimum functionality without removing the power supply. In this case, both RF function and USIM card are invalid.	
Airplane Mode	**AT+CFUN=4** command or driving W_DISABLE# low will set the module to airplane mode. In this case, the RF function is invalid.	
Sleep Mode	When **AT+QSCLK=1** command is executed and the host's USB bus enters suspend state, the module will enter sleep mode. The module keeps receiving paging messages, SMS and TCP/UDP data from the network with its power consumption reducing to the minimal level.	
Power Down Mode	The power management unit shuts down the power supply. Software is inactive, all application interfaces are inaccessible, and the operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

NOTE

See ***document [2]*** for details about AT commands mentioned above.

3.1.1. Sleep Mode

DRX can reduce the power consumption of the module to the minimum value during sleep mode, and DRX cycle index values are broadcasted by the wireless network. The figure below shows the relationship between the DRX run time and the power consumption in sleep mode. The longer the DRX cycle is, the lower the power consumption will be.

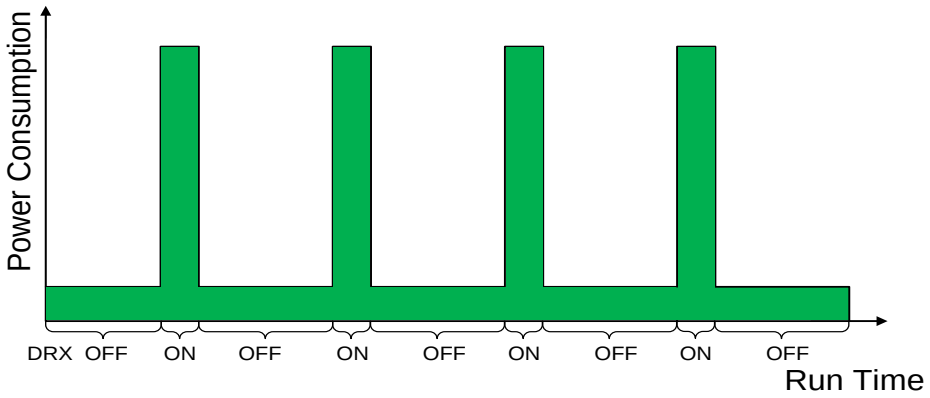


Figure 3: DRX Run Time and Power Consumption in Sleep Mode

The following part of this chapter presents the power saving procedure and sleep mode of the module.

3.1.1.1. UART Application Scenario

If the host communicates with the module via UART interfaces, meeting the following requirements will bring the module into sleep mode.

- Keep MAIN_DTR high (pulled up by default).
- Execute **AT+QSCLK=1**. See ***document [2]*** for details about **AT+QSCLK=1**.

The following figure shows the connection between the module and the host.

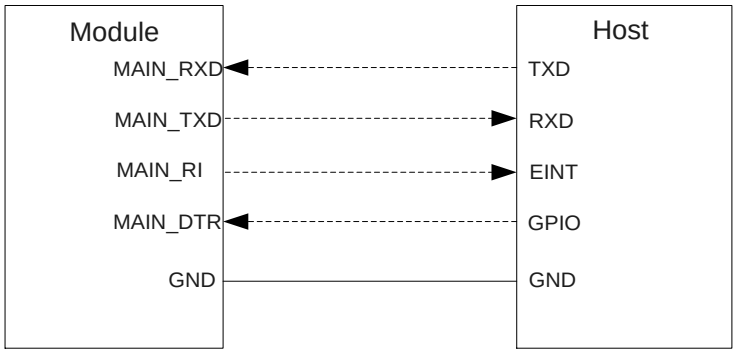


Figure 4: Sleep Mode Application via UART Interfaces

Driving MAIN_DTR low will wake up the module. When the module has a URC to report, MAIN_RI signal will wake up the host. See ***Chapter 4.7.3*** for details about MAIN_RI behavior.

3.1.1.2. USB Application Scenarios

USB application can be applied with USB remote wake-up function or USB suspend/resume and MAIN_RI functions.

- If the host supports USB suspend/resume and remote wake-up function, meeting the following three requirements will bring the module into sleep mode.

  - Keep MAIN_DTR high (pulled up by default).
  - Execute **AT+QSCLK=1** command. See ***document [2]*** for details about **AT+QSCLK=1**.
  - The host's USB bus, connected to the module's USB interface, has entered suspend state.

The following figure shows the above-mentioned connection between the module and the host.

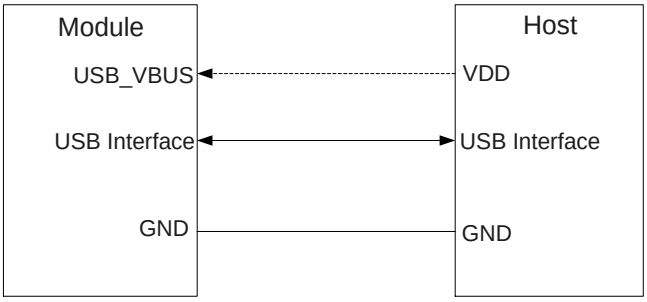


Figure 5: Sleep Mode Application with USB Remote Wake-up

Sending data to the module through USB will wake up the module. When the module has a URC to report, the module will send remote wake-up signals via USB bus to awaken the host.

- If the host supports USB suspend/resume but does not support remote wake-up function, meeting the following three requirements will bring the module into sleep mode.

  - Keep MAIN_DTR high (pulled up by default).
  - Execute **AT+QSCLK=1** command. See ***document [2]*** for details about **AT+QSCLK=1**.
  - The host's USB bus, connected with the module's USB interface, has entered suspend state.

The following figure shows the connection between the module and the host.

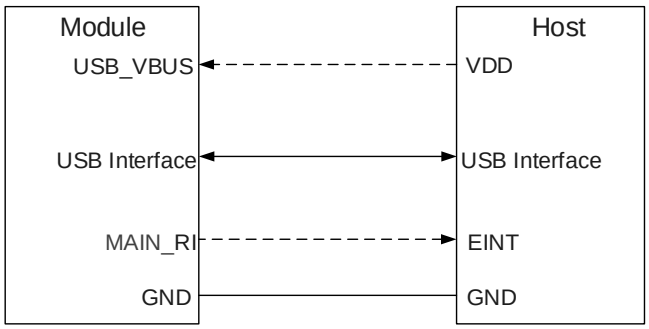


Figure 6: Sleep Mode Application with MAIN_RI

Sending data to the module through USB will awaken the module. When the module has a URC to report, MAIN_RI will wake up the host.

- If the host does not support USB suspend function, USB_VBUS should be disconnected with an external control circuit to bring the module into sleep mode.

  - Keep MAIN_DTR high (pulled up by default).
  - Execute **AT+QSCLK=1** command. See ***document [2]*** for details about **AT+QSCLK=1**.
  - Disconnect USB_VBUS.

The following figure shows the above-mentioned connection between the module and the host.

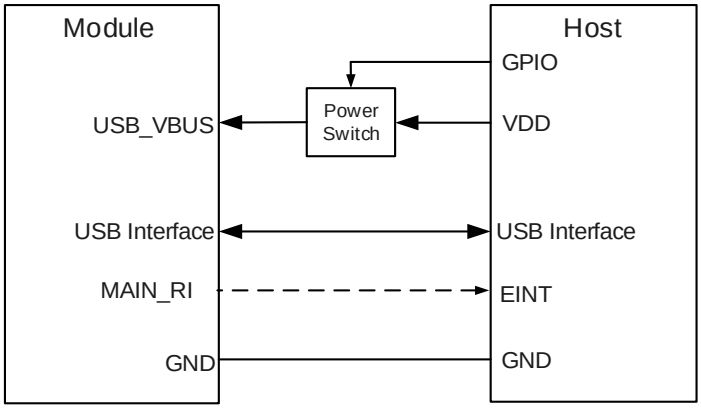


Figure 7: Sleep Mode Application without Suspend Function

To awaken the module, power USB_VBUS by turning on the power switch.

NOTE

Please heed the level-shifting of the connection shown in dotted line between the module and the host.

3.1.2. Airplane Mode

The module provides W_DISABLE# to disable or enable airplane mode via hardware operation. W_DISABLE# is pulled up by default. Driving it low will bring the module into airplane mode.

Table 7: Pin Description of W_DISABLE#

Pin Name	Pin No.	I/O	Description	Comment
W_DISABLE#	151	DI	Airplane mode control	Pulled up by default. In low level, the module will enter airplane mode. If unused, keep it open.

In airplane mode, the RF function is disabled by default, but it can also be enabled or disabled through AT commands. The following table shows the RF function status of the module.

Table 8: RF Function Status

W_DISABLE# Logic Level	AT Command	RF Function Status	Operating Modes
High Level	**AT+CFUN=1**	Enabled	Full functionality
	AT+CFUN=0	Disabled	Minimum functionality
	AT+CFUN=4	Disabled	Airplane mode
Low Level	**AT+CFUN=0** **AT+CFUN=1** **AT+CFUN=4**	Disabled	Airplane mode

NOTE

1. W_DISABLE# for airplane mode control function is disabled by default. It can be enabled through
2. The execution of **AT+CFUN** command will not affect GNSS function. See ***document [2]*** for details about the AT command.

3.2. Power Supply

3.2.1. Power Supply Pins

The module provides six VBAT pins dedicated to the connection to an external power supply. There are two separate voltage domains for VBAT.

Table 9: Pin Description of VBAT and GND Pins

Pin Name	Pin No.	I/O	Description	Min.	Typ.	Max.	Unit
VBAT_RF	85–88	PI	Power supply for the module's RF part	3.3	3.8	4.4	V
VBAT_BB	155, 156	PI	Power supply for the module's baseband part	3.3	3.8	4.4	V
GND	10, 13, 16, 17, 24, 30, 31, 35, 39, 44, 45, 54, 55, 63, 64, 69, 70, 75, 76, 81–84, 89, 90, 92–94, 96–100, 102–106, 108–112, 114–118, 120–126, 128-133, 141, 142, 148, 153, 154, 157, 158, 167, 174, 177, 178, 181, 184, 187, 191, 196, 202–208, 214–299						

The power supply of the module ranges from 3.3 V to 4.4 V. Make sure the input voltage never drops below 3.3 V, otherwise the module will be powered off automatically. The following figure shows the voltage drop during Tx power in 3G/4G networks.

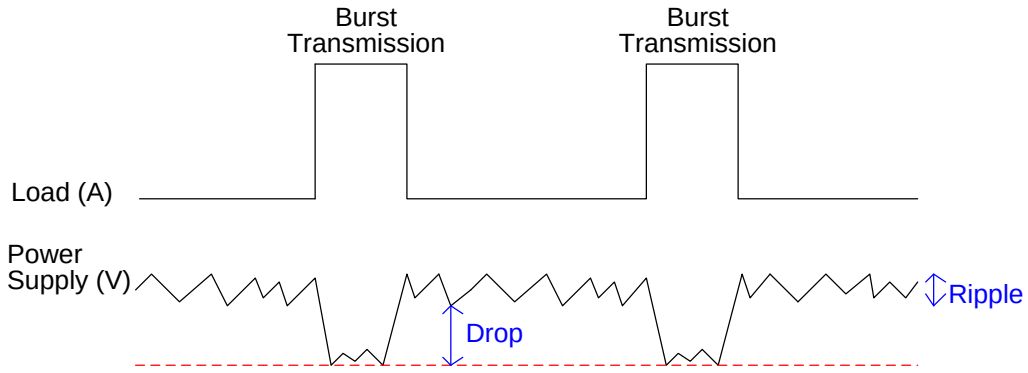


Figure 8: Power Supply Limits during Burst Transmission

To decrease voltage drop, bypass capacitors of about 100 μF with low ESR and one multilayer ceramic chip (MLCC) capacitor array with ultra-low ESR should be used for VBAT_BB/RF. It is recommended to use 4 ceramic capacitors (100 nF, 6.8 nF, 220 pF, 68 pF) for composing the MLCC array for VABT_BB and 6 ceramic capacitors (100 nF, 220 pF, 68 pF, 15 pF, 9.1 pF, 4.7 pF) for composing the MLCC array for VABT_RF, and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source which can supply power along two sub paths with star topology. The width of VBAT_BB trace should be no less than 1 mm. The width of VBAT_RF trace should be no less than 2 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, for stable power supply, it is necessary to add a high-power TVS near VBAT_BB and VBAT_RF. The star topology of the power supply is shown below.

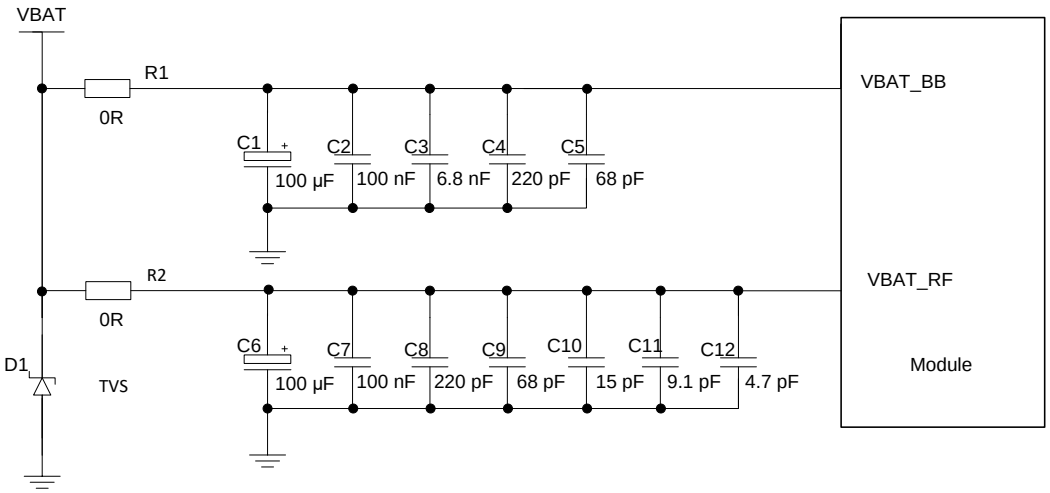


Figure 9: Star Topology of the Power Supply

3.2.2. Reference Design for Power Supply

The power design for the module is vital as the performance of the module largely relies on the power source. The power supply of the module should be able to provide a sufficient current of at least 2 A. If the voltage drop between the input and output is not too high, powering the module with an LDO is recommended. If a big voltage difference exists between the input source and the desired output (VBAT), a buck DC-DC converter is preferred.

The following figure shows a reference design for +5 V input power source. In this design, the typical power supply output is about 3.8 V and the maximum load current is 3 A.

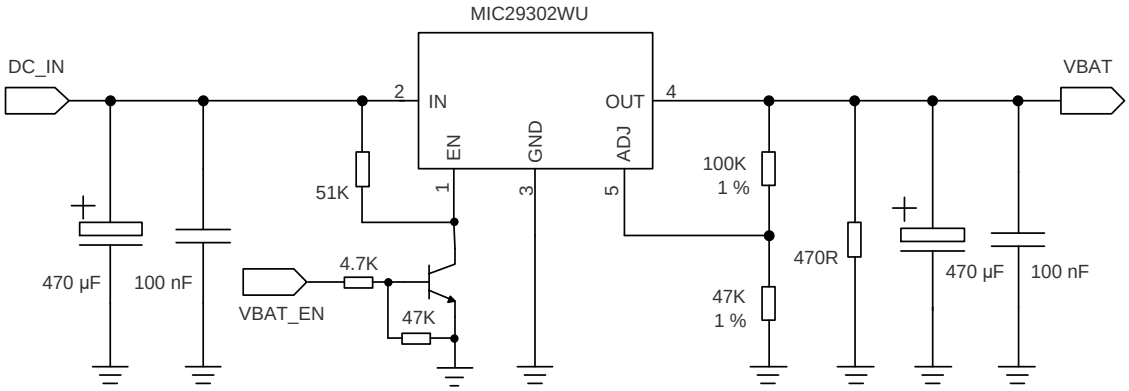


Figure 10: Reference Circuit of the Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off power supply when the module works normally. Only after the module is shut down with PWRKEY or AT command can you cut off the power

supply.

3.2.3. Power Supply Voltage Monitoring

AT+CBC command can be used to monitor the VBAT_BB voltage value. See ***document [2]*** for details.

3.3. Turn On

The module can be turned on via PWRKEY.

Table 10: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	2	DI	Turn on/off the module	Pulled-up internally. Active low.

When the module is in turn-off mode, it can be turned on by driving PWRKEY low for at least 500 ms. It is recommended to control PWRKEY with an open drain/collector driver. After STATUS outputs a high level, PWRKEY can be released. A simple reference circuit is given below.

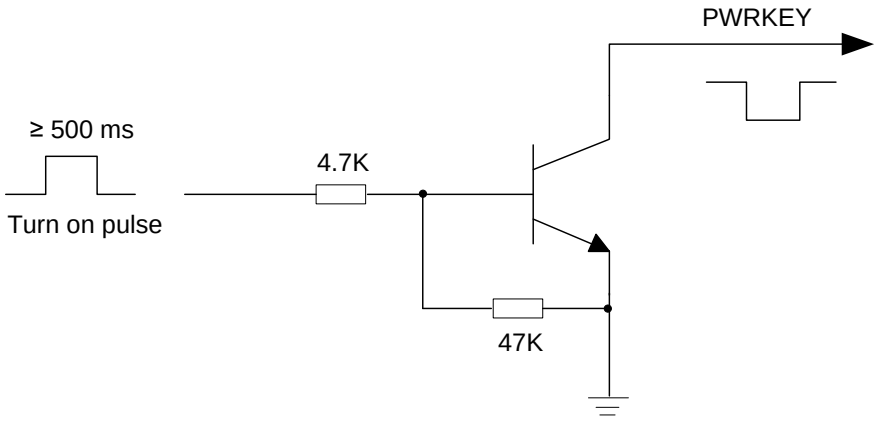


Figure 11: Turn On with a Driving Circuit

The other way to control PWRKEY is with a button. Pressing the button may result in a discharge of static electricity from your fingers. Therefore, it is necessary to place a TVS close to the button for ESD protection. A reference circuit is shown in the following figure.

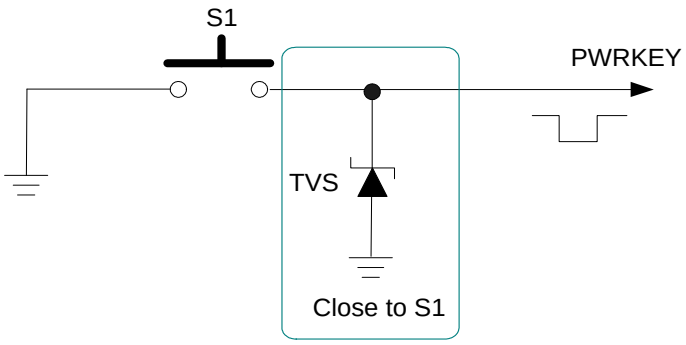


Figure 12: Turn On With a Button

The turn-on scenario is illustrated in the following figure.

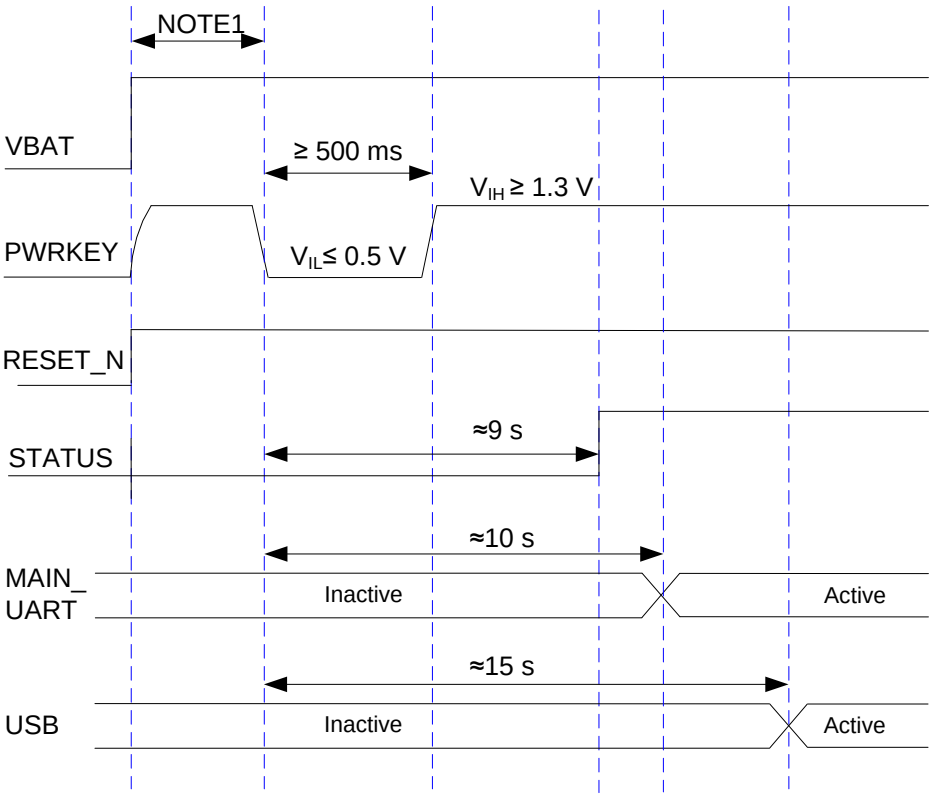


Figure 13: Turn On Timing

NOTE

1. Make sure VBAT is stable for over 30 ms before pulling down PWRKEY.
2. If the module needs to be turned on automatically and turn-off is not needed, PWRKEY can be pulled down directly to GND with a recommended 10 kΩ resistor.
3. Make sure there is no large capacitance on PWRKEY and RESET_N pins.

3.4. Turn Off

The module can be turned off normally via two methods: using PWRKEY or executing **AT+QPOWD**.

3.4.1. Turn Off with PWRKEY

Driving PWRKEY low for at least 800 ms, the module will execute the power-down procedure after PWRKEY is released. The turn-off scenario is illustrated in the following figure.

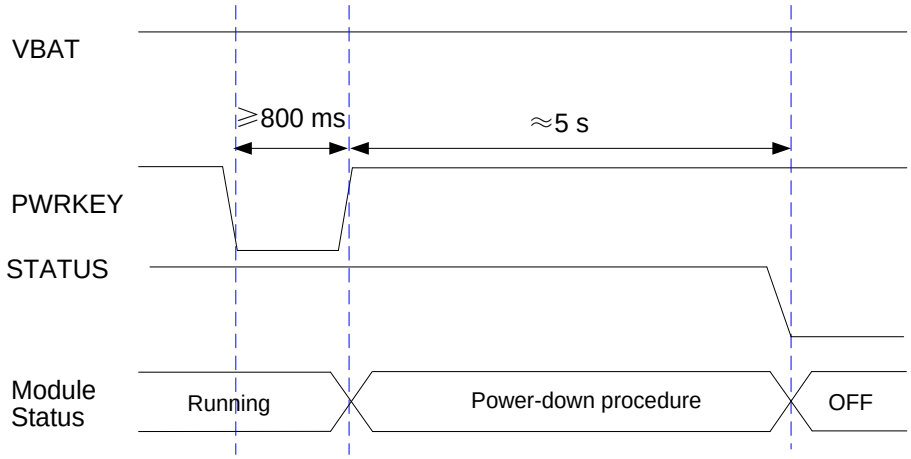


Figure 14: Turning-off Timing

3.4.2. Turn Off with AT Command

It is also a safe manner to turn off the module via **AT+QPOWD**. When turning off module with the AT command, keep PWRKEY at high level after the execution of the command. Otherwise the module will be turned on again after a successfully turn-off. See ***document [2]*** for details about the AT command.

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. The power supply can only be cut off after the module is shut down by PWRKEY or the AT command.

3.5. Reset

The module can be reset by driving RESET_N low for 250-600 ms and then releasing it.

Table 11: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	1	DI	Reset the module	Pulled up internally. Active low.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver can control RESET_N.

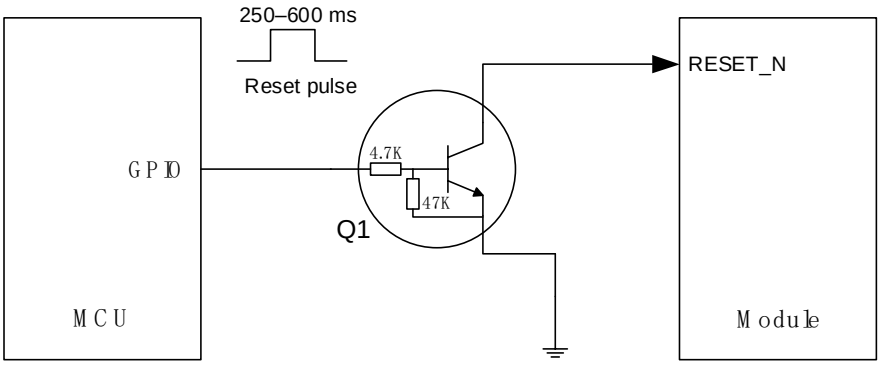


Figure 15: Reference Circuit of RESET_N with a Driving Circuit

The reset scenario is illustrated in the following figure.

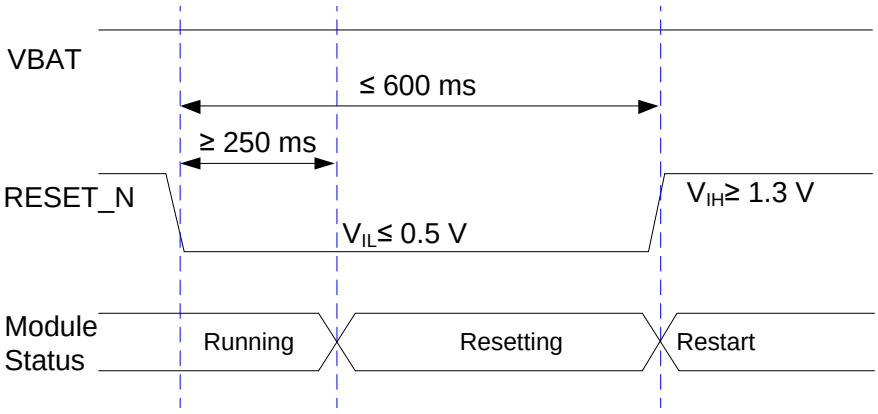


Figure 16: Reset Timing

NOTE

1. Reset the module with RESET_N only when it fails to be turned off with **AT+QPOWD** or PWRKEY. See ***document [2]*** for details about the AT command.
2. Make sure no large capacitance exists on PWRKEY and RESET_N pins.

4 Application Interfaces

4.1. USIM Interfaces

The module provides two USIM interfaces. The circuitry of USIM interfaces meets ETSI and IMT-2000 requirements. The interfaces support both 1.8 V and 3.0 V USIM cards and Dual USIM Single Standby function. USIM card hot-swap is enabled by **AT+QSIMDET**. See ***document [2]*** for details about the AT command.

Table 12: Pin Description of USIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_DET	25	DI	USIM1 card hot-plug detect	If unused, keep it open.
USIM1_VDD	26	PO	USIM1 card power supply	
USIM1_CLK	27	DO	USIM1 card clock	
USIM1_RST	28	DO	USIM1 card reset	
USIM1_DATA	29	DIO	USIM1 card data	
USIM2_VDD	74	PO	USIM2 card power supply	If USIM2 interface is unused, keep it open.
USIM2_DATA	77	DIO	USIM2 card data	If USIM2 interface is unused, keep it open.
USIM2_DET	78	DI	USIM2 card hot-plug detect	If USIM2 interface is unused, keep it open.
USIM2_RST	79	DO	USIM2 card reset	If USIM2 interface is unused, keep them open.
USIM2_CLK	80	DO	USIM2 card clock	

The module supports USIM card hot-plug via USIM_DET pins, and both high and low level detections. The function is disabled by default. See **AT+QSIMDET** in ***document [2]*** for more details.

The following figure shows a reference design for a USIM interface with an 8-pin USIM card connector.

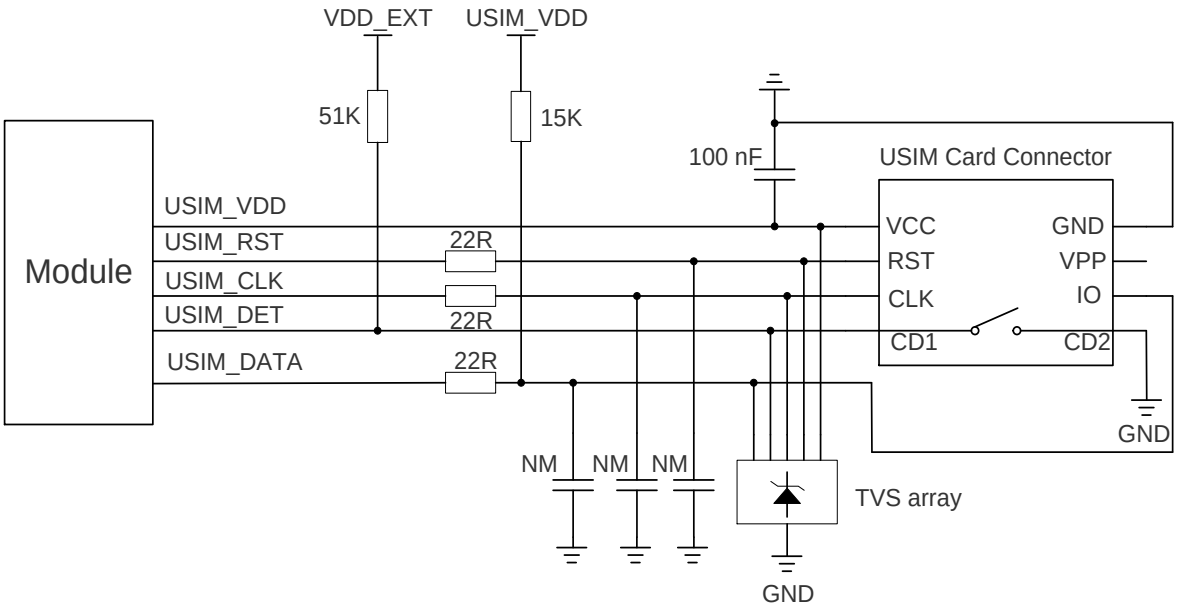


Figure 17: Reference Circuit of a USIM Interface with an 8-Pin USIM Card Connector

If USIM card detection function is unnecessary, keep USIM_DET open. A reference circuit for a USIM interface with a 6-pin USIM card connector is illustrated in the following figure.

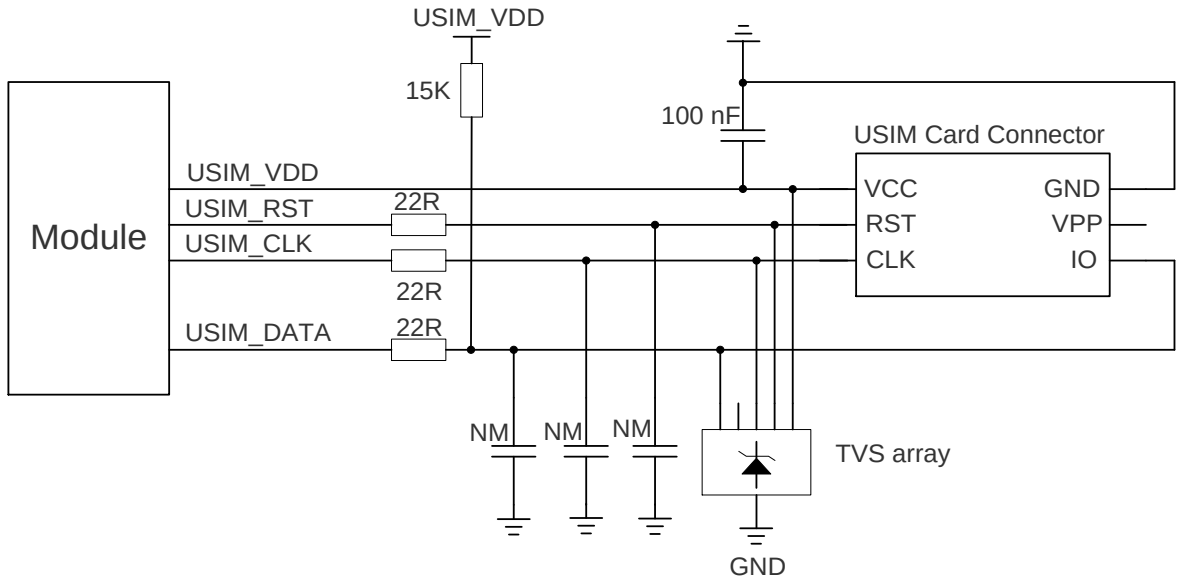


Figure 18: Reference Circuit of a USIM Interface with a 6-Pin USIM Card Connector

For better reliability and availability of the USIM card in applications, follow the criteria below in the USIM circuit design:

- Put the USIM card connector as close as possible to the module with a trace as short as possible, 200 mm at most.

- Keep USIM card signals away from RF and VBAT traces.
- Make sure the ground between the module and the USIM card connector is short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep their traces away from each other and shield them with ground.
- For better ESD protection, it is recommended to add a TVS array of which parasitic capacitance should be less than 50 pF. 22 Ω resistors should be added in series between the module and the USIM card connector to suppress the EMI spurious transmission and enhance the ESD protection. The USIM peripheral circuit should be close to the USIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability, and it should be close to the USIM card connector.

4.2. USB Interface

The module provides one integrated USB (Universal Serial Bus) interface which complies with the USB 3.0 and 2.0 specifications and supports SuperSpeed (5 Gbps) mode on USB 3.0 and high-speed(480 Mbps) and full-speed (12 Mbps) modes on USB 2.0. The USB interface is used for AT command communication, data transmission, GNSS NMEA sentence output, software debugging, firmware upgrade.

Table 13: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	32	DI	USB connection detect	Typical 5.0 V
USB_DP	34	AIO	USB 2.0 differential data (+)	Comply with USB 2.0 specifications. Require differential impedance of 90 Ω.
USB_DM	33	AIO	USB 2.0 differential data (-)	
USB_SS_TX_M	37	AO	USB 3.0 super-speed transmit (-)	Comply with USB 3.0 specifications. Require differential impedance of 90 Ω.
USB_SS_TX_P	38	AO	USB 3.0 super-speed transmit (+)	
USB_SS_RX_P	40	AI	USB 3.0 super-speed receive (+)	
USB_SS_RX_M	41	AI	USB 3.0 super-speed receive (-)	
USB_ID*	36	DI	USB ID detect	If unused, keep them open.
OTG_PWR_EN*	143	DO	OTG power control	

For more details about the USB 2.0 and USB 3.0 specifications, visit http://www.usb.org/home.

The USB interface is recommended to be reserved for firmware upgrade in your designs. The following figure shows a reference circuit of USB 2.0 and USB 3.0 interfaces.

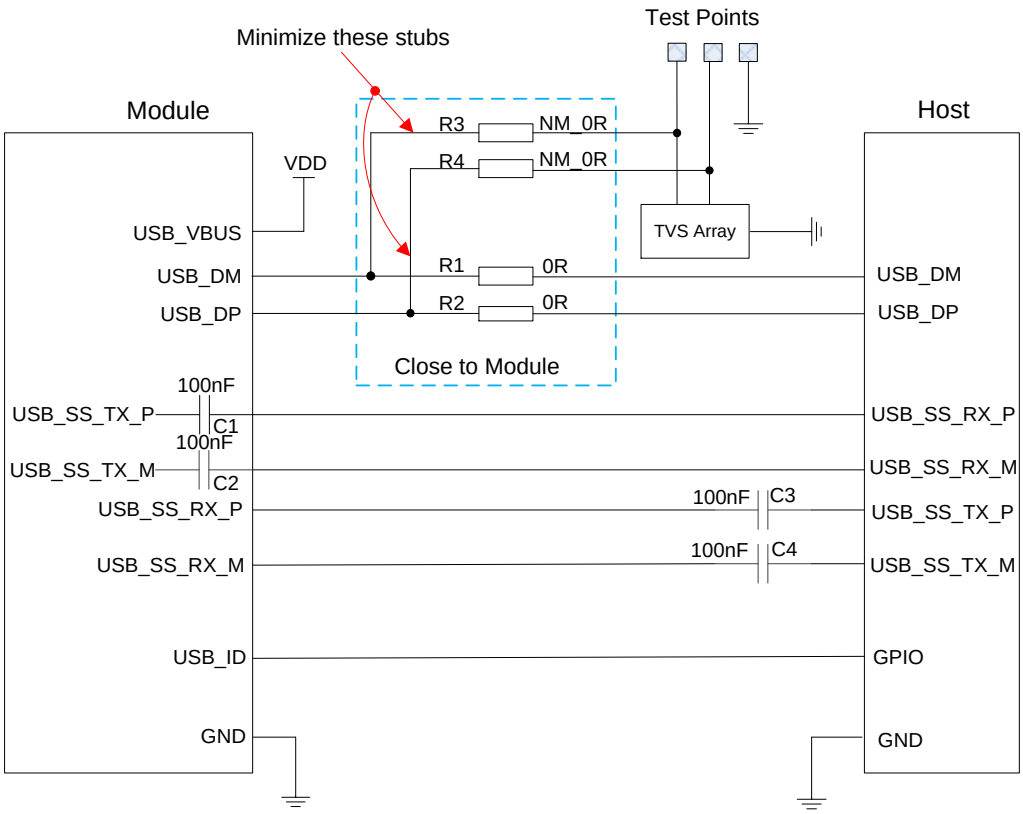


Figure 19: Reference Circuit of USB Application

To ensure the signal integrity of USB data traces, C1 and C2 have already been integrated in the module; C3 and C4 must be placed close to the host; and R1 to R4 should be placed close to each other. The extra stubs of trace must be as short as possible.

The following principles of USB interface should be followed during USB interface design to meet USB 2.0 and USB 3.0 specifications.

- Route the USB 2.0 and USB 3.0 signal traces as differential pairs with ground. The impedance of USB differential trace is 90 Ω.
- For USB 2.0 signal traces, the trace should be shorter than 120 mm, and the differential data pair matching should be less than 2 mm. For USB 3.0 signal traces, the maximum length of each differential data pair (Tx/Rx) is recommended to be less than 100 mm, and each differential data pair matching should be less than 0.7 mm. While the matching between Tx and Rx should be less than 15.24 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. It is vital to route the USB differential traces in inner-layers of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- If a USB connector is used, keep the ESD protection components as close to the USB connector as

possible.

- Junction capacitance of the ESD protection components might influence USB data traces, so pay attention to the selection of the components. Typically, the stray capacitance should be less than 2.0 pF for USB 2.0, and less than 0.4 pF for USB 3.0.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces respectively.

Table 14: USB Trace Length Inside the Module

Pin No.	Signal Trace	Length (mm)	Length Difference
34	USB_DP	16.02	0.32
33	USB_DM	16.34	
37	USB_SS_TX_M	20.57	0.36
38	USB_SS_TX_P	20.21	
40	USB_SS_RX_P	19.62	0.16
41	USB_SS_RX_M	19.46	

4.3. UART Interfaces

The module provides three UART interfaces: one main UART interface, one debug UART interface, and one Bluetooth UART interface* (multiplexed from SPI interface). Features of these interfaces are shown as below:

- Main UART interface supports 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps (default), 230400 bps, 460800 bps and 921600 bps baud rates. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 115200 bps baud rate. It is used for Linux console and log output.
- Bluetooth UART interface* supports 115200 bps baud rate. It is used for Bluetooth communication and it is multiplexed from SPI interface.

4.3.1. Main UART Interface

Table 15: Pin Description of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment

MAIN_CTS	56	DO	CTS: DTE clear to send signal from DCE	CTS: Connect to DTE's CTS. If unused, keep it open.
MAIN_RTS	57	DI	RTS: DTE request to send signal to DCE	RTS: Connect to DTE's RTS. If unused, keep it open.
MAIN_RXD	58	DI	Main UART receive	If unused, keep them open.
MAIN_DCD	59	DO	Main UART data carrier detect	
MAIN_TXD	60	DO	Main UART transmit	
MAIN_RI	61	DO	Main UART ring indication	
MAIN_DTR	62	DI	Main UART data terminal ready	Pulled up by default. Pulling it low will awaken the module. If unused, keep it open. Sleep mode control.

4.3.2. Debug UART Interface

Table 16: Pin Description of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	136	DI	Debug UART receive	If unused, keep them open.
DBG_TXD	137	DO	Debug UART transmit	

4.3.3. Bluetooth UART Interface*

The module provides one Bluetooth UART interface multiplexed from SPI interface.

Table 17: Pin Description of Bluetooth UART Interface

Pin Name	Pin No.	Multiplexed Function	I/O	Description	Comment
BT_EN	3	-	DO	Bluetooth function enable control	If unused, keep them open.
SPI_MOSI	163	BT_TXD	DO	Bluetooth UART transmit	
SPI_CLK	164	BT_CTS	DI	CTS: DTE clear to send signal from DCE	CTS: Connect to DTE's CTS. If unused, keep it open.
SPI_MISO	165	BT_RXD	DI	Bluetooth UART receive	If unused, keep it open.
SPI_CS	166	BT_RTS	DO	RTS: DTE request to send signal to DCE	RTS: Connect to DTE's RTS. If unused, keep it open.

4.3.4. UART Application

The module provides 1.8 V UART interfaces. A level-shifting circuit should be used if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended. The following figure shows a reference design.

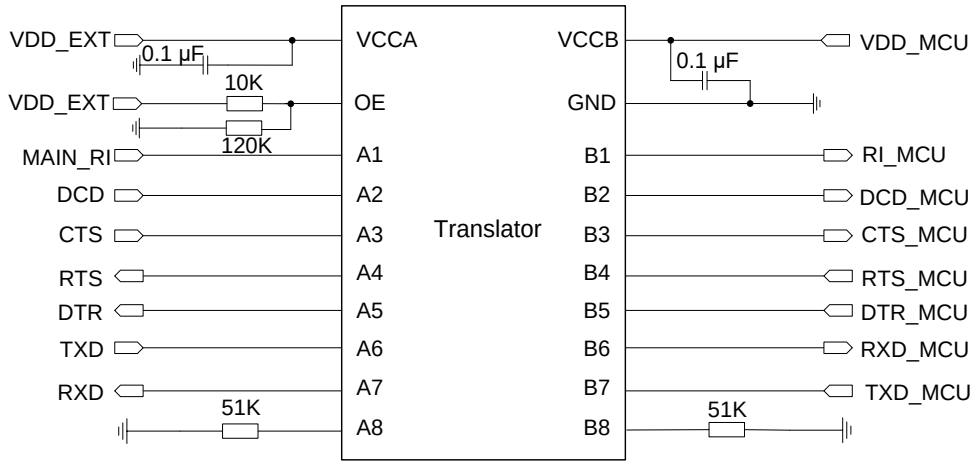


Figure 20: Reference Circuit (IC Solution)

Please visit http://www.ti.com for more information.

Another example with a transistor circuit is shown below. For the design of circuits shown in dotted lines, refer to that shown in solid lines, but pay attention to the direction of the connection.

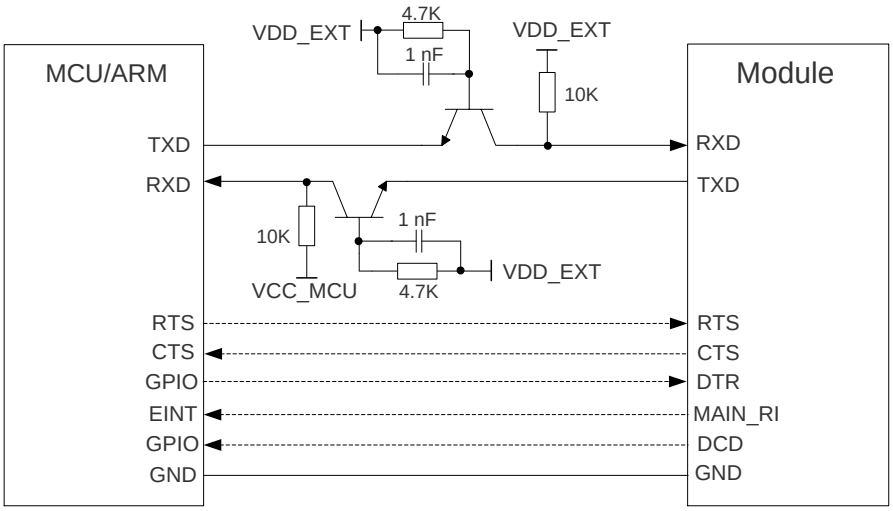


Figure 21: Reference Circuit (Transistor Solution)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates over 460 kbps.
2. Please note that the module CTS is connected to the host CTS, and the module RTS is connected to the host RTS.

4.4. SPI Interface

The module provides one SPI interface which only supports master mode with a maximum clock frequency up to 50 MHz.

Table 18: Pin Description of SPI Interface

Pin Name	Pin No.	I/O	Description	Comment
SPI_MOSI	163	DO	SPI master output slave input	Master only.
SPI_CLK	164	DO	SPI clock	
SPI_MISO	165	DI	SPI master input slave output	
SPI_CS	166	DO	SPI chip select	

The following figure shows a reference design of PCM and SPI interfaces with an external SLIC IC. The dotted line in figure below means an optional connection since some SLIC ICs need RST while some do not.

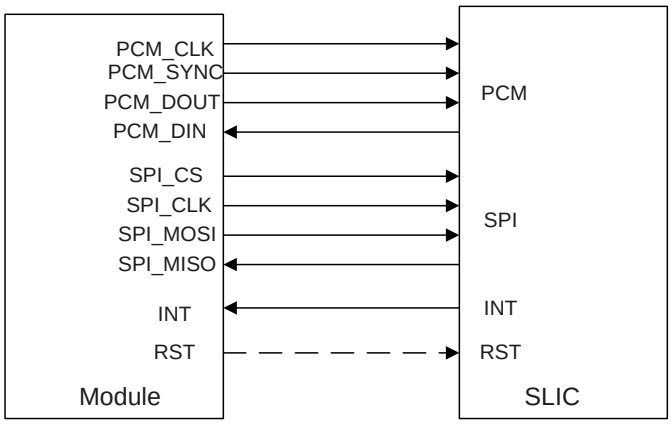


Figure 22: Reference Circuit of PCM and SPI Application with SLIC

4.5. PCM and I2C Interfaces

The module supports audio communication via PCM (Pulse Code Modulation) digital interface and I2C interfaces. Besides, the two interfaces can be applied to audio codec and SLIC designs.

Table 19: Pin Description of PCM and I2C Interfaces

Pin Name	Pin No.	I/O	Description	Comment
PCM_DIN	66	DI	PCM data input	If unused, keep them open.
PCM_DOUT	68	DO	PCM data output	
PCM_SYNC	65	DIO	PCM data frame sync	Output signal in master mode. Input signal in slave mode. If unused, keep them open.
PCM_CLK	67	DIO	PCM clock	
I2C_SDA	42	OD	I2C serial data	An external pull-up resistor is requisite. If unused, keep them open.
I2C_SCL	43	OD	I2C serial clock	
I2S_MCLK	152	DO	Clock output for codec	Provide a digital clock output for an external audio codec. If unused, keep it open. Master only.

The PCM interface supports the following modes:

- Primary mode (short frame synchronization): the module works as both master and slave.
- Auxiliary mode (long frame synchronization): the module works as master only.

In primary mode, the data is sampled on the falling edge of PCM_CLK and transmitted on the rising edge. The falling edge of PCM_SYNC represents the MSB. In this mode, the PCM interface supports 256 kHz, 512 kHz, 1024 kHz or 2048 kHz PCM_CLK at 8 kHz PCM_SYNC, and 4096 kHz PCM_CLK at 16 kHz PCM_SYNC.

In auxiliary mode, the data is sampled on the falling edge of the PCM_CLK and transmitted on the rising edge. The rising edge of PCM_SYNC represents the MSB. In this mode, the PCM interface operates with 256 kHz PCM_CLK and 8 kHz, 50 % duty cycle PCM_SYNC only.

The module supports 16-bit linear data format. The following figures show the primary mode's timing relationship with 8 kHz PCM_SYNC and 2048 kHz PCM_CLK, as well as the auxiliary mode's timing relationship with 8 kHz PCM_SYNC and 256 kHz PCM_CLK.

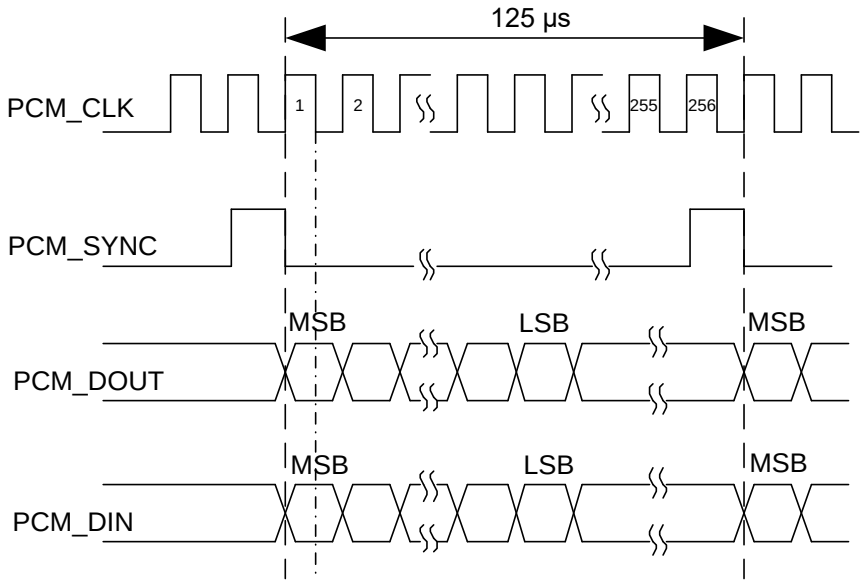


Figure 23: Primary Mode Timing

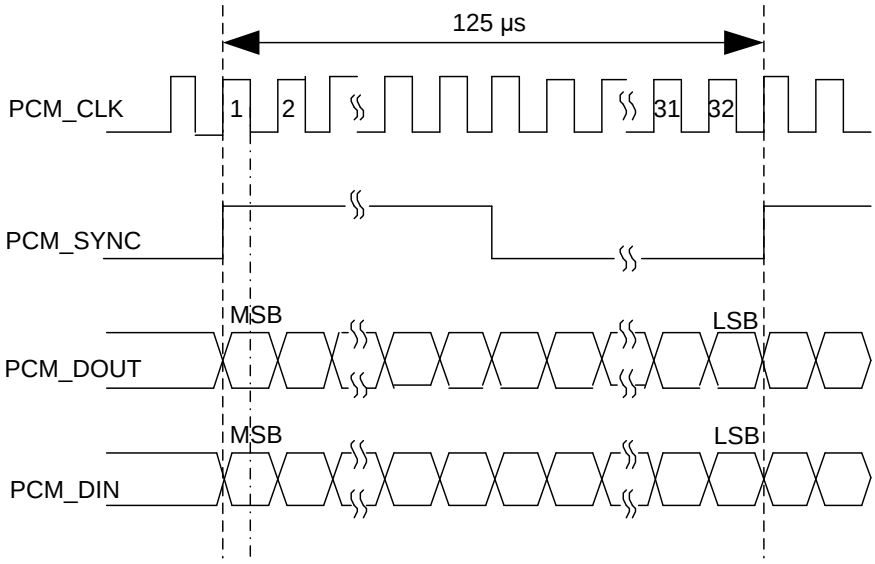


Figure 24: Auxiliary Mode Timing

The PCM clock and primary/auxiliary mode can be configured by **AT+QDAI**, and the default configuration is master mode using short frame synchronization format with 2048 kHz PCM_CLK and 8 kHz PCM_SYNC. See ***document [2]*** for details about the AT command.

The following figure shows a reference design of PCM and I2C interfaces with an external codec IC.

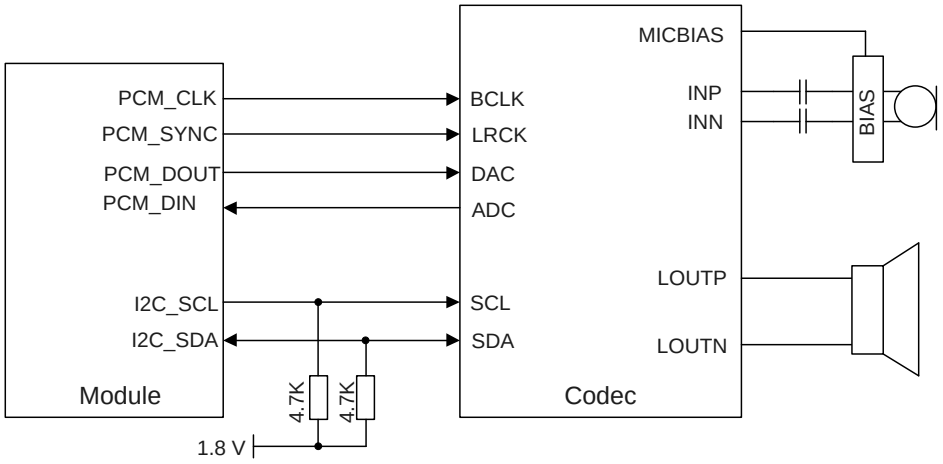


Figure 25: Reference Circuit of PCM and I2C Application with Audio Codec

NOTE

The module works as a master device pertaining to I2C interface.

4.6. ADC Interfaces

The module provides two ADC (Analog-to-Digital Converter) interfaces. Execute **AT+QADC=0** to read the voltage value on ADC0. Execute **AT+QADC=1** to read the voltage value on ADC1. See ***document [2]*** for details about these AT commands.

For higher accuracy of ADC, the trace of ADC should be shielded with ground.

Table 20: Pin Description of the ADC Interfaces

Pin Name	I/O	Pin No.	Description	Comment
ADC0	AI	173	General-purpose ADC interface	0–1.875 V. If unused, keep them open.
ADC1	AI	175		

Table 21: Characteristics of ADC Interfaces

Parameter	Min.	Typ.	Max.	Unit
ADC0 Voltage Range	0	-	1.875	V
ADC1 Voltage Range	0	-	1.875	V
ADC Resolution	-	14	-	bits

NOTE

1. The input voltage of ADC should not exceed 1.875 V.
2. It is prohibited to supply any voltage to ADC pins without VBAT.
3. It is recommended to use a resistor divider circuit for ADC application.

4.7. Indication Signals

4.7.1. Network Status Indication

The network indication pins NET_MODE and NET_STATUS can be used to drive network status indication LEDs. Their definitions and logic level changes upon the switch of network mode/status, which is described in the following tables.

Table 22: Pin Description of NET_MODE and NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	147	DO	Indicate the module's network registration mode.	If unused, keep them open.
NET_STATUS	170	DO	Indicate the module's network activity status.	

Table 23: Working Status of NET_MODE and NET_STATUS

Pin Name	Status	Description
NET_MODE	Always High	Registered on network
	Always Low	Others
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle

	Flicker quickly (125 ms High/125 ms Low)	Data transfer ongoing

A reference circuit is shown in the following figure.

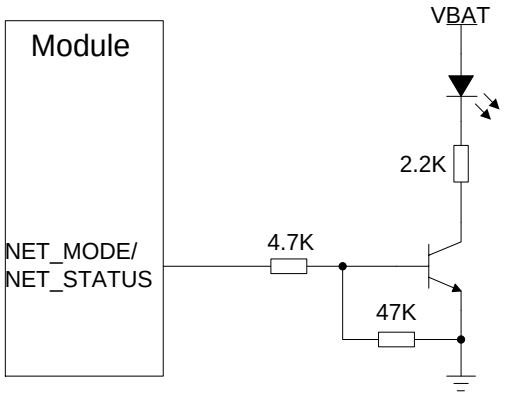


Figure 26: Reference Circuit of the NET_MODE and NET_STATUS

4.7.2. Module Status Indication

The STATUS pin is set as the module's status indicator. It outputs high level voltage when the module is turned on.

Table 24: Pin Description of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	171	DO	Indicate the module's operation status	If unused, keep it open.

A reference circuit is shown as below.

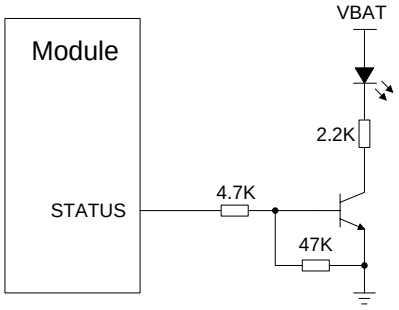


Figure 27: Reference Circuits of STATUS

4.7.3. MAIN_RI

Execute **AT+QCFG="risignaltype","physical"** command to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI. The behavior of MAIN_RI can be altered by executing **AT+QCFG="urc/ri/ring"** command.

In addition, MAIN_RI behavior can be configured flexibly. The default behavior of the MAIN_RI is shown as below.

Table 25: Default Behavior of MAIN_RI

State	Response
Idle	MAIN_RI keeps at high level.
URC	MAIN_RI outputs low pulse for 120 ms when a new URC returns.

NOTE

The URC can be output from UART interface, USB AT port (by default) and USB modem port by executing **AT+QURCCFG**. See ***document [2]*** for details about the AT command.

4.8. PCIe Interface

The module provides one integrated PCIe (Peripheral Component Interconnect Express) interface which can transmit data. The module supports PCIe Root Complex (RC) mode only.

- *PCI Express Base Specification Revision 2.0* compliant
- Data rate up to 5 Gbps/lane
- Can be connected to an external Ethernet IC (MAC and PHY) or WLAN IC

Table 26: Pin Description of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	179	AO	PCIe reference clock (+)	Require differential impedance of 95 Ω.

PCIE_REFCLK_M	180	AO	PCIe reference clock (-)	If unused, keep them open.
PCIE_TX_M	182	AO	PCIe transmit (-)	
PCIE_TX_P	183	AO	PCIe transmit (+)	
PCIE_RX_M	185	AI	PCIe receive (-)	
PCIE_RX_P	186	AI	PCIe receive (+)	
PCIE_CLKREQ_N	188	DI	PCIe clock request	Input signal in master mode. If unused, keep it open.
PCIE_RC_RST_N	189	DO	PCIe RC reset	Output signal in master mode. If unused, keep it open.
PCIE_WAKE_N	190	DI	PCIe wake up	Input signal, in master mode only. If unused, keep it open.

To enhance the reliability and availability in applications, follow the criteria below in the PCIe interface circuit design:

- Keep the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and clock signals.
- Add a capacitor in series on Rx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length matching of each differential data pair (Tx/Rx/REFCLK) less than 0.7 mm for PCIe routing traces.
- Keep the differential impedance of PCIe data trace as 85 Ω ±10 %.
- Do not route PCIe data traces under components or cross them with other traces.

The module only supports RC mode. In this mode, the module is configured to act as a PCIe RC device. The following figure shows a reference circuit of PCIe RC mode.

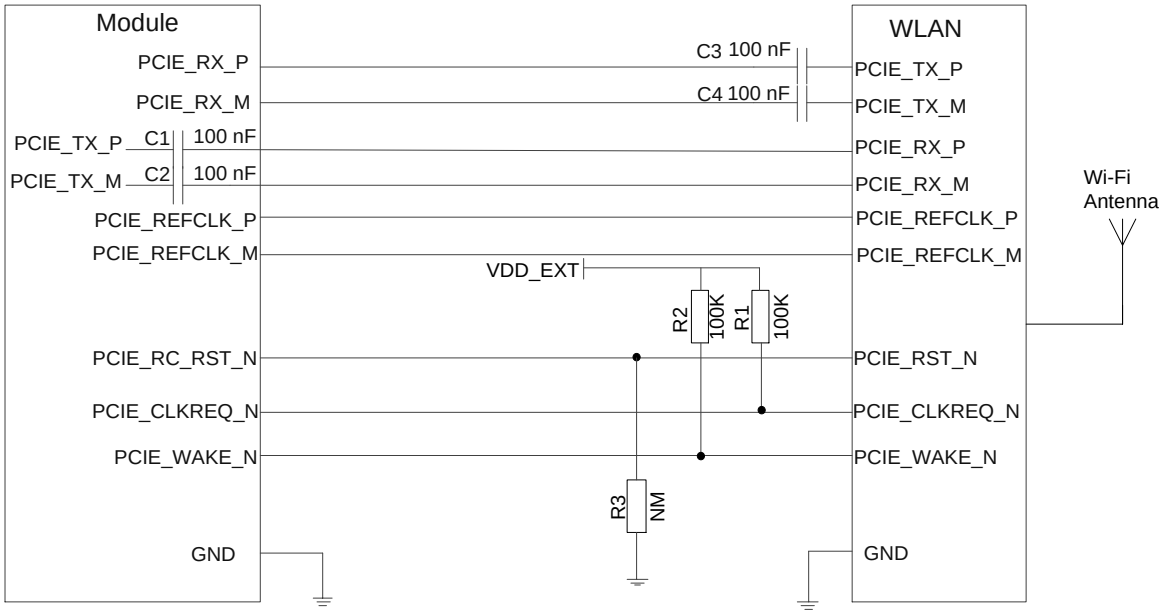


Figure 28: PCIe Interface Reference Circuit (RC Mode)

Table 27: PCIe Trace Length Inside the Module

Pin No.	Signal Trace	Length (mm)	Length Difference (mm)
179	PCIE_REFCLK_P	22.24	0.1
180	PCIE_REFCLK_M	22.14	
182	PCIE_TX_M	17.99	0.08
183	PCIE_TX_P	17.91	
185	PCIE_RX_M	13.91	0.07
186	PCIE_RX_P	13.98	

4.9. SDIO Interface*

The module provides one SDIO interface which supports SD 3.0 protocol and eMMC*.

Table 28: Pin Description of SDIO Interface*

Pin Name	Pin No.	I/O	Description	Comment
VDD_P2	135	PI	Power input for SDIO interface	If a SD card is used, connect VDD_P2 to SDIO_VDD. If an eMMC* is used or the SDIO interface* is unused, connect VDD_P2 to VDD_EXT.
SDIO_VDD	46	PO	**SD card application**: SDIO pull up power source **eMMC* application**: Keep it open as used for eMMC*	Cannot work as SD card power supply. SD card must be powered by an external power supply.
SDIO_DATA3	48	DIO	SDIO data bit 3	If unused, keep them open.
SDIO_DATA2	47	DIO	SDIO data bit 2	
SDIO_DATA1	50	DIO	SDIO data bit 1	
SDIO_DATA0	49	DIO	SDIO data bit 0	
SDIO_CMD	51	DIO	SDIO command	
SDIO_DET	52	DI	SD card detect	If unused, keep it open.
SDIO_CLK	53	DO	SDIO clock	If unused, keep it open.

The following figure shows an SDIO interface reference design.

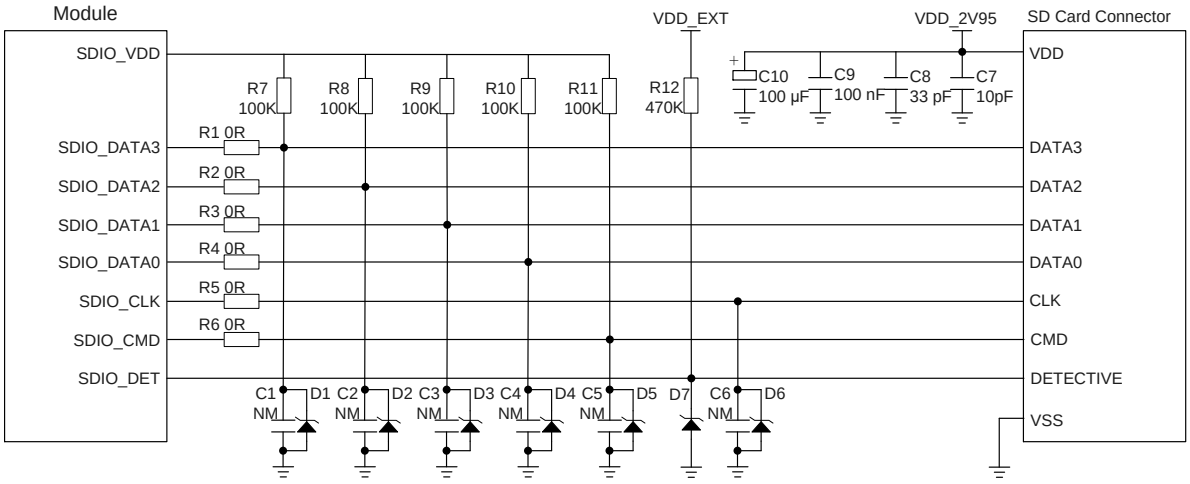


Figure 29: Reference Circuit of SD Card Application

Follow the principles below in the SD card circuit design:

- The voltage of SD power supply ranges from 2.7 V to 3.6 V and a sufficient current up to 0.8 A should be provided. As the maximum output current of SDIO_VDD is 50 mA which can only work as SDIO pull-up resistors, the SD card needs an external power supply.
- To avoid the jitter, resistors R7 to R11 are needed to pull up the SDIO signals to SDIO_VDD. The values of these resistors range from 10 kΩ to 100 kΩ and the preferred value is 100 kΩ.
- To improve signal quality, it is recommended to add resistors R1 to R6 of 0 Ω in series between the module and the SD card connector. The bypass capacitors C1 to C6 are reserved and not mounted by default. All resistors and bypass capacitors should be placed close to the module.
- For better ESD protection, it is recommended to add a TVS on each SD signal trace.
- It is important to route the SDIO signal traces with ground. The impedance of SDIO data trace is 50 Ω (± 10 %).
- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, and analog signals, as well as noisy signals such as clock signals and DC-DC signals.
- It is recommended to keep the trace length difference between SDIO_CLK and SDIO_DATA/SDIO_CMD within 1 mm and the total routing length less than 50 mm. The trace inside the module is 25 mm long in total, so the exterior trace should be less than 25 mm in total.
- Make sure the adjacent trace spacing is twice the trace width and the load capacitance of SDIO bus should be less than 15 pF.

4.10. Antenna Tuner Control Interfaces*

The module supports external antenna tuner control through the RFFE interface.

Table 29: Pin Description of RFFE Interfaces* for Antenna Tuner Control

Pin Name	Pin No.	I/O	Description	Comment
RFFE_CLK	71	DO	RFFE serial interface for external antenna tuner control.	If unused, keep them open.
RFFE_DATA	73	DIO		
VDD_RF	162	PO	Provide 2.85 V for external RF circuit.	

4.11. USB_BOOT Interface

The module provides one USB_BOOT pin. Pull up USB_BOOT to VDD_EXT before powering on the module, then the module will enter emergency download mode when powered on. In this mode, the module supports firmware upgrade over USB interface.

Table 30: Pin Description of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	140	DI	Force the module into emergency download mode	Active high. If unused, keep it open.

The following figure shows a reference circuit of USB_BOOT.

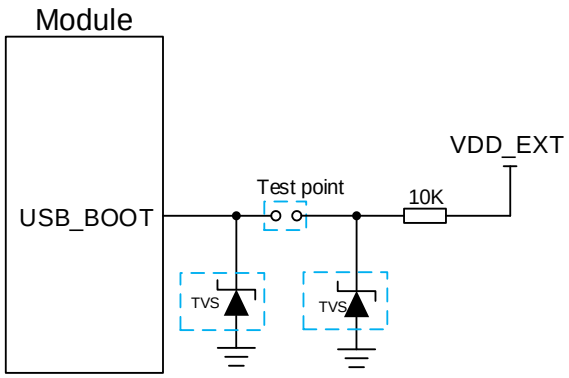


Figure 30: Reference Circuit of USB_BOOT

5 RF Specifications

The module provides one main antenna interface, one diversity antenna interface, and one GNSS antenna interface. The impedance of antenna port is 50 Ω.

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

Table 31: Pin Description of the Main/Diversity Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	107	AIO	Main antenna interface	50 Ω impedance
ANT1	127	AI	Diversity antenna interface	

Table 32: Frequency Bands

3GPP Band	Transmit	Receive	Unit
LTE B41	2496–2690	2496–2690	MHz
LTE B48	3550-3700	3550-3700	MHz

5.1.2. Tx Power

Table 33: Tx Power

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE B41/LTE B48	23 dBm ±2 dB	< -40 dBm

5.1.3. Rx Sensitivity

Table 34: Dual-Antenna Conducted Rx Sensitivity

Frequency Bands	Primary (dBm)	Diversity (dBm)	SIMO (dBm) [3]	3GPP (SIMO)
LTE-TDD B41 (10 MHz)	TBD	TBD	TBD	-94.3 dBm
LTE-TDD B48 (10 MHz)	TBD	TBD	TBD	-95 dBm

5.1.4. Reference Design

A reference design of ANT0, ANT1, interfaces is shown as below. It requires a π-type matching circuit for better RF performance. The π-type matching components (R1/C1/C2, R2/C3/C4) should be placed as close to the antennas as possible and are mounted according to the actual debugging. C1 to C4 are not mounted and a 0 Ω resistor is mounted on R1 to R2 respectively by default.

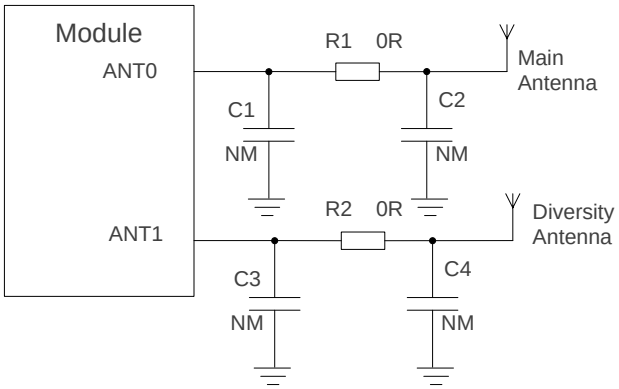


Figure 31: Reference Circuit of RF Antenna Interfaces

NOTE

Keep a proper distance between the main antenna and the diversity antenna to improve the receiving sensitivity.

3 SIMO is a smart antenna technology that uses a single antenna at the transmitter side and multiple (Primary + Diversity) antennas at the receiver side, which can improve Rx performance.

5.2. GNSS

5.2.1. Antenna Interface & Frequency Bands

The module includes a fully integrated global navigation satellite system solution that supports GPS, GLONASS, BDS, and Galileo. The module supports standard NMEA 0183 protocol, and outputs NMEA sentences at 1 Hz data update rate via USB interface by default.

By default, the module GNSS engine is off. It must be switched on via AT command. For more details, see ***document [3]***.

Table 35: Pin Description of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	119	AI	GNSS antenna interface	50 Ω impedance. If unused, keep it open.

Table 36: GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
Galileo	1575.42 ±2.046	MHz
BDS	1561.098 ±2.046	MHz

5.2.2. GNSS Performance

Table 37: GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity	Acquisition	Autonomous	TBD	dBm
	Reacquisition	Autonomous	TBD	dBm
	Tracking	Autonomous	TBD	dBm
TTFF	Cold start @ open sky	Autonomous	TBD	s

		XTRA enabled	TBD	s
	Warm start @ open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
	Hot start @ open sky	Autonomous	TBD	s
		XTRA enabled	TBD	s
Accuracy	CEP-50	Autonomous @ open sky	TBD	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix position successfully within 3 minutes after executing the cold start command.

5.2.3. Reference Design

A reference design of GNSS antenna is shown as below.

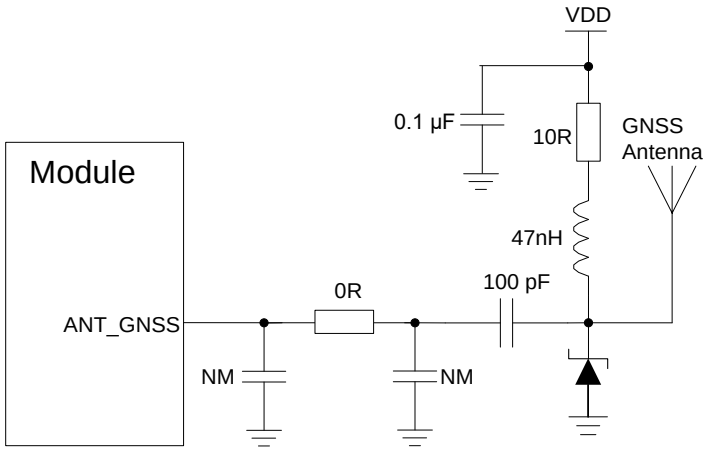


Figure 32: Reference Circuit of GNSS Antenna Interface

NOTE

1. An external LDO can be used to supply power according to the active antenna requirements.
2. The VDD circuit is unnecessary if the module is equipped with a passive antenna.

5.3. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

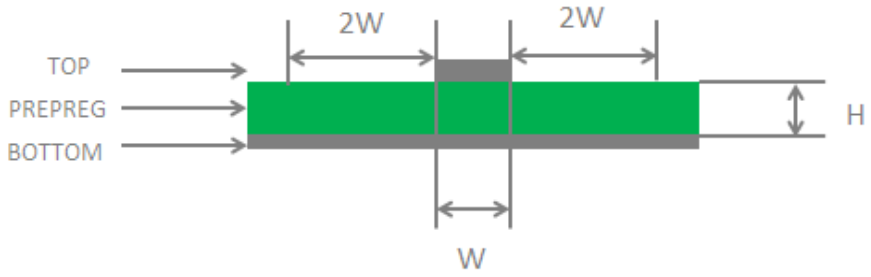


Figure 33: Microstrip Design on a 2-layer PCB

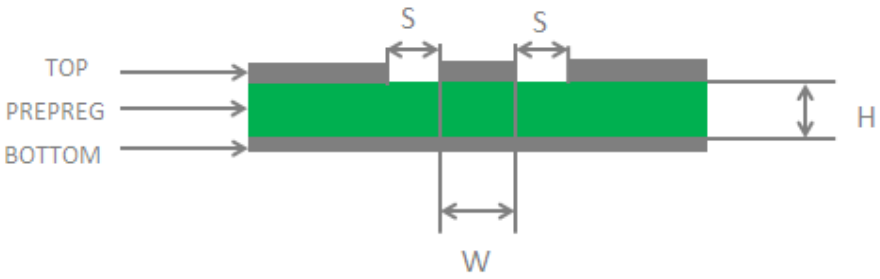


Figure 34: Coplanar Waveguide Design on a 2-layer PCB

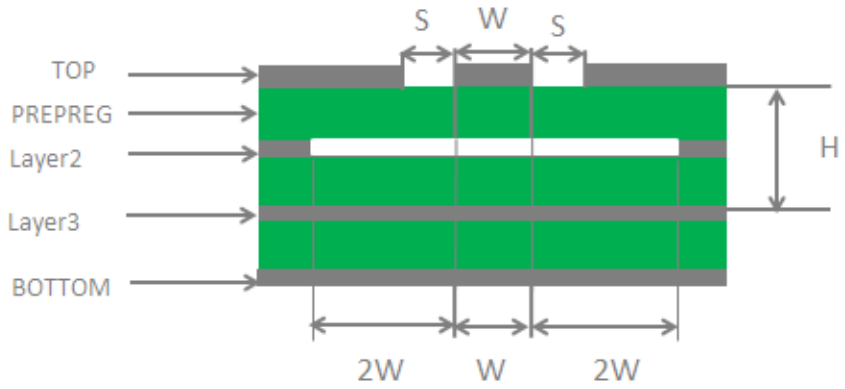


Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

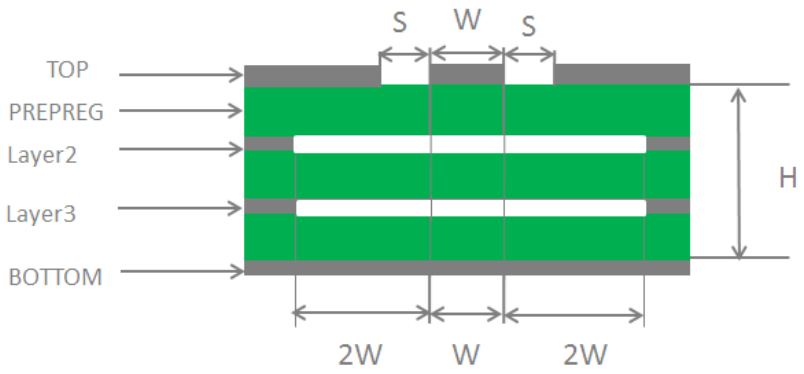


Figure 36: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be not less than twice the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [3]***.

5.4. Antenna Design Requirements

The following table shows the requirements on main antenna, diversity antenna and GNSS antenna.

Table 38: Antenna Design Requirements

Antenna Type	Requirements

GNSS	● Frequency range: 1559–1609 MHz ● Polarization: RHCP or linear ● VSWR: < 2 (Typ.) ● Passive antenna gain: > 0 dBi ● Active antenna noise figure: < 1.5 dB ● Active antenna gain: > 0 dBi ● Active antenna embedded LNA gain: < 17 dB
LTE	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Max input power: 50 W ● Input impedance: 50 Ω ● Cable insertion loss: **< 1 dB:** LB (<1 GHz) **< 1.5 dB:** MB (1–2.3 GHz) **< 2 dB:** HB (> 2.3 GHz)

5.5. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

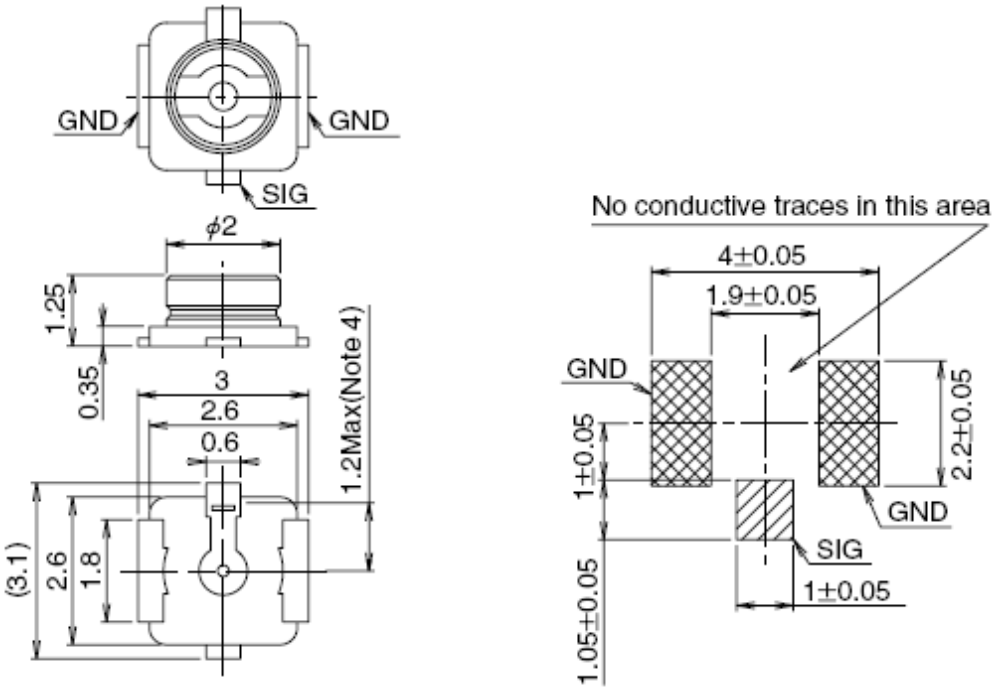


Figure 37: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

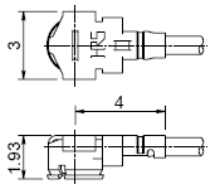
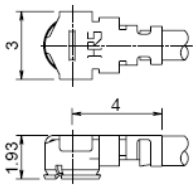
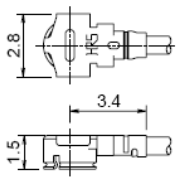
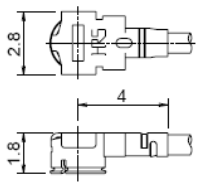
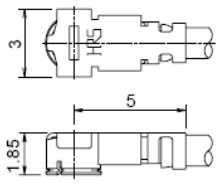
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 38: Specifications of Mated Plugs

The following figure describes the space factor of mating plugs.

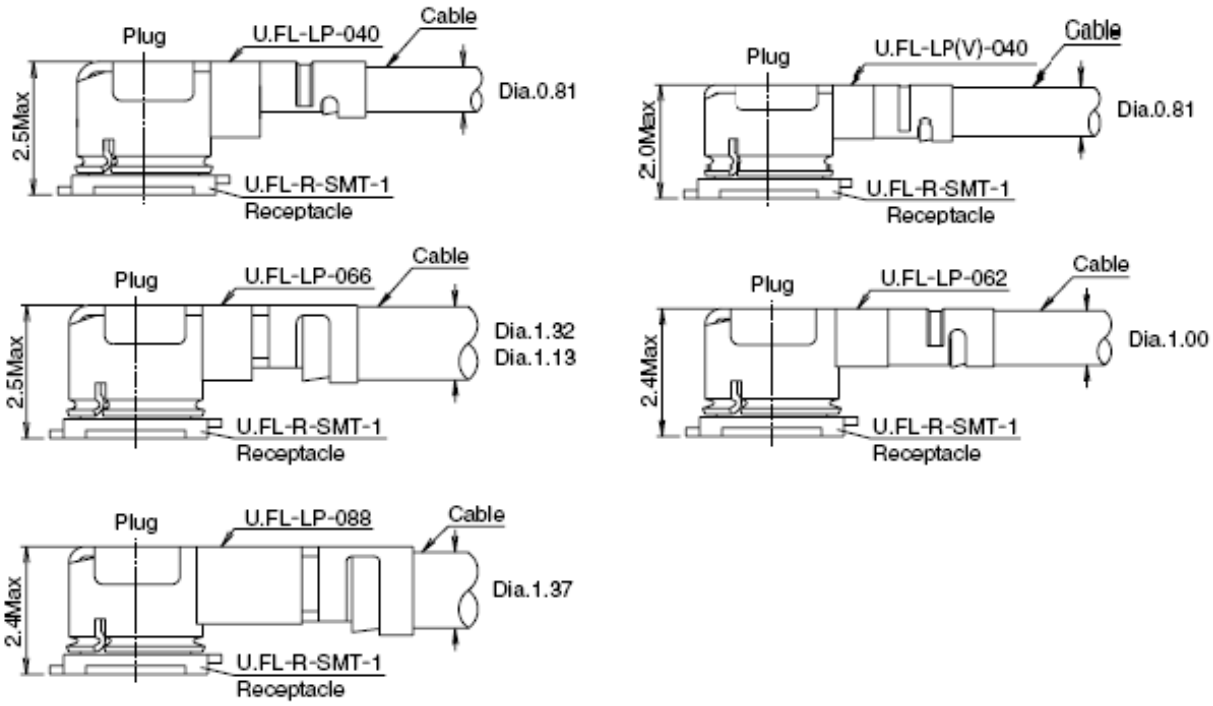


Figure 39: Space Factor of Mated Connectors (Unit: mm)

For more details, please visit http://www.hirose.com.

6 Electrical Characteristics and Reliability

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 39: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.0	A
Peak Current of VBAT_RF	-	1.2	A
Voltage at Digital Pins	-0.3	2.3	V
Voltage at ADC	-0.5	2.3	V

6.2. Power Supply Ratings

Table 40: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF	The actual input voltages must remain between the minimum and the maximum values.	3.3	3.8	4.4	V

6.3. Power Consumption

Table 41: Power Consumption

Description	Conditions	Typ.	Unit
OFF state	Power down	22	μA
Sleep state	-	TBD	mA
Idle state	TDD-LTE PF=64(USB disconnected)	12.43	mA
	TDD-LTE PF=64(USB2.0 connected)	18.91	mA
	LTE-TDD B41 CH41490 @ 22.48 dBm	391	mA
	LTE-TDD B48 CH55340 @ 22.61 dBm	331	mA
LTE data transfer (GNSS OFF)	LTE-TDD B41 CH41490 @ 22.48 dBm	391	mA
	LTE-TDD B48 CH55340 @ 22.61 dBm	331	mA

6.4. Digital I/O Characteristics

Table 42: VDD_EXT I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × VDD_EXT	VDD_EXT + 0.3	V
V_{IL}	Input low voltage	-0.3	0.3 × VDD_EXT	V
V_{OH}	Output high voltage	VDD_EXT - 0.45	VDD_EXT	V
V_{OL}	Output low voltage	0	0.45	V

Table 43: SDIO_VDD Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit

V_{IH}	Input high voltage	1.27	2.0	V
V_{IL}	Input low voltage	-0.3	0.58	V
V_{OH}	Output high voltage	1.4	-	V
V_{OL}	Output low voltage	-	0.45	V

Table 44: SDIO_VDD High-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.625 × SDIO_VDD	SDIO_VDD + 0.3	V
V_{IL}	Input low voltage	-0.3	0.25 × SDIO_VDD	V
V_{OH}	Output high voltage	0.75 × SDIO_VDD	-	V
V_{OL}	Output low voltage	-	0.125× SDIO_VDD	V

Table 45: VDD_USIM High/Low-voltage I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × VDD_USIM	VDD_USIM + 0.3	V
V_{IL}	Input low voltage	-0.3	0.2 × VDD_USIM	V
V_{OH}	Output high voltage	0.8 × VDD_USIM	-	V
V_{OL}	Output low voltage	-	0.4	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 46: Electrostatic Discharge Characteristics (Temperature: 25 °C, Humidity: 45 %)

Tested Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

6.6. Operation and Storage Temperatures

Table 47: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [4]	-30	+25	+75	ºC
Extended Operation Range [5]	-40	-	+85	ºC
Storage temperature range	-40	-	+90	ºC

6.7. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate, etc.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal ICs always work within in the recommended operating temperature.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as

4 To meet this operating temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this operation temperature range, the module can meet 3GPP specifications.
5 To meet this extended temperature range, additional thermal dissipation improvements are required, such as passive or active heatsink, heat-pipe, vapor chamber, cold-plate etc. Within this extended temperature range, the module remains the ability to establish and maintain functions like SMS, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as Pout, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

processor, power amplifier, and power supply.

- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the heatsink should be larger than the module to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

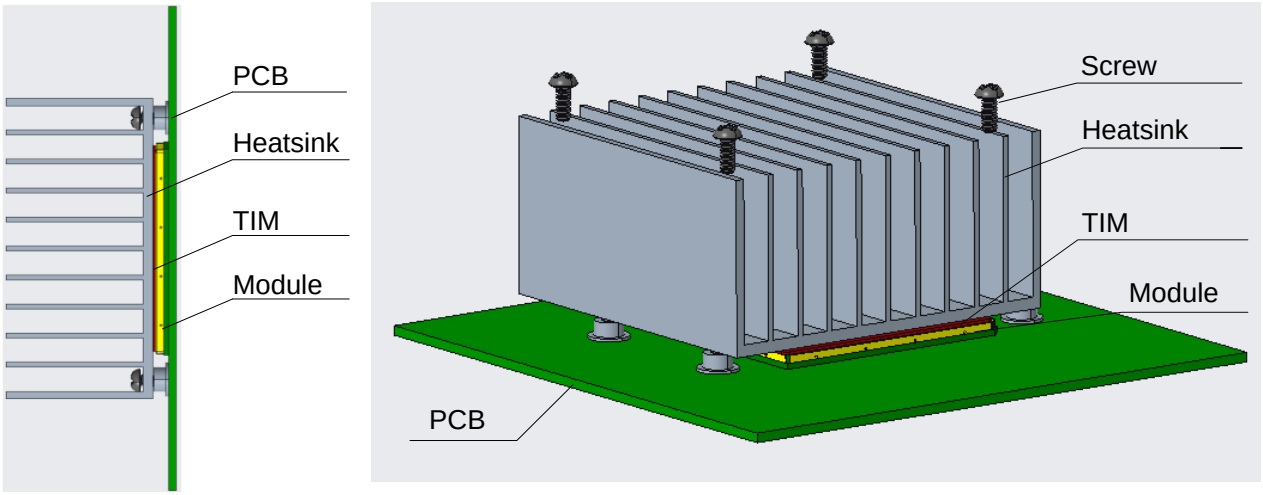


Figure 40: Placement and Fixing of the Heatsink

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

7.1. Mechanical Dimensions

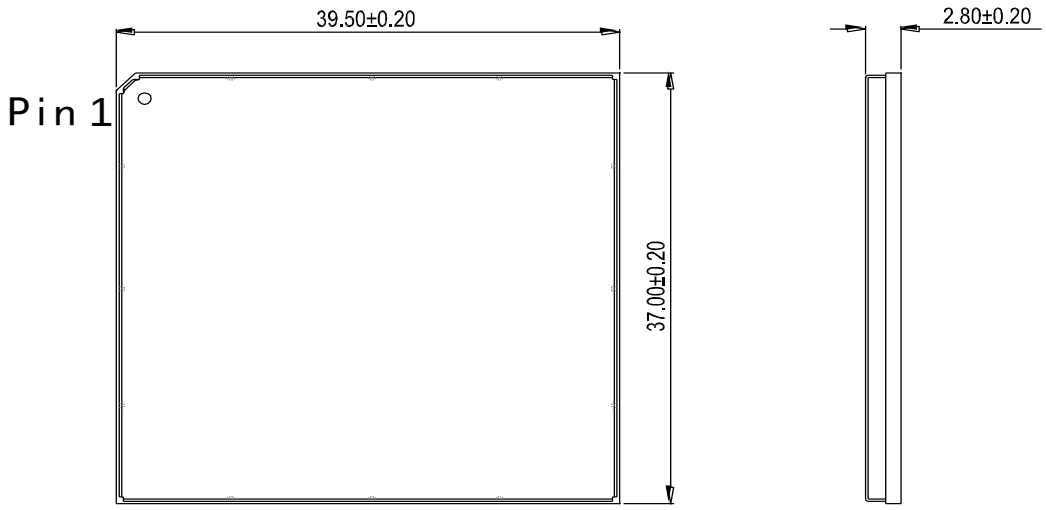


Figure 41: Module Top and Side Dimensions (Top View)

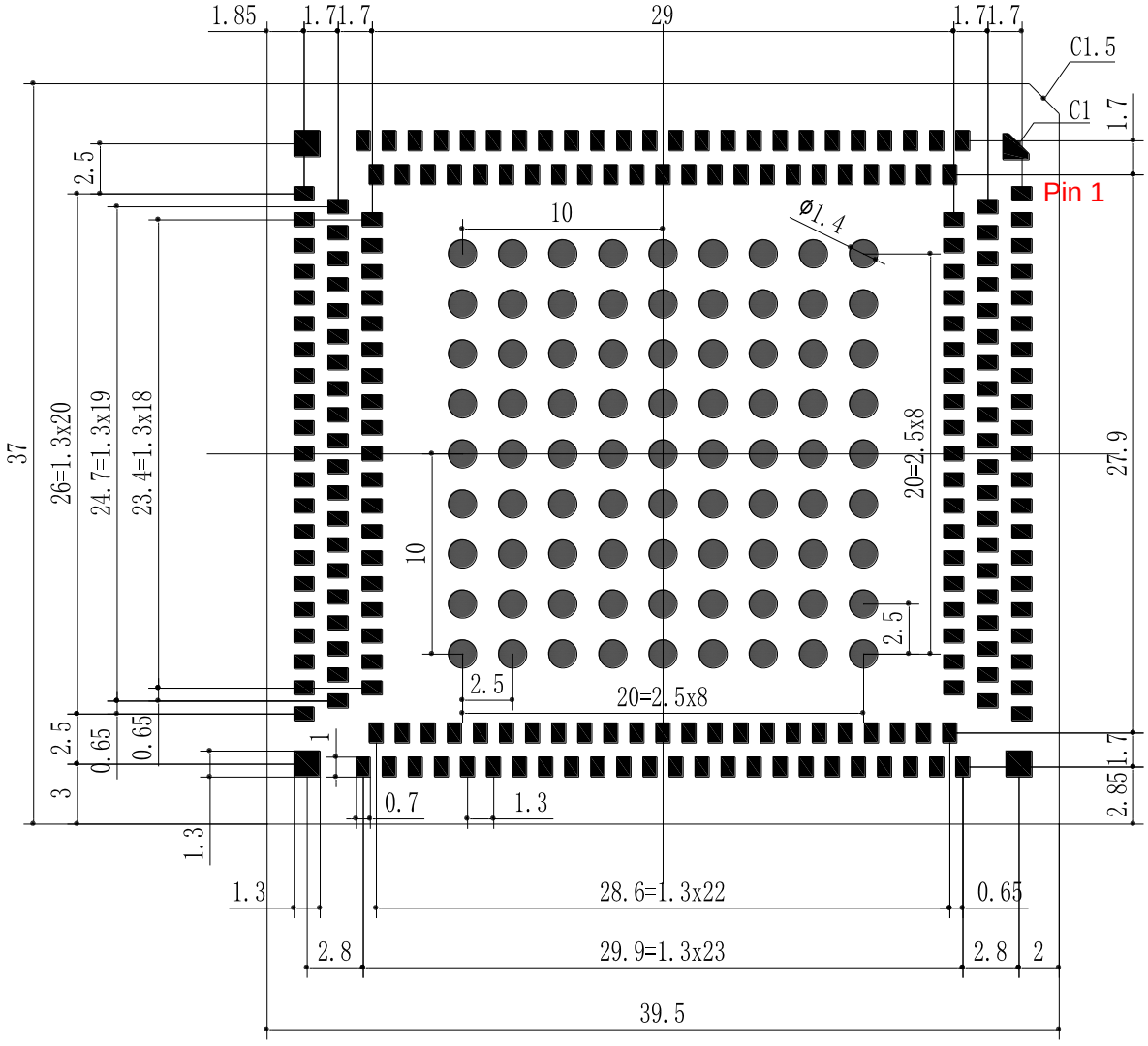


Figure 42: Module Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

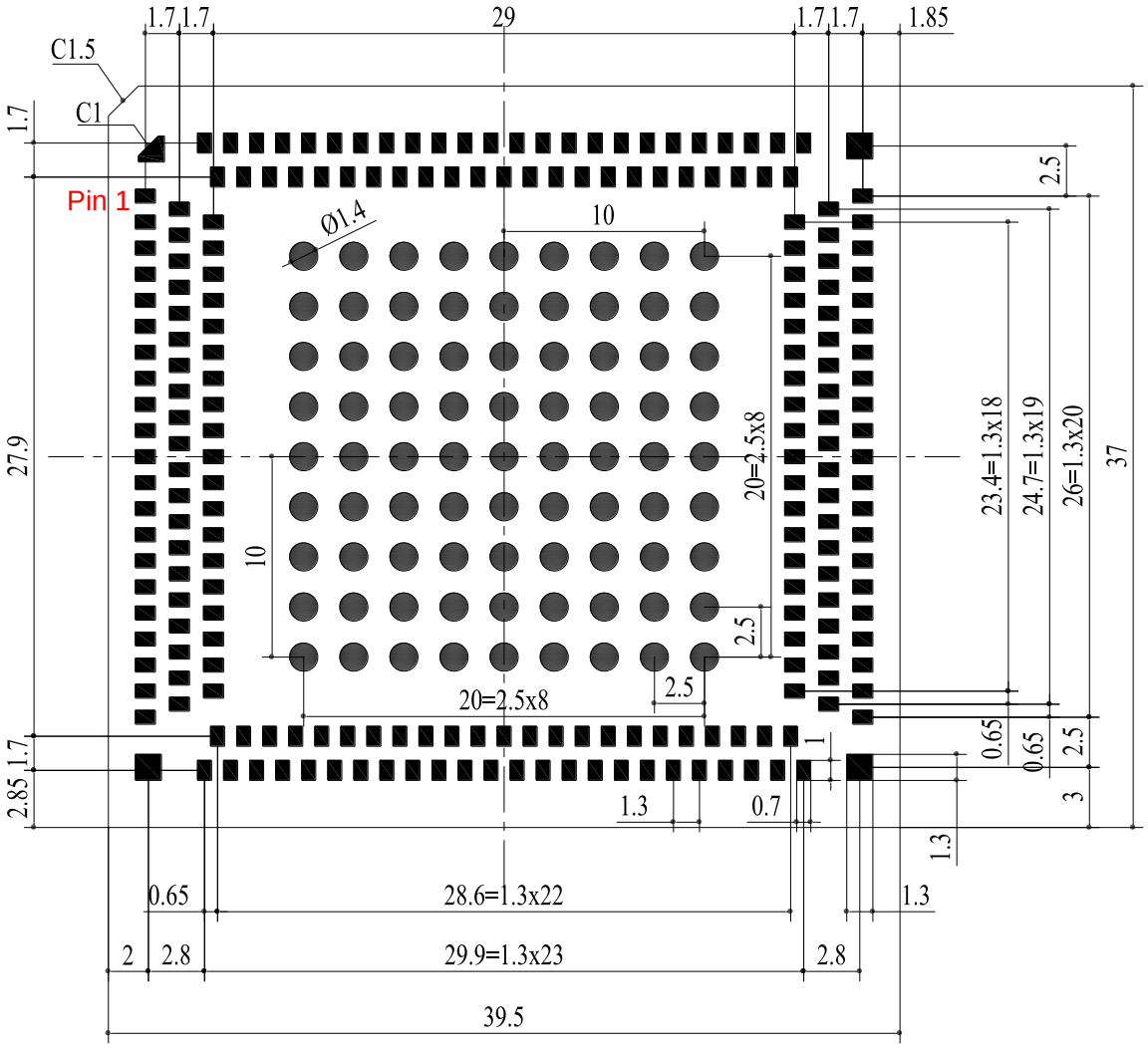


Figure 43: Recommended Footprint (Top View, Unit: mm)

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

7.3. Top and Bottom Views

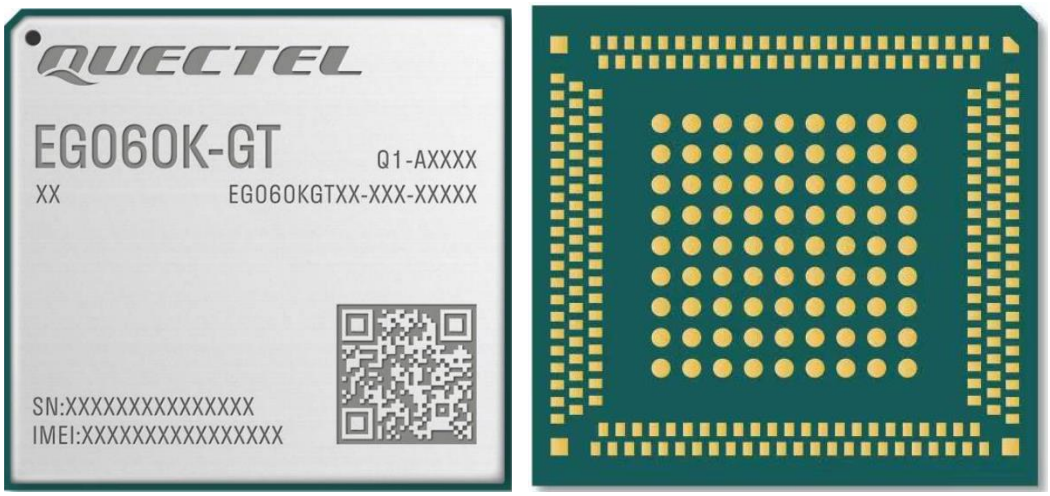


Figure 44: Top and Bottom Views

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, see the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [6] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

6 This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.13–0.18 mm. For more details, see ***document [4] .***

The peak reflow temperature ranges from 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

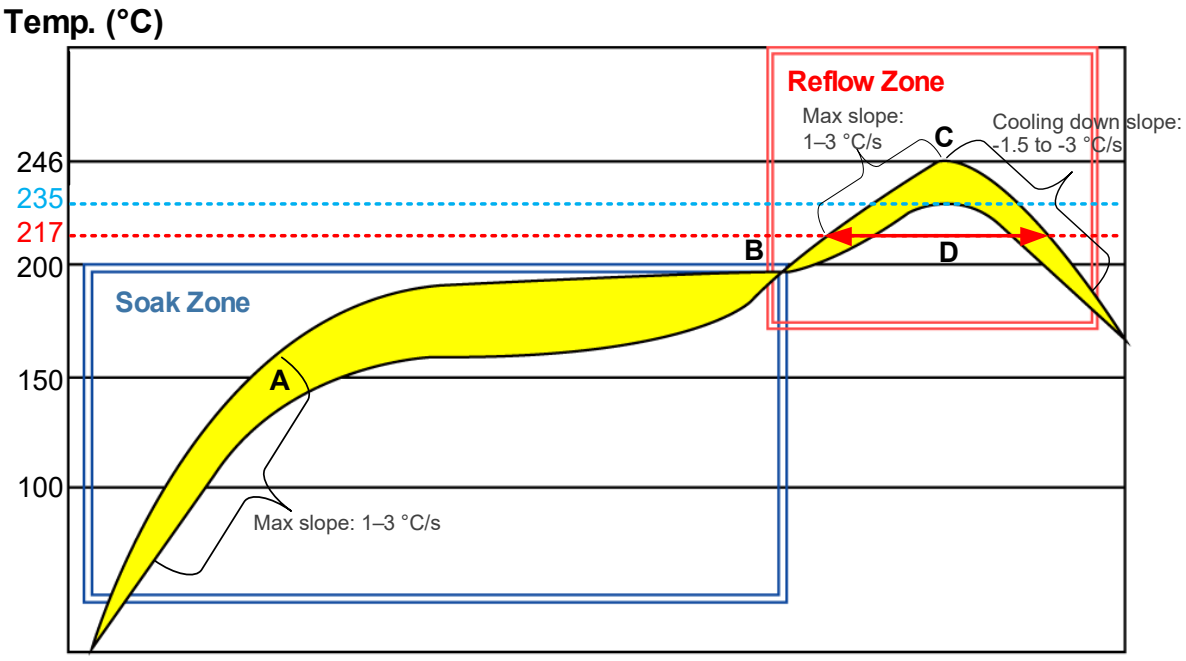


Figure 45: Reflow Soldering Thermal Profile

Table 48: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to -3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the complexity of the SMT process, please contact Quectel Technical Supports in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [4]***.

8.3. Packaging Specifications

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery. The module adopts injection tray packaging and details are as follow:

8.3.1. Carrier Tape

Dimension details are as follow:

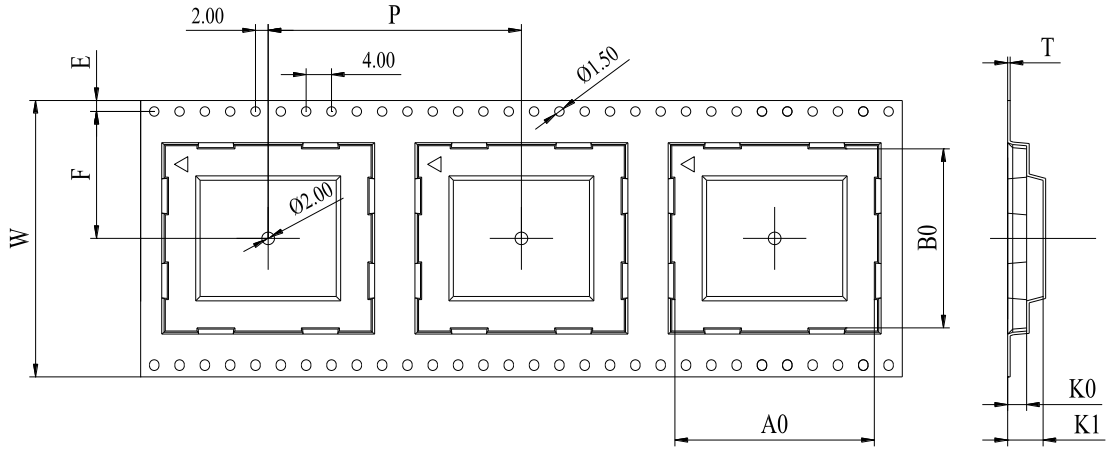


Figure 46: Carrier Tape Dimension Drawing

Table 49: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
56	48	0.35	40	37.5	3.9	5.3	26.2	1.75

8.3.2. Plastic Reel

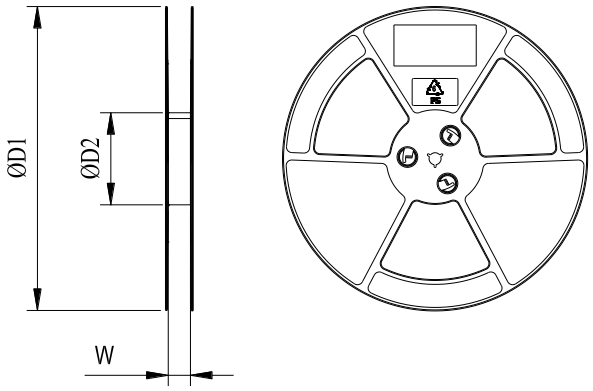
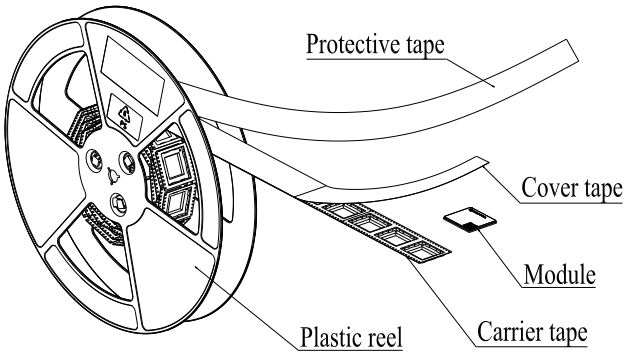


Figure 47: Plastic Reel Dimension Drawing

Table 50: Plastic Reel Dimension Table (Unit: mm)

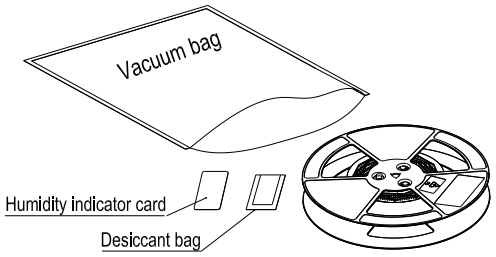
øD1	øD2	W
330	100	56.5

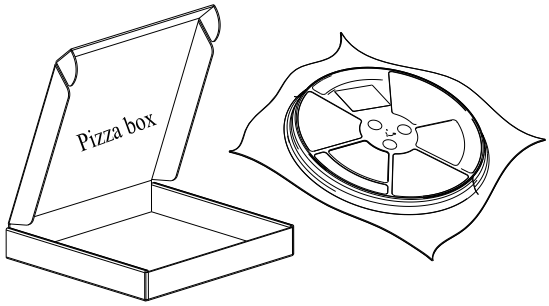
8.3.3. Packaging Process



Place the module into the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. One plastic reel can load 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 pizza boxes into 1 carton and seal it. One carton can pack 800 modules.

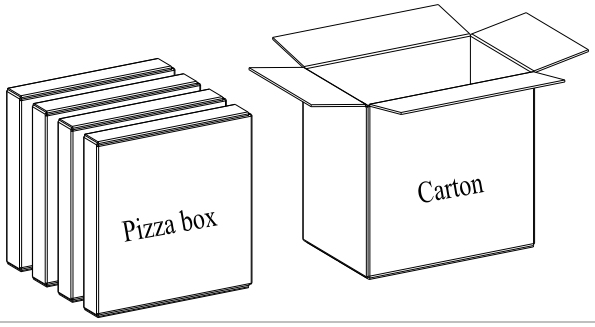


Figure 48: Packaging Process

9 Appendix References

Table 51: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_R2.0_User_Guide
[2] Quectel_EG06xK&Ex120K&EM060K_Series_AT_Commands_Manual
[3] Quectel_RF_Layout_Application_Note
[4] Quectel_Module_Secondary_SMT_Application_Note

Table 52: Term and Abbreviation

Abbreviation	Description
AMR	Adaptive Multi-Rate
AMR-WB	Adaptive Multi-Rate Wideband
APT	Average Power Tracking
BDS	BeiDou Navigation Satellite System
bps	bit(s) per second
CA	Carrier Aggregation
CHAP	Challenge-Handshake Authentication Protocol
CPE	Customer Premise Equipment
CS	Coding Scheme
CTS	Clear To Send
DFOTA	Delta Firmware Upgrade Over-the-Air

DL	Downlink
DRX	Discontinuous Reception
DTR	Data Terminal Ready
DTX	Discontinuous Transmission
eMMC	Embedded Multi Media Card
EFR	Enhanced Full Rate
ESD	Electrostatic Discharge
EVB	Evaluation Board
FR	Full Rate
FTP	File Transfer Protocol
GLONASS	Global Navigation Satellite System (Russia)
GMSK	Gaussian Minimum Shift Keying
GNSS	Global Navigation Satellite System
GPS	Global Positioning System
HR	Half Rate
HTTP	Hypertext Transfer Protocol
HTTPS	Hypertext Transfer Protocol Secure
IC	Integrated Circuit Chip
I/O	Input/Output
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low-Noise Amplifier
LPDDR2	Low Power Double Data Rate 2
LTE	Long-Term Evolution
LwM2M	Lightweight M2M

MAC	Medium Access Control
MBIM	Mobile Broadband Interface Model
MCP	Multiple Chip Package
ME	Mobile Equipment
MIMO	Multiple Input Multiple Output
MO	Mobile Originated
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MS	Mobile Station
MT	Mobile Terminated
M2M	Machine to Machine
NAND	NON-AND(gate)
NITZ	Network Identity and Time Zone/Network Informed Time Zone
PAP	Password Authentication Protocol
PC	Personal Computer
PCB	Printed Circuit Board
PDA	Personal Digital Assistant
PDU	Protocol Data Unit
PHY	Physical
PING	Packet Internet Groper
PMIC	power management IC
POS	Point of Sale
PPP	Point-to-Point Protocol
QAM	Quadrature Amplitude Modulation
QMI	Qualcomm MSM (Mobile Station Modem) Interface/Qualcomm Message Interface
QPSK	Quadrature Phase Shift Keying

RF	Radio Frequency
RHCP	Right Hand Circular Polarization
RST	Reset
Rx	Receive
SD Card	Secure Digital Card
SDRAM	synchronous dynamic random-access memory
SIMO	Single Input Multiple Output
SLIC	Subscriber Line Interface Circuit
SMD	Surface Mounted Devices
SMS	Short Message Service
TCP	Transmission Control Protocol
TDD	Time Division Duplex
Tx	Transmit
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
USIM	Universal Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-Level Input Voltage
V_{IH}min	Minimum High-Level Input Voltage
V_{IL}max	Maximum Low-Level input Voltage
V_{OH}max	Maximum High-level Output Voltage

V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio
WLAN	Wireless Local Area Networks